GE Vernova

MiCOM P40 Agile

5th Generation
P84

Technical Manual
Single and Dual CB Feeder and Autoreclose IED

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Firmware Version: AB
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The content of this document has been developed to provide guidance to properly install, configure and maintain this product for its intended applications. This guidance is not intended to cover every possible contingency that may arise during commissioning, operation, service, or maintenance activities. Should you encounter any circumstances not clearly addressed in this document, contact your local GE Vernova service site.

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Contents

CHAPTER 1

INTRODUCTION

1.1 CHAPTER OVERVIEW

This chapter provides some general information about the technical manual and an introduction to the device(s) described in this technical manual.

This chapter contains the following sections:

1.2 FOREWORD

This technical manual provides a functional and technical description of GE Vernova's 5th Generation transformer protection IED, as well as a comprehensive set of instructions for using the device. The level at which this manual is written assumes that you are already familiar with protection engineering and have experience in this discipline. The description of principles and theory is limited to that which is necessary to understand the product. For further details on general protection engineering theory, we refer you to GE Vernova's publication, Protection and Automation Application Guide, which is available online or from our Contact Centre.

We have attempted to make this manual as accurate, comprehensive and user-friendly as possible. However we cannot guarantee that it is free from errors. Nor can we state that it cannot be improved. We would therefore be very pleased to hear from you if you discover any errors, or have any suggestions for improvement. Our policy is to provide the information necessary to help you safely specify, engineer, install, commission, maintain, and eventually dispose of this product. We consider that this manual provides the necessary information, but if you consider that more details are needed, please contact us.

All feedback should be sent to our contact centre via:

contact.centre@ge.com

1.2.1 TARGET AUDIENCE

This manual is aimed towards all professionals charged with installing, commissioning, maintaining, troubleshooting, or operating any of the products within the specified product range. This includes installation and commissioning personnel as well as engineers who will be responsible for operating the product.

The level at which this manual is written assumes that installation and commissioning engineers have knowledge of handling electronic equipment. Also, system and protection engineers have a thorough knowledge of protection systems and associated equipment.

1.2.2 TYPOGRAPHICAL CONVENTIONS

The following typographical conventions are used throughout this manual.

- The names for special keys appear in capital letters.
  For example: ENTER
- When describing software applications, menu items, buttons, labels etc as they appear on the screen are written in bold type.
  For example: Select **Save** from the file menu.
- Filenames and paths use the courier font
  For example: `Example\File.text`
- Special terminology is written with leading capitals
  For example: Sensitive Earth Fault
- If reference is made to the IED's internal settings and signals database, the menu group heading (column) text is written in upper case italics
  For example: The *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the setting cells and DDB signals are written in bold italics
  For example: The ***Language*** cell in the *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the value of a cell's content is written in the Courier font
  For example: The ***Language*** cell in the *SYSTEM DATA* column contains the value `English`

1.2.3 NOMENCLATURE

Due to the technical nature of this manual, many special terms, abbreviations and acronyms are used throughout the manual. Some of these terms are well-known industry-specific terms while others may be special product-specific terms used by GE Vernova. The first instance of any acronym or term used in a particular chapter is explained. In addition, a separate glossary is available on the GE Vernova website, or from the GE Vernova contact centre.

We would like to highlight the following changes of nomenclature however:

- The word 'relay' is no longer used to describe the device itself. Instead, the device is referred to as the 'IED' (Intelligent Electronic Device), the 'device', or the 'product'. The word 'relay' is used purely to describe the electromechanical components within the device, i.e. the output relays.
- British English is used throughout this manual.
- The British term 'Earth' is used in favour of the American term 'Ground'.

1.2.4 COMPLIANCE

The device has undergone a range of extensive testing and certification processes to ensure and prove compatibility with all target markets. A detailed description of these criteria can be found in the Technical Specifications chapter.

1.3 PRODUCT SCOPE

The P84 is a multifunctional line terminal IED for control and protection of feeder bays, which is suitable for single and dual circuit breaker applications. The P84 is used in applications such as breaker-and-a-half, or ring bus topologies, where two circuit breakers feed each line. This device can also be used for 4-shot phase segregated autoreclose protection, and a range of standard current, voltage, power and frequency backup protection applications.

The P84 can be ordered in 40/60/80TE cases with several different digital input/output options also offered.

The P84 is available with conventional 1A/5A CT inputs and 100/120V VT inputs or with a IEC 61850-9-2LE redundant Ethernet process bus input for sampled analogue values. Unlike a conventional IED, a device with an IEC 61850-9-2 interface, or Sampled Value (SV) device accepts current and voltage measurement inputs, which have already been digitized in accordance with the IEC 61850-9-2LE standard. The IEC 61850-9-2LE version of the P84 IED accepts sampled analogue values from merging units. It does not accept analogue values directly and therefore does not have any current or voltage transformers. This provides a number of advantages over conventional devices, which are discussed throughout this technical manual.

The differences between the model variants for 1 and 2 CBs are summarised in the table below:

Feature	P841 1CB	P841 2CB
Number of CT Inputs	5	8
Number of VT inputs	4	5
Opto-coupled digital inputs	8-40	8-24
Standard relay output contacts	7-43	7-32
High speed high break output contacts	4-8	4-8

The 5 VTs in this model allow flexible configuration options, where one can be used to measure the residual voltage if required. To do this, you must first set all relevant residual voltage input settings to `measured`, then the ***VT2 Selection*** setting to `Broken Delta`.

1.3.1 PRODUCT VERSIONS

Products detailed in this manual belong to the 5th Generation of P40 protection devices.

The P84 relay software is based on 4th Generation software (SW):

- P841 - 80/81/82SW

5th Generation P84 models cover the digital input and output options of 4th Generation P841 single and dual breaker versions.

An IEC 61850-9-2LE option is included for P84 single and dual breaker models, which was previously only available on the P841 2CB models. P84 models are available in 40TE/60TE/80TE case sizes, whereas previous models only offered 60/80TE.

The rear communication port protocol is selectable in the settings, so there is no Cortec option. For 4th Generation this was required as an order option.

1.3.2 ORDERING OPTIONS

All current models and variants for this product are defined in an interactive spreadsheet called the Cortec. This is available on the company website.

Alternatively, you can obtain it via the Contact Centre at:

contact.centre@ge.com

A copy of the Cortec is also supplied as a static table in the Appendices of this document. However, it should only be used for guidance as it provides a snapshot of the interactive data taken at the time of publication.

1.4 FEATURES AND FUNCTIONS

1.4.1 PROTECTION FUNCTIONS

Feature	IEC 61850	ANSI
Tripping mode (1 & 3 pole)	PTRC	
ABC and ACB phase rotation		
Phase overcurrent, with optional directionality (4 stages)	OcpPTOC/RDIR	50/51/67
Earth/Ground overcurrent stages, with optional directionality (4 stages)	EfdPTOC/RDIR	50N/51N/ 67N
Sensitive Earth Fault (SEF) (4 stages)	SenPTOC/RDIR	50N/51N/67N
High impedance restricted earth fault (REF)	SenRefPDIF	64
Negative sequence overcurrent stages, with optional directionality (4 stages)	NgcPTOC/RDIR	67/46
Broken conductor, used to detect open circuit faults		46
Thermal overload protection	ThmPTTR	49
Phase directional power (4 stages)	PdpPDOP/PDUP	32
Undervoltage protection (2 stages)	VtpPhsPTUV	27
Overvoltage protection (2 stages)	VtpPhsPTOV	59
Remote overvoltage protection (2 stages)	VtpCmpPTOV	59R
Residual voltage protection (2 stages)	VtpResPTOV	59N
Underfrequency protection (4 stages)	FrqPTUF	81
Overfrequency protection (2 stages)	FrqPTOF	81
Rate of change of frequency protection (4 stages)	DfpPFRC	81
High speed breaker fail suitable for re-tripping and back-tripping (2 stages)	RBRF	50BF
Current Transformer supervision		46
Voltage Transformer supervision		47/27
Auto-reclose (4 shots)	RREC	79
Check synchronisation (2 stages)	RSYN	25

1.4.2 CONTROL FUNCTIONS

Feature	IEC 61850	ANSI
Watchdog contacts		
Read-only mode		
Function keys	FnkGGIO	
Programmable LEDs	LedGGIO	
Programmable hotkeys		
Programmable allocation of digital inputs and outputs		
Fully customizable menu texts		
Circuit breaker control, status & condition monitoring	XCBR	52
CT supervision		
VT supervision		
Trip circuit and coil supervision		

Feature	IEC 61850	ANSI
Control inputs	PloGGIO1	
Power-up diagnostics and continuous self-monitoring		
Dual rated 1A and 5A CT inputs		
Alternative setting groups (4)		
Graphical programmable scheme logic (PSL)		
Fault locator	RFLO	

1.4.3 MEASUREMENT FUNCTIONS

Measurement Function	IEC 61850	ANSI
Measurement of all instantaneous & integrated values (Exact range of measurements depend on the device model)		MET
Disturbance recorder for waveform capture – specified in samples per cycle	RDRE	DFR
Fault Records		
Maintenance Records		
Event Records/Event logging		Event records
Time Stamping of Opto-inputs	Yes	Yes

1.4.4 COMMUNICATION FUNCTIONS

Feature	ANSI
NERC compliant cyber-security	
Front RS232 serial communication port for configuration	16S
Rear serial RS485 communication port for SCADA control	16S
2 Additional rear serial communication ports for SCADA control and teleprotection (fibre and copper) (optional)	16S
Ethernet communication (optional)	16E
Redundant Ethernet communication (optional)	16E
Rear Ethernet engineering port for configuration	16E
Courier Protocol	16S
IEC 61850 edition 1 or edition 2 (optional)	16E
IEC 60870-5-103 (optional)	16S
DNP3.0 over serial link (optional)	16S
SNMP	16E
IRIG-B time synchronisation (optional)	CLK
IEEE 1588 PTP (Edition 2 devices only)	

1.5 LOGIC DIAGRAMS

This technical manual contains many logic diagrams, which should help to explain the functionality of the device. Although this manual has been designed to be as specific as possible to the chosen product, it may contain diagrams, which have elements applicable to other products. If this is the case, a qualifying note will accompany the relevant part.

The logic diagrams follow a convention for the elements used, using defined colours and shapes. A key to this convention is provided below. We recommend viewing the logic diagrams in colour rather than in black and white. The electronic version of the technical manual is in colour, but the printed version may not be. If you need coloured diagrams, they can be provided on request by calling the contact centre and quoting the diagram number.

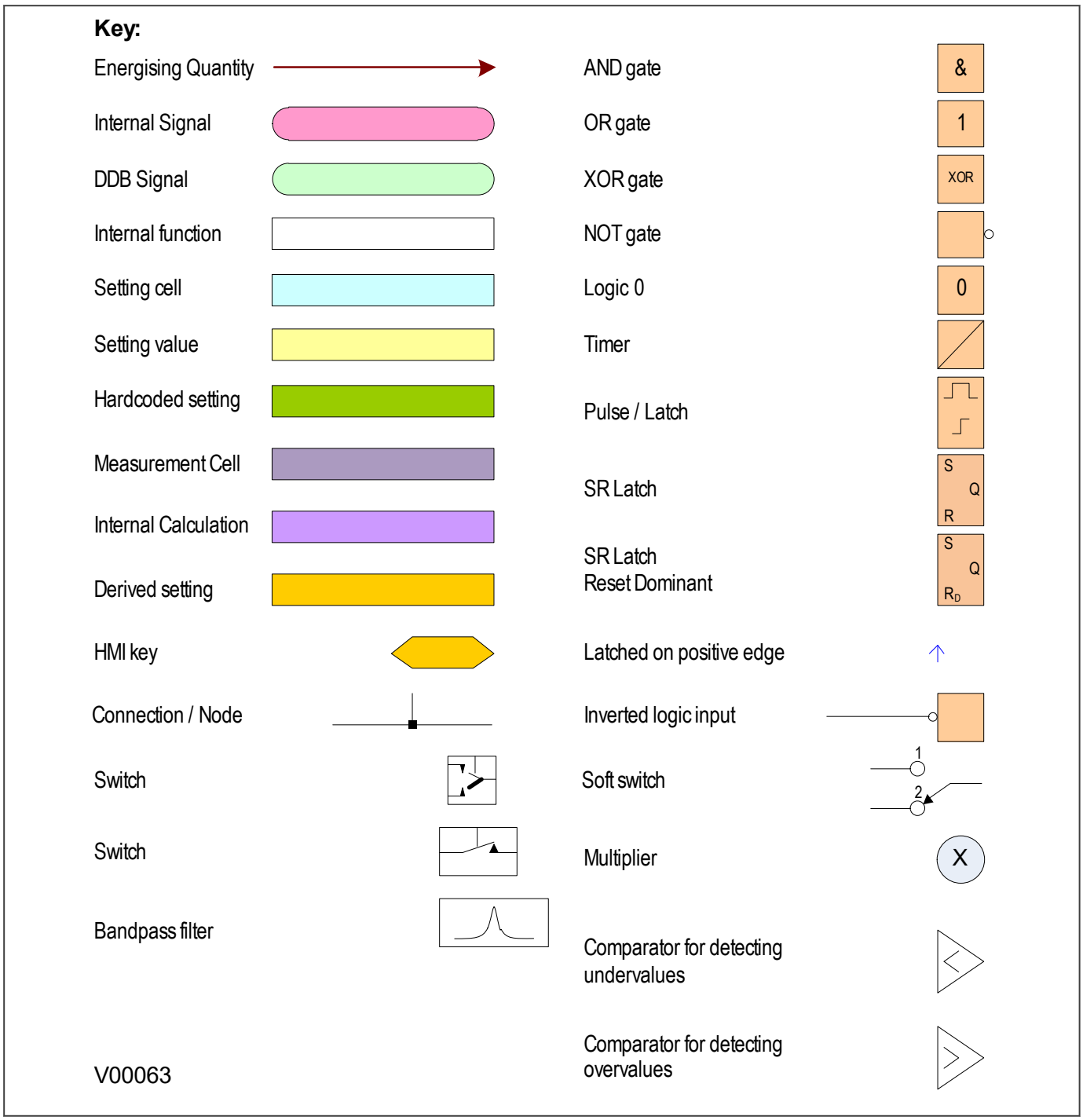


Figure 1: Key to logic diagrams

1.6 FUNCTIONAL OVERVIEW

This diagram is applicable to P84 product models. Use the key on the diagram to determine the features relevant to the product described in this technical manual.

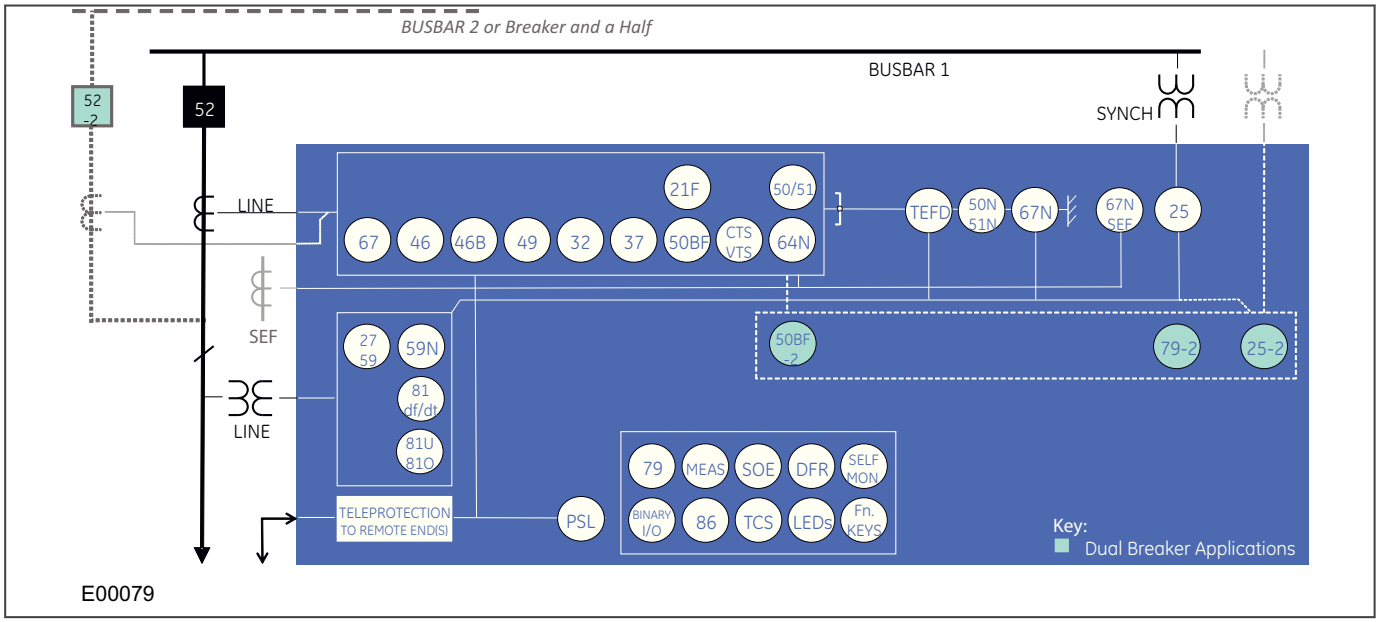


Figure 2: Functional Overview

The following table lists the P84 ANSI numbers and the corresponding function descriptions:

Device Number	Function
25	Check Sychronising
27	Phase and Line Undervoltage
32	Directional Power Protection
37	Undercurrent
46	Negative Sequence Overcurrent
49	Thermal Overload
50	Phase Definite Time Overcurrent
51	Phase Inverse-Time Overcurrent
52	Circuit Breaker Control
59	Phase and Line Overvoltage
67	Directional Phase Overcurrent
79	Autoreclose/Adaptive Autoreclose
86	Latching/Lockout Contacts
21FL	Fault Locator
46BC	Broken Conductor
50BF	CB Failure
50N	Earth Fault Definite Time Overcurrent
51N	Neutral/Ground IDMT Overcurrent
59N	Neutral Voltage Displacement
64N	Restricted Earth Fault
67N	Directional Neutral/Ground Overcurrent

Device Number	Function
81df/dt	Rate of Change of Frequency
81O	Overfrequency
81U	Underfrequency
CTS	CT Supervision
PSL	Programmable Logic
SEF	Sensitive Earth Fault
TEFD	Transient Earth Fault Detection
TCS	Trip Circuit Supervision
VTS	VT Supervision

CHAPTER 2

SAFETY INFORMATION

2.1 CHAPTER OVERVIEW

This chapter provides information about the safe handling of the equipment. The equipment must be properly installed and handled in order to maintain it in a safe condition and to keep personnel safe at all times. You must be familiar with information contained in this chapter before unpacking, installing, commissioning, or servicing the equipment.

This chapter contains the following sections:

2.2 HEALTH AND SAFETY

Personnel associated with the equipment must be familiar with the contents of this Safety Information.

When electrical equipment is in operation, dangerous voltages are present in certain parts of the equipment. Improper use of the equipment and failure to observe warning notices will endanger personnel.

Only qualified personnel may work on or operate the equipment. Qualified personnel are individuals who are:

- familiar with the installation, commissioning, and operation of the equipment and the system to which it is being connected.
- familiar with accepted safety engineering practises and are authorised to energise and de-energise equipment in the correct manner.
- trained in the care and use of safety apparatus in accordance with safety engineering practises
- trained in emergency procedures (first aid).

The documentation provides instructions for installing, commissioning and operating the equipment. It cannot, however cover all conceivable circumstances. In the event of questions or problems, do not take any action without proper authorisation. Please contact your local sales office and request the necessary information.

2.3 SYMBOLS

Throughout this manual you will come across the following symbols. You will also see these symbols on parts of the equipment.

Caution:
Refer to equipment documentation. Failure to do so could result in damage to the equipment

Warning:
Risk of electric shock

Warning:
Risk of damage to eyesight

Earth terminal. *Note: This symbol may also be used for a protective conductor (earth) terminal if that terminal is part of a terminal block or sub-assembly.*

Protective conductor (earth) terminal

Instructions on disposal requirements

Note:
The term 'Earth' used in this manual is the direct equivalent of the North American term 'Ground'.

2.4 INSTALLATION, COMMISSIONING AND SERVICING

2.4.1 LIFTING HAZARDS

Many injuries are caused by:

- Lifting heavy objects
- Lifting things incorrectly
- Pushing or pulling heavy objects
- Using the same muscles repetitively

Plan carefully, identify any possible hazards and determine how best to move the product. Look at other ways of moving the load to avoid manual handling. Use the correct lifting techniques and Personal Protective Equipment (PPE) to reduce the risk of injury.

2.4.2 ELECTRICAL HAZARDS

Caution:
All personnel involved in installing, commissioning, or servicing this equipment must be familiar with the correct working procedures.

Caution:
Consult the equipment documentation before installing, commissioning, or servicing the equipment.

Caution:
Always use the equipment as specified. Failure to do so will jeopardise the protection provided by the equipment.

Warning:
Removal of equipment panels or covers may expose hazardous live parts. Do not touch until the electrical power is removed. Take care when there is unlocked access to the rear of the equipment.

Warning:
Isolate the equipment before working on the terminal strips.

Warning:
Use a suitable protective barrier for areas with restricted space, where there is a risk of electric shock due to exposed terminals.

Caution:
Disconnect power before disassembling. Disassembly of the equipment may expose sensitive electronic circuitry. Take suitable precautions against electrostatic voltage discharge (ESD) to avoid damage to the equipment.

Warning:
NEVER look into optical fibres or optical output connections. Always use optical power meters to determine operation or signal level.

Warning:
Testing may leave capacitors charged to dangerous voltage levels. Discharge capacitors by reducing test voltages to zero before disconnecting test leads.

Caution:
Operate the equipment within the specified electrical and environmental limits.

Caution:
Before cleaning the equipment, ensure that no connections are energised. Use a lint free cloth dampened with clean water.

Note:
Contact fingers of test plugs are normally protected by petroleum jelly, which should not be removed.

2.4.3 UL/CSA/CUL REQUIREMENTS

The information in this section is applicable only to equipment carrying UL/CSA/CUL markings.

Caution:
Equipment intended for rack or panel mounting is for use on a flat surface of a Type 1 enclosure, as defined by Underwriters Laboratories (UL).

Caution:
To maintain compliance with UL and CSA/CUL, install the equipment using UL/CSA-recognised parts for: cables, protective fuses, fuse holders and circuit breakers, insulation crimp terminals, and replacement internal batteries.

2.4.4 FUSING REQUIREMENTS

Caution:
Where UL/CSA listing of the equipment is required for external fuse protection, a UL or CSA Listed fuse must be used for the auxiliary supply. The listed protective fuse type is: Class J time delay fuse, with a maximum current rating of 15 A and a minimum DC rating of 250 V dc (for example type AJT15).

Caution:
Where UL/CSA listing of the equipment is not required, a high rupture capacity (HRC) fuse type with a maximum current rating of 16 Amps and a minimum dc rating of 250 V dc may be used for the auxiliary supply (for example Red Spot type NIT or TIA).
For P50 models, use a 1A maximum T-type fuse.
For P60 models, use a 4A maximum T-type fuse.

Caution:
Digital input circuits should be protected by a high rupture capacity NIT or TIA fuse with maximum rating of 16 A. for safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.

Caution:
CTs must NOT be fused since open circuiting them may produce lethal hazardous voltages

2.4.5 EQUIPMENT CONNECTIONS

Warning:
Terminals exposed during installation, commissioning and maintenance may present a hazardous voltage unless the equipment is electrically isolated.

Caution:
Tighten M4 clamping screws of heavy duty terminal block connectors to a nominal torque of 1.3 Nm.
Tighten captive screws of terminal blocks to 0.5 Nm minimum and 0.6 Nm maximum.

Caution:
Always use insulated crimp terminations for voltage and current connections.

Caution:
Always use the correct crimp terminal and tool according to the wire size.

Caution:
Watchdog (self-monitoring) contacts are provided to indicate the health of the device on some products. We strongly recommend that you hard wire these contacts into the substation's automation system, for alarm purposes.

2.4.6 PROTECTION CLASS 1 EQUIPMENT REQUIREMENTS

Caution:
Earth the equipment with the supplied PCT (Protective Conductor Terminal).

Caution:
Do not remove the PCT.

Caution:
The PCT is sometimes used to terminate cable screens. Always check the PCT's integrity after adding or removing such earth connections.

Caution:
Use a locknut or similar mechanism to ensure the integrity of stud-connected PCTs.

Caution:
The recommended minimum PCT wire size is 2.5 mm² for countries whose mains supply is 230 V (e.g. Europe) and 3.3 mm² for countries whose mains supply is 110 V (e.g. North America). This may be superseded by local or country wiring regulations. For P60 products, the recommended minimum PCT wire size is 6 mm². See product documentation for details.

Caution:
The PCT connection must have low-inductance and be as short as possible.

Caution:
All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should be earthed, or connected to a common grouped potential.

2.4.7 PRE-ENERGISATION CHECKLIST

Caution:
Check voltage rating/polarity (rating label/equipment documentation).

Caution:
Check CT circuit rating (rating label) and integrity of connections.

Caution:
Check protective fuse or miniature circuit breaker (MCB) rating.

Caution:
Check integrity of the PCT connection.

Caution:
Check voltage and current rating of external wiring, ensuring it is appropriate for the application.

2.4.8 PERIPHERAL CIRCUITRY

Warning:
Do not open the secondary circuit of a live CT since the high voltage produced may be lethal to personnel and could damage insulation. Short the secondary of the line CT before opening any connections to it.

Note:
For most GE Vernova equipment with ring-terminal connections, the threaded terminal block for current transformer termination is automatically shorted if the module is removed. Therefore external shorting of the CTs may not be required. Check the equipment documentation and wiring diagrams first to see if this applies.

Caution:
Where external components such as resistors or voltage dependent resistors (VDRs) are used, these may present a risk of electric shock or burns if touched.

Warning:
Take extreme care when using external test blocks and test plugs such as the MMLG, MMLB and P990, as hazardous voltages may be exposed. Ensure that CT shorting links are in place before removing test plugs, to avoid potentially lethal voltages.

Warning:
Data communication cables with accessible screens and/or screen conductors, (including optical fibre cables with metallic elements), may create an electric shock hazard in a sub-station environment if both ends of the cable screen are not connected to the same equipotential bonded earthing system.

To reduce the risk of electric shock due to transferred potential hazards:

i. The installation shall include all necessary protection measures to ensure that no fault currents can flow in the connected cable screen conductor.

ii. The connected cable shall have its screen conductor connected to the protective conductor terminal (PCT) of the connected equipment at both ends. This connection may be inherent in the connectors provided on the equipment but, if there is any doubt, this must be confirmed by a continuity test.

iii. The protective conductor terminal (PCT) of each piece of connected equipment shall be connected directly to the same equipotential bonded earthing system.

iv. If, for any reason, both ends of the cable screen are not connected to the same equipotential bonded earth system, precautions must be taken to ensure that such screen connections are made safe before work is done to, or in proximity to, any such cables.

v. No equipment shall be connected to any download or maintenance circuits or connectors of this product except temporarily and for maintenance purposes only.

vi. Equipment temporarily connected to this product for maintenance purposes shall be protectively earthed (if the temporary equipment is required to be protectively earthed), directly to the same equipotential bonded earthing system as the product.

Warning:
Small Form-factor Pluggable (SFP) modules which provide copper Ethernet connections typically do not provide any additional safety isolation. Copper Ethernet SFP modules must only be used in connector positions intended for this type of connection.

2.4.9 UPGRADING/SERVICING

Warning:
Do not insert or withdraw modules, PCBs or expansion boards from the equipment while energised, as this may result in damage to the equipment. Hazardous live voltages would also be exposed, endangering personnel.

Caution:
Internal modules and assemblies can be heavy and may have sharp edges. Take care when inserting or removing modules into or out of the IED.

2.5 DECOMMISSIONING AND DISPOSAL

Caution:
Before decommissioning, completely isolate the equipment power supplies (both poles of any dc supply). The auxiliary supply input may have capacitors in parallel, which may still be charged. To avoid electric shock, discharge the capacitors using the external terminals before decommissioning.

Caution:
Avoid incineration or disposal to water courses. Dispose of the equipment in a safe, responsible and environmentally friendly manner, and if applicable, in accordance with country-specific regulations.

2.6 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.

CE

2.6.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

2.6.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

2.6.3 R&TTE COMPLIANCE: 2014/53/EU

Radio and Telecommunications Terminal Equipment (R&TTE) directive 2014/53/EU.

Conformity is demonstrated by compliance to both the EMC directive and the Low Voltage directive, to zero volts.

2.6.4 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.

c UL us

CHAPTER 3

HARDWARE DESIGN

3.1 CHAPTER OVERVIEW

This chapter provides information about the product's hardware design.

This chapter contains the following sections:

3.2 HARDWARE ARCHITECTURE

The main components comprising devices based on the Px4x platform are as follows:

- The housing, consisting of a front panel and connections at the rear
- The Main processor module consisting of the main CPU (Central Processing Unit), memory and an interface to the front panel HMI (Human Machine Interface)
- A selection of plug-in boards and modules with presentation at the rear for the power supply, communication functions, digital I/O, analogue inputs, and time synchronisation connectivity

All boards and modules are connected by a parallel data and address bus, which allows the processor module to send and receive information to and from the other modules as required. There is also a separate serial data bus for conveying sampled data from the input module to the CPU. These parallel and serial databuses are shown as a single interconnection module in the following figure, which shows typical modules and the flow of data between them.

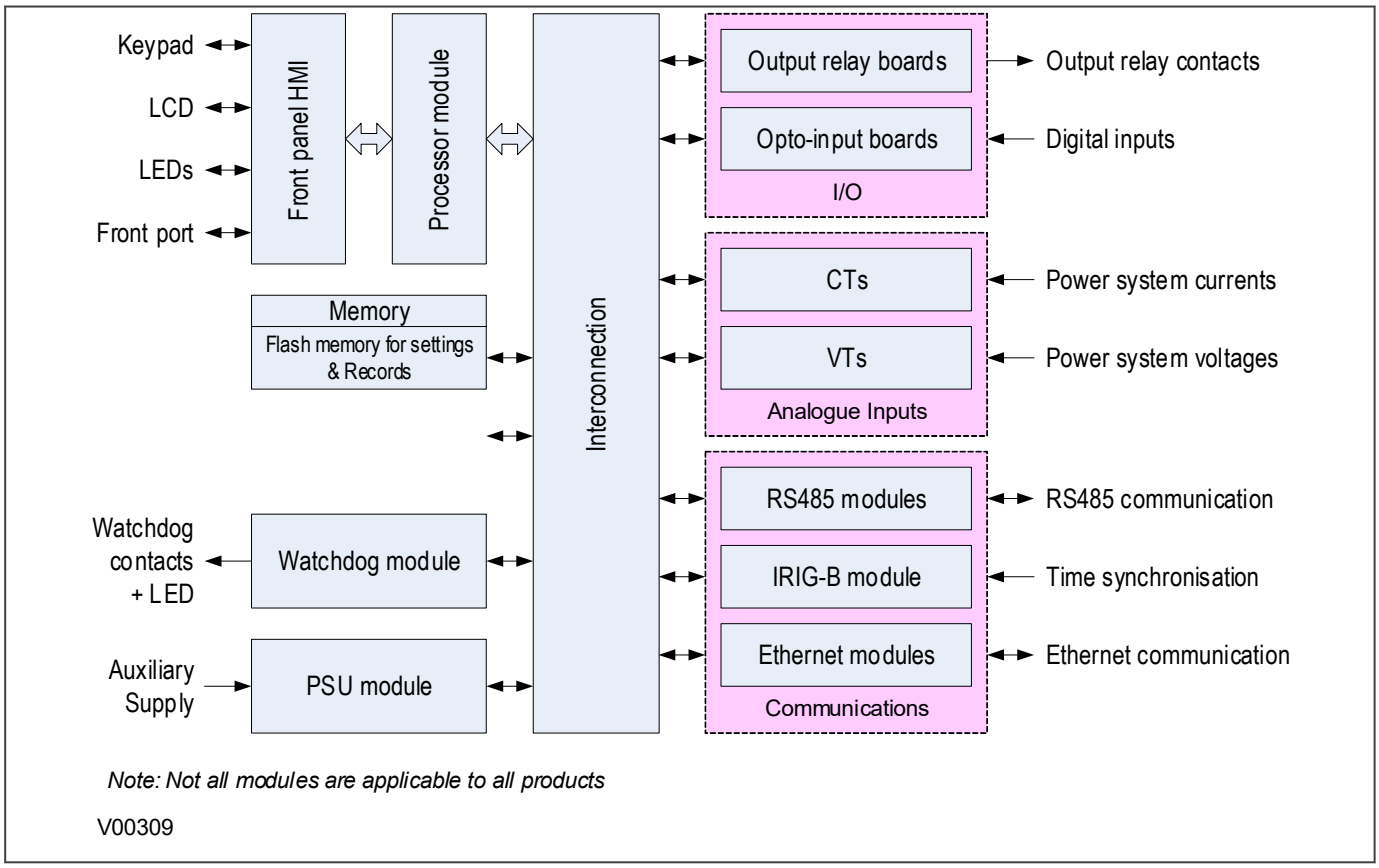


Figure 3: Hardware architecture

3.3 MECHANICAL IMPLEMENTATION

All products based on the Px4x platform have common hardware architecture. The hardware is modular and consists of the following main parts:

- Case and terminal blocks
- Boards and modules
- Front panel

The case comprises the housing metalwork and terminal blocks at the rear. The boards fasten into the terminal blocks and are connected together by a ribbon cable. This ribbon cable connects to the processor in the front panel.

The following diagram shows an exploded view of a typical product. The diagram shown does not necessarily represent exactly the product model described in this manual.

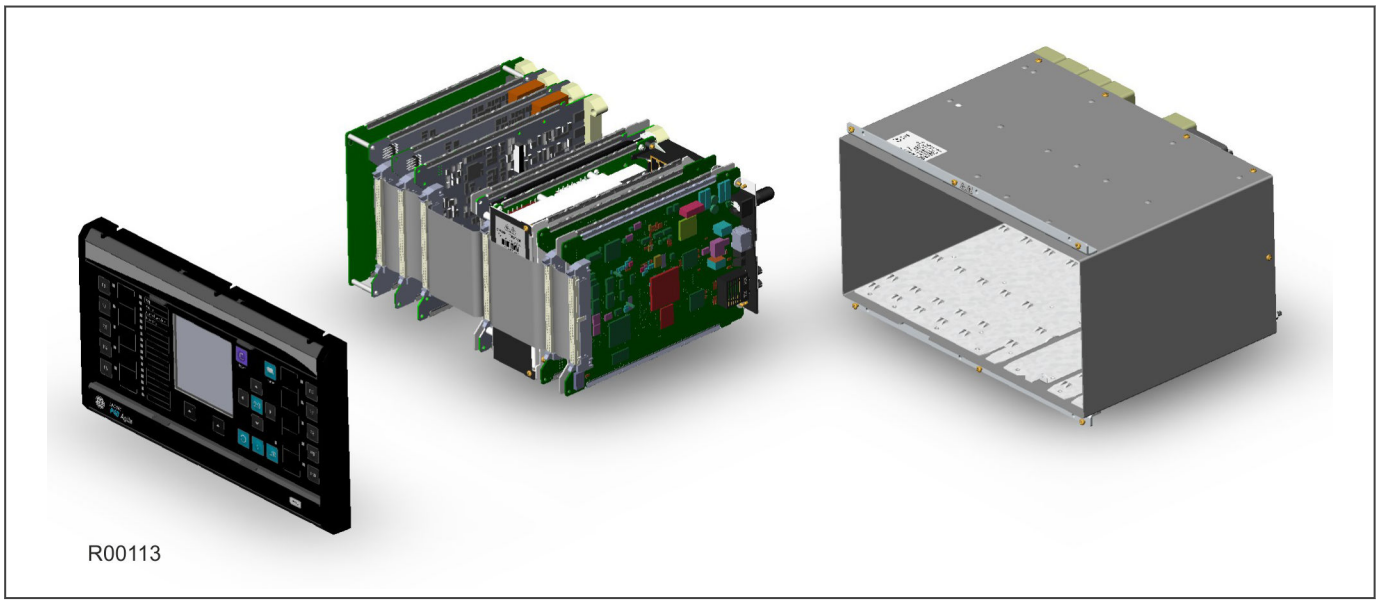


Figure 4: Exploded view of IED

3.3.1 HOUSING VARIANTS

The Px4x range of products are implemented in a range of case sizes. Case dimensions for industrial products usually follow modular measurement units based on rack sizes. These are: U for height and TE for width, where:

- 1U = 1.75 inches = 44.45 mm
- 1TE = 0.2 inches = 5.08 mm

The products are available in panel-mount or standalone versions. All products are nominally 4U high. This equates to 177.8 mm or 7 inches.

The cases are pre-finished steel with a conductive covering of aluminium and zinc. This provides good grounding at all joints, providing a low resistance path to earth that is essential for performance in the presence of external noise.

The case width depends on the product type and its hardware options. There are three different case widths for the described range of products: 40TE, 60TE and 80TE. The case dimensions and compatibility criteria are as follows:

Case width (TE)	Case width (mm)	Case width (inches)
40TE	203.2	8
60TE	304.8	12
80TE	406.4	16

Note:
Not all case sizes are available for all models.

3.3.2 LIST OF BOARDS

The product's hardware consists of several modules drawn from a standard range. The exact specification and number of hardware modules depends on the model number and variant. Depending on the exact model, the product in question will use a selection of the following boards.

Board	Use
Main Processor board - 40TE or smaller	Main Processor board - without support for function keys
Main Processor board - 60TE or larger	Main Processor board - with support for function keys
Power supply board - 24/54V DC	Power supply input. Accepts DC voltage between 24V and 54V
Power supply board - 48/125V DC	Power supply input. Accepts DC voltage between 48V and 125V
Power supply board - 110/250V DC	Power supply input. Accepts DC voltage between 110V and 125V
Transformer board	Contains the voltage and current transformers
Input board	Contains the A/D conversion circuitry
Input board with opto-inputs	Contains the A/D conversion circuitry + 8 digital opto-inputs
IRIG-B board - modulated input	Interface board for modulated IRIG-B timing signal
Fibre board + IRIG-B	Interface board for fibre-based RS485 connection + demodulated IRIG-B
2nd rear communications board	Interface board for RS232/RS485 connections
2nd rear communications board with IRIG-B input	Interface board for RS232/RS485 + IRIG-B connections
High-break output relay board	Output relay board with high breaking capacity relays
Single Ethernet, universal IRIG-B, IEEE1588, maintenance port	Single LC duplex Ethernet port with universal IRIG-B and 1 RJ45 maintenance/ engineering port
Redundant Ethernet RSTP + PRP + HSR + Failover ports, serial fibre port, universal IRIG-B	2 LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with IEC 60870-5-103 serial fibre ST ports with on-board universal IRIG-B and 1 RJ45 maintenance/engineering port
Redundant Ethernet RSTP + PRP + HSR + Failover universal IRIG-B	2 RJ45 duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two copper pairs), with on-board universal IRIG-B and 1 RJ45 maintenance/engineering port
Redundant Ethernet RSTP + PRP + HSR + Failover ports, universal IRIG-B	2 LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with on-board universal IRIG-B and 1 RJ45 maintenance/ engineering port
Output relay output board	Standard output relay board

3.4 FRONT PANEL

Depending on the exact model and chosen options, the product will be housed in either a 40TE, 60TE or 80TE case. By way of example, the following diagram shows the front panel of a typical unit. The front panels of the products based on 40TE, 60TE and 80TE cases have a lot of commonality and differ only in that the 40TE front panel does not include 10 function keys with their associated user-programmable LEDs.

R00110

Figure 5: Front panel (80TE)

The front panel consists of:

- Top and bottom compartments with hinged cover
- LCD display
- Keypad
- USB Type B port inside the bottom compartment
- Fixed function LEDs
- Function keys and LEDs (60TE and 80TE models)
- Programmable LEDs

3.4.1 FRONT PANEL COMPARTMENTS

The top compartment contains labels for the:

- Serial number
- Current and voltage ratings.

The bottom compartment contains:

- USB type B port

3.4.2 HMI PANEL

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the colour LCD display.

The colour LCD display is an active matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit and back-light unit. The resolution of the 4.0” TFT-LCD is 480x480 pixels and it can display up to 16.7M colours.

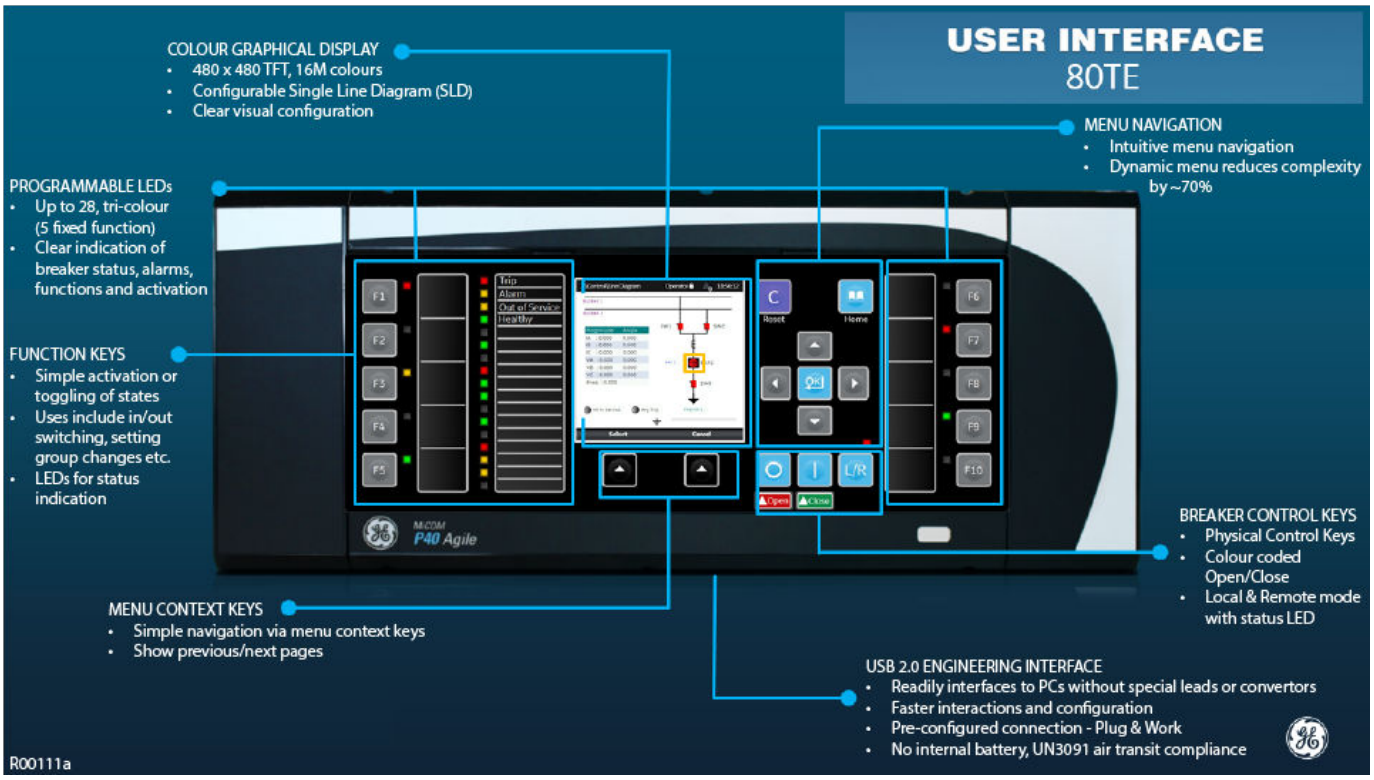
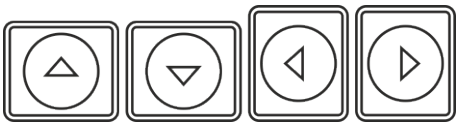
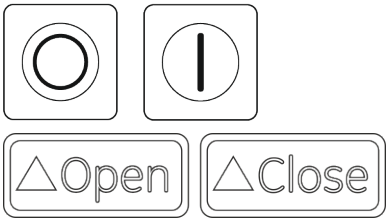


Figure 6: HMI panel

3.4.3 KEYPAD

The keypad consists of the following keys:

4 arrow keys to navigate the menus, changing values within the cell or to select the next item on the SLD (organised around the Enter key).	
An enter key for changing and executing settings. When a bottom banner menu context key label is selected, the OK key can also be used to navigate between pages.	
A clear/reset key for clearing the current setting dialogue or to navigate to the top menu.	
A home key for navigating to the default menu view.	
2 menu context keys used to navigate between pages.	

Open/Close keys (colour coded) **Note:** Colour coding is selectable via labels and configuration of PSL/ SLD.	
Local/remote key to select between local or remote modes.	

3.4.4 USB PORT

The USB port is situated inside the bottom compartment, and is used to communicate with a locally connected PC. It has two main purposes:

- To transfer settings between the PC and the device.
- For downloading firmware updates and menu text editing.

The port is intended for temporary connection during testing, installation and commissioning. It is not intended to be used for permanent SCADA communications. This port supports the Courier communication protocol only. Courier is a proprietary communication protocol to allow communication with a range of protection equipment, and between the device and the Windows-based support software package.

You can connect the unit to a PC with a USB cable up to 5 m in length.

The inactivity timer for the front port is set to 15 minutes. This controls how long the unit maintains its level of password access on the front port. If no messages are received on the front port for 15 minutes, any password access level that has been enabled is cancelled.

Note:
The front USB port does not support automatic extraction of event and disturbance records, although this data can be accessed manually.

Caution:
When not in use, always close the cover of the USB port to prevent contamination.

3.4.5 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

3.4.6 FUNCTION KEYS

The programmable function keys are available for custom use for some models.

Factory default settings associate specific functions to these keys, but by using programmable scheme logic, you can change the default functions of these keys to fit specific needs. Adjacent to these function keys are programmable LEDs, which are usually set to be associated with their respective function keys. The device has 10 function keys in the 60TE and 80TE case size models and no function keys in the 40TE case size model.

3.4.7 PROGRAMABLE LEDS

The device has 13 of programmable LEDs, which can be associated with PSL-generated signals. The programmable LEDs are tri-colour and can be set to RED, YELLOW or GREEN.

3.5 REAR PANEL

The MiCOM Px40 series uses a modular construction. Most of the internal structure consists of boards and modules that fit into slots. Some of the boards plug into terminal blocks, which are bolted onto the rear of the unit. However, some boards such as the communications boards have their own connectors. The rear panel consists of these terminal blocks plus the rears of the communications boards.

The back panel cut-outs and slot allocations vary. This depends on the product, the type of boards and the terminal blocks needed to populate the case. The following diagram shows a typical rear view of a case populated with various boards.

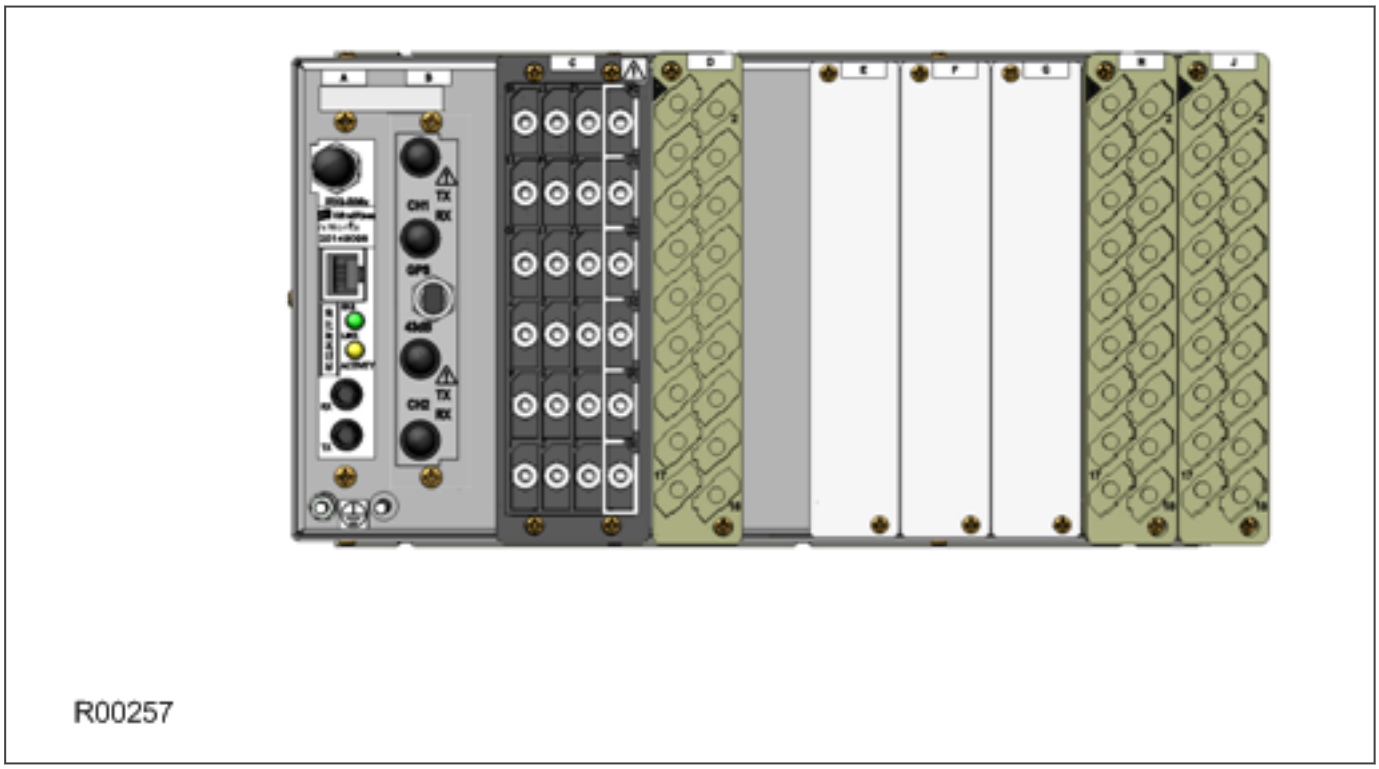


Figure 7: Rear view of populated case

Note:
This diagram is just an example and may not show the exact product described in this manual. It also does not show the full range of available boards, just a typical arrangement.

Not all slots are the same size. The slot width depends on the type of board or terminal block. For example, HD (heavy duty) terminal blocks, as required for the analogue inputs, require a wider slot size than MD (medium duty) terminal blocks. The board positions are not generally interchangeable. Each slot is designed to house a particular type of board. Again this is model-dependent.

The device may use one or more of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, opto-inputs, relay outputs and rear communications port
- MiDOS terminal blocks for CT and VT circuits
- RTD/CLIO terminal block for connection to analogue transducers

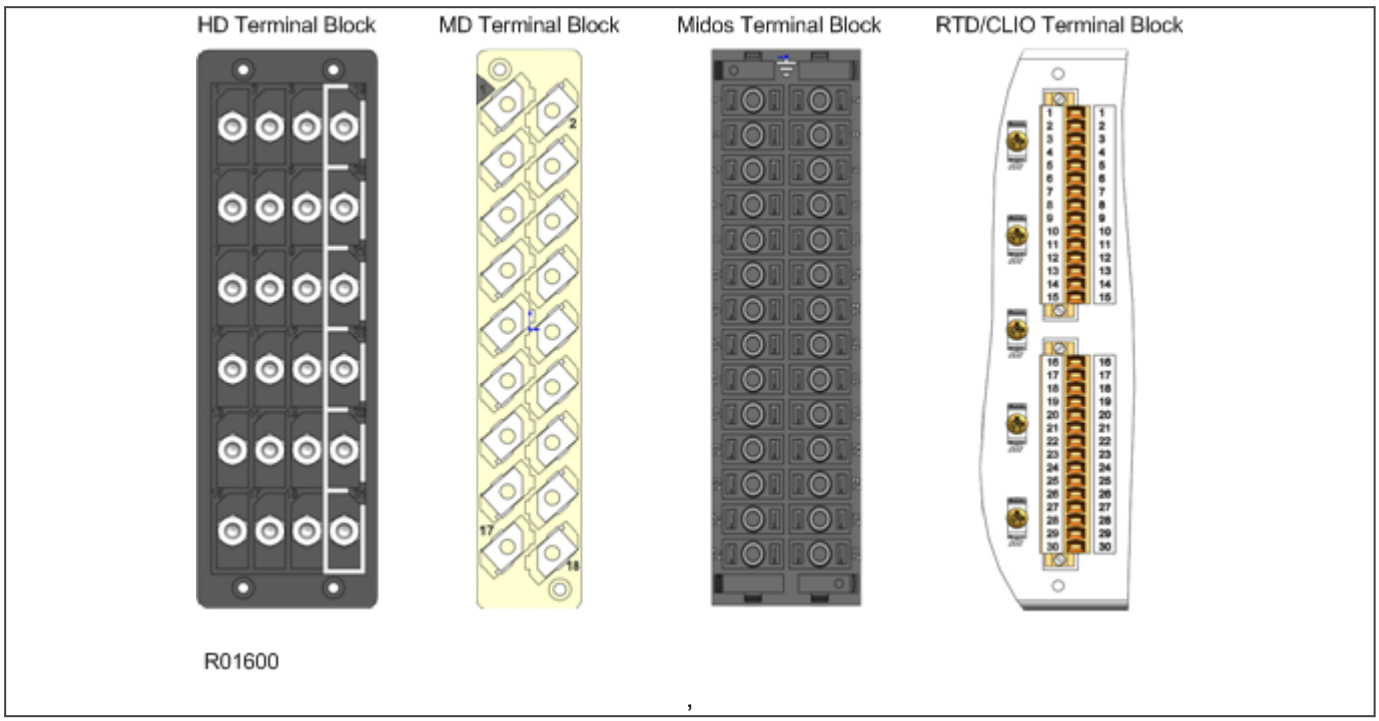


Figure 8: Terminal block types

Note:
Not all products use all types of terminal blocks. The product described in this manual may use one or more of the above types.

3.5.1 TERMINAL BLOCK INGRESS PROTECTION

IP2x shields and side cover panels are designed to provide IP20 ingress protection for MiCOM terminal blocks. The shields and covers may be attached during installation or retrofitted to upgrade existing installations - see figure below. For more information, contact your local sales office or our worldwide Contact Centre.

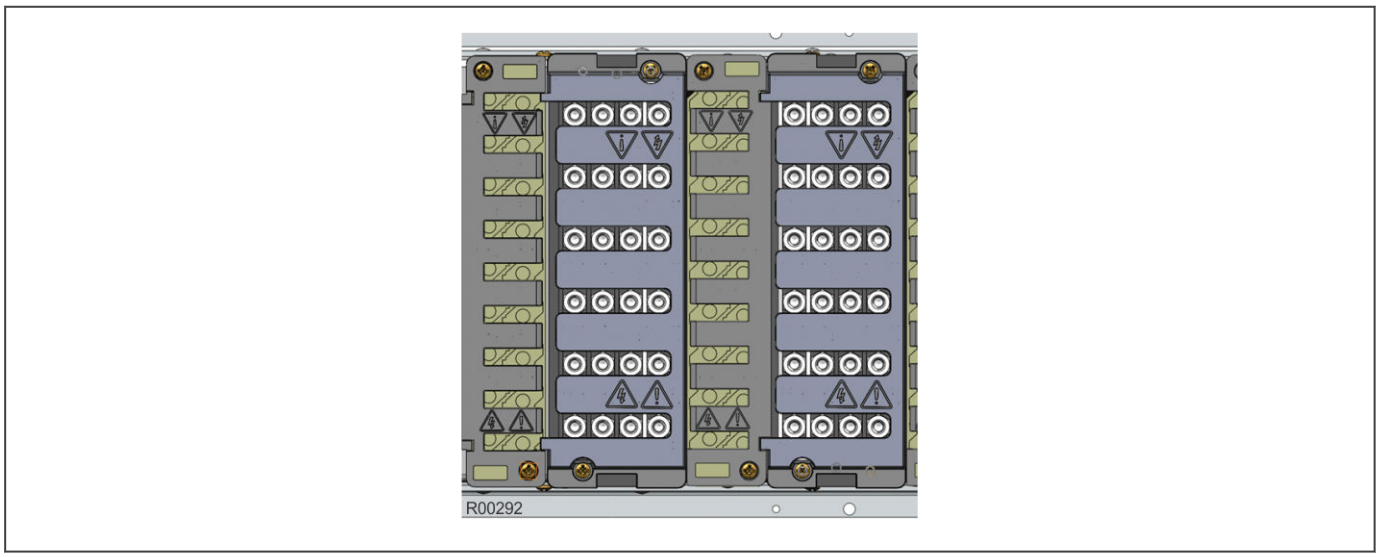


Figure 9: Example - fitted IP2x shields (cabling omitted for clarity)

3.6 BOARDS AND MODULES

Each product comprises a selection of PCBs (Printed Circuit Boards) and subassemblies, depending on the chosen configuration.

3.6.1 PCBS

A PCB typically consists of the components, a front connector for connecting into the main system parallel bus via a ribbon cable, and an interface to the rear. This rear interface may be:

- Directly presented to the outside world (as is the case for communication boards such as Ethernet Boards)
- Presented to a connector, which in turn connects into a terminal block bolted onto the rear of the case (as is the case for most of the other board types)

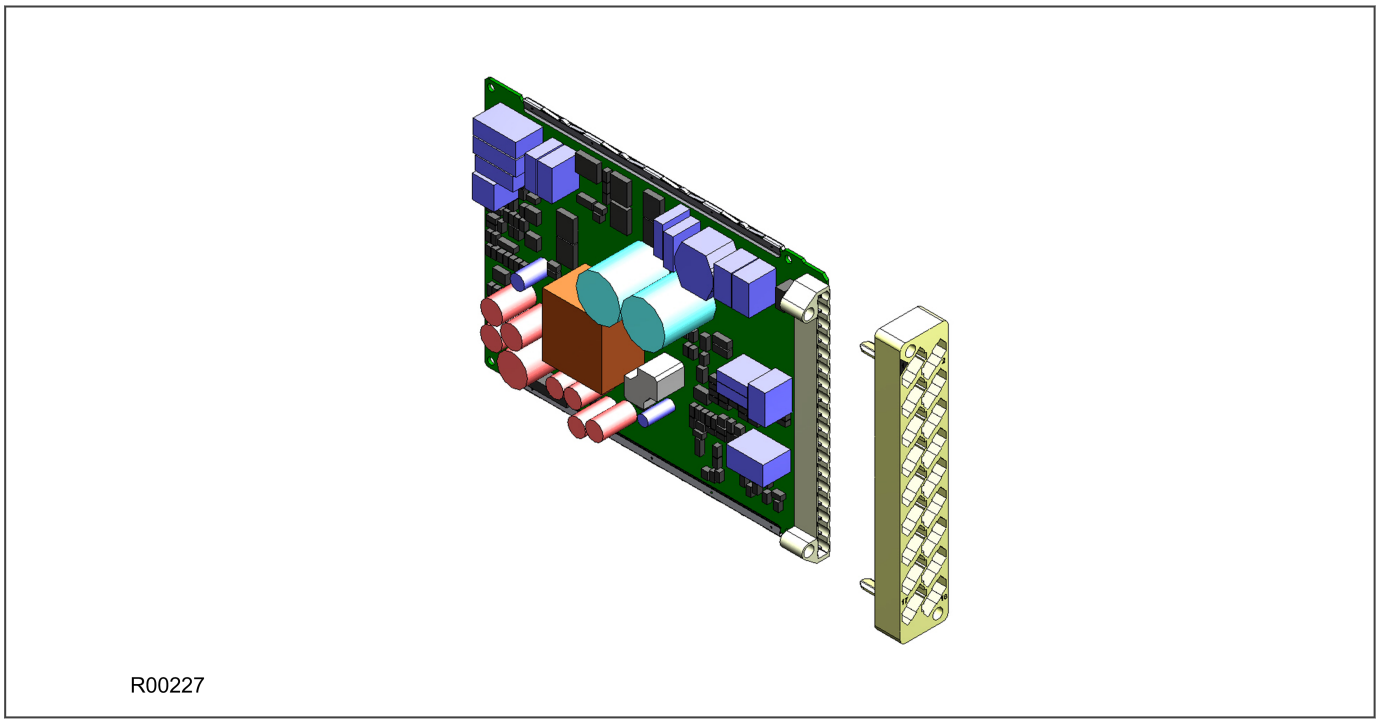


Figure 10: Rear connection to terminal block

3.6.2 SUBASSEMBLIES

A sub-assembly consists of two or more boards bolted together with spacers and connected with electrical connectors. It may also have other special requirements such as being encased in a metal housing for shielding against electromagnetic radiation.

Boards are designated by a part number beginning with ZN, whereas pre-assembled sub-assemblies are designated with a part number beginning with GN. Sub-assemblies, which are put together at the production stage, do not have a separate part number.

The products in the Px40 series typically contain two sub-assemblies:

- The power supply assembly comprising:
  - A power supply board
  - An output relay board
- The input module comprising:
  - One or more transformer boards, which contains the voltage and current transformers (partially or fully populated)
  - One or more input boards
  - Metal protective covers for EM (electromagnetic) shielding

The input module is pre-assembled and is therefore assigned a GN number, whereas the power supply module is assembled at production stage and does not therefore have an individual part number.

3.6.3 MAIN PROCESSOR BOARD

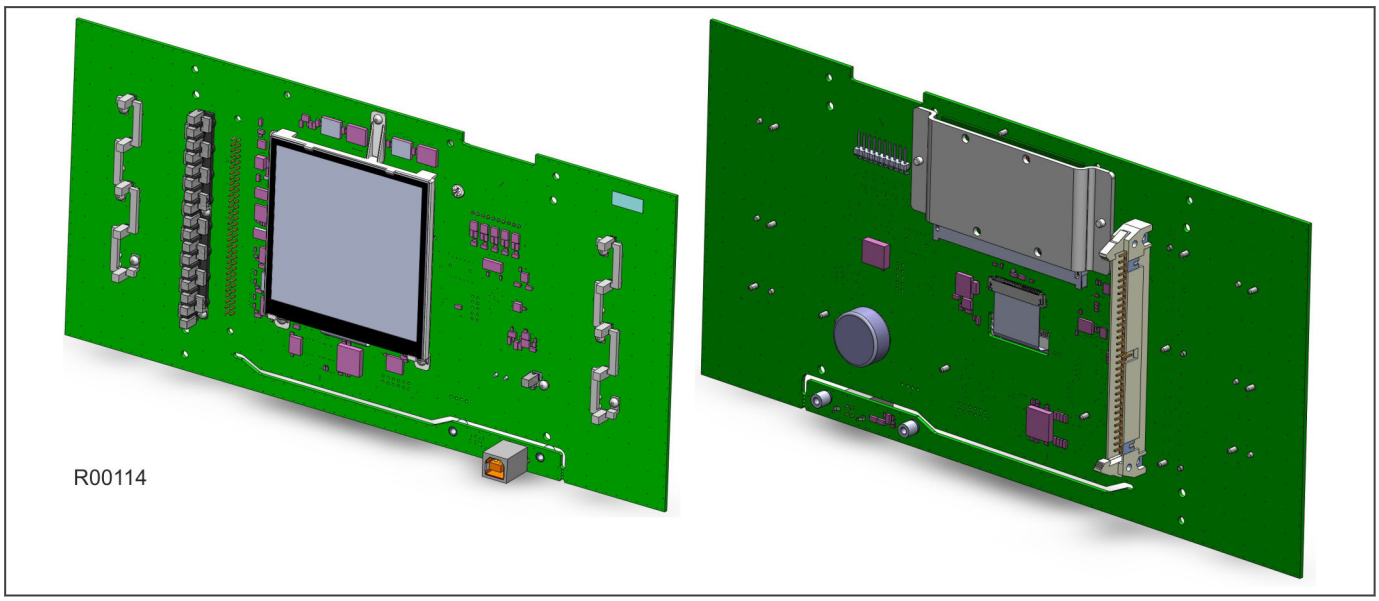


Figure 11: Main processor board

The main processor board performs all calculations and controls the operation of all other modules in the IED, including the data communication and user interfaces. This is the only board that does not fit into one of the slots. It resides in the front panel and connects to the rest of the system using an internal ribbon cable.

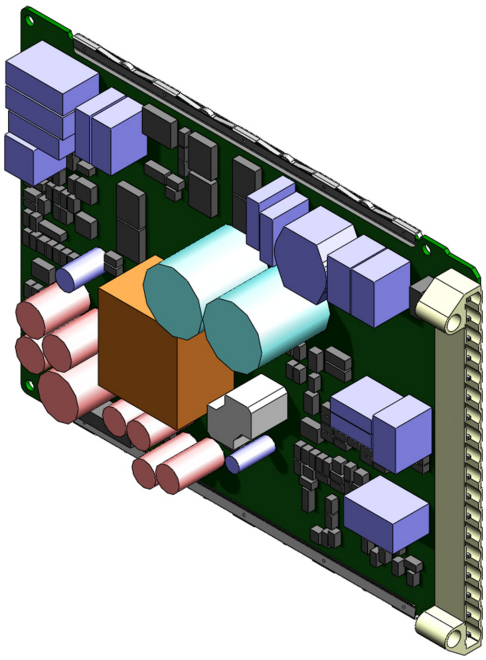
The LCD and LEDs are mounted on the processor board along with the front panel communication ports.

The memory on the main processor board is split into two categories: volatile and non-volatile. The volatile memory is DRAM, used by the processor to run the software and store data during calculations. The non-volatile memory is Flash memory and is used to store Product Firmware, text and configuration data including the present setting values, disturbance records, events, fault and maintenance record data.

There are two board types available depending on the size of the case:

- For models in 40TE cases
- For models in 60TE cases and larger

3.6.4 POWER SUPPLY BOARD



R00228

Figure 12: Power supply board

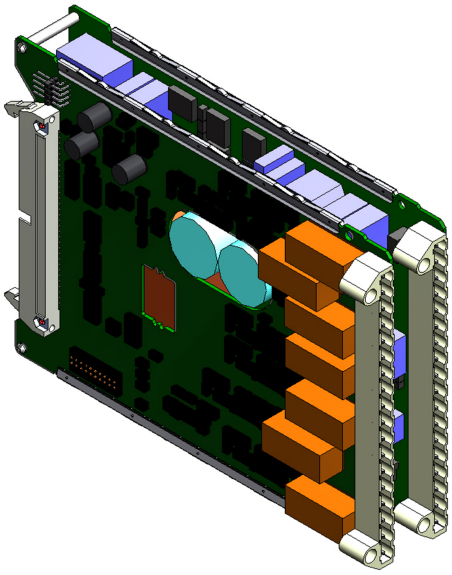
The power supply board provides power to the unit. One of three different configurations of the power supply board can be fitted to the unit. This is specified at the time of order and depends on the magnitude of the supply voltage that will be connected to it.

There are three board types, which support the following voltage ranges:

- 24/54 V DC
- 48/125 V DC or 40-100V AC
- 110/250 V DC or 100-240V AC

The power supply board connector plugs into a medium duty terminal block. This terminal block is always positioned on the right hand side of the unit looking from the rear.

The power supply board is usually assembled together with a relay output board to form a complete subassembly, as shown in the following diagram.



R00229

Figure 13: Power supply assembly

The power supply outputs are used to provide isolated power supply rails to the various modules within the unit. Three voltage levels are used by the unit's modules:

- 5.1 V for all of the digital circuits
- +/- 16 V for the analogue electronics such as on the input board
- 22 V for driving the output relay coils.

All power supply voltages, including the 0 V earth line, are distributed around the unit by the 64-way ribbon cable.

The power supply board incorporates inrush current limiting. This limits the peak inrush current to approximately 10 A.

Power is applied to pins 1 and 2 of the terminal block, where pin 1 is negative and pin 2 is positive. The pin numbers are clearly marked on the terminal block as shown in the following diagram.

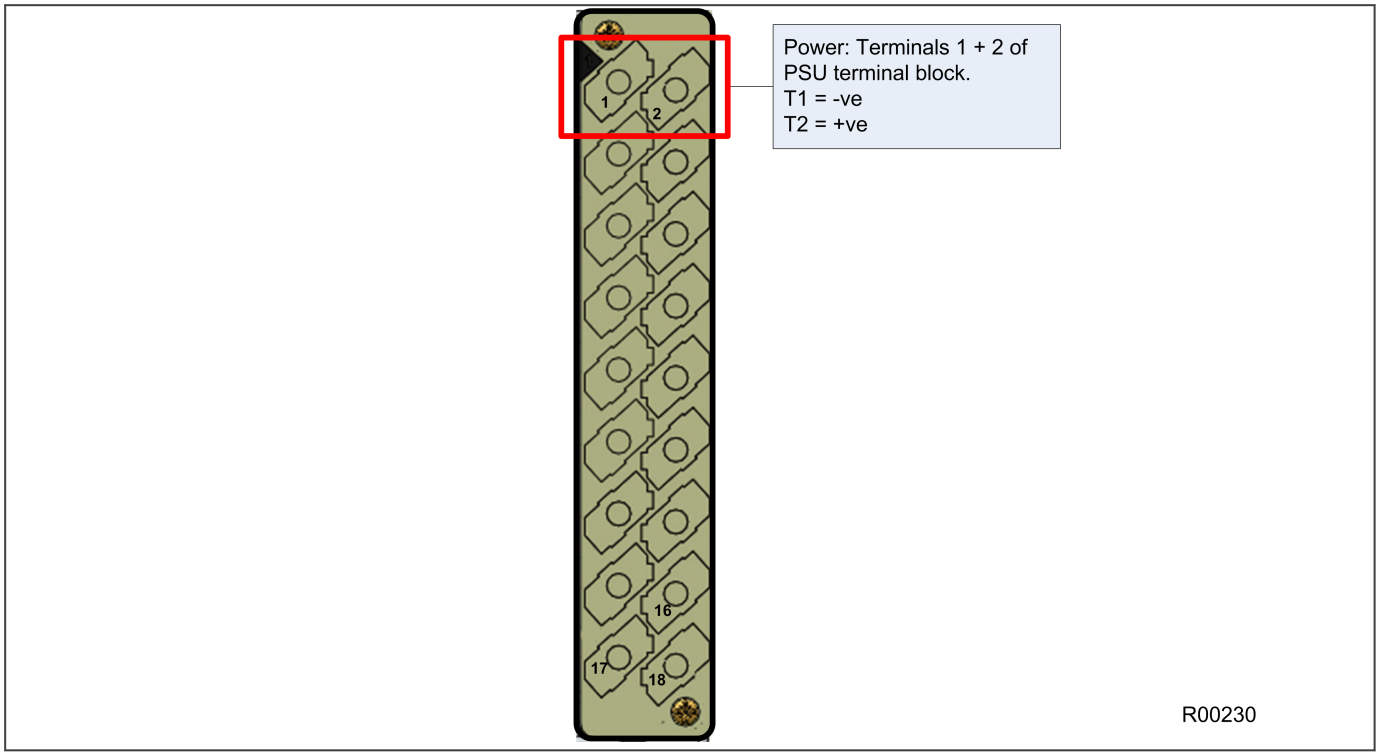


Figure 14: Power supply terminals

3.6.4.1 WATCHDOG

The Watchdog contacts are also hosted on the power supply board. The Watchdog facility provides two output relay contacts, one normally open and one normally closed. These are used to indicate the health of the device and are driven by the main processor board, which continually monitors the hardware and software when the device is in service.

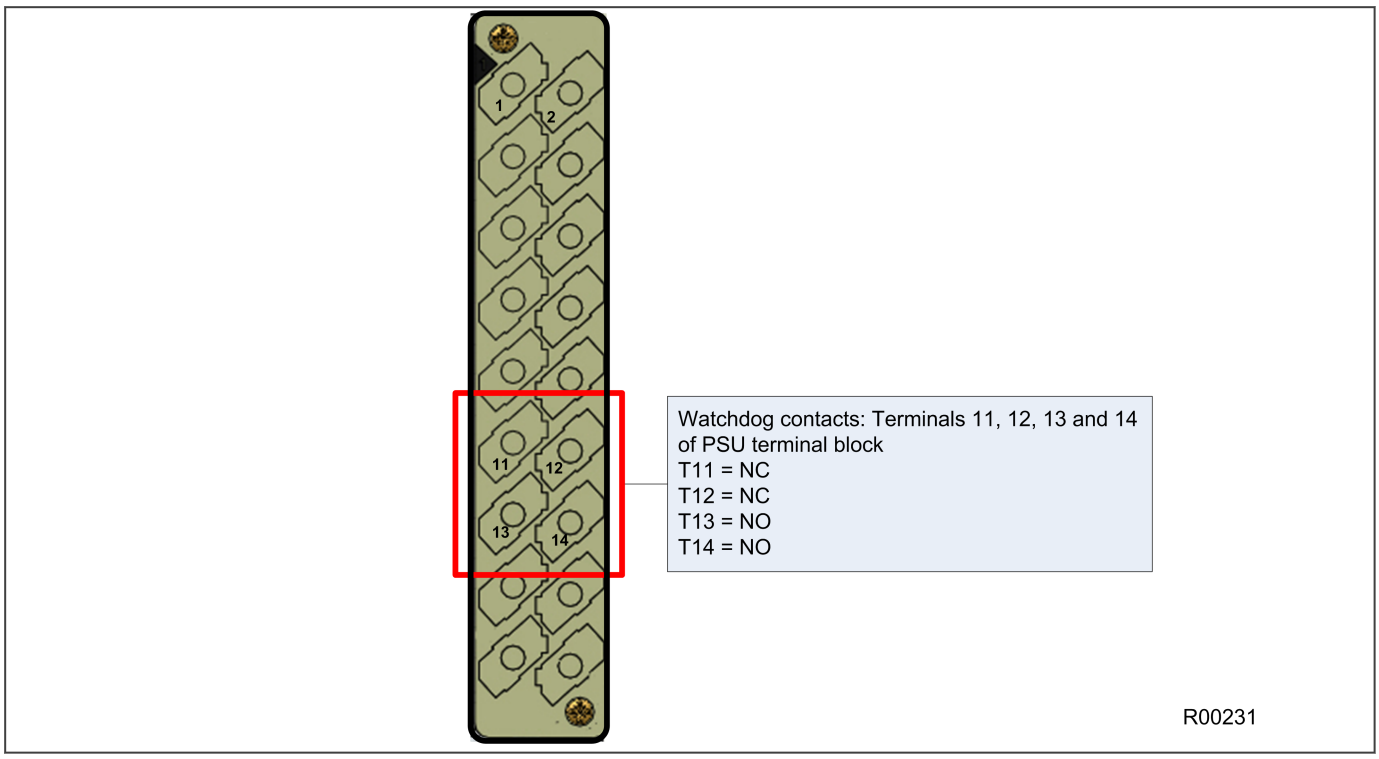


Figure 15: Watchdog contact terminals

3.6.4.2 REAR SERIAL PORT

The rear serial port (RP1) is housed on the power supply board. This is a three-terminal EIA(RS)485 serial communications port and is intended for use with a permanently wired connection to a remote control centre for SCADA communication. The interface supports half-duplex communication and provides optical isolation for the serial data being transmitted and received.

The physical connectivity is achieved using three screw terminals; two for the signal connection, and the third for the earth shield of the cable. These are located on pins 16, 17 and 18 of the power supply terminal block, which is on the far right looking from the rear. The interface can be selected between RS485 and K-bus. When the K-Bus option is selected, the two signal connections are not polarity conscious.

The polarity independent K-bus can only be used for the Courier data protocol. The polarity conscious MODBUS, IEC 60870-5-103 and DNP3.0 protocols need RS485.

The following diagram shows the rear serial port. The pin assignments are as follows:

- Pin 16: Earth shield
- Pin 17: Negative signal
- Pin 18: Positive signal

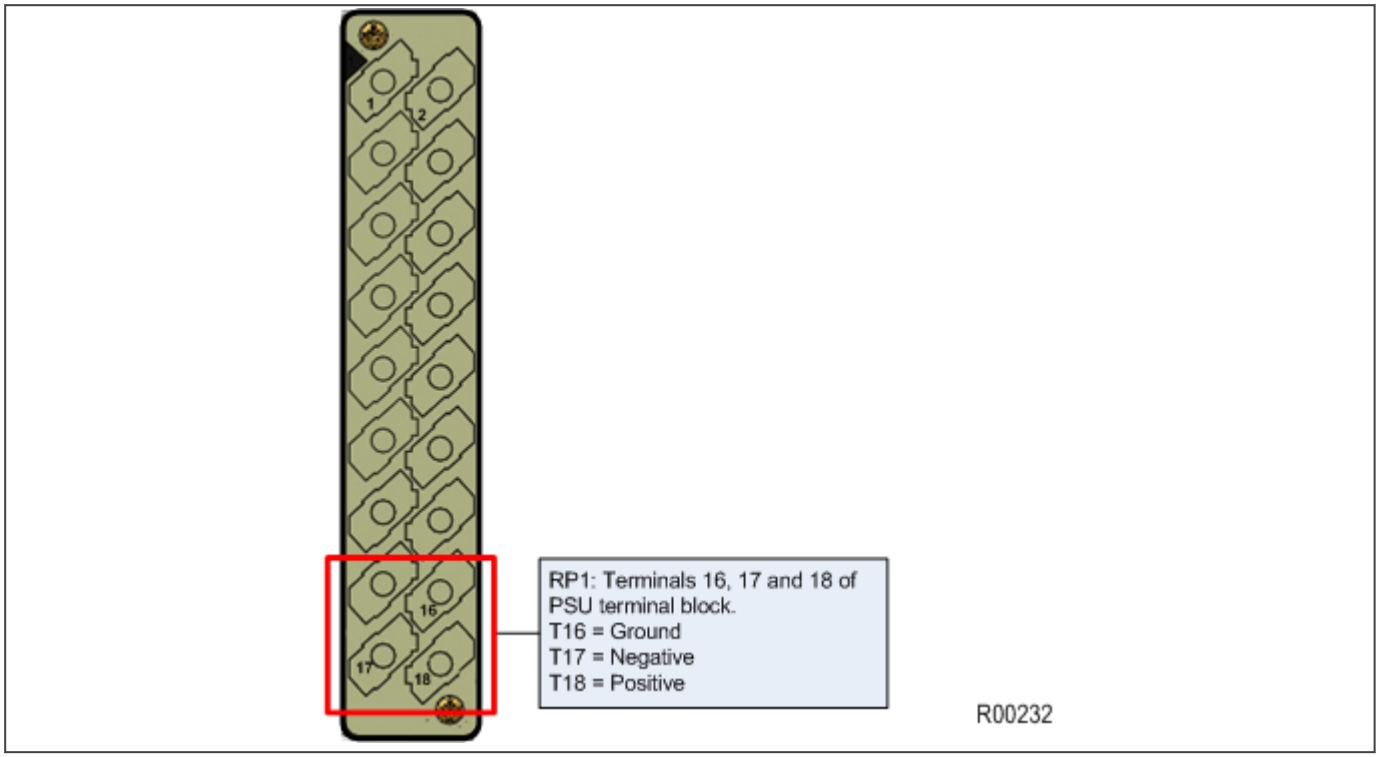


Figure 16: Rear serial port terminals

An additional serial port with D-type presentation is available as an optional board, if required.

3.6.5 INPUT MODULE - 1 TRANSFORMER BOARD

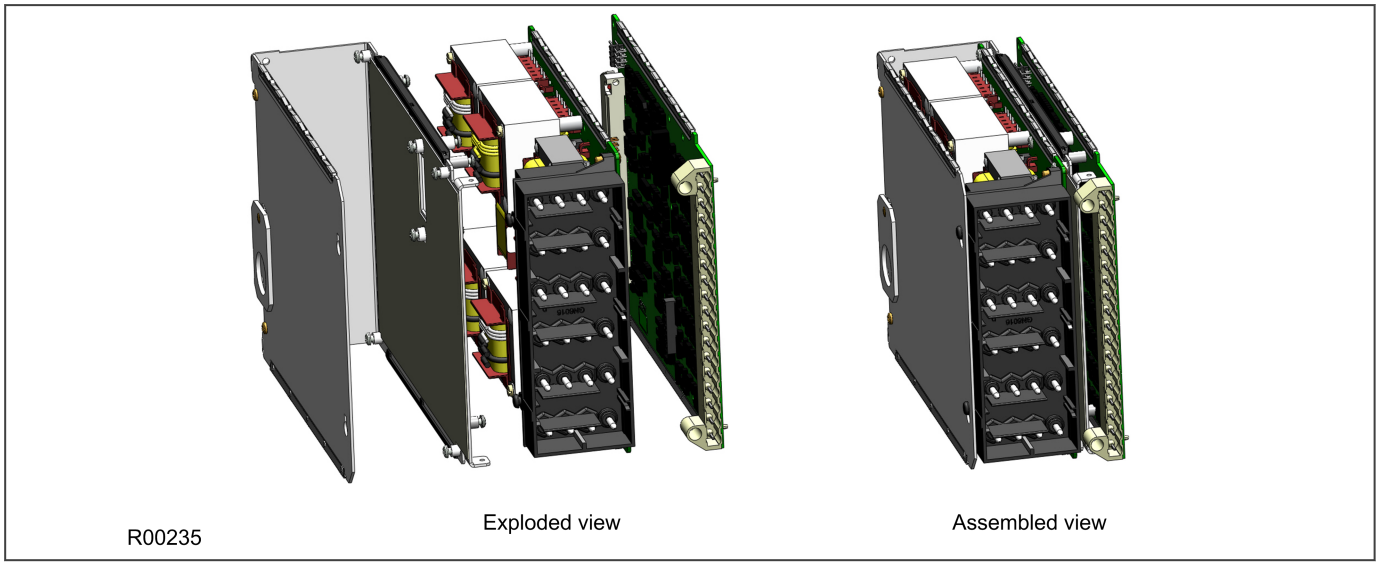


Figure 17: Input module - 1 transformer board

The input module consists of the main input board coupled together with an instrument transformer board. The instrument transformer board contains the voltage and current transformers, which isolate and scale the analogue input signals delivered by the system transformers. The input board contains the A/D conversion and digital processing circuitry, as well as eight digital isolated inputs (opto-inputs).

The boards are connected together physically and electrically. The module is encased in a metal housing for shielding against electromagnetic interference.

3.6.5.1 INPUT MODULE CIRCUIT DESCRIPTION

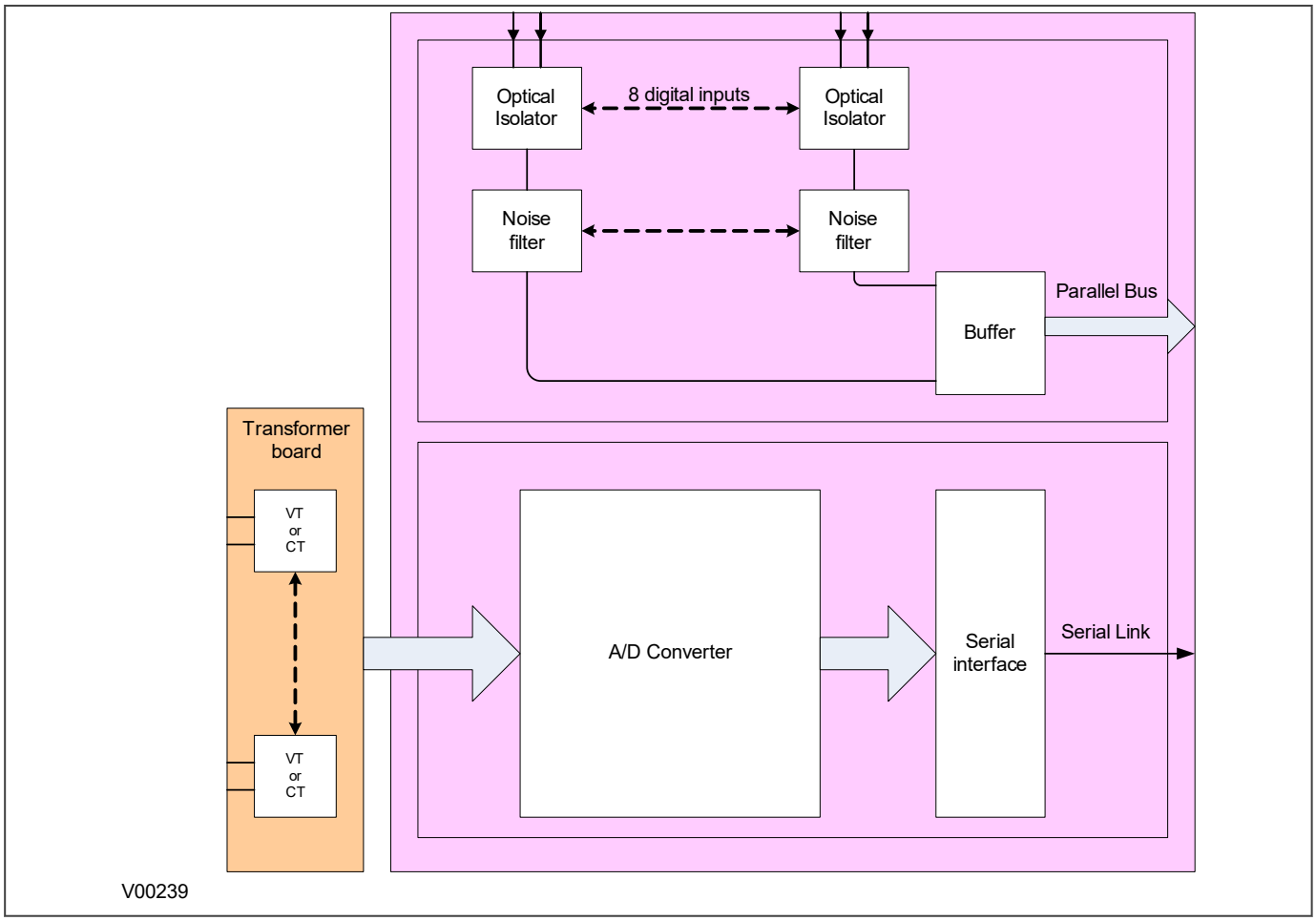


Figure 18: Input module schematic

A/D Conversion

The differential analogue inputs from the CT and VT transformers are presented to the main input board as shown. Each differential input is first converted to a single input quantity referenced to the input board's earth potential. The analogue inputs are sampled and converted to digital, then filtered to remove unwanted properties. The samples are then passed through a serial interface module which outputs data on the serial sample data bus.

The calibration coefficients are stored in non-volatile memory. These are used by the processor board to correct for any amplitude or phase errors introduced by the transformers and analogue circuitry.

Opto-isolated inputs

The other function of the input board is to read in the state of the digital inputs. As with the analogue inputs, the digital inputs must be electrically isolated from the power system. This is achieved by means of the 8 on-board optical isolators for connection of up to 8 digital signals. The digital signals are passed through an optional noise filter before being buffered and presented to the unit's processing boards in the form of a parallel data bus.

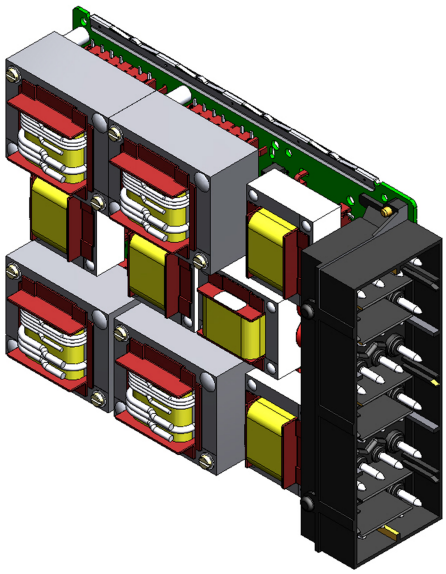
This selectable filtering allows the use of a pre-set filter of ½ cycle which renders the input immune to induced power-system noise on the wiring. Although this method is secure it can be slow, particularly for inter-tripping. This can be improved by switching off the ½ cycle filter, in which case one of the following methods to reduce ac noise should be considered.

- Use double pole switching on the input
- Use screened twisted cable on the input circuit

The opto-isolated logic inputs can be configured for the nominal battery voltage of the circuit for which they are a part, allowing different voltages for different circuits such as signalling and tripping.

Note:
The opto-input circuitry can be provided without the A/D circuitry as a separate board, which can provide supplementary opto-inputs.

3.6.5.2 TRANSFORMER BOARD



R00237

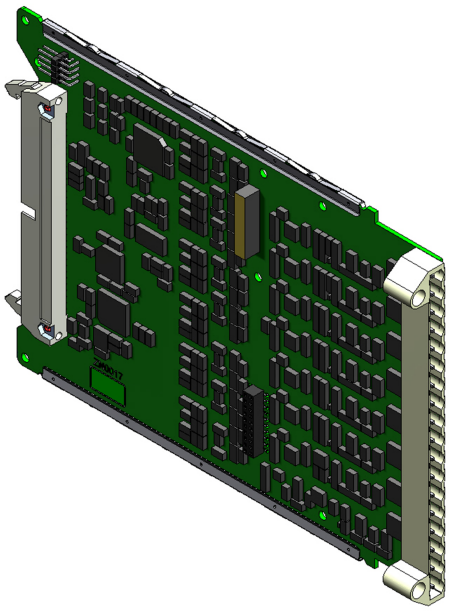
Figure 19: Transformer board

The transformer board hosts the current and voltage transformers. These are used to step down the currents and voltages originating from the power systems' current and voltage transformers to levels that can be used by the devices' electronic circuitry. In addition to this, the on-board CT and VT transformers provide electrical isolation between the unit and the power system.

The transformer board is connected physically and electrically to the input board to form a complete input module.

For terminal connections, please refer to the wiring diagrams.

3.6.5.3 INPUT BOARD



R00238

Figure 20: Input board

The input board is used to convert the analogue signals delivered by the current and voltage transformers into digital quantities used by the IED. This input board also has on-board opto-input circuitry, providing eight optically-isolated digital inputs and associated noise filtering and buffering. These opto-inputs are presented to the user by means of an MD terminal block, which sits adjacent to the analogue inputs HD terminal block.

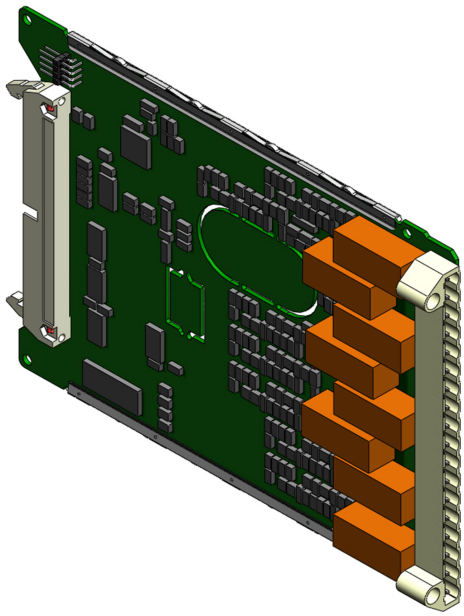
The input board is connected physically and electrically to the transformer board to form a complete input module.

The terminal numbers of the opto-inputs are as follows:

Terminal Number	Opto-input
Terminal 1	Opto 1 -ve
Terminal 2	Opto 1 +ve
Terminal 3	Opto 2 -ve
Terminal 4	Opto 2 +ve
Terminal 5	Opto 3 -ve
Terminal 6	Opto 3 +ve
Terminal 7	Opto 4 -ve
Terminal 8	Opto 4 +ve
Terminal 9	Opto 5 -ve
Terminal 10	Opto 5 +ve
Terminal 11	Opto 6 -ve
Terminal 12	Opto 6 +ve
Terminal 13	Opto 7 –ve
Terminal 14	Opto 7 +ve

Terminal Number	Opto-input
Terminal 15	Opto 8 –ve
Terminal 16	Opto 8 +ve
Terminal 17	Common
Terminal 18	Common

3.6.6 STANDARD OUTPUT RELAY BOARD



R00234

Figure 21: Standard relay output board - 8 contacts

This output relay board has 8 relays with 6 Normally Open contacts and 2 Changeover contacts.

The output relay board is provided together with the power supply board as a complete assembly, or independently for the purposes of relay output expansion.

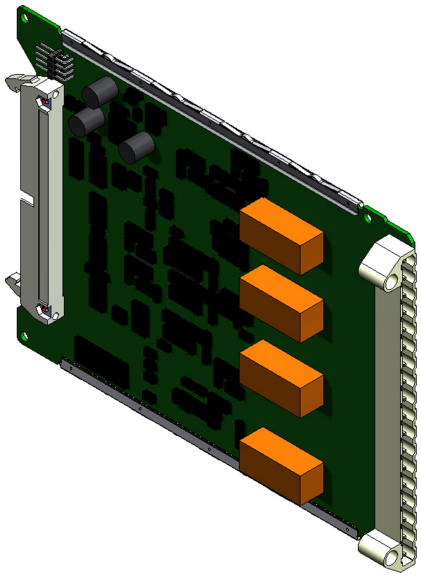
There are two cut-out locations in the board. These can be removed to allow power supply components to protrude when coupling the output relay board to the power supply board. If the output relay board is to be used independently, these cut-out locations remain intact.

The terminal numbers are as follows:

Terminal Number	Output Relay
Terminal 1	Relay 1 NO
Terminal 2	Relay 1 NO
Terminal 3	Relay 2 NO
Terminal 4	Relay 2 NO
Terminal 5	Relay 3 NO
Terminal 6	Relay 3 NO

Terminal Number	Output Relay
Terminal 7	Relay 4 NO
Terminal 8	Relay 4 NO
Terminal 9	Relay 5 NO
Terminal 10	Relay 5 NO
Terminal 11	Relay 6 NO
Terminal 12	Relay 6 NO
Terminal 13	Relay 7 changeover
Terminal 14	Relay 7 changeover
Terminal 15	Relay 7 common
Terminal 16	Relay 8 changeover
Terminal 17	Relay 8 changeover
Terminal 18	Relay 8 common

3.6.7 HIGH BREAK OUTPUT RELAY BOARD



R00245

Figure 22: High Break relay output board

A High Break output relay board is available as an option. It comprises four normally open output contacts, which are suitable for high breaking loads.

A High Break contact consists of a high capacity relay with a MOSFET in parallel with it. The MOSFET has a varistor placed across it to provide protection, which is required when switching off inductive loads. This is because the stored energy in the inductor causes a high reverse voltage that could damage the MOSFET, if not protected.

When there is a control input command to operate an output contact the miniature relay is operated at the same time as the MOSFET. The miniature relay contact closes in nominally 3.5 ms and is used to carry the continuous load current. The MOSFET operates in less than 0.2 ms, but is switched off after 7.5 ms.

When the control input is reset, the MOSFET is again turned on for 7.5 mS. The miniature relay resets in nominally 3.5 ms before the MOSFET. This means the MOSFET is used to break the load. The MOSFET absorbs the energy when breaking inductive loads and so limits the resulting voltage surge. This contact arrangement is for switching DC circuits only.

The board number is:

- ZN0042 001

High Break Contact Operation

The following figure shows the timing diagram for High Break contact operation.

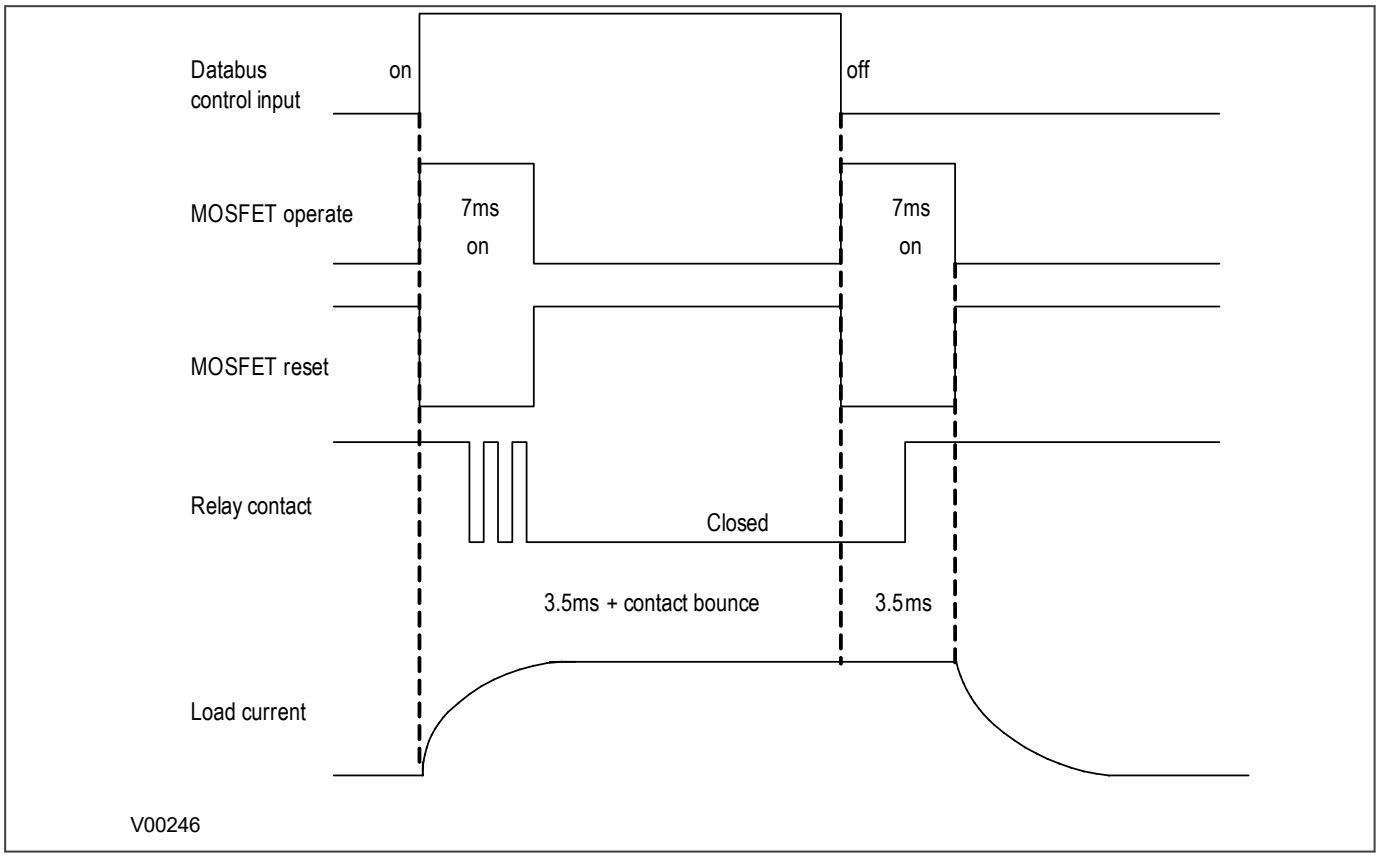


Figure 23: High Break contact operation

High Break Contact Applications

- Efficient scheme engineering

  In traditional hard wired scheme designs, High Break capability could only be achieved using external electromechanical trip relays. Instead, these internal High Break contacts can be used thus reducing space requirements.

- Accessibility of CB auxiliary contacts

  It is common practise to use circuit breaker 52a (CB Closed) auxiliary contacts to break the trip coil current on breaker opening, thereby easing the duty on the protection contacts. In some cases (such as operation of disconnectors, or retrofitting), it may be that 52a contacts are either unavailable or unreliable. In such cases, High Break contacts can be used to break the trip coil current in these applications.

- Breaker fail

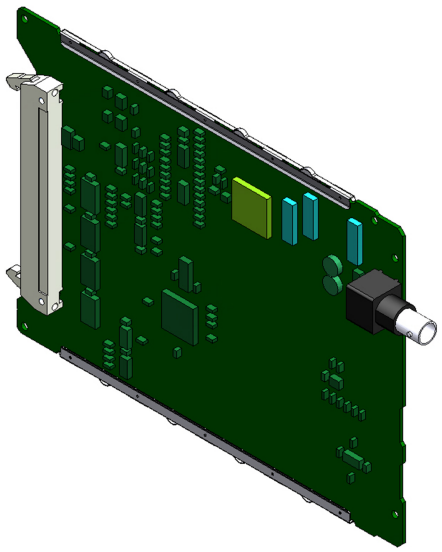
  In the event of failure of the local circuit breaker (stuck breaker), or defective auxiliary contacts (stuck contacts), it is incorrect to use 52a contact action. The interrupting duty at the local breaker then falls on the relay output contacts, which may not be rated to perform this duty. High Break contacts should be used in this case to avoid the risk of burning out relay contacts.

- Initiation of teleprotection

  The High Break contacts also offer fast making, which results in faster tripping. In addition, fast keying of teleprotection is a benefit. Fast keying bypasses the usual contact operation time, such that permissive, blocking and intertrip commands can be routed faster.

Warning:
These relay contacts are POLARITY SENSITIVE. External wiring must comply with the polarity requirements described in the external connection diagram to ensure correct operation.

3.6.8 IRIG-B BOARD



R00240

Figure 24: IRIG-B board

The IRIG-B board can be fitted to provide an accurate timing reference for the device. The IRIG-B signal is connected to the board via an BNC connector. The timing information is used to synchronise the IED's internal real-time clock to an accuracy of 1 ms. The internal clock is then used for time tagging events, fault, maintenance and disturbance records.

IRIG-B interface is available in modulated or demodulated formats.

The IRIG-B facility is provided in combination with other functionality on a number of additional boards, such as:

- Fibre board with IRIG-B
- Second rear communications board with IRIG-B
- Ethernet board with IRIG-B
- Redundant Ethernet board with IRIG-B

There are three types of each of these boards; one type which accepts a modulated IRIG-B input, one type which accepts a demodulated IRIG-B input and one type which accepts a universal IRIG-B input. The order code will indicate which variant it supports.

3.6.9 FIBRE OPTIC BOARD

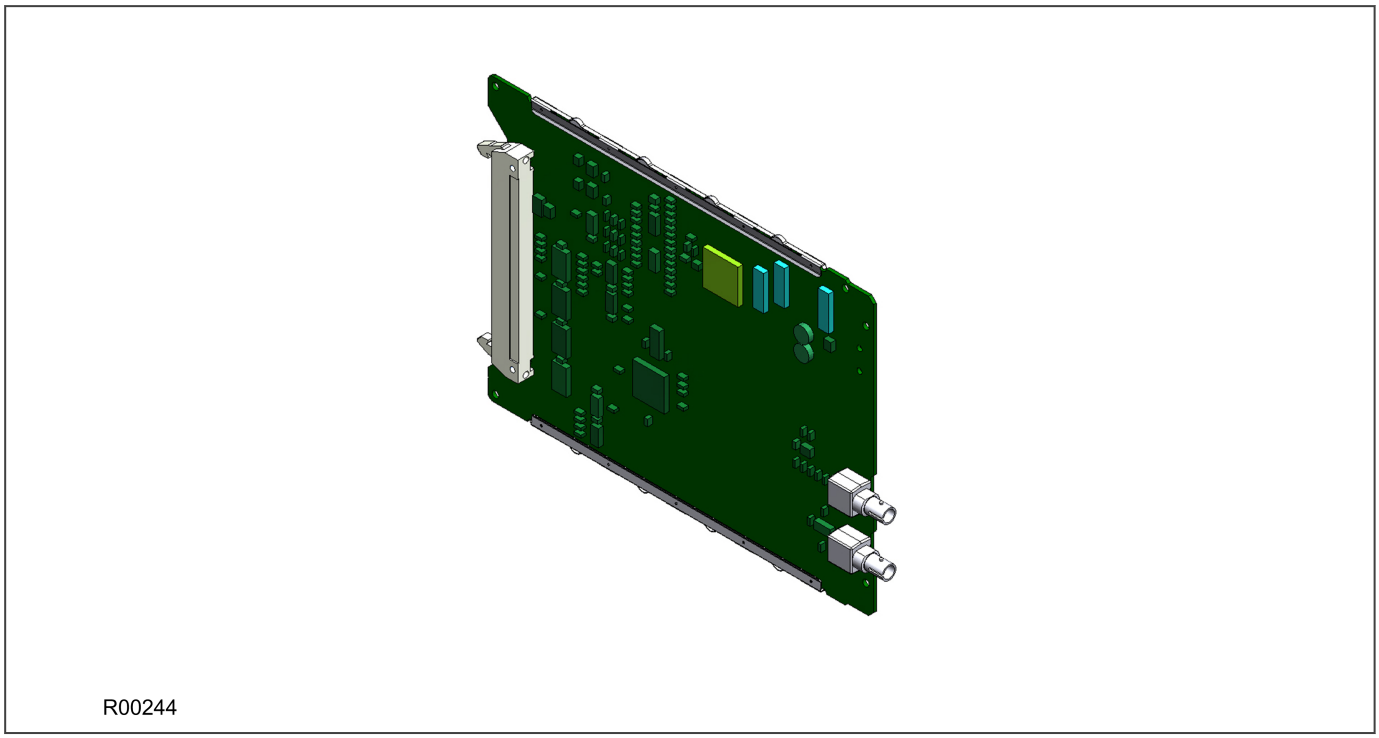


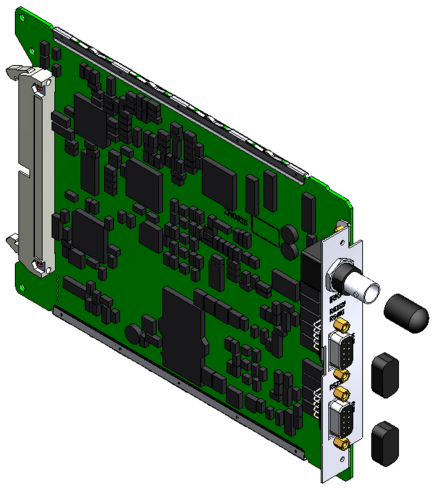
Figure 25: Fibre optic board

This board provides an interface for communicating with a master station. This communication link can use all compatible protocols (Courier, IEC 60870-5-103, MODBUS and DNP 3.0). It is a fibre-optic alternative to the metallic RS485 port presented on the power supply terminal block. The metallic and fibre optic ports are mutually exclusive.

The fibre optic port uses BFOC 2.5 ST connectors.

The board comes in two varieties; one with an IRIG-B input and one without:

3.6.10 REAR COMMUNICATION BOARD



R00243

Figure 26: Rear communication board

The optional communications board containing the secondary communication ports provide two serial interfaces presented on 9 pin D-type connectors. These interfaces are known as SK4 and SK5. Both connectors are female connectors, but are configured as DTE ports. This means pin 2 is used to transmit information and pin 3 to receive.

SK4 can be used with RS232, RS485 and K-bus. SK5 can only be used with RS232 and is used for electrical teleprotection. The optional rear communications board and IRIG-B board are mutually exclusive since they use the same hardware slot. However, the board comes in two varieties; one with an IRIG-B input and one without.

3.6.11 SINGLE ETHERNET BOARD

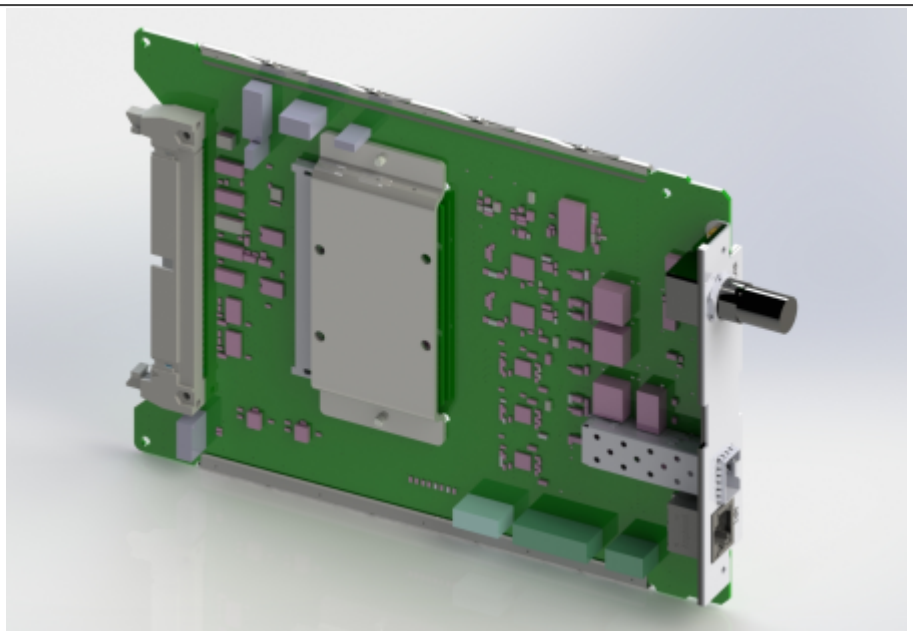


Figure 27: Ethernet board

This board provides one optical 100Mbps LC duplex Ethernet port (NP2A) for station bus communications, with a universal IRIG-B interface for time synchronisation, and a separate 10/100Mbps RJ45 Ethernet maintenance/ engineering interface (NP1) for monitoring and configuration purposes.

The Ethernet and other connection details are described below:

RJ45 Connector (NP1 only)

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

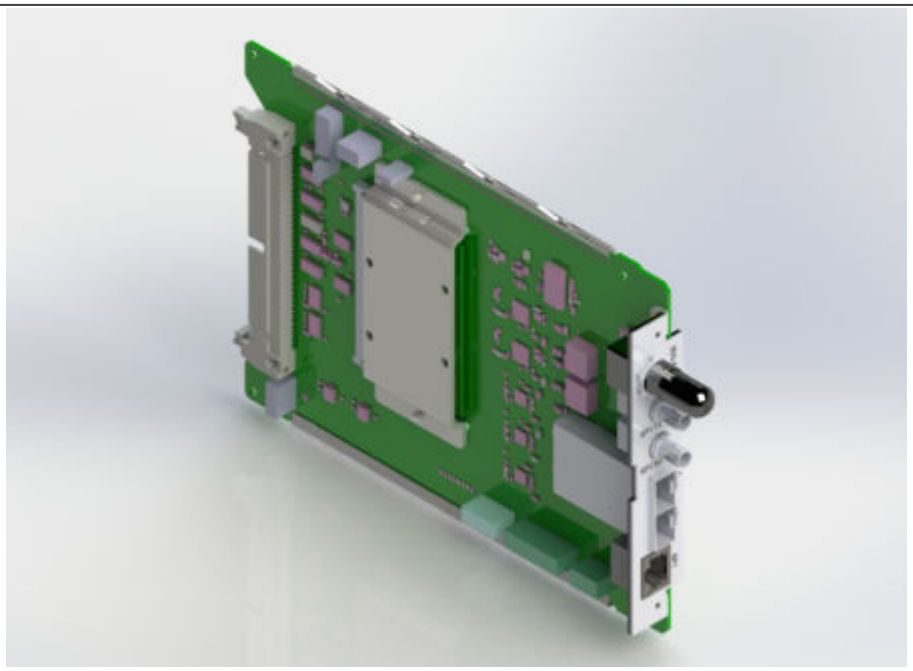
UNIVERSAL IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

LC Optical Fibre Connector (NP2A only)

Connector	SFP
A	TX
B	RX

3.6.12 REDUNDANT ETHERNET BOARD



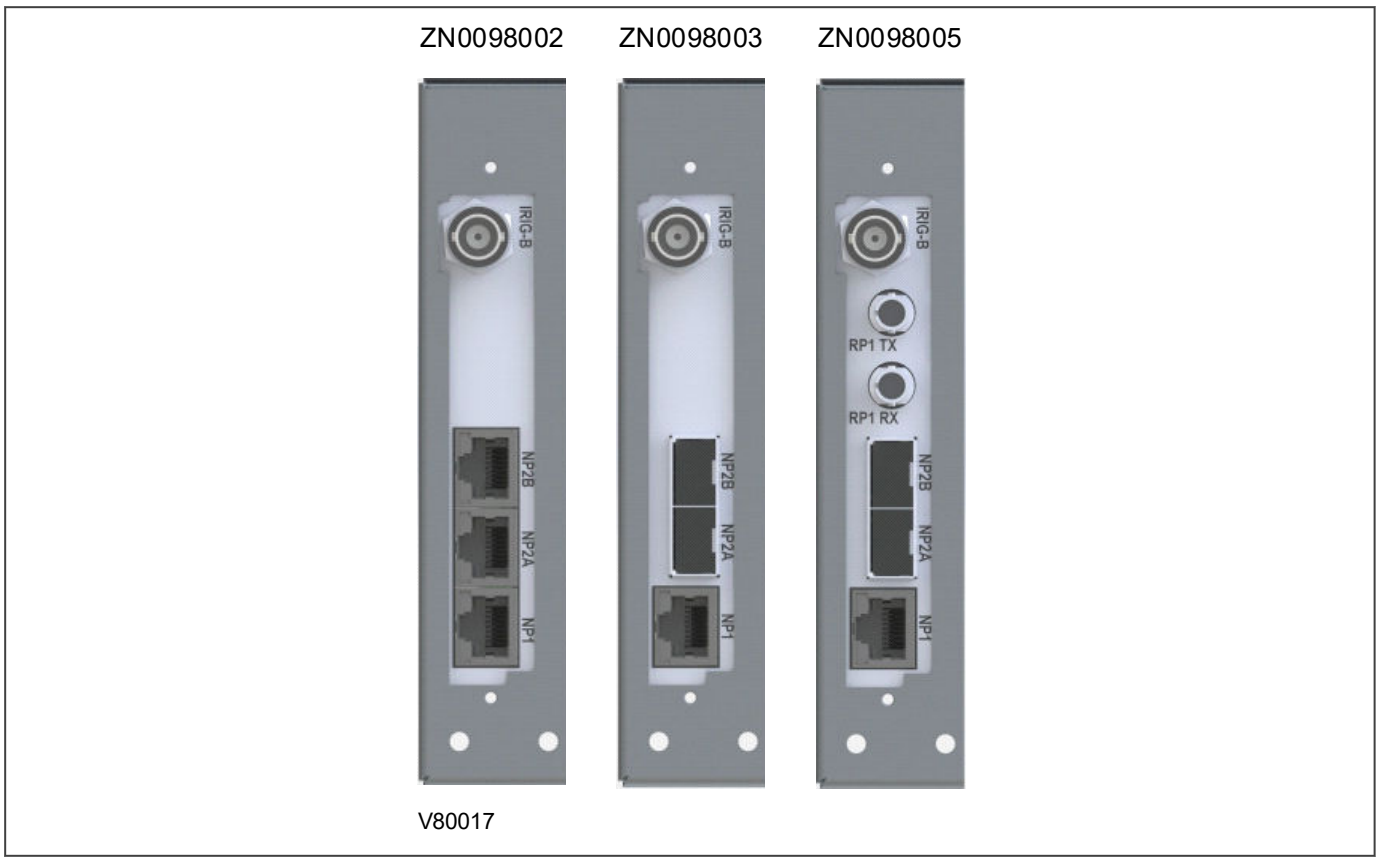


Figure 28: Redundant Ethernet board

This board provides dual redundant Ethernet (NP2A and NP2B) for station bus communications. A universal IRIG-B interface for time synchronisation and a separate Ethernet interface (NP1) for monitoring two variants. A new variant also provides serial protocol support on fiber optics (RP1).

The available redundancy protocols are:

- RSTP (Rapid Spanning Tree Protocol)
- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- Failover

There are several variants for this board as follows:

Two LC duplex redundant 100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with a serial protocol communications ST fibre port with on-board universal IRIG-B and one 10/100Mbps RJ45 maintenance/engineering port.

Two RJ45 duplex redundant 10/100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with on-board universal IRIG-B and one 10/100Mbps RJ45 maintenance/engineering port.

Two LC duplex redundant 100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with on-board universal IRIG-B and one 10/100Mbps RJ45 maintenance/engineering port.

The Ethernet and other connection details are described below:

UNIVERSAL IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

LC Optical Fibre Connector (only for NP2A or NP2B when ordering fibre ports on station bus ports)

Connector	SFP
A	TX
B	RX

ST Optical Fibre Connector (only for RP1 serial communications)

Connector	Communications
RP1	TX
RP2	RX

RJ45 Connector (NP1 or NP2A/NP2B when ordering two copper ports on station bus ports only)

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

CHAPTER 4

SOFTWARE DESIGN

4.1 CHAPTER OVERVIEW

This chapter describes the software design of the IED.

This chapter contains the following sections:

4.2 SOFWARE DESIGN OVERVIEW

The device software can be conceptually categorized into several elements as follows:

- The system level software
- The platform software
- The protection and control software

These elements are not distinguishable to the user, and the distinction is made purely for the purposes of explanation. The following figure shows the software architecture.

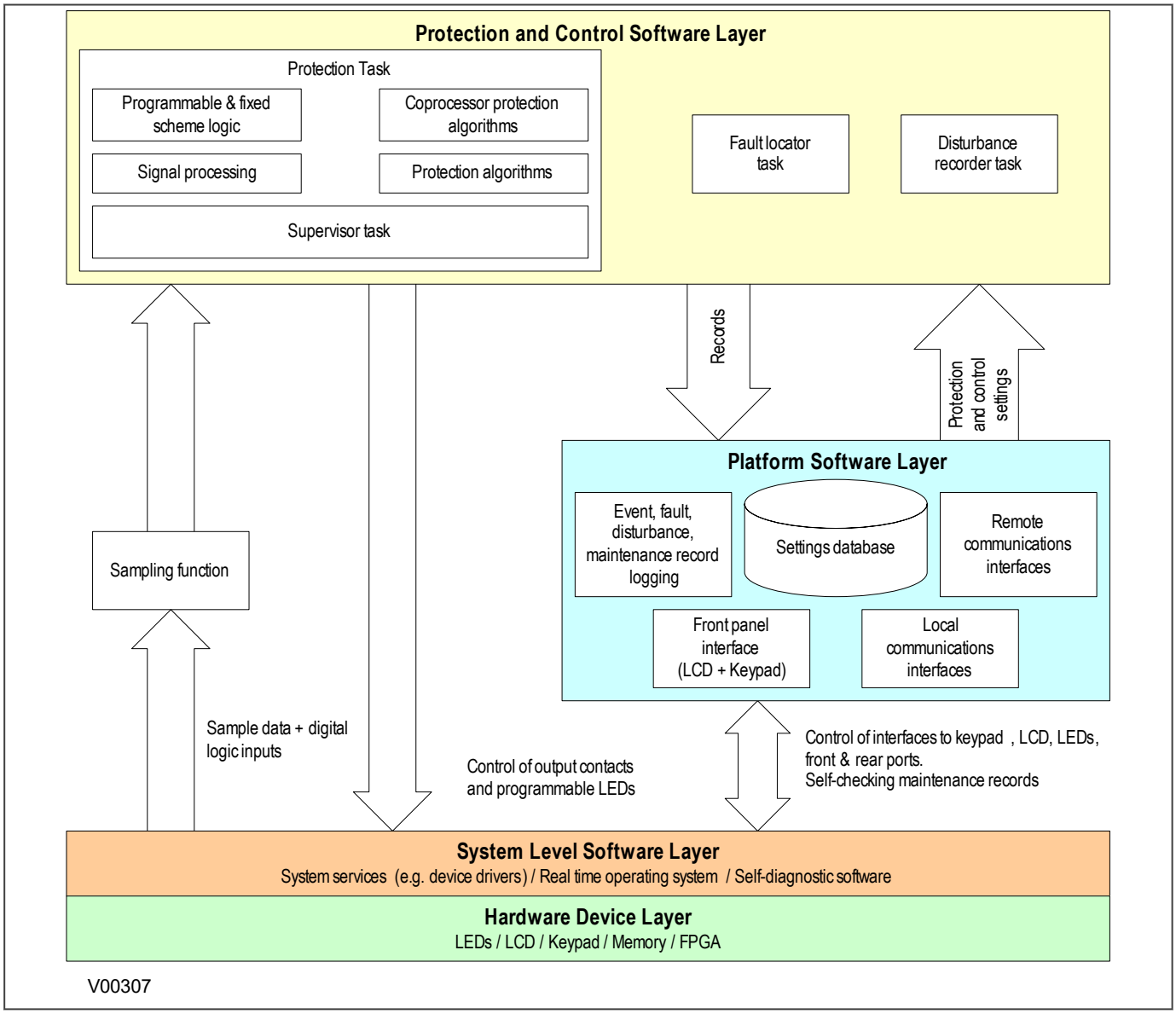


Figure 29: Software Architecture

The software, which executes on the main processor, can be divided into a number of functions as illustrated above. Each function is further broken down into a number of separate tasks. These tasks are then run according to a scheduler. They are run at either a fixed rate or they are event driven. The tasks communicate with each other as and when required.

4.3 SYSTEM LEVEL SOFTWARE

4.3.1 REAL TIME OPERATING SYSTEM

The real-time operating system is used to schedule the processing of the various tasks. This ensures that they are processed in the time available and in the desired order of priority. The operating system also plays a part in controlling the communication between the software tasks, through the use of operating system messages.

4.3.2 SYSTEM SERVICES SOFTWARE

The system services software provides the layer between the hardware and the higher-level functionality of the platform software and the protection and control software. For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports. It also controls things like the booting of the processor and the downloading of the processor code into DRAM at startup.

4.3.3 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the ‘Healthy’ LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the ‘Healthy’ LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

4.3.4 STARTUP SELF-TESTING

The self-testing takes a few seconds to complete, during which time the IEDs measurement, recording, control, and protection functions are unavailable. On a successful start-up and self-test, the ‘Healthy' state LED on the front of the device is switched on. If a problem is detected during the start-up testing, the device remains out of service until it is manually restored to working order.

The operations that are performed at start-up are:

1. System boot
2. System software initialisation
3. Platform software initialisation and monitoring

4.3.4.1 SYSTEM BOOT

The integrity of the Flash memory is verified using a checksum before the program code and stored data is loaded into DRAM for execution by the processor. When the loading has been completed, the data held in DRAM is compared to that held in the Flash memory to ensure that no errors have occurred in the data transfer and that the two are the same. The entry point of the software code in DRAM is then called. This is the IED's initialisation code.

4.3.4.2 SYSTEM LEVEL SOFTWARE INITIALISATION

The initialization process initializes the processor registers and interrupts, starts the watchdog timers (used by the hardware to determine whether the software is still running), starts the real-time operating system and creates and starts the supervisor task. In the initialization process the device checks the following:

- The status of the supercapacitor to maintain the real time clock
- The operation of the LCD controller
- The watchdog operation

At the conclusion of the initialization software the supervisor task begins the process of starting the platform software. Coprocessor board checks are also made as follows:

- A check is made for the presence of the coprocessor board
- The DRAM on the coprocessor board is checked

If any of these checks produces an error, the coprocessor board is left out of service. The other protection functions provided by the main processor board are left in service.

4.3.4.3 PLATFORM SOFTWARE INITIALISATION AND MONITORING

When starting the platform software, the IED checks the following:

- The integrity of the data held in non-volatile memory (using a checksum)
- The operation of the real-time clock
- The optional IRIG-B function (if applicable)
- The presence and condition of the input board
- The analog data acquisition system (it does this by sampling the reference voltage)

At the successful conclusion of all of these tests the unit is entered into service and the application software is started up.

4.3.5 CONTINUOUS SELF-TESTING

When the IED is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software and the results are reported to the platform software. The functions that are checked are as follows:

- The Flash memory containing all program code and language text is verified by a checksum.
- The code and constant data held in system memory is checked against the corresponding data in Flash memory to check for data corruption.
- The system memory containing all data other than the code and constant data is verified with a checksum.
- The integrity of the digital signal I/O data from the opto-inputs and the output relay coils is checked by the data acquisition function every time it is executed.
- The operation of the analog data acquisition system is continuously checked by the acquisition function every time it is executed. This is done by sampling the reference voltages.
- The operation of the optional Ethernet board is checked by the software on the main processor board. If the Ethernet board fails to respond an alarm is raised and the board is reset in an attempt to resolve the problem.
- The operation of the optional IRIG-B function is checked by the software that reads the time and date from the board.

In the event that one of the checks detects an error in any of the subsystems, the platform software is notified and it attempts to log a maintenance record.

If the problem is with the IRIG-B board, the device continues in operation. For problems detected in any other area, the device initiates a shutdown and re-boot, resulting in a period of up to 10 seconds when the functionality is unavailable.

A restart should clear most problems that may occur. If, however, the diagnostic self-check detects the same problem that caused the IED to restart, it is clear that the restart has not cleared the problem, and the device takes itself permanently out of service. This is indicated by the ‘’health-state’ LED on the front of the device, which switches OFF, and the watchdog contact which switches ON.

4.4 PLATFORM SOFTWARE

The platform software has three main functions:

- To control the logging of records generated by the protection software, including alarms, events, faults, and maintenance records
- To store and maintain a database of all of the settings in non-volatile memory
- To provide the internal interface between the settings database and the user interfaces, using the front panel interface and the front and rear communication ports

4.4.1 RECORD LOGGING

The logging function is used to store all alarms, events, faults and maintenance records. The records are stored in non-volatile memory to provide a log of what has happened. The IED maintains four types of log on a first in first out basis (FIFO). These are:

- Alarms
- Event records
- Fault records
- Maintenance records

The logs are maintained such that the oldest record is overwritten with the newest record. The logging function can be initiated from the protection software. The platform software is responsible for logging a maintenance record in the event of an IED failure. This includes errors that have been detected by the platform software itself or errors that are detected by either the system services or the protection software function. See the Monitoring and Control chapter for further details on record logging.

4.4.2 SETTINGS DATABASE

The settings database contains all the settings and data, which are stored in non-volatile memory. The platform software manages the settings database and ensures that only one user interface can modify the settings at any one time. This is a necessary restriction to avoid conflict between different parts of the software during a setting change. Changes to protection settings and disturbance recorder settings, are first written to a temporary location DRAM memory. This is sometimes called 'Scratchpad' memory. These settings are not written into non-volatile memory immediately. This is because a batch of such changes should not be activated one by one, but as part of a complete scheme. Once the complete scheme has been stored in DRAM, the batch of settings can be committed to the non-volatile memory where they will become active.

4.4.3 INTERFACES

The settings and measurements database must be accessible from all of the interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each of the interfaces (LCD display, keypad and all the communications interfaces).

4.5 PROTECTION AND CONTROL FUNCTIONS

The protection and control software processes all of the protection elements and measurement functions. To achieve this it has to communicate with the system services software, the platform software as well as organise its own operations.

The protection task software has the highest priority of any of the software tasks in the main processor board. This ensures the fastest possible protection response.

The protection and control software provides a supervisory task, which controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

4.5.1 ACQUISITION OF SAMPLES

After initialization, the protection and control task waits until there are enough samples to process. The acquisition of samples on the main processor board is controlled by a ‘sampling function’ which is called by the system services software.

This sampling function takes samples from the input module and stores them in a two-cycle FIFO buffer. These samples are also stored concurrently by the coprocessor. The sample rate is 48 samples per cycle. This results in a nominal sample rate of 2,400 samples per second for a 50 hz system and 2,880 samples per second for a 60 Hz system. However the sample rate is not fixed. It tracks the power system frequency as described in the next section.

In normal operation, the protection task is executed 16 times per cycle.

4.5.2 FREQUENCY TRACKING

The device provides a frequency tracking algorithm so that there are always 48 samples per cycle irrespective of frequency drift. The frequency range in which 48 samples per second are provided is between 45 Hz and 66 Hz. If the frequency falls outside this range, the sample rate reverts to its default rate of 2,400 Hz for 50 Hz or 2,880 Hz for 60 Hz.

The frequency tracking of the analog input signals is achieved by a recursive Fourier algorithm which is applied to one of the input signals. It works by detecting a change in the signal’s measured phase angle. The calculated value of the frequency is used to modify the sample rate being used by the input module, in order to achieve a constant sample rate per cycle of the power waveform. The value of the tracked frequency is also stored for use by the protection and control task.

The frequency tracks off any voltage or current in the order VA, VB, VC, IA, IB, IC, down to 10%Vn for voltage and 5%In for current.

4.5.3 DIRECT USE OF SAMPLED VALUES

Most of the IED’s protection functionality uses the Fourier components calculated by the device’s signal processing software. However RMS measurements and some special protection algorithms available in some products use the sampled values directly.

The disturbance recorder also uses the samples from the input module, in an unprocessed form. This is for waveform recording and the calculation of true RMS values of current, voltage and power for metering purposes.

In the case of special protection algorithms, using the sampled values directly provides exceptionally fast response because you do not have to wait for the signal processing task to calculate the fundamental. You can act on the sampled values immediately.

4.5.4 SYSTEM LEVEL SOFTWARE INITIALISATION

The differential protection requires that the devices at the line ends exchange data messages four times per cycle. To achieve this the coprocessor retrieves the frequency-tracked samples at 48 samples per cycle from the input

board and converts these to 8 samples per cycle based on the nominal frequency. The coprocessor calculates the Fourier transform of the fixed rate samples after every sample, using a one-cycle window. This generates current measurements eight times per cycle which are used for the differential protection algorithm. These are transmitted to the remote device(s) using the HDLC (high-level data link control) communication protocol.

The coprocessor is also responsible for managing intertripping commands via the communication link, as well as re-configuration instigated from the remote device(s).

Data exchange between the coprocessor board and the main processor board is achieved through the use of shared memory on the coprocessor board. When the main processor accesses this memory, the coprocessor is temporarily halted. After the coprocessor code has been copied onto the board at initialization, the main traffic between the two boards consists of setting change information, commands from the main processor, differential protection measurements and output data.

4.5.5 DISTANCE PROTECTION

The current and voltage inputs are filtered using Finite Impulse Response (FIR) digital filters. This reduces the effects of non-power frequency components in the input signals, such as DC offsets in current waveforms, and capacitor voltage transformer (CVT) transients in the voltages. The device uses a combination of a 1/4 cycle filter using 12 coefficients, a 1/2 cycle filter using 24 coefficients, and a single cycle filter using 48 coefficients. The device automatically performs intelligent switching in the application of the filters, to select the best balance of removal of transients with fast response. The protection elements themselves then perform additional filtering, implemented for example, by the trip count strategy.

The following figure shows the frequency response of the 12, 24 and 48 coefficient filters, noting that all have a gain of unity at the fundamental frequency:

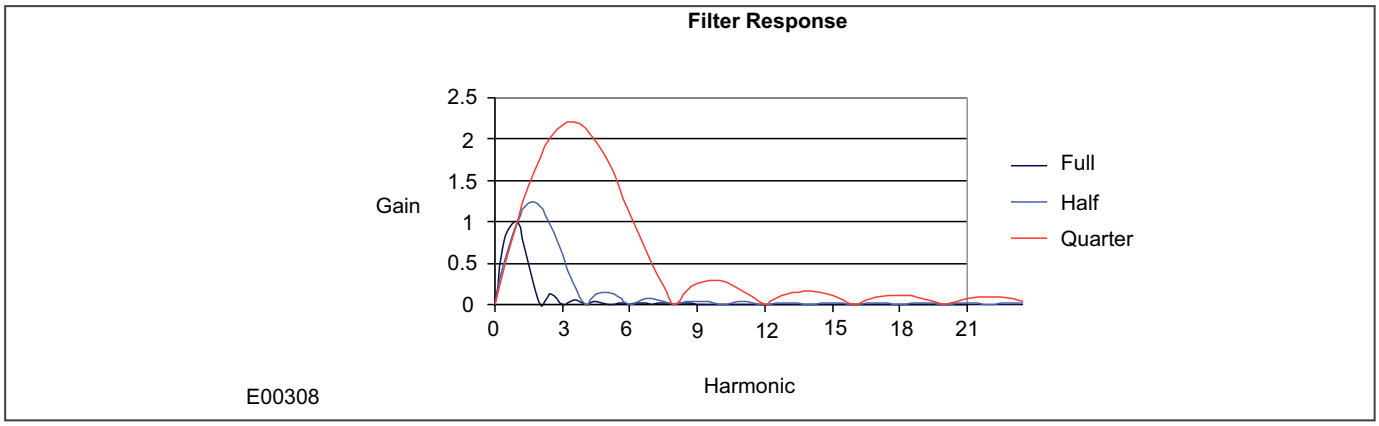


Figure 30: Frequency response of FIR filters

4.5.6 FOURIER SIGNAL PROCESSING

All backup protection and measurement functions use single-cycle fourier digital filtering to extract the power frequency component. This filtering is performed on the main processor board.

When the protection and control task is re-started by the sampling function, it calculates the Fourier components for the analog signals. Although some protection algorithms use some Fourier-derived harmonics (e.g. second harmonic for magnetizing inrush), most protection functions are based on the Fourier-derived fundamental components of the measured analog signals. The Fourier components of the input current and voltage signals are stored in memory so that they can be accessed by all of the protection elements' algorithms.

The Fourier components are calculated using single-cycle Fourier algorithm. This Fourier algorithm always uses the most recent 48 samples from the 2-cycle buffer.

Most protection algorithms use the fundamental component. In this case, the Fourier algorithm extracts the power frequency fundamental component from the signal to produce its magnitude and phase angle. This can be represented in either polar format or rectangular format, depending on the functions and algorithms using it.

The Fourier function acts as a filter, with zero gain at DC and unity gain at the fundamental, but with good harmonic rejection for all harmonic frequencies up to the nyquist frequency. Frequencies beyond this nyquist frequency are known as alias frequencies, which are introduced when the sampling frequency becomes less than twice the frequency component being sampled. However, the Alias frequencies are significantly attenuated by an anti-aliasing filter (low pass filter), which acts on the analog signals before they are sampled. The ideal cut-off point of an anti-aliasing low pass filter would be set at:

$$(\text{samples per cycle}) \times (\text{fundamental frequency})/2$$

At 48samples per cycle, this would be nominally 1200 Hz for a 50 Hz system, or 1440 Hz for a 60 Hz system.

The following figure shows the nominal frequency response of the anti-alias filter and the Fourier filter for a 48-sample single cycle fourier algorithm acting on the fundamental component:

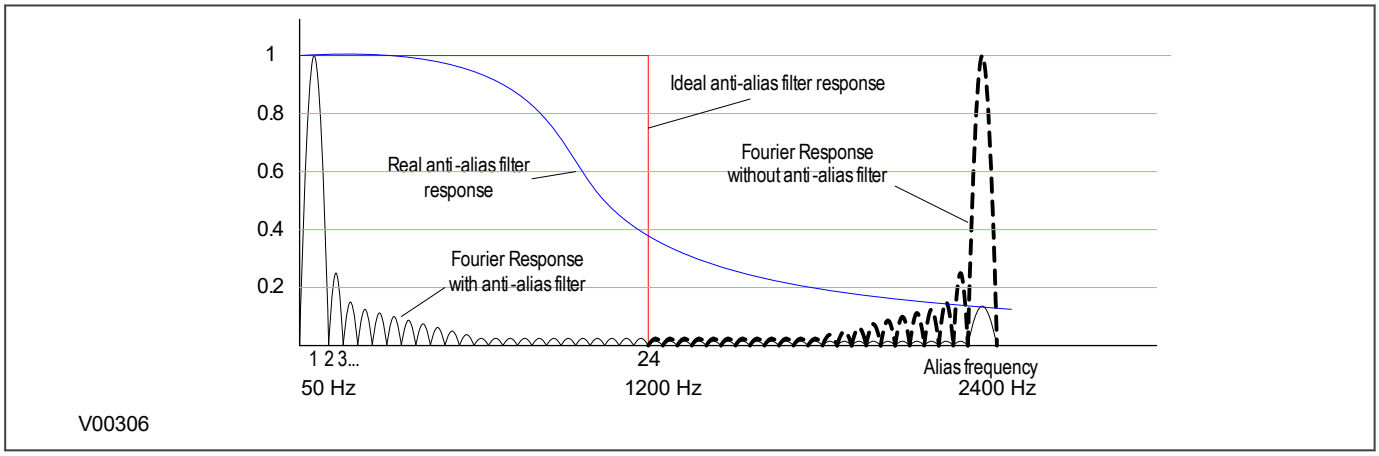


Figure 31: Frequency Response (indicative only)

4.5.7 PROGRAMMABLE SCHEME LOGIC

The purpose of the programmable scheme logic (PSL) is to allow you to configure your own protection schemes to suit your particular application. This is done with programmable logic gates and delay timers. To allow greater flexibility, different PSL is allowed for each of the four setting groups.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements such as protection starts and trips, and the outputs of the fixed protection scheme logic (FSL). The fixed scheme logic provides the standard protection schemes. The PSL consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, such as to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven. The logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection & control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

The PSL can be configured to create very complex schemes. Because of this PSL design is achieved by means of a PC support package called the PSL Editor. This is available as part of the settings application software MiCOM S1 Agile.

4.5.8 EVENT RECORDING

A change in any digital input signal or protection element output signal is used to indicate that an event has taken place. When this happens, the protection and control task sends a message to the supervisor task to indicate that

an event is available to be processed and writes the event data to a fast buffer controlled by the supervisor task. Up to 5000 time-tagged event records can be stored.

When the supervisor task receives an event record, it instructs the platform software to create the appropriate log in non-volatile memory (DRAM). The operation of the record logging to Flash is slower than the supervisor buffer. This means that the protection software is not delayed waiting for the records to be logged by the platform software. However, in the rare case when a large number of records to be logged are created in a short period of time, it is possible that some will be lost, if the supervisor buffer is full before the platform software is able to create a new log in Flash memory. If this occurs then an event is logged to indicate this loss of information.

Maintenance records are created in a similar manner, with the supervisor task instructing the platform software to log a record when it receives a maintenance record message. However, it is possible that a maintenance record may be triggered by a fatal error in the relay in which case it may not be possible to successfully store a maintenance record, depending on the nature of the problem.

For more information, see the Monitoring and Control chapter.

4.5.9 DISTURBANCE RECORDER

The disturbance recorder operates as a separate task from the protection and control task. It can record the waveforms for up to 30 calibrated analogue channels and values of up to 32 digital signals all at a high resolution of 24 samples/cycle. The recording time is user selectable. Typically, 100 waveforms of 10.5 seconds duration can be stored. The disturbance recorder is supplied with data by the protection and control task once per cycle. The disturbance recorder collates the data that it receives into the required length disturbance record. The disturbance records can be extracted by settings application software such as S1 Agile, which can also store the data in COMTRADE format, therefore allowing the use of other packages to view the recorded data.

For more information, see the Monitoring and Control chapter.

4.5.10 FAULT LOCATOR

The fault locator uses 12 cycles of the analog input signals to calculate the fault location. The result is returned to the protection and control task, which includes it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record. When the fault record is complete, including the fault location, the protection and control task sends a message to the supervisor task to log the fault record.

The Fault Locator is not available on all models.

4.5.11 FUNCTION KEY INTERFACE

The function keys interface directly into the PSL as digital input signals. A change of state is only recognized when a key press is executed on average for longer than 200 ms. The time to register a change of state depends on whether the function key press is executed at the start or the end of a protection task cycle, with the additional hardware and software scan time included. A function key press can provide a latched (toggled mode) or output on key press only (normal mode) depending on how it is programmed. It can be configured to individual protection scheme requirements. The latched state signal for each function key is written to non-volatile memory and read from non-volatile memory during relay power up thus allowing the function key state to be reinstated after power-up, should power be inadvertently lost.

CHAPTER 5

CONFIGURATION

5.1 CHAPTER OVERVIEW

Each product has different configuration parameters according to the functions it has been designed to perform. There is, however, a common methodology used across the entire product series to set these parameters.

Some of the communications setup cannot be carried out using the settings applications software, it can only be carried out using the HMI. This chapter includes concise instructions on how to configure the device, as well as a description of the common methodology used to configure the device in general.

This chapter contains the following sections:

5.2 SETTINGS APPLICATION SOFTWARE

To configure this device, you will need to use the Settings Application Software. The settings application software used in this range of IEDs is called MiCOM S1 Agile. It is a collection of software tools, which is used for setting up and managing the IEDs.

Although you can change many settings using the front panel HMI, some of the features cannot be configured without the Settings Application Software. For example, the programmable scheme logic, or the IEC 61850 communications or the SLD.

If you do not already have a copy of the Settings Application Software, you can obtain it from GE Vernova contact centre.

To configure your product, you will need a data model that matches your product. When you launch the Settings Application Software, you will be presented with a panel that allows you to invoke the “Data Model Manager”. This will close the other aspects of the software to allow an efficient import of the chosen data model. If you don’t have, or can’t find, the data model relating to your product, please call the GE Vernova contact centre.

When you have loaded all the data models you need, you should restart the Settings Application Software and start to create a model of your system using the “System Explorer” panel.

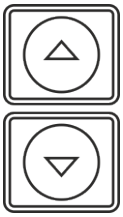
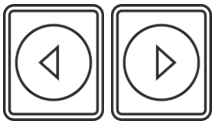
The software is designed to be intuitive, but help is available in an online help system and in the Settings Application Software user guide P40-M&CR-SAS-UG-EN-n, where 'Language' is a 2-letter code designating the language version of the user guide and 'n' is the latest version of the settings application software.

5.3 USING THE HMI PANEL

Using the Graphical HMI, you can:

- Display and modify settings
- Display measurements
- Display fault records
- Display the Single Line Diagram (SLD)
- View the digital I/O signal status
- Reset fault and alarm indications

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the screen.

Keys	Description	Function
	Up and down cursor keys	To change between settings in a particular column, changing values within a cell or to select the next item on the SLD
	Left and right cursor keys	To change between settings in a particular column, change values within a cell or to select the next item on the SLD
	ENTER/OK key	For changing and executing settings. When a bottom banner Menu context key label is selected, the OK key can also be used to navigate between pages.
	Menu context keys	Menu context keys situated directly below the graphical HMI are used to navigate between pages.
	Cancel/Reset key	To return to the menu header from any menu cell, or to cancel a setting input.
	Read/Home key	To navigate to the default Home page from anywhere in the menu.
	Function keys (not all models)	For executing user programmable functions

Keys	Description	Function
	Control key OPEN	Control key OPEN used to open the CB/Switch. **Note:** Colour coding is selectable via labels and configuration of PSL/SLD.
	Control key CLOSE	Control key CLOSE used to close the CB/Switch. **Note:** Colour coding is selectable via labels and configuration of PSL/SLD.
	Local/Remote key	To select between local and remote operating modes.

5.3.1 NAVIGATING THE HMI PANEL

The cursor keys are used to navigate the menu. To navigate between different menus, use the Menu context keys, which are located below the graphical display.

The cursor keys have an auto-repeat function if held down continuously. This can be used to speed up both setting value changes and menu navigation. The longer the key is held down, the faster the rate of change or movement.

5.3.2 GETTING STARTED

When you first start the IED, it will go through its power up procedure. After a few seconds it will settle down into the default display. If there are alarms present, the yellow Alarms LED will be flashing and the alarm counter on the top banner will show the number of alarms that are active.

The device should be in full working order when you first start it, but an alarm could still be present. For example, if there is no network connection for a device fitted with a network board. If this is the case, you can read the alarm by selecting the Alarm counter on the top banner of the display.

If the device is fitted with an Ethernet board, you will need to connect the device to an active Ethernet network to clear the alarm.

5.3.3 DEFAULT DISPLAY

The graphical HMI default display contains shortcuts to various sections of the menu, as well as a snapshot of the current device status.

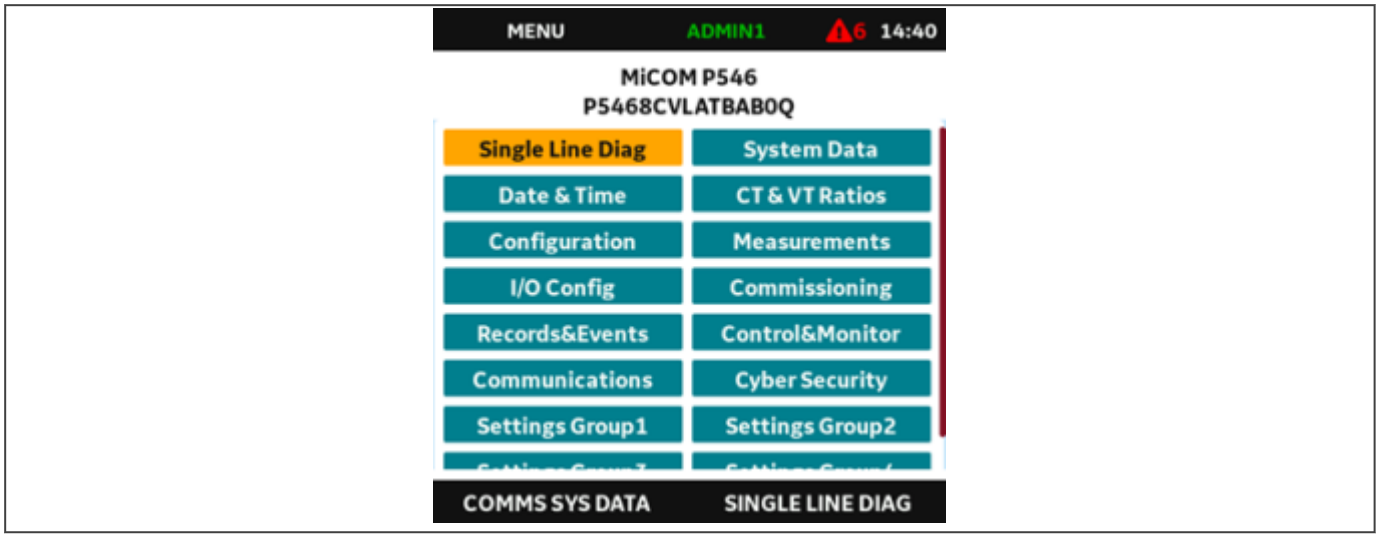


Figure 32: HMI Default Display

The graphical display screen consists of three main areas, which can be selected using the navigation keypad.

1. The top banner displays information left to right and includes the menu label for the current display, the user access level, the number of active alarms and the time.
2. The content area displays information related to the chosen area of navigation. For example, settings, measurements or SLD.
3. The bottom banner displays labels for the two Menu context keys, which are used for navigating between the menus.

Note:
After a period defined by the "LCD screen saver" , setting the HMI will enter rest mode. This allows the HMI to reduce power consumption and will dim the LCD backlight. The HMI may be woken from rest mode by pressing any front panel key. This mode has no effect on IED functional performance.

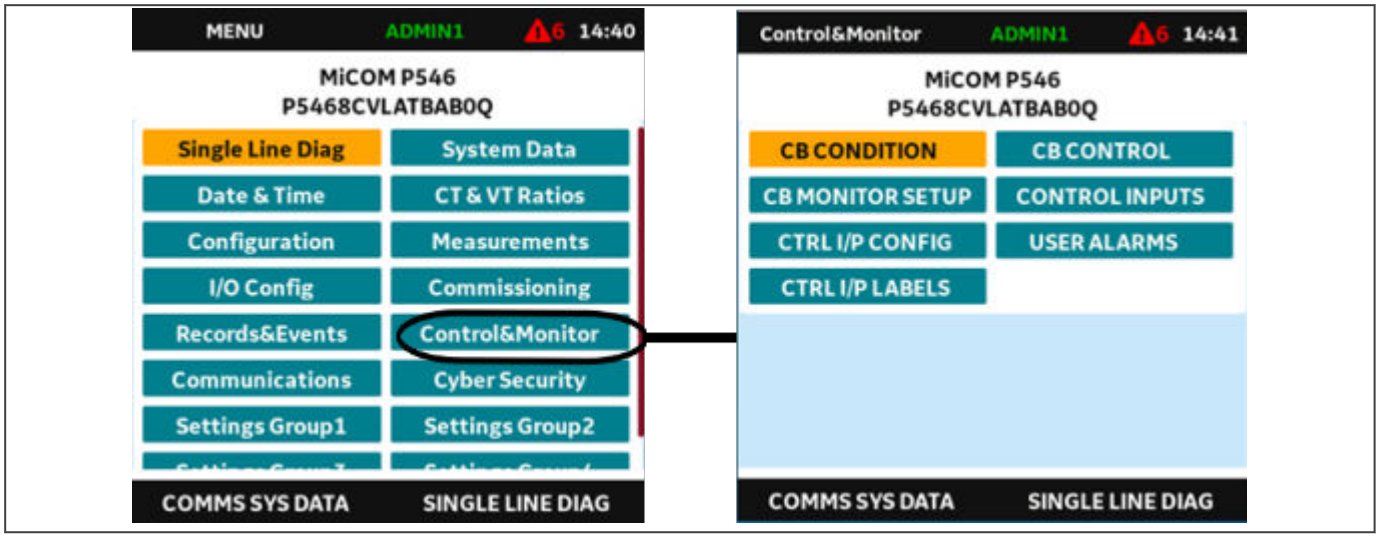
5.3.4 DEFAULT DISPLAY NAVIGATION

The default display provides quick and simple navigation of the complete menu database. Use the navigation keypad to change the highlighted cell. The highlighted entry can be selected using the Enter/OK Key. When the bottom of the screen is reached, the selected area moves to the Bottom Banner. From here the OK key can also be used to navigate between the pages.

The Menu view can be directly navigated to by long pressing the "Read/Home" key.

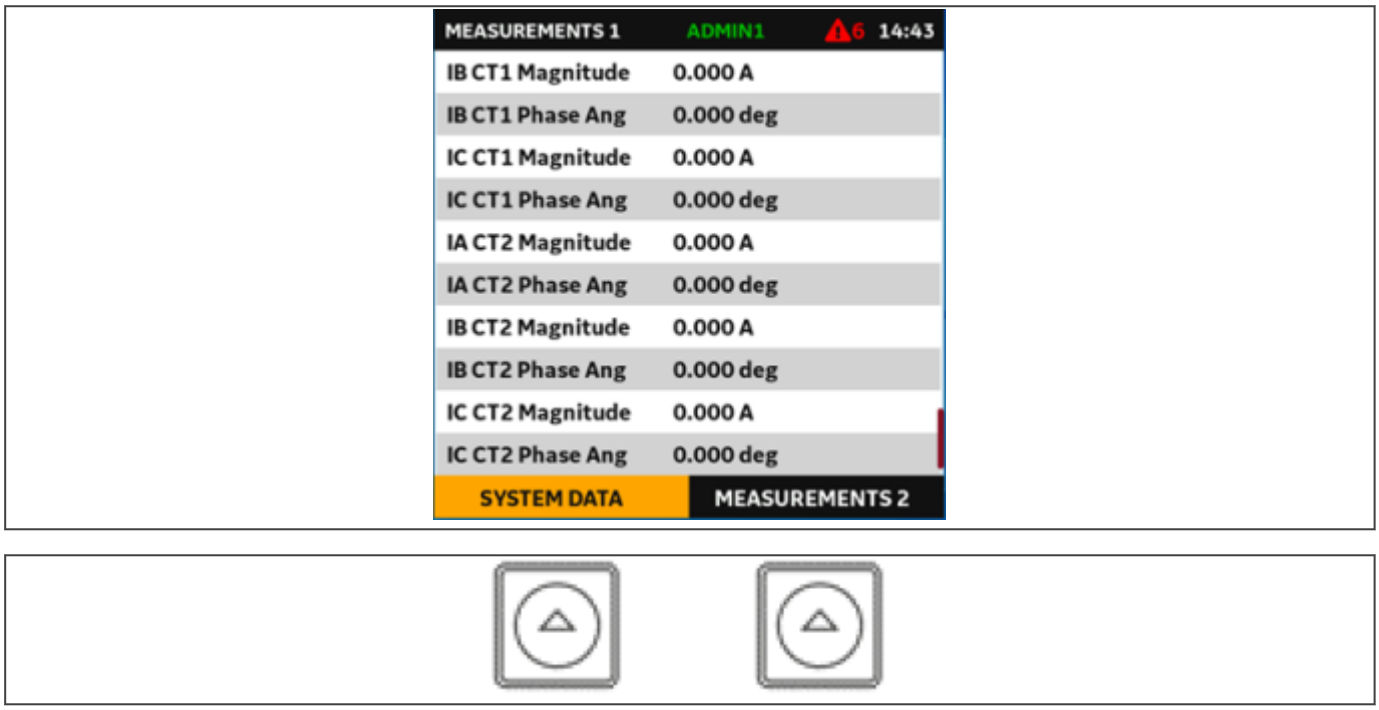
Previous level in the navigation hierarchy may be reached by pressing the "Cancel/Reset" key.

From the HMI Default Display, you can navigate to the required view or open up a Submenu using hierarchical navigation. For example, by selecting Controls & Monitor, a Submenu is opened.



As an alternative to hierarchical navigation, the views may be navigated to in sequence by using the hot keys as “Next” and “Previous” buttons, and is referred as horizontal navigation.

For example, you can move to either ***SYSTEM DATA*** or ***MEASUREMENTS 2*** Views using the horizontal navigation, menu contexts hot keys situated directly under the screen.



5.3.5 PROCESSING ALARMS AND RECORDS

When there are no alarms, the Alarm Icon on the top banner is shown as:

While there are any standing alarms, the standing alarm count will be highlighted in red in the top HMI banner and the yellow alarm LED will flash.

To launch the alarm list view, select the alarm counter in the HMI top banner and press the **OK** key. The alarm view list may be scrolled to view all alarms.

New standing and fleeting alarms may be accepted by selecting the alarm and pressing the **Ack/Clear** menu context key. Rescinded alarms may also be cleared by selecting the alarm and pressing the **Ack/Clear** menu context key.

All visible alarms may be selected by pressing the **Select All** menu context key.

The "*reset indication*" command may be issued to reset latched alarms and accept the flashing led notification. A "*reset indication*" may be issued from the "*View Records*" HMI settings view or by pressing **Ack/Clear** alarm context key.

"*Ack/Clear*" and "*reset indication*" commands are available to users with ENGINEER or OPERATOR or INSTALLER roles.

To return to the launch view from the alarm view press the **Cancel** key.

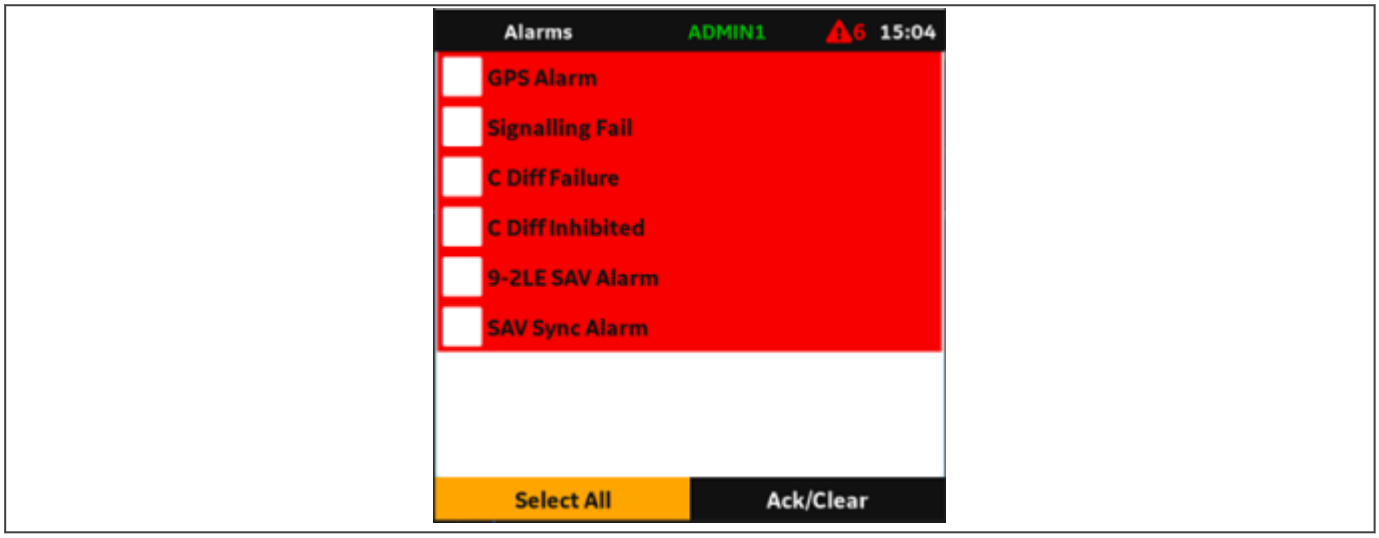


Figure 33: HMI Alarms Display

5.3.6 SINGLE LINE DIAGRAM (SLD) VIEWER

The SLD menu displays the saved SLD on the graphical HMI screen. You can navigate to the SLD menu using the bottom Menu context keys or by using the quick launch menu on the Home page. The SLD is configured and uploaded into the IED using the S1 Agile configuration tool. Items of plant can be selected on the SLD screen using the navigation keypad.

5.3.6.1 CIRCUIT BREAKER CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the circuit breaker selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the ***CB Control by*** setting is selected, to option 1 *Local*, option 3 *Local+Remote*, option 5 *Opto+local*, option 7 *Opto+Rem+local* or option 8 *L/R Key* in the *CB CONTROL* column users are allowed to use the Trip and Close Key on the front panel to operate the CB.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***CB control by*** setting to *L/R Key*
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R

Key LED is green and the REMOTE mode is selected. ***The L/R Key Status*** DDB status is stored in non-volatile memory, so that it's status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant which you require to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the Open or Close key to operate

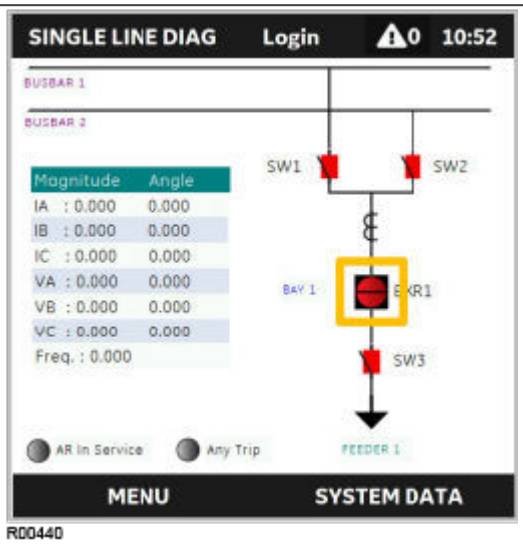


Figure 34: HMI SLD Display

For the Circuit Breaker Commands from HMI, additional checks are done:

If the CB is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "Control by" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "Control by" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "Control by" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - In Remote Control".

If the associated local DDB is set to local, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

5.3.6.2 SWITCH CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the switches selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the Switch Control by setting is selected to option 1 *LOCAL*, option 3 `Local+Remote` or option 4 `L/R Key` in the SWITCH CONTROL column, users are allowed to use the Open and Close Key on the front panel to operate the SWITCH.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***Switch Control by*** setting to `L/R Key`
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R

Key LED is green and the REMOTE mode is selected. The **L/R Key Status** DDB status is stored in non-volatile memory, so that its status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant you want to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the OPEN or CLOSE key to operate

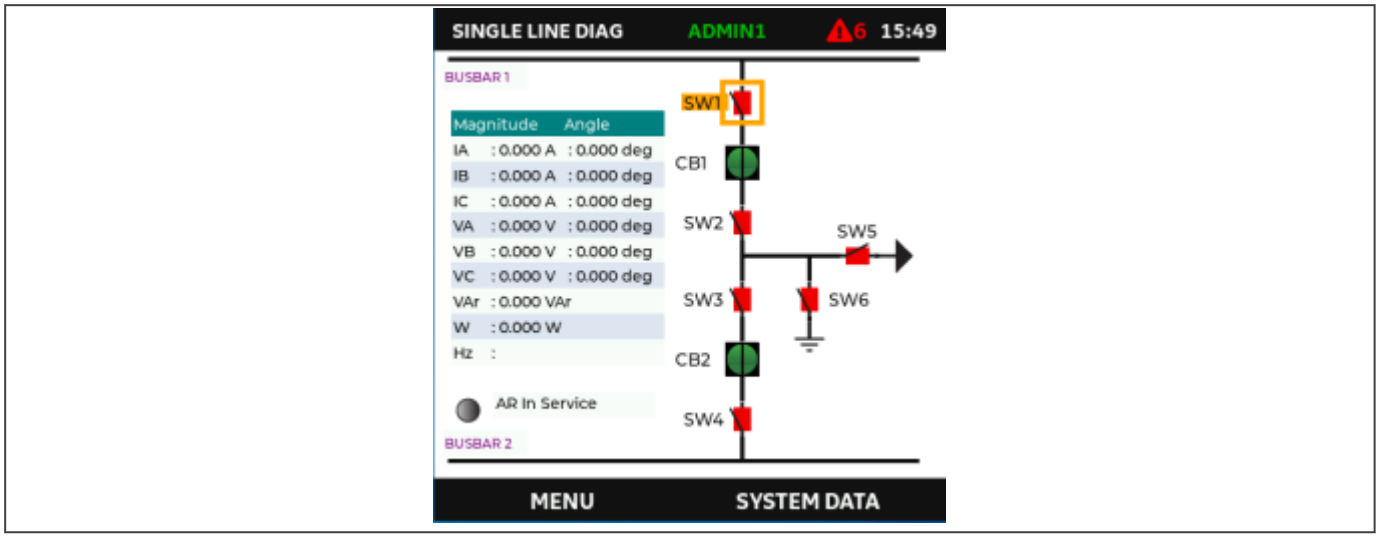


Figure 35: HMI SLD display

Figure 36: For the Switch Commands from HMI, these additional checks are done:

If the Switch is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "***Control by***" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - In Remote Control."

If the associated local DDB is set to local, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

5.3.7 MENU STRUCTURE

Settings, commands, records and measurements are stored in a local database inside the IED. When using the Human Machine Interface (HMI) it is convenient to visualise the menu navigation system as a table. Each item in the menu is known as a cell, which is accessed by reference to a column and row address. Each column and row is assigned 2-digit hexadecimal numbers, resulting in a unique 4-digit cell address for every cell in the database. The main menu groups are allocated columns and the items within the groups are allocated rows, meaning a particular item within a particular group is a cell.

You do not need to scroll through each of the columns horizontally to access a specific setting view. The ‘Home Page’ can be used to quickly access the required column/setting view. Each column contains all related items, for example all of the disturbance recorder settings and records are in the same column.

There are three types of cell:

- Settings: this is for parameters that can be set to different values
- Commands: this is for commands to be executed
- Data: this is for measurements and records to be viewed, which are not settable

Note:
Sometimes the term "Setting" is used generically to describe all of the three types.

The table below, provides an example of the menu structure:

SYSTEM DATA (Col 00)	VIEW RECORDS (Col 01)	MEASUREMENTS 1 (Col 02)	…
Language (Row 01)	"Select Event [0...n]" (Row 01)	IA Magnitude (Row 01)	…
Password (Row 02)	Menu Cell Ref (Row 02)	IA Phase Angle (Row 02)	…
Sys Fn Links (Row 03)	Time & Date (Row 03)	IB Magnitude (Row 03)	…
…	…	…	…

It is convenient to specify all the settings in a single column, detailing the complete Courier address for each setting. The above table may therefore be represented as follows:

Setting	Column	Row	Description
SYSTEM DATA	**00**	**00**	**First Column definition**
Language (Row 01)	00	01	First setting within first column
Password (Row 02)	00	02	Second setting within first column
Sys Fn Links (Row 03)	00	03	Third setting within first column
…	…	…	
VIEW RECORDS	**01**	**00**	**Second Column definition**
Select Event [0...n]	01	01	First setting within second column
Menu Cell Ref	01	02	Second setting within second column
Time & Date	01	03	Third setting within second column
…	…	…	
MEASUREMENTS 1	**02**	**00**	**Third Column definition**
IA Magnitude	02	01	First setting within third column
IA Phase Angle	02	02	Second setting within third column
IB Magnitude	02	03	Third setting within third column
…	…	…	

The first three column headers are common throughout much of the product ranges. However, the rows within each of these column headers may differ according to the product type. Many of the column headers are the same for all products within the series. However, there is no guarantee that the addresses will be the same for a particular column header. Therefore, you should always refer to the product settings documentation and not make any assumptions.

5.3.8 DIRECT ACCESS (MENU CONTEXT KEYS)

The IED provides a pair of menu context keys directly below the LCD display, which allows scrolling between column headings (navigation between menu screens). These keys can be pressed at any time during menu navigation to quickly access the menu label displayed in the bottom banner of the graphical HMI.

5.3.8.1 CONTROL INPUTS

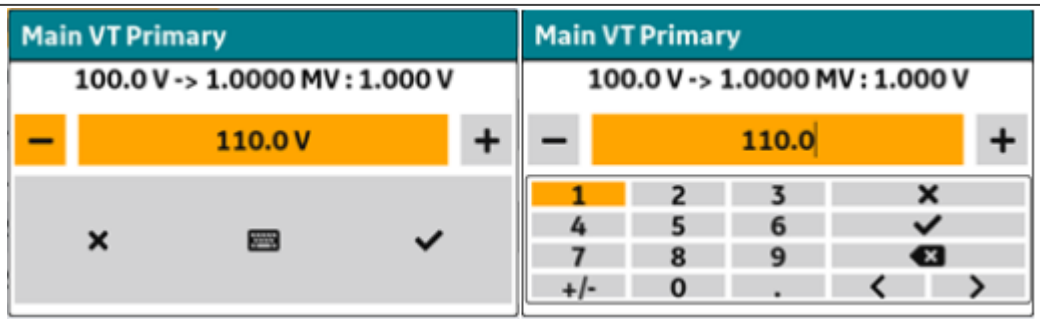
Control inputs cannot be operated through the Menu context keys. To operate control inputs, navigate to the Control Inputs settings view on the front graphical HMI screen, select the relevant control input and Set/Reset as required. RBAC is now applied to access control inputs for operation.

5.3.9 CHANGING THE SETTINGS

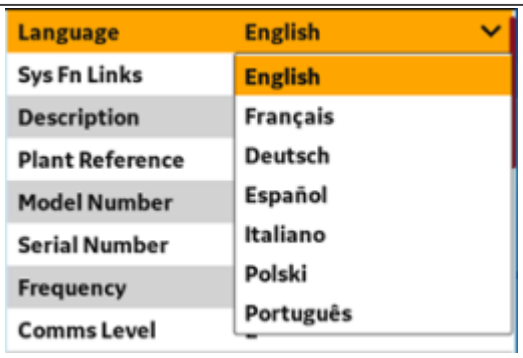
Appropriate user authority or bypass access is required to change the Settings. Please refer to the Cyber Security chapter for user authority details.

- Starting at the default display, highlight the required settings column/menu
- Use the OK key to enter the highlighted settings menu.
- To change the value of a setting, highlight the relevant cell in the menu, then press the **Enter** key to change the cell value. A settings screen will appear next to the cell. If the currently logged in user does not have the level of access required for changing the setting, a pop-up dialog box will inform the user and prevent the settings from being changed. Acknowledge the pop-up message, then navigate to the 'user accounts' section to the top of the screen (top banner) to enter the password for the required access level to change settings.
- To change the value on the settings screen, use the cursor keys to change the desired settings. When more settings are available than can fit on the screen, a scroll bar on the right-hand side appears. In some cases, a virtual keyboard is provided to enter complex characters. The IED maintains dependencies between various settings, and only the applicable settings are displayed for changing.

For Analog Value update, the new analogue value may be entered by selecting the +ve and -ve step buttons or free-form numerals entered by virtual keyboard.

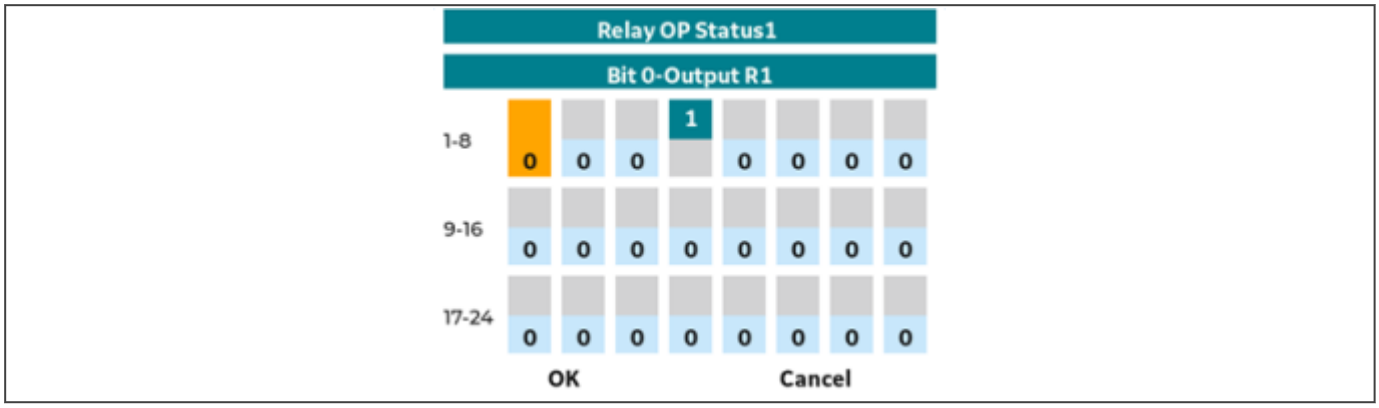


If the setting cell has the facility of drop down, the required setting can be selected from the drop down list.

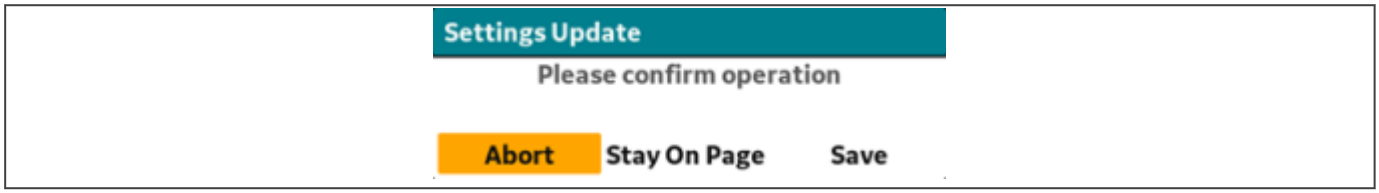


Some of the settings are in the form of Binary Data Bits update. By selecting each of the Bit position the data can be toggled.

Note:
Binary Data Bits can also be used to verify the present data of each bits for monitoring purpose.



- Press the **Enter** key to confirm the new setting value or the **Clear** key or the on-screen 'x' to discard it.
- To confirm the new settings, press the **Enter** key. Navigate away from the currently active group settings or press the **Home** key. A Settings update confirmation dialogue box will appear that requires choosing of one of the following options:
- Save - accept all settings including the recently changed settings
- Abort - discard recent changes and keep existing settings
- Stay on page - return to the active settings page without saving recent changes



- To return to the top of the menu, hold down the **Up** cursor key for a second or so, or press the **Clear** key once. It is possible to move across columns from anywhere in the menu by using the Menu context keys at the bottom of the display.
- To return to the default display, press the **Home** key at any time.
- Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.
- The Date and time can be adjusted by navigating to the top banner and selecting the displayed time. Press the **Enter** key to adjust the date and time using the calendar/clock widget that pops up.

Note:
For the protection group and disturbance recorder settings, the changes are not saved unless confirmed using the Settings update confirmation prompt.

Note:
All other Control and support settings (such as Communications and Control inputs), however, are updated immediately after they are entered on the front HMI without the need to confirm using the Settings update confirmation prompt.

5.3.10 FUNCTION KEYS

Most products have a number of function keys for programming control functionality using the programmable scheme logic (PSL).

Each function key has an associated programmable tri-colour LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are in the *FUNCTION KEYS* column.

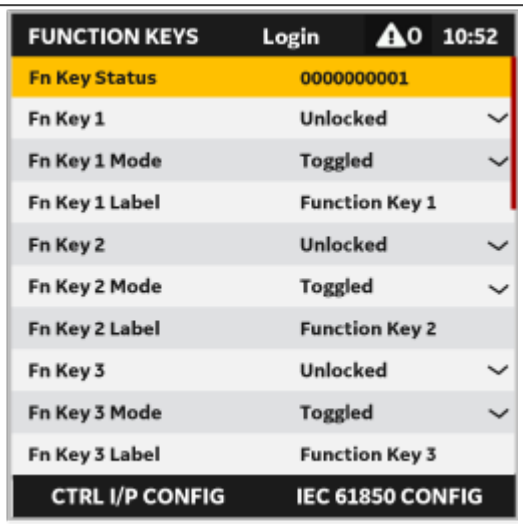


Figure 37: HMI Function Keys Display

The first cell down in the *FUNCTION KEYS* column is the ***Fn Key Status*** cell. This contains a binary string, which represents the function key commands. Their status can be read from the binary string.

The next cell down (***Fn Key 1***) allows you to activate or disable the first function key (1). The ***Lock*** setting allows a function key to be locked. This allows function keys that are set to `Toggled` mode and their DDB signal active 'high', to be locked in their active state, preventing any further key presses from deactivating the associated function. Locking a function key that is set to the Normal mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

The next cell down (***Fn Key 1 Mode***) allows you to set the function key to `Normal` or `Toggled`. In the Toggle mode the function key DDB signal output stays in the set state until a reset command is given, by activating the function key on the next key press. In the Normal mode, the function key DDB signal stays energised for as long as the function key is pressed then resets automatically. If required, a minimum pulse width can be programmed by adding a minimum pulse timer to the function key DDB output signal.

The next cell down (***Fn Key 1 Label***) allows you to change the label assigned to the function. The default label is `Function key 1` in this case. To change the label you need to press the enter key and then change the text on the bottom line, character by character. This text is displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

Subsequent cells allow you to carry out the same procedure as above for the other function keys.

The status of the function keys is stored in non-volatile memory. If the auxiliary supply is interrupted, the status of all the function keys is restored. The IED only recognises a single function key press at a time and a minimum key press duration of approximately 200 ms is required before the key press is recognised. This feature avoids accidental double presses.

The function keys needs operator permissions to operate. If operator permissions are not held by the present user an information dialogue is raised to inform the operation has failed.

5.3.10.1 VISUALISATION OF PROTECTION OPERATION

Where there is a protection operation/trip, in addition to the front panel LED indications, the standing trip is indicated on the LCD screen by a red trim around the top banner. Additionally, the LCD backlight becomes lit and a dialogue is presented with three options:

- “OK” - close the dialogue
- “View” - Navigate to the “record” data view and open the latest fault record
- “Reset Ind” - Attempt to reset the trip indication

CHAPTER 6

AUTORECLOSE

6.1 CHAPTER OVERVIEW

Selected models of this product provide sophisticated Autoreclose (AR) functionality. The purpose of this chapter is to describe the operation of this functionality including the principles, logic diagrams and applications.

This chapter contains the following sections:

6.2 INTRODUCTION TO AUTORECLOSE

Approximately 80 - 90% of faults on transmission lines and distribution feeders are transient in nature. This means that most faults do not last long, and are self-clearing if isolated. A common example of a transient fault is an insulator flashover, which may be caused, for example, by lightning, clashing conductors, or wind-blown debris. Protection functions detecting the flashover will cause one or more circuit breakers to trip and may also remove the fault. If the source is removed, the fault does not recur if the line is re-energised.

The remaining 10 – 20% of faults are either semi-permanent or permanent. A small tree branch falling onto the line for example, could cause a semi-permanent fault. Here the cause of the fault would not be removed by immediate tripping of the circuit, but could possibly be burnt away during a time-delayed trip. Permanent faults could be broken conductors, transformer faults, cable faults or machine faults, which must be located and repaired before the power supply can be restored. In many fault incidents, if the faulty line is immediately tripped out, and time is allowed for the fault arc to de-ionise, reclosing the circuit breakers will result in the line being successfully re-energised.

Autoreclose schemes are used to automatically reclose a circuit breaker a set time after it has been opened due to operation of a protection element. On EHV transmission networks, Autoreclose is usually characterised by high-speed single-phase operation for the first attempt at reclosure. This is intended to help maintain system stability during a transient fault condition. On HV/MV distribution networks, Autoreclose is applied mainly to radial feeders, where system stability problems do not generally arise, and is generally characterised by delayed three-phase operation with potentially multiple reclosure attempts.

Autoreclosing provides an important benefit on circuits using time-graded protection, in that it allows the use of instantaneous protection to provide a high speed first trip. With fast tripping, the duration of the power arc resulting from an overhead line fault is reduced to a minimum. This lessens the chance of damage to the line, which might otherwise cause a transient fault to develop into a permanent fault. Using instantaneous protection also prevents blowing of fuses in teed feeders, as well as reducing circuit breaker maintenance by eliminating pre-arc heating. When instantaneous protection is used with Autoreclose, the scheme is normally arranged to block the instantaneous protection after the first trip. Therefore, if the fault persists after re-closure, the time-graded protection will provide discriminative tripping resulting in the isolation of the faulted section. However, for certain applications, where the majority of the faults are likely to be transient, it is common practise to allow more than one instantaneous trip before the instantaneous protection is blocked.

Some schemes allow a number of re-closures and time-graded trips after the first instantaneous trip, which may result in the burning out and clearance of semi-permanent faults. Such a scheme may also be used to allow fuses to operate in teed feeders where the fault current is low.

When considering feeders that are partly overhead line and partly underground cable, any decision to install Autoreclose should be subject to analysis of the data (knowledge of the frequency of transient faults). This is because this type of arrangement probably has a greater proportion of semi-permanent and permanent

faults than for purely overhead feeders. In this case, the advantages of Autoreclose are small. It can even be disadvantageous because re-closing on to a faulty cable is likely to exacerbate the damage.

6.2.1 ADAPTIVE AUTORECLOSE OVERVIEW

Application of high-speed single-phase reclosing helps to increase the system stability limit as the system voltage and short circuit level increase. In order to have successful single-phase reclosing, the reclosing time should be greater than the de-ionization duration of the fault arc, which will vary based on several factors like duration of fault, system voltage, fault location, atmospheric conditions, capacitive coupling to adjacent conductors and many other factors. In general, the circuit voltage is the predominating factor influencing the de-ionizing time. For single pole autoreclosure there is another effect which has a significant influence on the success of the autoreclosure. The primary arc current is interrupted by disconnecting the faulted phase from the sources by opening the circuit breakers at both ends of the line. After this a secondary arc can prevent the fault clearance. During the single pole dead time capacitive and inductive coupling from the other two phases induces a voltage into the open phase conductor which feeds the secondary arc. The secondary arc is an arc between the open phase and earth which is fed by the two healthy phases via capacitive coupling. The voltage measured at the disconnected phase is characterised by the ohmic nonlinear behaviour of the secondary arc. If the secondary arc is extinguished the

equivalent circuit changes to a linear capacitive behaviour of the phase to earth capacitance of the open conductor. The voltage and current goes back to normal conditions after successful reclosing.

In the majority of cases, a fixed dead time setting is applied for transmission line autoreclose schemes. This may cause a problem if the dead time is not long enough for the fault arc to fully de-ionize. Reclosing before the arc extinction can result in arc restrike and could cause the line protection to trip again, which may incur more stress on the power system. Under certain conditions, the reclosing onto the fault may put system stability at risk or damage the equipment. Hence it is desirable to have an adaptive high-speed reclosing scheme that has a variable dead time interval to allow the breaker to close only after the fault arc has extinguished.

The patented adaptive autoreclose (AAR) technique in this relay overcomes the above issue for single pole autoreclose applications by detecting whether the fault arc is extinguished or not and adapts the dead time. AAR uses the pattern of the faulted phase voltage in the complex plane, which is compared with the other two healthy phase voltages, to distinguish between transient and permanent faults in the case of a single-phase earth fault in the transmission line. Also, it can detect when the arc is extinguished in case of a temporary fault and hence it can facilitate successful high-speed reclosing of a transmission line.

For a single-phase fault if the fault is permanent, the faulted phase voltage magnitude and angle do not change with time after line isolation. Whereas, for a transient fault, the faulted phase voltage magnitude increases as the arc resistance increases until the arc is extinguished. Moreover, the angle of faulted phase voltage at the moment when the arc is extinguished lags 90° the angle of faulted phase voltage immediately after line isolation.

The following facts can be observed for the secondary arc of single phase faults.

Fact 1. In the case of a permanent fault, the faulted phase voltage magnitude and angle remains almost constant after line isolation after the switching transients are damped.

Fact 2. In the case of a transient fault, the voltage magnitude drops immediately after the line isolation and then it slowly increases until the arc is extinguished.

Fact 3. In the case of a transient fault, after the line isolation, the angle δ either drops immediately and then increases slowly or increases from the beginning until the arc is extinguished.

δ is the angle between the sum of healthy phase voltages (δh, δk) and the faulted phase (δs) at line end, δ= δh+δk-δs

|Vs| is the voltage magnitude of the faulted phase at line end

For example, for an A phase fault, |Vs| is the A phase voltage magnitude and δ is the angle between the sum of healthy phase voltages B and C (δh, δk) and the faulted A phase voltage at line end (δs), δ= δB+δC- δA

Fact 4. In case of a transient fault, when the arc is extinguished, the magnitude of faulted phase voltage (|Vs|) either becomes constant after a small drop or becomes oscillatory with a constant DC component.

Fact 5. In case of a transient fault, when the arc is extinguished, the angle δ becomes constant or oscillatory with a constant DC component.

Based on the above-mentioned facts, a new algorithm is used to detect a permanent fault and the time of arc extinction in case of a transient fault. The adaptive reclosing function is initiated by the breaker open status which is also used for the faulted phase selection. The breaker interruption should be detected in less than two cycles in order to detect the fast extinguishing arcs. If the fault is a single-phase to ground fault, the faulted phase voltage is selected and the adaptive reclosing algorithm can be initiated.

Angle δ is calculated and the magnitude of the faulted phase voltage (|Vs|) is monitored to determine the reference time (t_{ref}). t_{ref} is the time that |Vs| starts increasing after the drop that occurs after line isolation. t_{ref} can be determined easily by calculation of the minimum |Vs| after the initiation. If |Vs| keeps to be greater than its minimum value for a cycle, the time point after that cycle and the corresponding δ are assigned to t_{ref} and δ_{ref}. If the reference time could not be found within 10 cycles after algorithm initiation, the time point after the 10 cycles and the corresponding δ are assigned to t_{ref} and δ_{ref}. The latter case normally happens only for permanent faults because the voltage magnitude does not increase after line isolation.

After algorithm initiation, δ and |Vs| is low-pass filtered to attenuate all the unwanted transients. Then, the long-window derivation of the filtered signals is obtained by fitting a line to the last 6 cycles of the data. The slope of the

fitted line is used as a long-window derivation. This method provides a smooth and reliable estimate for derivations of δ and |Vs|.

Fact 1 can be used to detect any permanent fault. This can be done by checking δ, δd and |Vs|d. If |Vs| and δ remain almost constant, δ_d and $|Vs|_d$ derivatves become very small (close to zero) and ($\delta - \delta_{ref}$) will be small as well.

Fact 2 to Fact 5 can be used to detect the transient fault and the time that the arc is extinguished. As per Facts 2 and 4, |Vs| slowly increases after t_{ref} until the arc is extinguished. This means that, after t_{ref}, |Vs|d is positive until the arc is extinguished where $|Vs|_d$ either becomes negative and then zero or becomes oscillatory with a zero DC component. As per Facts 3 and 5, δ slowly increases after t_{ref} until the arc is extinguished. This means that, after t_{ref}, δ_d is positive until the arc is extinguished where δ_d becomes zero or oscillatory with a zero DC component. Simply by checking the above-mentioned criteria, the permanent fault and transient fault with arc extinction time can be detected.

6.3 AUTORECLOSE IMPLEMENTATION

Before describing this function it is first necessary to understand the following terminology:

- A **Shot** is an attempt to close a circuit breaker using the Autoreclose function.
- **Multi-shot** is where more than one **Shot** is attempted.
- **Single-shot** is where only one **Shot** is attempted.
- **Dead Time** denotes the time between initiation of the Autoreclose operation and the attempt to close the circuit breaker. The dead time is normally a fixed time delay but can be can set to adaptive for single pole autoreclose schemes where it is dependent on the arc extinction time for a transient single-phase fault.
- **Reclaim time** is the time following the initiation of the circuit breaker closing and the resetting of the Autoreclose scheme should the Autoreclose attempt be successful and the protection does not detect a subsequent fault condition.
- **High-speed Autoreclose** is generally regarded as an Autoreclose application where the **Dead Time** is less than 1 second.
- **Delayed Autoreclose** is generally regarded as an Autoreclose application where the **Dead Time** is greater than 1 second.

This product features a multiple-shot Autoreclose function, which is suitable for both High-speed Autoreclose and Delayed Autoreclose.

The Autoreclose function can be set to perform a single-shot, two-shot, three-shot or four-shot cycle. Dead Times for all shots can be adjusted independently.

If a circuit breaker closes successfully at the end of the Dead Time, a Reclaim Time starts. If the circuit breaker does not trip again, the Autoreclose function resets at the end of the Reclaim Time. If the protection trips again during the Reclaim Time, the sequence advances to the next shot in the programmed cycle. If all programmed reclose attempts have been made and the circuit breaker does not remain closed, the Autoreclose function goes into Lockout, whereupon manual intervention is required.

An Autoreclose cycle can be initiated by operation of an internal or external protection element provided it is mapped correctly, and that the circuit breaker is closed when the protection operates.

You can choose to initiate the Dead Time on:

- Protection operation
- A protection reset
- A Line Dead condition
- Circuit breaker operation

At the end of the relevant Dead Time, provided system conditions are suitable, a circuit breaker close signal is given. The system conditions to be met for closing are that:

- the system voltages are in synchronism
- or that the dead line/live bus or live line/dead bus conditions exist as indicated by the internal system check synchronising element
- and that the circuit breaker closing spring, or other energy source, is fully charged as indicated by the circuit breaker healthy input.

The circuit breaker close signal is removed when the circuit breaker closes.

If the protection trips and the circuit breaker opens during the Reclaim Time, the Autoreclose function either advances to the next shot in the programmed cycle, or if all programmed reclose attempts have been made, goes into Lockout. Each time a closure is attempted, a sequence counter is incremented by 1 and the Reclaim Time starts again.

Autoreclose is configured in the *AUTORECLOSE* column of the relevant settings group. The function is disabled by default. If you wish to use it, you must enable it first in the *CONFIGURATION* column.

The Autoreclose function is a logic controller implemented in software. It takes inputs and processes them according to defined logic to generates appropriate outputs. The logic is controlled by user prescribed settings and commands. The controlling logic is complex and so, in order to facilitate its design and understanding, it is decomposed into smaller logic functions which, when combined together implement the complete scheme. This section concludes with a summary of:

- the logic inputs to the Autoreclose function,
- the logic outputs from the Autoreclose function
- the Autoreclose operating sequence
- the high-level design of the system logic functionality

6.3.1 AUTORECLOSE LOGIC INPUTS FROM EXTERNAL SOURCES

Logic inputs control the operation of the Autoreclose function. The logic inputs are mapped using DDB signals in the PSL.

Generally the inputs are from external equipment connected to opto-isolated inputs. They can also come from communications inputs, and some are internally derived.

This section provides an overview of the logic inputs originating from external sources.

6.3.1.1 CIRCUIT BREAKER HEALTHY INPUT

For circuit breakers to close, it needs energy. This energy usually comes from a spring (spring-charged circuit breakers) or from gas pressure (gas pressurised circuit breakers). After closing, it is necessary to re-establish sufficient energy in the circuit breaker before it can be closed again.

DDB signal inputs to the Autoreclose function allow the health of circuit breakers to be mapped to the logic. when asserted, these signals demonstrate that there is sufficient energy available to close and trip the circuit breaker before initiating a circuit breaker close command. If the signal indicating the health of the circuit breaker is low, and remains low for a defined period set in the circuit breaker healthy timer, the circuit breaker locks out and stays open.

If the circuit breaker healthy signal is not mapped in the PSL, the DDB signal defaults to high so that Autoreclose may proceed.

6.3.1.2 INHIBIT AUTORECLOSE INPUT

A logic input can be used to inhibit the Autoreclose function. The signal is mapped to the DDB signal ***Inhibit AR*** in the PSL.

Energising the input inhibits any auto-switching of connected circuit breakers. Any Autoreclose in progress is reset and inhibited but not locked out. This function ensures that auto-switching does not interfere with any manual switching. A typical application is on a mesh-corner scheme where manual switching is being performed on the mesh, for which any Autoreclose would cause interference.

For products that are capable of single-phase tripping and Autoreclose, if a single-phase Autoreclose cycle is in progress and a single pole of the circuit breaker is tripped when the inhibit Autoreclose signal is raised, the circuit breaker is instructed to trip all phases, ensuring that all poles are in the same state (and avoiding a pole stuck condition) when subsequent closing of the circuit breaker is attempted.

6.3.1.3 BLOCK AUTORECLOSE INPUT

External inputs can be used to block the Autoreclose function. If Autoreclose is in progress when the signal is asserted, it forces a lockout.

Typically this feature is used where Autoreclose may be required for some protections functions but not required for others. An example is on a transformer feeder, where Autoreclose can be initiated from the feeder protection but blocked from the transformer protection.

It can also be used if an Autoreclose cycle is likely to fail for conditions associated with the protected circuit, such as during the Dead Time, if a circuit breaker indicates that it is not healthy to switch.

6.3.1.4 RESET LOCKOUT INPUT

If a condition that forced a lockout has been removed, the lockout can be reset by energising a logic input appropriately mapped in the PSL. Energising the input will also reset any Autoreclose alarms.

6.3.1.5 POLE DISCREPANCY INPUT

Circuit breakers with independent mechanisms for each pole (phase), normally incorporate a mechanism to cater for cases where the phases are not together. This automatically trips all three phases if they are either not all open, or not all closed.

During single-phase Autoreclosing a pole discrepancy condition is necessarily introduced, but the pole discrepancy device should not operate for this condition. This can be achieved using a delayed action pole discrepancy device with a delay longer than the single-pole Autoreclose Dead Time (***SP AR Dead Time*** setting).

Alternatively, an input can be used for external devices to indicate a pole discrepancy condition. The pole discrepancy input is activated by an external device to indicate that all three poles of a circuit breaker are not in the same position. If mapped in the PSL, energising the input forces three-phase tripping (providing there is not a single-phase Autoreclose in progress). Otherwise, a signal indicating single-phase Autoreclose in progress can be used to inhibit the external pole discrepancy device.

6.3.1.6 EXTERNAL TRIP INDICATION

Protection operation from a different device can be used to initiate the Autoreclose function. By default these external trip inputs are mapped to initiate Autoreclose and to initiate breaker failure protection (if the functions are enabled). These inputs are not mapped to the trip outputs. With appropriate mapping in the PSL however, the external device can use this product to trip connected circuit breakers.

6.3.2 AUTORECLOSE LOGIC INPUTS

This section provides an overview of the logic inputs, which are derived internally.

6.3.2.1 TRIP INITIATION SIGNALS

The phase A, phase B and phase C trip inputs are used to initiate single-phase and three-phase autoreclose. For the Autoreclose to work, you must ensure that these Trip Input signals remain appropriately mapped in the PSL.

6.3.2.2 CIRCUIT BREAKER STATUS INPUTS

Circuit breaker status information must be available as logic input(s) for Autoreclose to work. You can select whether to use CB open, CB closed, or both, as inputs. The settings are made in the *CB CONTROL* column of the menu, and you need to ensure that the PSL mapping of the chosen input(s) is correct.

6.3.2.3 SYSTEM CHECK SIGNALS

System Check and Check Synchronization functions produce signals which are used by the Autoreclose logic ensure that the Autoreclose function is applied only when the system is in a suitable condition.

6.3.3 AUTORECLOSE LOGIC OUTPUTS

Output signals are provided to provide indication of an Autoreclose in progress (ARIP). An ARIP signal is asserted when an Autoreclose sequence starts. It remains high from initiation, either until lockout, or until successful Autoreclose.

An Autoreclose lockout condition resets any ‘Autoreclose in progress’ and associated signals. Signals are available to indicate that Autoreclose is in progress and that a circuit breakers has been successfully closed.

6.3.4 AUTORECLOSE OPERATING SEQUENCE

The Autoreclose sequence is controlled by so-called Dead Timers. Dead Time Control settings are used to select the conditions that initiate Dead Timers in the Autoreclose sequence (for example protection operate, protection reset, CB open, etc.). This section describes typical AR operation sequences in which Dead Timers start when protection operation resets.

Note:
In a multi-shot AR sequence, a number of Dead Timers are used (one for each shot). All Dead Timers are enabled when the sequence is initiated, but each timer only starts when the particular shot with which it is associated is triggered.

6.3.4.1 AR TIMING SEQUENCE - TRANSIENT FAULT

The figure below describes the operating sequence for a single-shot Autorecloser for a transient fault that clears when the faulted line is isolated.

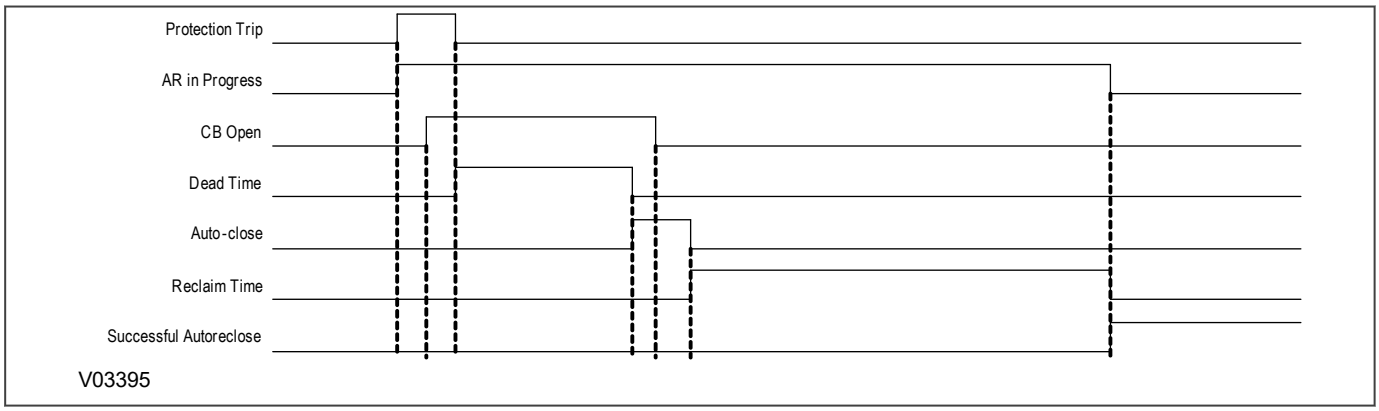


Figure 38: Autoreclose sequence for a Transient Fault

Following fault inception, the protection operates and issues a trip signal. At the same time the Autoreclose in Progress signal is asserted. Shortly afterwards the circuit breaker will open as indicated by the CB Open signal. Opening of the CB clears the fault and the protection resets. When this happens, the Dead Timer is started and the output remains high until the Dead Time setting expires, whereupon it resets and the Autorecloser issues the Auto-close command to close the circuit breaker. As the fault has been cleared, the circuit breaker closes and remains closed. When the Auto-close pulse is removed, the Reclaim Timer starts. If no further fault is detected before the Reclaim Timer expires, the Autoreclose is considered to be successful and this is indicated by the Successful Autoreclose signal.

6.3.4.2 AR TIMING SEQUENCE - TRANSIENT FAULT DUAL CB

The figure below describes the operating sequence for a single-shot on a dual CB (2CB) Autorecloser for a transient fault that clears when the faulted line is isolated.

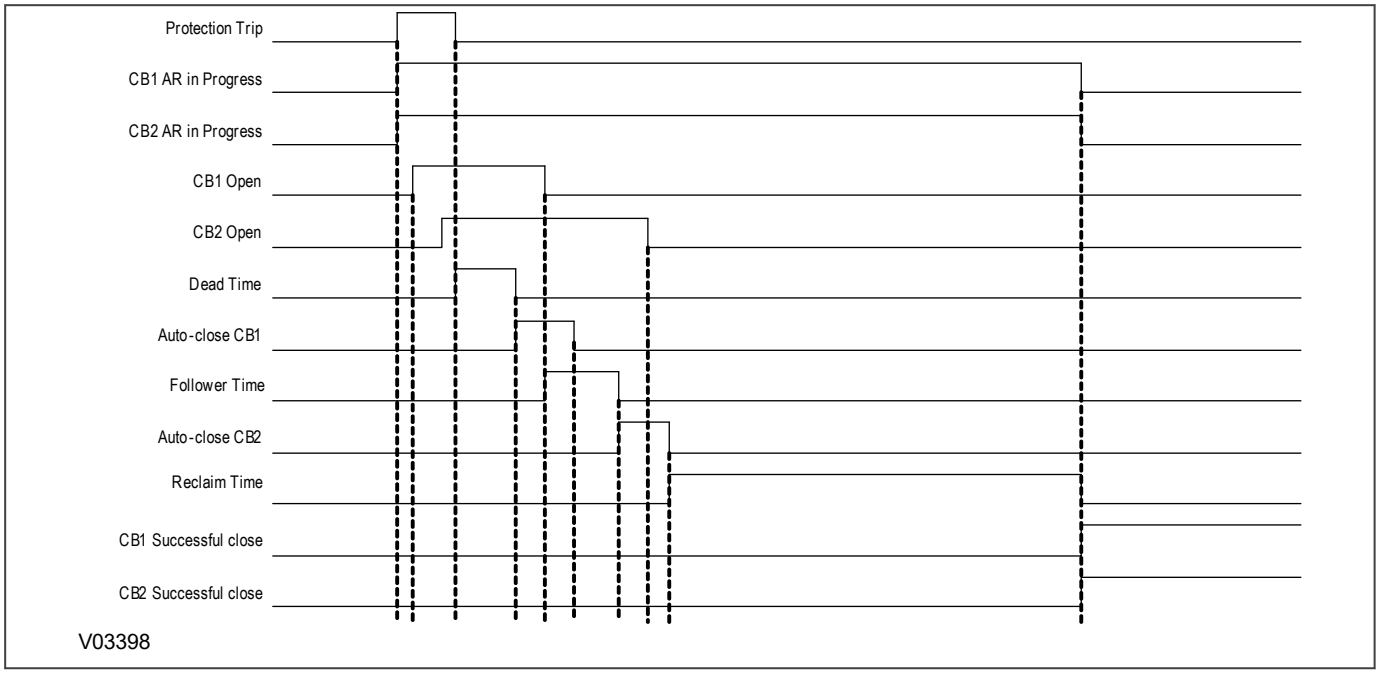


Figure 39: Dual CB Autoreclose Sequence for a Transient Fault

Following fault inception, the protection operates and issues a trip signal. At the same time an Autoreclose in Progress signal is asserted for each CB. Shortly afterwards, CB1 will open as indicated by the CB1 Open signal and after a short delay CB2 opens. Opening of CB2 clears the fault and the protection resets. When this happens, the Dead Timer is started and the output remains high until the Dead Time setting expires, whereupon it resets and the Autorecloser issues the Auto-close command to close CB1. When CB1 closes, the Follower Timer starts. When the Follower Timer expires, the Autorecloser issues the Autoclose command to close CB2. After CB2 has closed, as the fault has been cleared, both CBs remain closed. When the Auto-close 2 pulse is removed, the Reclaim Timer starts. If no further fault is detected before the Reclaim Timer expires, the Autoreclose is considered to be successful and this is indicated by the Successful Autoreclose signals.

6.3.4.3 AR TIMING SEQUENCE - EVOLVING/PERMANENT FAULT

The figure below shows a single-shot AR operating sequence where the fault is not cleared by the first AR cycle. The sequence starts in a similar way to that of a transient fault, but in this case the fault is not transient (it may be permanent, or it may evolve into a fault involving more than one phase). This case shows an evolving fault inception occurring before the Reclaim Time has expired. When the Autorecloser recognises that the protection has tripped, the cycle is terminated. The Autorecloser goes into Lockout, and the Autoreclose in Progress signal is reset.

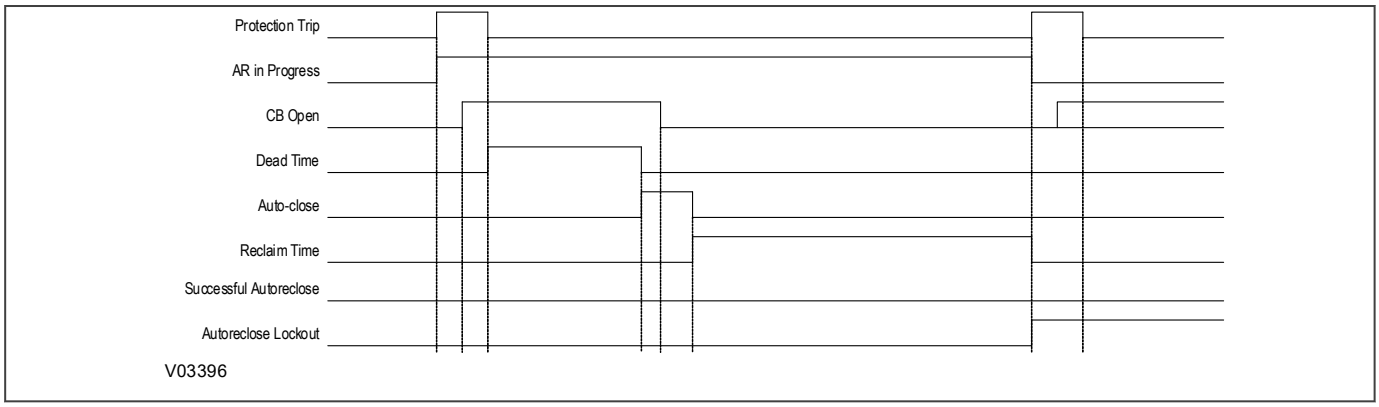


Figure 40: Autoreclose sequence for an evolving or permanent fault

6.3.4.4 AR TIMING SEQUENCE - EVOLVING/PERMANENT FAULT DUAL CB

The figure below shows a single-shot AR operating sequence where the fault is not cleared by the first AR cycle. The sequence starts in a similar way to that of a transient fault, but in this case the fault is not transient (it may be permanent, or it may evolve into a fault involving more than one phase). This case shows an evolving fault inception occurring before the Reclaim Time has expired. When the Autorecloser recognises that the protection has tripped, the cycle is terminated. The Autorecloser goes to Lockout, and the AR in Progress signals are reset

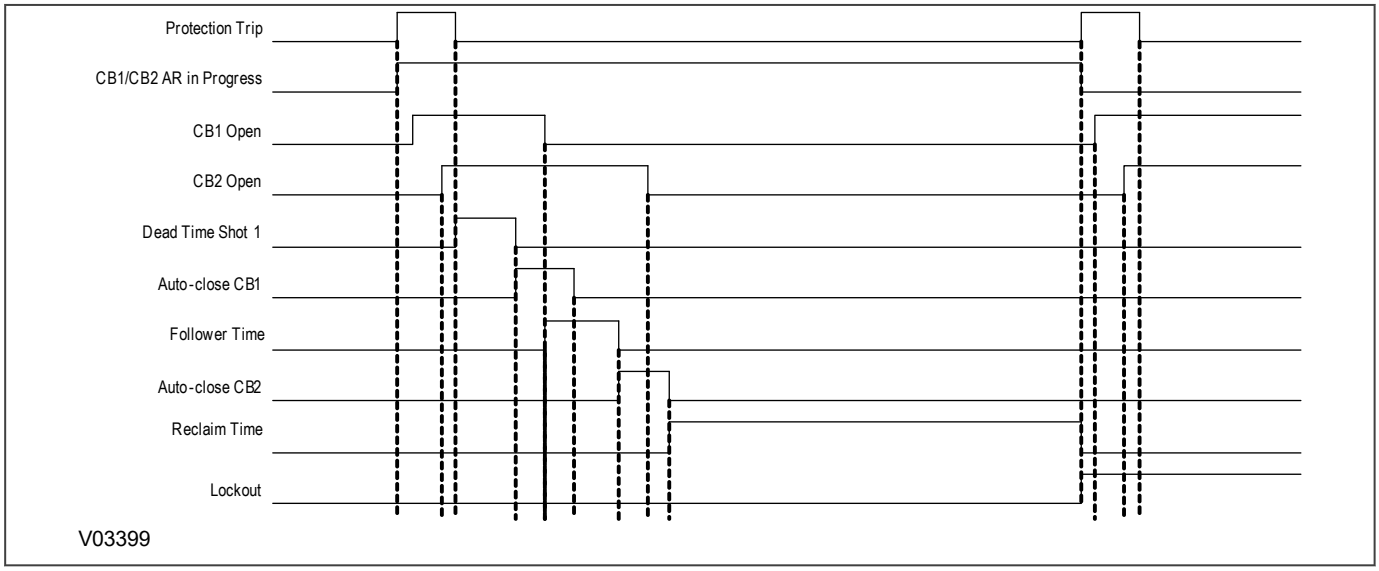


Figure 41: Autoreclose Sequence for an evolving/permanent fault on a dual CB application

6.3.4.5 AR TIMING SEQUENCE - EVOLVING/PERMANENT FAULT SINGLE-PHASE

If the Autorecloser is set for single-phase operation, then single phase operation is only allowed on the first shot. Subsequent tripping will be three-phase only until the AR has been successful or until AR has locked out as shown in the figure below.

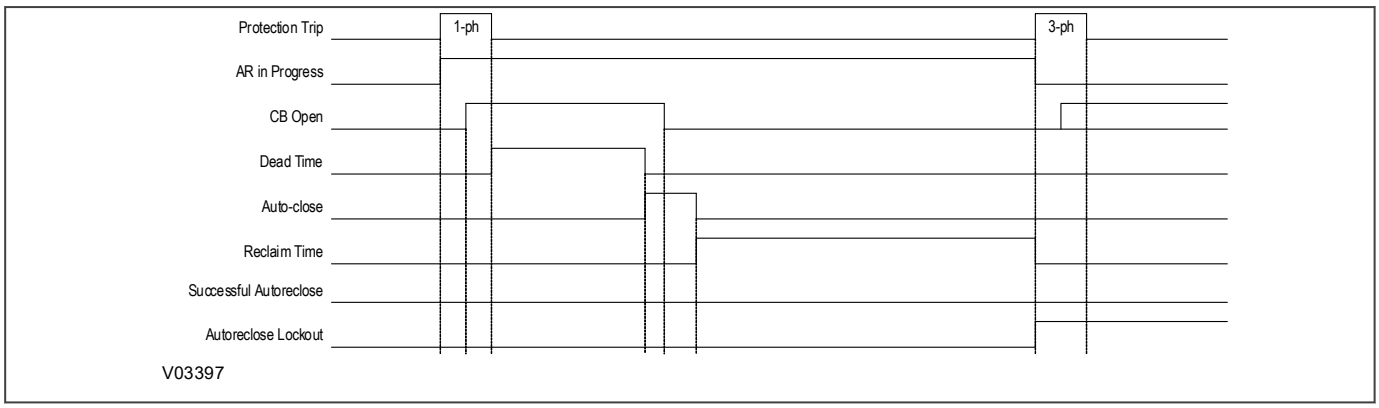


Figure 42: Autoreclose sequence for an evolving or permanent fault - single-phase operation

6.3.4.6 AR TIMING SEQUENCE - PERSISTENT FAULT

The figure below shows the start of a multi-shot AR operating sequence where a single-phase fault is not cleared by the first AR cycle. The sequence starts in a similar way to that of a transient fault, but in this case the fault is not transient (it may be permanent, or it may evolve into a fault involving more than one phase). This case shows a second fault inception occurring before the Reclaim Time has expired. The significant point here is that after the first trip has occurred, the Autorecloser forces the 2 CBs into three-pole operation and different Dead Timers are used for the single-phase cycle compared with the three-phase cycle.

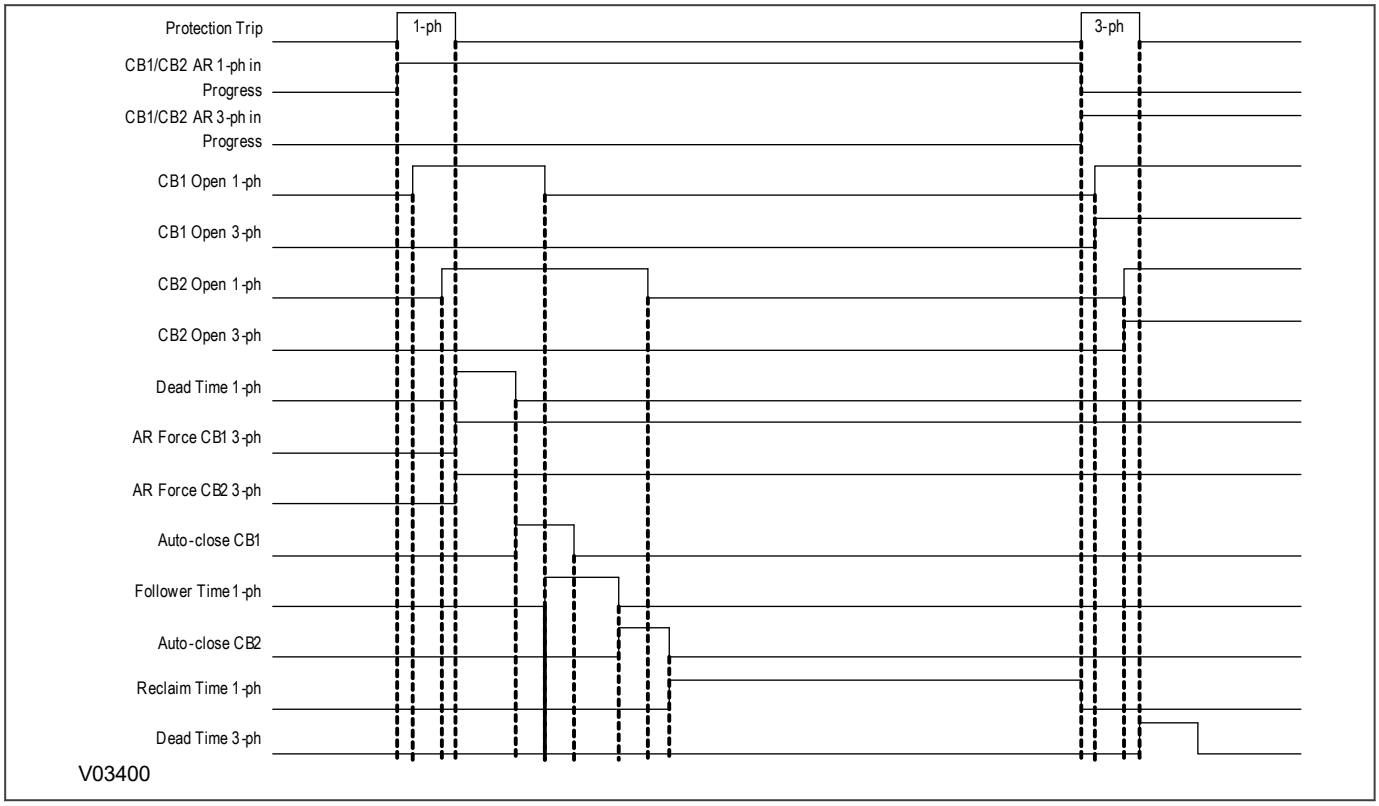


Figure 43: Autoreclose Sequence for a persistent fault on a multishot dual CB application set for single-phase operation

Note:
For three-phase Autoreclosing, for the first shot only, Autoreclose can be performed without checking that the voltages are in synchronism using a setting. This setting, CB1L SC Shot 1 or CB2L SC Shot 1, can be enabled to perform synch-checks on shot 1 for CB1 or CB2, or disabled to not perform the checks.

6.4 LOGIC MODULES (SINGLE CB)

This section contains a complete set of logic diagrams for single CB models, which will help to explain the Autoreclose function. Most of the logic diagrams shown are logic modules that comprise the overall Autoreclose system. Some of the diagrams shown are not directly related to Autoreclose functionality, however, they may use some inputs are produce outputs that are used by the Autoreclose system. The diagrams shown in this section are for the sake of completeness.

"Mod" numbers indicate the related Module Numbers of the fixed logic (as mentioned in the Figure description).

"Mod" numbers in red indicate Module Numbers applicable only for dual breaker logic.

6.4.1 CIRCUIT BREAKER STATUS MONITOR

The Circuit Breaker State Monitor logic is part of the Monitoring and Control functionality and is fully described in that chapter. The logic diagram is repeated in this section because some of the outputs of this logic module are used as inputs to some of the Autoreclose logic modules.

6.4.1.1 CB STATE MONITOR LOGIC DIAGRAM

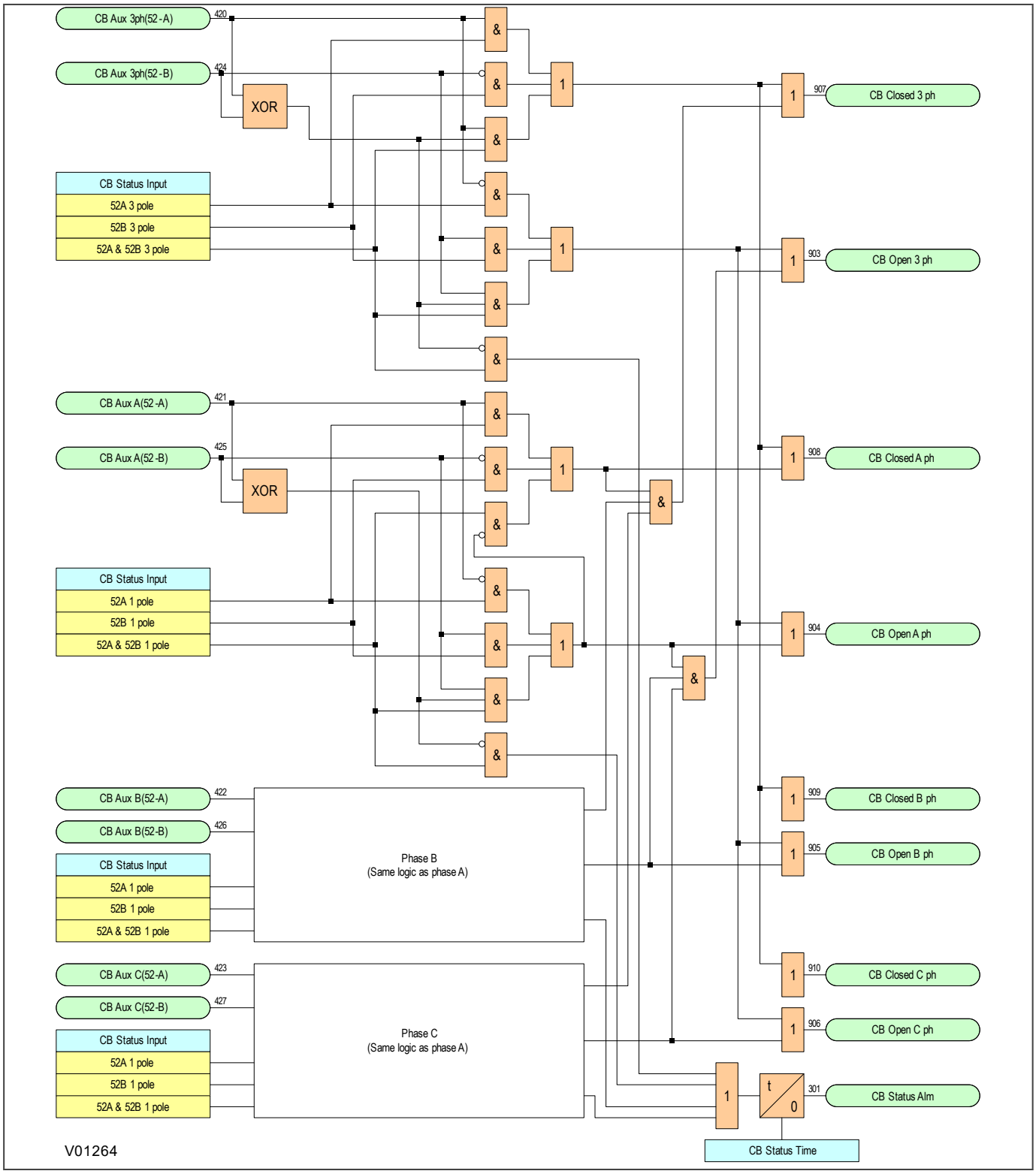


Figure 44: CB State Monitor logic diagram (Module 1)

6.4.2 CIRCUIT BREAKER OPEN LOGIC

The Circuit Breaker Open logic module produces internal signals indicating the open status of one or more phases. These signals are used by some of the Autoreclose logic modules.

6.4.2.1 CIRCUIT BREAKER OPEN LOGIC DIAGRAM

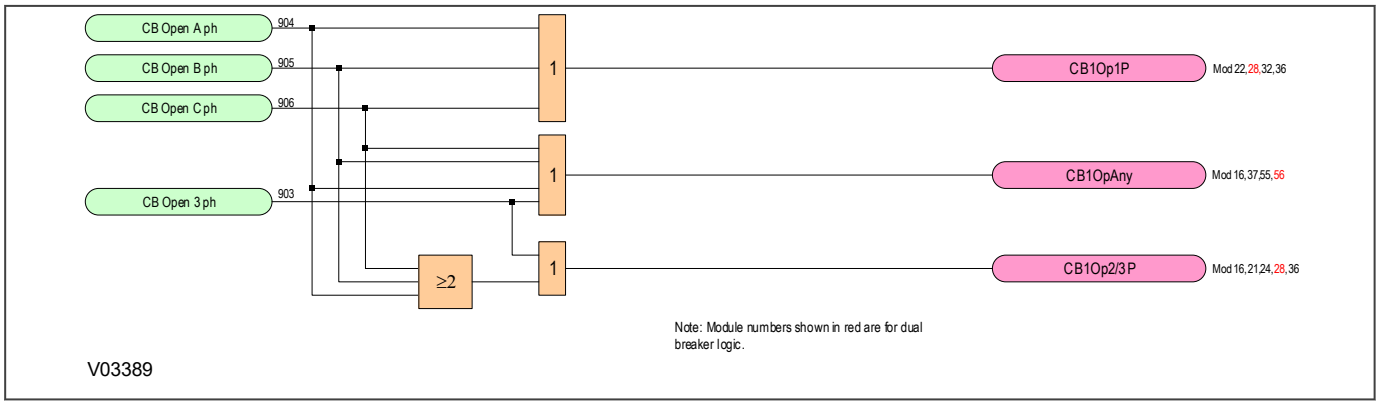


Figure 45: Circuit Breaker Open logic diagram (Module 3)

6.4.3 CIRCUIT BREAKER IN SERVICE LOGIC

For Autoreclose to proceed, a circuit breaker has to be in service when the Autoreclose is initiated. A circuit breaker is considered to be in service if it has been closed for more than the CB IS Time setting.

For applications with fast-acting circuit breaker auxiliary switches, a time delay setting CB IS Memory Time is provided. This is used to ensure correct operation if a delay between the circuit breaker tripping and recognition by the protection, is expected.

When an Autoreclose cycle starts, the “in service” signal for a circuit breaker stays set until the Autoreclose cycle finishes.

The circuit breaker “in service” signal resets if the circuit breaker opens, or if the corresponding Autoreclose in progress (ARIP) signal resets.

6.4.3.1 CIRCUIT BREAKER IN SERVICE LOGIC DIAGRAM

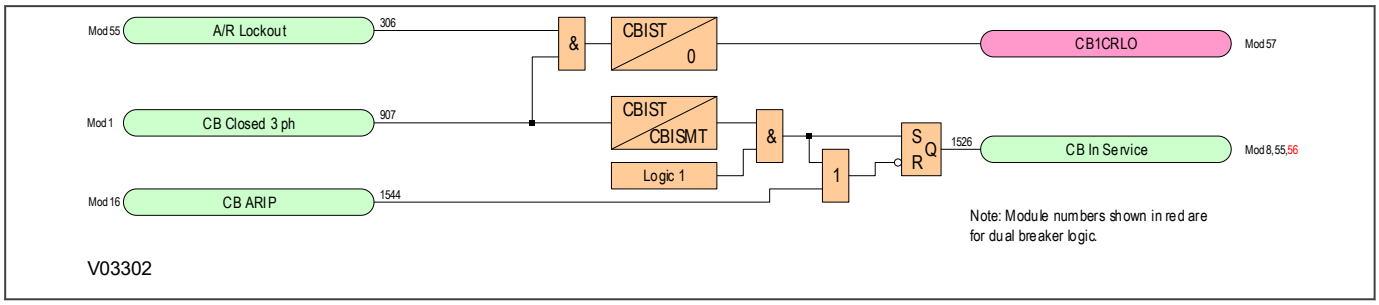


Figure 46: CB In Service logic diagram (Module 4)

6.4.3.2 AUTORECLOSE OK LOGIC DIAGRAM

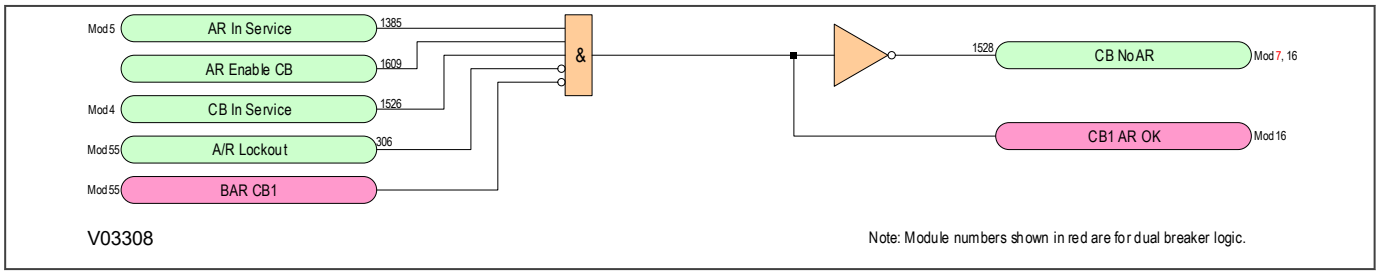


Figure 47: Autoreclose OK logic diagram (Module 8)

6.4.4 AUTORECLOSE ENABLE

The Autoreclose function must be enabled in the *CONFIGURATION* column before it can be brought into service. It can be brought into service by:

- using an opto-input mapped to the ***AR Enable*** DDB signal
- pulsing the DDB signal ***AR Pulse On*** (use ***AR Pulse Off*** to bring it out of service)
- programming a function key on the HMI.
- if applicable, using IEC 60870-5-103 communications

A further validation signal is also required to switch on Autoreclose. This is the DDB signals ***AR Enable CB***. Once Autoreclose is in service, the ***AR In Service*** DDB signal is asserted and the ***AR Status*** cell in the *CB CONTROL* column is set accordingly.

6.4.4.1 AUTORECLOSE ENABLE LOGIC DIAGRAM

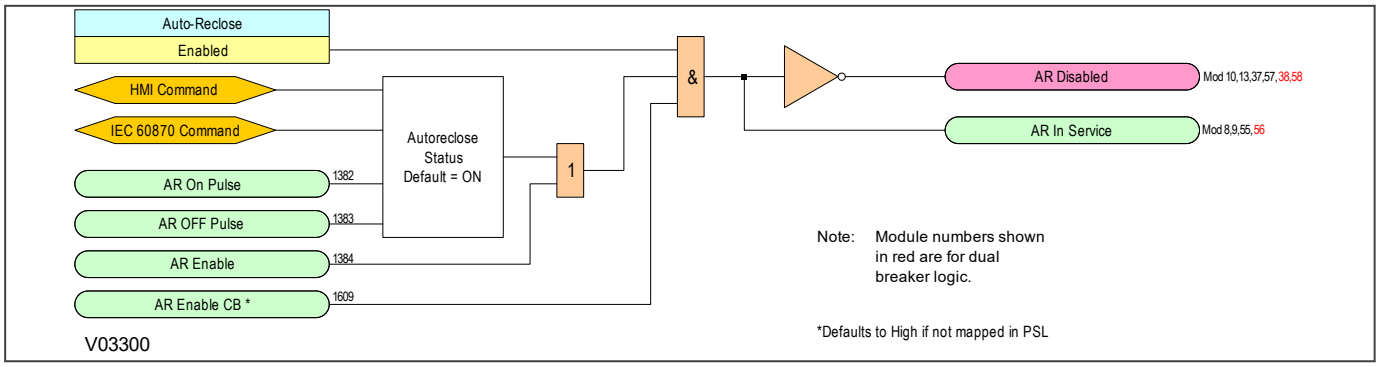


Figure 48: Autoreclose Enable logic diagram (Module 5)

6.4.5 AUTORECLOSE MODES

The device can provide Single-phase and/or Three-phase Autoreclose. The Autoreclose mode is configured by the ***AR Mode*** setting in the *AUTORECLOSE* column. You can choose from:

- Single-phase (`AR 1P`)
- Three-phase (`AR 3P`)
- Single-phase and Three-phase (`AR 1/3P`)
- Controlled by commands from DDB signals that must be mapped to opto-isolated inputs in the PSL (`AR Opto`).

Single-phase Autoreclosing is permitted only for the first shot of an Autoreclose cycle. In a multi-shot Autoreclose cycle the second and subsequent trips will always be three-phase.

For multi-phase faults, you can use the ***Multi Phase AR*** setting in the *AUTORECLOSE* column to configure the following options:

- Allow Autoreclose for all fault types (`Allow Autoclose`)
- Block Autoreclose for 2-phase and 3-phase faults (`BAR 2 and 3 ph`)
- Block Autoreclose for 3-phase faults (`BAR 3 Phase`)

6.4.5.1 SINGLE-PHASE AND THREE-PHASE AUTORECLOSE

Single-phase Autoreclose Only

If single-phase Autoreclose is enabled, the logic allows only a single shot Autoreclose. For a single-phase fault, the single phase dead timer ***SP AR Dead Time*** starts, and the DDB signal ***CB AR 1pole in prog*** is asserted, which indicates that single-phase Autoreclose is in progress. In this case, for a multi-phase fault the logic triggers a three-phase trip and goes to lockout.

Three-phase Autoreclose Only

During three-phase Autoreclose, for any fault, the three-phase dead timers: ***3P AR DT Shot 1***, ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** are started and the DDB signal ***CB AR 3pole in prog*** is asserted, which indicates that three-phase Autoreclose is in progress.

If three-phase only Autoreclose is enabled, the logic forces a three-phase trip by setting the DDB signal ***AR Force 3 pole*** for any single-phase fault.

Single-phase and Three-phase Autoreclose

With single-phase and three-phase Autoreclose enabled then, if the first fault is a single-phase fault the single-phase dead time ***SP AR Dead Time*** is started and the single-phase Autoreclose in progress signal is asserted. If the first fault is a multi-phase fault the three phase dead timer ***3P AR DT Shot 1*** is started and the three-phase Autoreclose in progress signal is asserted. If set to allow more than one reclose (***AR Shots*** >'1') then any subsequent faults are converted to three-phase trips by setting the force three-pole tripping signal. The three-phase dead times ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** (Dead Times 2, 3, 4) are started for the 2nd, 3rd and 4th trips (shots) respectively. The DDB signal ***AR 3pole in prog*** is asserted. If a single-phase fault evolves to a multi-phase fault during the single-phase dead time (***SP AR Dead Time***), single-phase Autoreclose is stopped. The single-phase Autoreclose in progress signal is reset, the three-phase Autoreclose in progress signal is set, and the three-phase dead timer ***3P AR DT Shot 1*** is started.

6.4.5.2 AUTORECLOSE MODES ENABLE LOGIC DIAGRAM

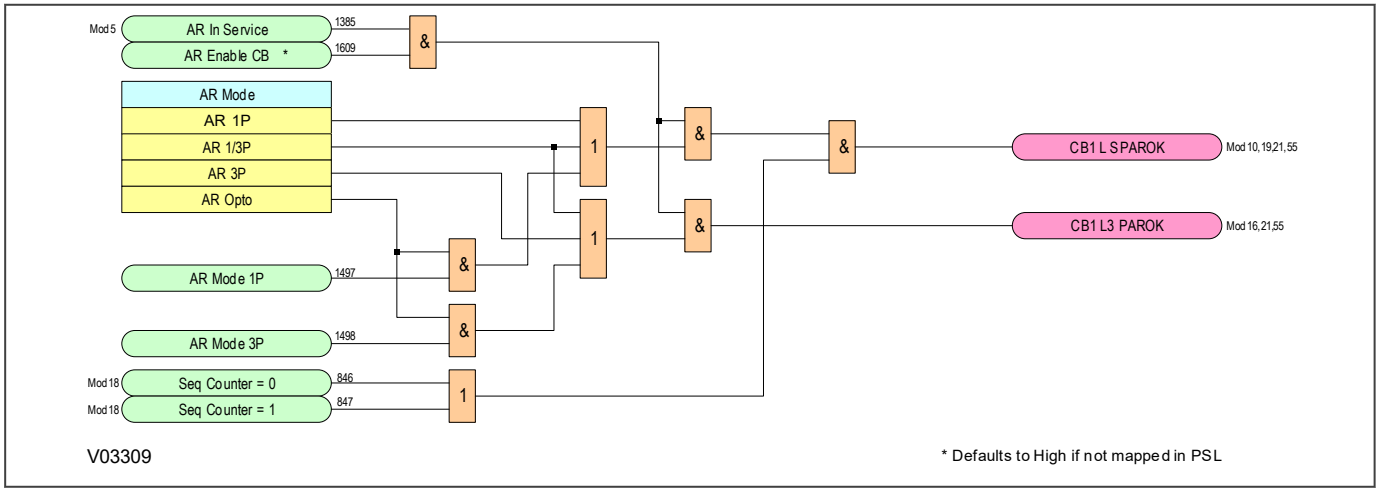


Figure 49: Autoreclose Modes Enable logic diagram (Module 9)

6.4.6 AR FORCE THREE-PHASE TRIP LOGIC

Following single-phase tripping, while the Autoreclose cycle is in progress, and upon resetting of the protection elements, tripping switches to three-phase.

Any protection operations that occur for subsequent faults while the Autoreclose cycle remains in progress will be tripped three-phase.

6.4.6.1 AR FORCE THREE-PHASE TRIP LOGIC DIAGRAM

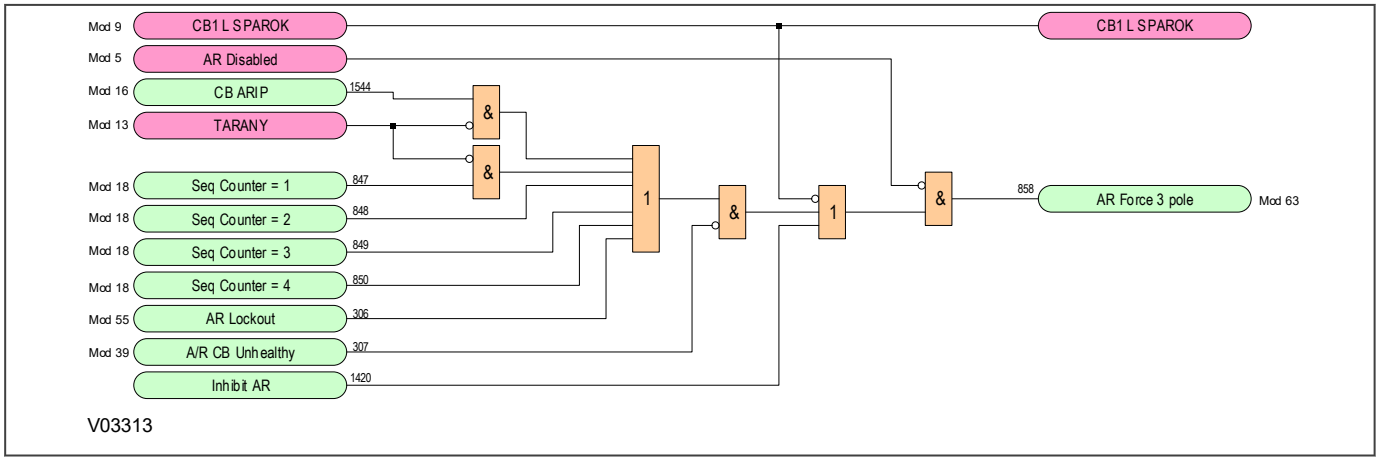


Figure 50: Force Three-phase Trip logic diagram (Module 10)

When a three-phase trip is forced, the DDB signal ***AR Force 3 pole*** is asserted.

6.4.7 AUTORECLOSE INITIATION LOGIC

Autoreclose initiation starts Autoreclose for a circuit breaker only if Autoreclose is enabled for the circuit breaker, and the circuit breaker is in service. When an Autoreclose cycle is started, Autoreclose in progress (ARIP) is indicated. The indication remains until the end of the cycle. The end of the cycle is signified by successful Autoreclose, or by lockout.

Autoreclose cycles can be initiated by:

- Protection functions internal to the product
- A Trip Test feature
- External protection equipment
- Evolving fault combinations

Internal Protection Functions

Many of the protection functions in the product can be programmed to initiate or block Autoreclose. The associated settings are found in the Autoreclose column and the available options are `No Action`, `Initiate AR`, or `Block AR`. If set to `Block AR` operation of the protection function blocks the Autoreclose function and forces a lockout.

Trip Test Feature

The ***Test Autoreclose*** command cell in the *COMMISSION TESTS* column can be used to initiate an Autoreclose cycle. Each option provides a 100 ms pulse output. There is also a 'No Operation' option to exit the command field without initiating a test.

External Protection Equipment

Protection operation from a different device can be used to initiate Autoreclose via PSL. By default these external trip input signals are mapped to initiate Autoreclose. These inputs are not mapped to the trip outputs. With appropriate mapping in the PSL, however, the external device can use this product to trip connected circuit breakers.

Evolving Fault Combinations

The Autoreclose function would normally be initiated by a single condition (such as a single-phase fault). If, however, the system conditions evolve such that other conditions that could initiate Autoreclose, then the dynamics of the Autoreclose logic need to adapt. For example, if a single-phase fault evolves into a multi-phase fault, then the operation of the Autorecloser must consequently adapt. To achieve this signals are generated to indicate conditions such as evolving faults, re-operation of protection, combinations of initiation by internal protection, external protection, or test features, which control the Autoreclose sequencing.

Records of initiating conditions are stored and used to control the sequencing. Initiation can be from a protection function integrated in the product, from external protection and internal sources such as the Autoreclose test function. Initiation can be further qualified by the phases causing the initiation. These conditions are stored in signals that generally feature “MEM”- memory, or “AR” – Autoreclose, in the signal name.

6.4.7.1 AUTORECLOSE INITIATION LOGIC DIAGRAM

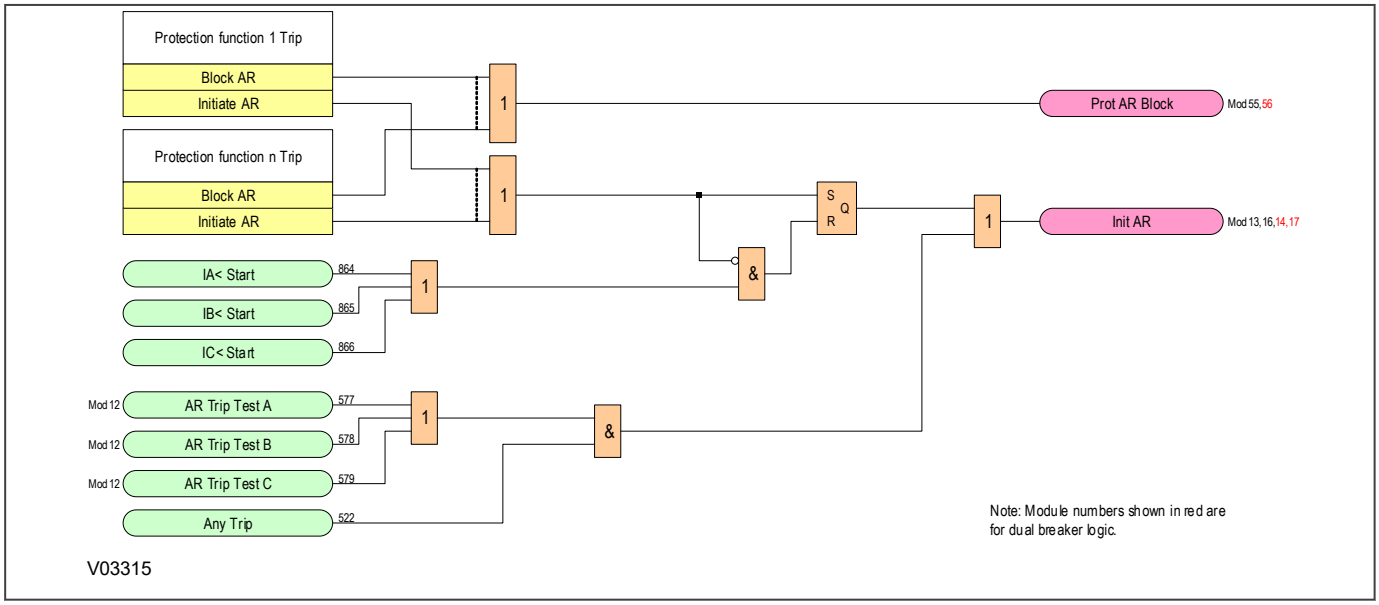


Figure 51: Autoreclose Initiation logic diagram (Module 11)

6.4.7.2 AUTORECLOSE TRIP TEST LOGIC DIAGRAM

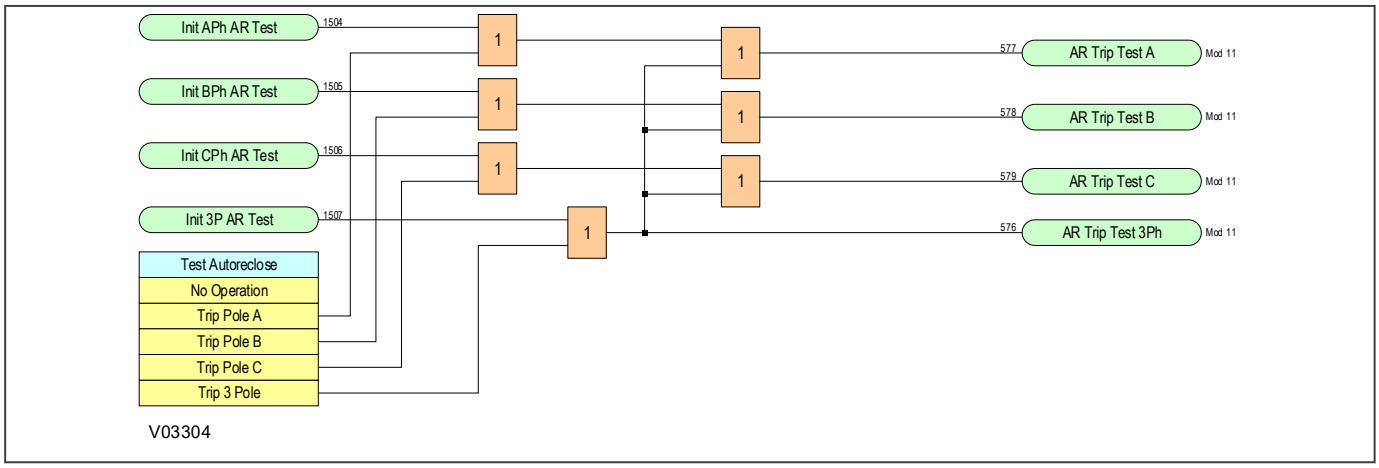


Figure 52: Autoreclose Trip Test logic diagram (Module 12)

6.4.7.3 AR EXTERNAL TRIP INITIATION LOGIC DIAGRAM

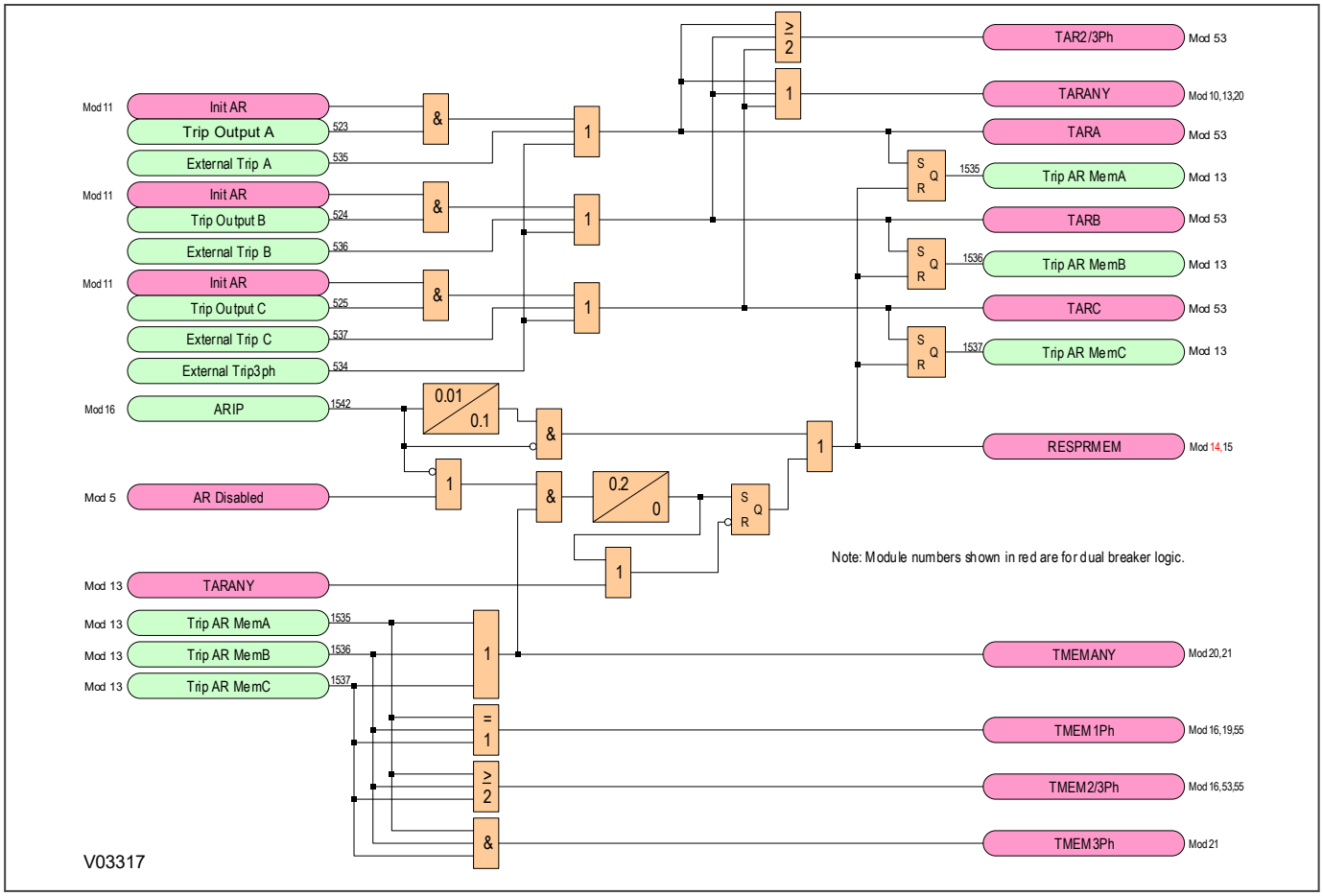


Figure 53: Autoreclose initiation by external trip or evolving conditions (Module 13)

Note:
The signals must be mapped as shown in the default PSL scheme.

6.4.7.4 PROTECTION REOPERATION AND EVOLVING FAULT LOGIC DIAGRAM

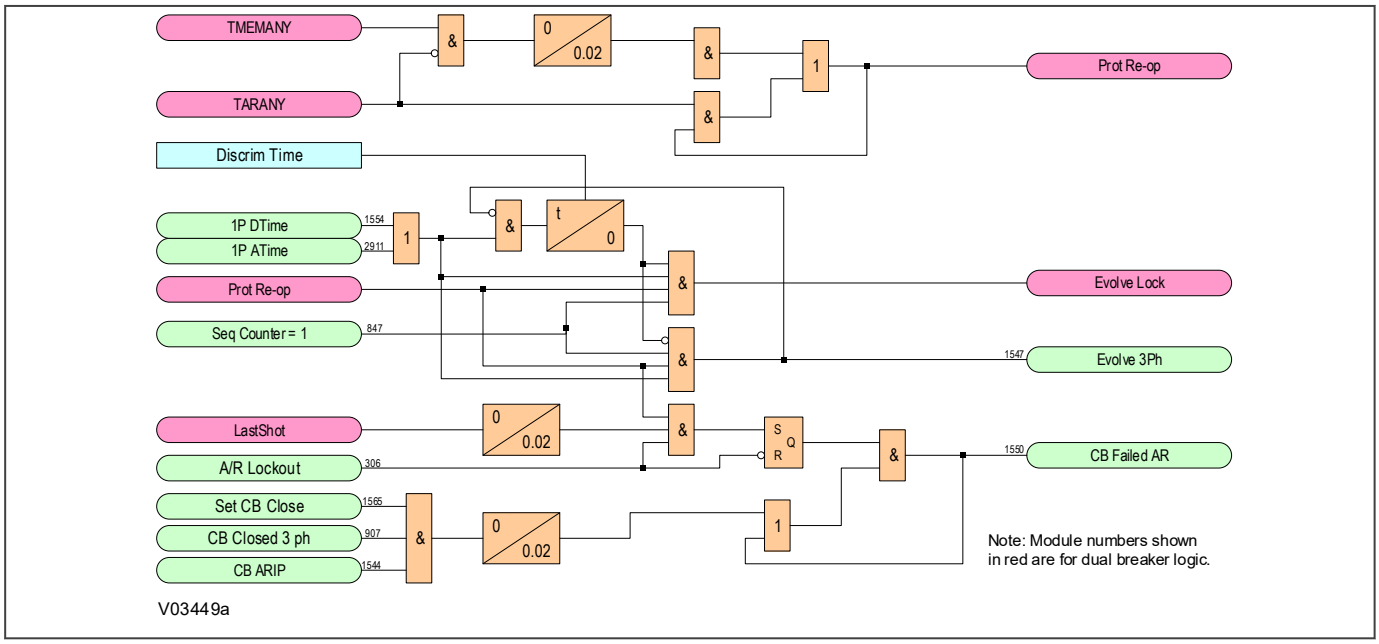


Figure 54: Protection Reoperation and Evolving Fault logic diagram (Module 20)

6.4.7.5 FAULT MEMORY LOGIC DIAGRAM

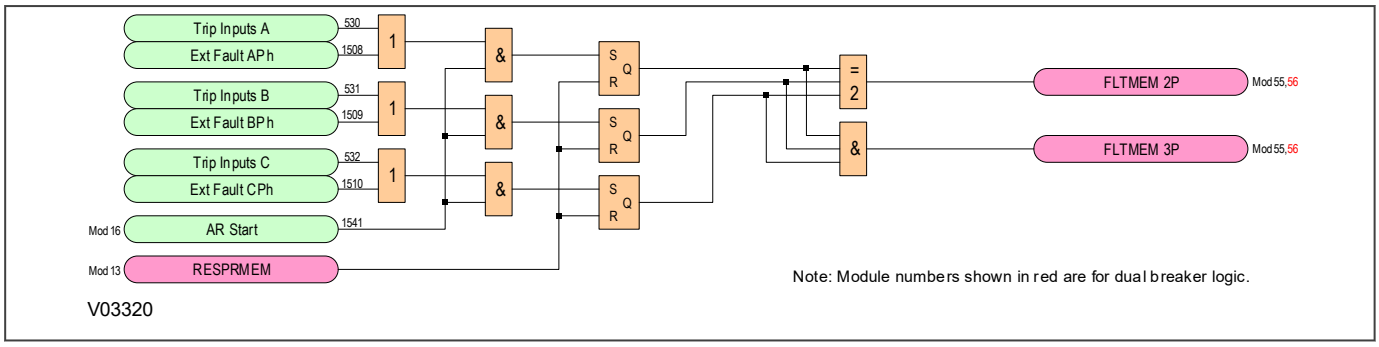


Figure 55: Fault Memory logic diagram (Module 15)

6.4.8 AUTORECLOSE IN PROGRESS

The AR In Progress module produces various signals to indicate to other modules and functions that an Autoreclose operation is currently in progress.

6.4.8.1 AUTORECLOSE IN PROGRESS LOGIC DIAGRAM

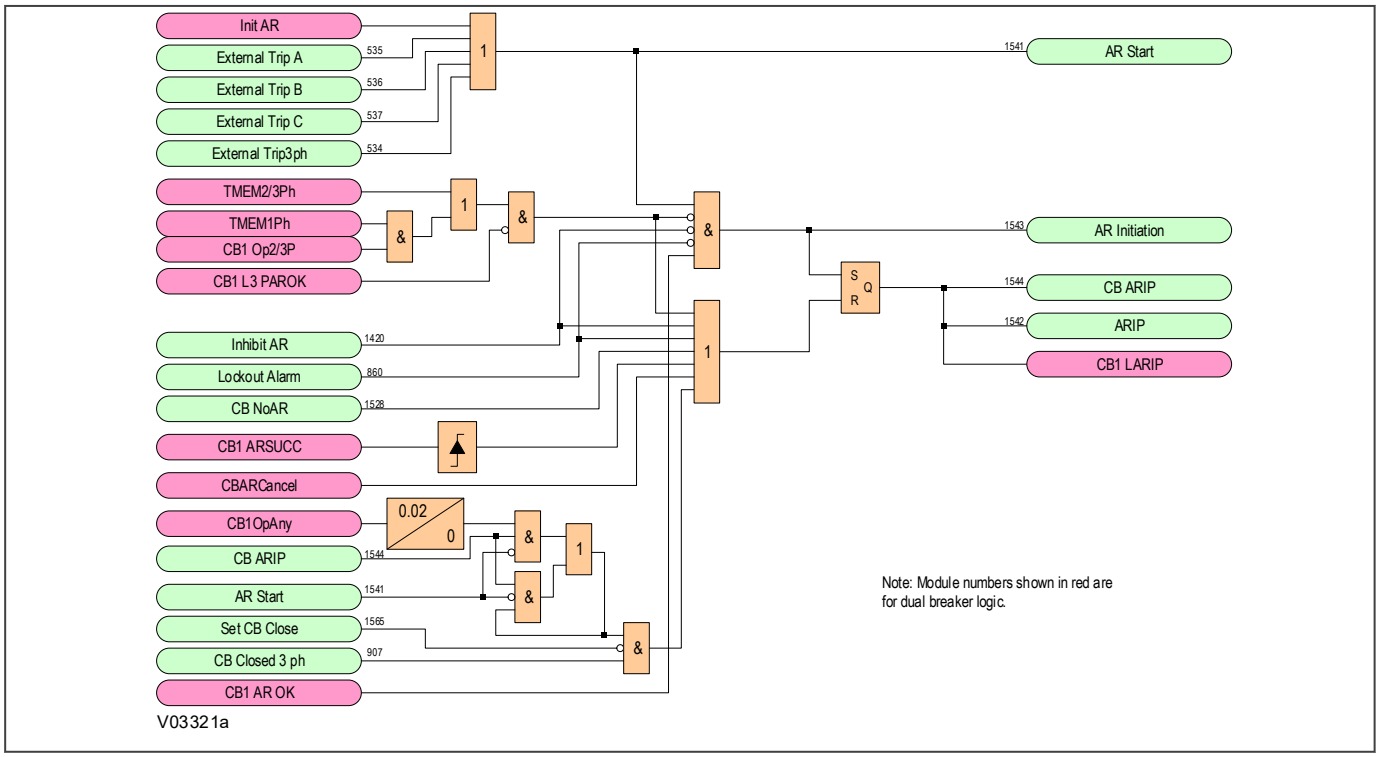


Figure 56: Autoreclose In Progress logic diagram (Module 16)

6.4.9 SEQUENCE COUNTER

The Autoreclose logic includes a counter for counting the number of Autoreclose shots. This is referred to as the sequence counter. The sequence counter has a value of zero if Autoreclose is not in progress. Following a trip, and subsequent Autoreclose initiation, the sequence counter is incremented. The counter provides output signals indicating how many initiation events have occurred in any Autoreclose cycle. These signals are available as user indications and are used in the logic to select the appropriate dead times or, for a persistent fault, force a lockout.

It is possible to skip the first Autoreclose attempt by enabling the ***AR Skip Shot 1*** setting. If this is set, the sequence counter will skip the first Autoreclose attempt (Shot 1) and move to the second (Shot 2) immediately upon Autoreclose initiation. Each time the protection trips the sequence counter is incremented by 1. The Autoreclose logic compares the sequence counter value to the number of Autoreclose shots setting ***AR Shots***. If the counter value exceeds this setting then the Autoreclose is locked out. If Autoreclose is successful, the sequence counter resets to zero.

6.4.9.1 AUTORECLOSE SEQUENCE COUNTER LOGIC DIAGRAM

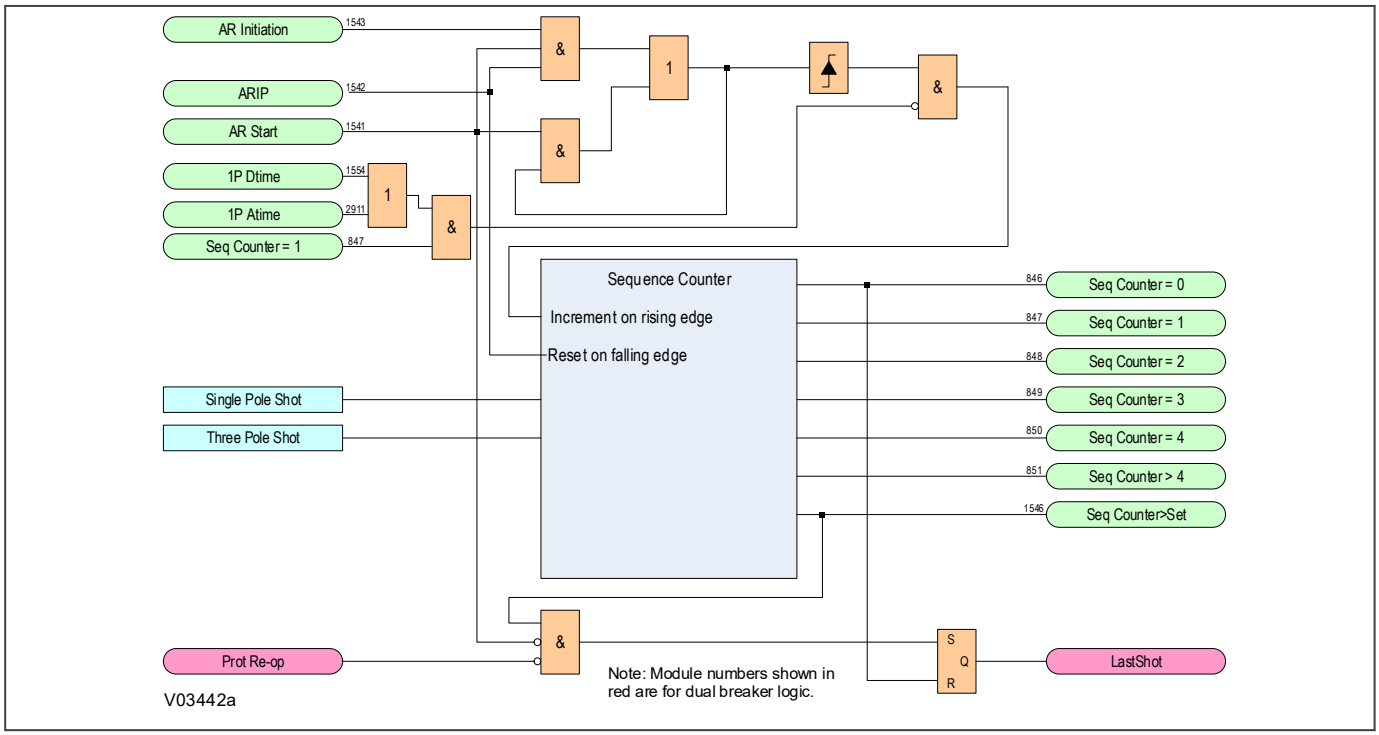


Figure 57: Autoreclose Sequence Counter logic diagram (Module 18)

6.4.10 AUTORECLOSE CYCLE SELECTION

The Autoreclose cycle selection logic is responsible for determining whether the Autoreclose will start as single-phase or three-phase.

6.4.10.1 SINGLE-PHASE AUTORECLOSE CYCLE SELECTION LOGIC DIAGRAM

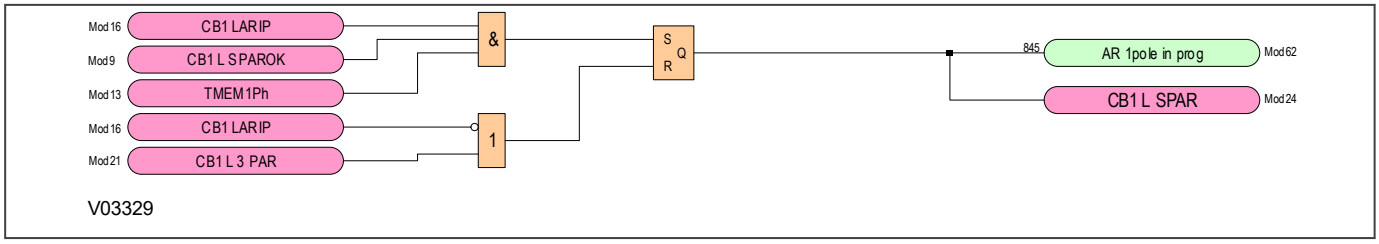


Figure 58: Single-phase Autoreclose Cycle Selection logic diagram (Module 19)

6.4.10.2 3-PHASE AUTORECLOSE CYCLE SELECTION

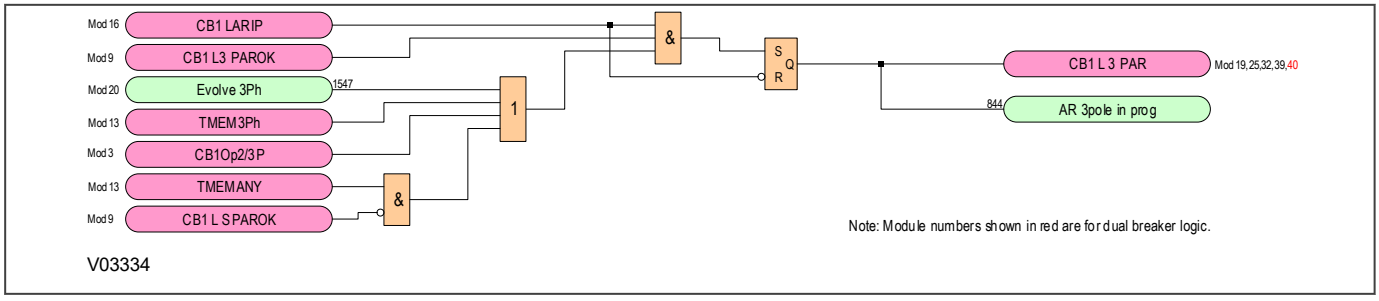


Figure 59: Three-phase Autoreclose Cycle Selection logic diagram (Module 21)

6.4.11 DEAD TIME CONTROL

Once an Autoreclose cycle has started, the conditions to enable the dead time to run are determined by the menu settings, the circuit breaker status, the protection status, the nature of the AR cycle (single-phase or three-phase), and the opto-isolated inputs from external sources.

Three settings are involved in controlling the dead time start:

- ***DT Start by Prot***
- ***3PDTStart WhenLD***
- ***DTStart by CB Op***

The ***DT Start by Prot*** determines how the protection action will initiate a dead time. The setting is always visible and has three options `Protection Reset`, `Protection Op` (protection operation), and `Disable` which should be selected if you don't want protection action to start the dead time. These options set the basic conditions for starting the dead time.

Selecting protection operation to start the dead time can, optionally, be qualified by a check that the line is dead.

Selecting protection reset to start the dead time can, optionally, be qualified by a check, that the circuit breaker is open (***DTStart by CB Op***) before starting the dead time. For three-phase tripping applications, there is a further option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time.

If ***DT Start by Prot*** is disabled, the circuit breaker must be open for the dead time to start. For three-phase tripping applications, there is an option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time. To check that the line is dead, set ***3PDTStart WhenLD*** to `enabled`. To check that the circuit breaker is open, set ***DTStart by CB Op*** to `Enabled`.

6.4.11.1 DEAD TIME START ENABLE LOGIC DIAGRAM

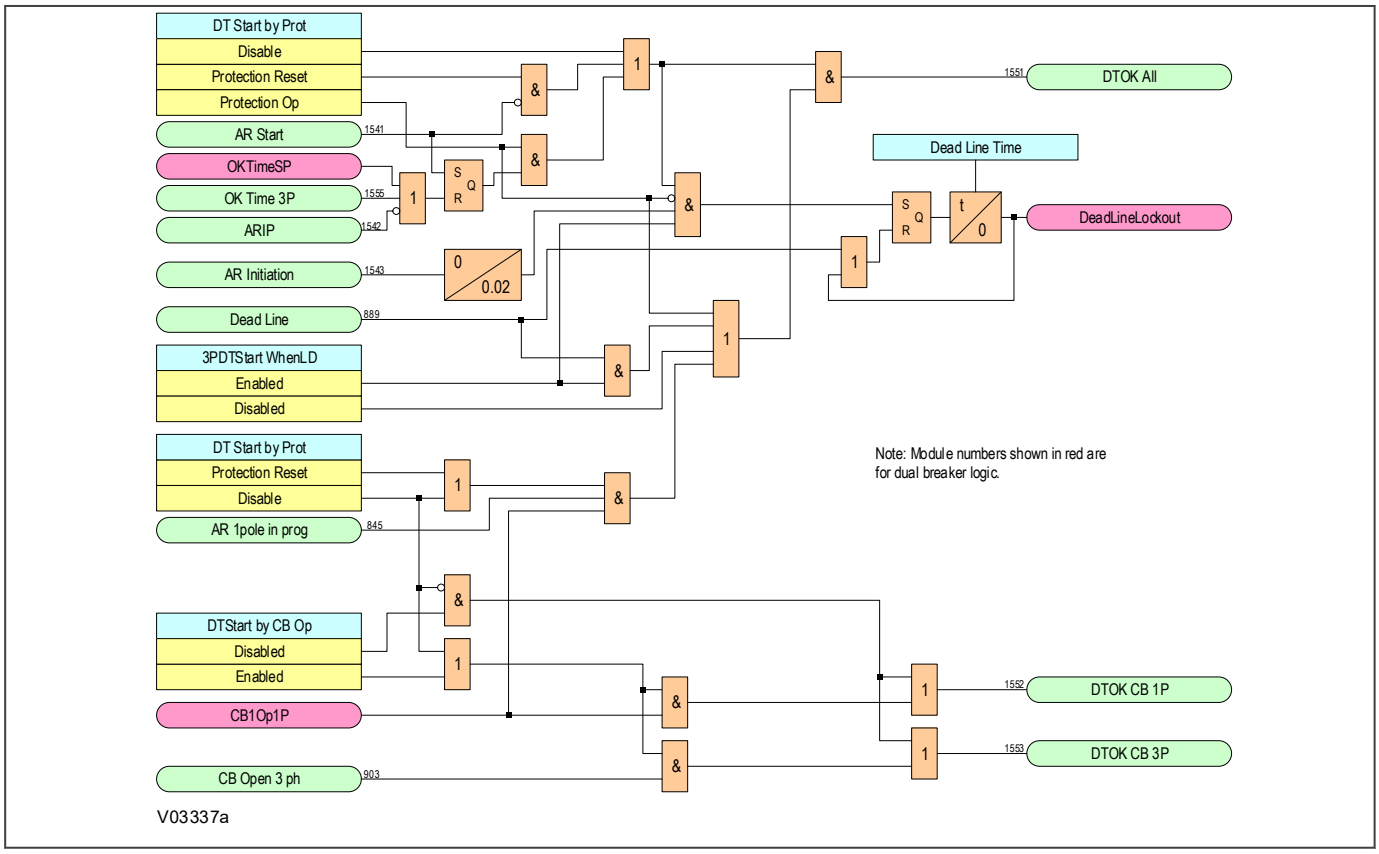


Figure 60: Dead time Start Enable logic diagram (Module 22)

6.4.11.2 SINGLE-PHASE DEAD TIME AND ADAPTIVE AUTORECLOSE (AAR) LOGIC

The autoreclose scheme is adaptive when the ***Adaptive SP AR*** setting is *Enabled*. The adaptive autoreclose is only available for single pole autoreclose applications. When adaptive autoreclose is enable, ***SP AR Dead Time*** is hidden, and two new timer settings are visible: ***SP Min Dead Time*** and ***SP Max Dead Time***. Those two timers are the limits of the single pole dead time.

The Fault Type and Arc Extinction (FTAE) detection algorithm is initiated when the ***Adaptive SP AR*** setting is *Enabled* and the ***OkTimeSP*** signal of the dead time is high, as shown in Module 24.

The breaker open status (***CB Open A PH***/***CB Open B PH*** /***CB Open C PH***) signals are used to identify the single phase to ground fault isolation. The phase voltage information is provided to a six cycle buffer and the δ and |Vs| and derivatives are fed to the ***FTAED*** Module.

The output signals from the ***FTAED*** Module are the ***P_Fault***, ***T_Fault*** and the ***Arc complete*** signals which indicate a permanent fault detection, transient fault detection and arc extinction.

The ***T_Fault*** signal is high during a transient fault condition and the Arc complete signal is high only after complete de-ionization of the faulted arc during transient fault conditions. During a permanent fault condition, the ***P_Fault*** output signal of the AAR module is high, and it is routed to the AR lockout logic diagram (Module 55) to stop further autoreclose actions if required.

The ***CB1SPDTCOMP*** and ***CB1SPATCOMP*** signals in Module 24 are inputs to the Circuit Breaker Auto Close Logic Diagram (Module 32). The ***CB1SPDTCOMP*** signal is high in cases where the ***Adaptive SP AR*** is setting is *0* and ***CB1SPATCOMP*** is high in cases where the ***Adaptive SP AR*** setting is *1*.

6.4.11.3 1-PHASE DEAD TIME LOGIC DIAGRAM

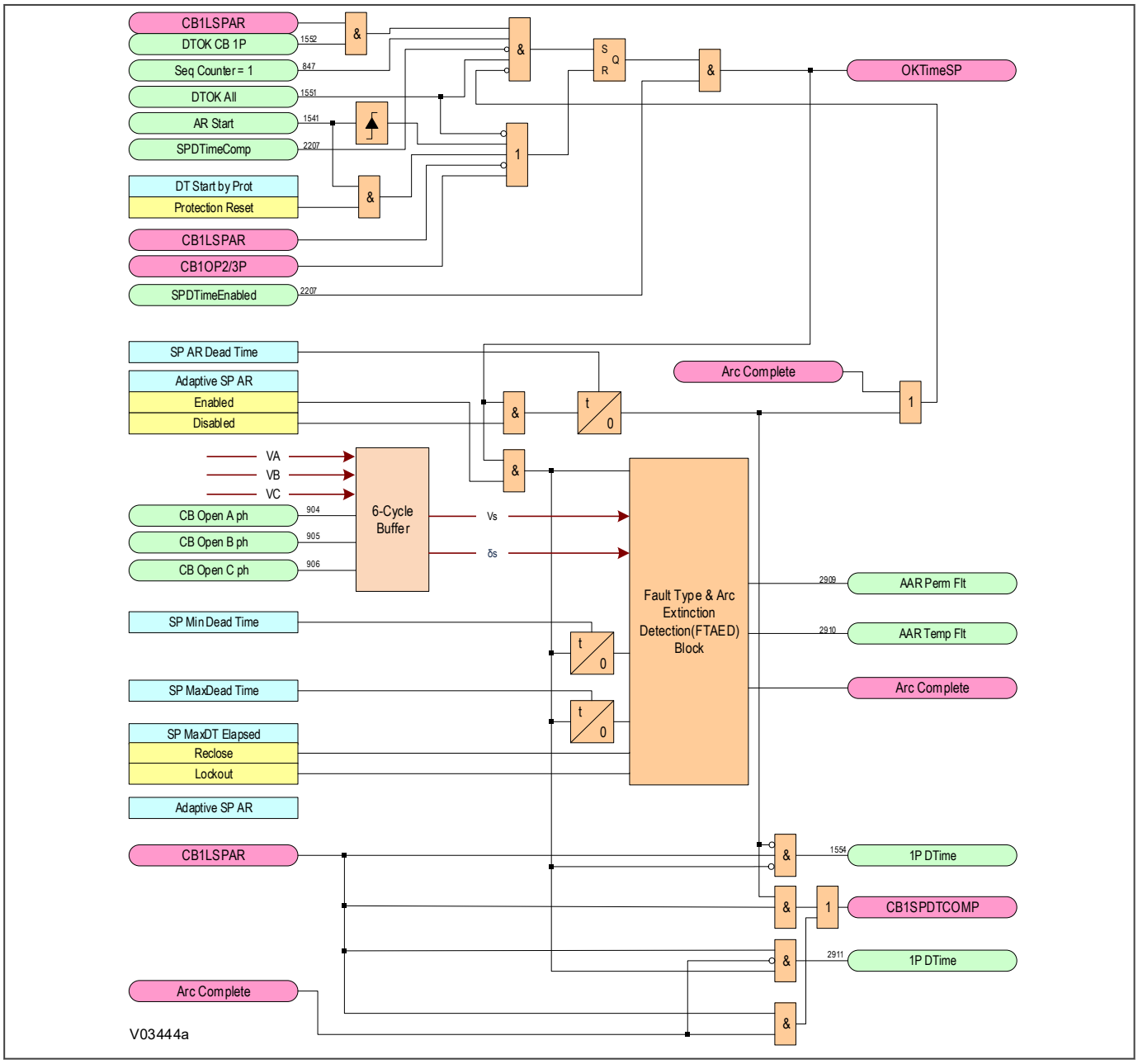


Figure 61: Single-phase Dead Time logic diagram (Module 24)

6.4.11.4 3-PHASE DEAD TIME LOGIC DIAGRAM

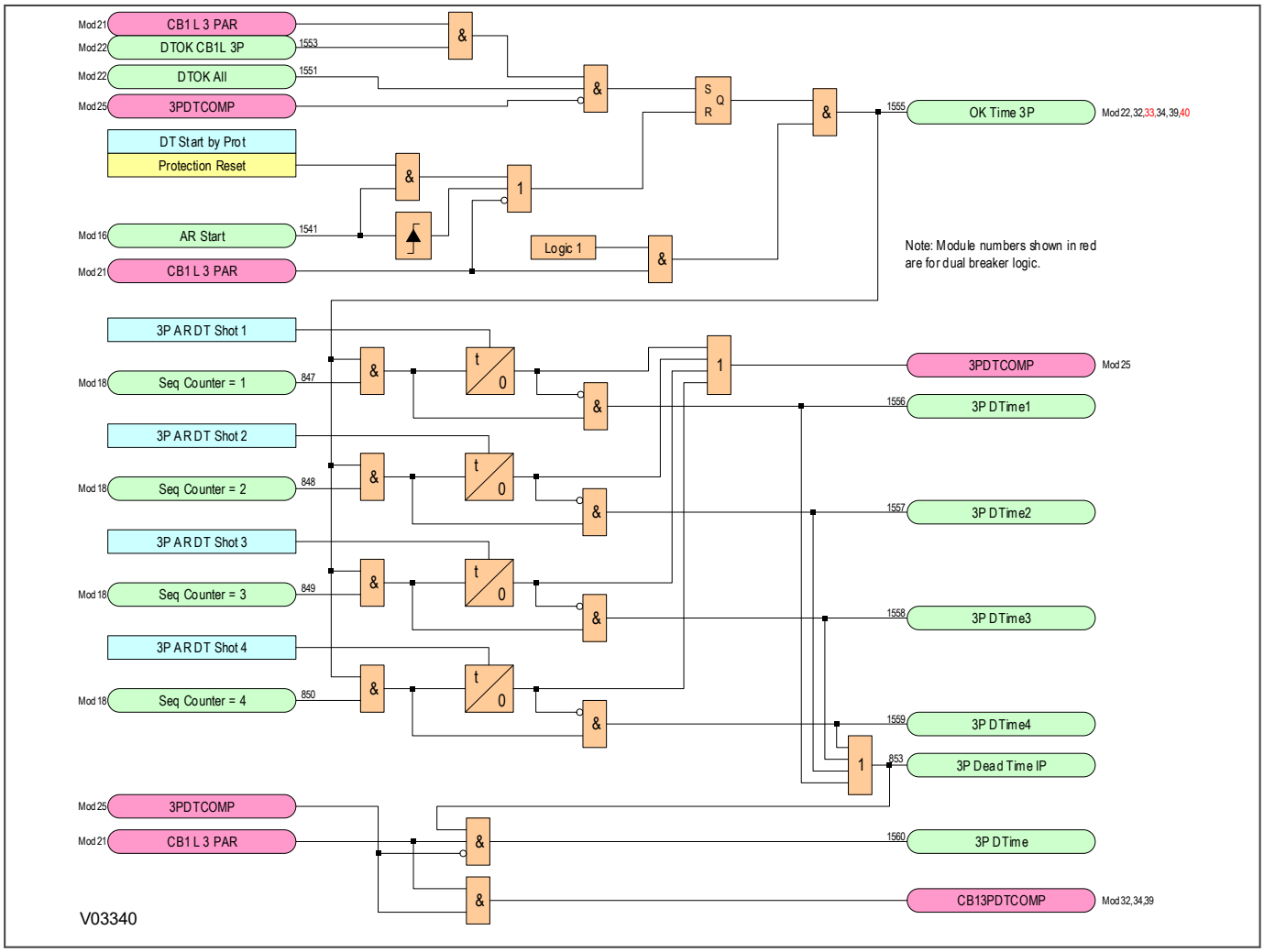


Figure 62: Three-phase Dead Time logic diagram (Module 25)

6.4.12 CIRCUIT BREAKER AUTOCLOSE

Autoclose logic takes effect when dead times have expired.

The Autoclose logic checks that all necessary conditions are satisfied before issuing an Autoclose command to the circuit breaker control scheme.

Before a circuit breaker can be closed, it must be healthy (sufficient energy to close, and if necessary re-trip) and it must not be in a lockout condition.

For three-phase Autoreclose, the circuit breaker must be open on all three phases and the appropriate system check conditions must be met. For single-phase Autoreclose, the circuit breaker must be open on that phase.

The Autoclose command is a pulse lasting 100 milliseconds. Another command (***Set CB Close***) to set the circuit breaker to close is asserted as well as the Autoclose command. This signal will remain set either until the end of the Autoreclose cycle, or until the next protection operation. These commands are used to initiate the Reclaim Time logic and the Autoreclose Shot Counter logic.

6.4.12.1 CIRCUIT BREAKER AUTOCLOSE LOGIC DIAGRAM

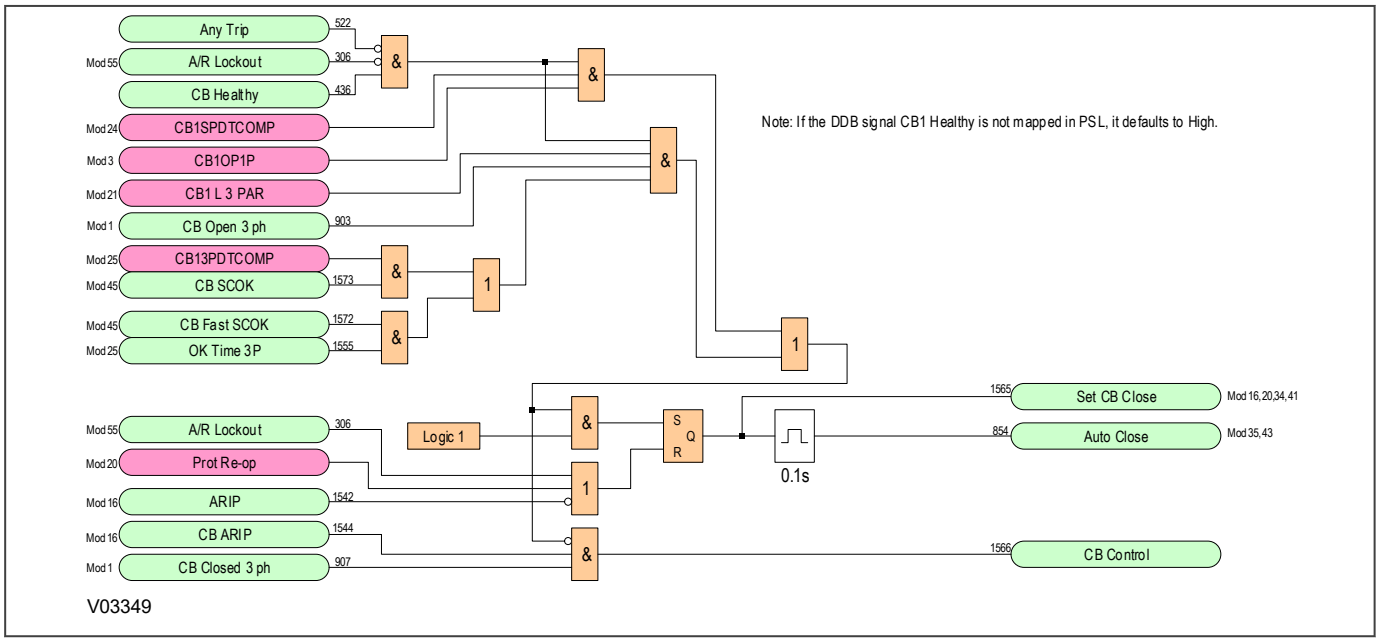


Figure 63: Circuit Breaker Autoclose Logic Diagram (Module 32)

6.4.13 RECLAIM TIME

If the protection operates again before the reclaim time has expired, the corresponding sequence counter is incremented. At the same time, any “dead time complete” (….DTCOMP) signals are reset and the logic is prepared for the next dead time to start when conditions are suitable. The operation also resets the signal that would set the circuit breaker to close, and stops and resets the reclaim timer. The reclaim time starts again if the signal to set a circuit breaker to close goes high following completion of a dead time in a subsequent Autoreclose cycle. Where the reclaim extend time signal is set, the reclaim time cannot time out and reset the Autoreclose cycle before the time delayed protection has fully operated

If the circuit breaker is closed and has not tripped again when the reclaim time expires, signals are generated to indicate successful Autoreclose. These signals increment the relevant circuit breaker successful Autoreclose shot counters and reset the relevant Autoreclose in progress signal.

The “successful Autoreclose” signals generated from the logic can be reset by various commands and settings options available under *CB CONTROL* menu settings as follows:

If ***Res AROK by UI*** is set to `Enabled`, all the signals can be reset by user interface command ***Reset AROK Ind*** from the *CB CONTROL* menu.

If ***Res AROK by NoAR*** is set to `Enabled`, the signals for each circuit breaker can be reset by temporarily generating an Autoreclose disabled signal according to the logic shown.

If ***Res AROK by Ext*** is set to `Enabled`, the signals can be reset by activation of an external input signal appropriately mapped in the PSL.

If ***Res AROK by TDly*** is set to `Enabled`, the signals are automatically reset after a time delay set in ***AROK Reset Time***.

6.4.13.1 PREPARE RECLAIM INITIATION LOGIC DIAGRAM

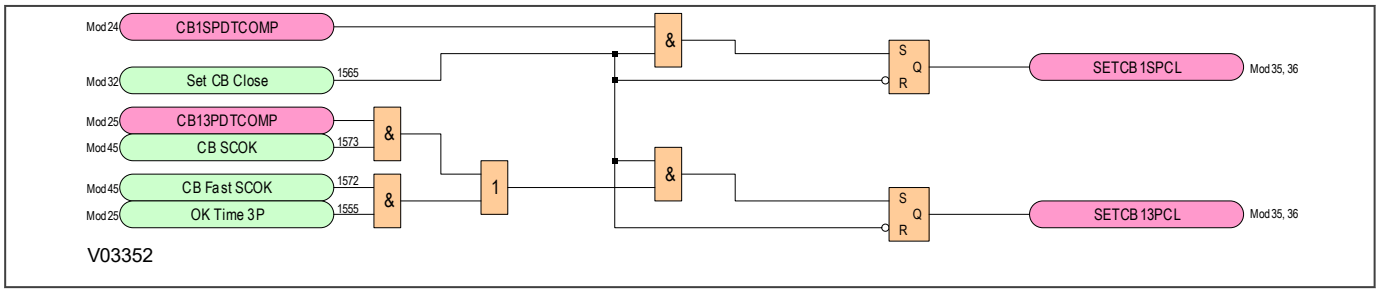


Figure 64: Prepare Reclaim Initiation Logic Diagram (Module 34)

6.4.13.2 RECLAIM TIME LOGIC DIAGRAM

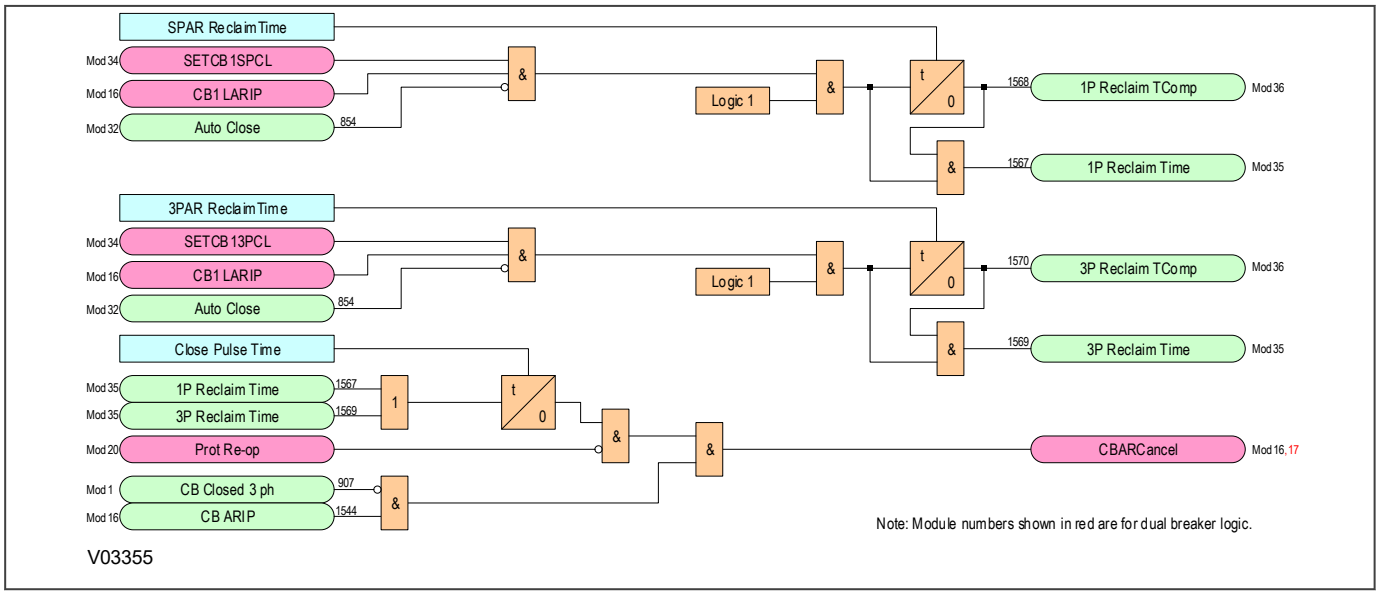


Figure 65: Reclaim Time logic diagram (Module 35)

6.4.13.3 SUCCESSFUL AUTORECLOSE SIGNALS LOGIC DIAGRAM

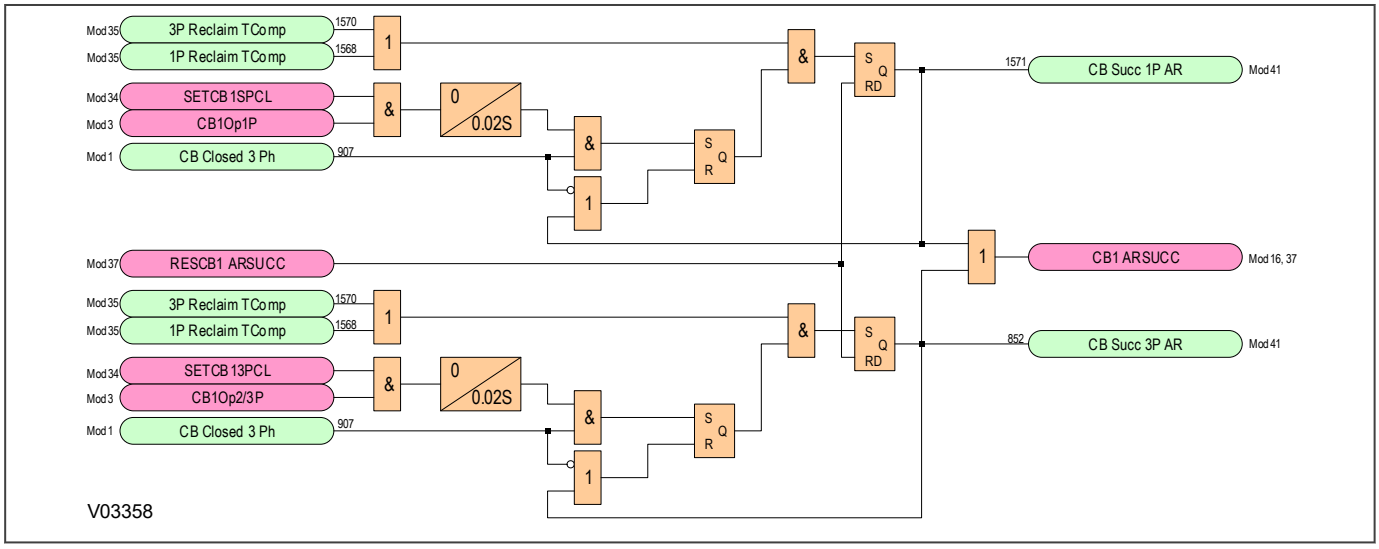


Figure 66: Successful Autoreclose Signals logic diagram (Module 36)

6.4.13.4 AUTORECLOSE RESET SUCCESSFUL INDICATION LOGIC DIAGRAM

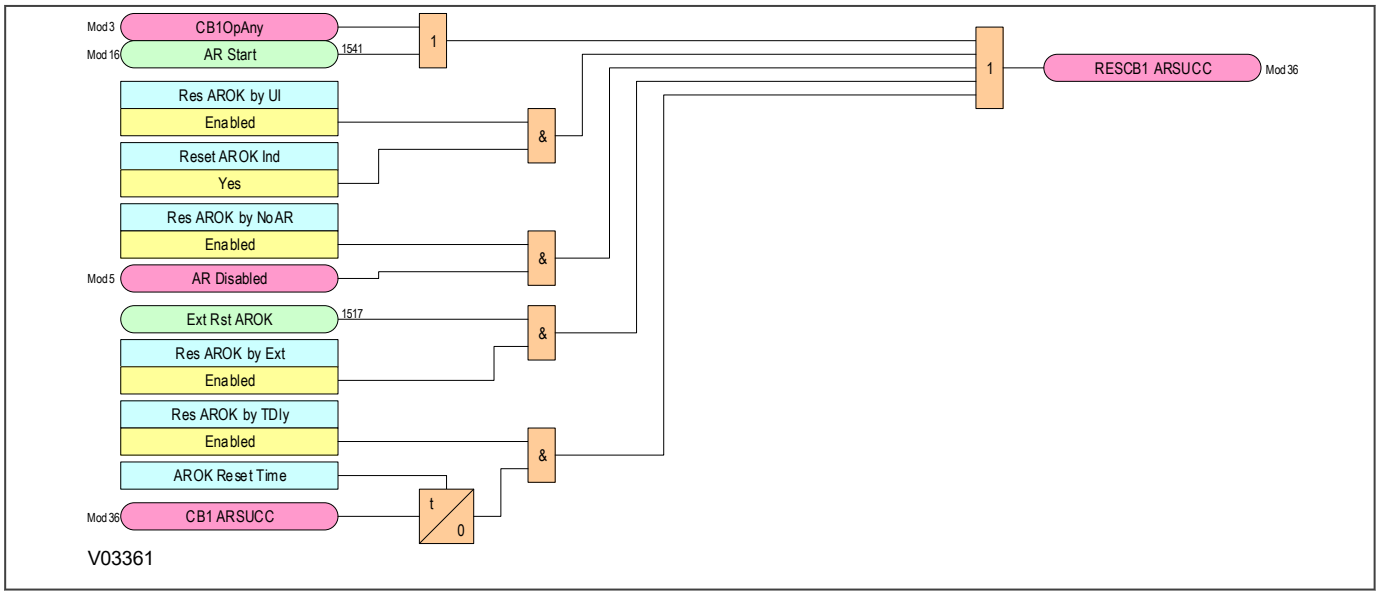


Figure 67: Autoreclose Reset Successful Indication logic diagram (Module 37)

6.4.14 CB HEALTHY AND SYSTEM CHECK TIMERS

This logic provides signals to cancel Autoreclose if the circuit breaker is not healthy (for example low gas pressure) or system check conditions are not satisfied (for example required line & bus voltage conditions) when the scheme is ready to close the circuit breaker.

At the completion of a dead time, the logic starts an Autoreclose healthy timer. If a circuit breaker healthy signal becomes high before the Autoreclose healthy time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker healthy signal stays low, then, at the end of the Autoreclose healthy time, a circuit breaker unhealthy alarm is raised. This forces the Autoreclose sequence to be cancelled.

Additionally, at the completion of any three-phase dead time, the logic starts an Autoreclose check synchronism timer. If the circuit breaker synchronism-check OK signal goes high before the time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker synchronism-check OK signal stays low, then when the Autoreclose check synchronism timer expires, an alarm is set to inform that the check synchronism is not satisfied and cancels the Autoreclose cycle.

6.4.14.1 CB HEALTHY AND SYSTEM CHECK TIMERS LOGIC DIAGRAM

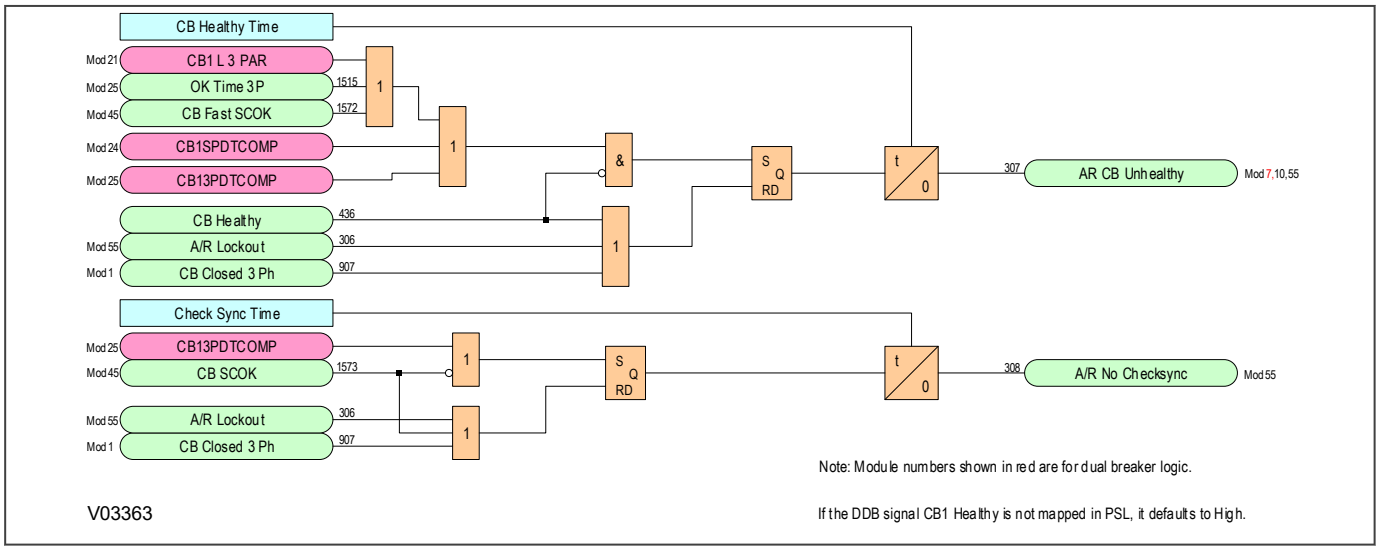


Figure 68: Circuit Breaker Healthy and System Check Timers Healthy logic diagram (Module 39)

6.4.15 AUTORECLOSE SHOT COUNTERS

A number of counters are provided to enable analysis of circuit breaker Autoreclose history. The counters are stored in non-volatile memory, so that the data is maintained even in the event of a failure of the auxiliary supply. The counter values are accessible through the *CB CONTROL* column. The counters can be reset manually, or by activation of an input appropriately mapped in the PSL.

The logic provides the following summary information for each circuit breaker

- Overall total number of shots (Number of Autoreclose attempts)
- Number of successful 1st shot single-phase Autoreclose sequences
- Number of successful 1st shot three-phase Autoreclose sequences
- Number of successful 2nd shot three-phase Autoreclose sequences
- Number of successful 3rd shot three-phase Autoreclose sequences
- Number of successful 4th shot three-phase Autoreclose sequences
- Number of failed Autoreclose cycles which forced a circuit breaker to lockout

6.4.15.1 AUTORECLOSE SHOT COUNTERS LOGIC DIAGRAM

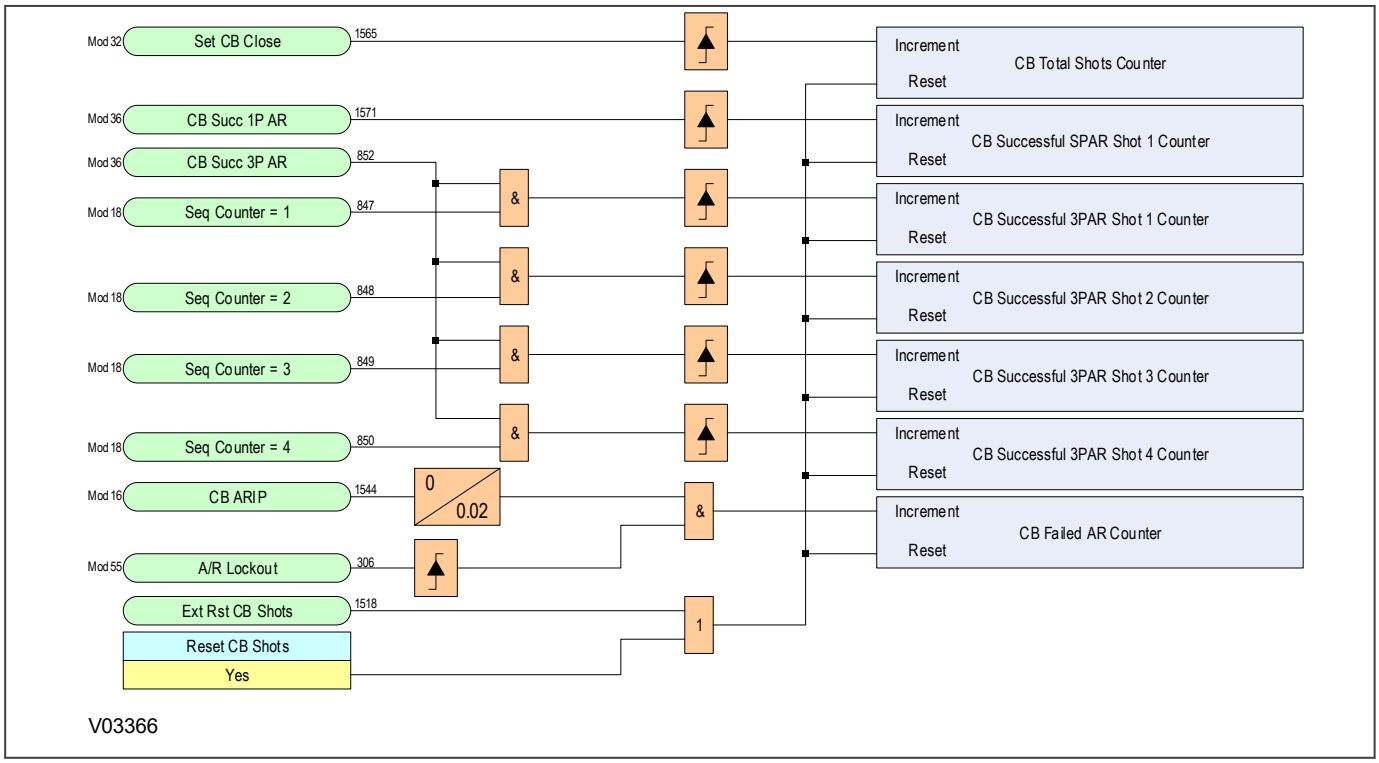


Figure 69: Autoreclose Shot Counters logic diagram (Module 41)

6.4.16 CIRCUIT BREAKER CONTROL

6.4.16.1 CB CONTROL LOGIC DIAGRAM

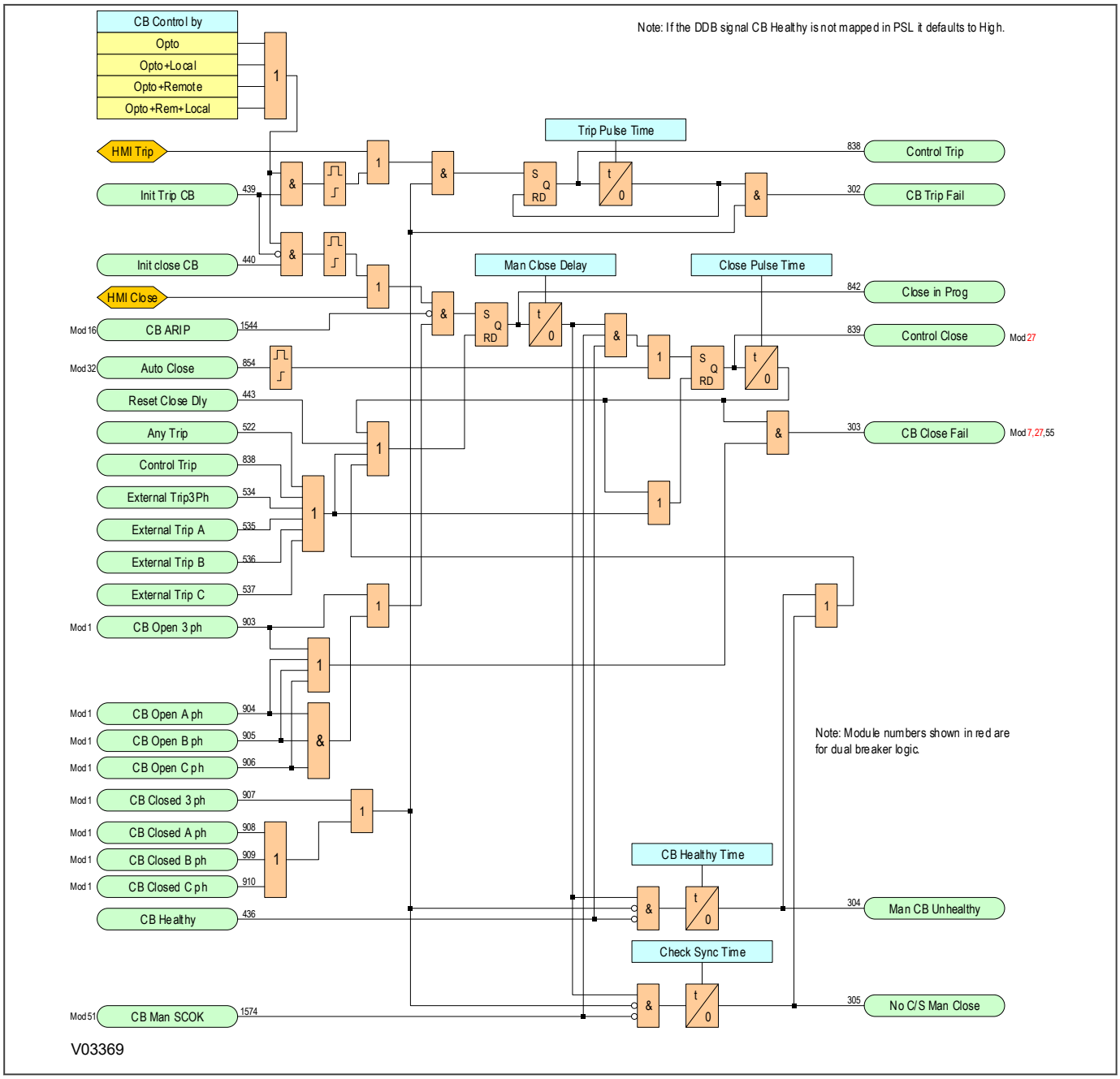


Figure 70: CB Control logic diagram (Module 43)

6.4.17 CIRCUIT BREAKER TRIP TIME MONITORING

The circuit breaker trip time monitoring logic checks for correct circuit breaker tripping following the issue of a protection trip signal. When the protection trip signal is issued, a timer controlled by the ***Trip Pulse Time*** setting in the *CB CONTROL* column is started.

If the circuit breaker trips correctly the timer resets. If Autoreclose is enabled and the timer resets, the cycle continues. If the circuit breaker fails to trip correctly within the set time, the Autoreclose cycle is forced to lock out and a signal is issued indicating that the circuit breaker failed to trip in response to the protection operation.

6.4.17.1 CB TRIP TIME MONITORING LOGIC DIAGRAM

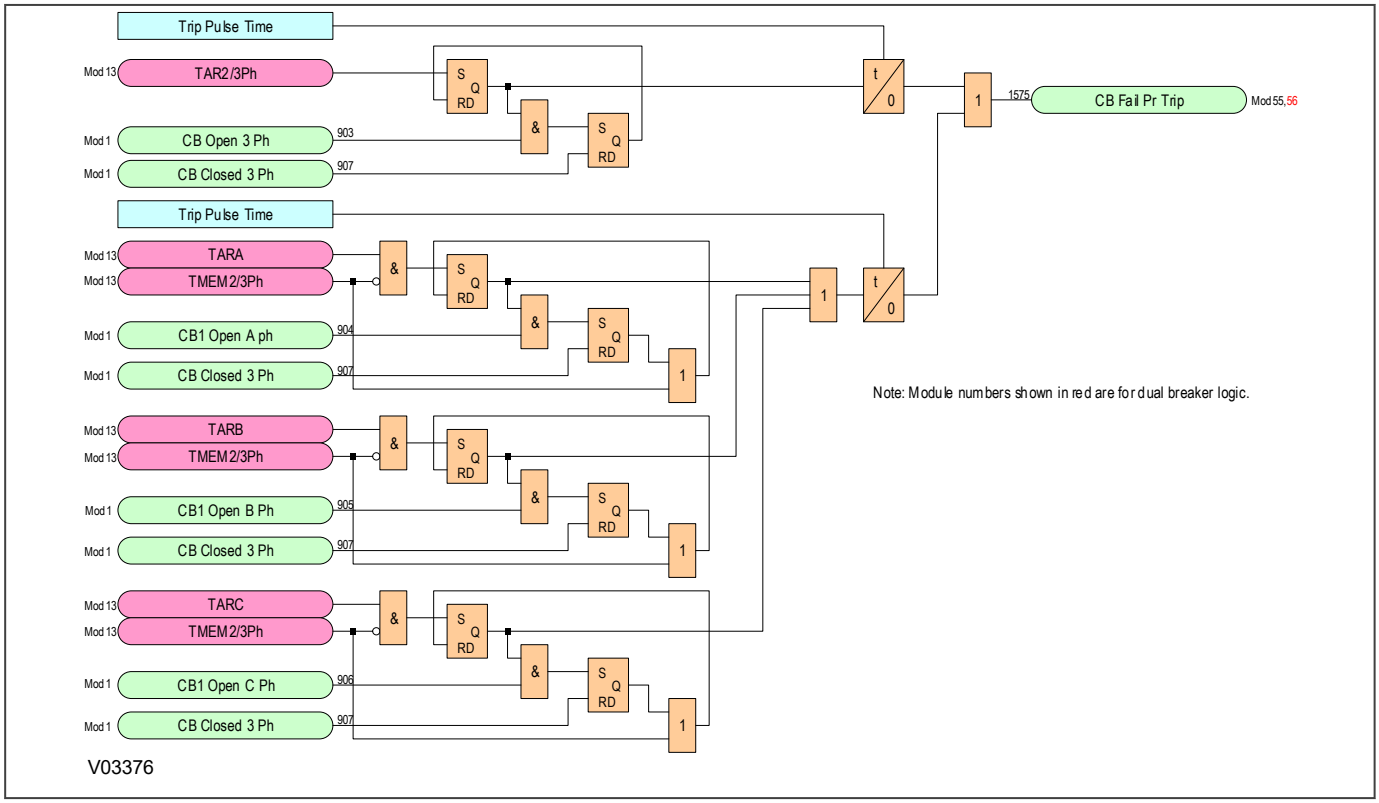


Figure 71: Circuit Breaker Trip Time Monitoring logic diagram (Module 53)

6.4.18 AUTORECLOSE LOCKOUT

A number of events will cause Autoreclose lockout. If this happens an Autoreclose lockout alarm is raised. In this condition, Autoreclose cannot be initiated until the corresponding lockout has been reset.

The following events force Autoreclose lockout:

- Protection operation during reclaim time. Following the final Autoreclose attempt, if the protection operates during the reclaim time, the AR cycle goes to AR lockout and the Autoreclose function is disabled until the AR lockout condition is reset.
- Persistent fault. A fault is considered persistent if the protection re-operates after the last permitted shot.
- Block Autoreclose. If the block Autoreclose DDB is asserted whilst Autoreclose is in progress, the cycle goes to lockout.
- Protection function selection. Setting ‘Block AR’ against a particular protection function in the AUTORECLOSE column means that operation of the protection will block Autoreclose and force lockout.
- Circuit breaker failure to close. If a circuit breaker fails to close Autoreclose is blocked and forced to lockout.
- Circuit breaker remains open at the end of the reclaim time. An Autoreclose lockout is forced if the circuit breaker is open at the end of the reclaim time.

- Circuit breaker fails to close when the close command is issued.
- Circuit breaker fails to trip correctly.
- Three-phase dead time started by 'line dead' violation. If the line does not go dead within the ***Dead Line Time*** setting, the logic forces the Autoreclose sequence to lockout. Determination of when to start the timer is made in the ***3PDTStart WhenLD*** setting.
- Multi-phase faults. The logic can be set to block Autoreclose either for two-phase or three-phase faults, or to block Autoreclose for three-phase faults only. For this, the setting ***Multi Phase AR*** in the *AUTORECLOSE* column applies.
- Single-phase evolving into multi-phase fault. A discriminating time (***Discrim Time*** in the *AUTORECLOSE* settings) is provided for this feature If, after expiry of the discriminating time, a single-phase fault evolves into a two-phase or three-phase fault, the internal signal 'Evolve Lock' is asserted and the Autoreclose is forced to lockout.

6.4.18.1 CB LOCKOUT LOGIC DIAGRAM

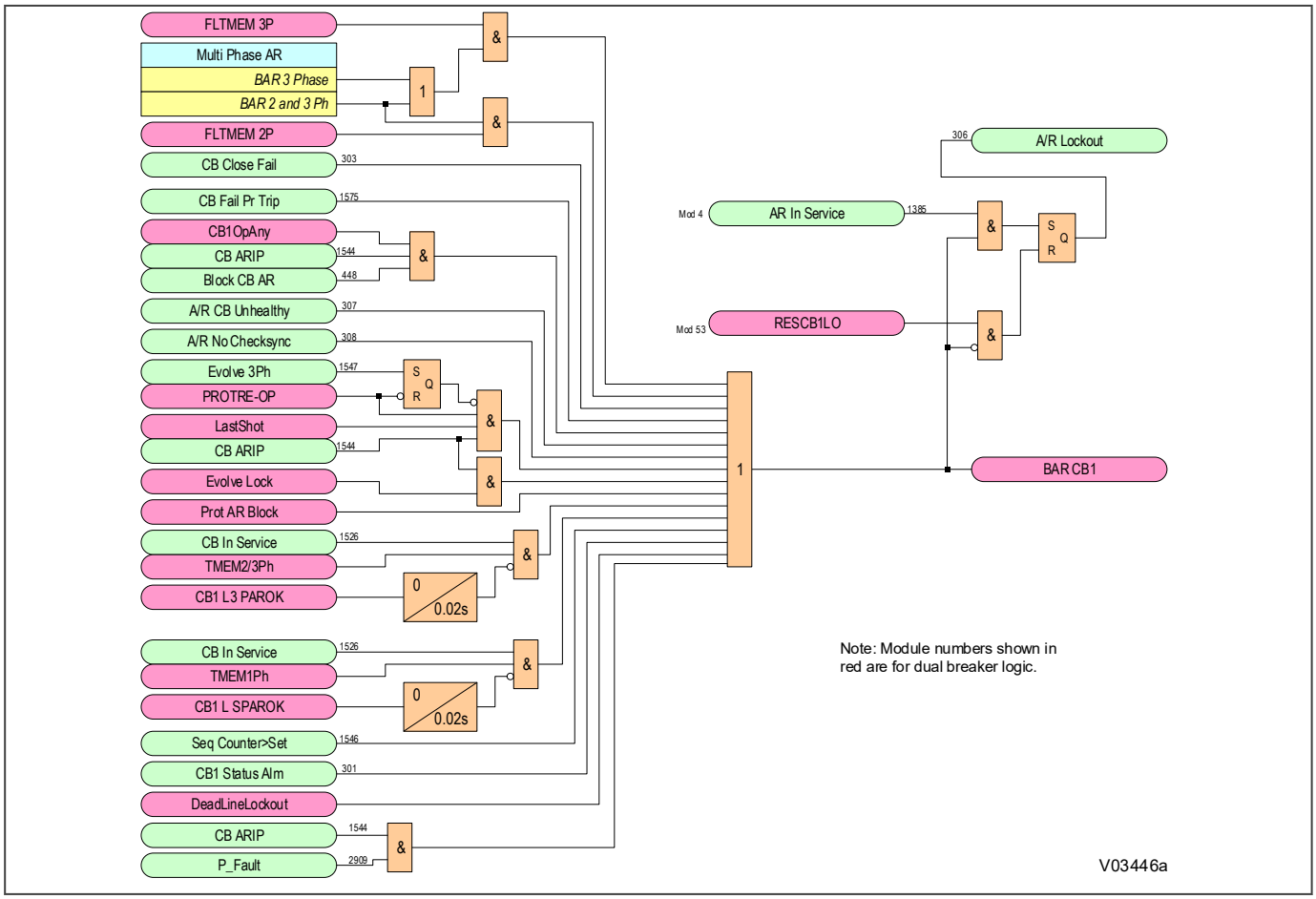


Figure 72: AR Lockout Logic Diagram (Module 55)

6.4.19 RESET CIRCUIT BREAKER LOCKOUT

Lockout conditions caused by the circuit breaker condition monitoring functions can be reset according to the condition of the ***Rst CB mon LO*** by setting found in the *CB CONTROL* column. There are two options; `CB Close` and `User interface`.

If set to `CB Close`, a timer setting, ***CB mon LO RstDly***, becomes visible. When the circuit breaker closes, the ***CB mon LO RstDly*** time starts. The lockout is reset when the timer expires.

If set to `User Interface` then a command, ***CB mon LO reset***, becomes visible. This command can be used to reset the lockout from a user interface.

An Autoreclose lockout generates an Autoreclose lockout alarm. Autoreclose lockout conditions can be reset by various commands and setting options found under the *CB CONTROL* column.

If ***Res LO by CB IS*** is set to `Enabled`, a lockout is reset if the circuit breaker is successfully closed manually. For this, the circuit breaker must remain closed long enough so that it enters the “In Service” state.

If ***Res LO by UI*** is set to `Enabled`, the circuit breaker lockout can be reset from a user interface using the reset circuit breaker lockout command in the *CB CONTROL* column.

If ***Res LO by NoAR*** is set to `Enabled`, the circuit breaker lockout can be reset by temporarily generating an ***AR disabled*** signal.

If ***Res LO by TDelay*** is set to `Enabled`, the circuit breaker lockout is automatically reset after a time delay set in the ***LO Reset Time*** setting.

If ***Res LO by ExtDDB*** is `Enabled`, the circuit breaker lockout can be reset by activation of an external input mapped in the PSL to the relevant reset lockout DDB signal.

6.4.19.1 RESET CB LOCKOUT LOGIC DIAGRAM

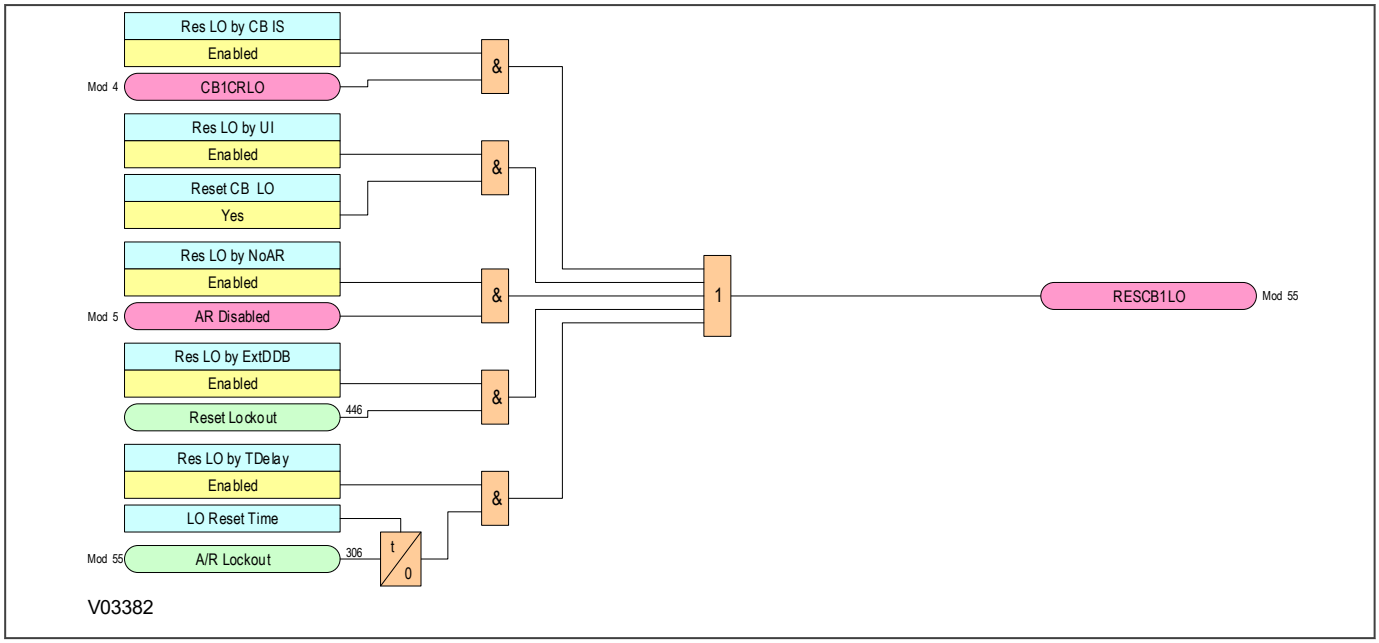


Figure 73: Reset Circuit Breaker Lockout Logic Diagram (Module 57)

6.4.20 POLE DISCREPANCY

In a three-pole CB, certain combinations of poles open and closed are indicative of a problem. The Pole Discrepancy Logic combines an indication of a Pole Discrepancy condition from the CB Monitoring logic with signals from the internal Autoreclose logic to produce a combined Pole Discrepancy indication for the CB.

6.4.20.1 POLE DISCREPANCY LOGIC DIAGRAM

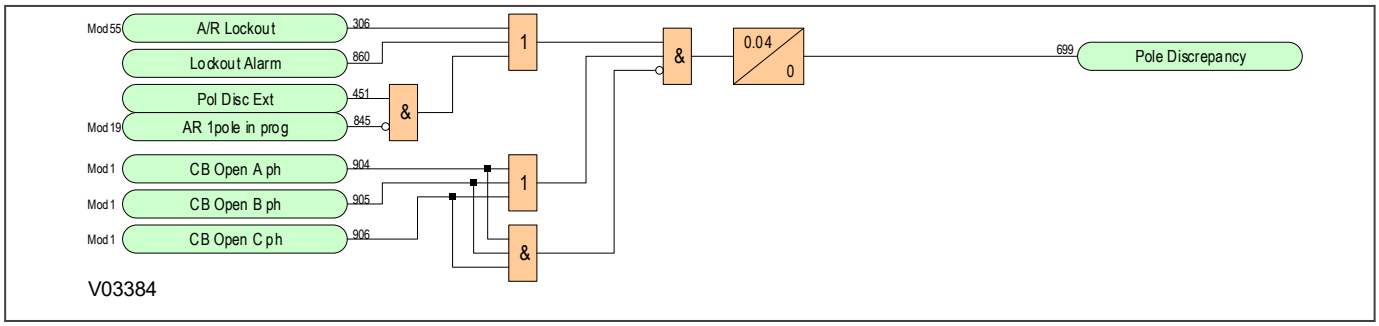


Figure 74: Pole Discrepancy Logic Diagram (Module 62)

6.4.21 CIRCUIT BREAKER TRIP CONVERSION

Circuit breakers should only trip single-pole or three-pole. The trip conversion logic ensures that the tripping is either single-pole or three-pole. The trip conversion logic ensures that all conditions that should cause three-pole tripping do so. Indication of the number of phases that caused tripping is provided.

6.4.21.1 CB TRIP CONVERSION LOGIC DIAGRAM

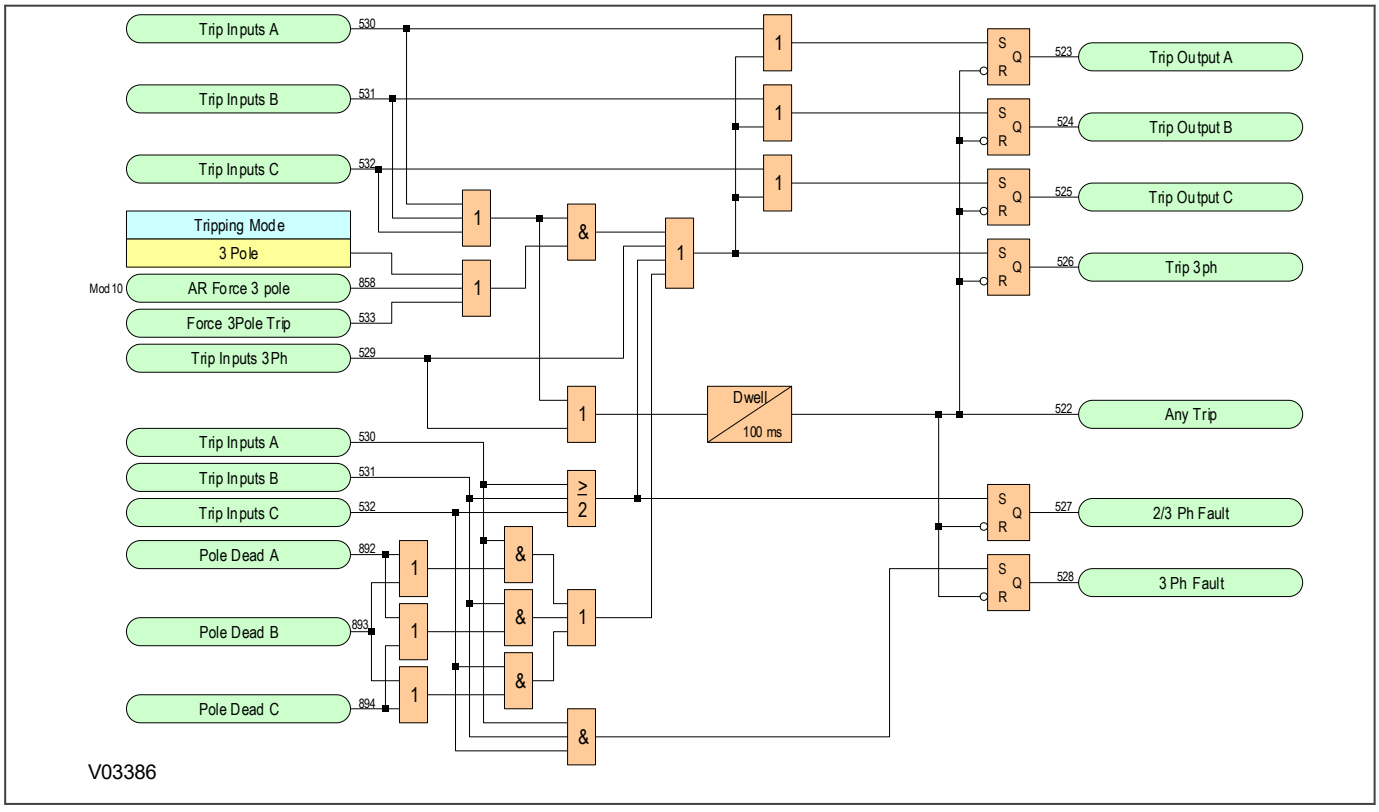


Figure 75: Circuit Breaker Trip Conversion Logic Diagram (Module 63)

6.4.22 MONITOR CHECKS FOR CB CLOSURE

For single-phase Autoreclose neither voltage nor synchronisation checks are needed as synchronising power should be flowing in the two healthy phases. For three-phase Autorelcose, for the first shot (and only the first shot), you can choose to attempt reclosure without performing a synchronisation check. The setting to permit Autoreclose without checking synchronising conditions is ***CB SC Shot 1***.

Otherwise, synchronising checks on voltages, relative frequencies, and relative phase angles are needed to ensure that sympathetic conditions exist before CB closure is attempted.

The following diagrams detail the Monitor Checks for CB closure.

6.4.22.1 VOLTAGE MONITOR FOR CB CLOSURE

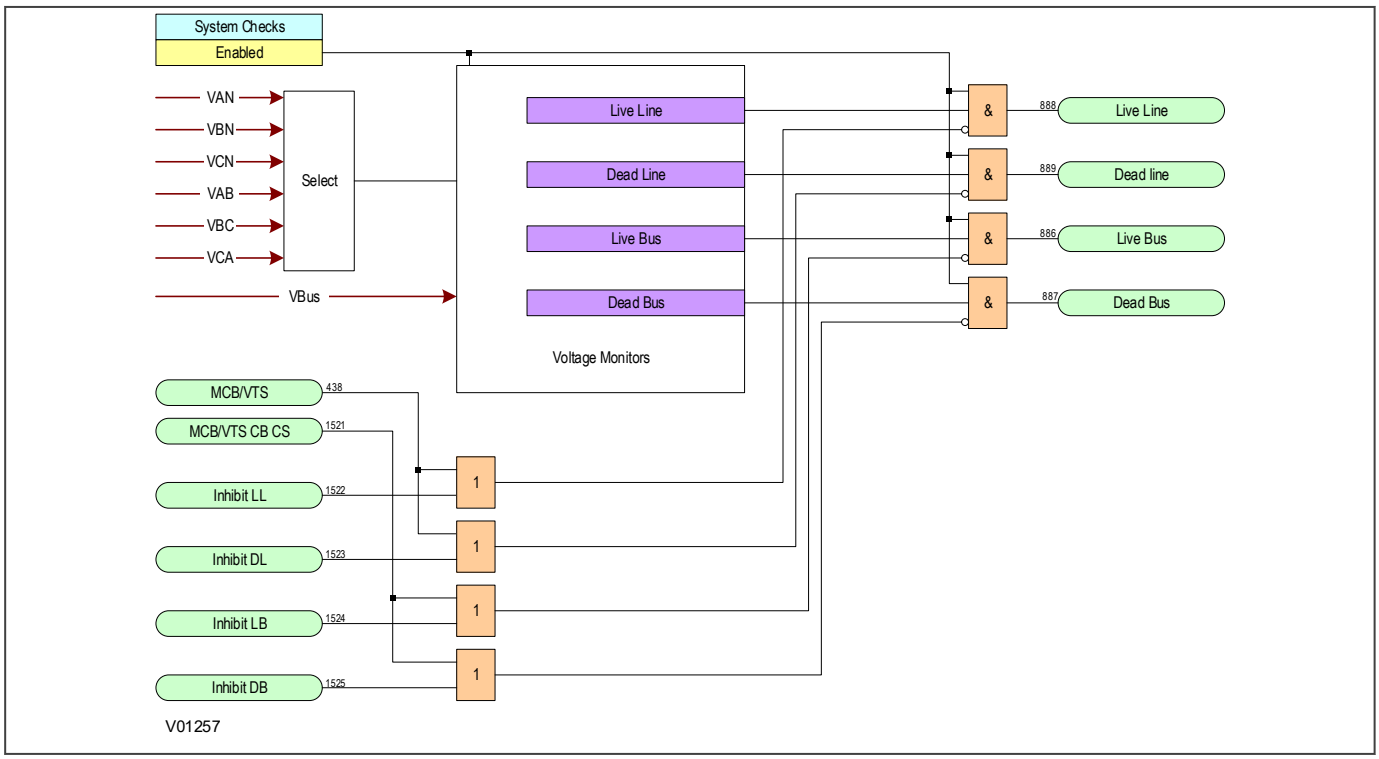


Figure 76: Voltage Monitor for CB Closure (Module 59)

6.4.22.2 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

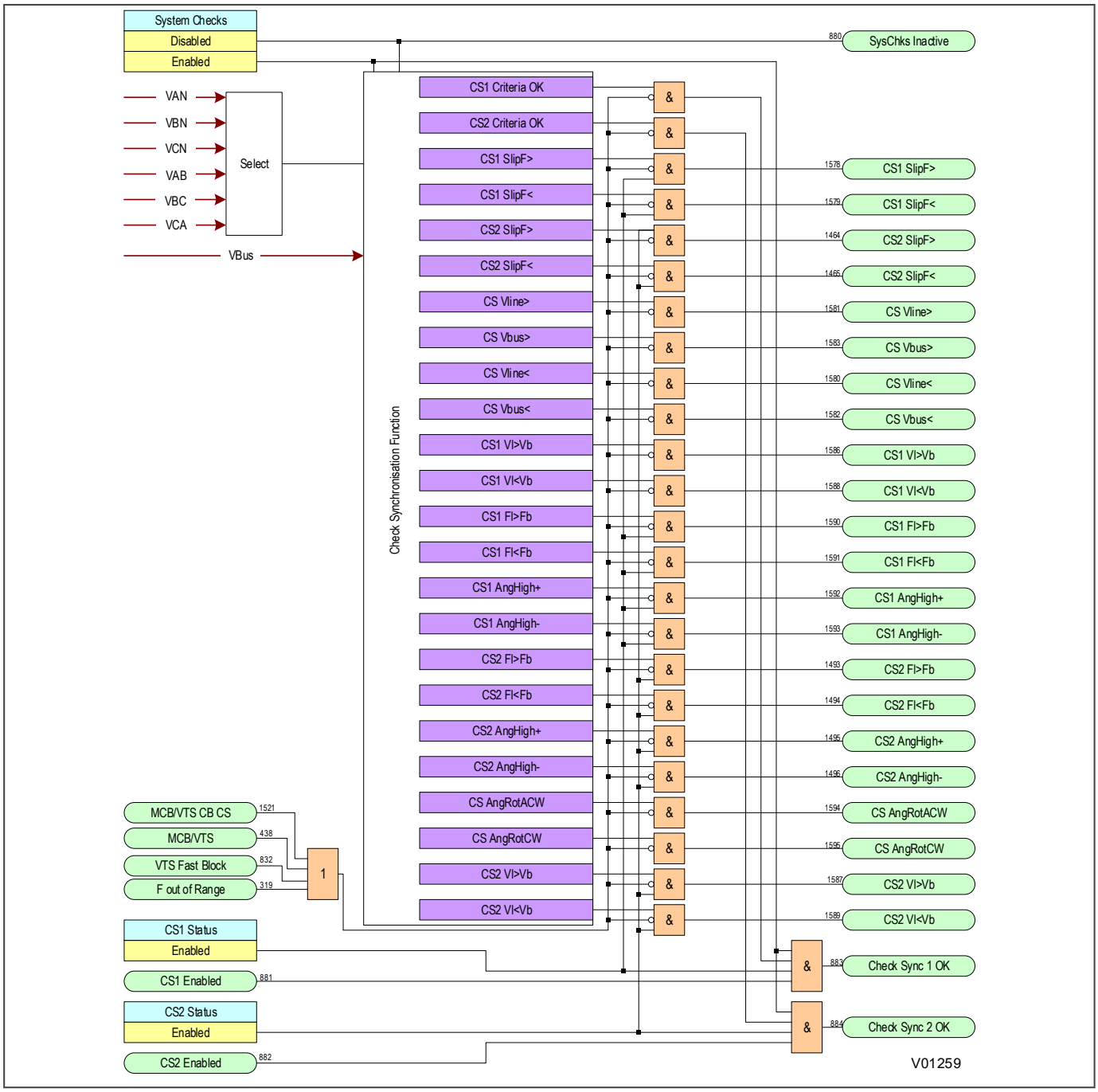


Figure 77: Check Synchronisation Monitor for CB closure (Module 60)

6.4.23 SYNCHRONISATION CHECKS FOR CB CLOSURE

Logical checking of the outputs from the CB closure monitors is performed to generate signals to indicate that it is OK to close circuit breakers.

Signals are provided to indicate that manual CB closure conditions are OK (***CB Man SCOK***), as are signals to indicate that automatic CB closure conditions are OK (***CB SCOK*** and ***CB Fast SCOK***). The ***CB Fast SCOK*** signal allows CB autoreclosure without waiting for the Dead Time to expire.

For single-phase Autoreclose no voltage or synchronism check is required as synchronising power is flowing in the two healthy phases. Three-phase Autoreclose can be performed without checking that voltages are in synchronism for the first shot (and only the first shot). The settings to permit Autoreclose without checking voltage synchronism on the first shot are:

- ***CB1L SC Shot 1*** for circuit breaker 1 as a leader,
- ***CB1F SC Shot 1*** for circuit breaker 1 as a follower,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a leader,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a follower.

When the circuit breaker has closed, the Autoreclose function asserts a DDB signal ***Set CB1 Close***, which indicates that an attempt has been made to close the circuit breaker. At this point, the Reclaim Time starts. If the circuit breaker remains closed after the reclaim timer expires, the Autoreclose cycle is complete, and signals are generated to indicate that Autoreclose was successful. These are:

- ***CB1 Succ 1P AR*** (Single-phase Autoreclose CB1)
- ***CB2 Succ 1P AR*** (Single-phase Autoreclose CB2)
- ***CB1 Succ 3P AR*** (Three-phase Autoreclose CB1)
- ***CB2 Succ 3P AR*** (Three-phase Autoreclose CB2)

These signals increment the relevant circuit breaker successful Autoreclose shot counters, as well as resetting the Autoreclose in progress signal.

The relevant circuit breaker successful Autoreclose shot counters are:

- ***CB1 SUCC SPAR*** (Single-phase Autoreclose CB1)
- CB1 SUCC 3PAR Shot1 (Three-phase Autoreclose CB1, Shot 1)
- CB1 SUCC 3PAR Shot2 (Three-phase Autoreclose CB1, Shot 2)
- CB1 SUCC 3PAR Shot3 (Three-phase Autoreclose CB1, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB1, Shot 4)
- ***CB2 SUCC SPAR*** (Single-phase Autoreclose CB2)
- CB2 SUCC 3PAR Shot1 (Three-phase Autoreclose CB2, Shot 1)
- CB2 SUCC 3PAR Shot2 (Three-phase Autoreclose CB2, Shot 2)
- CB2 SUCC 3PAR Shot3 (Three-phase Autoreclose CB2, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB2, Shot 4)

6.4.23.1 THREE-PHASE AUTORECLOSE SYSTEM CHECK LOGIC DIAGRAM

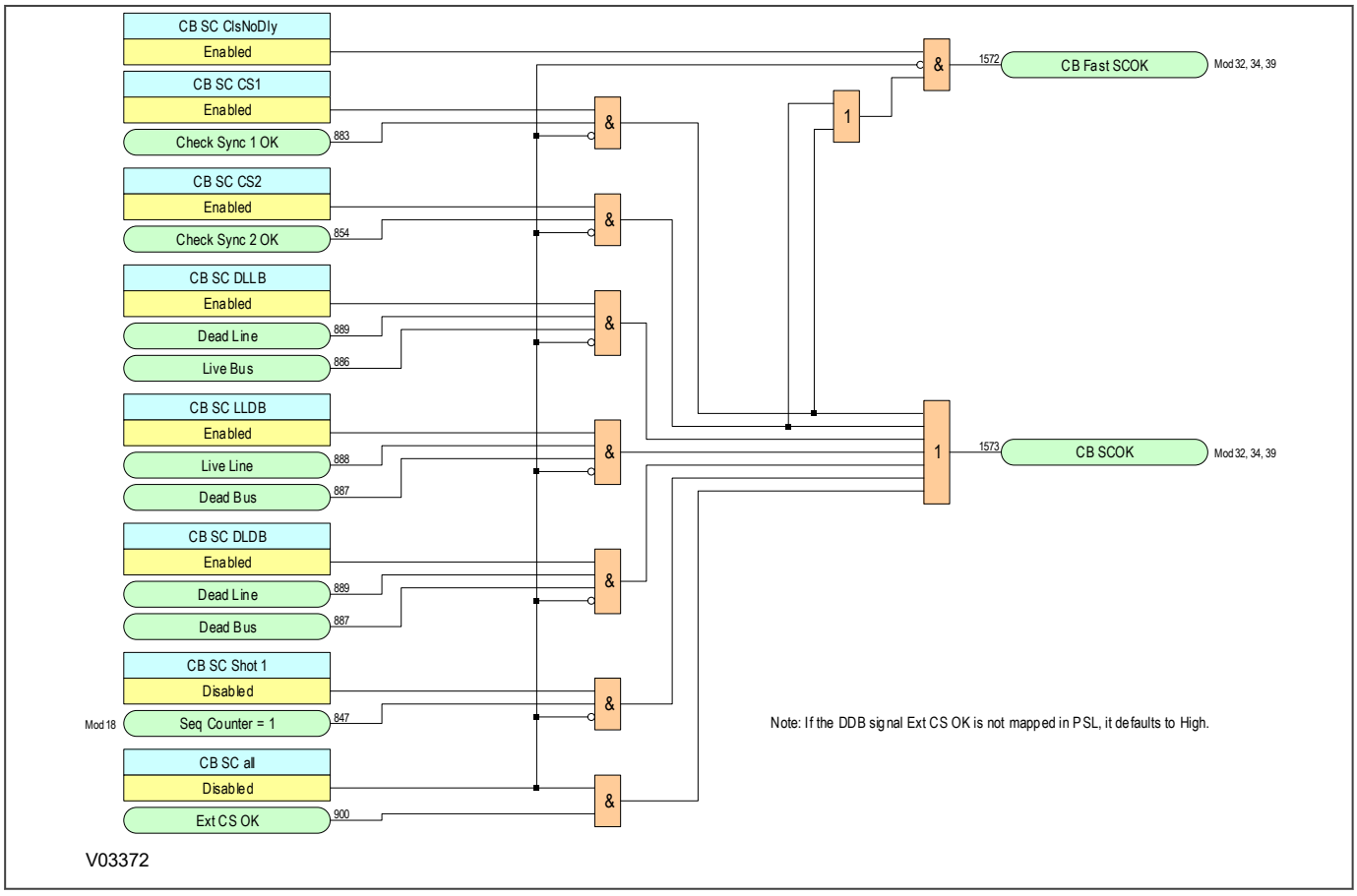


Figure 78: Three-phase Autoreclose System Check Logic Diagram (Module 45)

6.4.23.2 CB MANUAL CLOSE SYSTEM CHECK LOGIC DIAGRAM

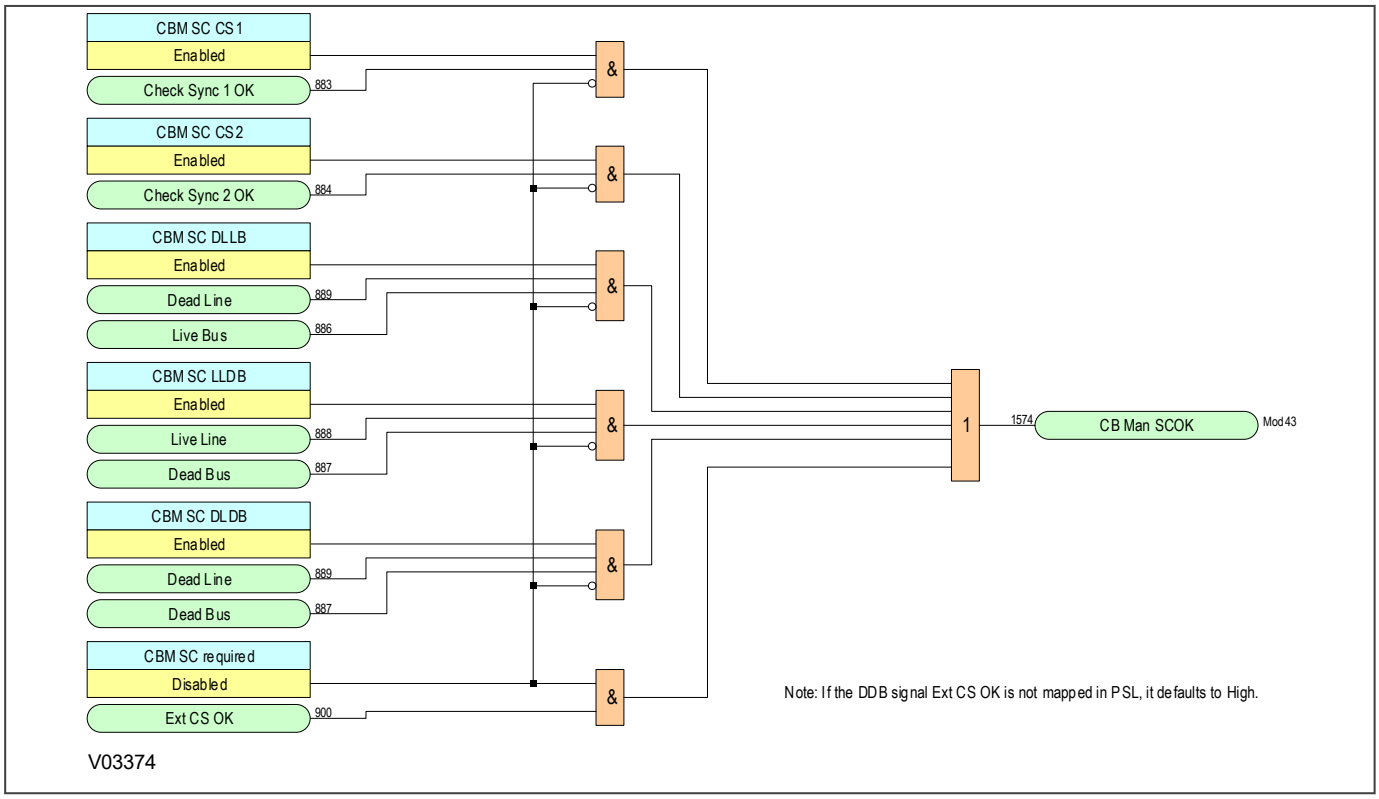


Figure 79: CB Manual Close System Check Logic Diagram (Module 51)

6.5 LOGIC MODULES (DUAL CB)

This section contains a complete set of logic diagrams for dual CB models, which will help to explain the Autoreclose function. Most of the logic diagrams shown are logic modules that comprise the overall Autoreclose system. Some of the diagrams shown are not directly related to Autoreclose functionality, however, they may use some inputs are produce outputs that are used by the Autoreclose system. These diagrams are shown in this section for the sake of completeness.

6.5.1 CIRCUIT BREAKER STATUS MONITOR

The Circuit Breaker State Monitor logic is part of the Monitoring and Control functionality and is fully described in that chapter. The logic diagram is repeated in this section because some of the outputs of this logic module are used as inputs to some of the Autoreclose logic modules.

6.5.1.1 CB STATE MONITOR

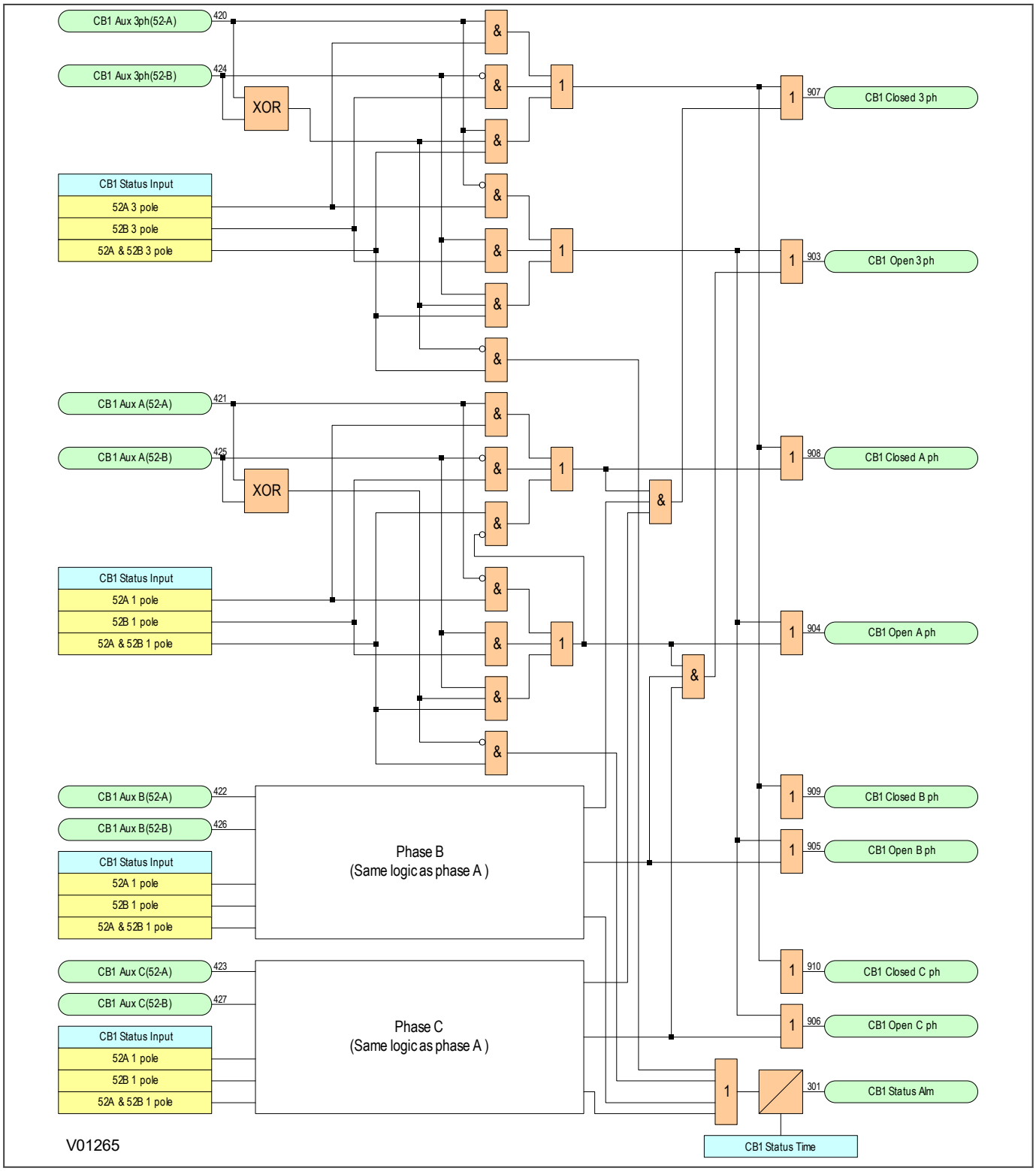


Figure 80: CB State logic diagram (Module 1)

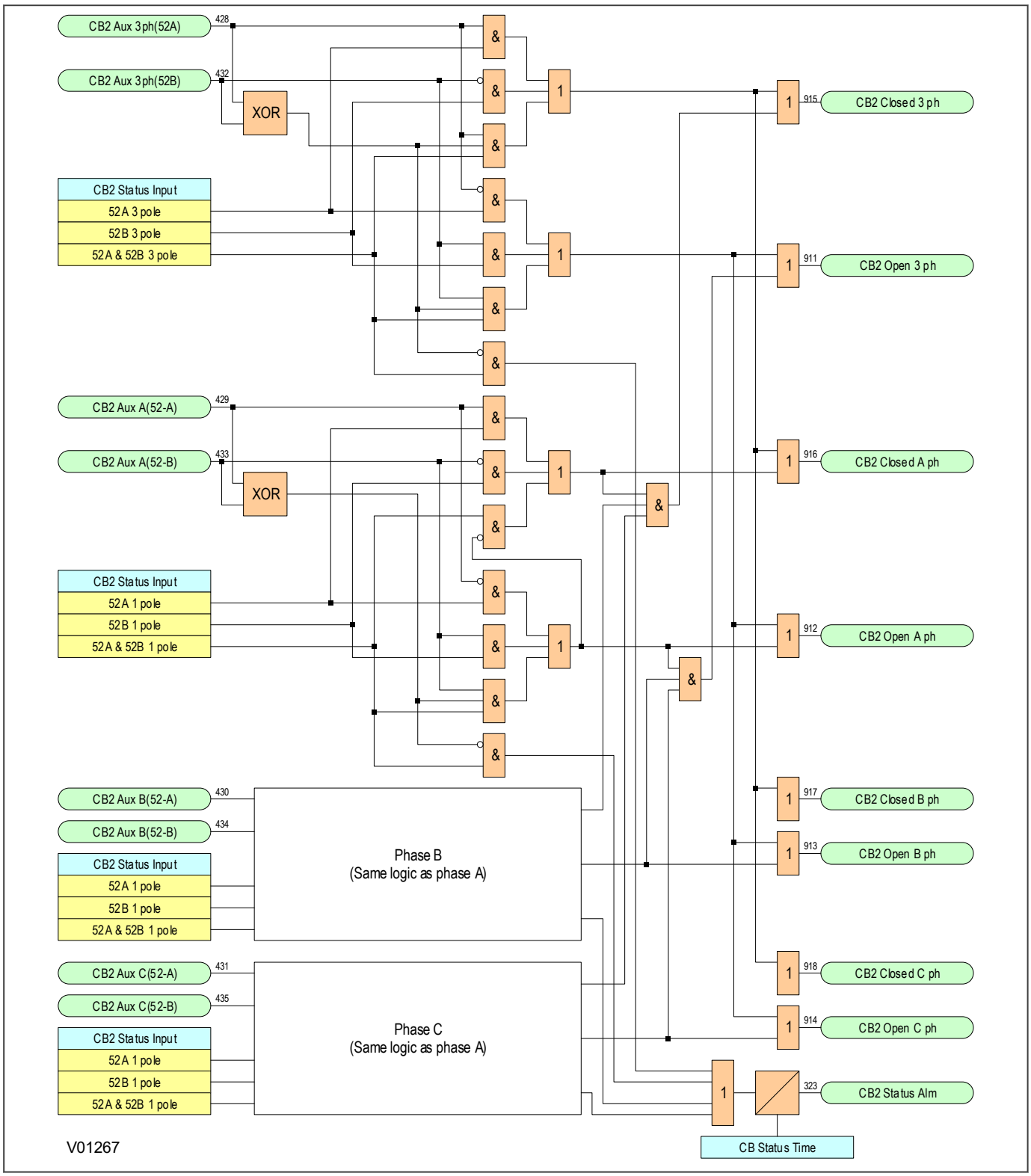


Figure 81: CB State logic diagram (Module 2)

6.5.2 CIRCUIT BREAKER OPEN LOGIC

The Circuit Breaker Open logic module produces internal signals indicating the open status of one or more phases. These signals are used by some of the Autoreclose logic modules.

6.5.2.1 CIRCUIT BREAKER OPEN LOGIC DIAGRAM

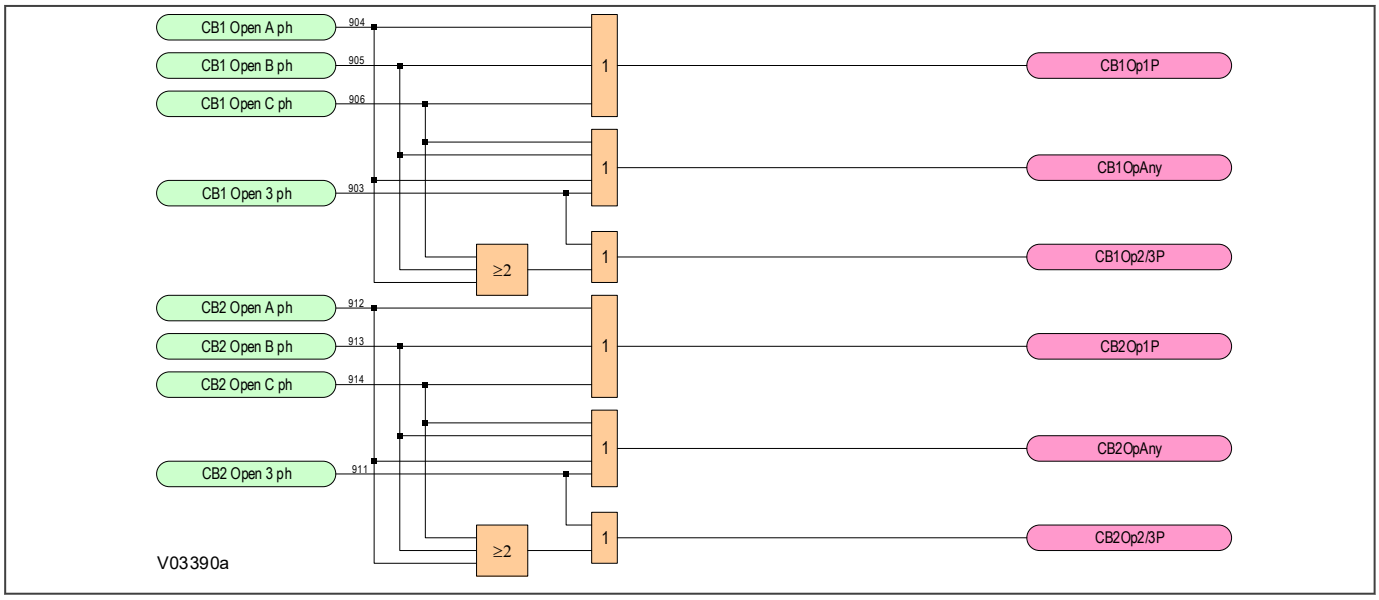


Figure 82: Circuit Breaker Open logic diagram (Module 3)

6.5.3 CIRCUIT BREAKER IN SERVICE LOGIC

For Autoreclose to proceed, a circuit breaker has to be in service when the Autoreclose is initiated. A circuit breaker is considered to be in service if it has been closed for more than the CB IS Time setting.

For applications with fast-acting circuit breaker auxiliary switches, a time delay setting CB IS Memory Time is provided. This is used to ensure correct operation if a delay between the circuit breaker tripping and recognition by the protection, is expected.

When an Autoreclose cycle starts, the “in service” signal for a circuit breaker stays set until the Autoreclose cycle finishes.

The circuit breaker “in service” signal resets if the circuit breaker opens, or if the corresponding Autoreclose in progress (ARIP) signal resets.

6.5.3.1 CIRCUIT BREAKER IN SERVICE LOGIC DIAGRAM

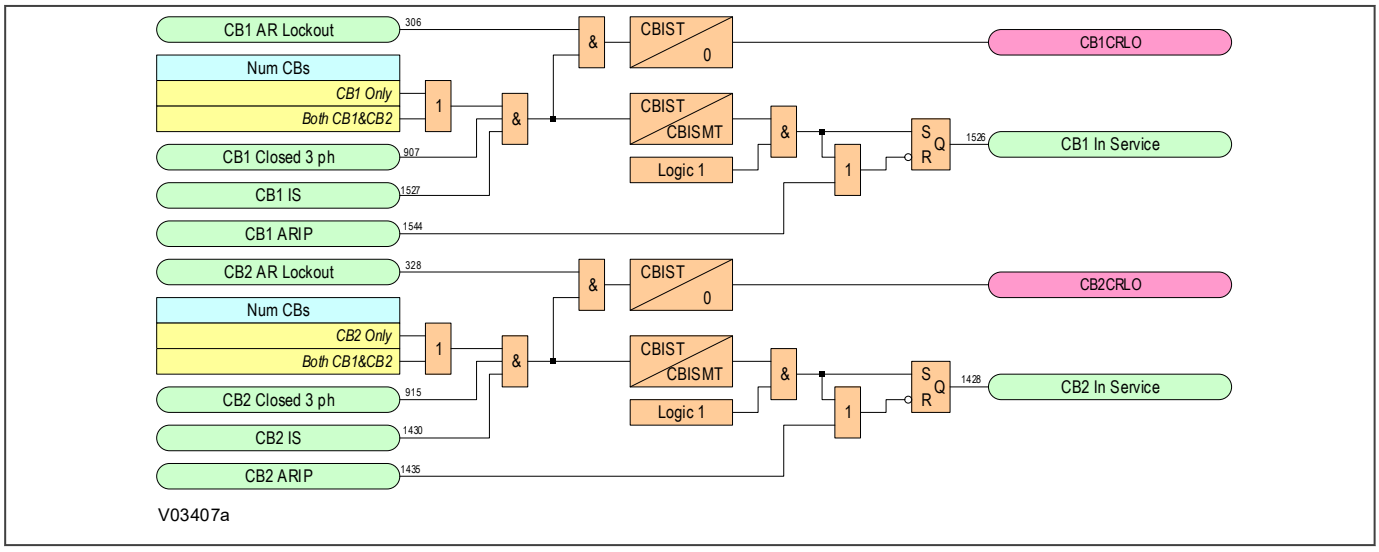


Figure 83: CB In Service logic diagram (Module 4)

6.5.4 AUTORECLOSE ENABLE LOGIC

The Autoreclose function must be enabled in the *CONFIGURATION* column before it can be brought into service. It can be brought into service by:

- using an opto-input mapped to the ***AR Enable*** DDB signal
- pulsing the DDB signal ***AR On Pulse*** (use ***AR Off Pulse*** to bring it out of service)
- programming a function key on the HMI.
- if applicable, using IEC 60870-5-103 communications

Further validation signals are also required to switch on Autoreclose. These are the DDB signals ***AR Enable CB1*** and ***AR Enable CB2***. Once Autoreclose is in service, the ***AR In Service*** DDB signal is asserted and the ***AR Status*** cell in the *CB CONTROL* column is set accordingly.

6.5.4.1 AUTORECLOSE ENABLE LOGIC DIAGRAM

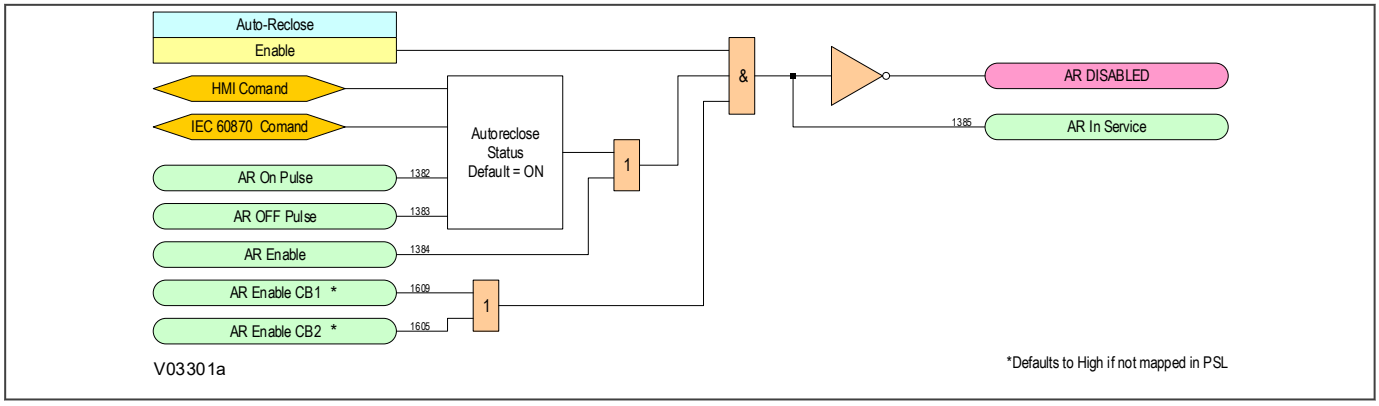


Figure 84: Autoreclose Enable logic diagram (Module 5)

6.5.5 AUTORECLOSE LEADER/FOLLOWER

You can select either CB1 or CB2 to be the leader, with CB2 or CB1 as the follower respectively.

6.5.5.1 LEADER/FOLLOWER CB SELECTION LOGIC DIAGRAM

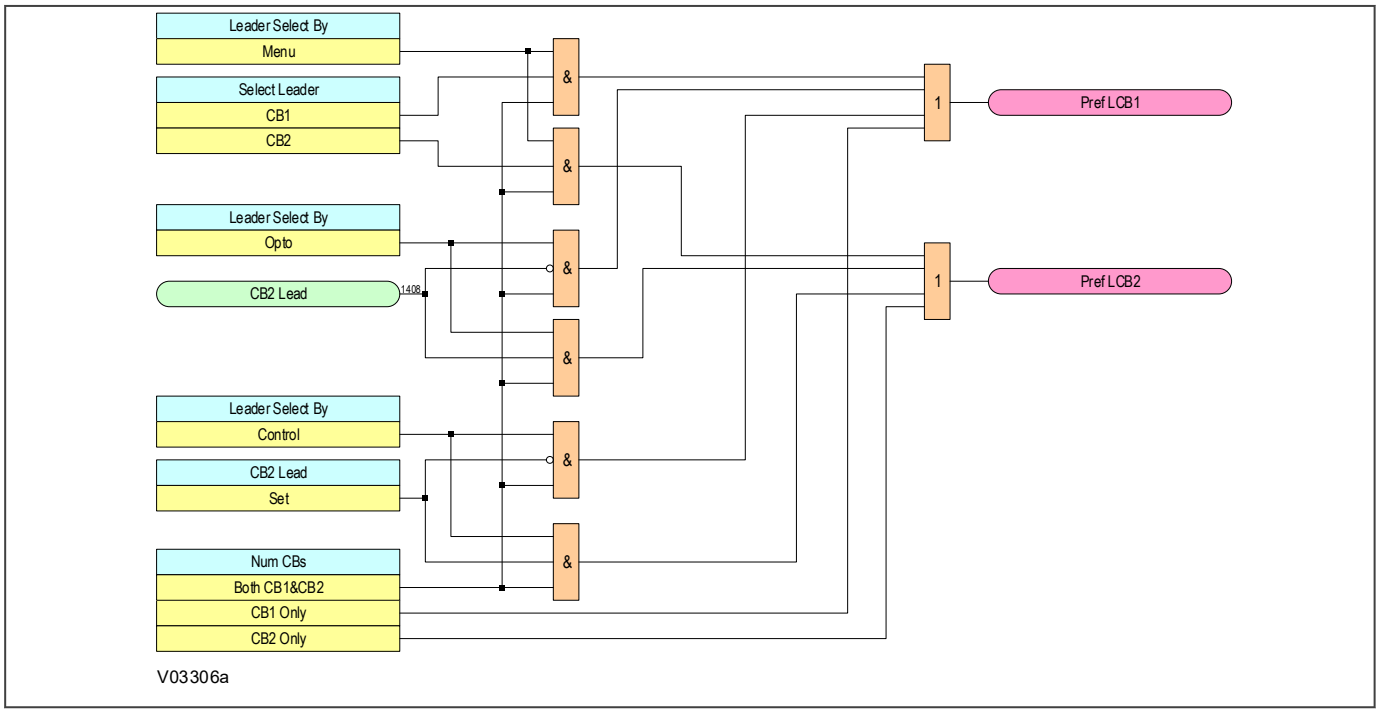


Figure 85: Leader/Follower CB Selection Logic Diagram (Module 6)

6.5.5.2 LEADER FOLLOWER LOGIC DIAGRAM

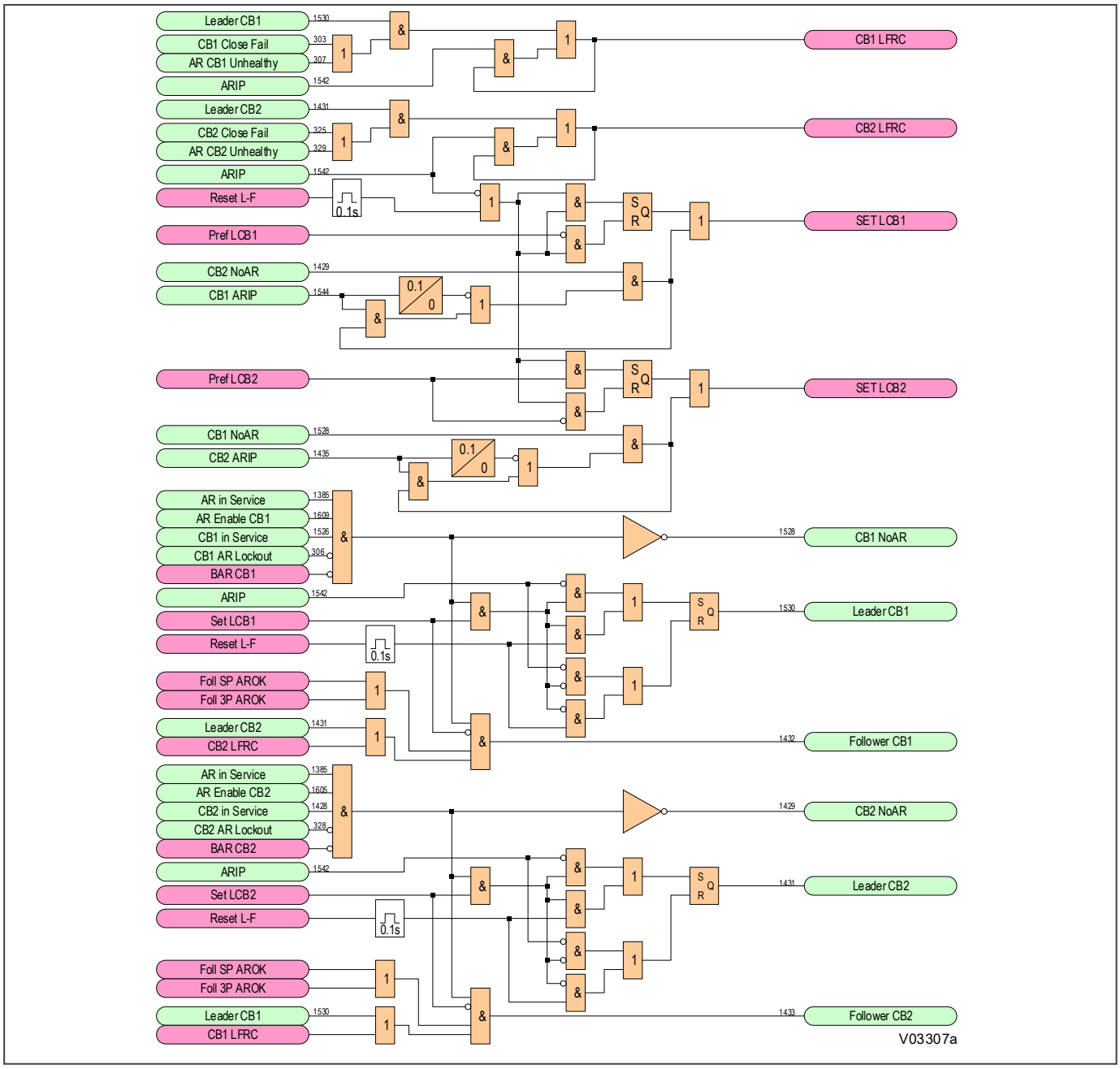


Figure 86: Leader/Follower logic diagram (Module 7 & 8)

6.5.6 AUTORECLOSE MODES

The device can provide Single-phase and/or Three-phase Autoreclose. The Autoreclose mode is configured by the ***AR Mode*** setting in the *AUTORECLOSE* column. You can choose from:

- Single-phase (`AR 1P`)
- Three-phase (`AR 3P`)
- Single-phase and Three-phase (`AR 1/3P`)
- Controlled by commands from DDB signals that must be mapped to opto-isolated inputs in the PSL (`AR Opto`).

Single-phase Autoreclosing is permitted only for the first shot of an Autoreclose cycle. In a multi-shot Autoreclose cycle the second and subsequent trips will always be three-phase.

For multi-phase faults, you can use the ***Multi Phase AR*** setting in the *AUTORECLOSE* column to configure the following options:

- Allow Autoreclose for all fault types (`Allow Autoclose`)
- Block Autoreclose for 2-phase and 3-phase faults (`BAR 2 and 3 ph`)
- Block Autoreclose for 3-phase faults (`BAR 3 Phase`)

6.5.6.1 SINGLE-PHASE AND THREE-PHASE AUTORECLOSE

This section applies to dual-CB devices. Where there are signals and settings for each of the two circuit breakers, only the first CB (CB1) is shown, to improve clarity and save repetition. Where settings and signals include "CB1", there is a "CB2" equivalent.

Single-phase Autoreclose Only

If single-phase Autoreclose is enabled, the logic allows only a single shot Autoreclose. For a single-phase fault, the single phase dead timer ***SP AR Dead Time*** starts, and the DDB signal ***CB1 AR 1p Inprog*** is asserted, which indicates that single-phase Autoreclose is in progress. In this case, for a multi-phase fault the logic triggers a three-phase trip and goes to lockout.

Three-phase Autoreclose Only

During three-phase Autoreclose, for any fault, the three-phase dead timers: ***3P AR DT Shot 1***, ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** are started and the DDB signal is ***CB1 AR 3p InProg*** is asserted, which indicates that three-phase Autoreclose is in progress.

If three-phase only Autoreclose is enabled, the logic forces a three-phase trip by setting the DDB signal ***AR Force CB1 3P*** for any single-phase fault.

Single-phase and Three-phase Autoreclose

With single-phase and three-phase Autoreclose enabled then, if the first fault is a single-phase fault the single-phase dead time ***SP AR Dead Time*** is started and the single-phase Autoreclose in progress signal is asserted. If the first fault is a multi-phase fault the three phase dead timer ***3P AR DT Shot 1*** is started and the three-phase Autoreclose in progress signal is asserted. If set to allow more than one reclose (***AR Shots*** > 1) then any subsequent faults are converted to three-phase trips by setting the force three-pole tripping signal. The three-phase dead times ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** (Dead Times 2, 3, 4) are started for the 2nd, 3rd and 4th trips (shots) respectively. The DDB signal ***CB1 AR 3p InProg*** is asserted. If a single-phase fault evolves to a multi-phase fault during the single-phase dead time (***SP AR Dead Time***), single-phase Autoreclose is stopped. The single-phase Autoreclose in progress signal is reset, the three-phase Autoreclose in progress signal is set, and the three-phase dead timer ***3P AR DT Shot 1*** is started.

6.5.6.2 AUTORECLOSE MODES ENABLE LOGIC DIAGRAM

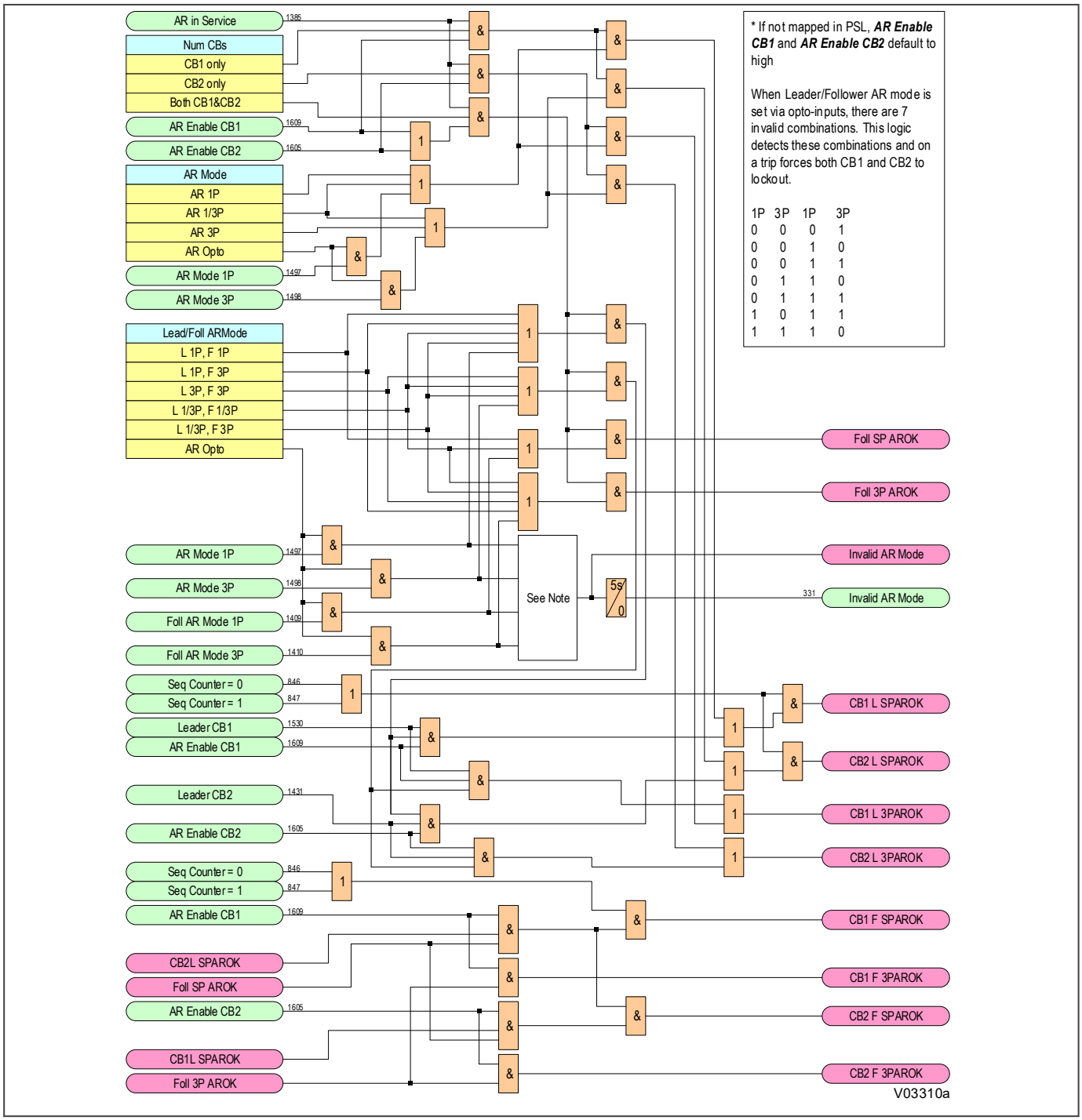


Figure 87: Autoreclose Modes Enable logic diagram (Module 9)

6.5.7 AR FORCE THREE-PHASE TRIP LOGIC

Following single-phase tripping, while the Autoreclose cycle is in progress, and upon resetting of the protection elements, tripping switches to three-phase.

Any protection operations that occur for subsequent faults while the Autoreclose cycle remains in progress will be tripped three-phase.

6.5.7.1 FORCE THREE-PHASE TRIP LOGIC DIAGRAM

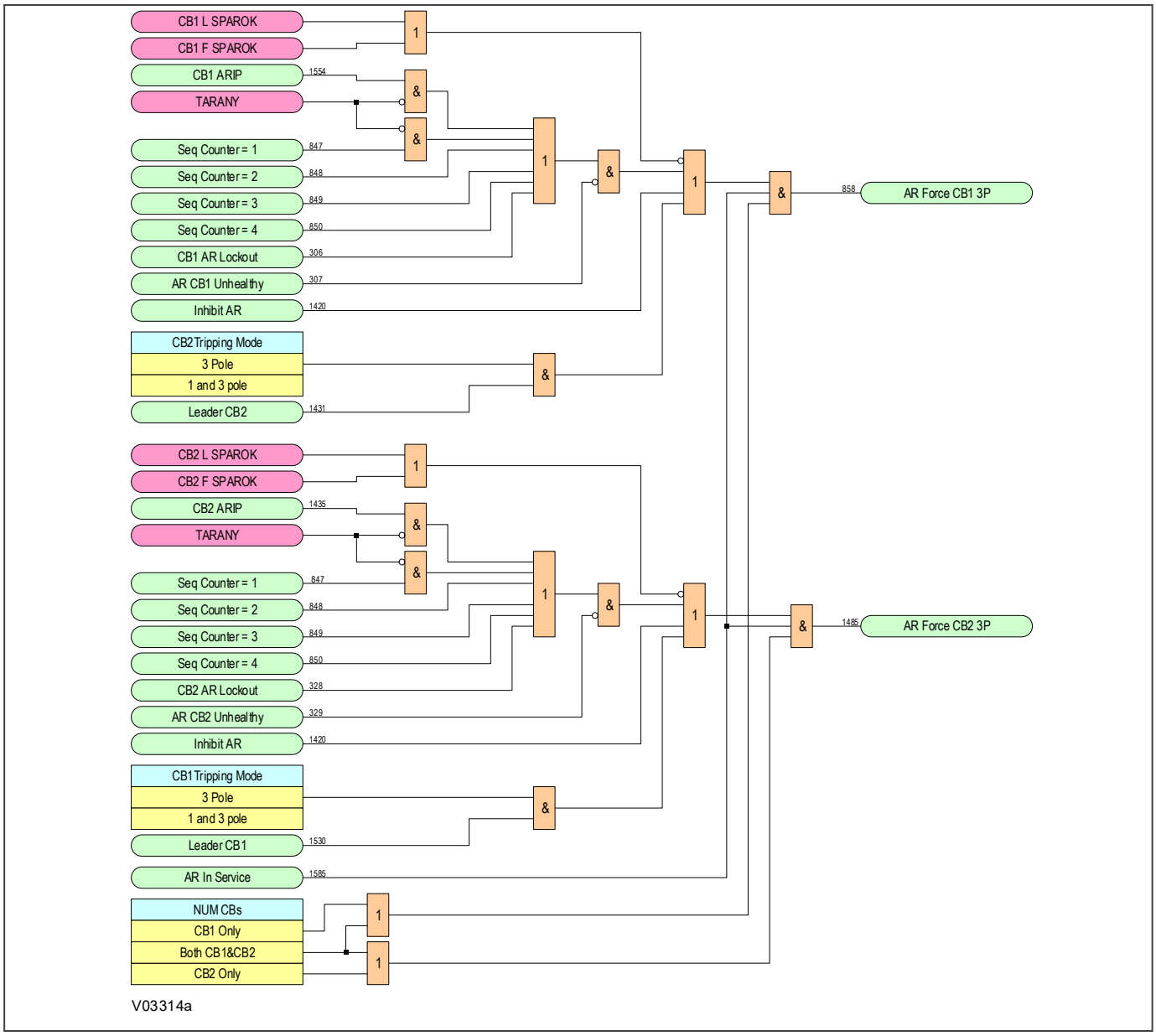


Figure 88: Force three-phase trip logic diagram (Module 10)

6.5.8 AUTORECLOSE INITIATION LOGIC

Autoreclose initiation starts Autoreclose for a circuit breaker only if Autoreclose is enabled for the circuit breaker, and the circuit breaker is in service. When an Autoreclose cycle is started, Autoreclose in progress (ARIP) is indicated. The indication remains until the end of the cycle. The end of the cycle is signified by successful Autoreclose, or by lockout.

Autoreclose cycles can be initiated by:

- Protection functions internal to the product
- A Trip Test feature
- External protection equipment
- Evolving fault combinations

Internal Protection Functions

Many of the protection functions in the product can be programmed to initiate or block Autoreclose. The associated settings are found in the Autoreclose column and the available options are *No Action*, *Initiate AR*, or *Block AR*. If set to *Block AR* operation of the protection function blocks the Autoreclose function and forces a lockout.

Trip Test Feature

The ***Test Autoreclose*** command cell in the *COMMISSION TESTS* column can be used to initiate an Autoreclose cycle. Each option provides a 100 ms pulse output. There is also a 'No Operation' option to exit the command field without initiating a test.

External Protection Equipment

Protection operation from a different device can be used to initiate Autoreclose via PSL. By default these external trip input signals are mapped to initiate Autoreclose. These inputs are not mapped to the trip outputs. With appropriate mapping in the PSL, however, the external device can use this product to trip connected circuit breakers.

Evolving Fault Combinations

The Autoreclose function would normally be initiated by a single condition (such as a single-phase fault). If, however, the system conditions evolve such that other conditions that could initiate Autoreclose, then the dynamics of the Autoreclose logic need to adapt. For example, if a single-phase fault evolves into a multi-phase fault, then the operation of the Autorecloser must consequently adapt. To achieve this signals are generated to indicate conditions such as evolving faults, re-operation of protection, combinations of initiation by internal protection, external protection, or test features, which control the Autoreclose sequencing.

Records of initiating conditions are stored and used to control the sequencing. Initiation can be from a protection function integrated in the product, from external protection and internal sources such as the Autoreclose test function. Initiation can be further qualified by the phases causing the initiation. These conditions are stored in signals that generally feature "MEM"- memory, or "AR" – Autoreclose, in the signal name.

6.5.8.1 AUTORECLOSE INITIATION LOGIC DIAGRAM

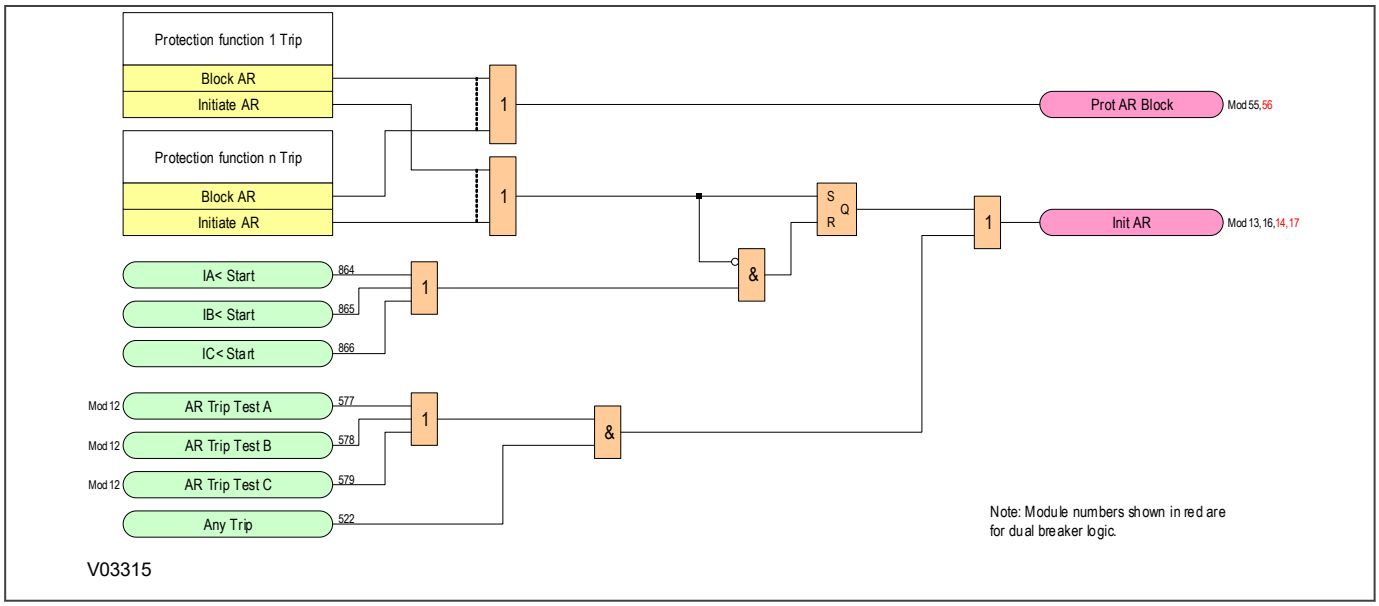


Figure 89: Autoreclose Initiation logic diagram (Module 11)

6.5.8.2 AUTORECLOSE TRIP TEST LOGIC DIAGRAM

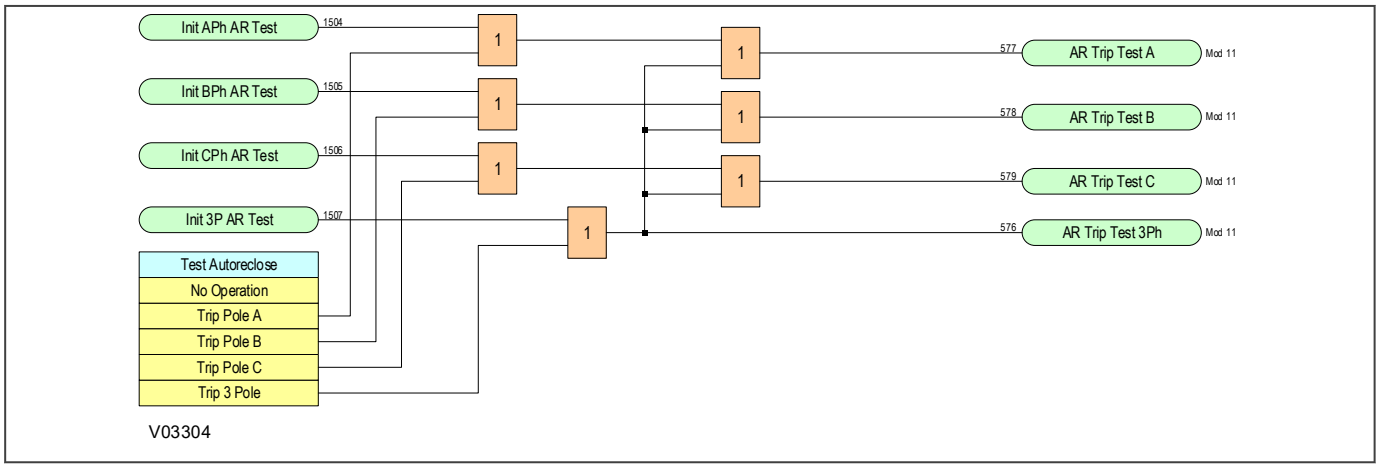


Figure 90: Autoreclose Trip Test logic diagram (Module 12)

6.5.8.3 EXTERNAL TRIP LOGIC DIAGRAM FOR CB1

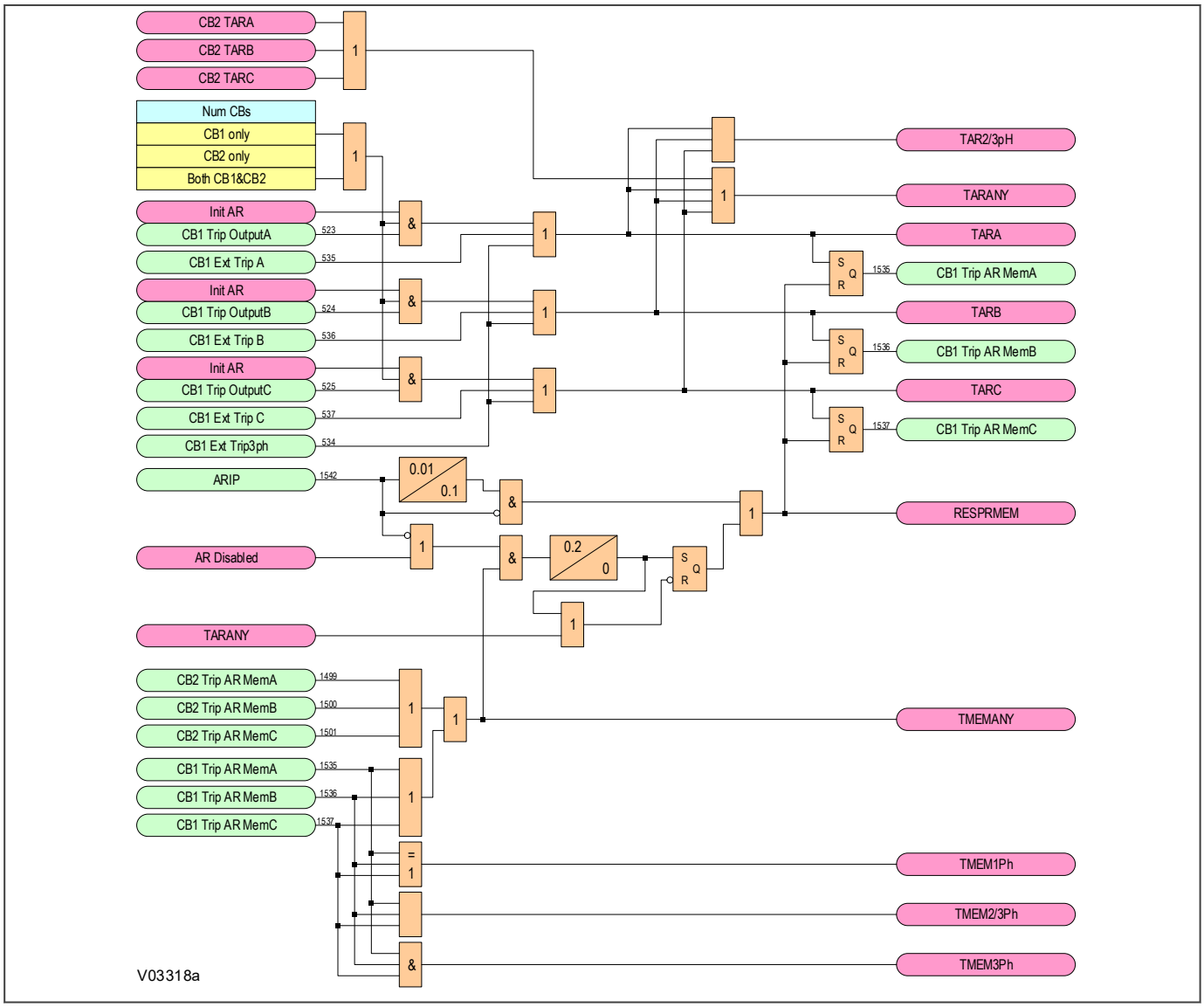


Figure 91: Autoreclose initiation by internal single and three phase trip or external trip for CB1 (Module 13)

Note:
For single-phase Autoreclose, these signals must be mapped as shown in the default PSL scheme.

6.5.8.4 EXTERNAL TRIP LOGIC DIAGRAM FOR CB2

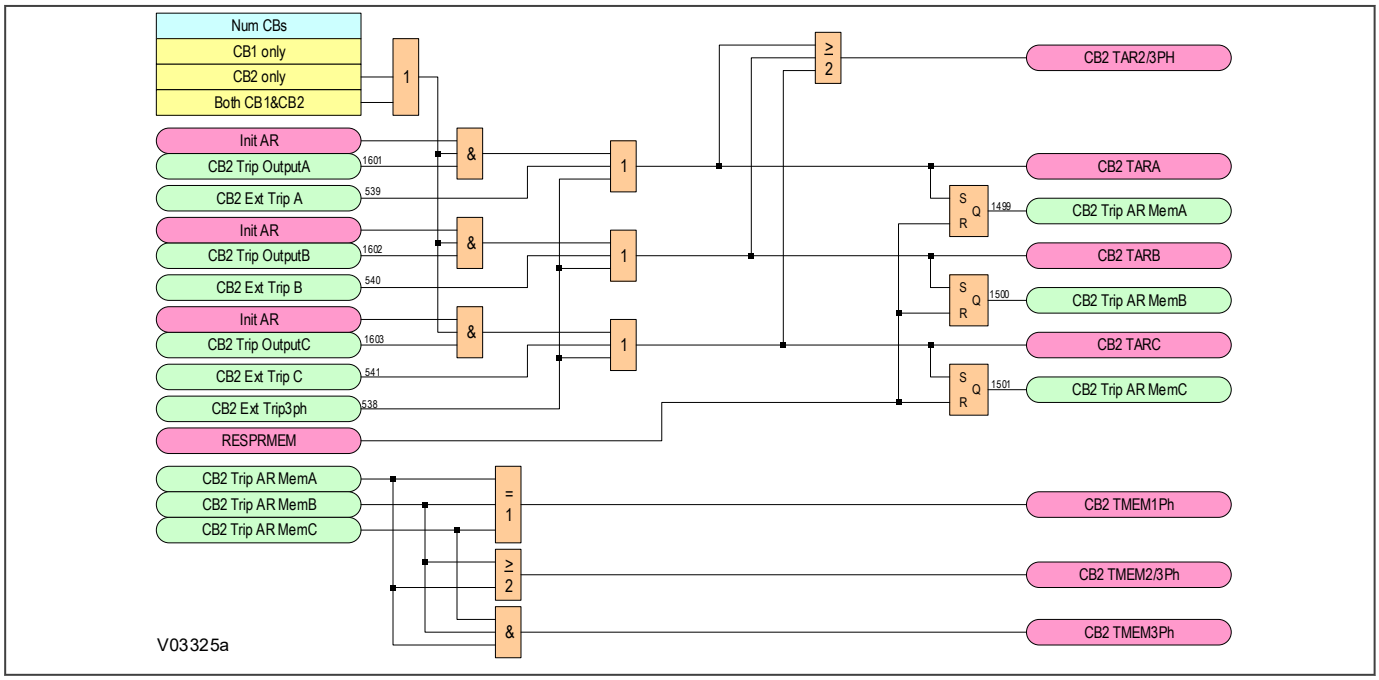


Figure 92: Autoreclose initiation by internal single and three phase trip or external trip for CB2 (Module 14)

Note:
For single-phase Autoreclose, these signals must be mapped as shown in the default PSL scheme.

6.5.8.5 PROTECTION REOPERATION AND EVOLVING FAULT LOGIC DIAGRAM

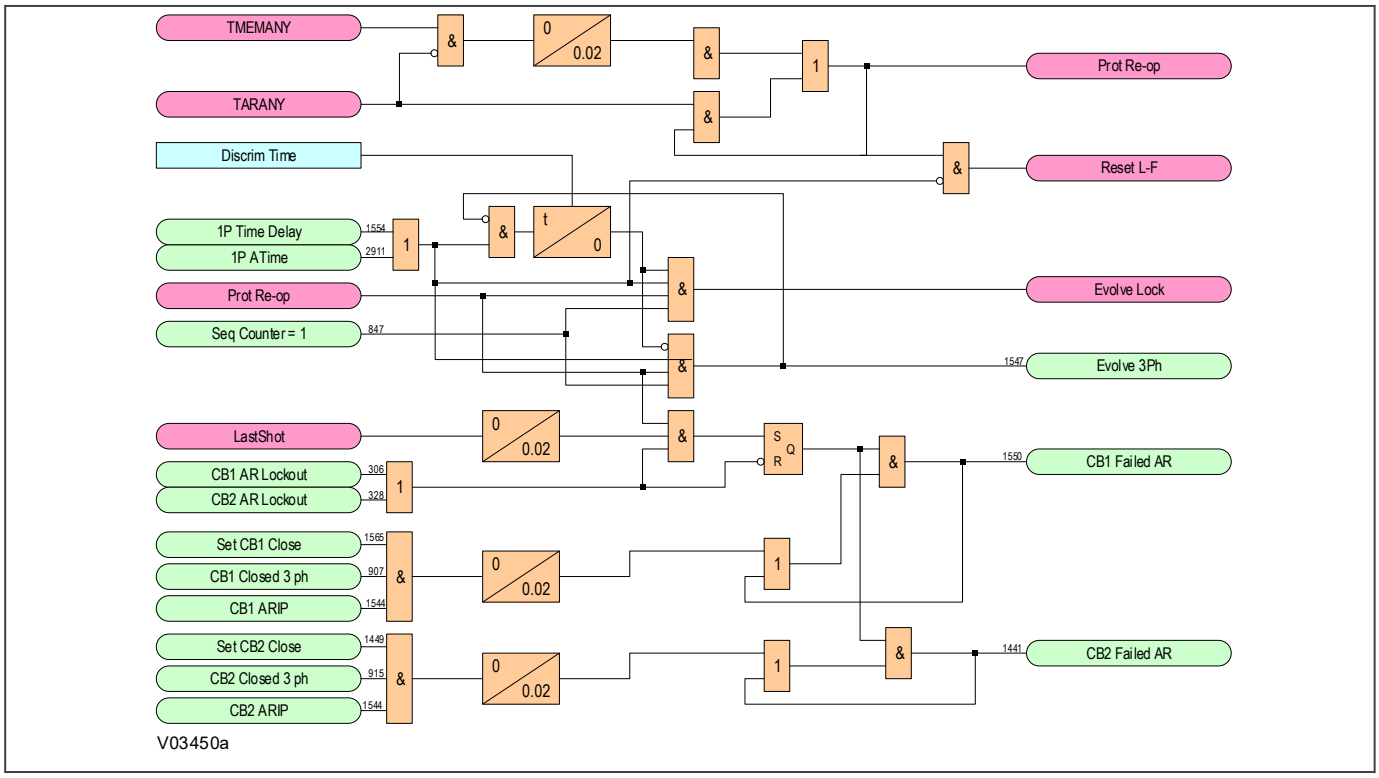


Figure 93: Protection Reoperation and Evolving Fault logic diagram (Module 20)

6.5.8.6 FAULT MEMORY LOGIC DIAGRAM

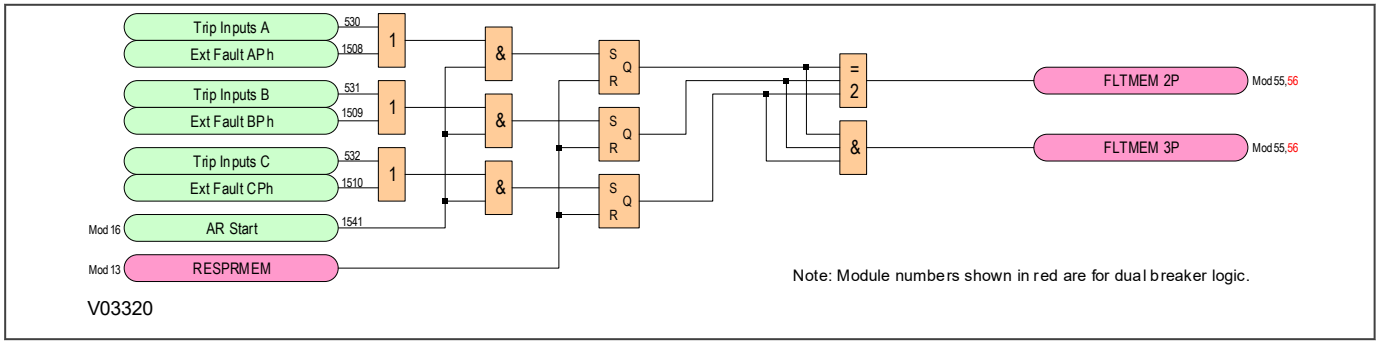


Figure 94: Fault Memory logic diagram (Module 15)

6.5.9 AUTORECLOSE IN PROGRESS

The AR In Progress module produces various signals to indicate to other modules and functions that an Autoreclose operation is currently in progress.

6.5.9.1 AUTORECLOSE IN PROGRESS LOGIC DIAGRAM FOR CB1

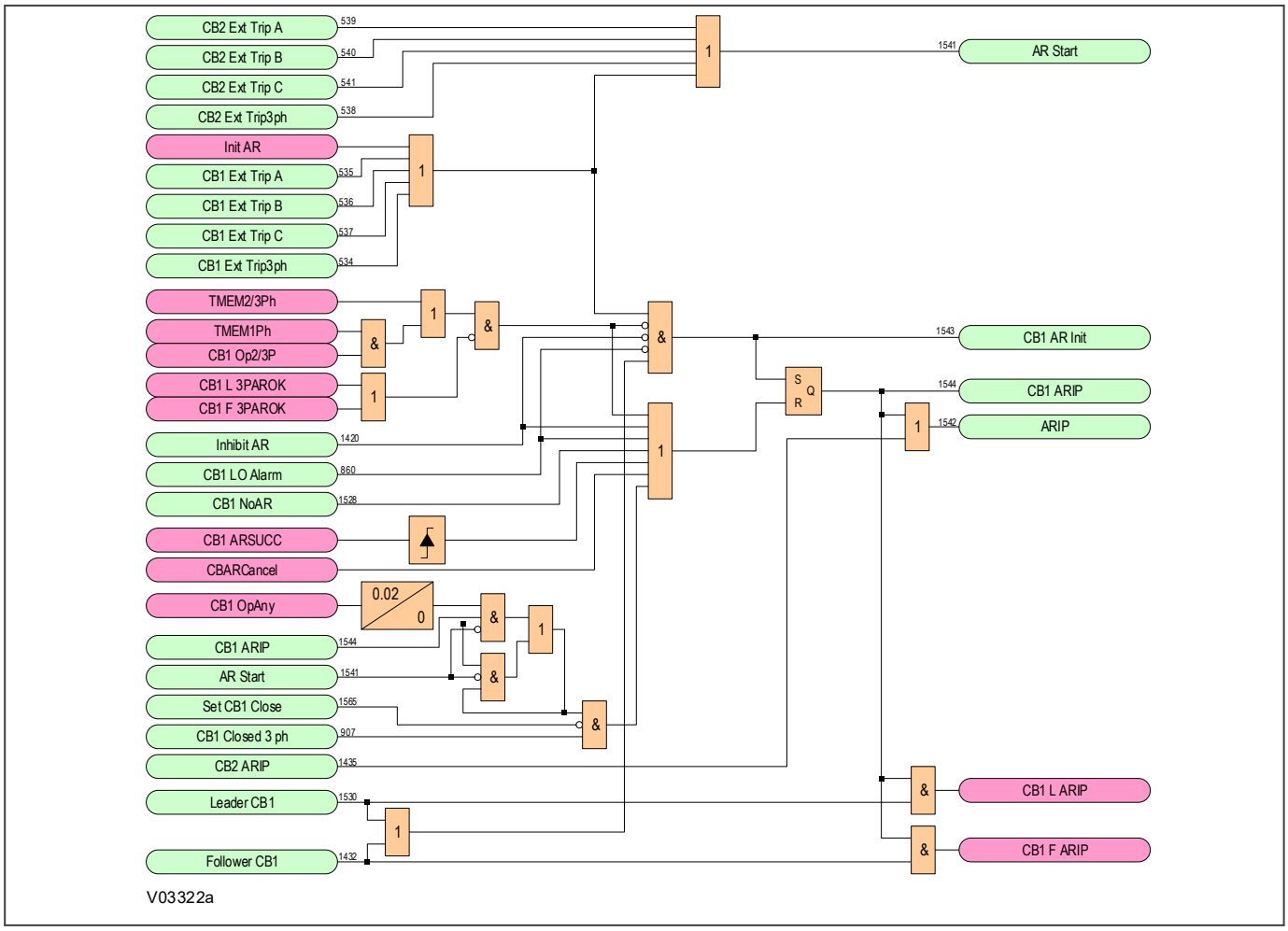


Figure 95: Autoreclose In Progress logic diagram for CB1 (Module 16)

6.5.9.2 AUTORECLOSE IN PROGRESS LOGIC DIAGRAM FOR CB2

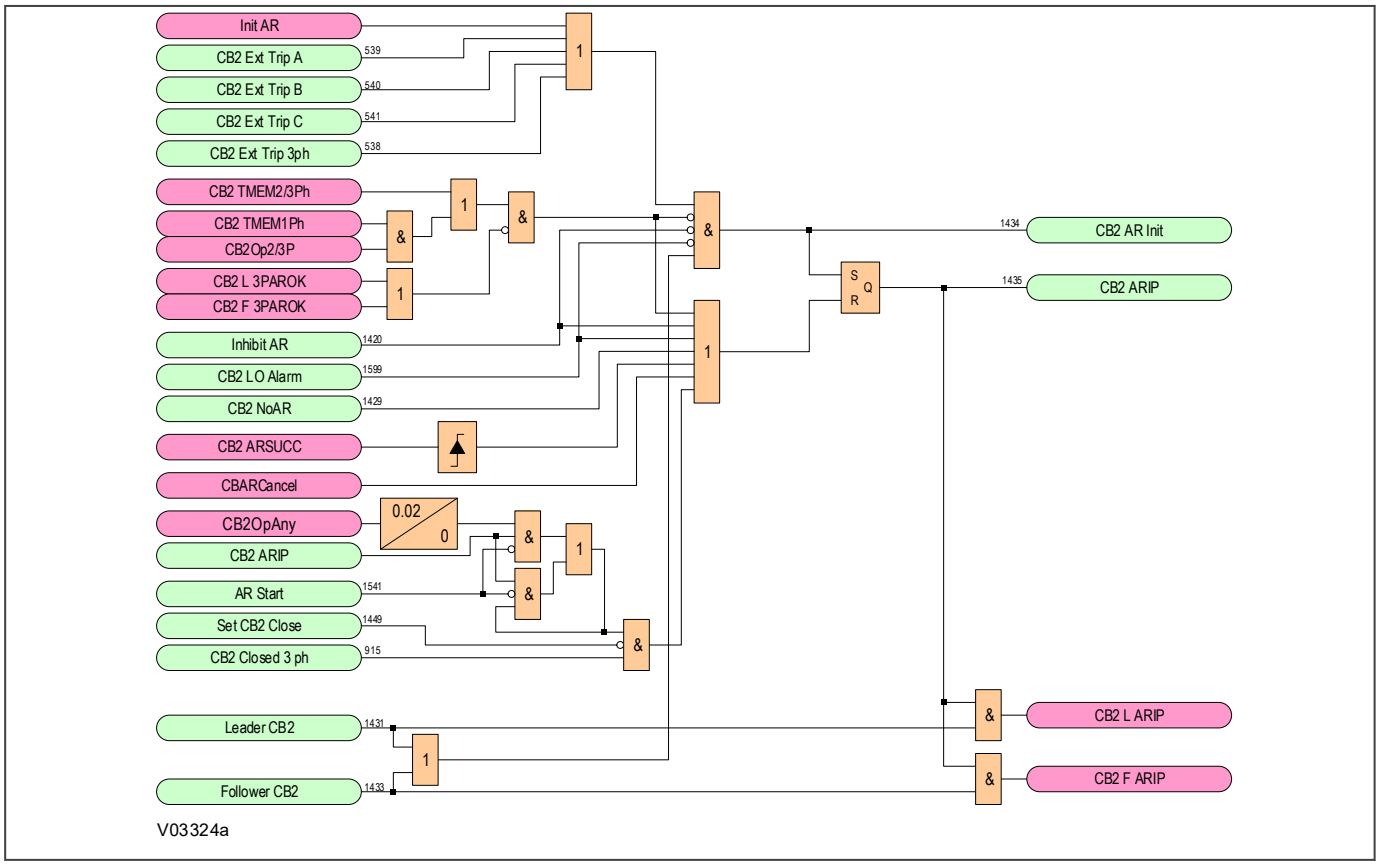


Figure 96: Autoreclose In Progress logic diagram for CB2 (Module 17)

6.5.10 SEQUENCE COUNTER

The Autoreclose logic includes a counter for counting the number of Autoreclose shots. This is referred to as the sequence counter. The sequence counter has a value of zero if Autoreclose is not in progress. Following a trip, and subsequent Autoreclose initiation, the sequence counter is incremented. The counter provides output signals indicating how many initiation events have occurred in any Autoreclose cycle. These signals are available as user indications and are used in the logic to select the appropriate dead times or, for a persistent fault, force a lockout.

It is possible to skip the first Autoreclose attempt by enabling the ***AR Skip Shot 1*** setting. If this is set, the sequence counter will skip the first Autoreclose attempt (Shot 1) and move to the second (Shot 2) immediately upon Autoreclose initiation. Each time the protection trips the sequence counter is incremented by 1. The Autoreclose logic compares the sequence counter value to the number of Autoreclose shots setting ***AR Shots***. If the counter value exceeds this setting then the Autoreclose is locked out. If Autoreclose is successful, the sequence counter resets to zero.

6.5.10.1 AUTORECLOSE SEQUENCE COUNTER LOGIC DIAGRAM

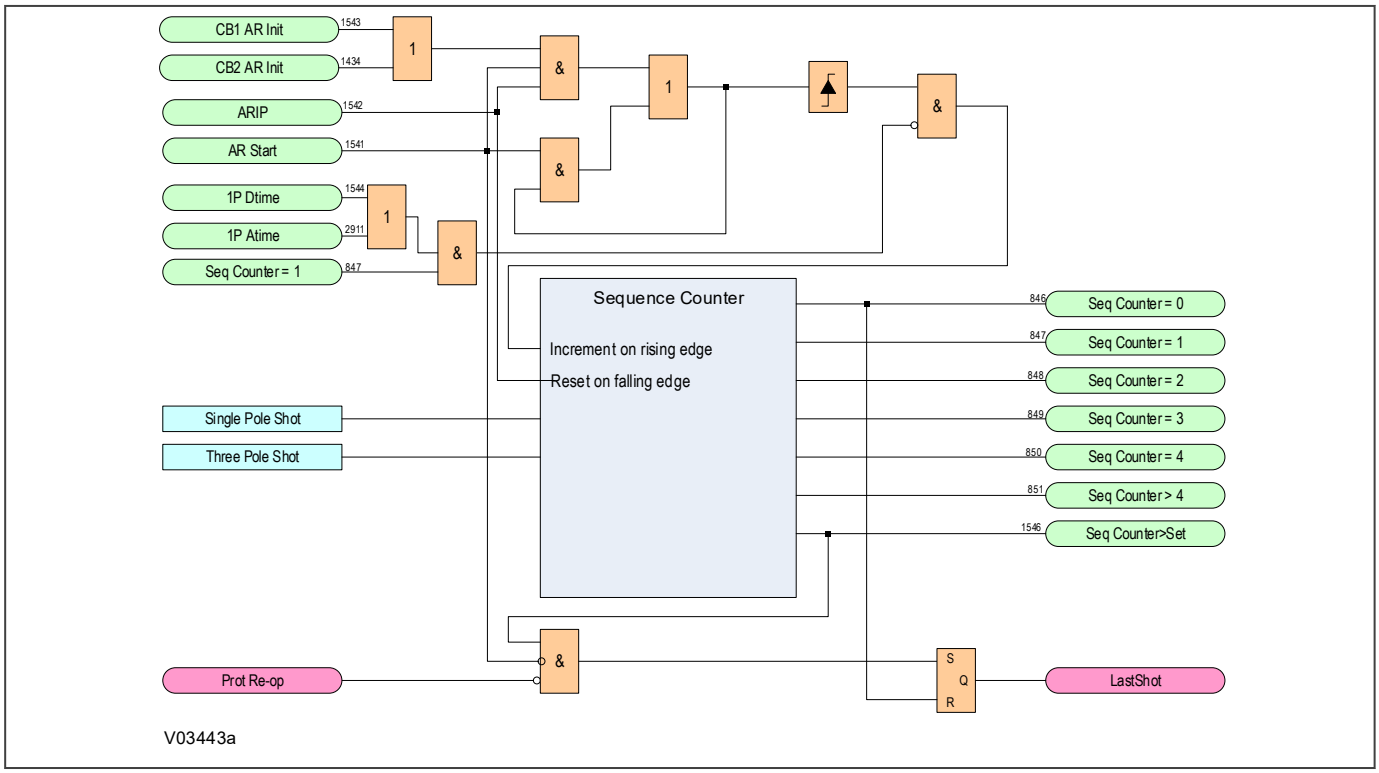


Figure 97: Autoreclose Sequence Counter logic diagram (Module 18)

6.5.11 AUTORECLOSE CYCLE SELECTION

The Autoreclose cycle selection logic is responsible for determining whether the Autoreclose will start as single-phase or three-phase.

6.5.11.1 SINGLE PHASE AUTORECLOSE CYCLE SELECTION LOGIC DIAGRAM

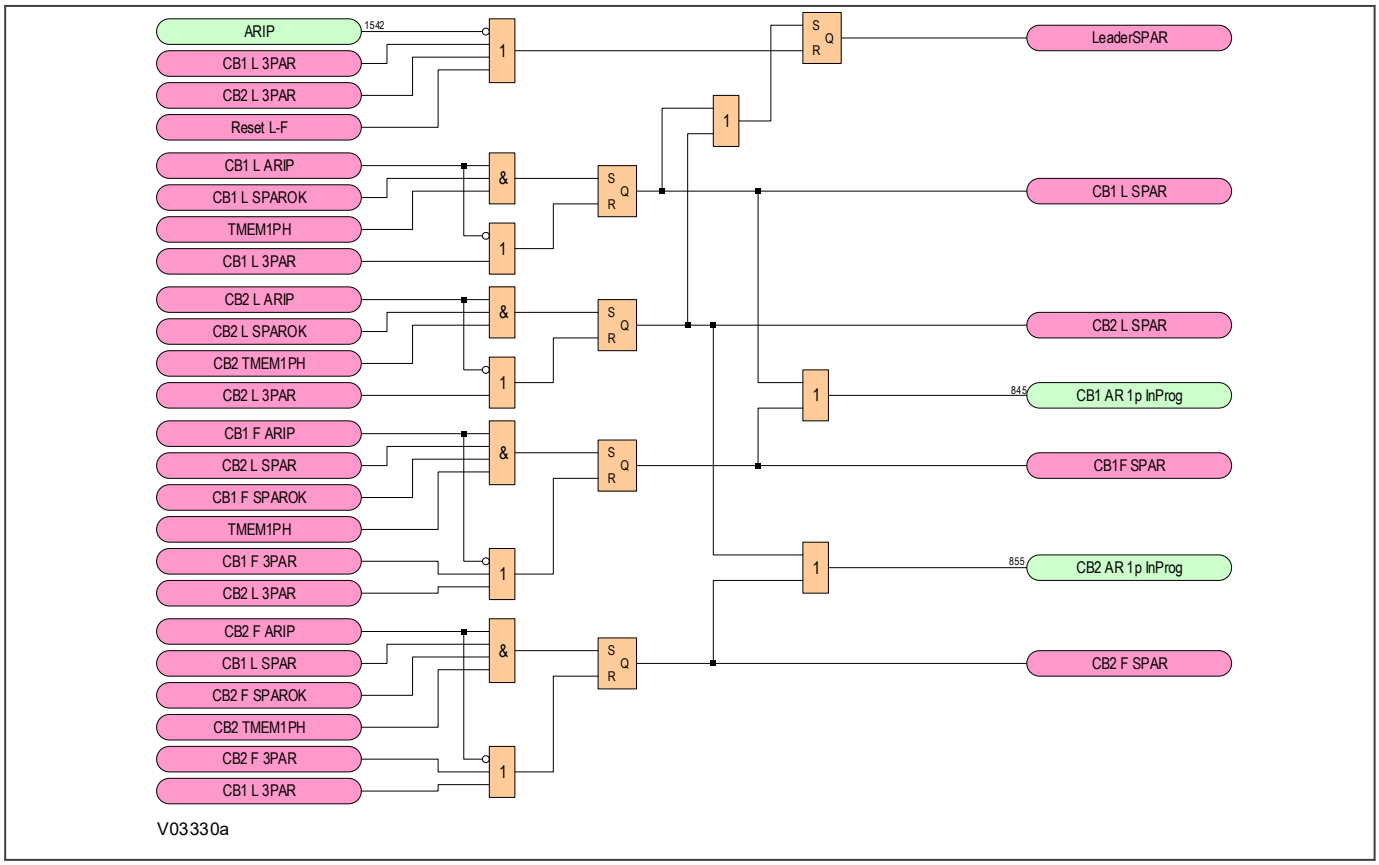


Figure 98: Single-phase Autoreclose Cycle Selection logic diagram (Module 19)

6.5.11.2 3-PHASE AUTORECLOSE CYCLE SELECTION

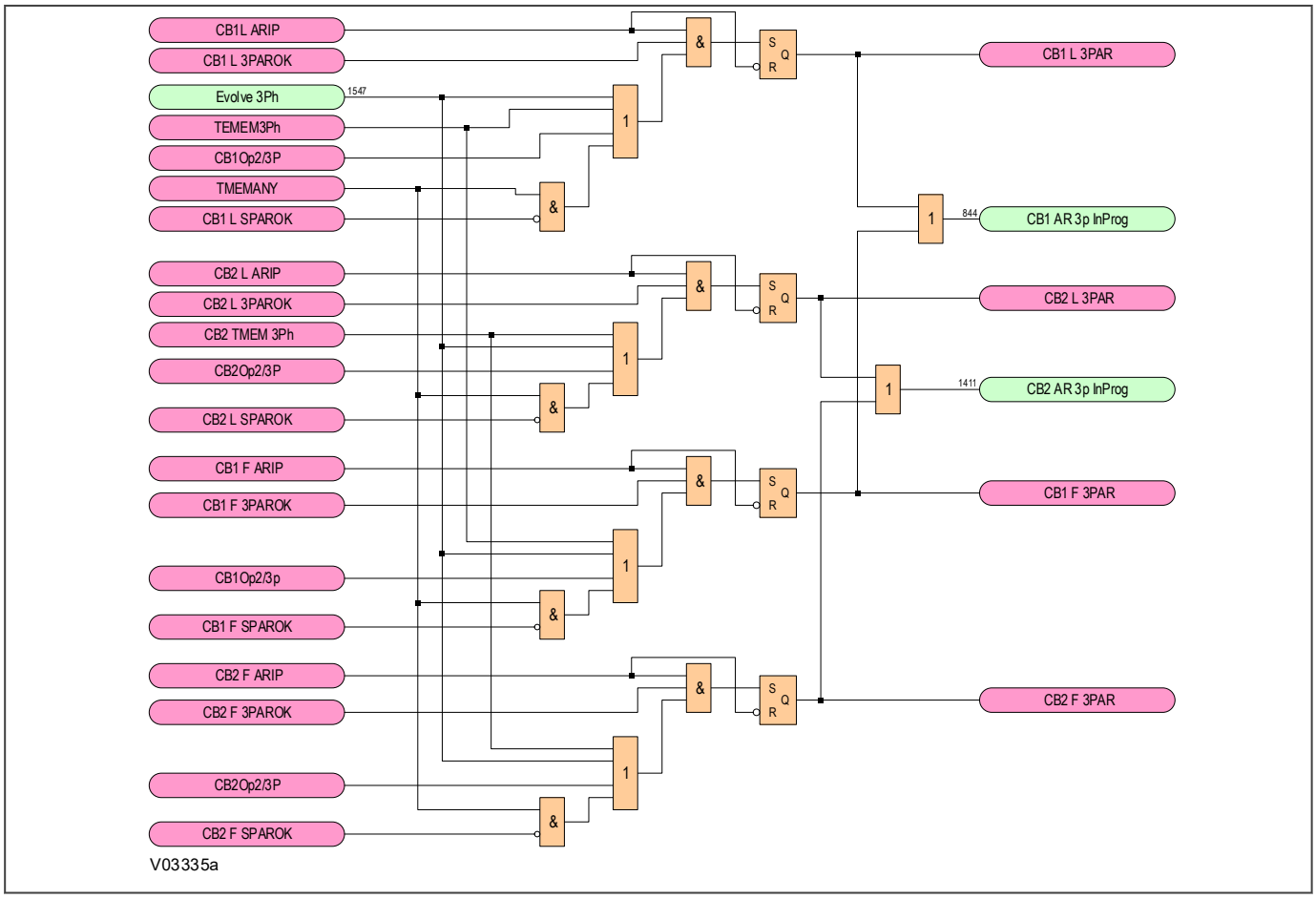


Figure 99: Three-phase Autoreclose Cycle Selection logic diagram (Module 21)

6.5.12 DEAD TIME CONTROL

Once an Autoreclose cycle has started, the conditions to enable the dead time to run are determined by the menu settings, the circuit breaker status, the protection status, the nature of the AR cycle (single-phase or three-phase), and the opto-isolated inputs from external sources.

Three settings are involved in controlling the dead time start:

- ***DT Start by Prot***
- ***3PDTStart WhenLD***
- ***DTStart by CB Op***

The ***DT Start by Prot*** determines how the protection action will initiate a dead time. The setting is always visible and has three options `Protection Reset`, `Protection Op` (protection operation), and `Disable` which should be selected if you don't want protection action to start the dead time. These options set the basic conditions for starting the dead time.

Selecting protection operation to start the dead time can, optionally, be qualified by a check that the line is dead.

Selecting protection reset to start the dead time can, optionally, be qualified by a check, that the circuit breaker is open (***DTStart by CB Op***) before starting the dead time. For three-phase tripping applications, there is a further option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time.

If ***DT Start by Prot*** is disabled, the circuit breaker must be open for the dead time to start. For three-phase tripping applications, there is an option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time. To

check that the line is dead, set ***3PDTStart WhenLD*** to `enabled`. To check that the circuit breaker is open, set ***DTStart by CB Op*** to `Enabled`.

6.5.12.1 DEAD TIME START ENABLE LOGIC DIAGRAM

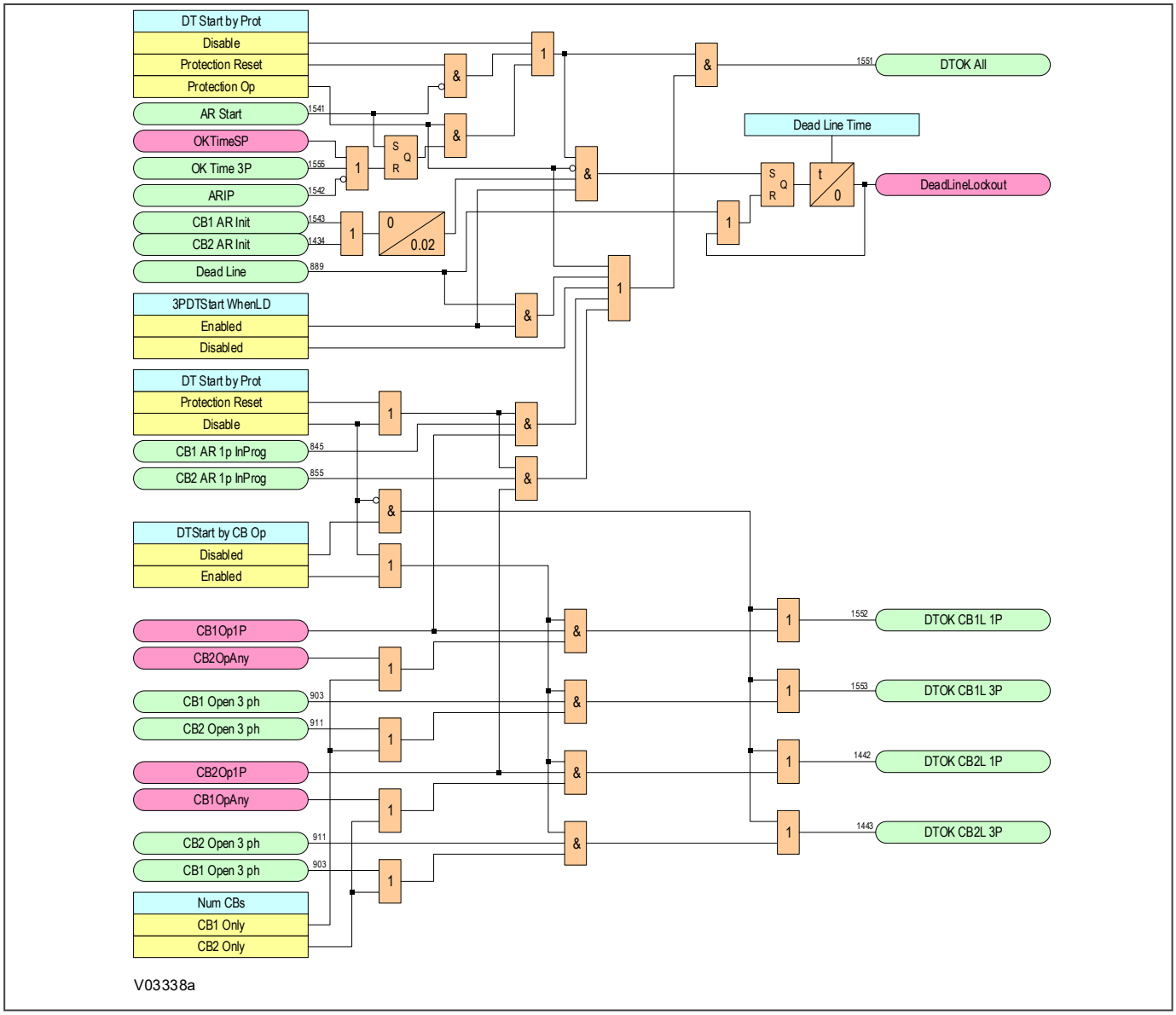


Figure 100: Dead time Start Enable logic diagram (Module 22)

6.5.12.2 SINGLE-PHASE DEAD TIME AND ADAPTIVE AUTORECLOSE (AAR) LOGIC

The autoreclose scheme is adaptive when the ***Adaptive SP AR*** setting is `Enabled`. The adaptive autoreclose is only available for single pole autoreclose applications. When adaptive autoreclose is enable, ***SP AR Dead Time*** is hidden, and two new timer settings are visible: ***SP Min Dead Time*** and ***SP Max Dead Time***. Those two timers are the limits of the single pole dead time.

The Fault Type and Arc Extinction (FTAE) detection algorithm is initiated when the ***Adaptive SP AR*** setting is `Enabled` and the ***OkTimeSP*** signal of the dead time is high, as shown in Module 24.

The breaker open status (***CB Open A PH***/***CB Open B PH*** /***CB Open C PH***) signals are used to identify the single phase to ground fault isolation. The phase voltage information is provided to a six cycle buffer and the δ and |Vs| and derivatives are fed to the ***FTAED*** Module.

The output signals from the ***FTAED*** Module are the ***P_Fault***, ***T_Fault*** and the ***Arc complete*** signals which indicate a permanent fault detection, transient fault detection and arc extinction.

The ***T_Fault*** signal is high during a transient fault condition and the Arc complete signal is high only after complete de-ionization of the faulted arc during transient fault conditions. During a permanent fault condition, the ***P_Fault*** output signal of the AAR module is high, and it is routed to the AR lockout logic diagram (Module 55) to stop further autoreclose actions if required.

The ***CB1SPDTCOMP*** and ***CB1SPATCOMP*** signals in Module 24 are inputs to the Circuit Breaker Auto Close Logic Diagram (Module 32). The ***CB1SPDTCOMP*** signal is high in cases where the ***Adaptive SP AR*** is setting is `0` and ***CB1SPATCOMP*** is high in cases where the ***Adaptive SP AR*** setting is `1`.

6.5.12.3 SINGLE-PHASE LEADER DEAD TIME LOGIC DIAGRAM

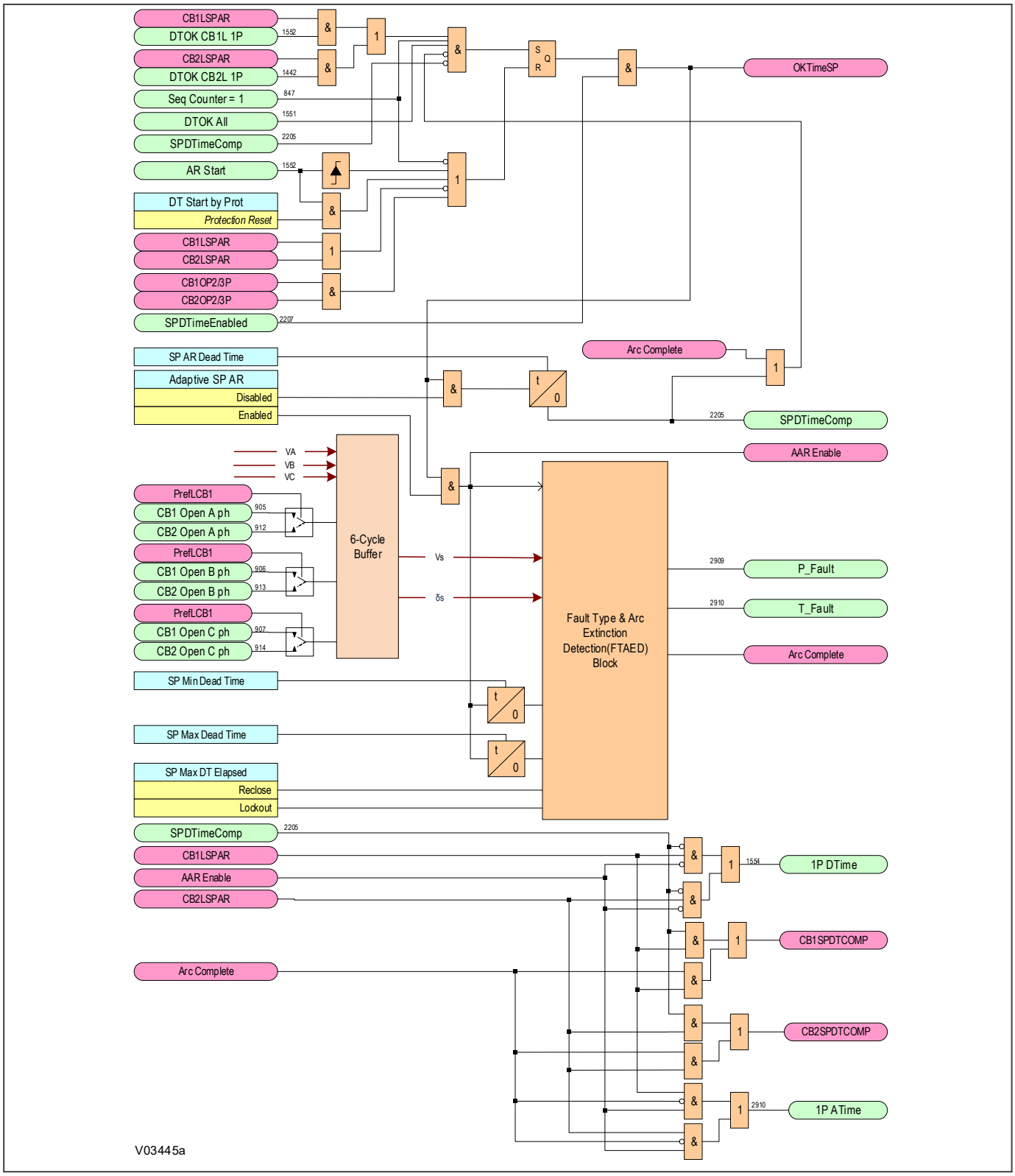


Figure 101: Single-phase Leader Dead Time logic diagram (Module 24)

6.5.12.4 3-PHASE LEADER DEAD TIME LOGIC DIAGRAM

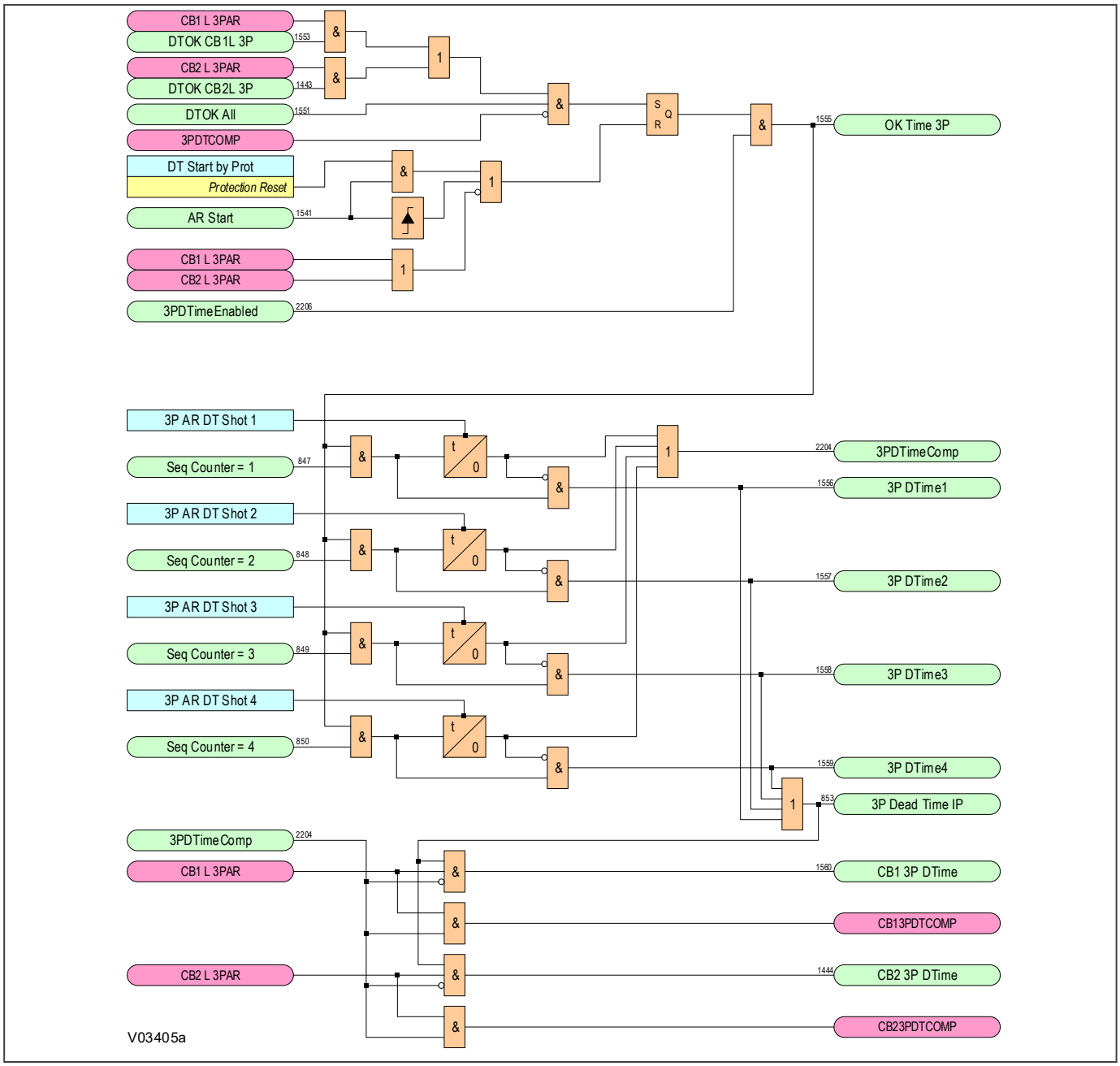


Figure 102: Three-phase Leader CB Dead Time logic diagram (Module 25 and Module 26)

6.5.12.5 FOLLOWER ENABLE LOGIC DIAGRAM

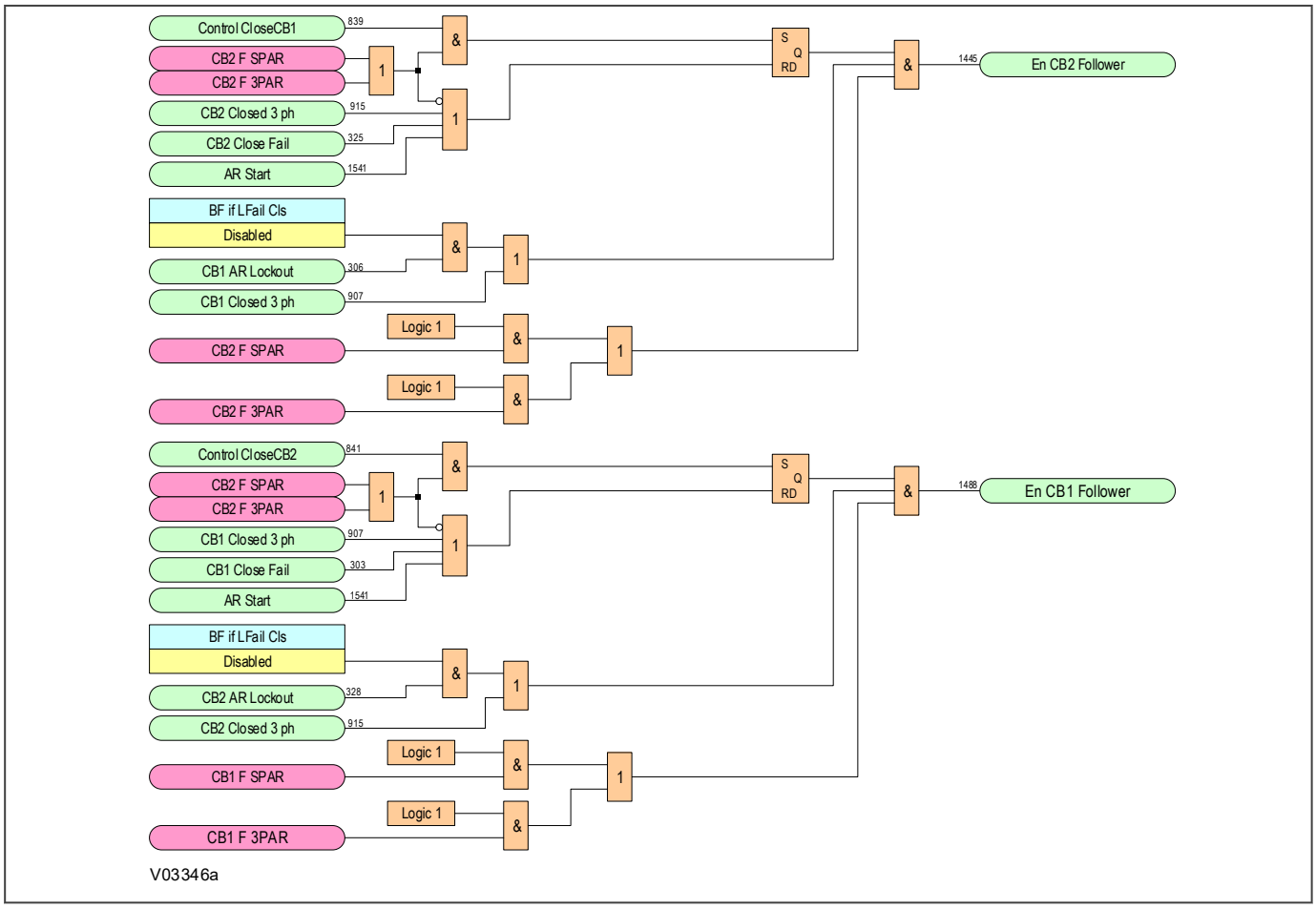


Figure 103: Follower Enable logic diagram (Module 27)

6.5.12.6 SINGLE-PHASE FOLLOWER TIMING LOGIC DIAGRAM

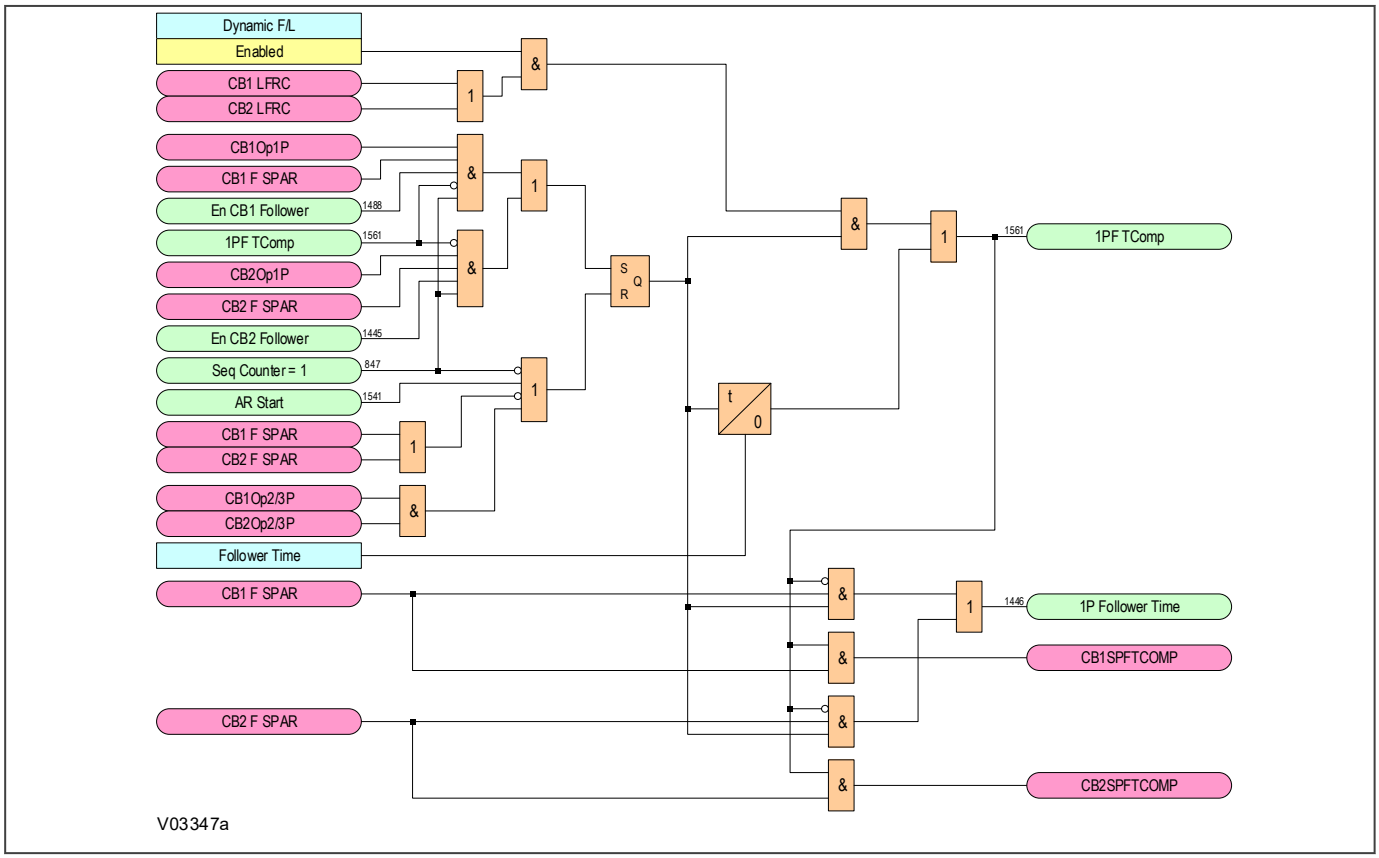


Figure 104: Single-phase Follower CB timing logic diagram (Module 28)

6.5.12.7 THREE-PHASE FOLLOWER TIMING LOGIC DIAGRAM

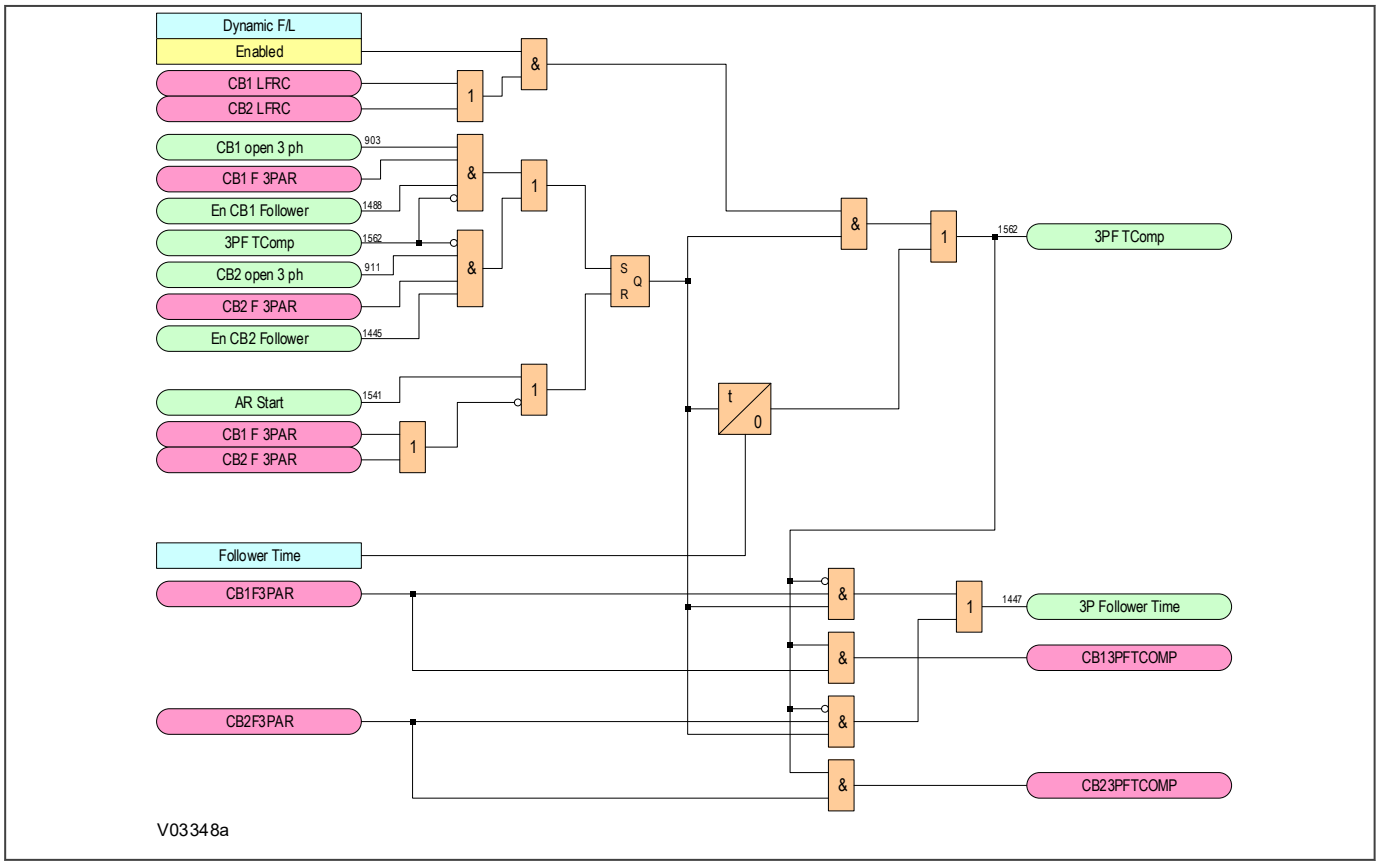


Figure 105: Three-phase Follower CB timing logic diagram (Module 29)

6.5.13 CIRCUIT BREAKER AUTOCLOSE

Autoclose logic takes effect when dead times have expired.

The Autoclose logic checks that all necessary conditions are satisfied before issuing an Autoclose command to the circuit breaker control scheme.

Before a circuit breaker can be closed, it must be healthy (sufficient energy to close, and if necessary re-trip) and it must not be in a lockout condition.

For three-phase Autoreclose, the circuit breaker must be open on all three phases and the appropriate system check conditions must be met. For single-phase Autoreclose, the circuit breaker must be open on that phase.

The Autoclose command is a pulse lasting 100 milliseconds. Another command (***Set CB Close***) to set the circuit breaker to close is asserted as well as the Autoclose command. This signal will remain set either until the end of the Autoreclose cycle, or until the next protection operation. These commands are used to initiate the Reclaim Time logic and the Autoreclose Shot Counter logic.

6.5.13.1 CIRCUIT BREAKER AUTOCLOSE LOGIC DIAGRAM

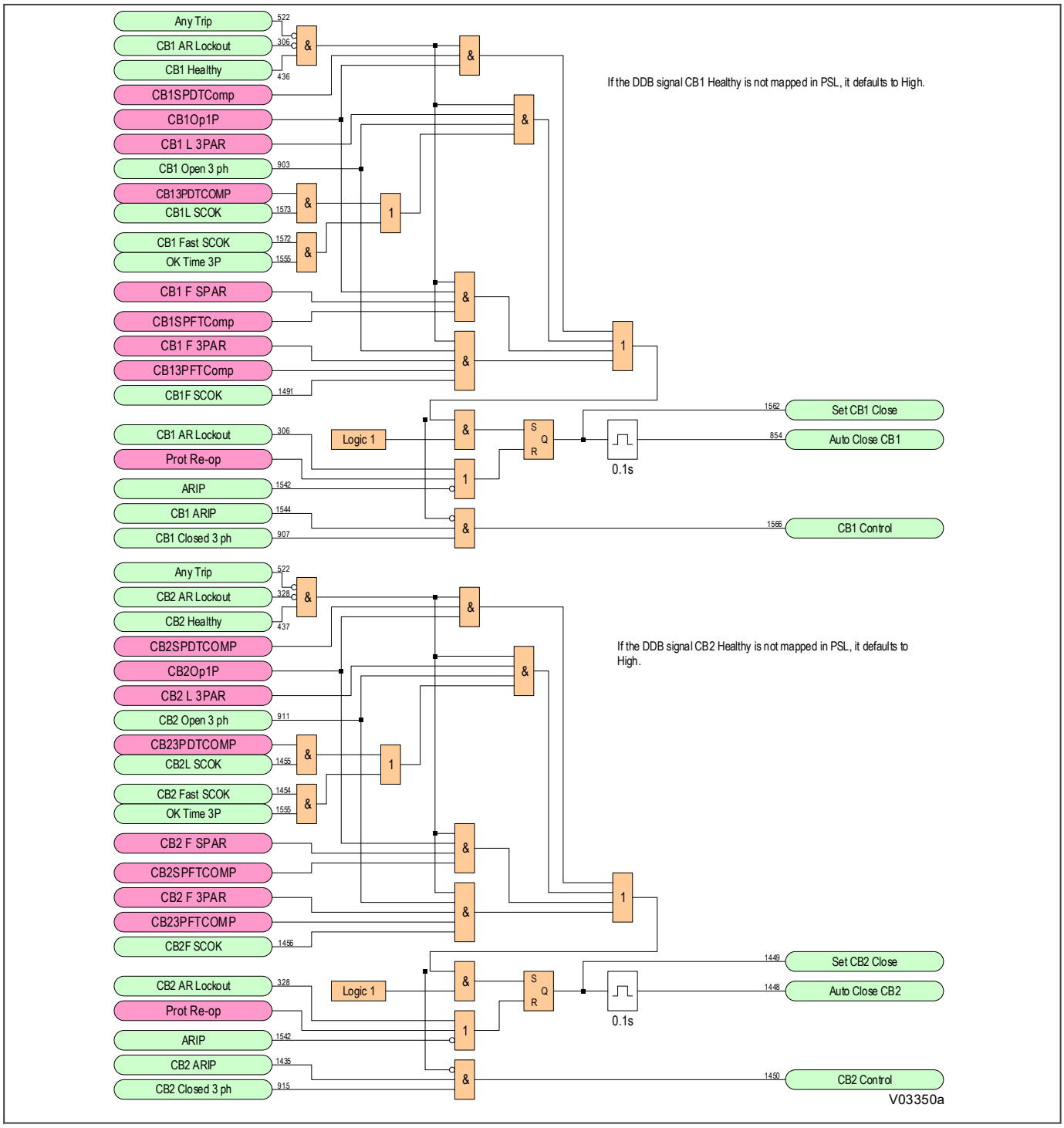


Figure 106: Circuit Breaker Autoclose Logic Diagram (Modules 32 & 33)

6.5.14 RECLAIM TIME

If the protection operates again before the reclaim time has expired, the corresponding sequence counter is incremented. At the same time, any “dead time complete” (….DTCOMP) signals are reset and the logic is prepared for the next dead time to start when conditions are suitable. The operation also resets the signal that would set the circuit breaker to close, and stops and resets the reclaim timer. The reclaim time starts again if the signal to set a

circuit breaker to close goes high following completion of a dead time in a subsequent Autoreclose cycle. Where the reclaim extend time signal is set, the reclaim time cannot time out and reset the Autoreclose cycle before the time delayed protection has fully operated

If the circuit breaker is closed and has not tripped again when the reclaim time expires, signals are generated to indicate successful Autoreclose. These signals increment the relevant circuit breaker successful Autoreclose shot counters and reset the relevant Autoreclose in progress signal.

The “successful Autoreclose” signals generated from the logic can be reset by various commands and settings options available under *CB CONTROL* menu settings as follows:

If ***Res AROK by UI*** is set to `Enabled`, all the signals can be reset by user interface command ***Reset AROK Ind*** from the *CB CONTROL* menu.

If ***Res AROK by NoAR*** is set to `Enabled`, the signals for each circuit breaker can be reset by temporarily generating an Autoreclose disabled signal according to the logic shown.

If ***Res AROK by Ext*** is set to `Enabled`, the signals can be reset by activation of an external input signal appropriately mapped in the PSL.

If ***Res AROK by TDly*** is set to `Enabled`, the signals are automatically reset after a time delay set in ***AROK Reset Time***.

6.5.14.1 PREPARE RECLAIM INITIATION LOGIC DIAGRAM

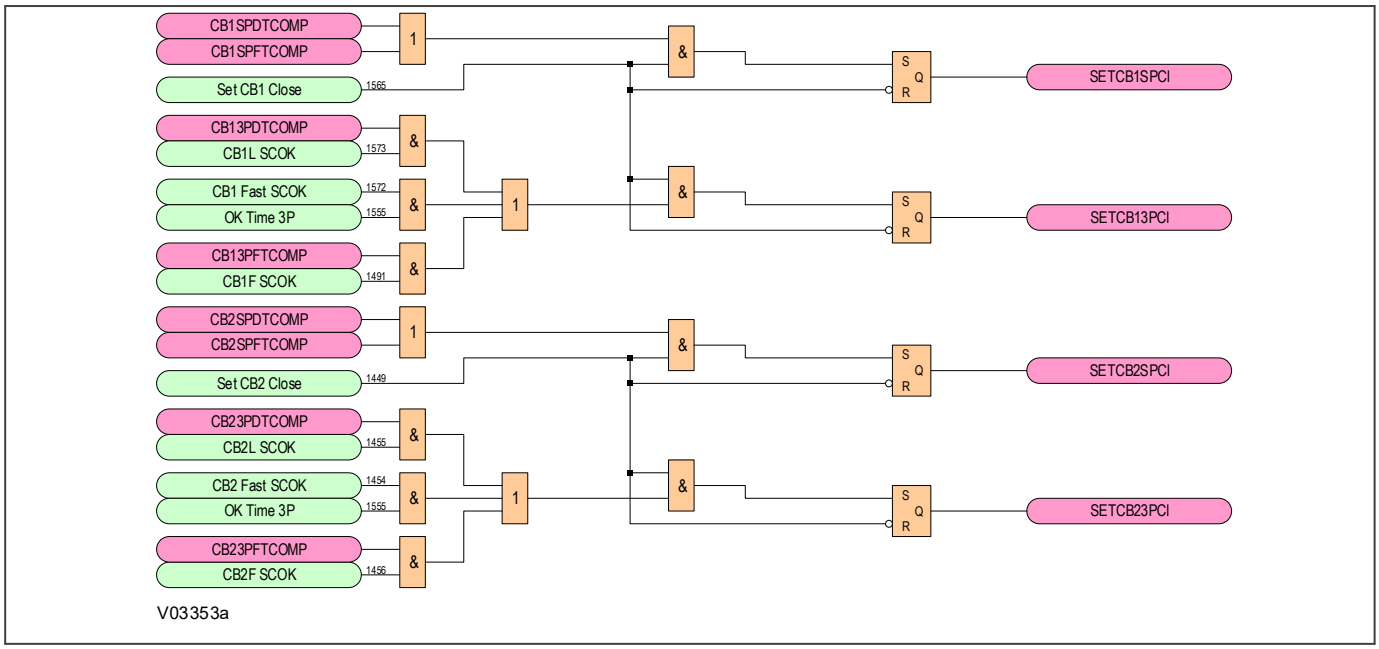


Figure 107: Prepare Reclaim Initiation logic diagram (Module 34)

6.5.14.2 RECLAIM TIME LOGIC DIAGRAM

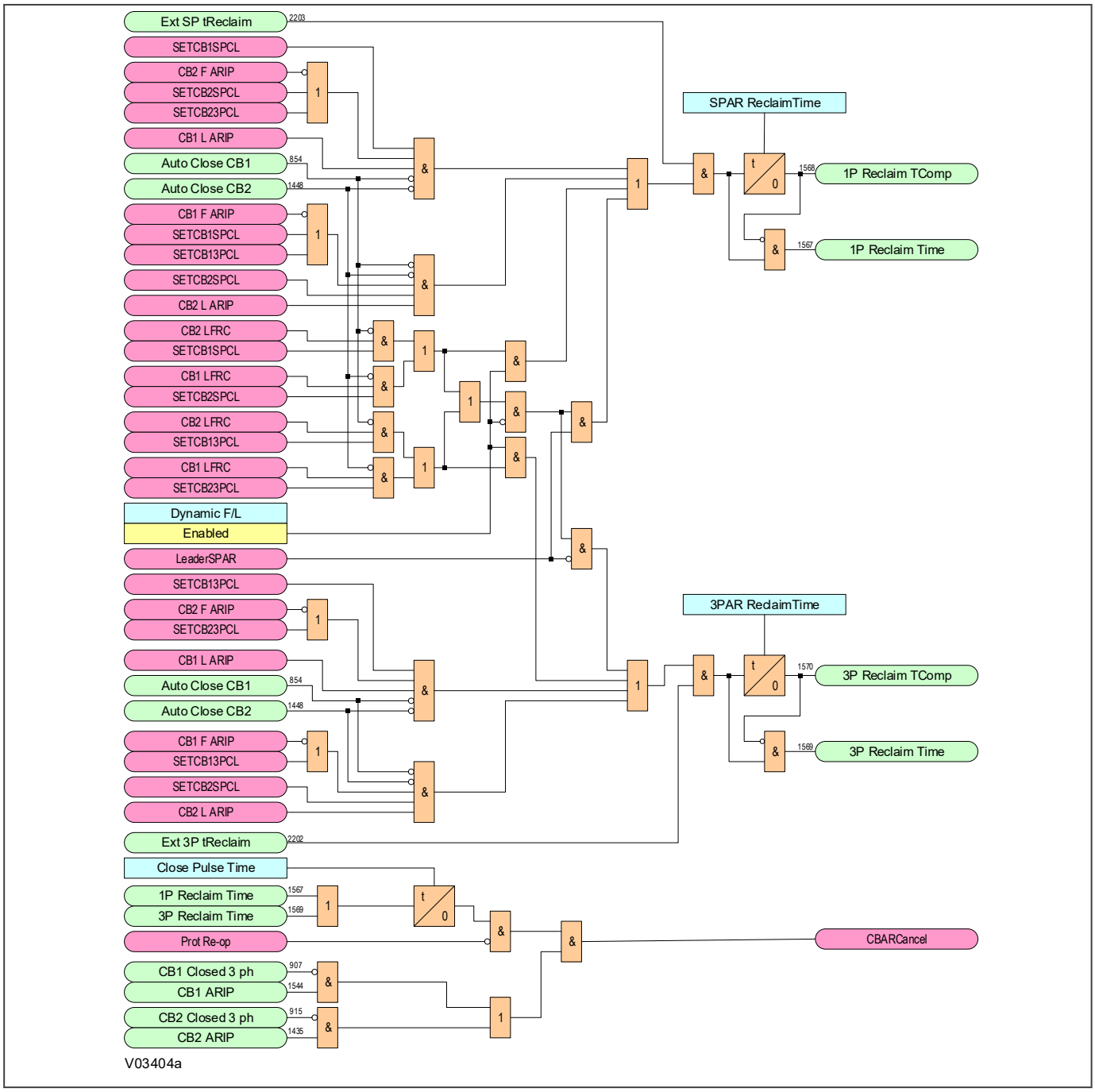


Figure 108: Reclaim Time logic diagram (Module 35)

6.5.14.3 SUCCESSFUL AUTORECLOSE SIGNALS LOGIC DIAGRAM

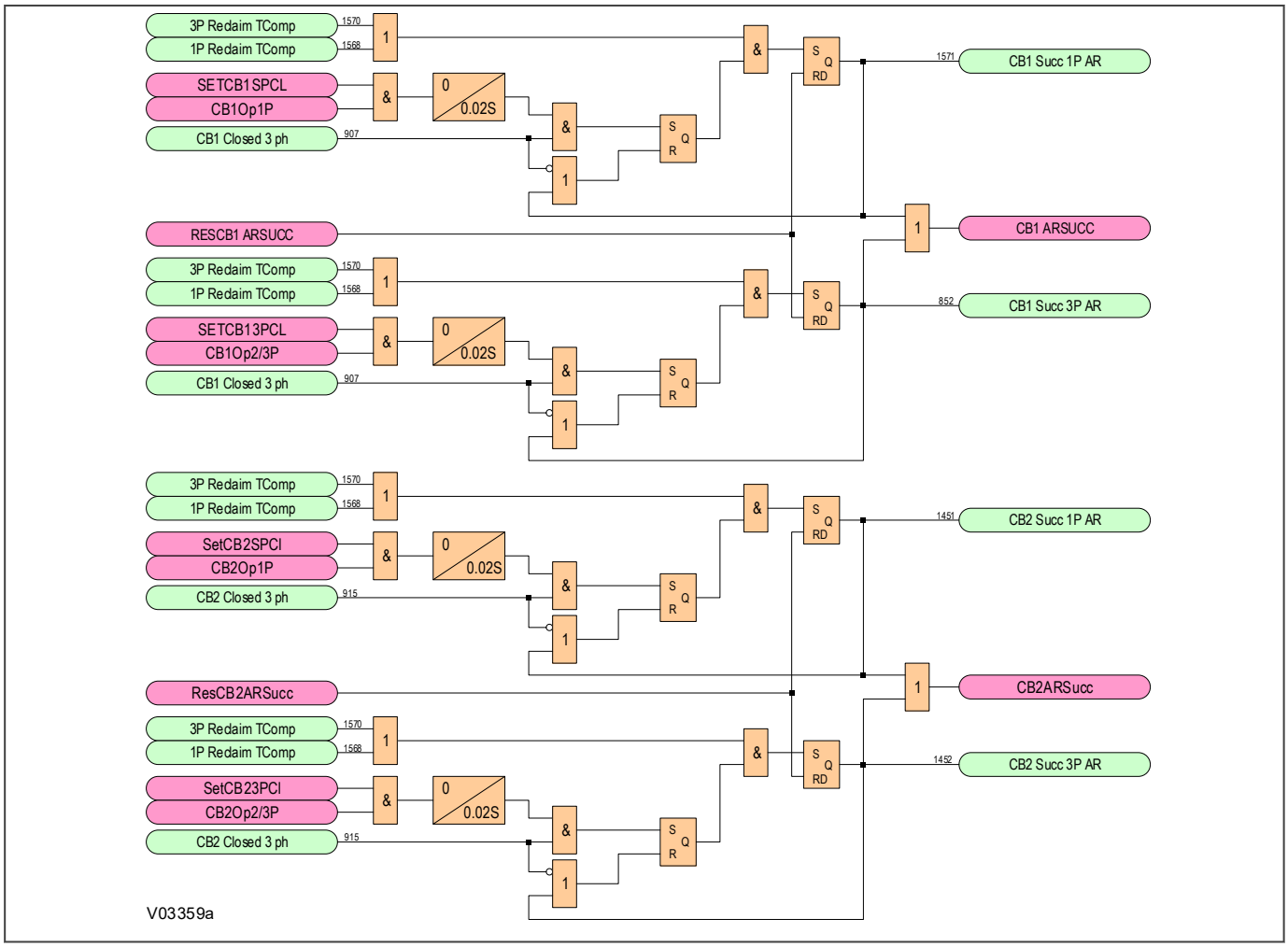


Figure 109: Successful Autoreclose Signals logic diagram (Module 36)

6.5.14.4 AUTORECLOSE RESET SUCCESSFUL INDICATION LOGIC DIAGRAM

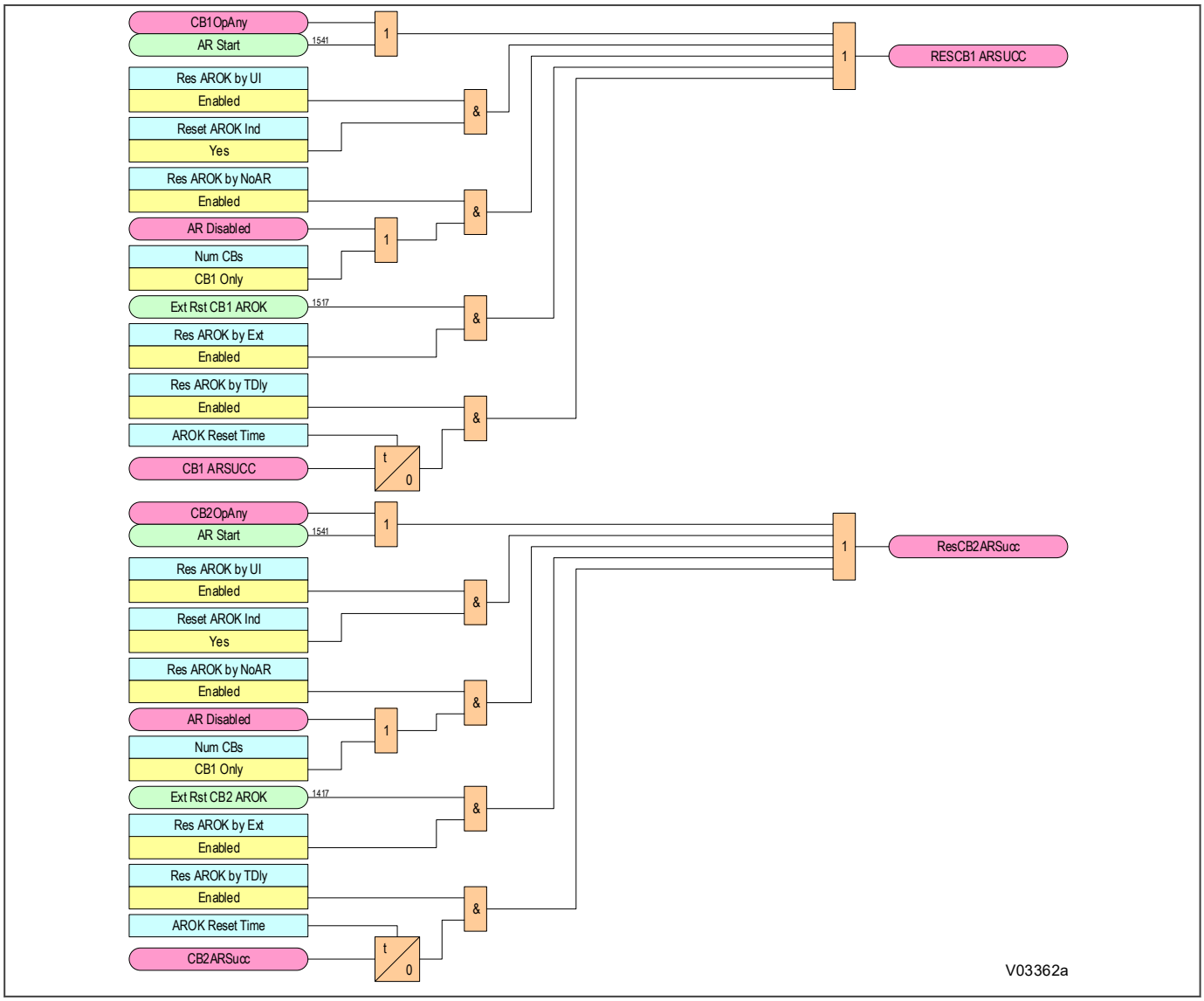


Figure 110: Autoreclose Reset Successful Indication logic diagram (Modules 37 & 38)

6.5.15 CB HEALTHY AND SYSTEM CHECK TIMERS

This logic provides signals to cancel Autoreclose if the circuit breaker is not healthy (for example low gas pressure) or system check conditions are not satisfied (for example required line & bus voltage conditions) when the scheme is ready to close the circuit breaker.

At the completion of a dead time, the logic starts an Autoreclose healthy timer. If a circuit breaker healthy signal becomes high before the Autoreclose healthy time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker healthy signal stays low, then, at the end of the Autoreclose healthy time, a circuit breaker unhealthy alarm is raised. This forces the Autoreclose sequence to be cancelled.

Additionally, at the completion of any three-phase dead time, the logic starts an Autoreclose check synchronism timer. If the circuit breaker synchronism-check OK signal goes high before the time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker synchronism-check OK signal stays low, then when the Autoreclose check synchronism

timer expires, an alarm is set to inform that the check synchronism is not satisfied and cancels the Autoreclose cycle.

6.5.15.1 CB HEALTHY AND SYSTEM CHECK TIMERS LOGIC DIAGRAM

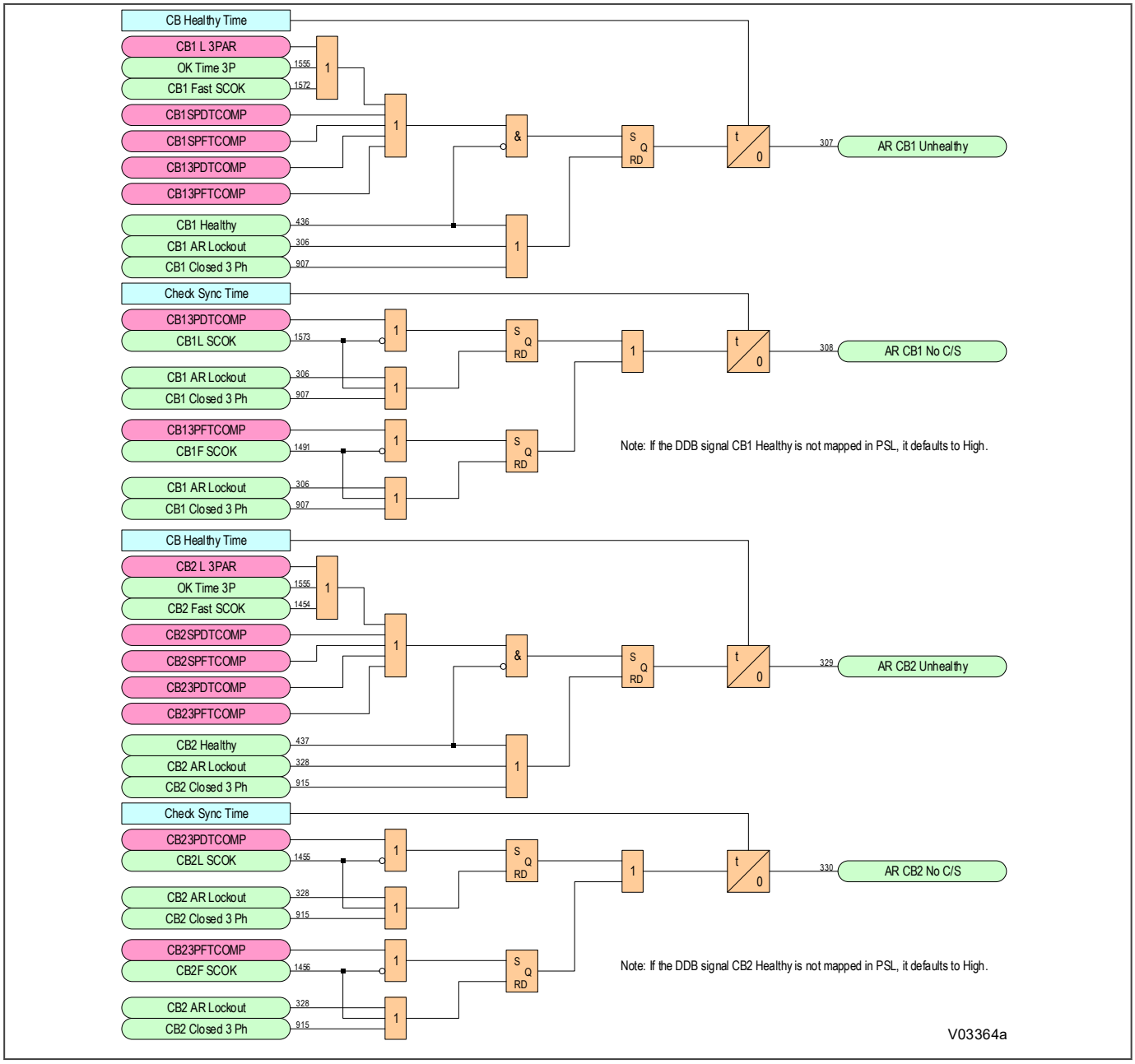


Figure 111: Circuit Breaker Healthy and System Check Timers Healthy logic diagram (Module 38 & 40)

6.5.16 AUTORECLOSE SHOT COUNTERS

A number of counters are provided to enable analysis of circuit breaker Autoreclose history. The counters are stored in non-volatile memory, so that the data is maintained even in the event of a failure of the auxiliary supply. The counter values are accessible through the *CB CONTROL* column. The counters can be reset manually, or by activation of an input appropriately mapped in the PSL.

The logic provides the following summary information for each circuit breaker

- Overall total number of shots (Number of Autoreclose attempts)
- Number of successful 1st shot single-phase Autoreclose sequences
- Number of successful 1st shot three-phase Autoreclose sequences
- Number of successful 2nd shot three-phase Autoreclose sequences
- Number of successful 3rd shot three-phase Autoreclose sequences
- Number of successful 4th shot three-phase Autoreclose sequences
- Number of failed Autoreclose cycles which forced a circuit breaker to lockout

6.5.16.1 AUTORECLOSE SHOT COUNTERS LOGIC DIAGRAM

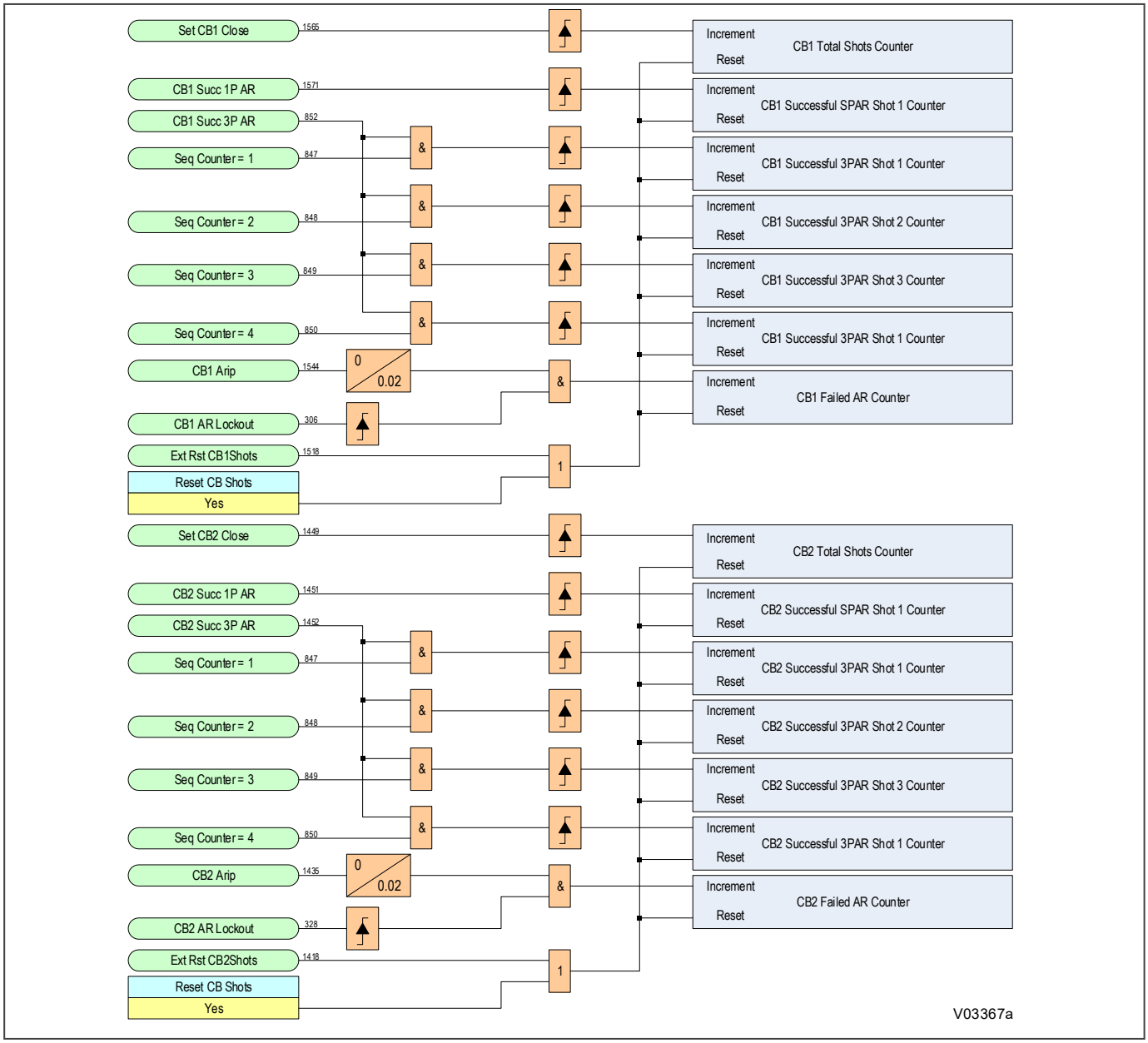


Figure 112: Autoreclose Shot Counters logic diagram (Modules 41 & 42)

6.5.17 CIRCUIT BREAKER CONTROL

6.5.17.1 CB CONTROL LOGIC DIAGRAM

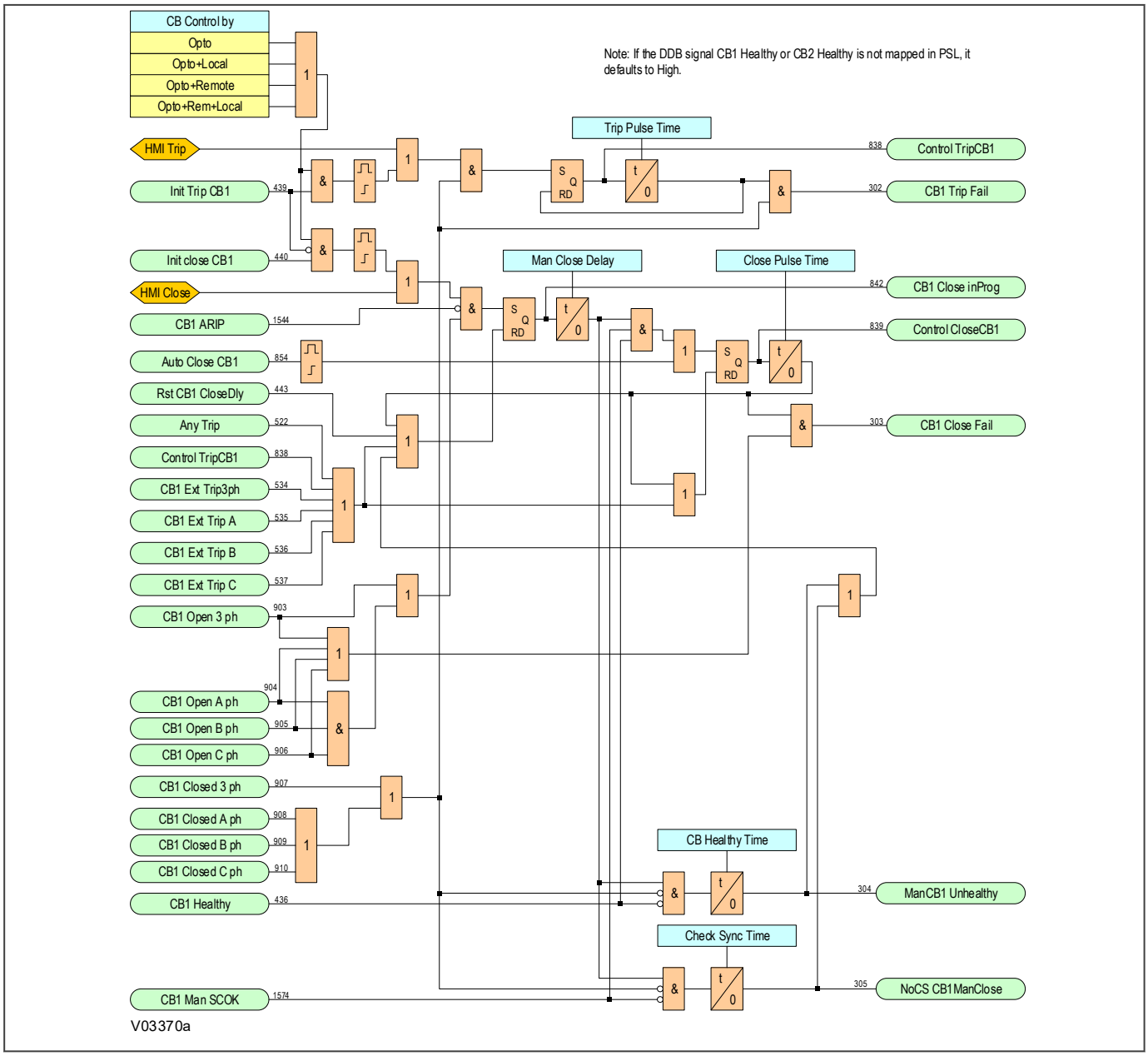


Figure 113: CB1 Control Logic (Module 43)

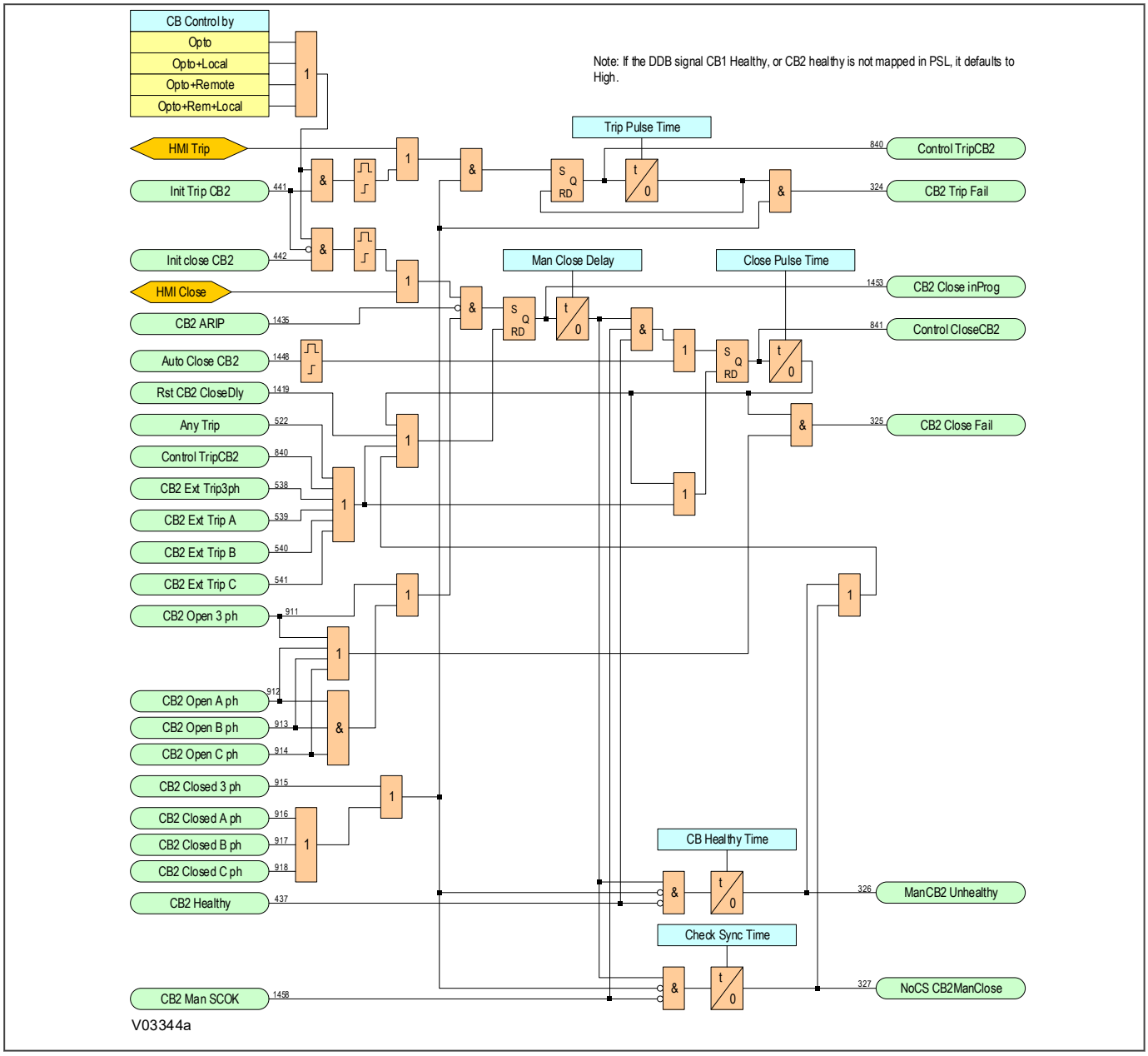


Figure 114: CB2 Control Logic (Module 44)

6.5.18 CIRCUIT BREAKER TRIP TIME MONITORING

The circuit breaker trip time monitoring logic checks for correct circuit breaker tripping following the issue of a protection trip signal. When the protection trip signal is issued, a timer controlled by the ***Trip Pulse Time*** setting in the *CB CONTROL* column is started.

If the circuit breaker trips correctly the timer resets. If Autoreclose is enabled and the timer resets, the cycle continues. If the circuit breaker fails to trip correctly within the set time, the Autoreclose cycle is forced to lock out and a signal is issued indicating that the circuit breaker failed to trip in response to the protection operation.

6.5.18.1 CB TRIP TIME MONITORING LOGIC DIAGRAM

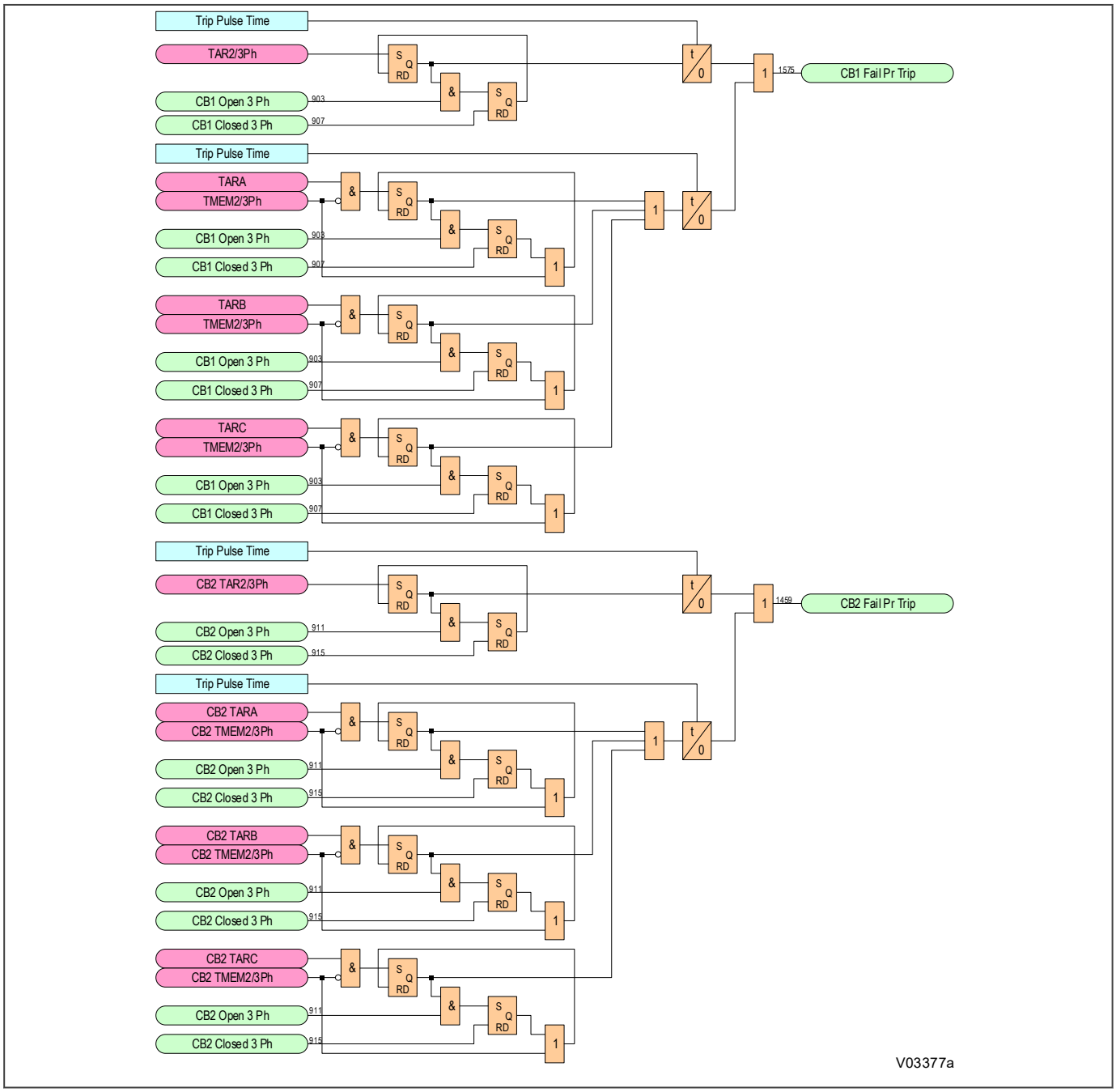


Figure 115: Circuit Breaker Trip Time Monitoring logic diagram (Modules 53 & 54)

6.5.19 AUTORECLOSE LOCKOUT

A number of events will cause Autoreclose lockout. If this happens an Autoreclose lockout alarm is raised. In this condition, Autoreclose cannot be initiated until the corresponding lockout has been reset.

The following events force Autoreclose lockout:

- Protection operation during reclaim time. Following the final Autoreclose attempt, if the protection operates during the reclaim time, the AR cycle goes to AR lockout and the Autoreclose function is disabled until the AR lockout condition is reset.
- Persistent fault. A fault is considered persistent if the protection re-operates after the last permitted shot.

- Block Autoreclose. If the block Autoreclose DDB is asserted whilst Autoreclose is in progress, the cycle goes to lockout.
- Protection function selection. Setting ‘Block AR’ against a particular protection function in the AUTORECLOSE column means that operation of the protection will block Autoreclose and force lockout.
- Circuit breaker failure to close. If a circuit breaker fails to close Autoreclose is blocked and forced to lockout.
- Circuit breaker remains open at the end of the reclaim time. An Autoreclose lockout is forced if the circuit breaker is open at the end of the reclaim time.
- Circuit breaker fails to close when the close command is issued.
- Circuit breaker fails to trip correctly.
- Three-phase dead time started by ‘line dead’ violation. If the line does not go dead within the ***Dead Line Time*** setting, the logic forces the Autoreclose sequence to lockout. Determination of when to start the timer is made in the ***3PDTStart WhenLD*** setting.
- Block Follower if Leader fails to close is set. If the setting ***BF if Lfail Cls*** in the *AUTORECLOSE* column is set to *Enable*, the active Follower circuit breaker will lockout if the Leader circuit breaker fails to reclose.
- Leader/Follower invalid selection using opto-isolated input. If the Leader/Follower Autoreclose mode in the *AUTORECLOSE* settings is set to be selected using the opto-isolated inputs, then if the logic detects an invalid Autoreclose mode combination, it forces both circuit breakers to lockout if a trip occurs.

6.5.19.1 CB LOCKOUT LOGIC DIAGRAM

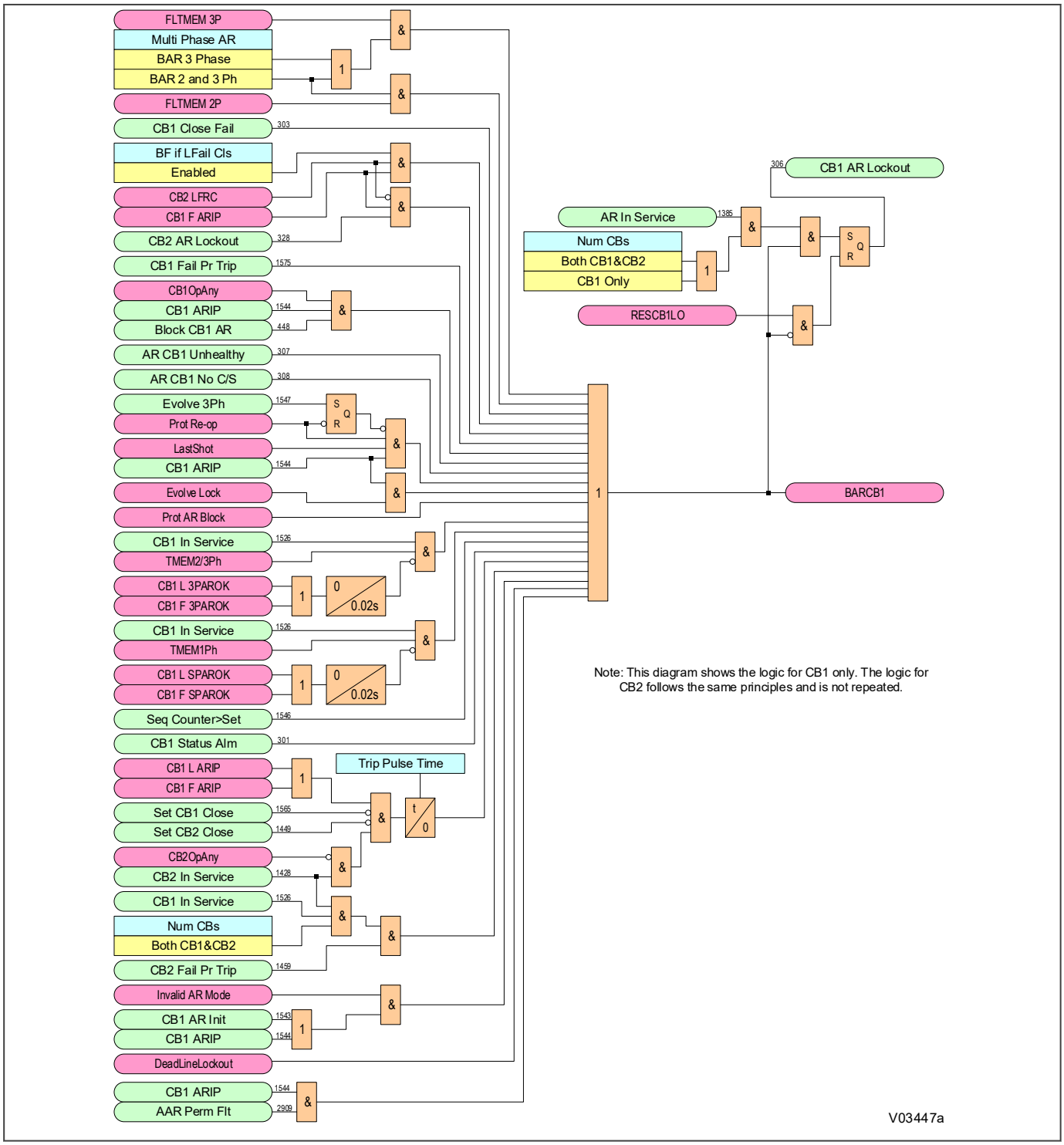


Figure 116: CB1 Lockout Logic Diagram (Module 55)

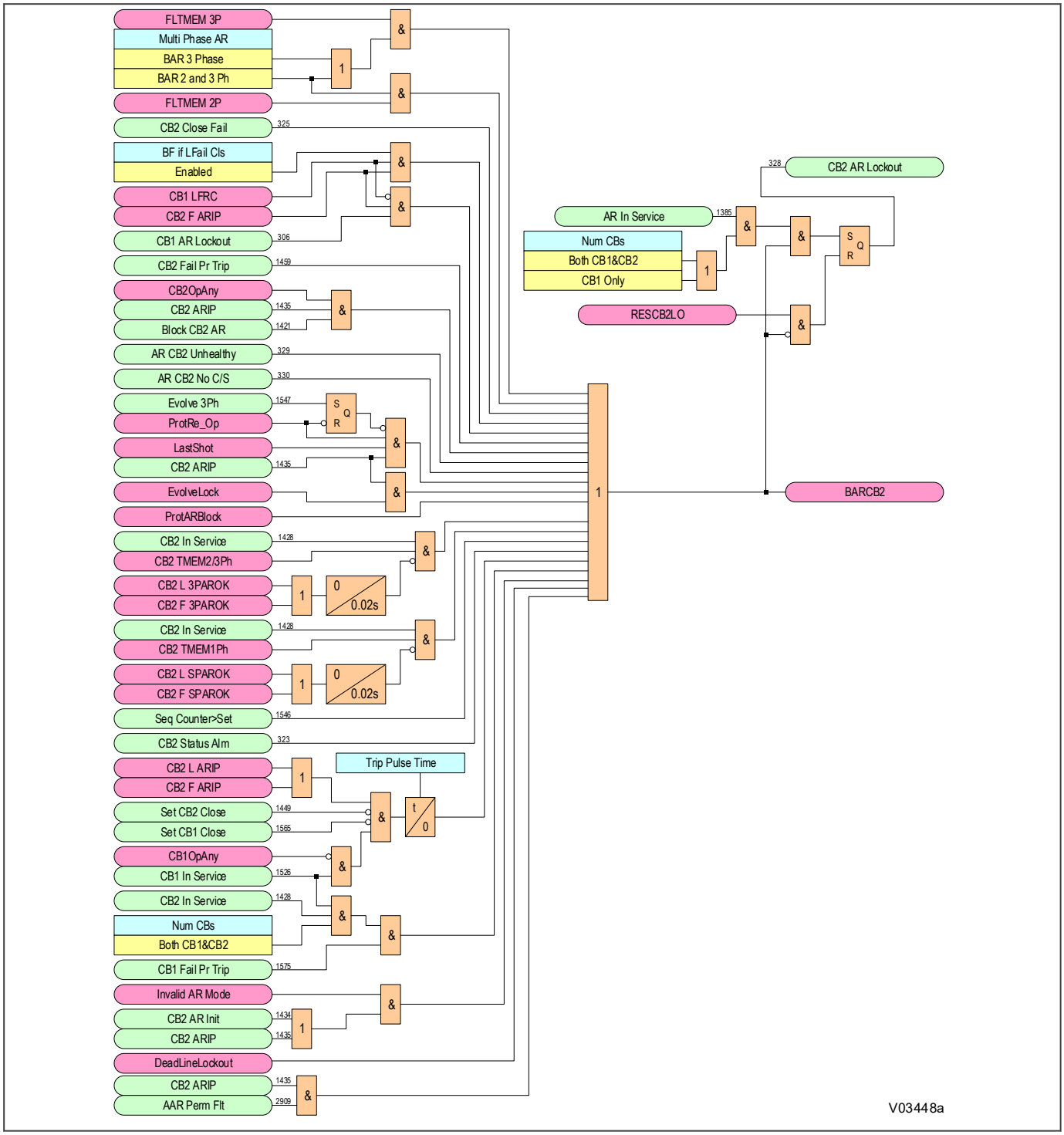


Figure 117: CB2 Lockout Logic Diagram (Module 56)

6.5.20 RESET CIRCUIT BREAKER LOCKOUT

Lockout conditions caused by the circuit breaker condition monitoring functions can be reset according to the condition of the ***Rst CB mon LO*** by setting found in the *CB CONTROL* column. There are two options; `CB Close` and `User interface`.

If set to `CB Close`, a timer setting, ***CB mon LO RstDly***, becomes visible. When the circuit breaker closes, the ***CB mon LO RstDly*** time starts. The lockout is reset when the timer expires.

If set to `User Interface` then a command, ***CB mon LO reset***, becomes visible. This command can be used to reset the lockout from a user interface.

An Autoreclose lockout generates an Autoreclose lockout alarm. Autoreclose lockout conditions can be reset by various commands and setting options found under the *CB CONTROL* column.

If ***Res LO by CB IS*** is set to `Enabled`, a lockout is reset if the circuit breaker is successfully closed manually. For this, the circuit breaker must remain closed long enough so that it enters the “In Service” state.

If ***Res LO by UI*** is set to `Enabled`, the circuit breaker lockout can be reset from a user interface using the reset circuit breaker lockout command in the *CB CONTROL* column.

If ***Res LO by NoAR*** is set to `Enabled`, the circuit breaker lockout can be reset by temporarily generating an ***AR disabled*** signal.

If ***Res LO by TDelay*** is set to `Enabled`, the circuit breaker lockout is automatically reset after a time delay set in the ***LO Reset Time*** setting.

If ***Res LO by ExtDDB*** is `Enabled`, the circuit breaker lockout can be reset by activation of an external input mapped in the PSL to the relevant reset lockout DDB signal.

6.5.20.1 RESET CB LOCKOUT LOGIC DIAGRAM

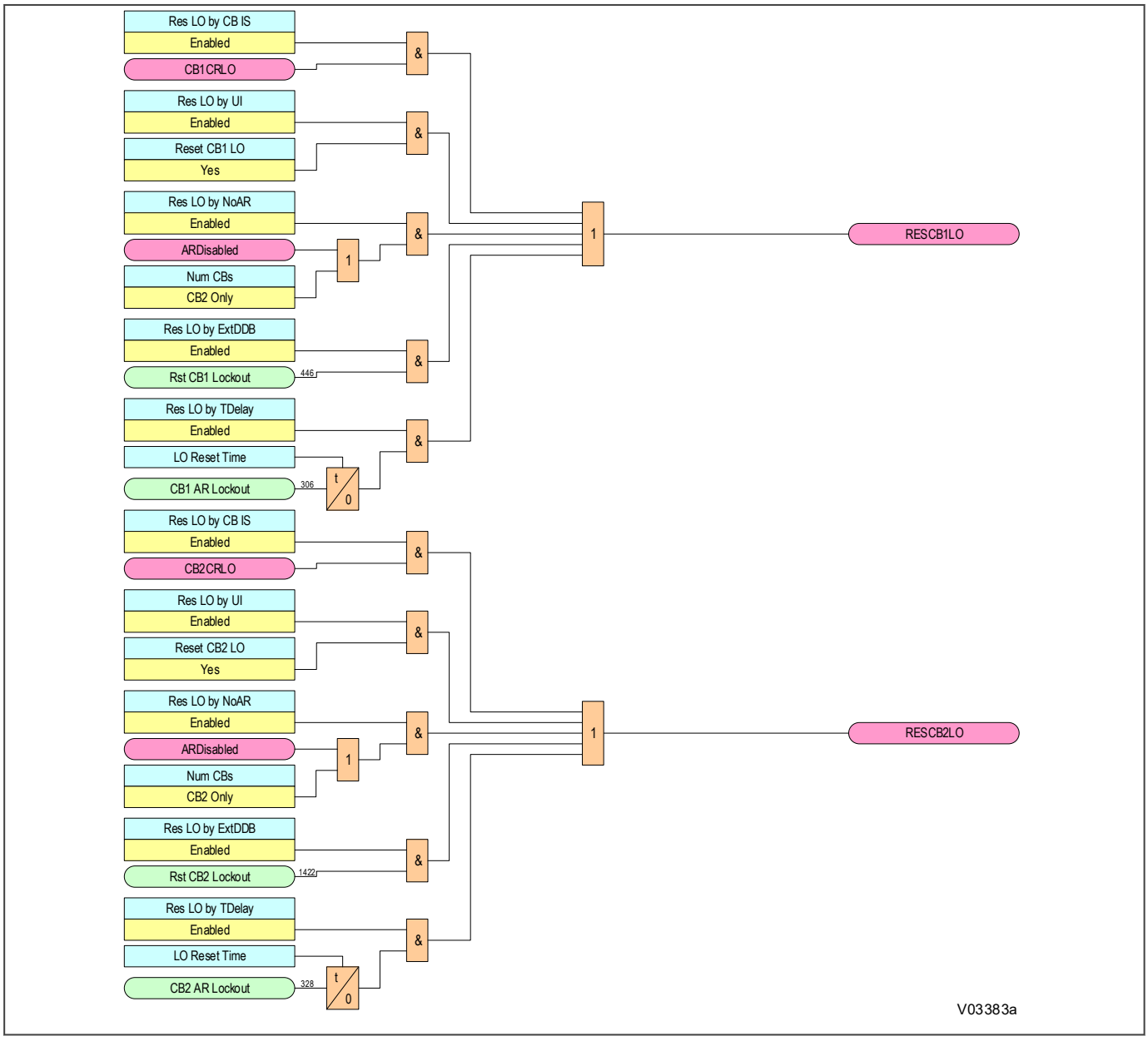


Figure 118: Reset Circuit Breaker Lockout Logic Diagram (Modules 57 & 58)

6.5.21 POLE DISCREPANCY

In a three-pole CB, certain combinations of poles open and closed are indicative of a problem. The Pole Discrepancy Logic combines an indication of a Pole Discrepancy condition from the CB Monitoring logic with signals from the internal Autoreclose logic to produce a combined Pole Discrepancy indication for the CB.

6.5.21.1 POLE DISCREPANCY LOGIC DIAGRAM

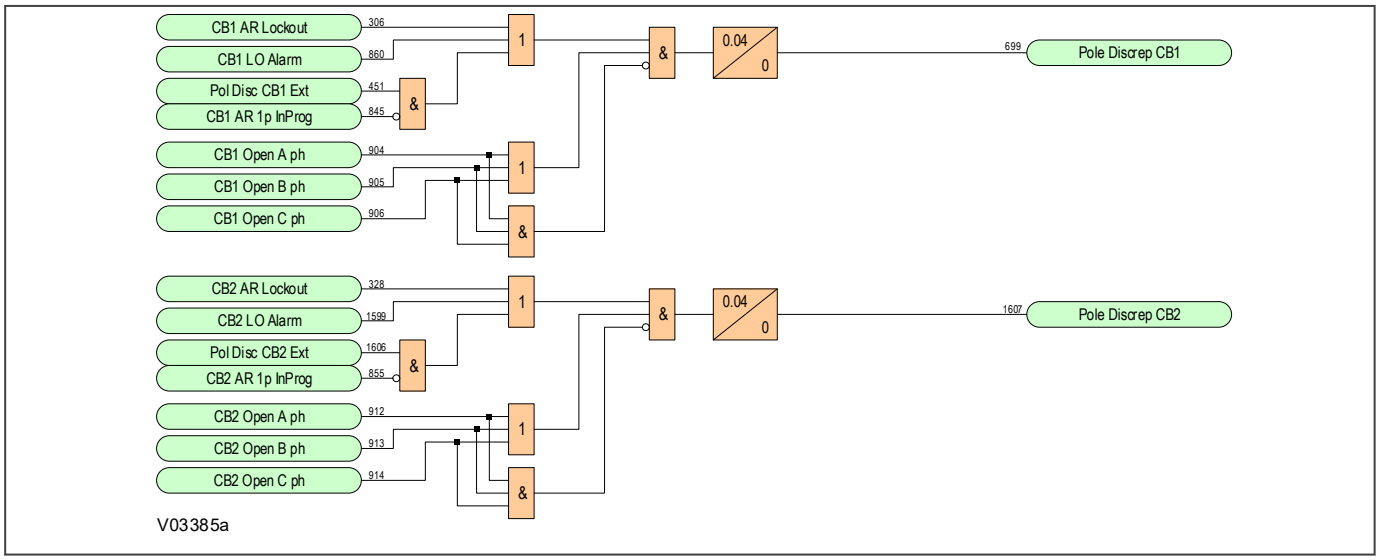


Figure 119: Pole Discrepancy Logic Diagram (Module 62)

6.5.22 CIRCUIT BREAKER TRIP CONVERSION

Circuit breakers should only trip single-pole or three-pole. The trip conversion logic ensures that the tripping is either single-pole or three-pole. The trip conversion logic ensures that all conditions that should cause three-pole tripping do so. Indication of the number of phases that caused tripping is provided.

6.5.22.1 CB TRIP CONVERSION LOGIC DIAGRAM

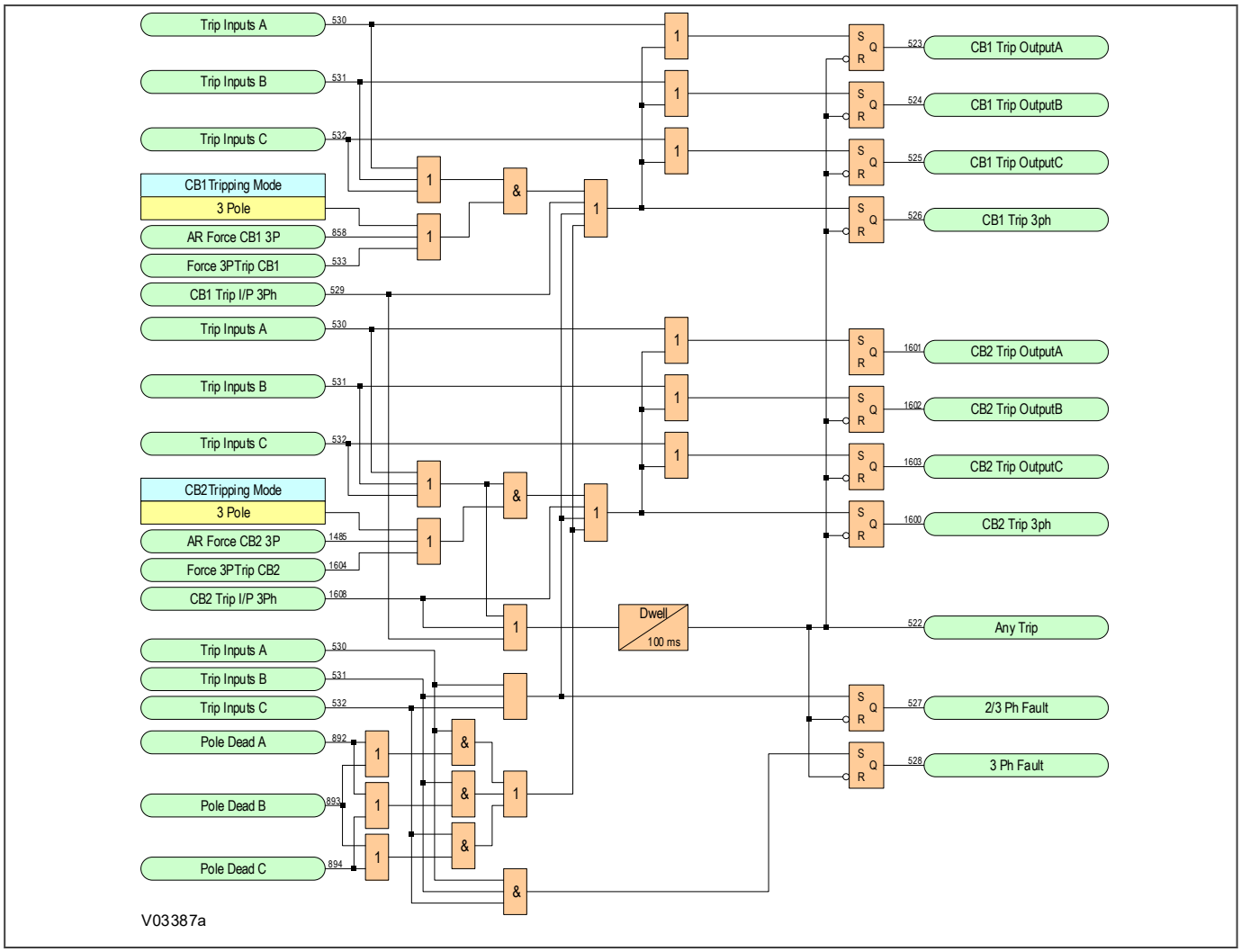


Figure 120: Circuit Breaker Trip Conversion Logic Diagram (Module 63)

6.5.23 MONITOR CHECKS FOR CB CLOSURE

For single-phase Autoreclose neither voltage nor synchronisation checks are needed as synchronising power should be flowing in the two healthy phases. For three-phase Autorelcose, for the first shot (and only the first shot), you can choose to attempt reclosure without performing a synchronisation check. The setting to permit Autoreclose without checking synchronising conditions is ***CB SC Shot 1***.

Otherwise, synchronising checks on voltages, relative frequencies, and relative phase angles are needed to ensure that sympathetic conditions exist before CB closure is attempted.

The following diagrams detail the Monitor Checks for CB closure.

6.5.23.1 VOLTAGE MONITOR FOR CB CLOSURE

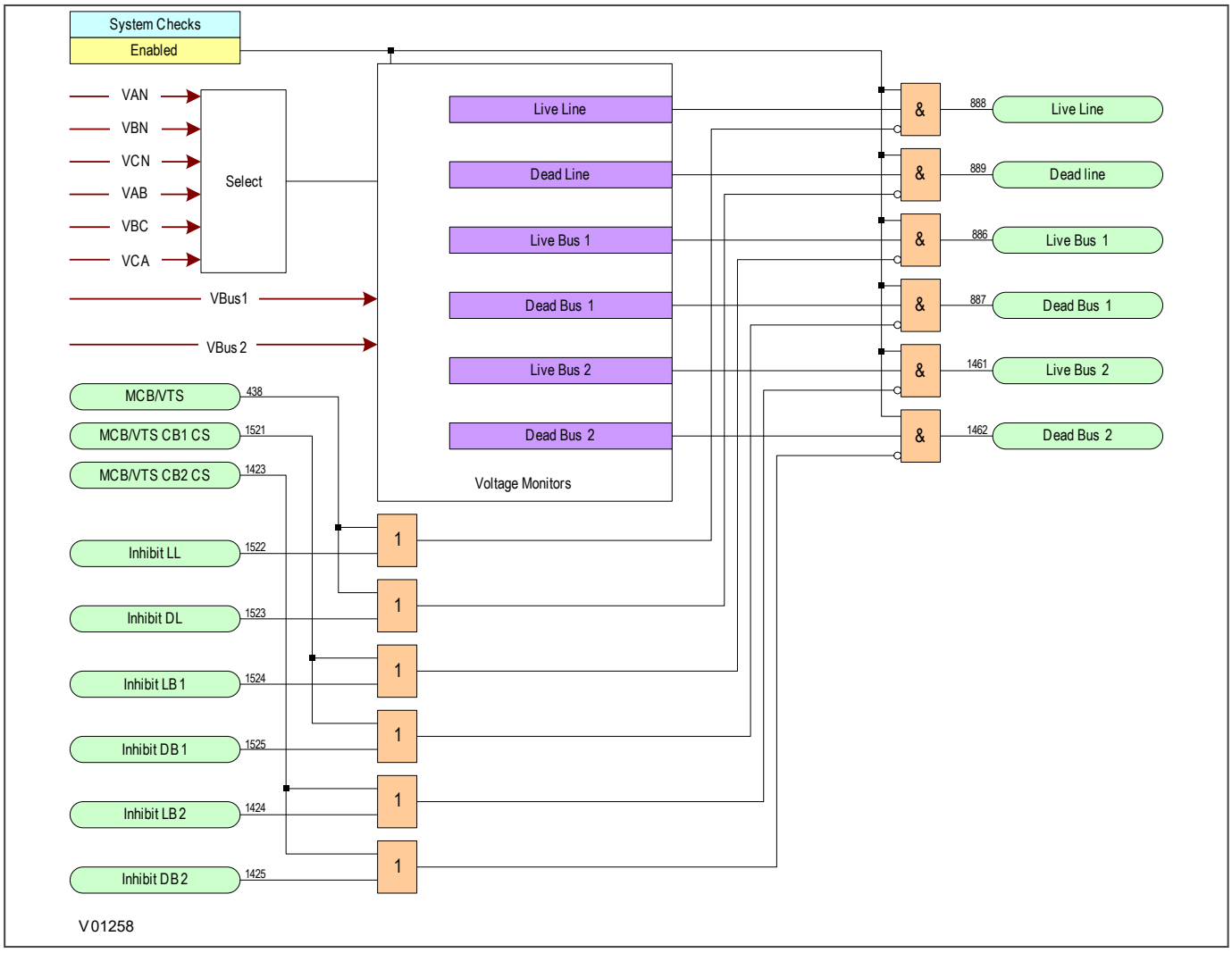


Figure 121: Voltage Monitor for CB Closure (Module 59)

6.5.23.2 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

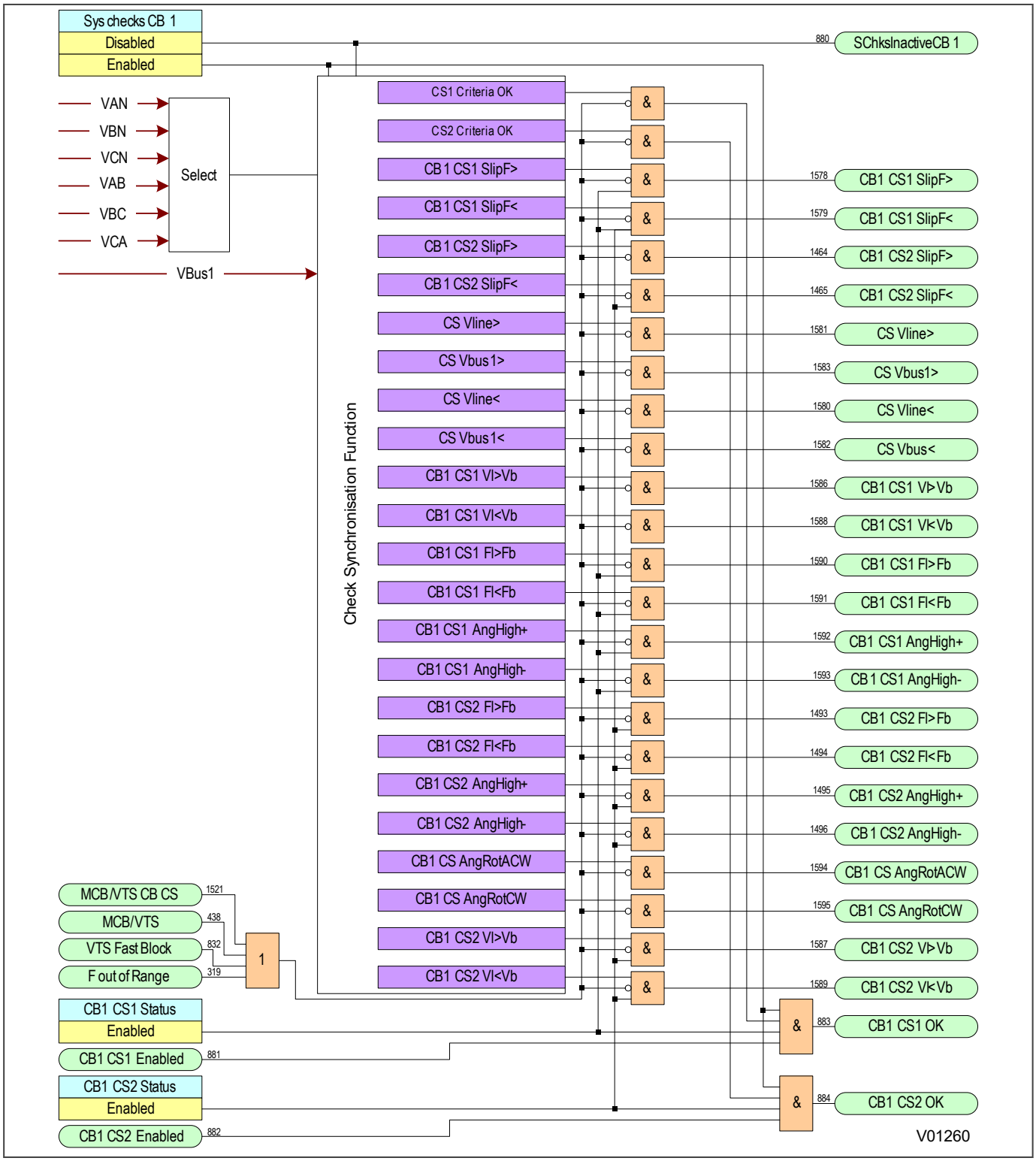


Figure 122: Check Synchronisation Monitor for CB1 closure (Module 60)

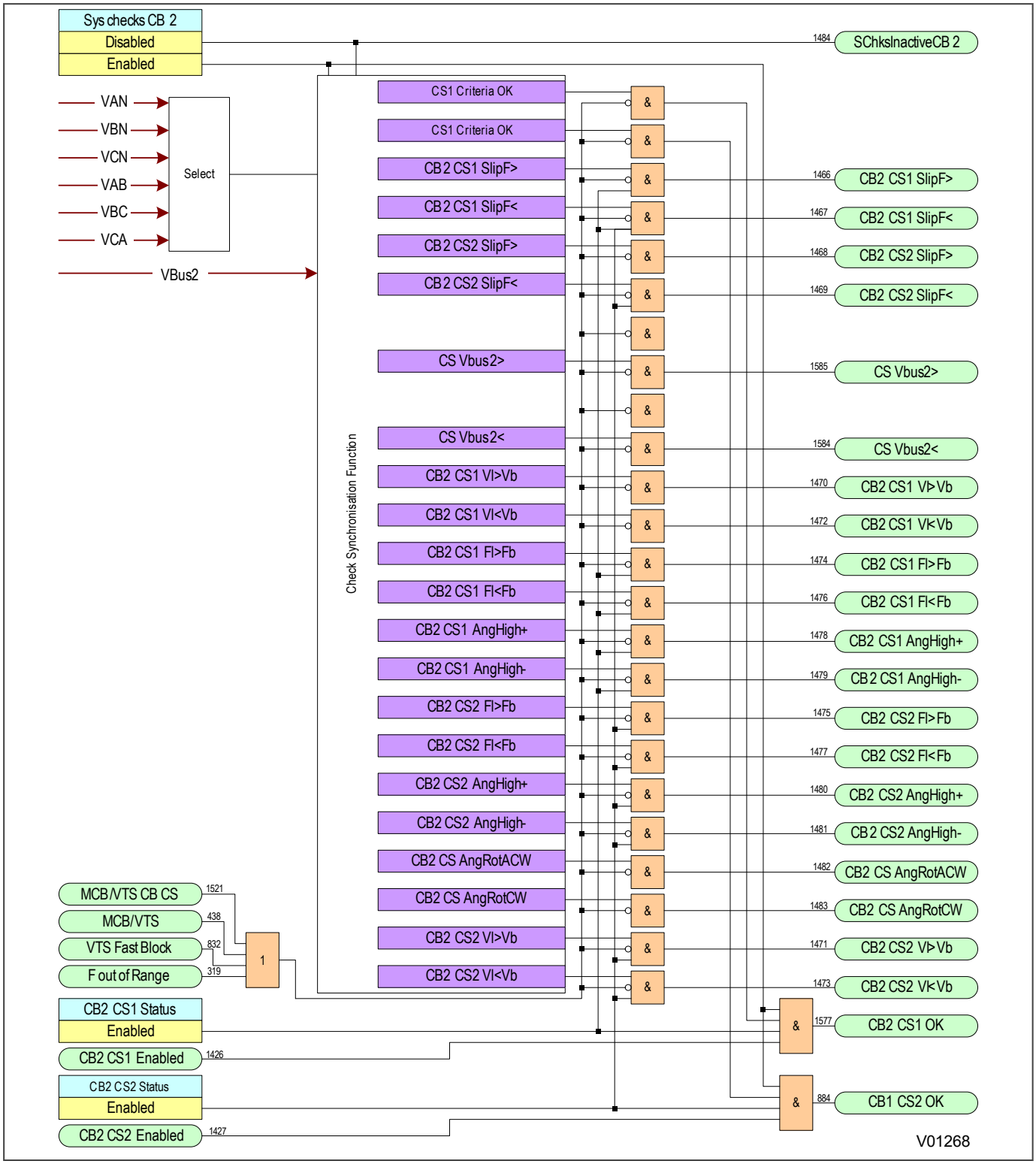


Figure 123: Check Synchronisation Monitor for CB2 closure (Module 61)

6.5.24 SYNCHRONISATION CHECKS FOR CB CLOSURE

Logical checking of the outputs from the CB closure monitors is performed to generate signals to indicate that it is OK to close circuit breakers.

Signals are provided to indicate that manual CB closure conditions are OK (***CB Man SCOK***), as are signals to indicate that automatic CB closure conditions are OK (***CB SCOK*** and ***CB Fast SCOK***). The ***CB Fast SCOK*** signal allows CB autoreclosure without waiting for the Dead Time to expire.

For single-phase Autoreclose no voltage or synchronism check is required as synchronising power is flowing in the two healthy phases. Three-phase Autoreclose can be performed without checking that voltages are in synchronism for the first shot (and only the first shot). The settings to permit Autoreclose without checking voltage synchronism on the first shot are:

- ***CB1L SC Shot 1*** for circuit breaker 1 as a leader,
- ***CB1F SC Shot 1*** for circuit breaker 1 as a follower,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a leader,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a follower.

When the circuit breaker has closed, the Autoreclose function asserts a DDB signal ***Set CB1 Close***, which indicates that an attempt has been made to close the circuit breaker. At this point, the Reclaim Time starts. If the circuit breaker remains closed after the reclaim timer expires, the Autoreclose cycle is complete, and signals are generated to indicate that Autoreclose was successful. These are:

- ***CB1 Succ 1P AR*** (Single-phase Autoreclose CB1)
- ***CB2 Succ 1P AR*** (Single-phase Autoreclose CB2)
- ***CB1 Succ 3P AR*** (Three-phase Autoreclose CB1)
- ***CB2 Succ 3P AR*** (Three-phase Autoreclose CB2)

These signals increment the relevant circuit breaker successful Autoreclose shot counters, as well as resetting the Autoreclose in progress signal.

The relevant circuit breaker successful Autoreclose shot counters are:

- ***CB1 SUCC SPAR*** (Single-phase Autoreclose CB1)
- CB1 SUCC 3PAR Shot1 (Three-phase Autoreclose CB1, Shot 1)
- CB1 SUCC 3PAR Shot2 (Three-phase Autoreclose CB1, Shot 2)
- CB1 SUCC 3PAR Shot3 (Three-phase Autoreclose CB1, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB1, Shot 4)
- ***CB2 SUCC SPAR*** (Single-phase Autoreclose CB2)
- CB2 SUCC 3PAR Shot1 (Three-phase Autoreclose CB2, Shot 1)
- CB2 SUCC 3PAR Shot2 (Three-phase Autoreclose CB2, Shot 2)
- CB2 SUCC 3PAR Shot3 (Three-phase Autoreclose CB2, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB2, Shot 4)

6.5.24.1 THREE-PHASE AUTORECLOSE LEADER CHECK LOGIC DIAGRAM

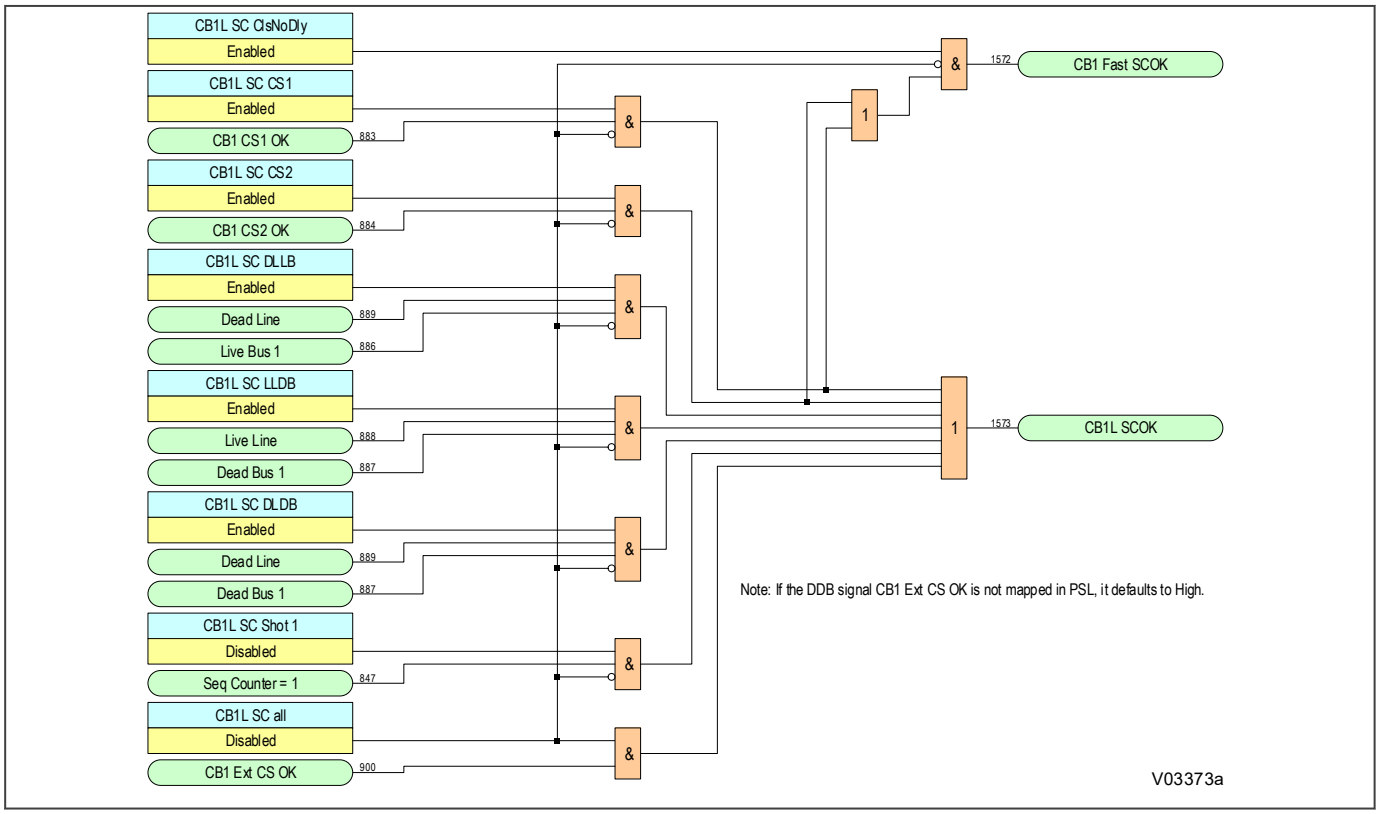


Figure 124: Three-phase AR System Check logic diagram for CB1 as leader (Module 45)

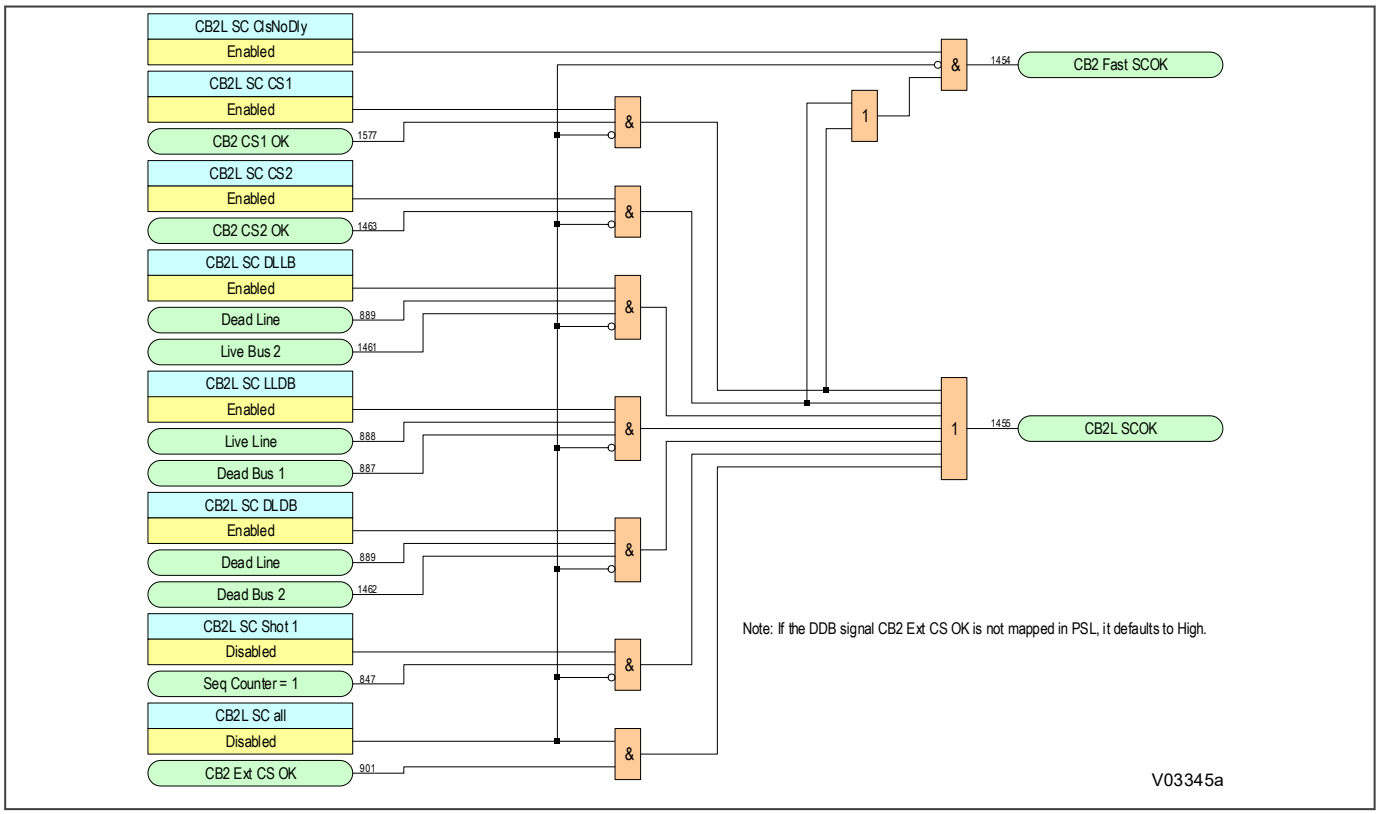


Figure 125: Three-phase AR System Check logic diagram for CB2 as leader (Module 46)

6.5.24.2 THREE-PHASE AUTORECLOSE FOLLOWER CHECK LOGIC DIAGRAM

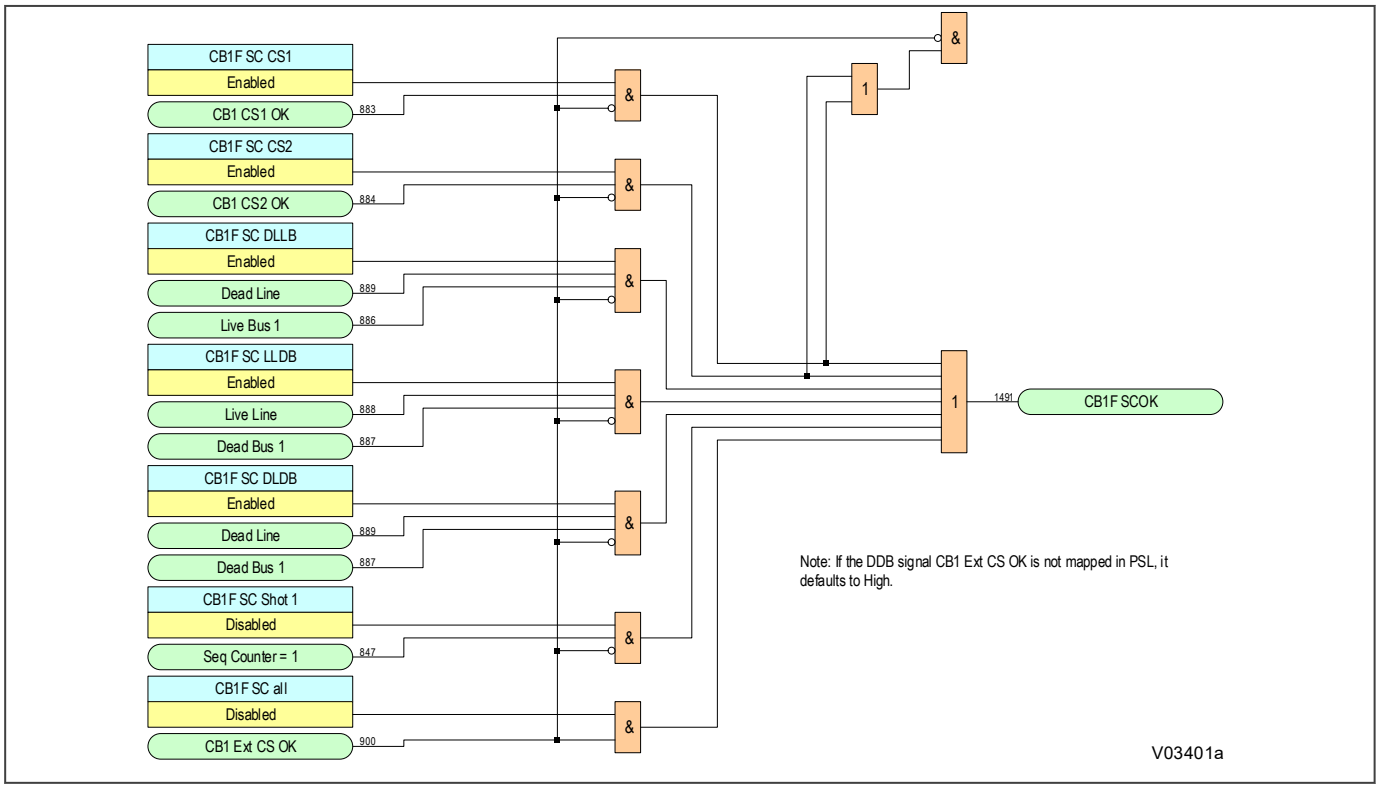


Figure 126: Three-phase AR System Check logic d for CB1 as follower (Module 47)

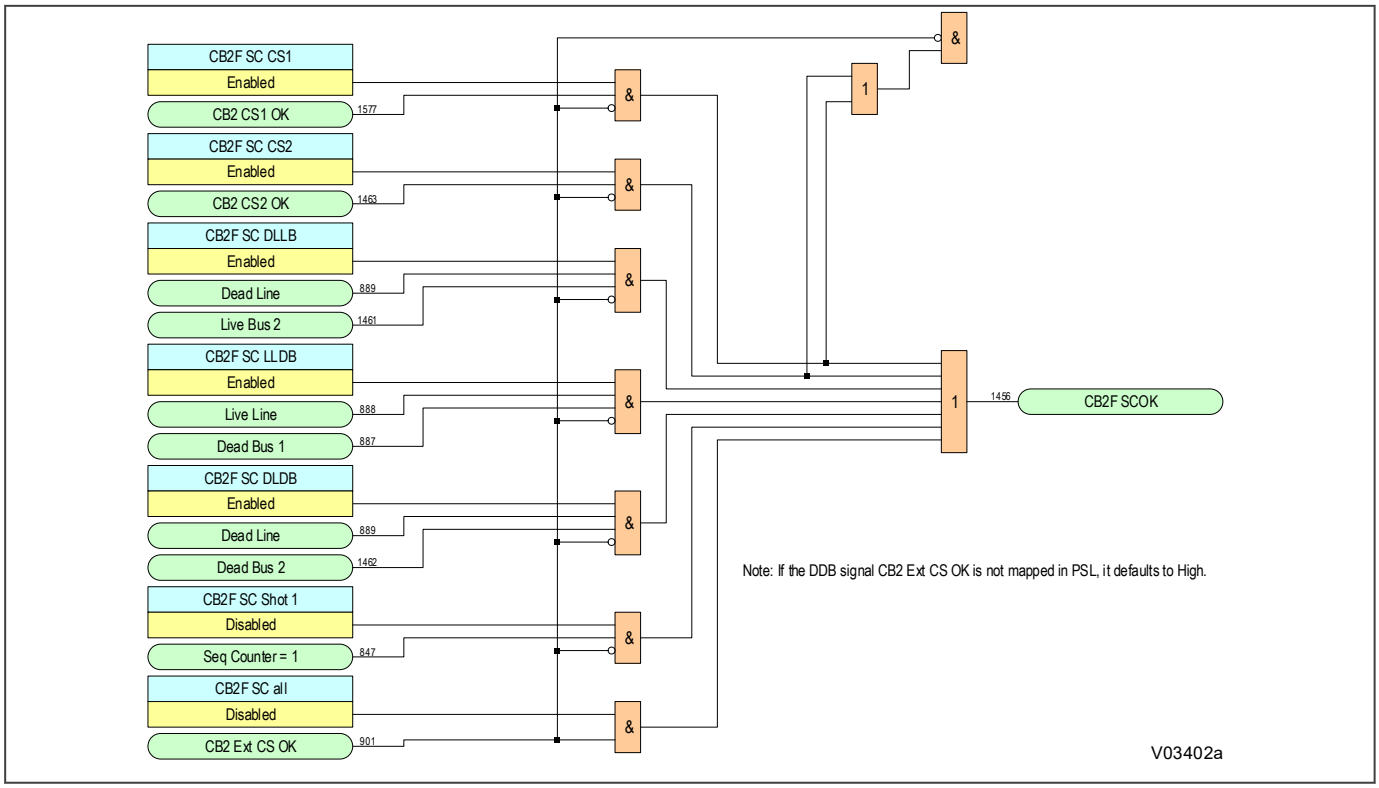


Figure 127: Three-phase AR System Check logic diagram for CB2 as follower (Module 48)

6.5.24.3 CB MANUAL CLOSE SYSTEM CHECK LOGIC DIAGRAM

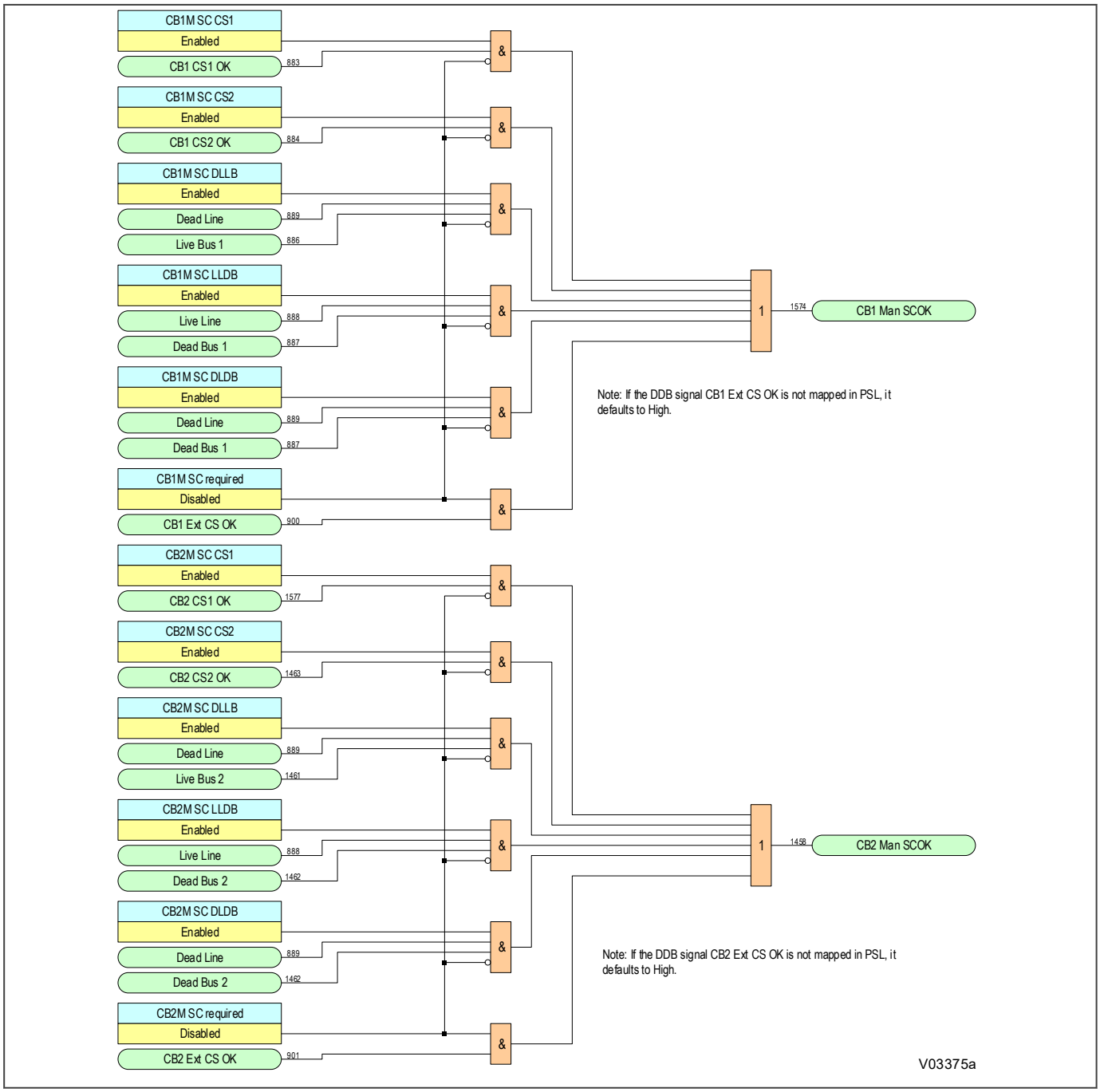


Figure 128: CB Manual Close System Check Logic Diagram (Modules 51 & 52)

6.6 SETTING GUIDELINES

6.6.1 DE-IONISING TIME GUIDANCE

The de-ionisation time of a fault arc depends on several factors such as circuit voltage, conductor spacing, fault current and duration, atmospheric conditions, wind speed and capacitive coupling from adjacent conductors. For this reason it is difficult to estimate the de-ionisation time. Circuit voltage is, generally the most significant factor and experience tells us that typical minimum de-ionising times for a three-phase fault are as follows:

- 66 kV: 100 ms
- 110 kV: 150 ms
- 132 kV: 170 ms
- 220 kV: 280 ms
- 275 kV: 300 ms
- 400 kV: 500 ms

Where single-pole high speed Autoreclose is used, the capacitive current induced between the healthy phases and the faulty phase tends to maintain the arc. This significantly increases the de-ionisation time and hence required dead time.

Single-pole Autoreclose is generally only used at transmission voltages. A typical de-ionisation time at 220 kV may be as high as 560 ms.

6.6.2 DEAD TIMER SETTING GUIDELINES

High speed Autoreclose may need to maintain stability on a network with two or more power sources. For high speed Autoreclose the system disturbance time should be minimised by using fast protection (typically <30 ms) and fast circuit breakers (typically <60 ms). For stability between two sources a system dead time of ≤300 ms may typically be required.

The minimum system dead time (considering just the circuit breaker) is the trip mechanism reset time plus the circuit breaker closing time.

The Autoreclose minimum dead time settings are governed primarily by two factors:

- Time taken for de-ionisation of the fault path
- Circuit breaker characteristics

It is essential that the protection fully resets during the dead time, so that correct time discrimination will be maintained after Autoreclose onto a fault. For high speed Autoreclose instantaneous reset of protection is required.

For highly interconnected systems synchronism is unlikely to be lost by the tripping out of a single line. Here the best policy may be to adopt longer dead times, to allow time for power swings resulting from the fault to settle.

The dead time is normally a fixed time delay but can be can set to adaptive for single-pole autoreclose schemes where it is dependent on the arc extinction time for a transient single-phase fault.

The autoreclose scheme is adaptive when the ***Adaptive SP AR*** setting is `Enabled`. The adaptive autoreclose is only available for single-pole autoreclose applications. The ***SP Min Dead Time*** (0-10s) is the minimum dead time for a single-pole autoreclose. The actual dead time is set to the SP minimum dead time or the time for the secondary arc to extinguish if it is within maximum dead time, whichever is greater. The ***SP Max Dead Time*** (0-10s) is the maximum dead time for single-pole autoreclose. If the secondary arc does not extinguish or it is detected as a permanent fault within the SP maximum dead time, the autoreclose will issue a three-phase trip command and lock out. If a transient fault is detected within the SP maximum dead time, the autoreclose logic will issue a close command to close the open pole. When the AAR dead time exceeds the SP Max Dead Time or there is no output from the AAR logic within the ***SP Max Dead Time***, the output of the autoreclose logic will either reclose or go to A/R lockout based on selection of the ***SP Max Dead Time Elapsed*** – `Reclose`/`Lockout` setting.

6.6.2.1 EXAMPLE DEAD TIME CALCULATION

The following circuit breaker and system characteristics can be used for the minimum dead time calculation:

- a) Circuit breaker Operating time (Trip coil energized to Arc interruption): 50 ms
- b) Circuit breaker Opening + Reset time (Trip coil energized to trip mechanism reset): 200 ms
- c) Protection reset time: < 80 ms
- d) Circuit breaker Closing time (Close command to Contacts make): 85 ms
- e) De-ionisation time (280 ms for 3-phase, or 560 ms for 1-phase)

Three-phase de-ionisation time for 220 kV line is typically 280 ms.

The minimum Autoreclose dead time setting is therefore the greater of:

(a) + (c) = 50 ms + 80 ms = 130 ms, to allow protection reset

(a) + (e) - (d) = 50 ms + 280 ms - 85 ms = 245 ms, to allow de-ionising

In practice a few additional cycles would be added to allow for tolerances, so Dead Time 1 could be set to 300 ms or greater. The overall system dead time is found by adding (d) to the chosen settings then subtracting (a). This gives 335 ms.

A typical de-ionising time value for single-phase trip on a 220 kV line is 560 ms, so the 1 Pole Dead Time could be chosen as 600 ms or greater. The overall system dead time is found by adding (d) to the chosen settings then subtracting (a). This gives 635 ms.

6.6.3 RECLAIM TIME SETTING GUIDELINES

Several factors influence the choice of the reclaim timer, such as:

- Fault incidence/Past experience: Small reclaim times may be required where there is a high incidence of recurrent lightning strikes to prevent unnecessary lockout for transient faults.
- Spring charging time: For high speed Autoreclose the reclaim time may be set longer than the spring charging time. A minimum reclaim time of more than 5s may be needed to allow the circuit breaker time to recover after a trip and close before it can perform another trip-close-trip cycle. This time will depend on the duty (rating) of the circuit breaker. For delayed Autoreclose this may not be needed as the dead time can be extended by an extra circuit breaker healthy check / Autoreclose Inhibit Time window time if there is insufficient energy in the circuit breaker.
- Switchgear Maintenance: Excessive operation resulting from short reclaim times can mean shorter maintenance intervals.

When used in conjunction with distance protection, the Reclaim Time setting is generally set greater than the zone 2 delay.

6.6.4 AUTORECLOSE SHOT COUNTERS

In dual circuit breaker applications, the two circuit breakers are normally arranged to reclose sequentially with one designated the Leader circuit breaker reclosing after a set dead time. If the Leader circuit breaker remains closed after the dead time, the second circuit breaker referred to as the Follower recloses after a further delay, the Follower Time.

The Follower Time is provided to prevent un-necessary operation of the Follower circuit breaker. The Follower Time should be set sufficiently long as to avoid an un-necessary closure of the Follower circuit breaker where conditions are such that it would be required to trip again.

After expiry of the dead time, the Leader circuit breaker will attempt Autoreclose. The minimum value of the Follower time should allow sufficient time for the Autoreclose of the Leader circuit breaker to be considered successful.

An extreme case may be where instantaneous protection is only provided by distance elements and where Autoreclose is onto a dead line with a persistent fault at the remote end of the line.

Local end protection (Time delayed Back up protection, like distance Z2 element) may detect this fault after a time delay (typically > 200 ms). In addition to the delays associated with the back-up protection (typically >200 ms), time must be allowed for the Leader circuit breaker to re-trip (50 - 100 ms), and a safety margin needs to be added so that a minimum Follower time could be around 500 ms.

If the Autoreclose of the Leader circuit breaker is successful, the Follower circuit breaker can be allowed to Autoreclose. Delaying the Autoreclose of the Follower circuit breaker will allow any transients to decay before the switching. If the transient decay figure is known, it can be used to determine a minimum Follower Time value. The larger of the two values can then be used as the minimum Follower Time.

Note:
The Follower circuit breaker should only be reclosed if the system is healthy. In a dual circuit breaker scheme where the system is healthy, the Follower circuit breaker acts more like a bus coupler. In this case there is no need for fast switching and a time delay in excess of 1s is often appropriate. The default Follower time in this product is chosen as 5 s and this can comfortably be applied to most applications.

CHAPTER 7

CB FAIL PROTECTION

7.1 CHAPTER OVERVIEW

The device provides a Circuit Breaker Fail Protection function. This chapter describes the operation of this function including the principles, logic diagrams and applications.

This chapter contains the following sections:

7.2 CIRCUIT BREAKER FAIL PROTECTION

When a fault occurs, one or more protection devices will operate and issue a trip command to the relevant circuit breakers. Operation of the circuit breaker is essential to isolate the fault and prevent, or at least limit, damage to the power system. For transmission and sub-transmission systems, slow fault clearance can also threaten system stability.

For these reasons, it is common practice to install Circuit Breaker Failure protection (CBF). CBF protection monitors the circuit breaker and establishes whether it has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, the CBF protection will operate, whereby the upstream circuit breakers are back-tripped to ensure that the fault is isolated.

CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

7.3 CIRCUIT BREAKER FAIL IMPLEMENTATION

Circuit Breaker Failure Protection is implemented in the *CB FAIL & P.DEAD* column of the relevant settings group. Independent CB Fail settings are provided for CB1 and CB2 in dual CB versions.

7.3.1 CIRCUIT BREAKER FAIL TIMERS

The circuit breaker failure protection incorporates two timers, ***CB Fail 1 Timer*** and ***CB Fail 2 Timer***, allowing configuration for the following scenarios:

- Simple CBF, where only ***CB Fail 1 Timer*** is enabled. For any protection trip, the **CB Fail 1** ***Timer*** is started, and normally reset when the circuit breaker opens to isolate the fault. If breaker opening is not detected, the CB Fail 1 Timer times out and closes an output contact assigned to breaker fail (using the programmable scheme logic). This contact is used to back-trip upstream switchgear, generally tripping all infeeds connected to the same busbar section.
- A retripping scheme, plus delayed back-tripping. Here, ***CB Fail 1 Timer*** is used to issue a trip command to a second trip circuit of the same circuit breaker. This requires the circuit breaker to have duplicate circuit breaker trip coils. This mechanism is known as retripping. If retripping fails to open the circuit breaker, a back-trip may be issued following an additional time delay. The back-trip uses ***CB Fail 2 Timer***, which was also started at the instant of the initial protection element trip.

You can configure the CBF elements ***CB Fail 1 Timer*** and ***CBF Fail 2 Timer*** to operate for trips triggered by protection elements within the device. Alternatively you can use an external protection trip by allocating one of the opto-inputs to the ***External Trip*** DDB signal in the PSL.

You can reset the CBF from a breaker open indication (from the pole dead logic) or from a protection reset. In these cases resetting is only allowed if the undercurrent elements have also been reset. The resetting mechanism is determined by the settings ***NonIProt Rst*** and ***Ext Prot Rst***.

The resetting options are summarised in the following table:

Initiation (Menu Selectable)	CB Fail Timer Reset Mechanism
Current based protection (e.g.50/51/46/21/87)	IA< operates AND IB< operates AND IC< operates AND IN< operates or through Ext Rst DDB in PSL
Sensitive Earth Fault element	ISEF< Operates or Ext Rst SEF DDB
Non-current based protection (e.g. 27/59/81/32L)	Five options are available: All I< and IN< elements operate or Ext Rst CBF DDB Protection element reset AND (all I< and IN< elements operate or Ext Rst DDB CB open (all 3 poles) AND all I< and IN< elements operate
External protection	Five options are available. All I< and IN< elements operate External trip reset AND all I< and IN< elements operate CB open (all 3 poles) AND all I< and IN< elements operate Prot Reset OR I<: External trip reset OR all I< and IN< elements operate Rst or CBOp & I<: External trip reset OR Pole Dead AND all I< and IN< elements operate

7.3.2 CIRCUIT BREAKER FAIL INITIATION

If ***ExtTrip Only Ini*** setting is `Disabled`, the CBF protection can be initiated when any internal protection function issues a trip or if an external protection trip occurs. If ***ExtTrip Only Ini*** setting is `Enabled`, then only external protection is allowed to initiate the CBF function. An external protection and internal current-based protections (except SEF protection) initiate the CB Fail function on per-phase basis, while non-current-based protections and SEF initiate CB Fail for all three phases simultaneously.

7.3.3 ZERO CROSSING DETECTION

When there is a fault and the circuit breaker interrupts the CT primary current, the flux in the CT core decays to a residual level. This decaying flux introduces a decaying DC current in the CT secondary circuit known as subsidence current. The closer the CT is to its saturation point, the higher the subsidence current.

The time constant of this subsidence current depends on the CT secondary circuit time constant and it is generally long. If the protection clears the fault, the CB Fail function should reset fast to avoid maloperation due to the subsidence current. To compensate for this the device includes a zero-crossing detection algorithm, which ensures that the CB Fail re-trip and back-trip signals are not asserted while subsidence current is flowing. If all the samples within half a cycle are greater than or smaller than 0 A (10 mS for a 50 Hz system), then zero crossing detection is asserted, thereby blocking the operation of the CB Fail function. The zero-crossing detection algorithm is used after the circuit breaker in the primary system has opened ensuring that the only current flowing in the AC secondary circuit is the subsidence current.

7.4 CIRCUIT BREAKER FAIL LOGIC

7.4.1 CIRCUIT BREAKER FAIL LOGIC - PART 1

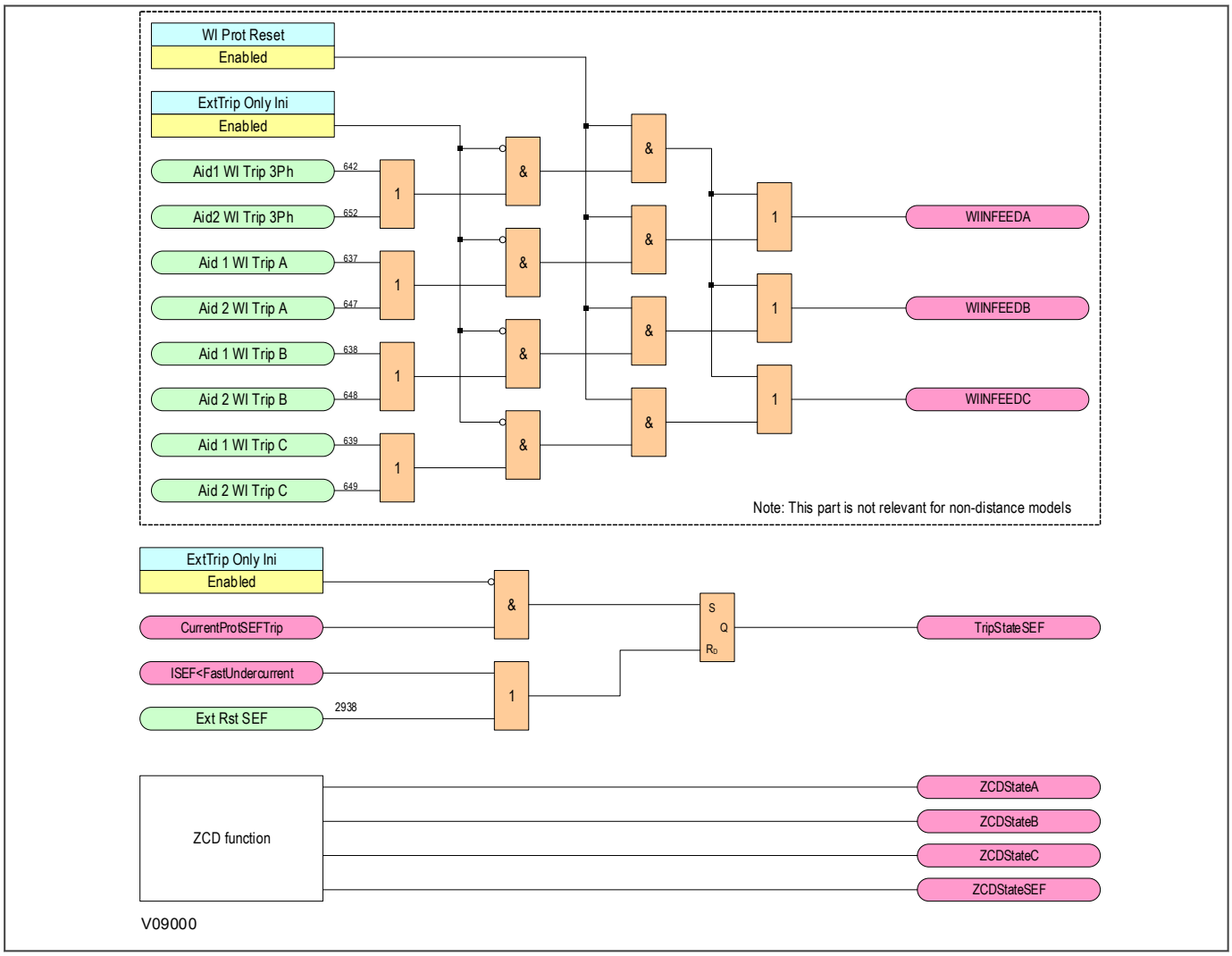


Figure 129: Circuit Breaker Fail logic - part 1

7.4.2 CIRCUIT BREAKER FAIL LOGIC - PART 2

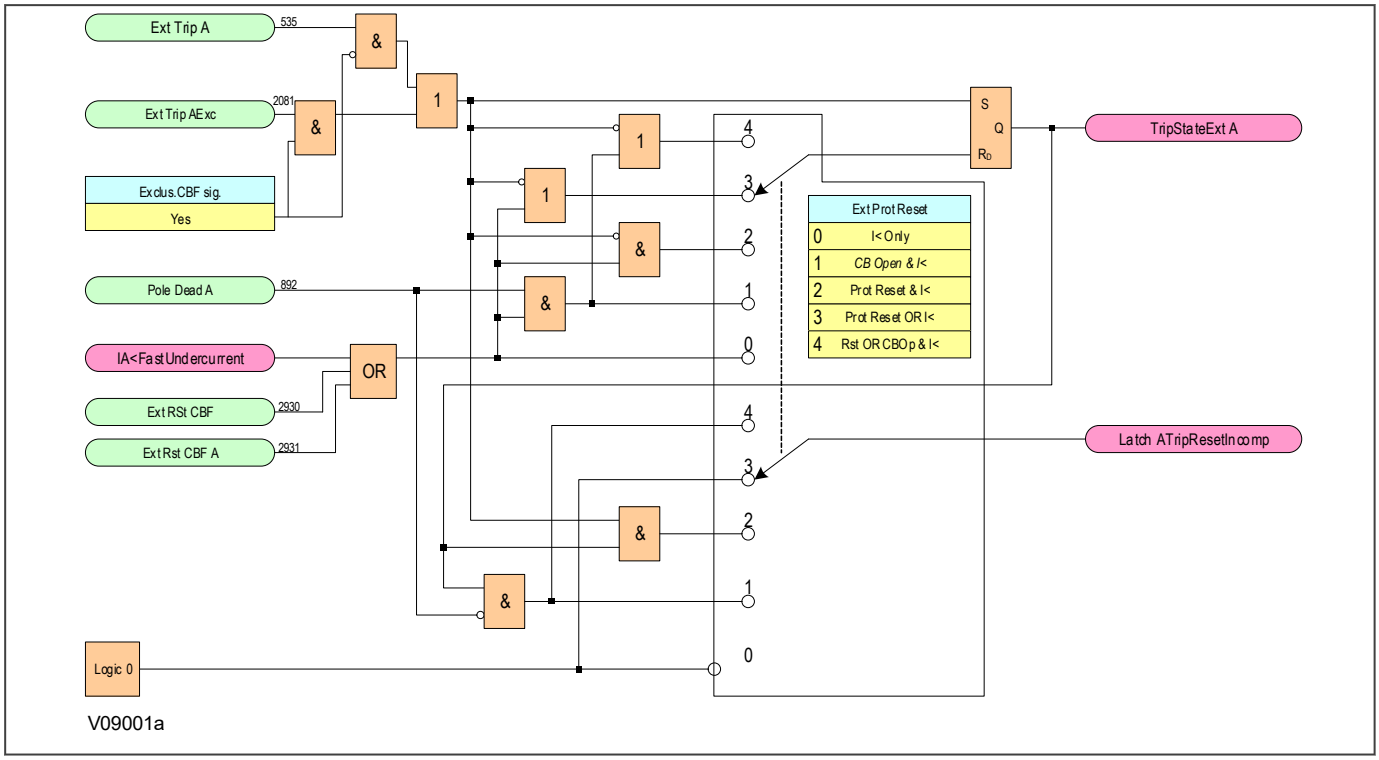


Figure 130: Circuit Breaker Fail logic - part 2

7.4.3 CIRCUIT BREAKER FAIL LOGIC - PART 2

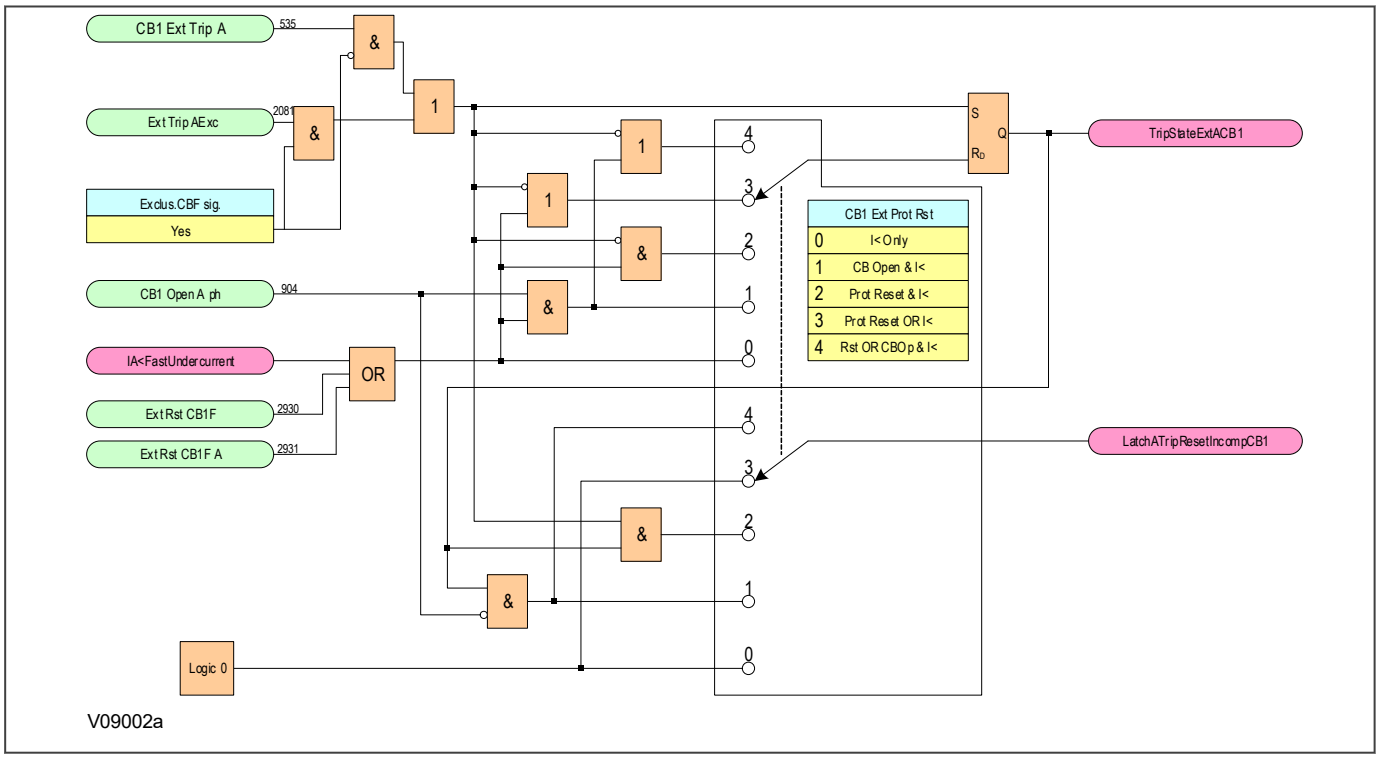


Figure 131: Circuit Breaker Fail logic - part 2

7.4.4 CIRCUIT BREAKER FAIL LOGIC - PART 3

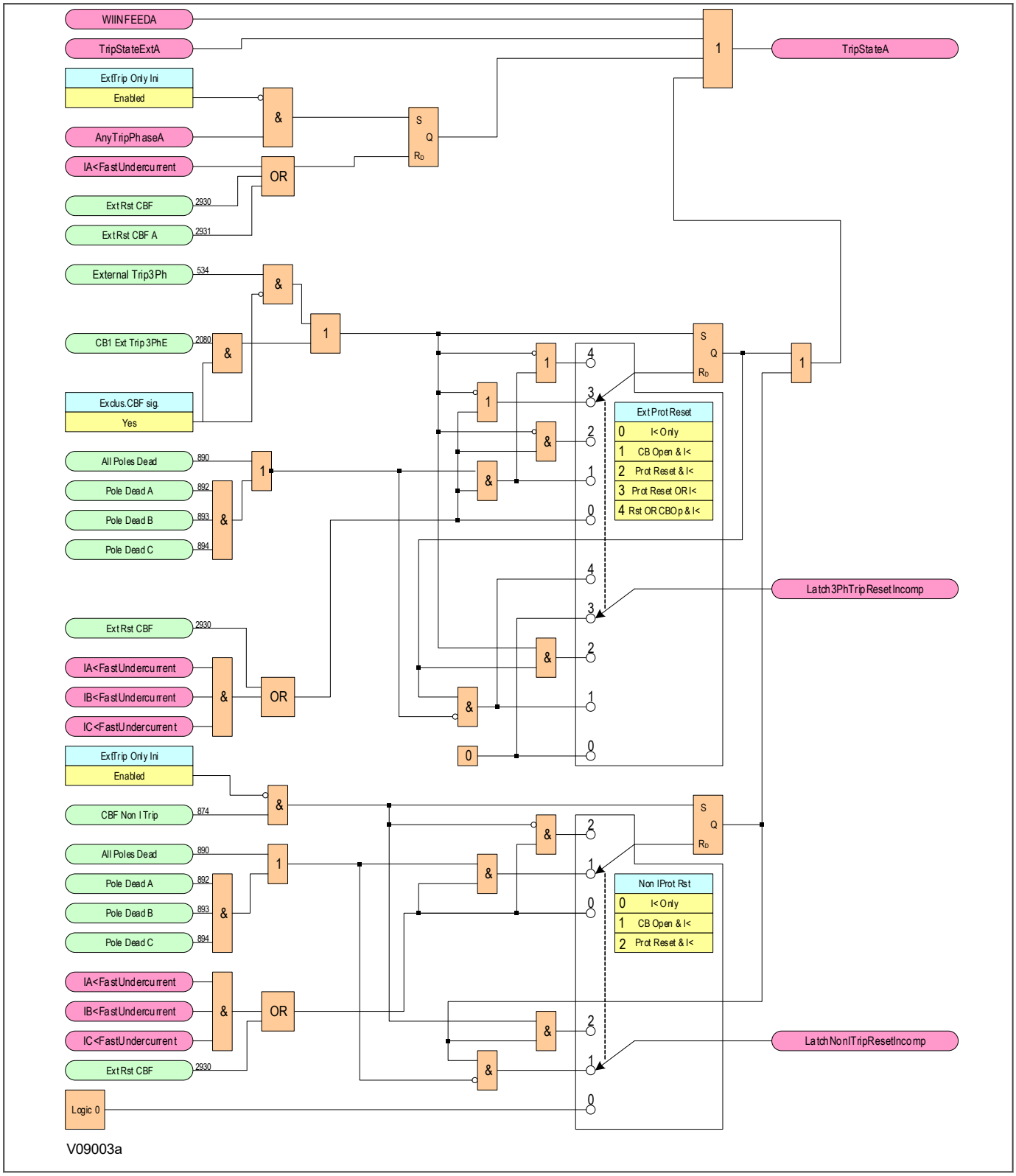


Figure 132: Circuit Breaker Fail logic - part 3

7.4.5 CIRCUIT BREAKER FAIL LOGIC - PART 3

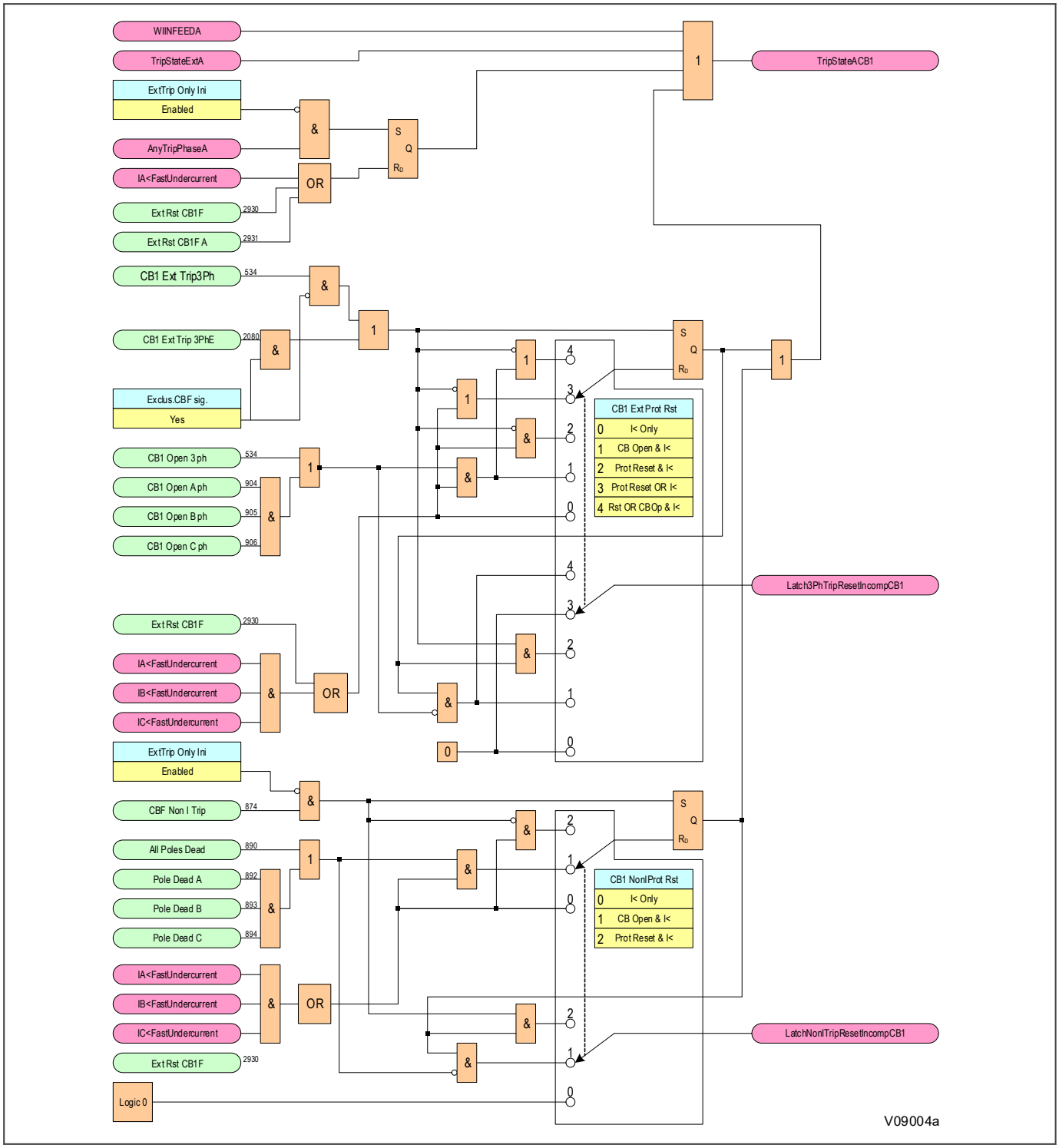


Figure 133: Circuit Breaker Fail logic - part 3

7.4.6 CIRCUIT BREAKER FAIL LOGIC - PART 4

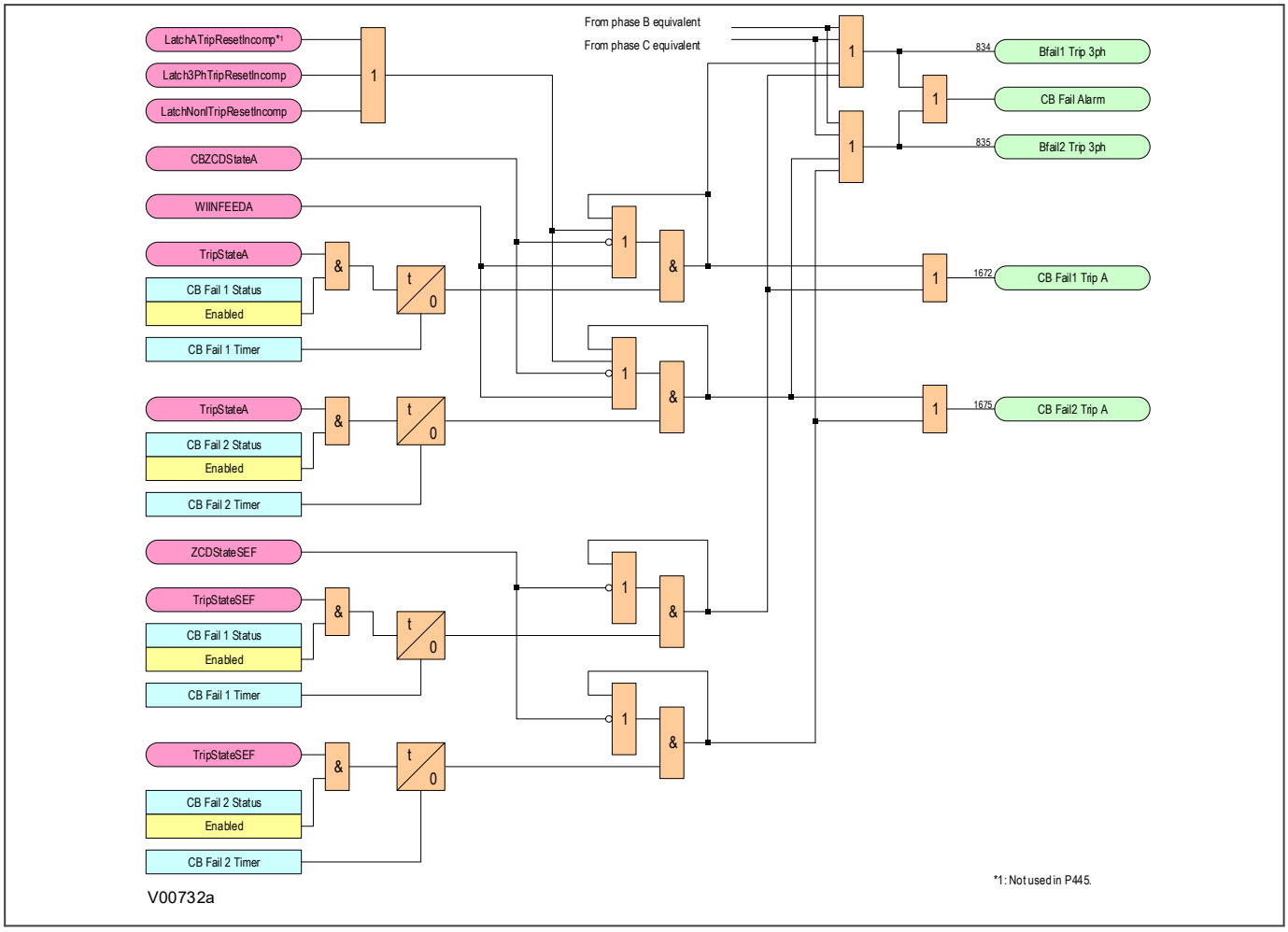


Figure 134: Circuit Breaker Fail logic - part 4

Note:
This diagram shows only phase-A for a single-CB device. The diagrams for phases B and C follow the same principle and are not repeated here.

7.4.7 CIRCUIT BREAKER FAIL LOGIC - PART 4

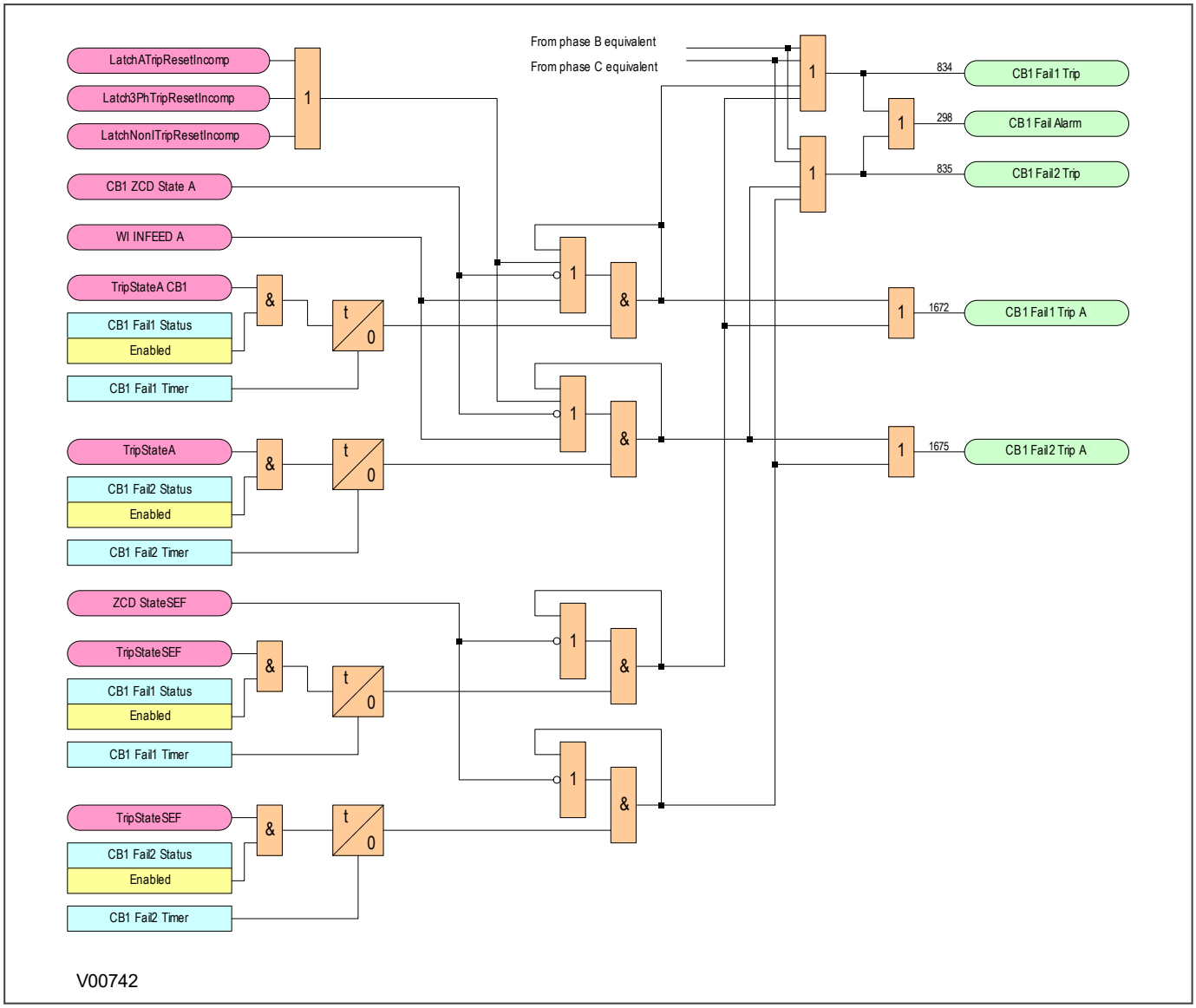


Figure 135: Circuit Breaker Fail logic - part 4

Note:
This diagram shows only phase-A for the first CB (CB1) of a dual-CB device. The diagrams for phases B and C and for the second CB (CB2) follow the same principle and are not repeated here.

7.5 APPLICATION NOTES

7.5.1 RESET MECHANISMS FOR CB FAIL TIMERS

It is common practise to use low set undercurrent elements to indicate that circuit breaker poles have interrupted the fault or load current. This covers the following situations:

- Where circuit breaker auxiliary contacts are defective, or cannot be relied on to definitely indicate that the breaker has tripped.
- Where a circuit breaker has started to open but has become jammed. This may result in continued arcing at the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance severely limit fault current, the initiating protection element may reset. Therefore, reset of the element may not give a reliable indication that the circuit breaker has opened fully.

For any protection function requiring current to operate, the device uses operation of undercurrent elements to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting CBF in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the protected circuit would always have load current flowing. In this case, detecting drop-off of the initiating protection element might be a more reliable method.
- Where distance schemes include Weak Infeed trip logic. The reset of the Weak infeed trip condition should be used in addition to the undercurrent check. ***WI Prot Reset*** should be set to `enabled`.
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again using I< would rely on the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, and so drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

You can reset the CBF from a breaker open indication (from the pole dead logic) or from a protection reset. In these cases resetting is only allowed if the undercurrent elements have also been reset. The resetting mechanism is determined by the settings ***Non I Prot Reset*** and ***Ext Prot Reset***.

If the CBF protection is initiated by an external protection trip, then two resetting options ***Prot Reset OR I<*** and ***Rst or CBOp & I<*** are provided. These settings don't necessarily require undercurrent element (I<) operation, as shown in the table below. These options are useful if re-tripping is not implemented, as they allow avoiding back-tripping due to spurious short-time energisation of External Trip opto-inputs.

Warning:
If you are using *Prot Reset OR I<* or *Rst or CBOp & I<*, do not connect the *External Trip* inputs to the Trip Conversion logic inputs in the PSL.

7.5.2 SETTING GUIDELINES (CB FAIL TIMER)

The following timing chart shows the CB Fail timing during normal and CB Fail operation. The maximum clearing time should be less than the critical clearing time which is determined by a stability study. The CB Fail back-up trip time delay considers the maximum CB clearing time, the CB Fail reset time plus a safety margin. Typical CB clearing times are 1.5 or 3 cycles. The CB Fail reset time should be short enough to avoid CB Fail back-trip during normal operation. Phase and ground undercurrent elements must be asserted for the CB Fail to reset. The assertion of the undercurrent elements might be delayed due to the subsidence current that might be flowing through the secondary AC circuit.

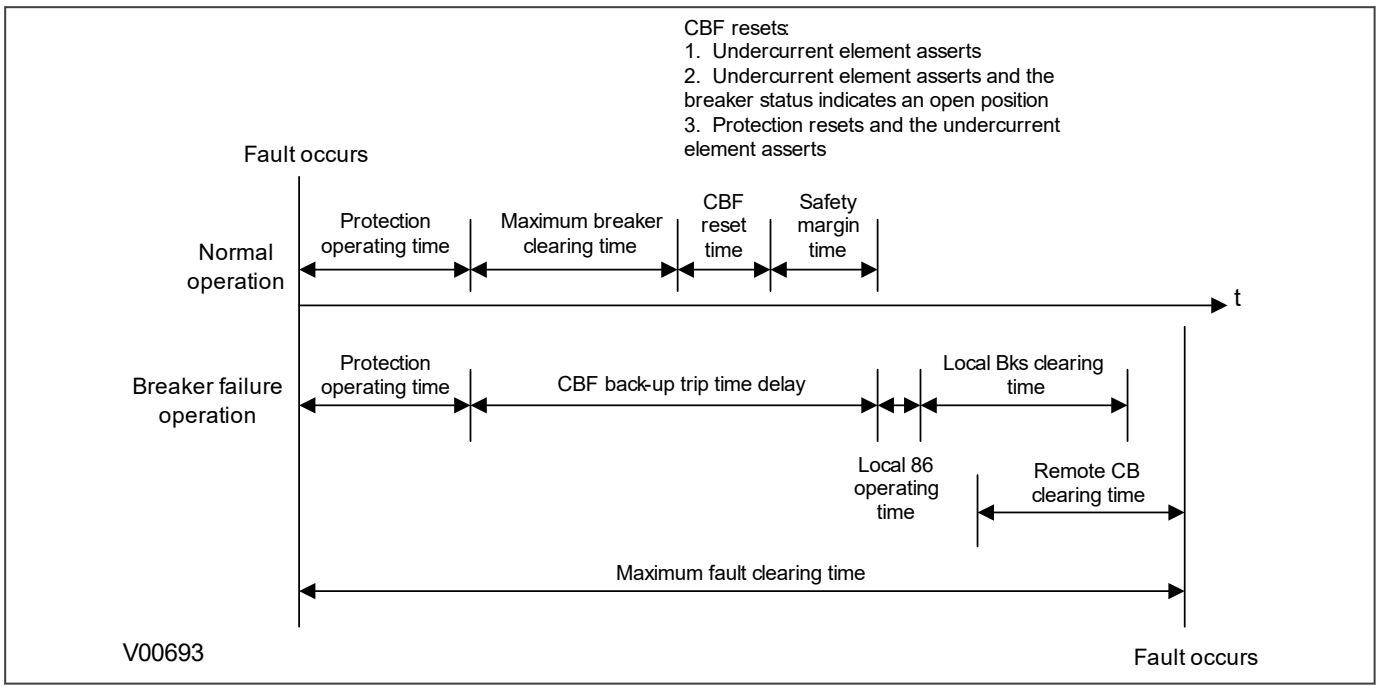


Figure 136: CB Fail timing

The following examples consider direct tripping of a 2-cycle circuit breaker. Typical timer settings to use are as follows:

CB Fail Reset Mechanism	tBF Time Delay	Typical Delay For 2 Cycle Circuit Breaker
Initiating element reset	CB interrupting time + element reset time (max.) + error in tBF timer + safety margin	50 + 50 + 10 + 50 = 160 ms
CB open	CB auxiliary contacts opening/ closing time (max.) + error in tBF timer + safety margin	50 + 10 + 50 = 110 ms
Undercurrent elements	CB interrupting time + undercurrent element (max.) + safety margin operating time	50 + 25 + 50 = 125 ms

Note:
All CB Fail resetting involves the operation of the undercurrent elements. Where element resetting or CB open resetting is used, the undercurrent time setting should still be used if this proves to be the worst case.
Where auxiliary tripping relays are used, an additional 10-15 ms must be added to allow for trip relay operation.

7.5.3 SETTING GUIDELINES (UNDERCURRENT)

The phase undercurrent settings (I<) must be set less than load current to ensure that I< operation correctly indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20%In. Settings of 5% of In are common for generator CB Fail.

The earth fault undercurrent elements must be set less than the respective trip. For example:

$$IN< = (IN> \text{ trip})/2$$

CHAPTER 8

CURRENT PROTECTION FUNCTIONS

8.1 CHAPTER OVERVIEW

The primary purpose of this product is not overcurrent protection. It does however provide a range of current protection functions to be used as backup protection. This chapter assumes you are familiar with overcurrent protection principles and does not provide detailed information here. If you require further information about general overcurrent protection principles, please refer either to GE Vernova's publication, Protection and Automation Application Guide, earlier incarnations of this technical manual, or one of our technical manuals from our P40 Agile Modular distribution range of products such as the P14.

This chapter contains the following sections:

8.2 PHASE FAULT OVERCURRENT PROTECTION

Phase fault overcurrent protection is provided as a form of back-up protection that could be:

- Permanently disabled
- Permanently enabled
- Enabled only in case of VT fuse/MCB failure
- Enabled only in case of protection communication channel failure
- Enabled if VT fuse/MCB or protection communication channel fail
- Enabled if VT fuse/MCB and protection communication channel fail

In addition, each stage may be inhibited/blocked by a DDB signal.

It should be noted that phase overcurrent protection is phase segregated, but the operation of any phase is mapped to 3 phase tripping in the default PSL.

The VTS element of the IED can be selected to either block the directional element or simply remove the directional control.

8.2.1 POC IMPLEMENTATION

Phase Overcurrent Protection is configured in the OVERCURRENT column of the relevant settings group.

The product provides four stages of three-phase overcurrent protection, each with independent time delay characteristics. The settings are independent for each stage, but for each stage, the settings apply to all phases.

Stages 1 and 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves based on IEC and IEEE standards
- A range of programmable user-defined curves
- DT (Definite Time) characteristic

This is achieved using the cells:

- ***I>(n) Function*** for the overcurrent operate characteristic
- ***I>(n) Reset Char*** for the overcurrent reset characteristic
- ***I>(n) Usr Rst Char*** for the reset characteristic for user-defined curves

where (n) is the number of the stage.

The IDMT-equipped stages, (1 and 2) also provide a Timer Hold facility. This is configured using the cells ***I>(n) tReset***, where (n) is the number of the stage. This does not apply to IEEE curves.

Stages 3 and 4 have definite time characteristics only.

8.2.2 DIRECTIONAL ELEMENT

If fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Once the direction has been determined the device can decide whether to allow tripping or to block tripping. To determine the direction of a phase overcurrent fault, the device must compare the phase angle of the fault current with that of a known reference quantity. The phase angle of this known reference quantity must be independent of the faulted phase. Typically this will be the line voltage between the other two phases.

The phase fault elements of the IEDs are internally polarized by the quadrature phase-phase voltages, as shown in the table below:

Phase of Protection	Operate Current	Polarising Voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

Under system fault conditions, the fault current vector lags its nominal phase voltage by an angle depending on the system X/R ratio. The IED must therefore operate with maximum sensitivity for currents lying in this region. This is achieved by using the IED characteristic angle (RCA). This is the is the angle by which the current applied to the IED must be displaced from the voltage applied to the IED to obtain maximum sensitivity.

The device provides a setting ***I> Char Angle***, which is set globally for all overcurrent stages. It is possible to set characteristic angles anywhere in the range –95° to +95°.

A directional check is performed based on the following criteria:

Directional forward

$$-90° < (\text{angle}(I) - \text{angle}(V) - RCA) < 90°$$

Directional reverse

$$-90° > (\text{angle}(I) - \text{angle}(V) - RCA) > 90°$$

For close up three-phase faults, all three voltages will collapse to zero and no healthy phase voltages will be present. For this reason, the device includes a synchronous polarisation feature that stores the pre-fault voltage information and continues to apply this to the directional overcurrent elements for a time period of 3.2 seconds. This ensures that either instantaneous or time-delayed directional overcurrent elements will be allowed to operate, even with a three-phase voltage collapse.

8.2.3 POC LOGIC

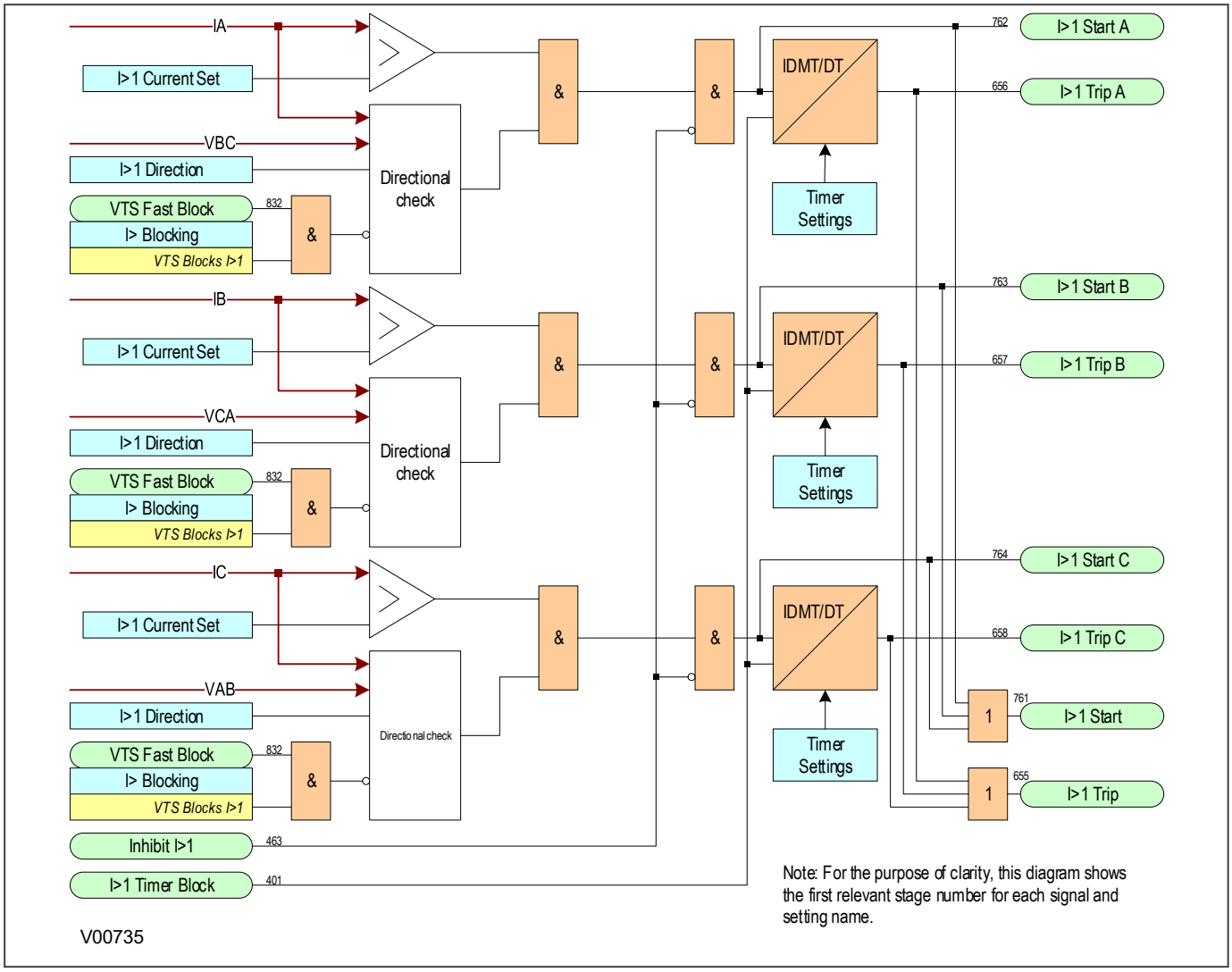


Figure 137: Phase Overcurrent Protection logic diagram

8.2.4 POC LOGIC

If there is a need to inhibit the overcurrent element during inrush condition, an additional logic as shown below can be created in PSL.

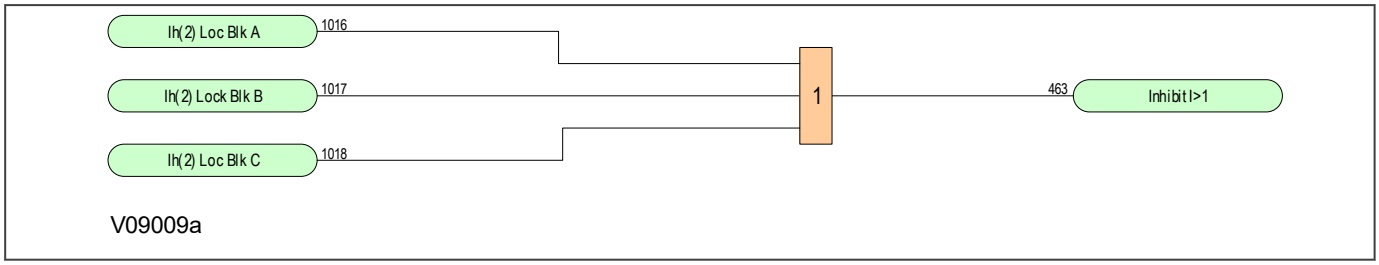


Figure 138: 2nd Harmonic block

The settable threshold for 2nd harmonic is available in Supervision/Inrush detection.

8.3 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

When applying standard phase overcurrent protection, the overcurrent elements must be set significantly higher than the maximum load current. This limits the element's sensitivity. Most protection schemes also use an earth fault element operating from residual current, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes. Negative Phase Sequence Overcurrent elements can help in such cases.

Any unbalanced fault condition will produce a negative sequence current component. Therefore, a negative phase sequence overcurrent element can be used for both phase-to-phase and phase-to-earth faults. Negative Phase Sequence Overcurrent protection offers the following advantages:

- Negative phase sequence overcurrent elements are more sensitive to resistive phase-to-phase faults, where phase overcurrent elements may not operate.
- In certain applications, residual current may not be detected by an earth fault element due to the system configuration. For example, an earth fault element applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side. However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore, a negative phase sequence overcurrent element may be used to provide time-delayed back-up protection for any uncleared asymmetrical faults downstream.

8.3.1 NEGATIVE SEQUENCE OVERCURRENT PROTECTION IMPLEMENTATION

Negative Sequence Overcurrent Protection is implemented in the *NEG SEQ O/C* column of the relevant settings group.

The product provides four stages of negative sequence overcurrent protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of standard IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells

- ***I2>(n) Function*** for the overcurrent operate characteristic
- ***I2>(n) Reset Char*** for the overcurrent reset characteristic

where (n) is the number of the stage.

The IDMT-capable stages, (1 and 2) also provide a Timer Hold. This is configured using the cells ***I2>(n) tReset***, where (n) is the number of the stage. This is not applicable for curves based on the IEEE standard.

Stages 3 and 4 have definite time characteristics only.

8.3.2 DIRECTIONAL ELEMENT

Where negative phase sequence current may flow in either direction, directional control should be used.

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current. A directional element is available for all of the negative sequence overcurrent stages. This is found in the ***I2> Direction*** cell for the relevant stage. It can be set to non-directional, directional forward, or directional reverse.

A suitable characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (**–V2**), in order to be at the centre of the directional characteristic.

8.3.3 NPSOC LOGIC

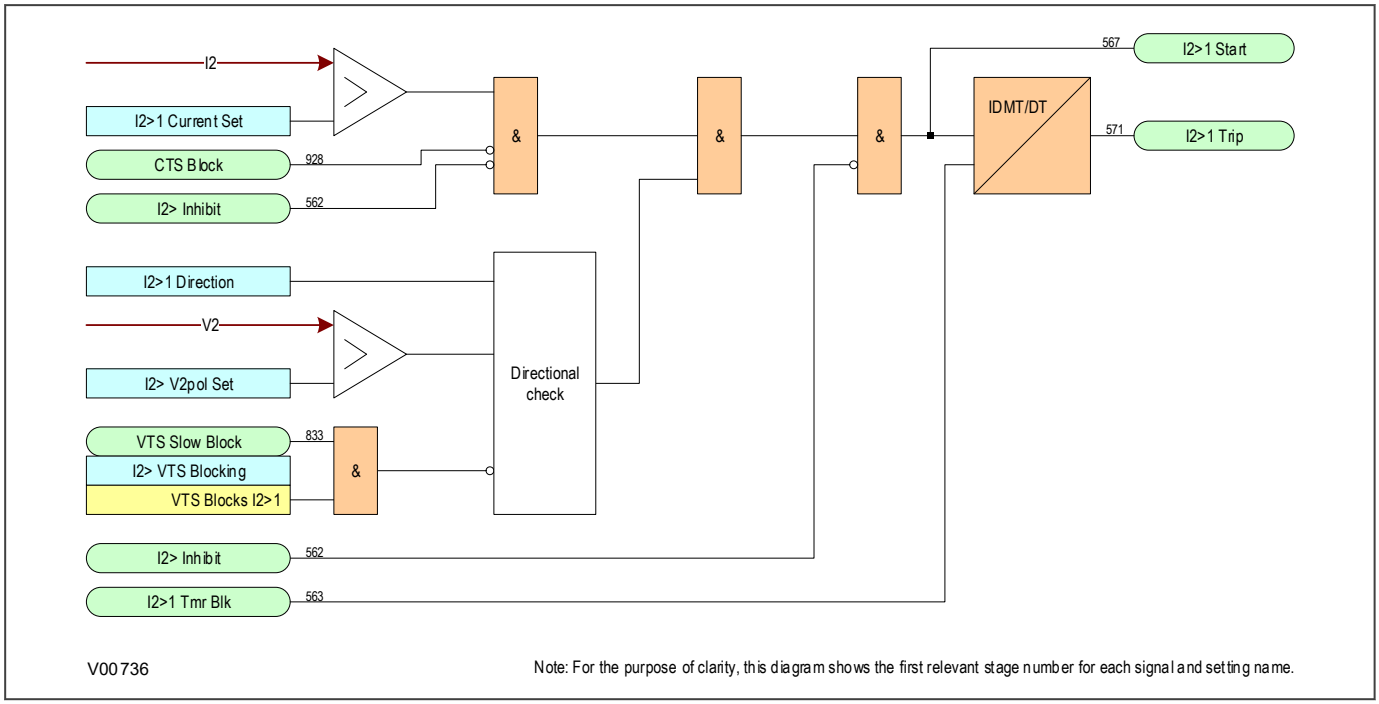


Figure 139: Negative Phase Sequence Overcurrent Protection logic diagram

8.3.4 APPLICATION NOTES

8.3.4.1 SETTING GUIDELINES (CURRENT THRESHOLD)

A negative phase sequence element can be connected in the primary supply to the transformer and set as sensitively as required to protect for secondary phase-to-earth or phase-to-phase faults. This function will also provide better protection than the phase overcurrent function for internal transformer faults. The NPS overcurrent protection should be set to coordinate with the low-side phase and earth elements for phase-to-earth and phase-to-phase faults.

The current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load imbalance. This can be set practically at the commissioning stage, making use of the measurement function to display the standing negative phase sequence current. The setting should be at least 20% above this figure.

Where the negative phase sequence element needs to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

8.3.4.2 SETTING GUIDELINES (TIME DELAY)

Correct setting of the time delay for this function is vital. You should also be very aware that this element is applied primarily to provide back-up protection to other protection devices or to provide an alarm. It would therefore normally have a long time delay.

The time delay set must be greater than the operating time of any other protection device (at minimum fault level) that may respond to unbalanced faults such as phase overcurrent elements and earth fault elements.

8.3.4.3 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

Where negative phase sequence current may flow in either direction through an IED location, such as parallel lines or ring main systems, directional control of the element should be employed (VT models only).

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the centre of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent on the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the relay characteristic angle (RCA) should be set equal to –60°
- For a distribution system the relay characteristic angle (RCA) should be set equal to –45°

For the negative phase sequence directional elements to operate, the device must detect a polarising voltage above a minimum threshold, ***I2> V2pol Set***. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the device.

8.4 EARTH FAULT PROTECTION

Earth faults are overcurrent faults where the fault current flows to earth. Earth faults are the most common type of fault.

Earth faults can be measured directly from the system by means of:

- A separate current Transformer (CT) located in a power system earth connection
- A separate Core Balance Current Transformer (CBCT), usually connected to the SEF transformer input
- A residual connection of the three line CTs, where the Earth faults can be derived mathematically by summing the three measured phase currents

Depending on the device model, it will provide one or more of the above means for Earth fault protection.

8.4.1 EARTH FAULT PROTECTION IMPLEMENTATION

Earth fault protection is implemented in the *EARTH FAULT* column of the relevant settings group. The element uses quantities derived internally from summing the three-phase currents.

The product provides four stages of Earth Fault protection with independent time delay characteristics, for each *EARTH FAULT* column.

Stages 1 and 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells:

- ***IN>(n) Function*** for the overcurrent operate characteristics
- ***IN>(n) Reset Char*** for the overcurrent reset characteristic

where (n) is the number of the stage.

Stages 1 and 2 provide a Timer Hold facility. This is configured using the cells ***IN>(n) tReset***

Stages 3 and 4 can have definite time characteristics only.

Earth fault Overcurrent IN> can be set to:

- Permanently disabled
- Permanently enabled
- Enabled only if VT fuse/MCB fails
- Enabled only if protection communication channel fails
- Enabled if VT fuse/MCB or protection communication channel fail
- Enabled if VT fuse/MCB and protection communication channel fail

Each stage can be individually inhibited with a DDB signal ***Inhibit IN>(n)***, where n is the stage number.

8.4.2 IDG CURVE

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stage 1 of the Earth Fault protection.

The IDG curve is represented by the following equation:

$$t_{op} = 5.8 - 1.35 log_e \left(\frac{I}{IN > Setting} \right)$$

where:

t_{op} is the operating time

I is the measured current

IN> Setting is an adjustable setting, which defines the start point of the characteristic

Note:
Although the start point of the characteristic is defined by the "IN>" setting, the actual current threshold is a different setting called "IDG Is". The "IDG Is" setting is set as a multiple of "IN>".

Note:
When using an IDG Operate characteristic, DT is always used with a value of zero for the Rest characteristic.

An additional setting "IDG Time" is also used to set the minimum operating time at high levels of fault current.

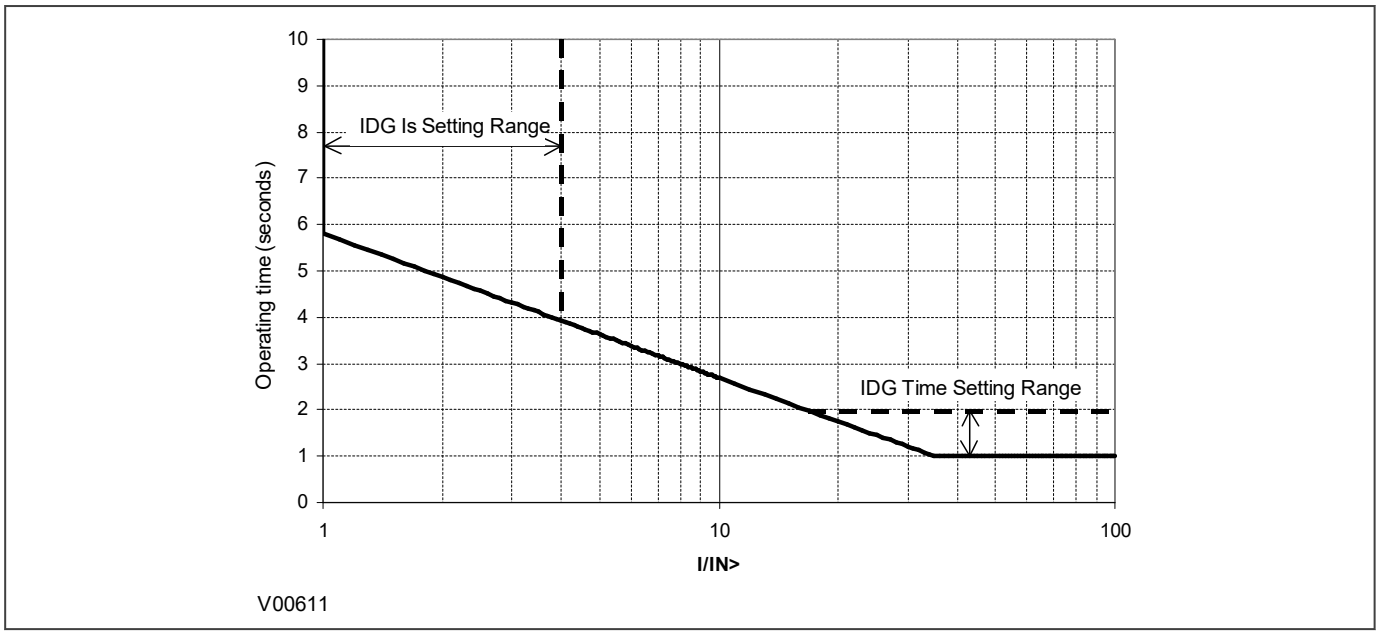


Figure 140: IDG Characteristic

8.4.3 DIRECTIONAL ELEMENT

If Earth fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Typical systems that require such protection are parallel feeders and ring main systems.

A directional element is available for all of the Earth Fault stages. These are found in the direction setting cells for the relevant stage. They can be set to non-directional, directional forward, or directional reverse.

Directional control can be blocked by the VTS element if required.

For standard earth fault protection, two options are available for polarisation; Residual Voltage (zero sequence) or Negative Sequence.

8.4.3.1 RESIDUAL VOLTAGE POLARISATION

With earth fault protection, the polarising signal needs to be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarise directional earth fault

elements. This is known as Zero Sequence Voltage polarisation, Residual Voltage polarisation or Neutral Displacement Voltage (NVD) polarisation.

Small levels of residual voltage could be present under normal system conditions due to system imbalances, VT inaccuracies, device tolerances etc. For this reason, the device includes a user settable threshold (***IN> VNPol set***), which must be exceeded in order for the DEF function to become operational. The residual voltage measurement provided in the *MEASUREMENTS 1* column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

Note:
Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarised from the "-Vres" quantity. This 180° phase shift is automatically introduced within the device.

The directional criteria with residual voltage polarisation is given below:

- Directional forward: -90° < (angle(IN) - angle(VN + 180°) - RCA) < 90°
- Directional reverse : -90° > (angle(IN) - angle(VN + 180°) - RCA) > 90°

8.4.3.2 NEGATIVE SEQUENCE POLARISATION

In some applications, the use of residual voltage polarisation may not be possible to achieve or it can be problematic. For example, a suitable type of VT may be unavailable, or an HV/EHV parallel line application may present problems with zero sequence mutual coupling.

In such situations, the problem may be solved by using Negative Phase Sequence (NPS) quantities for polarisation. This method determines the fault direction by comparing the NPS voltage with the NPS current. The operating quantity, however, is still residual current.

This can be used for both the derived and measured standard earth fault elements. It requires a suitable voltage and current threshold to be set in cells ***IN> V2pol set*** and ***IN> I2pol set*** respectively.

Negative phase sequence polarising is not recommended for impedance earthed systems regardless of the type of VT feeding the relay. This is due to the reduced earth fault current limiting the voltage drop across the negative sequence source impedance to negligible levels. If this voltage is less than 0.5 volts the device will stop providing directionalisation.

The directional criteria with negative sequence polarisation is given below:

- Directional forward: -90° < (angle(I2) - angle(V2 + 180°) - RCA) < 90°
- Directional reverse : -90° > (angle(I2) - angle(V2 + 180°) - RCA) > 90°

8.4.4 EARTH FAULT PROTECTION LOGIC

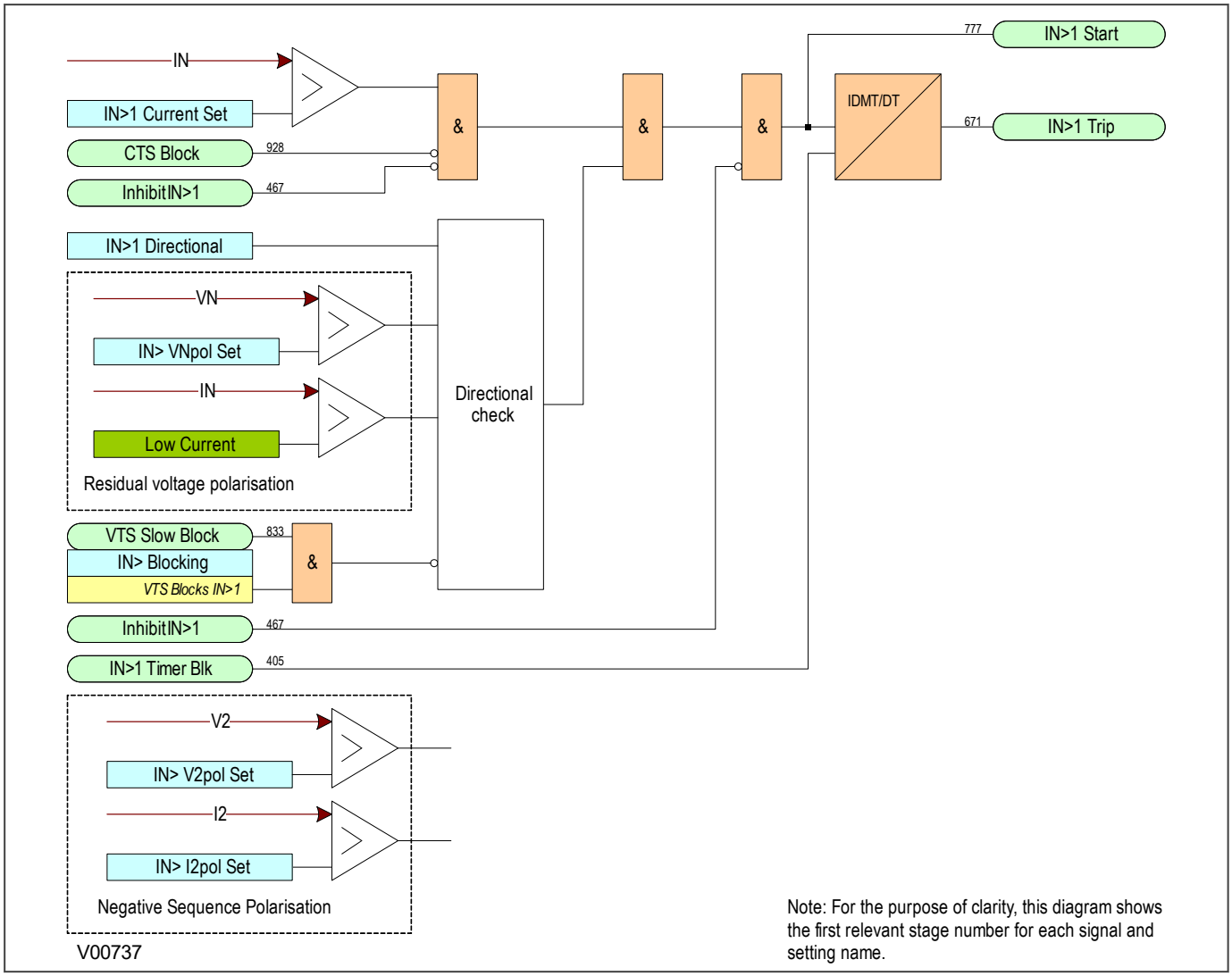


Figure 141: Earth Fault Protection logic diagram

8.4.5 APPLICATION NOTES

8.4.5.1 RESIDUAL VOLTAGE POLARISATION SETTING GUIDELINES

It is possible that small levels of residual voltage will be present under normal system conditions due to system imbalances, VT inaccuracies, IED tolerances etc. Hence, the IED includes a user settable threshold (***IN> VNPol Set***) which must be exceeded in order for the DEF function to be operational. In practice, the typical zero sequence voltage on a healthy system can be as high as 1% (i.e. 3% residual), and the VT error could be 1% per phase. A setting between 1% and 4% is therefore typical. The residual voltage measurement may assist in determining the required threshold setting during commissioning, as this will indicate the level of standing residual voltage present.

8.4.5.2 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

With directional earth faults, the residual current under fault conditions lies at an angle lagging the polarising voltage. Hence, negative RCA settings are required for DEF applications. This is set in the cell ***I> Char Angle*** in the relevant earth fault menu.

We recommend the following RCA settings:

- Resistance earthed systems: 0°
- Distribution systems (solidly earthed): -45°
- Transmission systems (solidly earthed): -60°

8.5 SENSITIVE EARTH FAULT PROTECTION

With some earth faults, the fault current flowing to earth is limited by either intentional resistance (as is the case with some HV systems) or unintentional resistance (e.g. in very dry conditions and where the substrate is high resistance, such as sand or rock).

To provide protection in such cases, it is necessary to provide an earth fault protection system with a setting that is considerably lower than for normal line protection. Such sensitivity cannot be provided with conventional CTs, therefore the SEF input would normally be fed from a core balance current transformer (CBCT) mounted around the three phases of the feeder cable. The SEF transformer should be a special measurement class transformer.

8.5.1 SEF PROTECTION IMPLEMENTATION

The product provides four stages of SEF protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells

- ***ISEF>(n) Function*** for the overcurrent operate characteristic
- ***ISEF>(n) Reset Chr*** for the overcurrent reset characteristic

where (n) is the number of the stage.

Stages 1 and 2 also provide a Timer Hold facility. This is configured using the cells ***ISEF>(n) tReset***.

Stages 3 and 4 have definite time characteristics only.

Each stage can be individually inhibited with a DDB signal Inhibit ISEF>(n), where n is the stage number.

8.5.2 EPATR B CURVE

The EPATR B curve is commonly used for time-delayed Sensitive Earth Fault protection in certain markets. This curve is only available in the Sensitive Earth Fault protection stages 1 and 2. It is based on primary current settings, employing a SEF CT ratio of 100:1 A.

The EPATR_B curve has 3 separate segments defined in terms of the primary current. It is defined as follows:

Segment	Primary Current Range Based on 100A:1A CT Ratio	Current/Time Characteristic
1	ISEF = 0.5A to 6.0A	t = 432 x TMS/ISEF 0.655 secs
2	ISEF = 6.0A to 200A	t = 800 x TMS/ISEF secs
3	ISEF above 200A	t = 4 x TMS secs

where TMS (time multiplier setting) is 0.025 - 1.2 in steps of 0.025.

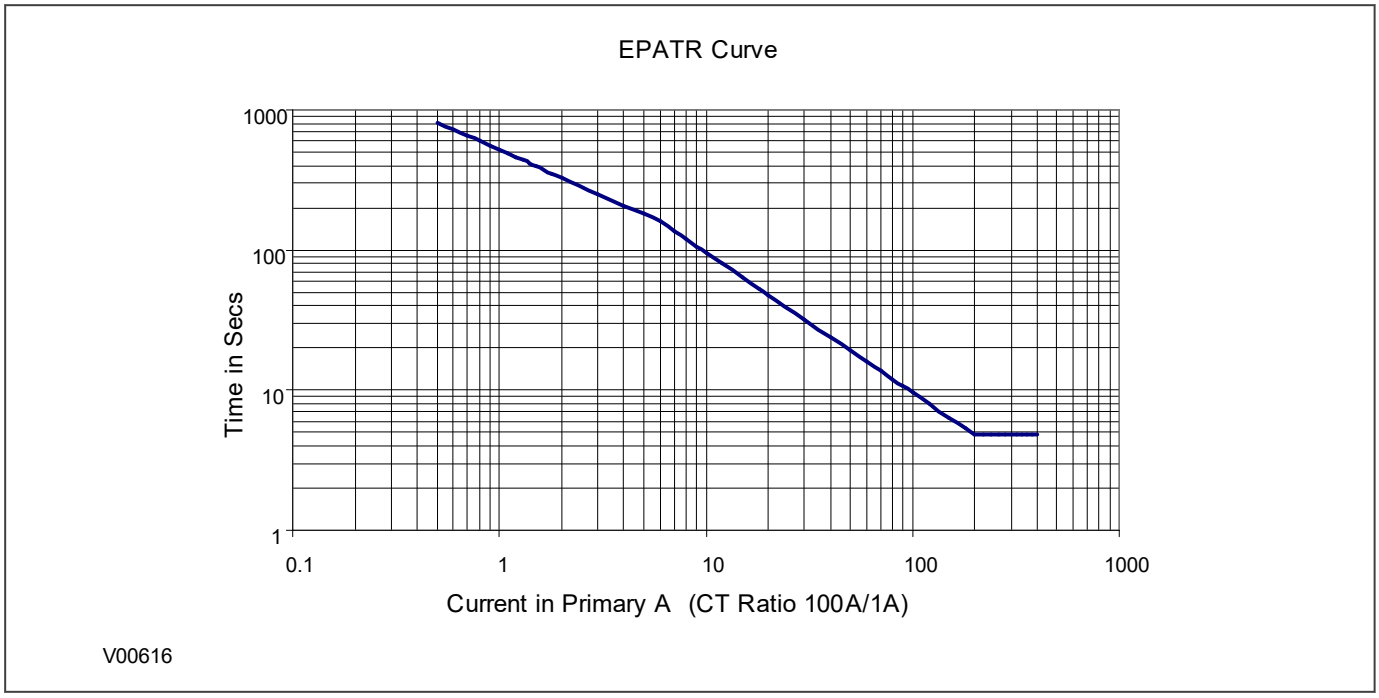


Figure 142: EPATR B characteristic shown for TMS = 1.0

8.5.3 SENSITIVE EARTH FAULT PROTECTION LOGIC

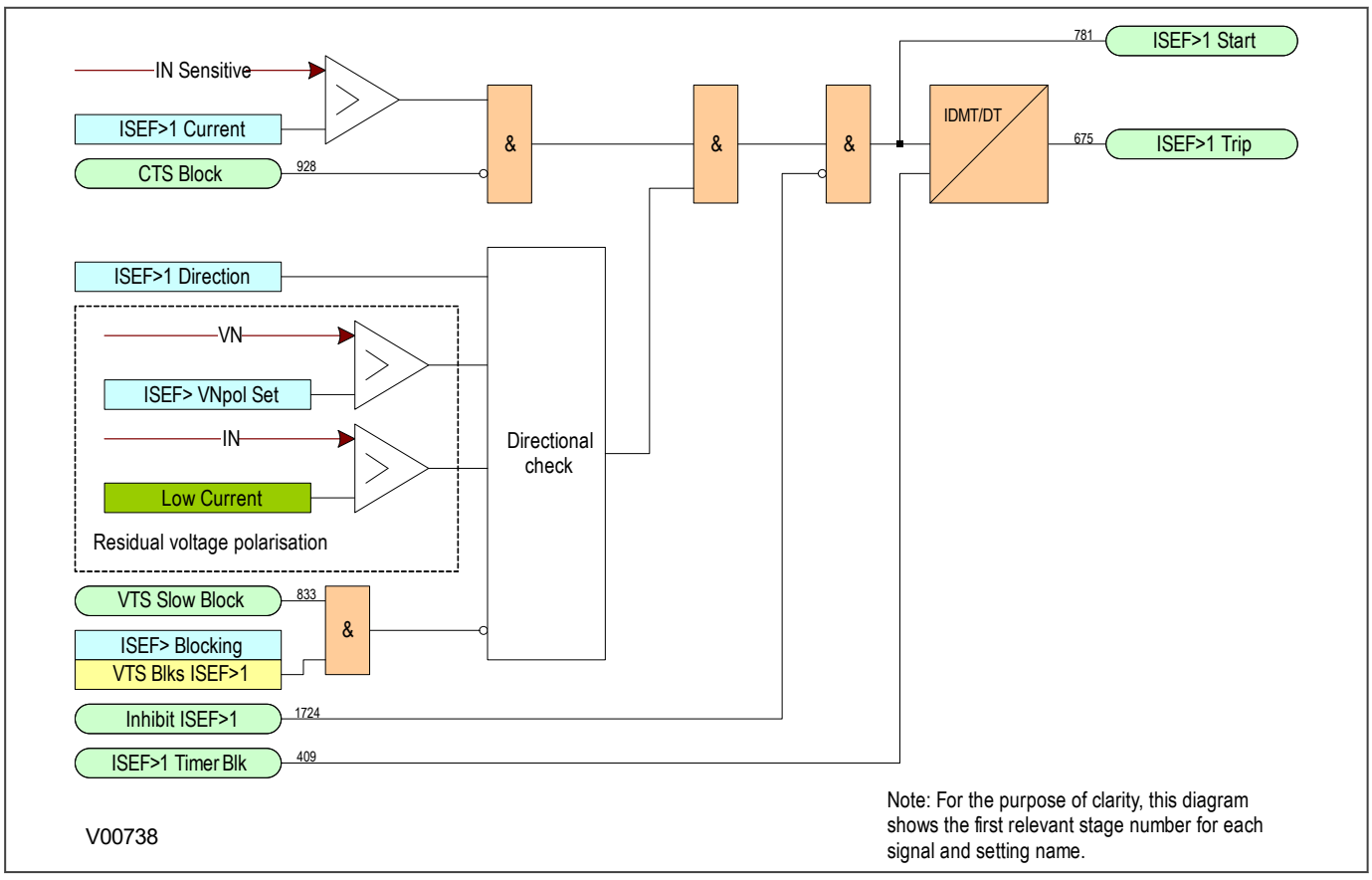


Figure 143: Sensitive Earth Fault Protection logic diagram

8.5.4 APPLICATION NOTES

8.5.4.1 INSULATED SYSTEMS

When insulated systems are used, it is not possible to detect faults using standard earth fault protection. It is possible to use a residual overvoltage device to achieve this, but even with this method full discrimination is not possible. Fully discriminative earth fault protection on this type of system can only be achieved by using a SEF (Sensitive Earth Fault) element. This type of protection detects the resultant imbalance in the system charging currents that occurs under earth fault conditions. A core balanced CT must be used for this application. This eliminates the possibility of spill current that may arise from slight mismatches between residually connected line CTs. It also enables a much lower CT ratio to be applied, thereby allowing the required protection sensitivity to be more easily achieved.

The following diagram shows an insulated system with a C-phase fault.

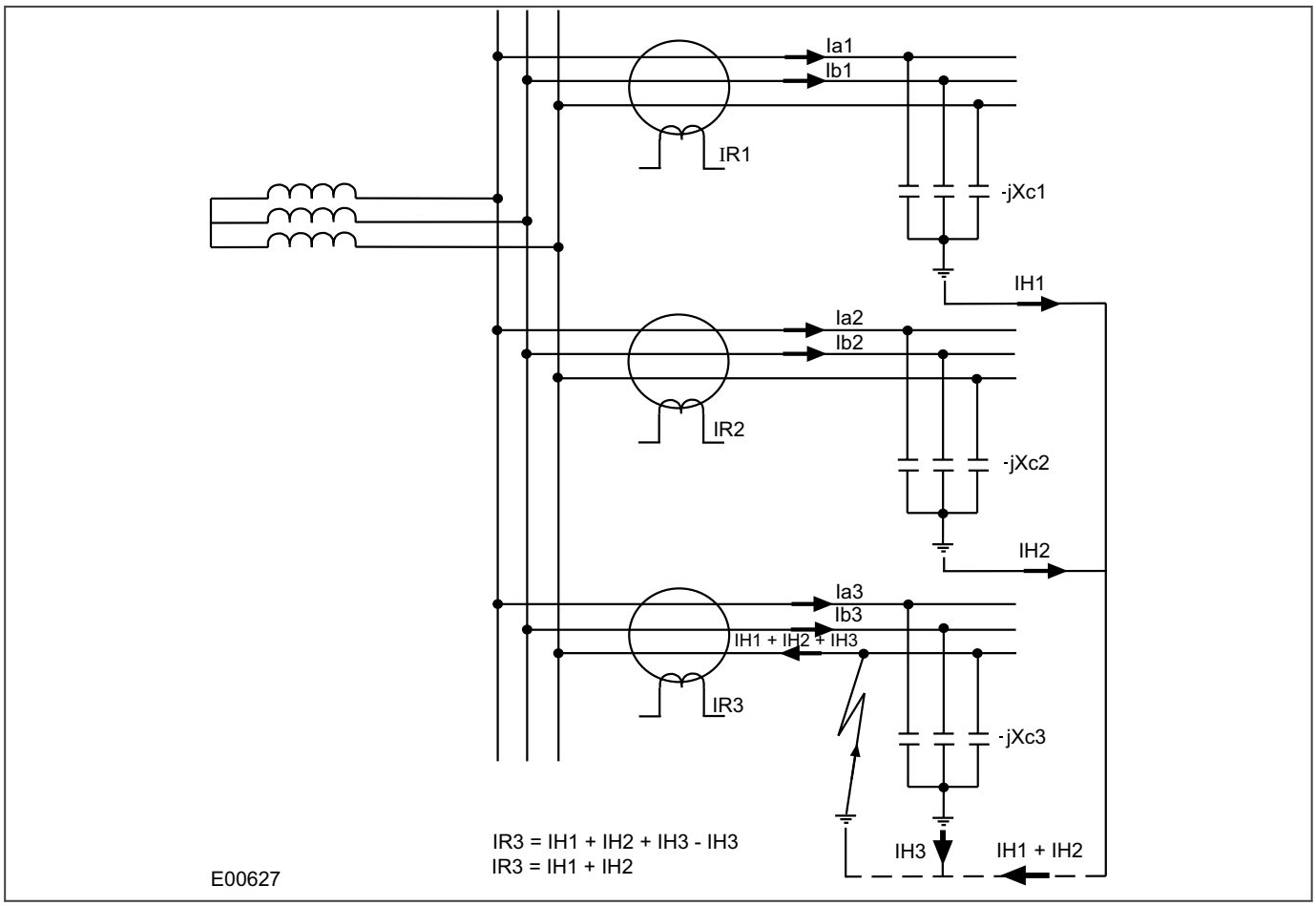


Figure 144: Current distribution in an insulated system with C phase fault

The protection elements on the healthy feeder see the charging current imbalance for their own feeder. The protection element on the faulted feeder, however, sees the charging current from the rest of the system (IH1 and IH2 in this case). Its own feeder's charging current (IH3) is cancelled out.

With reference to the associated vector diagram, it can be seen that the C-phase to earth fault causes the voltages on the healthy phases to rise by a factor of √3. The A-phase charging current (Ia1), leads the resultant A phase voltage by 90°. Likewise, the B-phase charging current leads the resultant Vb by 90°.

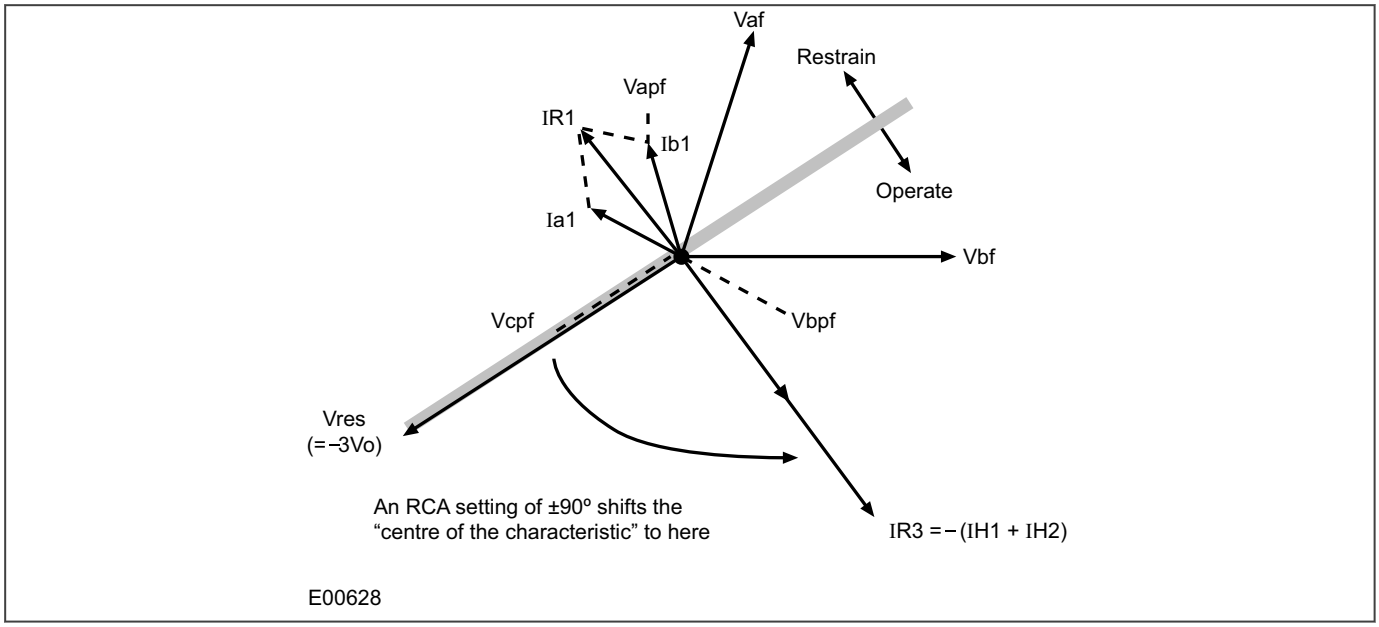


Figure 145: Phasor diagrams for insulated system with C phase fault

The current imbalance detected by a core balanced current transformer on the healthy feeders is the vector addition of Ia1 and Ib1. This gives a residual current which lags the polarising voltage (–3Vo) by 90°. As the healthy phase voltages have risen by a factor of √3, the charging currents on these phases are also √3 times larger than their steady state values. Therefore, the magnitude of the residual current IR1, is equal to 3 times the steady state per phase charging current.

The phasor diagram indicates that the residual currents on the healthy and faulted feeders (IR1 and IR3 respectively) are in anti-phase. A directional element (if available) could therefore be used to provide discriminative earth fault protection.

If the polarising is shifted through +90°, the residual current seen by the relay on the faulted feeder will lie within the operate region of the directional characteristic and the current on the healthy feeders will fall within the restrain region.

The required characteristic angle setting for the SEF element when applied to insulated systems, is +90°. This is for the case when the protection is connected such that its direction of current flow for operation is from the source busbar towards the feeder. If the forward direction for operation were set such that it is from the feeder into the busbar, then a –90° RCA would be required.

Note:
Discrimination can be provided without the need for directional control. This can only be achieved, however, if it is possible to set the IED in excess of the charging current of the protected feeder and below the charging current for the rest of the system.

8.5.4.2 SETTING GUIDELINES (INSULATED SYSTEMS)

The residual current on the faulted feeder is equal to the sum of the charging currents flowing from the rest of the system. Further, the addition of the two healthy phase charging currents on each feeder gives a total charging current which has a magnitude of three times the per phase value. Therefore, the total imbalance current is equal to three times the per phase charging current of the rest of the system. A typical setting may therefore be in the order of 30% of this value, i.e. equal to the per phase charging current of the remaining system. Practically though, the required setting may well be determined on site, where suitable settings can be adopted based on practically obtained results.

When using a core-balanced transformer, care must be taken in the positioning of the CT with respect to the earthing of the cable sheath:

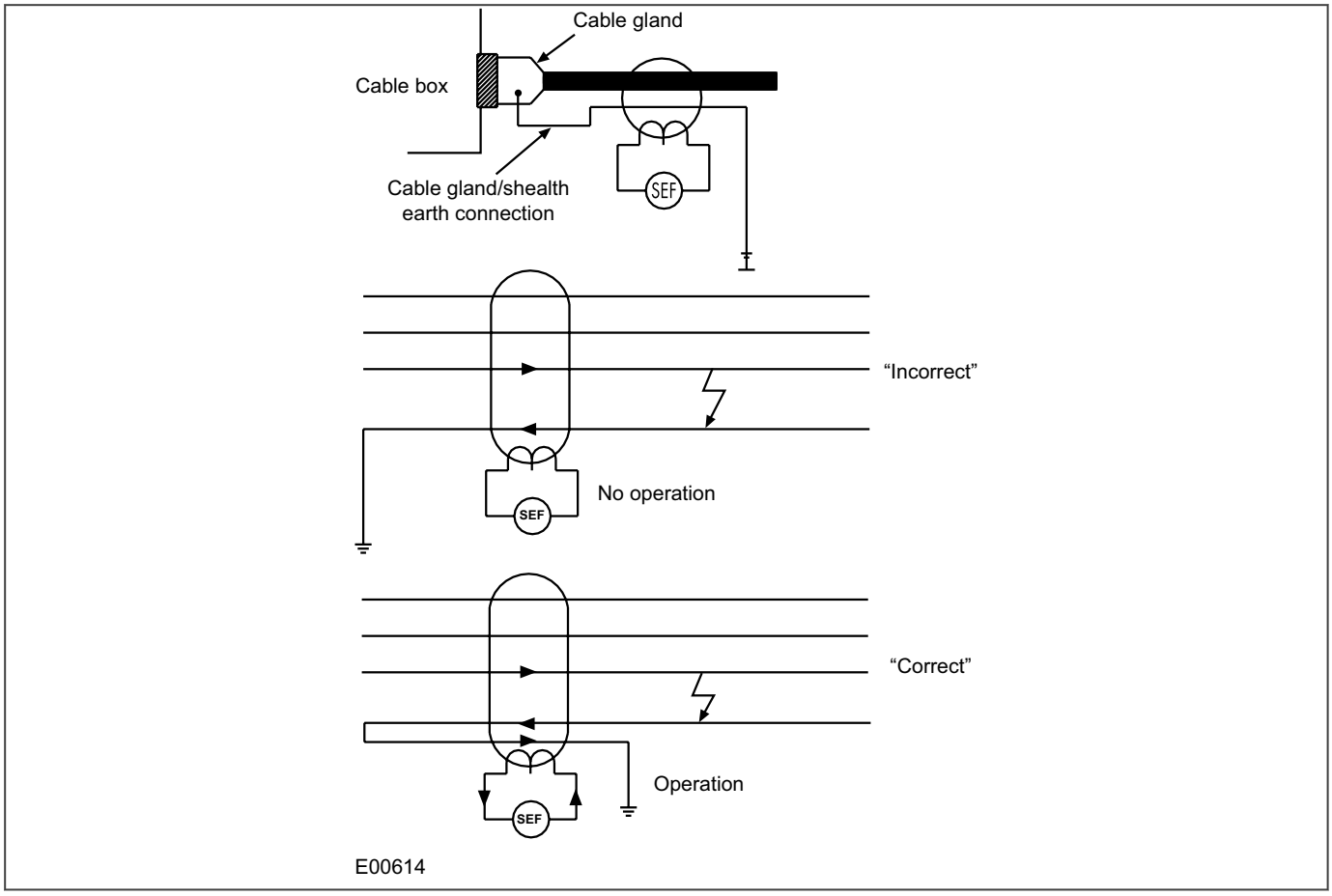


Figure 146: Positioning of core balance current transformers

If the cable sheath is terminated at the cable gland and directly earthed at that point, a cable fault (from phase to sheath) will not result in any unbalanced current in the core balance CT. Therefore, prior to earthing, the connection must be brought back through the CBCT and earthed on the feeder side. This then ensures correct relay operation during earth fault conditions.

8.6 HIGH IMPEDANCE REF

The device provides a high impedance restricted earth fault protection function. An external resistor is required to provide stability in the presence of saturated line current transformers. Current transformer supervision signals do not block the high impedance REF protection. The appropriate logic must be configured in PSL to block the high impedance REF when any of the above signals is asserted.

8.6.1 HIGH IMPEDANCE REF PRINCIPLE

This scheme is very sensitive and can protect against low levels of fault current, typical of winding faults.

High Impedance REF protection is based on the differential principle. It works on the circulating current principle as shown in the following diagram.

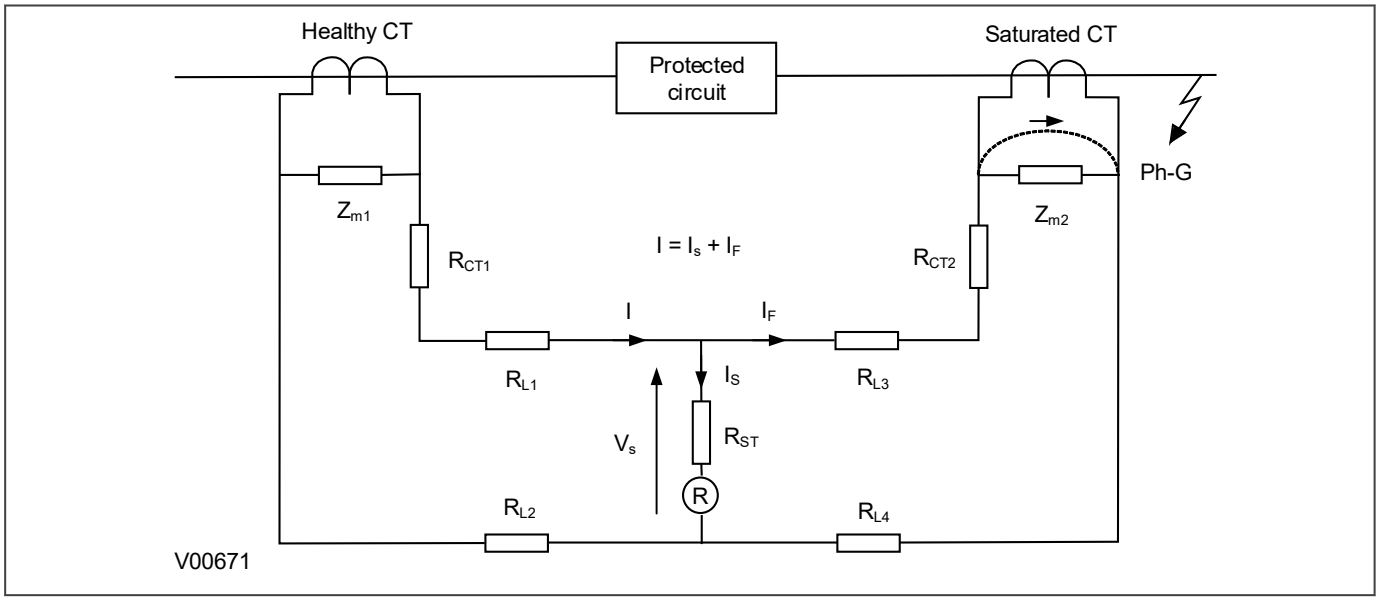


Figure 147: High impedance REF principle

When subjected to heavy through faults the line current transformer may enter saturation unevenly, resulting in imbalance. To ensure stability under these conditions a series connected external resistor is required, so that most of the unbalanced current will flow through the saturated CT. As a result, the current flowing through the device will be less than the setting, therefore maintaining stability during external faults.

Voltage across REF element $V_s = I_F (R_{CT2} + R_{L3} + R_{L4})$

Stabilising resistor $R_{ST} = V_s/I_s - R_R$

where:

- I_F = maximum secondary through fault current
- R_R = device burden
- R_{CT} = CT secondary winding resistance
- R_{L2} and R_{L3} = Resistances of leads from the device to the current transformer
- R_{ST} = Stabilising resistor

High Impedance REF can be used for either delta windings or star windings in both solidly grounded and resistance grounded systems. The connection to a modern IED are as follows:

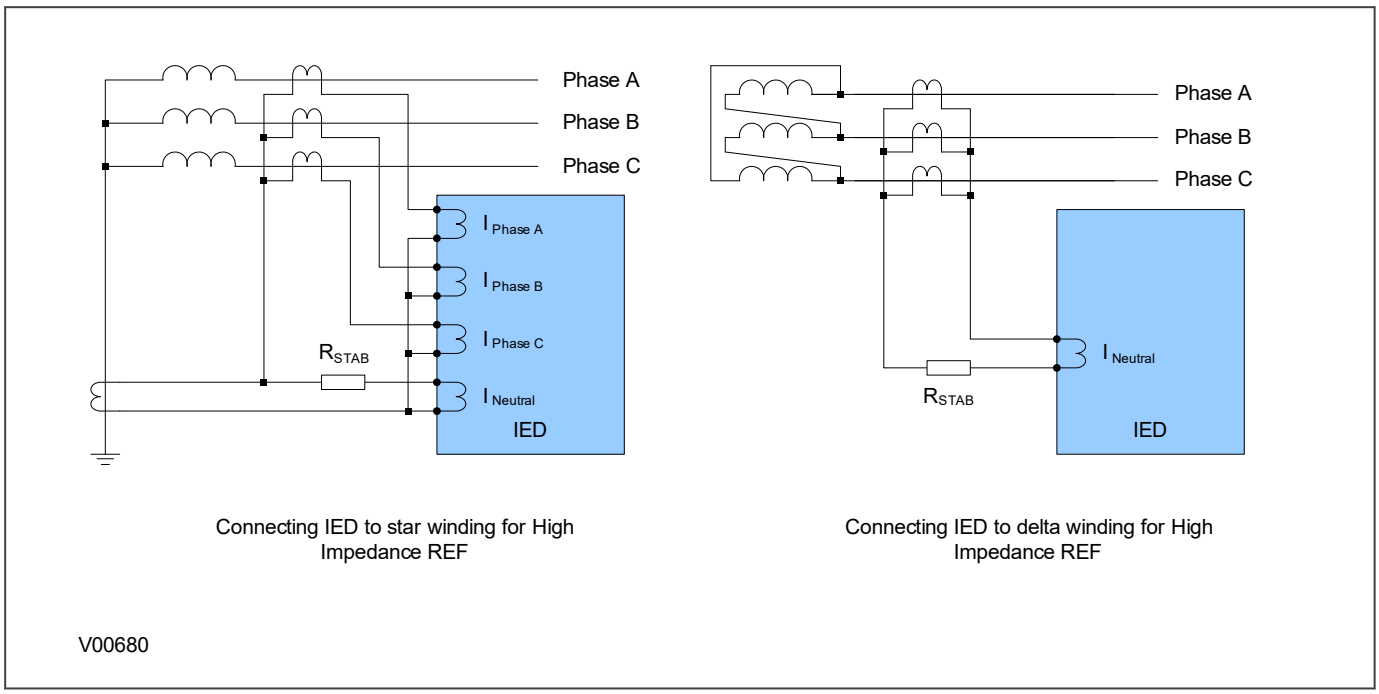


Figure 148: High impedance REF connection

8.7 THERMAL OVERLOAD PROTECTION

The heat generated within an item of plant is the resistive loss. The thermal time characteristic is therefore based on the equation I^2Rt. Over-temperature conditions occur when currents in excess of their maximum rating are allowed to flow for a period of time.

Temperature changes during heating follow exponential time constants. The device provides two characteristics for thermal overload protection; a single time constant characteristic and a dual time constant characteristic. You select these according to the application.

8.7.1 SINGLE TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect cables, dry type transformers and capacitor banks.

The single constant thermal characteristic is given by the equation:

$$t = -\tau \log_e \left[\frac{I^2 - \left(KI_{FLC}\right)^2}{I^2 - I_p{}^2} \right]$$

where:

- t = time to trip, following application of the overload current I
- τ = heating and cooling time constant of the protected plant
- I = largest phase current
- I_{FLC} full load current rating (the Thermal Trip setting)
- K = a constant with the value of 1.05
- I_p = steady state pre-loading before application of the overload

8.7.2 DUAL TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect equipment such as oil-filled transformers with natural air cooling. The thermal model is similar to that with the single time constant, except that two timer constants must be set.

For marginal overloading, heat will flow from the windings into the bulk of the insulating oil. Therefore, at low current, the replica curve is dominated by the long time constant for the oil. This provides protection against a general rise in oil temperature.

For severe overloading, heat accumulates in the transformer windings, with little opportunity for dissipation into the surrounding insulating oil. Therefore at high current levels, the replica curve is dominated by the short time constant for the windings. This provides protection against hot spots developing within the transformer windings.

Overall, the dual time constant characteristic serves to protect the winding insulation from ageing and to minimise gas production by overheated oil. Note however that the thermal model does not compensate for the effects of ambient temperature change.

The dual time constant thermal characteristic is given by the equation:

$$0.4e^{(-t/\tau_1)} + 0.6e^{(-t/\tau_2)} = \left[\frac{I^2 - \left(KI_{FLC}\right)^2}{I^2 - I_p{}^2} \right]$$

where:

- τ_1 = heating and cooling time constant of the transformer windings
- τ_2 = heating and cooling time constant of the insulating oil

8.7.3 THERMAL OVERLOAD PROTECTION IMPLEMENTATION

The device incorporates a current-based thermal characteristic, using Fourier based load current to model heating and cooling of the protected plant. The element can be set with both alarm and trip stages.

Thermal Overload Protection is implemented in the *THERMAL OVERLOAD* column of the relevant settings group.

This column contains the settings for the characteristic type, the alarm and trip thresholds and the time constants.

8.7.4 THERMAL OVERLOAD PROTECTION LOGIC

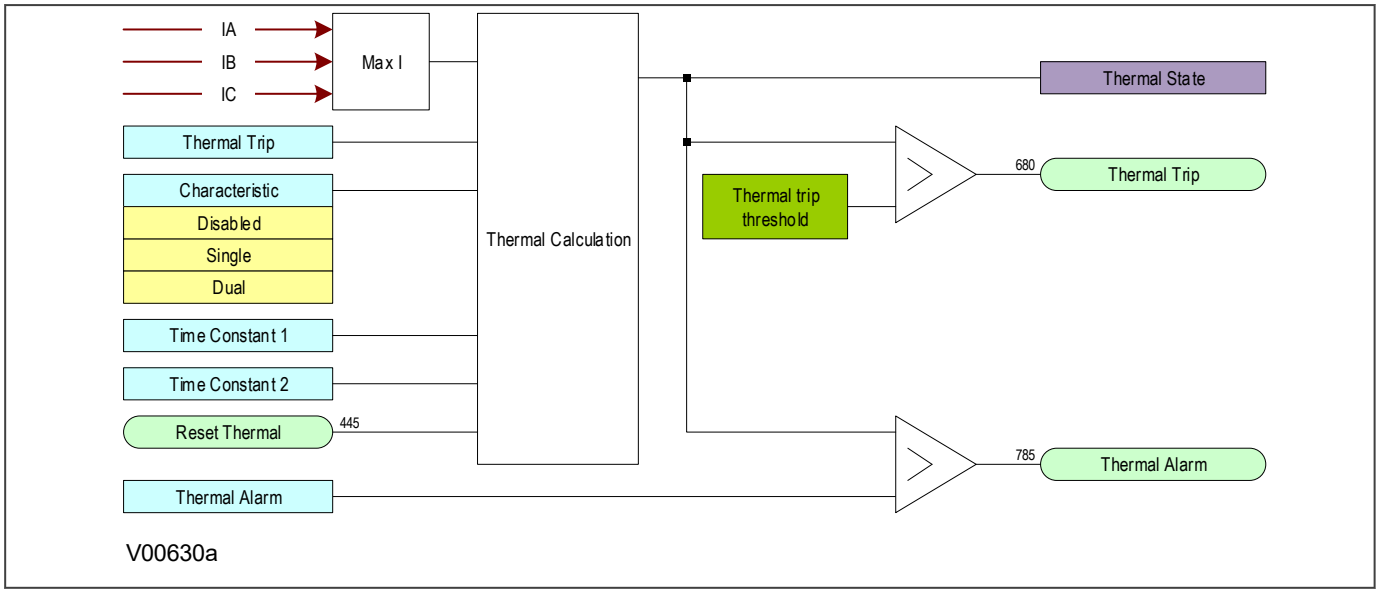


Figure 149: Thermal overload protection logic diagram

The magnitudes of the three phase input currents are compared and the largest magnitude is taken as the input to the thermal overload function. If this current exceeds the thermal trip threshold setting a start condition is asserted.

The Start signal is applied to the chosen thermal characteristic module, which has three outputs signals; alarm trip and thermal state measurement. The thermal state measurement is made available in one of the *MEASUREMENTS* columns.

The thermal state can be reset by either a digital signal (Opto, GOOSE, InterMiCOM), if assigned to this function using programmable scheme logic or the HMI panel menu.

8.7.5 APPLICATION NOTES

8.7.5.1 SETTING GUIDELINES FOR DUAL TIME CONSTANT CHARACTERISTIC

The easiest way of solving the dual time constant thermal equation is to express the current in terms of time and to use a spreadsheet to calculate the current for a series of increasing operating times using the following equation, then plotting a graph.

$$I = \sqrt{\frac{0.4I_p^{\,2}.e^{(-t/\tau 1)} + 0.6I_p^{\,2}.e^{(-t/\tau 2)} - k^2.I_{FLC}^{\,2}}{0.4e^{(-t/\tau 1)} + 0.6e^{(-t/\tau 2)} - 1}}$$

	A	B	C	D	E	F
1						
2	**Time constant 1 =**		**300**	seconds		
3	**Time constant 2 =**		**7200**	seconds		
4	**Pre-overload current Ip =**		**0.9**	per unit		
5	**Full load current =**		**1**	Amps		
6						
7	**OP Time (t)**	**Overload current (I)**				
8	1	14.40852032				
9	1.5	11.7805774				
10	2	10.21617905				
11	2.5	9.150045407				
12	3	8.364131776				
13	3.5	7.754150044				
14	4	7.263123888				
15	4.5	6.856949012				

Figures based on equation

E00728

Figure 150: Spreadsheet calculation for dual time constant thermal characteristic

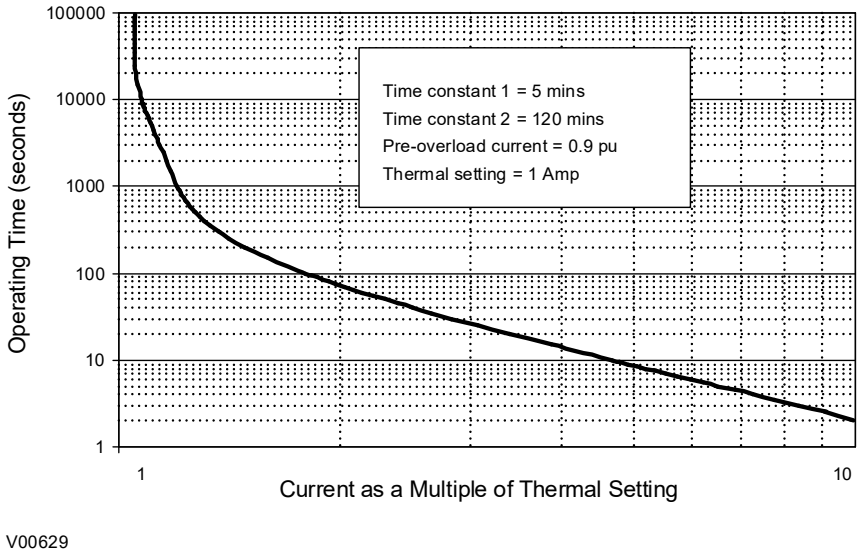


Figure 151: Dual time constant thermal characteristic

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the transformer item/CT ratio.

For an oil-filled transformer with rating 400 to 1600 kVA, the approximate time constants are:

- τ_1 = 5 minutes
- τ_2 = 120 minutes

An alarm can be raised on reaching a thermal state corresponding to a percentage of the trip threshold. A typical setting might be "Thermal Alarm" = 70% of thermal capacity.

Note:
The thermal time constants given in the above tables are typical only. Reference should always be made to the plant manufacturer for accurate information.

8.7.5.2 SETTING GUIDELINES FOR SINGLE TIME CONSTANT CHARACTERISTIC

The time to trip varies depending on the load current carried before application of the overload, i.e. whether the overload was applied from hot or cold.

The thermal time constant characteristic may be rewritten as:

$$e^{(-t/\tau)} = {}_{e}\left[\frac{\theta - \theta_p}{\theta - 1}\right]$$

where:

- θ = thermal state = $I^2/K^2I_{FLC}^2$
- θ_p = pre-fault thermal state = $I_p^2/K^2I_{FLC}^2$
- I_p is the pre-fault thermal state
- I_{FLC} is the full load current

Note:
A current of 105%Is (KI_{FLC}) has to be applied for several time constants to cause a thermal state measurement of 100%.

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the plant item/CT ratio.

The following tables show the approximate time constant in minutes, for different cable rated voltages with various conductor cross-sectional areas, and other plant equipment.

Area mm^2	6 - 11 kV	22 kV	33 kV	66 kV
25 - 50	10 minutes	15 minutes	40 minutes	–
70 - 120	15 minutes	25 minutes	40 minutes	60 minutes
150	25 minutes	40 minutes	40 minutes	60 minutes
185	25 minutes	40 minutes	60 minutes	60 minutes
240	40 minutes	40 minutes	60 minutes	60 minutes
300	40 minutes	60 minutes	60 minutes	90 minutes

Plant Type	Time Constant (Minutes)
Dry-type transformer <400 kVA	40
Dry-type transformers 400 – 800 kVA	60 - 90
Air-core reactors	40
Capacitor banks	10
Overhead lines with cross section > 100 mm^2	10
Overhead lines	10
Busbars	60

8.8 BROKEN CONDUCTOR PROTECTION

One type of unbalanced fault is the 'Series' or 'Open Circuit' fault. This type of fault can arise from, among other things, broken conductors. Series faults do not cause an increase in phase current and so cannot be detected by overcurrent protection. However, they do produce an imbalance, resulting in negative phase sequence current, which can be detected.

It is possible to apply a negative phase sequence overcurrent element to detect broken conductors. However, on a lightly loaded line, the negative sequence current resulting from a series fault condition may be very close to, or less than, the full load steady state imbalance arising from CT errors and load imbalances, making it very difficult to distinguish. A regular negative sequence element would therefore not work at low load levels. To overcome this, the device incorporates a special Broken Conductor protection element.

The Broken Conductor element measures the ratio of negative to positive phase sequence current (I2/I1). This ratio is approximately constant with variations in load current, therefore making it more sensitive to series faults than standard negative sequence protection.

8.8.1 BROKEN CONDUCTOR PROTECTION IMPLEMENTATION

Broken Conductor protection is implemented in the *BROKEN CONDUCTOR* column of the relevant settings group.

This column contains the settings to enable the function, for the pickup threshold and the time delay.

8.8.2 BROKEN CONDUCTOR PROTECTION LOGIC

The ratio of I_2/I_1 is calculated and compared with the threshold setting. If the threshold is exceeded, the delay timer is initiated. The CTS block signal is used to block the operation of the delay timer.

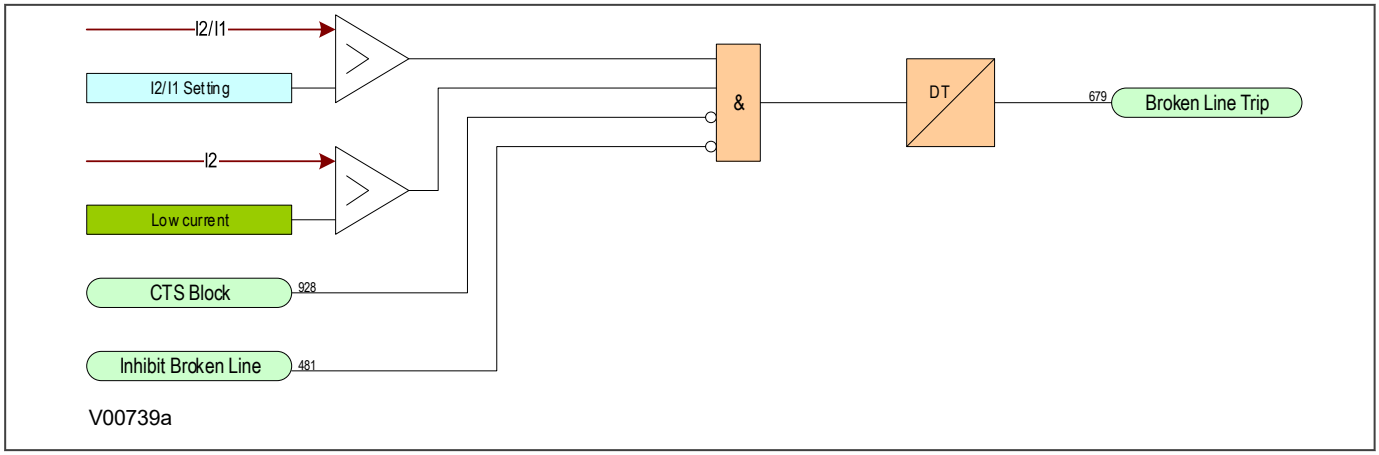


Figure 152: Broken conductor logic

8.8.3 APPLICATION NOTES

8.8.3.1 SETTING GUIDELINES

For a broken conductor affecting a single point earthed power system, there will be little zero sequence current flow and the ratio of I_2/I_1 that flows in the protected circuit will approach 100%. In the case of a multiple earthed power system (assuming equal impedance's in each sequence network), the ratio I_2/I_1 will be 50%.

In practise, the levels of standing negative phase sequence current present on the system govern this minimum setting. This can be determined from a system study, or by making use of the measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during maximum system load conditions, to ensure that all single-phase loads are accounted for.

Note:
A minimum value of 8% negative phase sequence current is required for successful operation.

Since sensitive settings have been employed, we can expect that the element will operate for any unbalanced condition occurring on the system (for example, during a single pole autoreclose cycle). For this reason, a long time delay is necessary to ensure co-ordination with other protection devices. A 60 second time delay setting may be typical.

The following example was recorded by an IED during commissioning:

$$I_{\text{full load}} = 500\text{A}$$

$$I_2 = 50\text{A}$$

therefore the quiescent I_2/I_1 ratio = 0.1

To allow for tolerances and load variations a setting of 20% of this value may be typical: Therefore set:

$$I_2/I_1 = 0.2$$

In a double circuit (parallel line) application, using a 40% setting will ensure that the broken conductor protection will operate only for the circuit that is affected. A setting of 0.4 results in no pick-up for the parallel healthy circuit.

Set I_2/I_1 Time Delay = 60 s to allow adequate time for short circuit fault clearance by time delayed protections.

8.9 TRANSIENT EARTH FAULT DETECTION

Some distribution systems run completely insulated from earth. Such systems are called unearthed systems. The advantage of an unearthed system is that a single phase to earth fault does not cause an earth fault current to flow. This means the whole system remains operational and the supply is not interrupted. The system must be designed to withstand high transient and steady state overvoltages, however, and so its use is generally restricted to low and medium voltage distribution systems.

When there is an earth fault in an unearthed 3-phase system, the voltage of the faulted phase is reduced to the earth potential. This causes the phase voltage in the other two phases to increase, which causes a significant charging current between the phase-to-earth capacitances. This can cause arcing at the fault location. Many systems use a Petersen coil to compensate for this, thus eliminating the arcing problem. Such systems are called compensated networks. The network is earthed with an inductive reactor, where its reactance is made nominally equal to the total system capacitance to earth. Under this condition, a single-phase earth fault does not result in any steady state earth fault current.

The introduction of a Petersen coil introduces major difficulties when it comes to determining the direction of the fault. This is because the faulted line current is the sum of the inductive current introduced by the Petersen coil and the capacitive current of the line, which are in anti-phase with each other. If they are equal in magnitude, the current in the faulted line is zero. If the inductive current is larger than capacitance current, the direction of the faulted line current will appear to be in the same direction as that of the healthy line.

Standard directionalizing techniques used by conventional feeder protection devices are not adequate for this scenario, therefore we need a different method for determining the direction of the fault. Two commonly used methods are the First Half Wave method and the Residual Active Power method.

First Half Wave Method

The initial transient wave, generated at the fault point travels towards the bus along the faulted line, until it reaches the healthy line. For forward faults the high frequency fault voltage and current components are in opposite directions during the first half wave, whereas for reverse faults, they are in phase. This fact can be used to determine the fault direction. This method, however, is subject to the following disadvantages:

- The time duration of the characteristic is very short, in most cases not more than 3 ms. Because of this, it requires a high sampling frequency (3000Hz or even higher)
- It requires an analogue high pass filter, necessitating special hardware
- It is affected by the fault inception angle. For example, when the fault inception angle is 0°, there are no initial travelling waves.

Residual Active Power Method

Residual Active power, which is sometimes used to detect the instance of a fault can also in some cases be used for detecting the fault direction. Although the capacitive currents can be compensated by an inductive current generated by a Petersen coil, the active (instantaneous) current can never be compensated for and this is still opposite to that of the healthy line. This fact can also be used to directionalise the fault.

For a forward directional fault, the zero-sequence active power is the power loss of Petersen's coil, which is negative. For a reverse fault, the zero-sequence active power is the power loss of the transmission line, which is positive. This method, however, is subject to the following disadvantages:

- The zero-sequence active power will be very small in magnitude for a reverse directional fault. Its value depends on the power loss of transmission line.
- The zero-sequence active power may be too small in magnitude to be detected for a forward directional fault. Its value depends on the power loss of Petersen coil.
- High resolution CTs are required

Due to the low magnitude of measured values, reliability is compromised

This product does not use the above techniques for directionalisation. This product uses an innovative patented technique called Transient Reactive Power method to determine the fault direction of an earth fault in a compensated network.

8.9.1 TRANSIENT EARTH FAULT DETECTION IMPLEMENTATION

Transient Earth Fault Detection (TEFD) in this device comprises three modules:

- Transient Earth Fault Detection module (TEF)
- Fault Type Detector (FTD)
- Direction Detector (DD)

Note:
In this product, TEFD is implemented for 50Hz only.

8.9.1.1 TRANSIENT EARTH FAULT DETECTOR

To establish if there is an earth fault on the system somewhere is straightforward. A simple residual overvoltage comparison can determine this. Therefore, a TEF> Start signal is produced by comparing the neutral voltage with a threshold voltage set by ***TEF VN> Start*** in the *TEF DETECTION* column. The difficulty comes with establishing the type of fault and its direction.

8.9.1.2 FAULT TYPE DETECTOR

The FTD uses a Fundamental analysis (FA) technique to establish whether the fault is an intermittent fault or a steady state faults. For Transient Earth Fault Detection, the detector counts the Residual Voltage bursts within a specified time window. With some clever signal processing the detector module creates pulses by comparing the bursts with a settable threshold, then counts these pulses. If the number of pulses equals or exceeds the number specified by the ***FTD> Fault Count*** setting, within the time window specified by ***FTD> Time Window***, the fault is deemed to be intermittent and the ***TEF> Intermit DDB*** signal is asserted. If there are fewer pulses than this number, this indicates either a disturbance or a permanent fault. To establish which, we need to look at the RMS value of the residual voltage.

If there are fewer pulses than specified and the RMS value does not drop below setting within the specified time window, the fault is deemed to be permanent. In this case the ***TEF> Steady*** DDB signal is asserted.

If there are fewer pulses than specified and the RMS value does drop below setting, this indicates that a disturbance has been detected but it is not a fault. In this case, the ***TEF> Steady*** DDB signal is not asserted.

The user can map the signals ***TEF>Steady***, ***TEF>Intermit***, ***TEF>DIR FWD*** or ***TEF> DIR REV*** to the TEF Alarm Logic DDB to generate a TEF Alarm.

The inputs to this module are:

- The residual voltage
- ***FTD> VN*** (defines the threshold which converts the residual voltage burst into a pulse
- ***FTD> Time Window*** (defines the time window - default is 2 seconds)
- ***FTD> Fault Count*** (defines the fault count)

The FTD outputs two signals to indicate whether the fault is steady state or intermittent.

8.9.1.3 DIRECTION DETECTOR

The Direction Detector (DD) uses a patented technique based on Transient Reactive Power (TRP) to establish the direction of the fault. Unlike traditional methods, this TRP method does not require high resolution CTs or special analogue filtering hardware and is therefore cheaper to implement.

It can be shown that the residual voltage and residual current components can be reliably used as discriminative criteria between a faulty and healthy feeder at 220Hz.

The admittance response of a healthy distributed feeder is shown below using a Pi model:

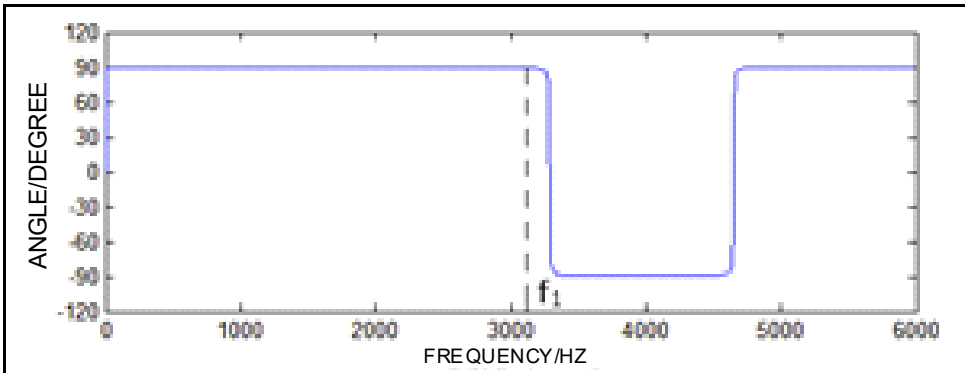


Figure 153: Healthy line response

In the above figure, the phase response of the admittance is consistent at 90o up to frequency f1 (approximately 3000Hz). For a compensated faulty feeder, the admittance response is shown below using a Pi model:

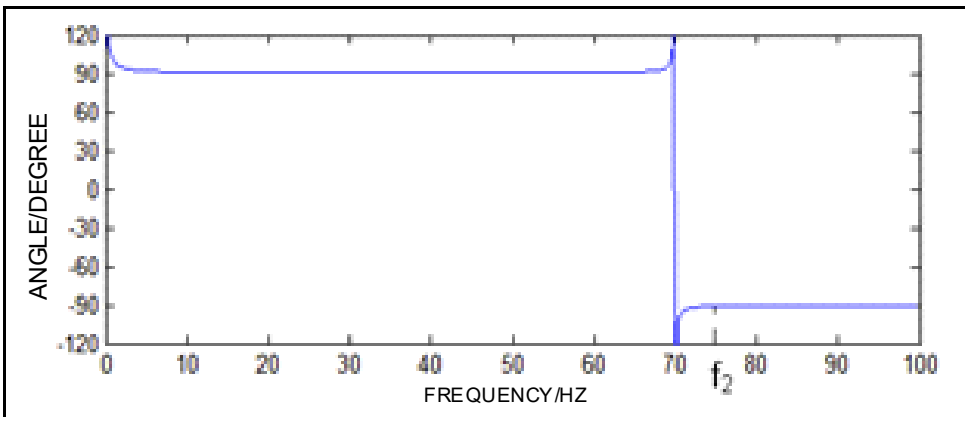


Figure 154: Faulty line response

We can observe that the phase angle (and thus, the reactive power flow) changes from 90o to -90o at frequencies higher than f2. Based on the above, we have clear direction discrimination between a healthy and faulted feeder at any frequency between f2 and f1 approximately.

Note:
The resonant frequency in the above system is 70Hz. For a perfectly compensated system, this will be 50Hz.

MiCOM relays use an anti-aliasing band pass filter with cut-off frequency of 150Hz. Furthermore, at 220Hz the post-filter magnitude is approximately 0.5pu, and at 330Hz, it is less than 0.2pu. To avoid any integer harmonics, and to avoid severely attenuated quantities due to the filter, we have chosen 220Hz as the most suitable frequency for direction determination.

In the forward direction, the residual voltage leads the residual current by 90°, and in the reverse direction the residual voltage lags the residual current by 90°. These criteria can be used to directionalise the fault.

The residual voltage (Vres) after passing through the bandpass filter tuned to 220 Hz, has 90° added to its phase. The residual current (Ires) is also passed through a 220 Hz bandpass filter, but no phase shift is applied. The resulting components which we shall call VH1 and IH2 are therefore in antiphase with each other for forward faults and in phase if the forward line is not faulted.

The VH1 and IH2 components are passed through a sign filter and multiplied to create a reactive power component in the range of -1 to +1. This is the transient reactive power Q_{tran}. If $Q_{tran} > 0$, then there forward line is healthy. If $Q_{tran} < 0$, then the forward line is faulty.

There are two modes of operation for the direction detector; Standard and Advanced. Standard mode is used in most cases and is described here. Advanced mode is for special applications that deviate from the standard model of two or more geographically close feeders outgoing from a power transformer. The following default settings are recommended for majority of applications:

- Dir>Vnf Thresh 8.000 V
- Dir>Inf Thresh 50.00 mA
- Dir>Qn Thresh 100.0e-3
- Dir>Qr Thresh 40.00e-3

When ***TEF>Dir Mod*** is set to ***Advance***, the following settings become visible:

- ***Dir>Qs Thresh*** 50.00e-3
- ***Qn Smooth fct*** 20.00e-3
- ***Operate.Cycles*** 6

Here, Qs is an integration of Q_n, with the window of integration being the first ***Operate cycles*** setting after the start signal is triggered. Q_s is used as a further discriminative directional feature if direction cannot be determined by Q_n only. Q_S is calculated by the following formula:

$$Q_S = \int_{(t=0)}^{(t=K*T)} (Q_{N(t)})$$

Where ‘K’ is the setting Operate Cycles. Operate Cycles affects Qs only.

Qn Smooth fact is a smoothing factor for consecutive Qn values which prevents sudden changes in the value of Qn. The calculated new value of Qn is:

new_valueQn = old_value*(1-smoothing_factor)+ new_value*smoothing_factor.

It is important to note that all settings for the TGFD function, including those at 220Hz, can be set based on 50Hz nominal secondary values. This is because the gain of the 220Hz transient filter is 1.

The inputs to this module are:

- The residual voltage
- The residual current
- ***Dir> Vnf Thresh*** (defines the threshold for the residual voltage sign filter).
- ***Dir> Inf Thresh*** (defines the threshold for the residual current sign filter

The DD outputs two signals to indicate a forward fault and a reverse fault

Sign Filter Thresholds

The ***Dir> Vnf Thresh*** setting is used to get the sign of instantaneous voltage value by sign filter. If the input value is larger than Vnf, the output is +1. If the input value is less than -1*Vnf, the output is -1. Otherwise the output is 0.

The ***Dir> Inf Thresh*** setting is used to get the sign of instantaneous current value by sign filter. If the input value is larger than Vnf, the output is +1. If the input value is less than -1*Vnf, the output is -1. Otherwise the output is 0.

Q_{tran} Thresholds

The setting ***Dir>Qn Thresh*** is the forward direction Q_{tran} threshold calculated from the quantised Vnf and Inf values.

The setting ***Dir>Qr*** is the reverse direction Q_{trans} threshold calculated from the quantised Vnf and Inf values.

The following DDBs are also available:

Timer Block: used to inhibit the TEF function and reset all associated DDBs

Reset TEF: can be configured as a user-defined manual reset alarms

TEF Alarm Output: This is the main TEF alarm that can be mapped to a relay output for a trip

8.9.2 TRANSIENT EARTH FAULT DETECTION LOGIC

8.9.2.1 TRANSIENT EARTH FAULT DETECTION LOGIC OVERVIEW

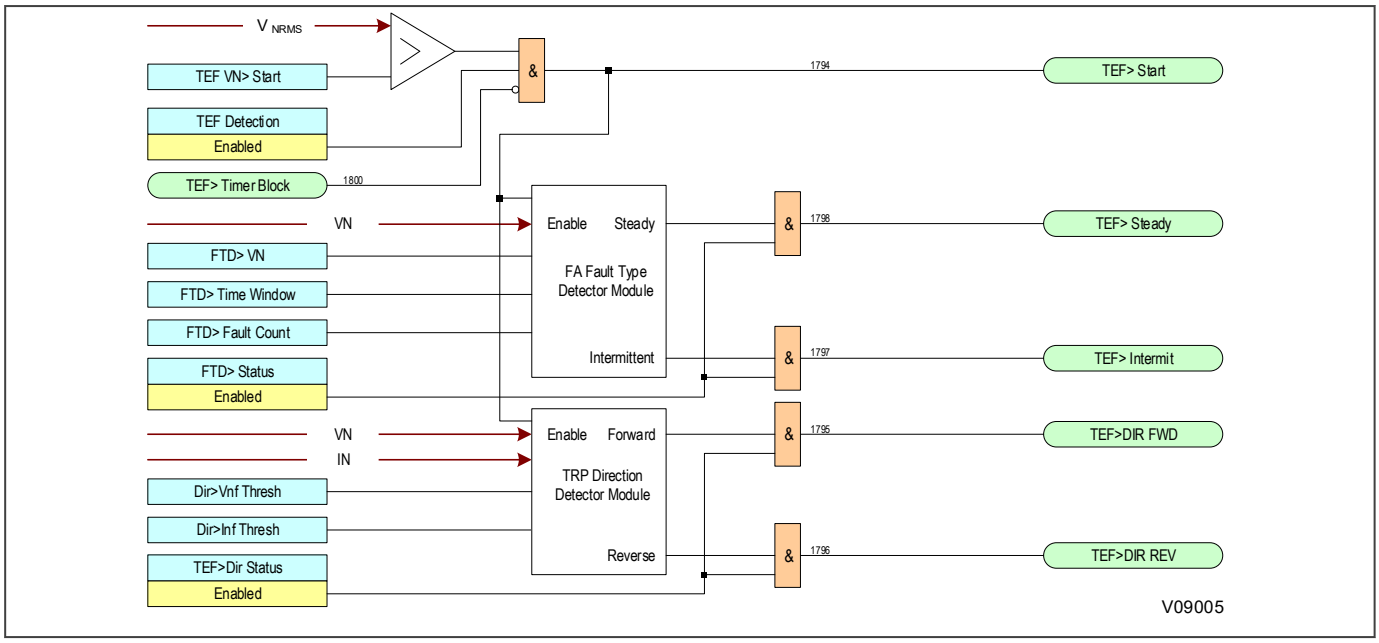


Figure 155: Transient Earth Fault Logic Overview

8.9.2.2 FAULT TYPE DETECTOR LOGIC

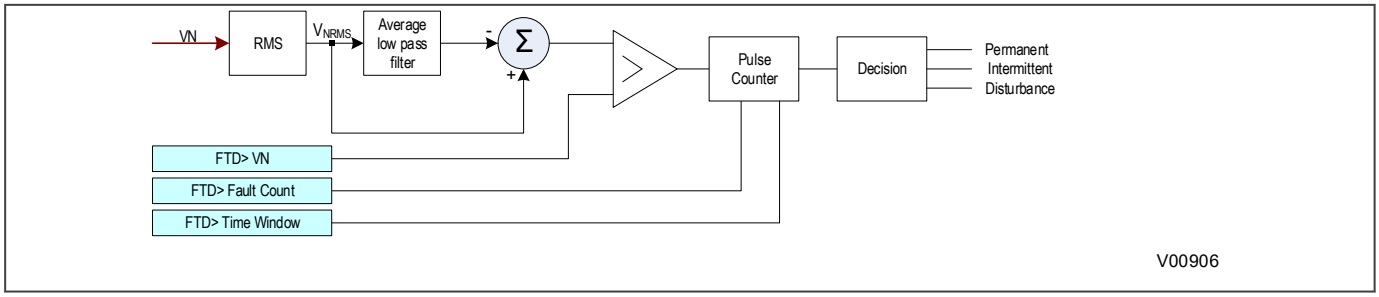


Figure 156: Fault Type Detector Logic

8.9.2.3 DIRECTION DETECTOR LOGIC - STANDARD MODE

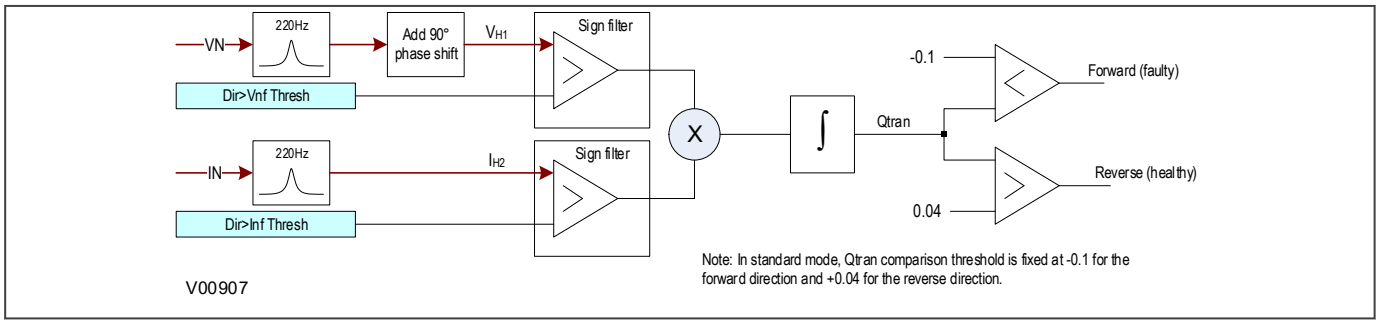


Figure 157: Direction Detector Logic - Standard Mode

8.9.2.4 TRANSIENT EARTH FAULT DETECTION OUTPUT ALARM LOGIC

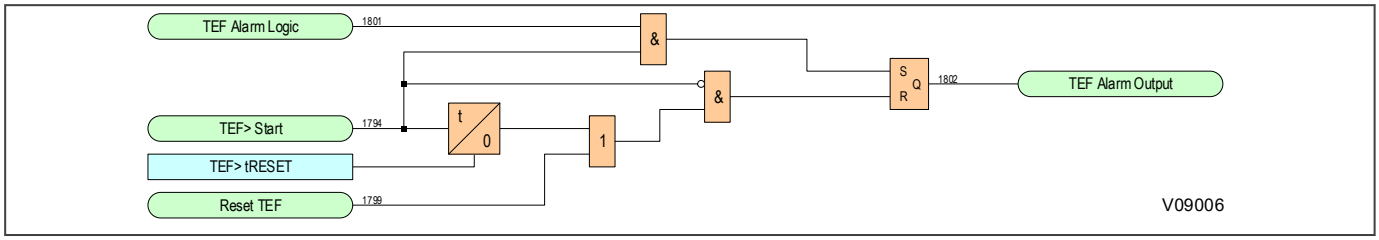


Figure 158: TEFD output alarm logic

8.9.2.5 APPLICATION NOTES

8.9.2.5.1 TRANSIENT EARTH FAULT DETECTION: ACTIVE POWER CHECK

A preventive measure should be taken in cases when relays are located at the extremities of a radial system, where the charging current component reduces the further the relay is from the source, and the active component remains small but constant. In these cases, the transient active current component can be comparable to the transient reactive current during the directional check of the TEFD algorithm.

To ensure correct directionality for all fault positions and system configurations (radial, ring or meshed), the TEFD algorithm shall be supplemented with an additional element - 'Active Power Check'. This scheme ensures the correct directional decision is raised regardless of residual active power levels present in the system at the time of the fault. Sensitive Directional Earth Fault (SDEF) with Active Power Check shall be applied in parallel with the TEFD algorithm.

The combined logic for the TEFD and SDEF is shown in Figure below. A 'Forward START' (shown as a name modified User Alarm) signal is raised when either TEFD FWD or SDEF FWD signals are active. However, 'Forward START' is inhibited if the SDEF REV signal is ever active. This ensures SDEF takes priority if there is enough residual active power during a fault condition. For cases where the residual active power is low, the TEFD algorithm provides the directional decision.

An additional 100ms delay is included to delay the start conditions, thus ensuring the SDEF protection is not adversely affected by the initial fault transient. The TEFD logic is unaffected by the additional timer as its directional decision is latched for a minimum of 200ms after fault inception.

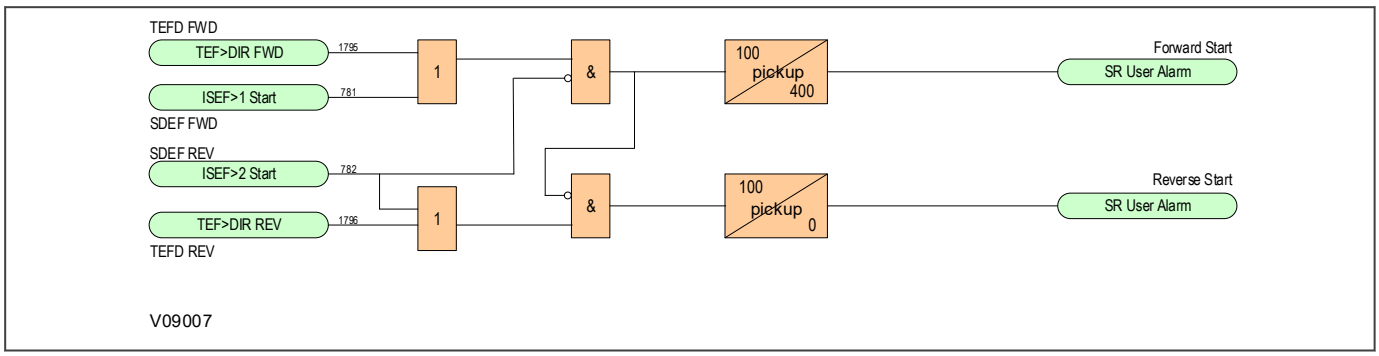


Figure 159: Combined TEFD and SDEF start PSL logic

CHAPTER 9

VOLTAGE PROTECTION FUNCTIONS

9.1 CHAPTER OVERVIEW

The device provides a wide range of voltage protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

9.2 UNDERVOLTAGE PROTECTION

Undervoltage conditions may occur on a power system for a variety of reasons, some of which are outlined below:

- Undervoltage conditions can be related to increased loads, whereby the supply voltage will decrease in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an undervoltage condition, which must be cleared.
- If the regulating equipment is unsuccessful in restoring healthy system voltage, then tripping by means of an undervoltage element is required.
- Faults occurring on the power system result in a reduction in voltage of the faulty phases. The proportion by which the voltage decreases is dependant on the type of fault, method of system earthing and its location. Consequently, co-ordination with other voltage and current-based protection devices is essential in order to achieve correct discrimination.
- Complete loss of busbar voltage. This may occur due to fault conditions present on the incomer or busbar itself, resulting in total isolation of the incoming power supply. For this condition, it may be necessary to isolate each of the outgoing circuits, such that when supply voltage is restored, the load is not connected. Therefore, the automatic tripping of a feeder on detection of complete loss of voltage may be required. This can be achieved by a three-phase undervoltage element.
- Where outgoing feeders from a busbar are supplying induction motor loads, excessive dips in the supply may cause the connected motors to stall, and should be tripped for voltage reductions that last longer than a pre-determined time.

9.2.1 UNDERVOLTAGE PROTECTION IMPLEMENTATION

Undervoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Undervoltage parameters are contained within the sub-heading *UNDERVOLTAGE*.

The product provides two stages of Undervoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V<1 Function*** setting.

The IDMT characteristic is defined by the following formula:

$$t = K/(M-1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage / IED setting voltage (***V<(n) Voltage Set***)

The undervoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V< Measur't Mode*** cell.

There is no Timer Hold facility for Undervoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V<2 Status*** cell.

Outputs are available for single or three-phase conditions via the ***V< Operate Mode*** cell for each stage.

9.2.2 UNDERVOLTAGE PROTECTION LOGIC

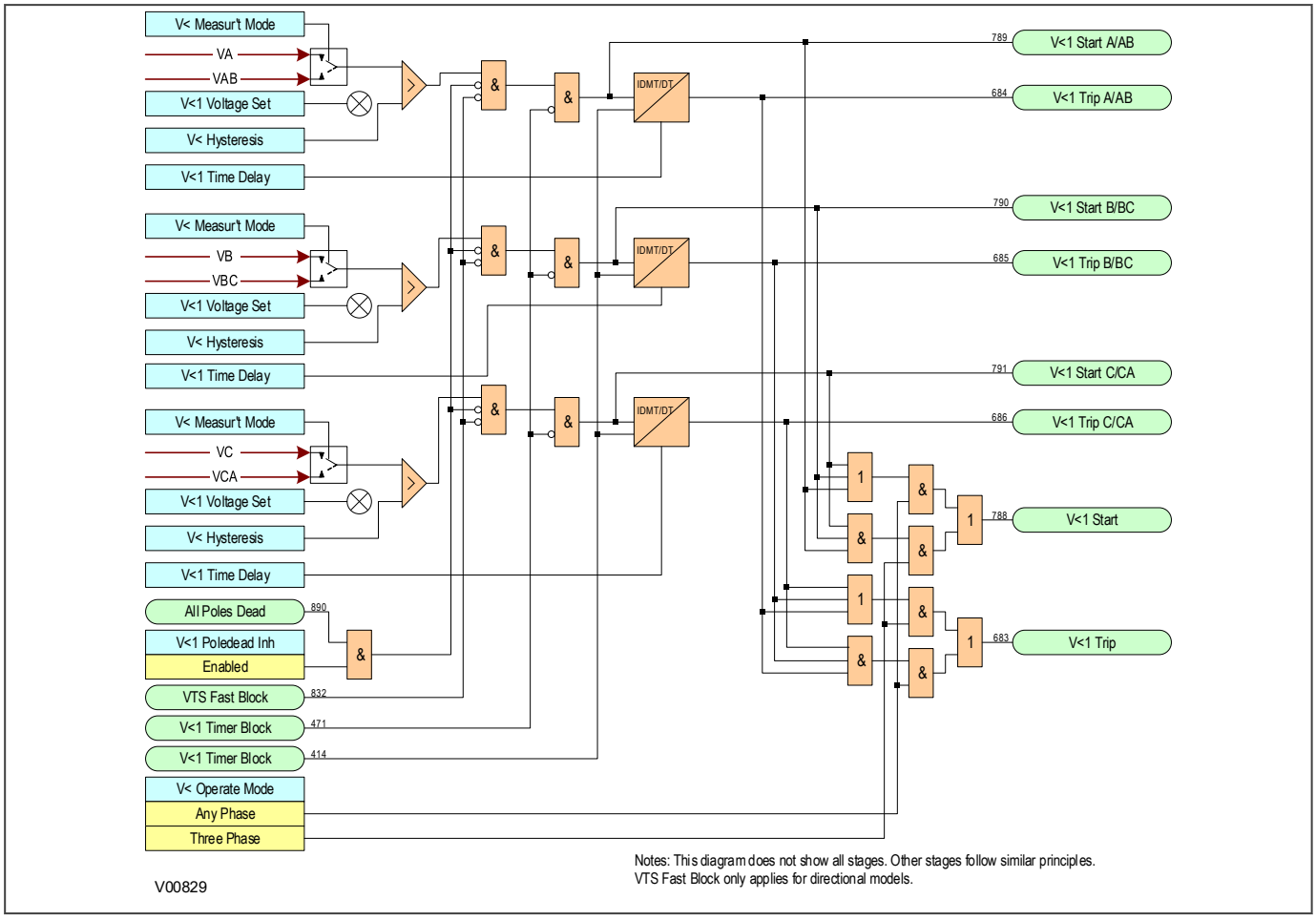


Figure 160: Undervoltage - single and three phase tripping mode (single stage)

The Undervoltage protection function detects when the voltage magnitude for a certain stage falls short of a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal and an ***All Poles Dead*** signal. This ***Start*** signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the undervoltage timer block signal (***V<(n) Timer Block***). For each stage, there are three Phase undervoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V<(n) Start***), which can be be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V< Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V< Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

In some cases, we do not want the undervoltage element to trip; for example, when the protected feeder is de-energised, or the circuit breaker is opened, an undervoltage condition would obviously be detected, but we would not want to start protection. To cater for this, an ***All Poles Dead*** signal blocks the ***Start*** signal for each phase. This is controlled by the ***V<Poledead Inh*** cell, which is included for each of the stages. If the cell is enabled, the relevant stage will be blocked by the integrated pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the opto-inputs or it detects a combination of both undercurrent and undervoltage on any one phase.

Voltage drop-off threshold, defined as a percentage of set voltage, may be adjusted via the ***V< Hysteresis*** setting. For example, where the ***V<Hysteresis*** default setting is *2*, relay pick-up will be at set voltage and drop-off will be at 102% of set voltage.

9.2.3 APPLICATION NOTES

9.2.3.1 UNDERVOLTAGE SETTING GUIDELINES

In most applications, undervoltage protection is not required to operate during system earth fault conditions. If this is the case you should select phase-to-phase voltage measurement, as this quantity is less affected by single-phase voltage dips due to earth faults.

The voltage threshold setting for the undervoltage protection should be set at some value below the voltage excursions that may be expected under normal system operating conditions. This threshold is dependant on the system in question but typical healthy system voltage excursions may be in the order of 10% of nominal value.

The same applies to the time setting. The required time delay is dependant on the time for which the system is able to withstand a reduced voltage.

If motor loads are connected, then a typical time setting may be in the order of 0.5 seconds.

9.3 OVERVOLTAGE PROTECTION

Overvoltage conditions are generally related to loss of load conditions, whereby the supply voltage increases in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an overvoltage condition which must be cleared.

Note:
During earth fault conditions on a power system there may be an increase in the healthy phase voltages. Ideally, the system should be designed to withstand such overvoltages for a defined period of time.

9.3.1 OVERVOLTAGE PROTECTION IMPLEMENTATION

Overvoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Overvoltage parameters are contained within the sub-heading *OVERVOLTAGE*.

The product provides two stages of overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V>1 Function*** setting.

The IDMT characteristic is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage setting voltage (***V>(n) Voltage Set***)

The overvoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V> Measur't Mode*** cell.

There is no Timer Hold facility for Overvoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V>2 Status*** cell.

Outputs are available for single or three-phase conditions via the ***V> Operate Mode*** cell for each stage.

9.3.2 OVERVOLTAGE PROTECTION LOGIC

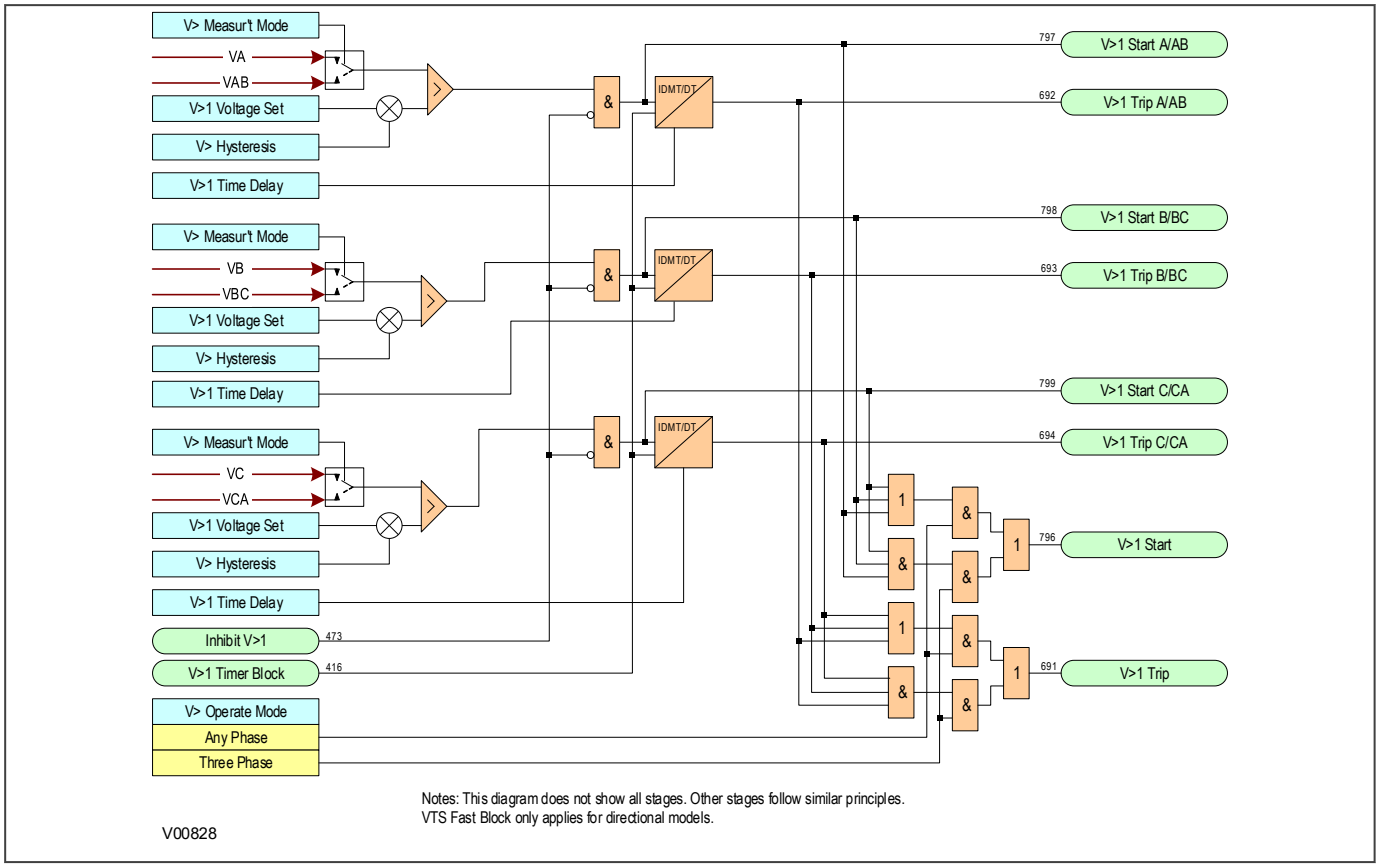


Figure 161: Overvoltage - single and three phase tripping mode (single stage)

The Overvoltage protection function detects when the voltage magnitude for a certain stage exceeds a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal. This start signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the overvoltage timer block signal (***V>(n) Timer Block***). For each stage, there are three Phase overvoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V>(n) Start***), which can then be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V> Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V> Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

Voltage drop-off threshold, defined as a percentage of set voltage, may be adjusted via the ***V> Hysteresis*** setting. For example, where the ***V>Hysteresis*** default setting is 2, relay pick-up will be at set voltage and drop-off will be at 98% of set voltage.

9.3.3 APPLICATION NOTES

9.3.3.1 OVERVOLTAGE SETTING GUIDELINES

The provision of multiple stages and their respective operating characteristics allows for a number of possible applications:

- Definite Time can be used for both stages to provide the required alarm and trip stages.
- Use of the IDMT characteristic allows grading of the time delay according to the severity of the overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time-delayed alarm stage.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled.

This type of protection must be co-ordinated with any other overvoltage devices at other locations on the system.

9.4 COMPENSATED OVERVOLTAGE

The Compensated Overvoltage function calculates the positive sequence voltage at the remote terminal using the positive sequence local current and voltage and the line impedance and susceptance. This can be used on long transmission lines where Ferranti Overvoltages can develop under remote circuit breaker open conditions.

9.4.1 COMPENSATED OVERVOLTAGE IMPLEMENTATION

The Compensated overvoltage protection function can be set in the *VOLT PROTECTION* column under the sub heading COMP OVERVOLTAGE. The remote voltage is calculated using line impedance settings and the line charging admittance in the *LINE PARAMETERS* column.

The IED uses the [A,B,C,D] transmission line equivalent model given the following parameters:

- Total Impedance Z = $z\angle\theta$ ohms
- Total Susceptance Y = $y\angle -90°$
- Line Length l

The remote voltage is calculated using the following equations:

$$\begin{bmatrix} \bar{V}r \\ \bar{I}r \end{bmatrix} = \begin{bmatrix} D & -C \\ -BA & \end{bmatrix} \times \begin{bmatrix} \bar{V}s \\ \bar{I}s \end{bmatrix}$$

where

- V_r is the voltage at the receiving end
- I_r is the current at the receiving end
- V_s is the measured voltage at the sending end
- I_s is the measured current at the sending end
- A= D = cosh(y.l)
- B = Z_c.sinh(y.l)
- C = Y_c.sinh(y.l)
- y.l = $\sqrt{}$(Z.Y)
- Z_c = 1/Y_c = $\sqrt{}$(Z/Y)
- Y = total line capacitive charging susceptance
- Z_c = characteristic impedance of the line (surge impedance)

There are two stages to provide both alarm and trip stages where required. Both stages can be set independently.

Stage 1 can be set to `IDMT`, `DT` or `Disabled`, in the ***V1>1 Cmp Funct*** cell. Stage 2 is DT only and is enabled or disabled in the ***V1>2 Cmp Status*** cell.

The IDMT characteristic on the first stage is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K = Time multiplier setting
- t =Operating time in seconds
- M = Remote Calculated voltage / IED setting voltage

9.4.2 COMPENSATED OVERVOLTAGE LOGIC

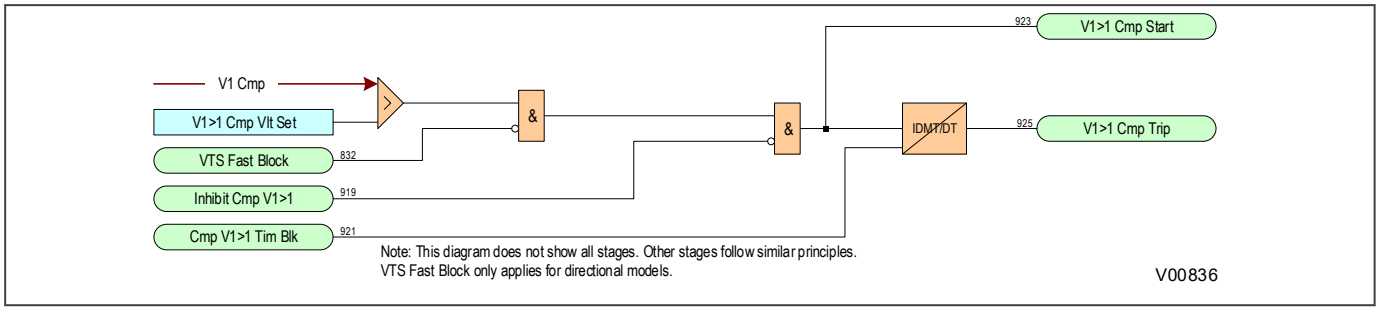


Figure 162: Compensated Overvoltage Logic

The Compensated Overvoltage module (***V1 Cmp***) is a level detector that detects when the voltage magnitude exceeds a set threshold, for each stage. When this happens, the comparator output produces a ***Start*** signal (***V1>(n) Cmp Start***), which signifies the "Start of protection". This can be blocked by a ***VTS Fast block*** signal. This ***Start*** signal is applied to the timer module. The output of the timer module is the ***V1> (n) Cmp Trip*** signal which is used to drive the tripping output relay.

Voltage drop-off threshold, defined as a percentage of set voltage, may be adjusted via the ***Cp V Hysteresis*** setting. For example, where the ***Cp V Hysteresis*** default setting is *2*, relay pick-up will be at set voltage and drop-off will be at 98% of set voltage.

9.4.3 APPLICATION NOTES

9.4.3.1 COMPENSATED OVERVOLTAGE SETTING GUIDELINES

The provision of multiple stages and their respective operating characteristics allows for a number of possible applications:

- Definite Time can be used for both stages to provide the required alarm and trip stages.
- Use of the IDMT characteristic allows grading of the time delay according to the severity of the overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time-delayed alarm stage.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled.

This type of protection must be co-ordinated with any other overvoltage devices at other locations on the system.

9.5 RESIDUAL OVERVOLTAGE PROTECTION

On a healthy three-phase power system, the sum of the three-phase to earth voltages is nominally zero, as it is the vector sum of three balanced vectors displaced from each other by 120°. However, when an earth fault occurs on the primary system, this balance is upset and a residual voltage is produced. This condition causes a rise in the neutral voltage with respect to earth. Consequently this type of protection is also commonly referred to as 'Neutral Voltage Displacement' or NVD for short.

This residual voltage may be derived (from the phase voltages) or measured (from a measurement class open delta VT). Derived values will normally only be used where the model does not support measured functionality (a dedicated measurement class VT). If a measurement class VT is used to produce a measured Residual Voltage, it cannot be used for other features such as Check Synchronisation.

This offers an alternative means of earth fault detection, which does not require any measurement of current. This may be particularly advantageous in high impedance earthed or insulated systems, where the provision of core balanced current transformers on each feeder may be either impractical, or uneconomic, or for providing earth fault protection for devices with no current transformers.

9.5.1 RESIDUAL OVERVOLTAGE PROTECTION IMPLEMENTATION

Residual Overvoltage Protection is implemented in the *RESIDUAL O/V NVD* column of the relevant settings group.

Some applications require more than one stage. For example an insulated system may require an alarm stage and a trip stage. It is common in such a case for the system to be designed to withstand the associated healthy phase overvoltages for a number of hours following an earth fault. In such applications, an alarm is generated soon after the condition is detected, which serves to indicate the presence of an earth fault on the system. This gives time for system operators to locate and isolate the fault. The second stage of the protection can issue a trip signal if the fault condition persists.

The product provides two stages of Derived Residual Overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

The IDMT characteristic is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K= Time multiplier setting
- t = Operating time in seconds
- M = Derived residual voltage setting voltage (***VN> Voltage Set***)

You set this using the ***VN>1 Function*** setting.

Stage 1 also provides a Timer Hold facility.

Stage 2 can have definite time characteristics only. This is set in the ***VN>2 status*** cell

The device derives the residual voltage internally from the three-phase voltage inputs supplied from either a 5-limb VT or three single-phase VTs. These types of VT design provide a path for the residual flux and consequently permit the device to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. Three-limb VTs have no path for residual flux and are therefore unsuitable for this type of protection.

9.5.2 RESIDUAL OVERVOLTAGE LOGIC

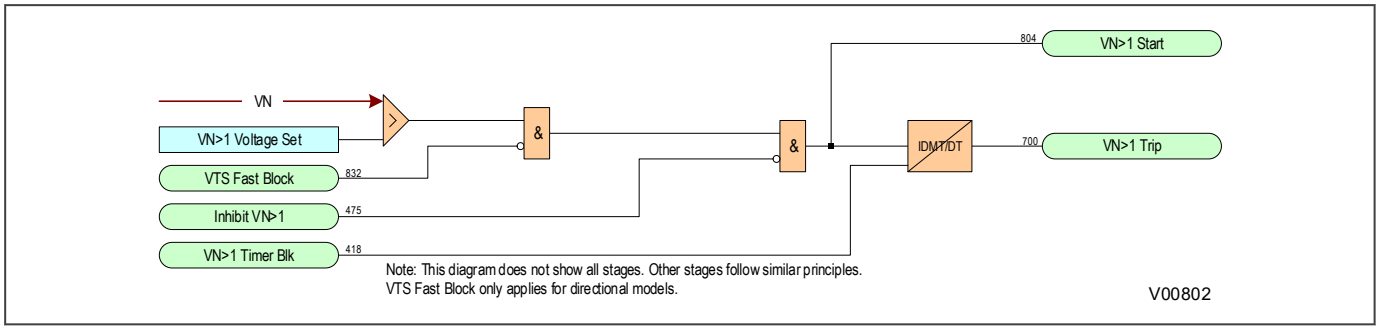


Figure 163: Residual Overvoltage logic

The Residual Overvoltage module (VN>) is a level detector that detects when the voltage magnitude exceeds a set threshold, for each stage. When this happens, the comparator output produces a ***Start*** signal (***VN>(n) Start***), which signifies the "Start of protection". This can be blocked by a ***VTS Fast block*** signal. This ***Start*** signal is applied to the timer module. The output of the timer module is the ***VN> (n) Trip*** signal which is used to drive the tripping output relay.

9.5.3 APPLICATION NOTES

9.5.3.1 CALCULATION FOR SOLIDLY EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

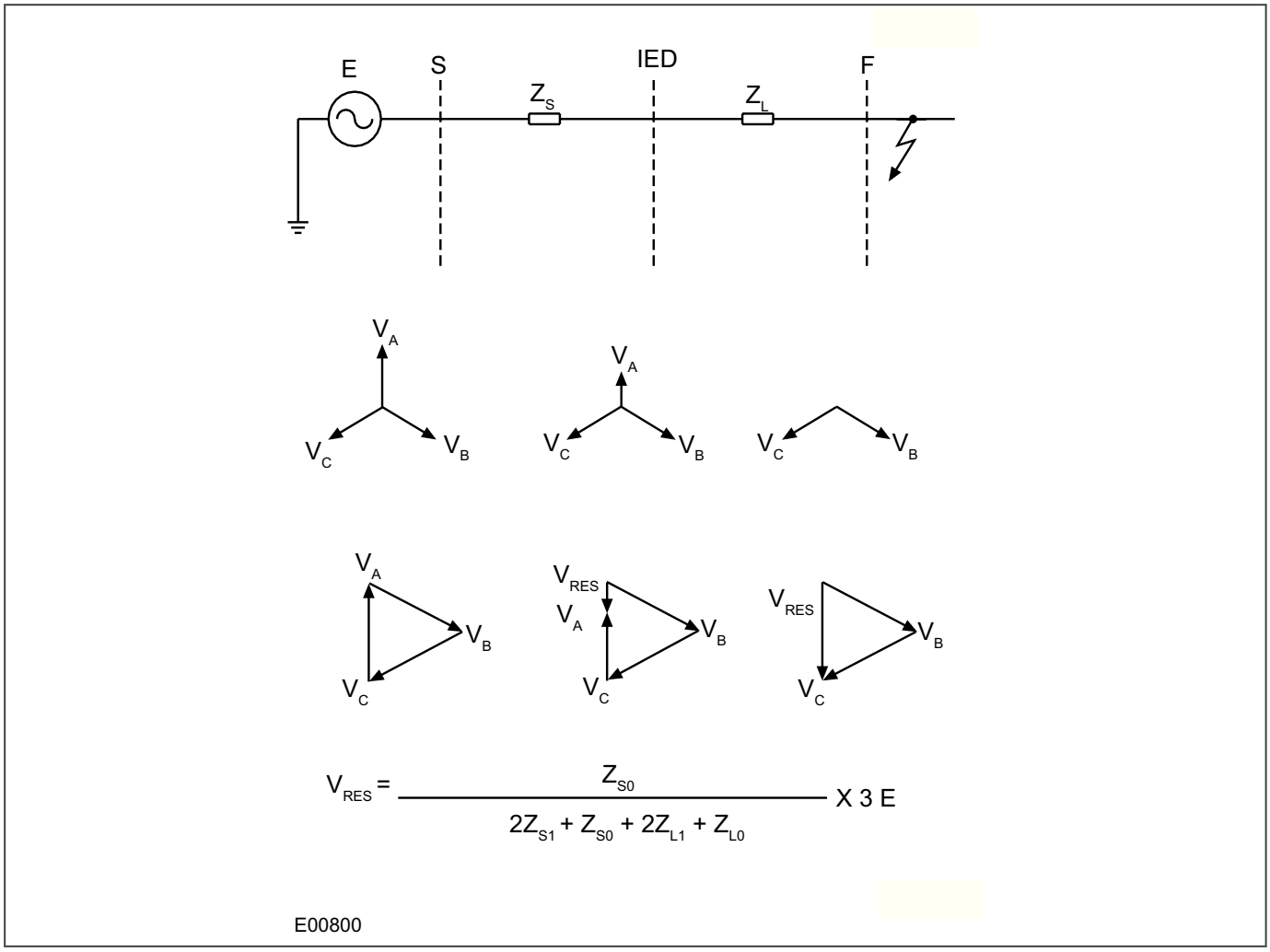


Figure 164: Residual voltage for a solidly earthed system

As can be seen from the above diagram, the residual voltage measured on a solidly earthed system is solely dependant on the ratio of source impedance behind the protection to the line impedance in front of the protection, up to the point of fault. For a remote fault far away, the Z_S/Z_L: ratio will be small, resulting in a correspondingly small residual voltage. Therefore, the protection only operates for faults up to a certain distance along the system. The maximum distance depends on the device setting.

9.5.3.2 CALCULATION FOR IMPEDANCE EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

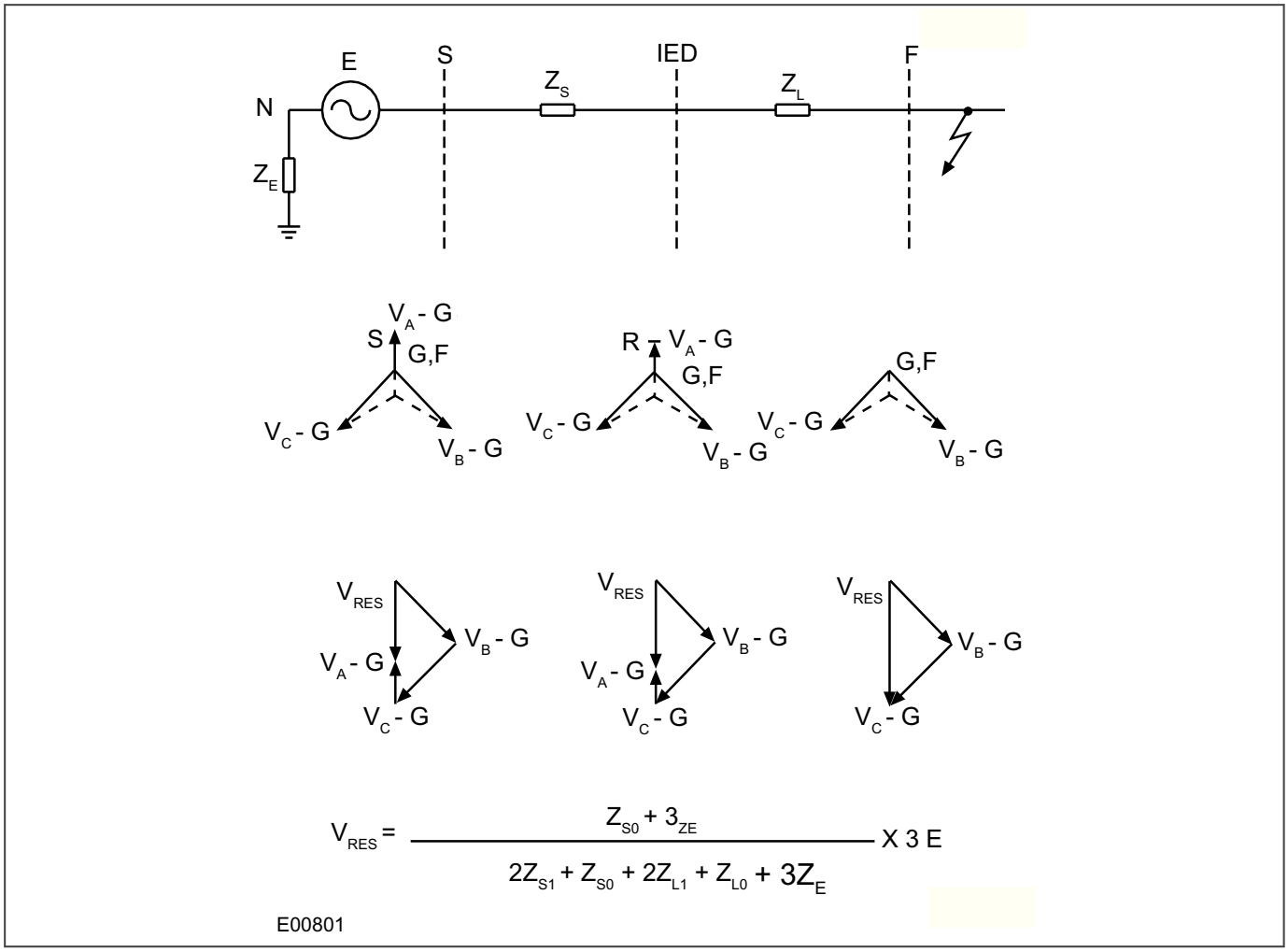


Figure 165: Residual voltage for an impedance earthed system

An impedance earthed system will always generate a relatively large degree of residual voltage, as the zero sequence source impedance now includes the earthing impedance. It follows then that the residual voltage generated by an earth fault on an insulated system will be the highest possible value (3 x phase-neutral voltage), as the zero sequence source impedance is infinite.

9.5.3.3 SETTING GUIDELINES

The voltage setting applied to the elements is dependant on the magnitude of residual voltage that is expected to occur during the earth fault condition. This in turn is dependant on the method of system earthing employed.

Also, you must ensure that the protection setting is set above any standing level of residual voltage that is present on the system.

CHAPTER 10

FREQUENCY PROTECTION FUNCTIONS

10.1 CHAPTER OVERVIEW

The device provides a range of frequency protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

10.2 FREQUENCY PROTECTION

Power generation and utilisation needs to be well balanced in any industrial, distribution or transmission network. These electrical networks are dynamic entities, with continually varying loads and supplies, which are continually affecting the system frequency. Increased loading reduces the system frequency and generation needs to be increased to maintain the frequency of the supply. Conversely decreased loading increases the system frequency and generation needs to be reduced. Sudden fluctuations in load can cause rapid changes in frequency, which need to be dealt with quickly.

Unless corrective measures are taken at the appropriate time, frequency decay can go beyond the point of no return and cause widespread network collapse, which has dire consequences.

Normally, generators are rated for a particular band of frequency. Operation outside this band can cause mechanical damage to the turbine blades. Protection against such contingencies is required when frequency does not improve even after load shedding steps have been taken. This type of protection can be used for operator alarms or turbine trips in case of severe frequency decay.

Clearly a range of methods is required to ensure system frequency stability. The frequency protection in this device provides both underfrequency and overfrequency protection.

Frequency Protection is implemented in the *FREQ PROTECTION* column of the relevant settings group.

10.2.1 UNDERFREQUENCY PROTECTION

A reduced system frequency implies that the net load is in excess of the available generation. Such a condition can arise, when an interconnected system splits, and the load left connected to one of the subsystems is in excess of the capacity of the generators in that particular subsystem. Industrial plants that are dependant on utilities to supply part of their loads will experience underfrequency conditions when the incoming lines are lost.

Many types of industrial loads have limited tolerances on the operating frequency and running speeds (e.g. synchronous motors). Sustained underfrequency has implications on the stability of the system, whereby any subsequent disturbance may damage equipment and even lead to blackouts. It is therefore essential to provide protection for underfrequency conditions.

10.2.1.1 UNDERFREQUENCY PROTECTION IMPLEMENTATION

Simple underfrequency Protection is configured in the FREQ PROTECTION column of the relevant settings group.

The device provides 4 stages of underfrequency protection. The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***F<1 Status:*** enables or disables underfrequency protection for the relevant stage
- ***F<1 Setting***: defines the frequency pickup setting
- ***F<1 Time Delay***: sets the time delay

10.2.1.2 UNDERFREQUENCY PROTECTION LOGIC

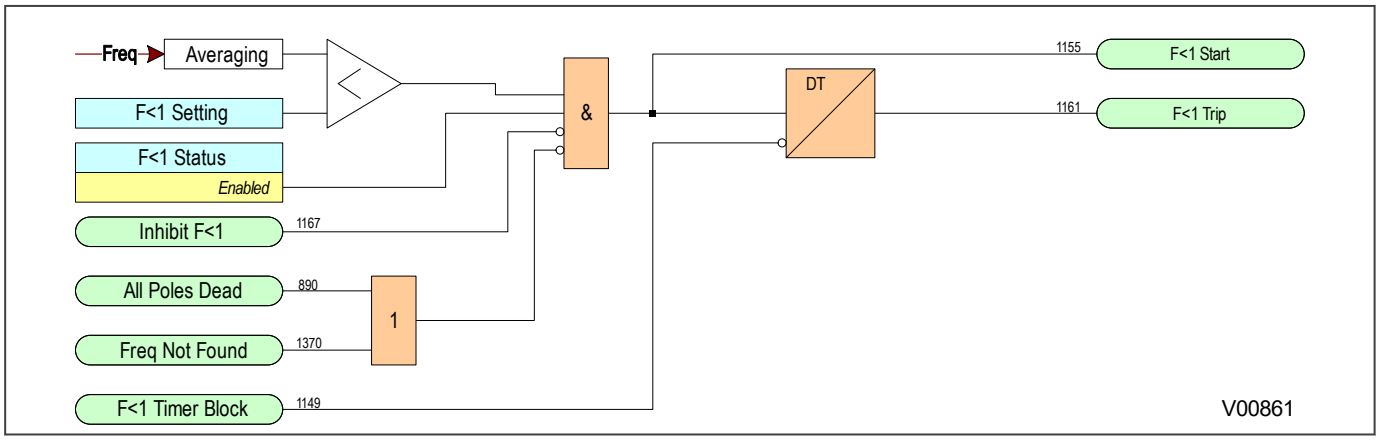


Figure 166: Underfrequency logic (single stage)

If the frequency is below the setting and not blocked the DT timer is started. If the frequency cannot be determined, the function is blocked.

10.2.1.3 APPLICATION NOTES

10.2.1.3.1 SETTING GUIDELINES

In order to minimise the effects of underfrequency, a multi-stage load shedding scheme may be used with the plant loads prioritised and grouped. During an underfrequency condition, the load groups are disconnected sequentially, with the highest priority group being the last one to be disconnected.

The effectiveness of each load shedding stage depends on the proportion of power deficiency it represents. If the load shedding stage is too small compared with the prevailing generation deficiency, then there may be no improvement in the frequency. This should be taken into account when forming the load groups.

Time delays should be sufficient to override any transient dips in frequency, as well as to provide time for the frequency controls in the system to respond. These should not be excessive as this could jeopardize system stability. Time delay settings of 5 - 20 s are typical.

The protection function should be set so that declared frequency-time limits for the generating set are not infringed. Typically, a 10% underfrequency condition should be continuously sustainable.

10.2.2 OVERFREQUENCY PROTECTION

An increased system frequency arises when the mechanical power input to a generator exceeds the electrical power output. This could happen, for instance, when there is a sudden loss of load due to tripping of an outgoing feeder from the plant to a load centre. Under such conditions, the governor would normally respond quickly to obtain a balance between the mechanical input and electrical output, thereby restoring normal frequency. Overfrequency protection is required as a backup to cater for cases where the reaction of the control equipment is too slow.

10.2.2.1 OVERFREQUENCY PROTECTION IMPLEMENTATION

Simple overfrequency Protection is configured in the FREQ PROTECTION column of the relevant settings group.

The device provides 2 stages of overfrequency protection. The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***F>1 Status:*** enables or disables underfrequency protection for the relevant stage
- ***F>1 Setting***: defines the frequency pickup setting
- ***F>1 Time Delay***: sets the time delay

10.2.2.2 OVERFREQUENCY PROTECTION LOGIC

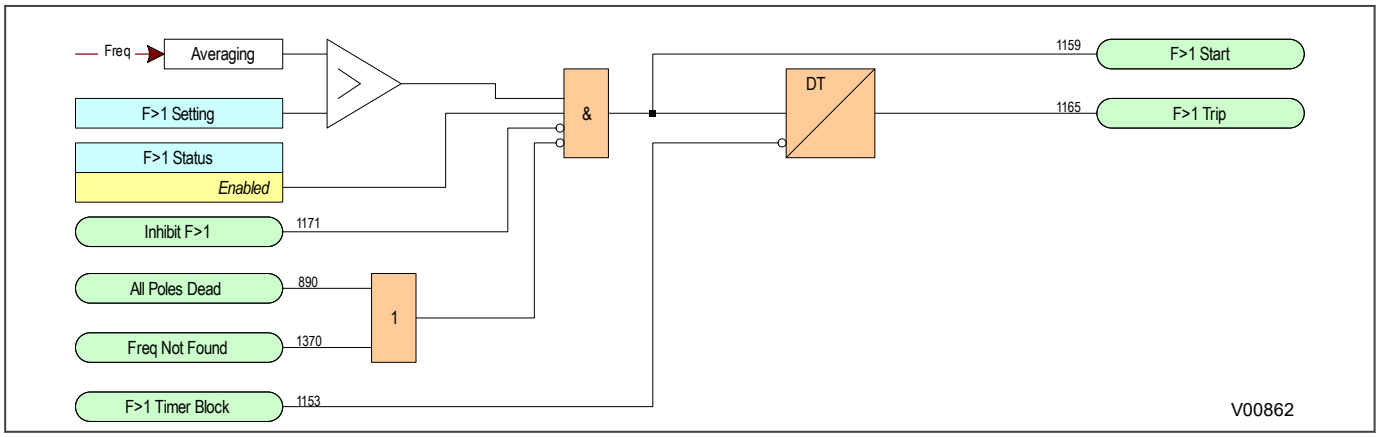


Figure 167: Overfrequency logic (single stage)

If the frequency is above the setting and not blocked, the DT timer is started and after this has timed out, the trip is produced. If the frequency cannot be determined, the function is blocked.

10.2.2.3 APPLICATION NOTES

10.2.2.3.1 SETTING GUIDELINES

Following changes on the network caused by faults or other operational requirements, it is possible that various subsystems will be formed within the power network. It is likely that these subsystems will suffer from a generation/ load imbalance. The "islands" where generation exceeds the existing load will be subject to overfrequency conditions. Severe over frequency conditions may be unacceptable to many industrial loads, since running speeds of motors will be affected. The overfrequency element can be suitably set to sense this contingency.

10.3 INDEPENDENT R.O.C.O.F PROTECTION

Where there are very large loads, imbalances may occur that result in rapid decline in system frequency. The situation could be so bad that shedding one or two stages of load is unlikely to stop this rapid frequency decline. In such a situation, standard underfrequency protection will normally have to be supplemented with protection that responds to the rate of change of frequency. An element is therefore required which identifies the high rate of decline of frequency, and adapts the load shedding scheme accordingly.

Such protection can identify frequency variations occurring close to nominal frequency thereby providing early warning of a developing frequency problem. The element can also be used as an alarm to warn operators of unusually high system frequency variations.

10.3.1 INDEPENENT R.O.C.O.F PROTECTION IMPLEMENTATION

The device provides four independent stages of protection. Each stage can respond to either rising or falling frequency conditions. This depends on whether the frequency threshold is set above or below the system nominal frequency. For example, if the frequency threshold is set above nominal frequency, the rate of change of frequency setting is considered as positive and the element will operate for rising frequency conditions. If the frequency threshold is set below nominal frequency, the setting is considered as negative and the element will operate for falling frequency conditions.

The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***df/dt Avg.Cycles*** calculates the rate of change of frequency over a fixed period of several cycles.
- ***df/dt>1 Status***: determines whether the stage is for falling or rising frequency conditions
- ***df/dt>1 Setting***: defines the rate of change of frequency pickup setting
- ***df/dt>1 Time***: sets the time delay
- ***df/dt>1 Dir'n***: sets the direction of change you wish to check (positive, negative, or both)

In addition, start, trip and timer block DDB signals are available for each stage, as well as an inhibit signal to inhibit all four stages.

Note:
It is recommended to only use df/dt settings <8Hz/s to maintain the claimed performance accuracy for pick-up and operating time, and to ensure the relay is within the frequency operating range, 45-65Hz.

10.3.2 INDEPENDENT R.O.C.O.F PROTECTION LOGIC

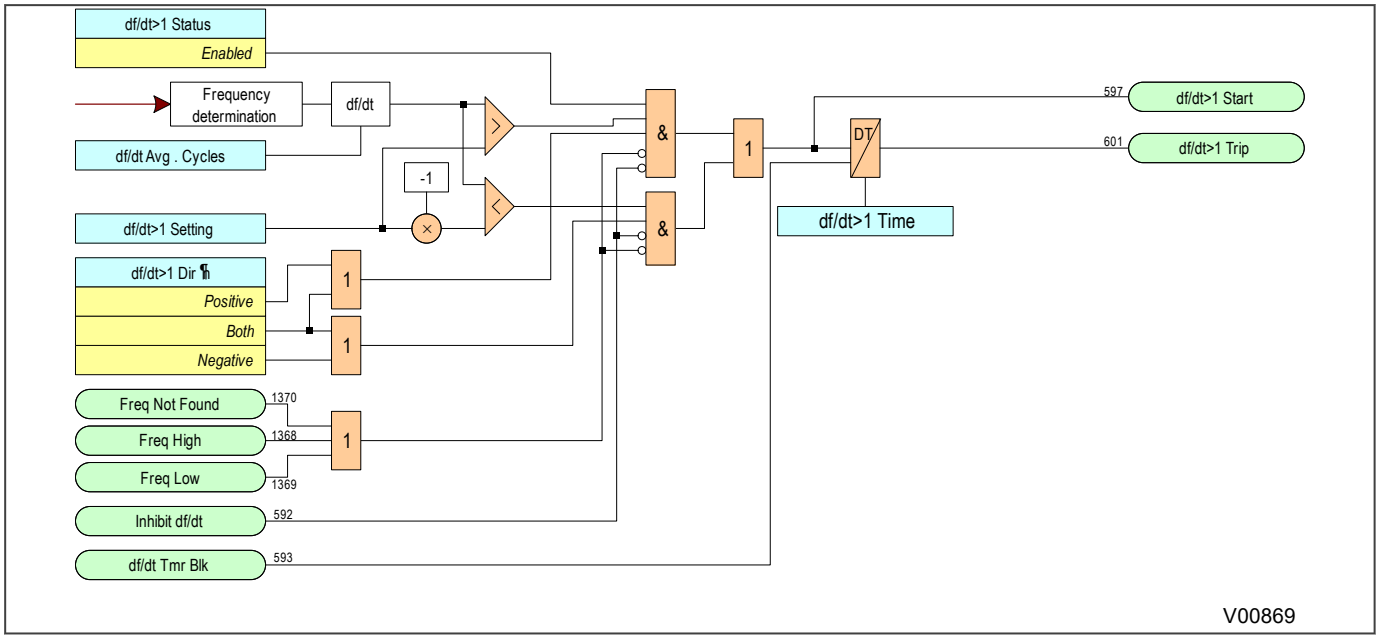


Figure 168: Rate of change of frequency logic (single stage)

CHAPTER 11

POWER PROTECTION FUNCTIONS

11.1 CHAPTER OVERVIEW

Power protection is used for protecting generators. Although the main function of this device is for feeder applications, it can also be used as a cost effective alternative for protecting small distributed generators, typically less than 2 MW.

This chapter contains the following sections:

11.2 OVERPOWER PROTECTION

With Overpower, we should consider two distinct conditions: Forward Overpower and Reverse Overpower.

A forward overpower condition occurs when the system load becomes excessive. A generator is rated to supply a certain amount of power and if it attempts to supply power to the system greater than its rated capacity, it could be damaged. Therefore overpower protection in the forward direction can be used as an overload indication. It can also be used as back-up protection for failure of governor and control equipment. Generally the Overpower protection element would be set above the maximum power rating of the machine.

A reverse overpower condition occurs if the generator prime mover fails. When this happens, the power system may supply power to the generator, causing it to motor. This reversal of power flow due to loss of prime mover can be very damaging and it is important to be able to detect this with a Reverse Overpower element.

11.2.1 OVERPOWER PROTECTION IMPLEMENTATION

Overpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group.

The Power Protection elements provide 4 stages of directional power for both active and reactive power, any of which can be configured as Overpower by selecting the `Over` value in the ***Power1 Function*** (or other stage) setting. The directional element can be configured as forward or reverse and for single-phase or three-phase operation.

The elements use three-phase power and single phase power measurements (based on A, B and/or C phases) as the energising quantities. A Start condition occurs when two consecutive measurements exceed the setting threshold. A trip condition occurs if the Start condition is present for the set time delay. This can be inhibited by the VTS Slow Block and Pole Dead logic if desired.

The Start and Trip timer resets if the power falls below the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent reset functionality, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

11.2.2 OVERPOWER LOGIC

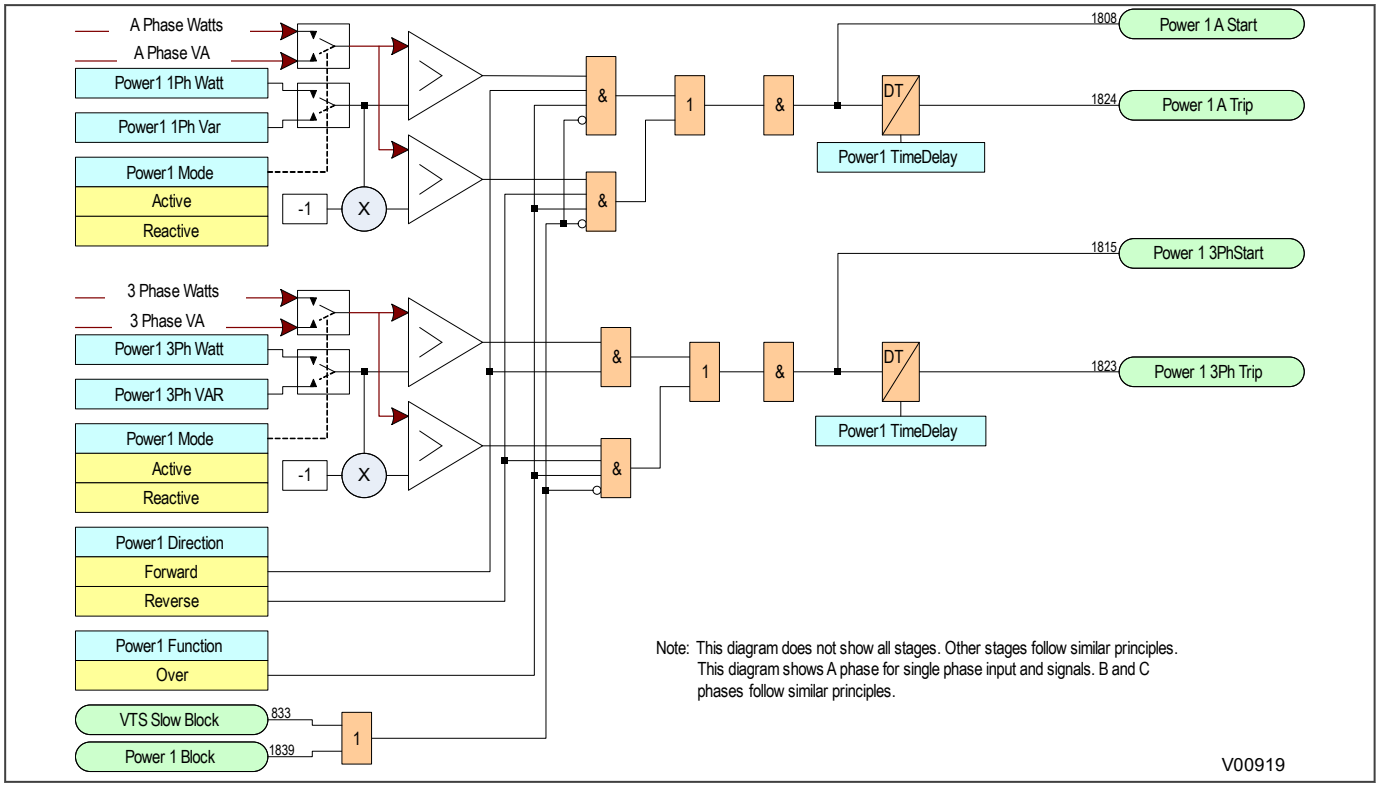


Figure 169: Overpower logic

11.2.3 APPLICATION NOTES

11.2.3.1 FORWARD OVERPOWER SETTING GUIDELINES

The relevant power threshold settings should be set greater than the full load rated power.

The operating mode should be set to Forward.

A time delay setting, ***Power1 TimeDelay*** (or other stage) should be applied. This setting is dependant on the application. The delay on the reset timer, ***Power1 tRESET*** (or other stage) setting, would normally be set to zero.

11.2.3.2 REVERSE POWER CONSIDERATIONS

A generator is expected to supply power to the connected system in normal operation. If the generator prime mover fails, it will begin to take motoring power from the power system (if the power system to which it is connected has other generating sources). The consequences of this reversal of power and the level of power drawn from the power system will be dependant on the type of prime mover.

Typical levels of motoring power and possible motoring damage that could occur for various types of generating plant are given in the following table.

Prime Mover	Motoring Power	Possible Damage (Percentage Rating)
Diesel Engine	5% - 25%	Risk of fire or explosion from unburned fuel
Motoring level depends on compression ratio and cylinder bore stiffness. Rapid disconnection is required to limit power loss and risk of damage.		
Gas Turbine	10% - 15% (Split-shaft) >50% (Single-shaft)	With some gear-driven sets, damage may arise due to reverse torque on gear teeth.

Prime Mover	Motoring Power	Possible Damage (Percentage Rating)
Compressor load on single shaft machines leads to a high motoring power compared to split-shaft machines. Rapid disconnection is required to limit power loss or damage.		
Hydraulic Turbines	0.2 - >2% (Blades out of water) >2.0% (Blades in water)	Blade and runner damage may occur with a long period of motoring
Power is low when blades are above tail-race water level. Hydraulic flow detection devices are often the main means of detecting loss of drive. Automatic disconnection is recommended for unattended operation.		
Steam Turbines	0.5% - 3% (Condensing sets) 3% - 6% (Non-condensing sets)	Thermal stress damage may be inflicted on low-pressure turbine blades when steam flow is not available to dissipate losses due to air resistance.
Damage may occur rapidly with non-condensing sets or when vacuum is lost with condensing sets. Reverse power protection may be used as a secondary method of detection and might only be used to raise an alarm.		

In some applications, the level of reverse power in the case of prime mover failure may fluctuate. This may be the case for a failed diesel engine. To prevent cyclic initiation and reset of the main trip timer, an adjustable reset time delay is provided. You will need to set this time delay longer than the period for which the reverse power could fall below the power setting. This setting needs to be taken into account when setting the main trip time delay.

Note:
A delay in excess of half the period of any system power swings could result in operation of the reverse power protection during swings.

11.2.3.3 REVERSE OVERPOWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a reverse power stage by setting the ***Power1 Direction*** (or other stage) cell to `Reverse`.

The relevant power threshold settings should be set to less than 50% of the motoring power.

The operating mode should be set to Reverse.

The reverse power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation.

A time delay setting, of approximately 5 s would be typically applied.

The delay on the reset timer, ***Power1 tRESET*** (or other stage), would normally be set to zero.

When settings of greater than zero are used for the reset time delay, the pick-up time delay setting may need to be increased to ensure that false tripping does not result in the event of a stable power swinging event.

Reverse overpower protection can also be used for loss of mains applications. If the distributed generator is connected to the grid but not allowed to export power to the grid, it is possible to use reverse power detection to switch off the generator. In this case, the threshold setting should be set to a sensitive value, typically less than 2% of the rated power. It should also be time-delayed to prevent false trips or alarms being given during power system disturbances, or following synchronisation. A typical time delay is 5 seconds.

11.3 UNDERPOWER PROTECTION

Although the Underpower protection is directional and can be configured as forward or reverse, the most common application is for Low Forward Power protection.

When a machine is generating and the circuit breaker connecting the generator to the system is tripped, the electrical load on the generator is cut off. This could lead to overspeeding of the generator if the mechanical input power is not reduced quickly. Large turbo-alternators, with low-inertia rotor designs, do not have a high over speed tolerance. Trapped steam in a turbine, downstream of a valve that has just closed, can rapidly lead to over speed. To reduce the risk of over speed damage, it may be desirable to interlock tripping of the circuit breaker and the mechanical input with a low forward power check. This ensures that the generator circuit breaker is opened only after the mechanical input to the prime mover has been removed, and the output power has reduced enough such that overspeeding is unlikely. This delay in tripping the circuit breaker may be acceptable for non-urgent protection trips (e.g. stator earth fault protection for a high impedance earthed generator). For urgent trips however (e.g. stator current differential protection), this Low Forward Power interlock should not be used.

11.3.1 UNDERPOWER PROTECTION IMPLEMENTATION

Underpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group..

The Power Protection element provides 4 stages of directional power for both active and reactive power, any of which can be configured as Underpower by selecting the `Under` value in the ***Power1 Function*** (or other stage) setting. The directional element can be configured as forward or reverse and for single-phase or three-phase operation.

The elements use three-phase power or single phase power measurements (based on A, B or/and or C phases) as the energising quantity. A start condition occurs when two consecutive measurements fall below the setting threshold. A trip condition occurs if the start condition is present for the set trip time. This can be inhibited by the VTS slow block and pole dead logic if desired.

The Start and Trip timer resets if the power exceeds the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent reset functionality, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

11.3.2 UNDERPOWER LOGIC

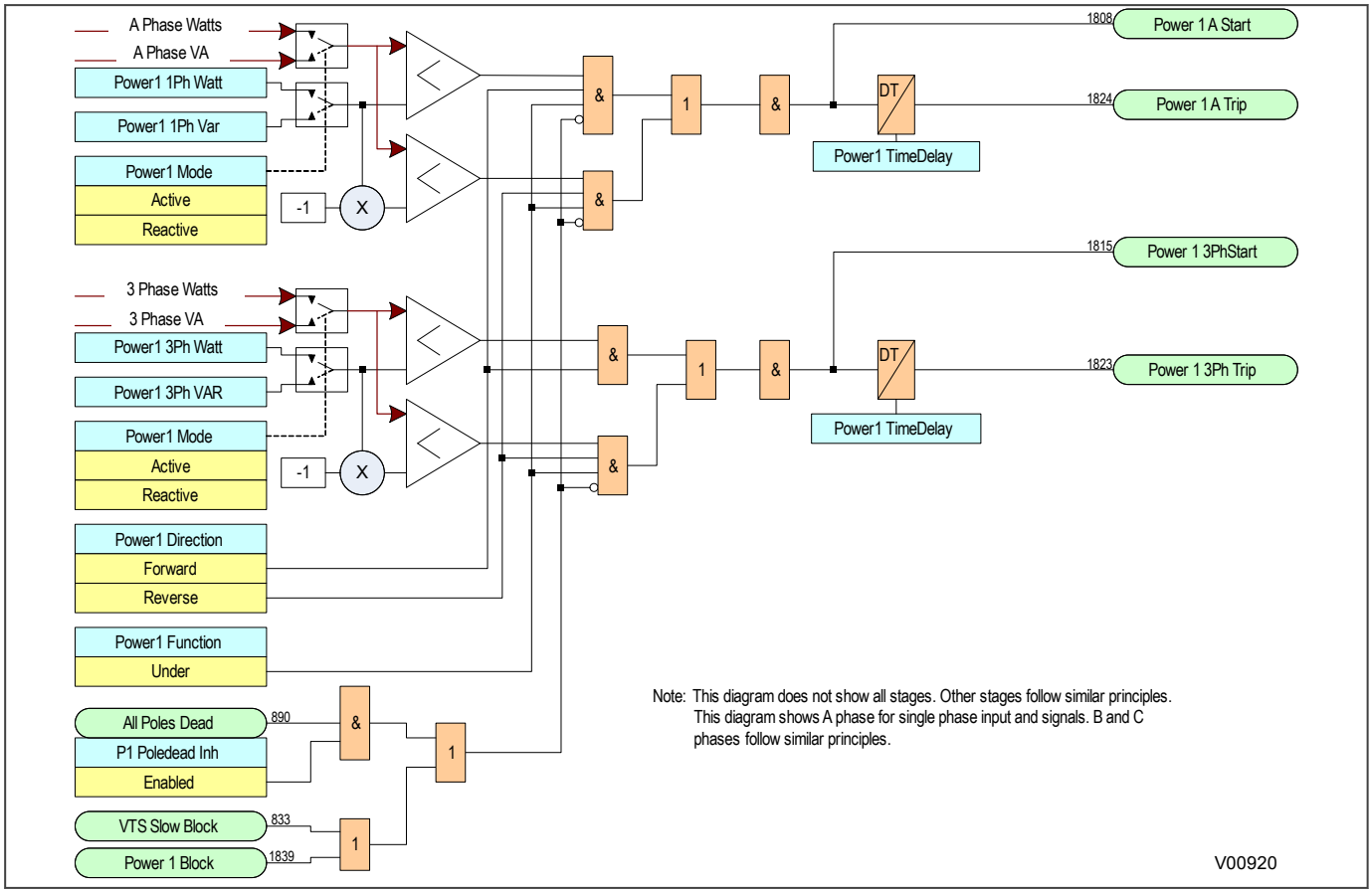


Figure 170: Underpower logic

11.3.3 APPLICATION NOTES

11.3.3.1 LOW FORWARD POWER CONSIDERATIONS

The Low Forward Power protection can be arranged to interlock 'non-urgent' protection tripping using the Flexlogic Equation Editor. It can also be arranged to provide a contact for external interlocking of manual tripping. To prevent unwanted alarms and flags, a Low Forward Power protection element can be disabled when the circuit breaker is opened via Pole Dead logic.

The Low Forward Power protection can also be used to provide loss of load protection when a machine is motoring. It can be used for example to protect a machine which is pumping from becoming unprimed, or to stop a motor in the event of a failure in the mechanical transmission.

A typical application would be for pump storage generators operating in the motoring mode, where there is a need to prevent the machine becoming unprimed which can cause blade and runner damage. During motoring conditions, it is typical for the protection to switch to another setting group with the low forward power enabled and correctly set and the protection operating mode set to `Reverse`.

A low forward power element may also be used to detect a loss of mains or loss of grid condition for applications where the distributed generator is not allowed to export power to the system.

11.3.3.2 LOW FORWARD POWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a forward power stage by setting the ***Power1 Direction*** (or other stage) cell to `Forward`.

When required for interlocking of non-urgent tripping applications, the threshold setting of the low forward power protection function should be less than 50% of the power level that could result in a dangerous overspeed condition on loss of electrical loading.

When required for loss of load applications, the threshold setting of the low forward power protection function, is system dependent, however, it is typically set to 10 - 20% below the minimum load. The operating mode should be set to operate for the direction of the load current, which would typically be reverse for a pump storage machine application where *Forward* is the Generating direction and *Reverse* is the motoring direction.

For interlocking non-urgent trip applications the time delay associated with the low forward power protection function could be set to zero. However, some delay is desirable so that permission for a non-urgent electrical trip is not given in the event of power fluctuations arising from sudden steam valve/throttle closure. A typical time delay is 2 seconds.

For loss of load applications the pick-up time delay is application dependent but is normally set in excess of the time between motor starting and the load being established. Where rated power cannot be reached during starting (for example where the motor is started with no load connected) and the required protection operating time is less than the time for load to be established then it will be necessary to inhibit the power protection during this period. This can be done in the PSL using AND logic and a pulse timer triggered from the motor starting to block the power protection for the required time.

When required for loss of mains or loss of grid applications where the distributed generator is not allowed to export power to the system, the threshold setting of the reverse power protection function, should be set to a sensitive value, typically <2% of the rated power.

The low forward power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation. A time delay setting, of 5 s should be applied typically.

The delay on the reset timers would normally be set to zero.

To prevent unwanted alarms and flags, the protection element can be disabled when the circuit breaker is open via Pole Dead logic.

11.3.3.3 REACTIVE POWER PROTECTION

Some applications provide underexcitation protection using negative reactive power elements. This is popular for synchronous motors and small generators.

A reverse reactive power element may also be used to detect a loss of mains or loss of grid condition for applications where the distributed generator is not allowed to export power to the system.

Setting guidelines

Each stage of power protection can be selected to operate as a reverse reactive power stage by selecting the ***Power1 Function*** (or other stage) cell to *Over* and the ***Power1 Direction*** (or other stage) cell to *Reverse*.

The power threshold setting of the negative reactance power protection, ***Power1 3Ph VAr*** or ***Power1 1Ph VAr*** (or other stage) should be set to supervise the steady state and dynamic stability limits for under excitation protection. The following figure shows an example of the typical settings, Q1 and Q2.

The disadvantage of this method is that the measurement is not very sensitive during low voltage operation of the generator. The reactive power elements can be blocked in the PSL from an undervoltage start signal if this is a problem. This method is less secure than the impedance method and so is often used just to alarm.

If the static limit characteristic Q1 is exceeded, the voltage regulator must first have the opportunity of increasing the excitation. For this reason, a time delayed trip of typically 5-10s is used ***Power1 TimeDelay*** (or other stage). A shorter delay of 0.5s can be used for Q2.

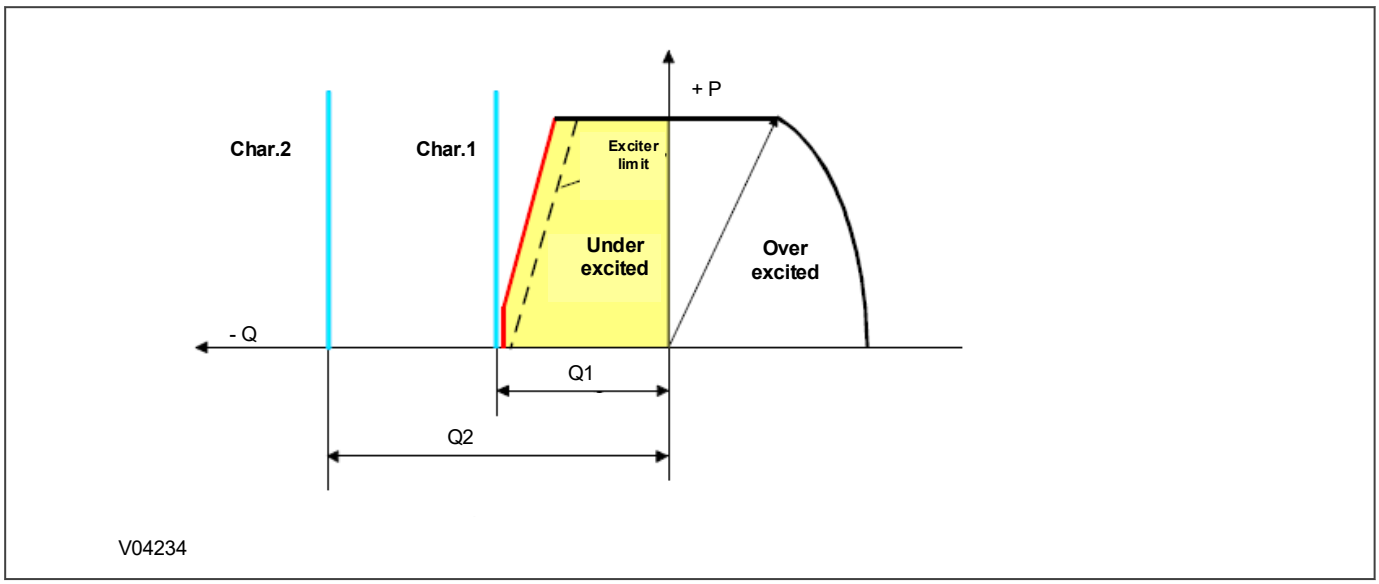


Figure 171: Reactive power protection for underexcitation protection

$Q1 = VN^2/Xd$

$Q2 >= 2\ VN^2/Xd$

Where:

VN = Machine nominal voltage

Xd = Generator direct-axis synchronous reactance in ohms

When required for loss of mains or loss of grid applications where the distributed generator is not allowed to export power to the system, the threshold setting of the reverse reactive power protection function, ***Power1 3Ph VAr*** or ***Power1 1Ph VAr*** (or other stage), should be set to a suitable value, typically <2% of the rated reactive power. The reverse reactive power protection function should be time-delayed, to prevent false trips or alarms being given during power system disturbances or following synchronization, a typical time delay is 5 s.

CHAPTER 12

CURRENT TRANSFORMER REQUIREMENTS

12.1 CHAPTER OVERVIEW

This chapter contains the following sections:

12.2 CT REQUIREMENTS

The current transformer requirements are based on a maximum fault current of 50 times the rated current (In) with the device having an instantaneous overcurrent setting of 25 times the rated current. The current transformer requirements are designed to provide operation of all protection elements.

Where the criteria for a specific application are in excess of this, or the lead resistance exceeds the limiting lead resistance shown in the following table, the CT requirements may need to be modified according to the formulae in the subsequent sections:

Nominal Rating	Nominal Output	Accuracy Class	Accuracy Limited Factor	Limiting Lead Resistance
1A	2.5 VA	10P	20	1.3 ohms
5A	7.5 VA	10P	20	0.11 ohms

The formula subscripts used in the subsequent sections are as follows:

K = A constant affected by the dynamic response of the relay

I_{cn} = Maximum prospective secondary earth fault current or 30 times I> setting (whichever is lower) (amps)

I_{cp} = Maximum prospective secondary phase fault current or 30 times I> setting (whichever is lower) (amps)

I_f = Maximum through-fault current level (amps)

I_{fn} = Maximum prospective secondary earth fault current (amps)

I_{fp} = Maximum prospective secondary phase fault current (amps)

I_n = Rated secondary current (amps)

I_s = Current setting of REF elements (amps)

I_{sn} = Stage 3 & 4 earth fault setting (amps)

I_{sp} = Stage 3, 4, 5 and 6 setting (amps)

I_{st} = Motor start up current referred to CT secondary side (amps)

R_{CT} = Resistance of current transformer secondary winding (ohms)

R_L = Resistance of a single lead from relay to current transformer (ohms)

R_n = Impedance of the neutral current input at 30In (ohms)

R_p = Impedance of the phase current input at 30In (ohms)

R_{st} = Value of stabilising resistor for REF applications (ohms)

V_K = Required CT knee-point voltage (volts)

V_S = Required stability voltage

12.2.1 PHASE OVERCURRENT PROTECTION

12.2.1.1 DIRECTIONAL ELEMENTS

Time-delayed phase overcurrent elements

$$V_K = \frac{I_{cp}}{2}(R_{CT} + R_L + R_p)$$

Instantaneous phase overcurrent elements

$$V_K = \frac{I_{fp}}{2}(R_{CT} + R_L + R_p)$$

12.2.1.2 NON-DIRECTIONAL ELEMENTS

Time-delayed phase overcurrent elements

$$V_K = \frac{I_{cp}}{2}(R_{CT} + R_L + R_p)$$

Instantaneous phase overcurrent elements

$$V_K = I_{sp}(R_{CT} + R_L + R_p)$$

12.2.2 EARTH FAULT PROTECTION

12.2.2.1 DIRECTIONAL ELEMENTS

Instantaneous earth fault overcurrent elements

$$V_K = \frac{I_{fn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

12.2.2.2 NON-DIRECTIONAL ELEMENTS

Time-delayed earth fault overcurrent elements

$$V_K = \frac{I_{cn}}{2}(R_{CT} + 2R_L + R_p + R_n)$$

Instantaneous earth fault overcurrent elements

$$V_K = I_{sn}(R_{CT} + 2R_L + R_p + R_n)$$

12.2.3 SEF PROTECTION (RESIDUALLY CONNECTED)

12.2.3.1 DIRECTIONAL ELEMENTS

Time delayed SEF protection

$$V_K \geq \frac{I_{cn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

Instantaneous SEF protection

$$V_K \geq \frac{I_{fn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

12.2.3.2 NON-DIRECTIONAL ELEMENTS

Time delayed SEF protection

$$V_K \geq \frac{I_{cn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

Instantaneous SEF protection

$$V_K \geq \frac{I_{sn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

12.2.4 SEF PROTECTION (CORE-BALANCED CT)

12.2.4.1 DIRECTIONAL ELEMENTS

Instantaneous element

$$V_K \geq \frac{I_{fn}}{2}(R_{CT} + 2R_L + Rn)$$

Note:
Ensure that the phase error of the applied core balance current transformer is less than 90 minutes at 10% of rated current and less than 150 minutes at 1% of rated current.

12.2.4.2 NON-DIRECTIONAL ELEMENTS

Time delayed element

$$V_K \geq \frac{I_{cn}}{2}(R_{CT} + 2R_L + Rn)$$

Instantaneous element

$$V_K \geq I_{sn}(R_{CT} + 2R_L + Rn)$$

Note:
Ensure that the phase error of the applied core balance current transformer is less than 90 minutes at 10% of rated current and less than 150 minutes at 1% of rated current.

12.2.5 HIGH IMPEDANCE REF PROTECTION

The high impedance REF element will maintain stability for through-faults and operate in less than 40ms for internal faults, provided the following equations are met:

$$R_{st} = \frac{I_f(R_{CT} + 2R_L)}{I_s}$$

$$V_K \geq 4I_s R_{st}$$

Note:
Class x CTs should be used for high impedance REF applications.

12.2.6 USE OF METROSIL NON-LINEAR RESISTORS

Current transformers can develop high peak voltages under internal fault conditions. Metrosils are used to limit these peak voltages to a value below the maximum withstand voltage (usually 3 kV).

You can use the following formulae to estimate the peak transient voltage that could be produced for an internal fault. The peak voltage produced during an internal fault is a function of the current transformer kneepoint voltage and the prospective voltage that would be produced for an internal fault if current transformer saturation did not occur.

$$Vp = 2\sqrt{(2VK(V_F - V_K))}$$

$$Vf = I'f(R_{CT} + 2_{RL} + R_{ST})$$

where:

- Vp = Peak voltage developed by the CT under internal fault conditions
- Vk = Current transformer kneepoint voltage
- Vf = Maximum voltage that would be produced if CT saturation did not occur
- I'f = Maximum internal secondary fault current
- R_{CT} = Current transformer secondary winding resistance
- R_L = Maximum lead burden from current transformer to relay
- R_{ST} = Relay stabilising resistor

You should always use Metrosils when the calculated values are greater than 3000 V. Metrosils are connected across the circuit to shunt the secondary current output of the current transformer from the device to prevent very high secondary voltages.

Metrosils are externally mounted and take the form of annular discs. Their operating characteristics follow the expression:

$$V = CI^{0.25}$$

where:

- V = Instantaneous voltage applied to the Metrosil
- C = Constant of the Metrosil
- I = Instantaneous current through the Metrosil

With a sinusoidal voltage applied across the Metrosil, the RMS current would be approximately 0.52 x the peak current. This current value can be calculated as follows:

$$I_{RMS} = 0.52\left(\frac{\sqrt{2}V_{S(RMS)}}{C}\right)^4$$

where:

- $V_{S(RMS)}$ = RMS value of the sinusoidal voltage applied across the metrosil.

This is due to the fact that the current waveform through the Metrosil is not sinusoidal but appreciably distorted.

The Metrosil characteristic should be such that it complies with the following requirements:

- The Metrosil current should be as low as possible, and no greater than 30 mA RMS for 1 A current transformers or 100 mA RMS for 5 A current transformers.
- At the maximum secondary current, the Metrosil should limit the voltage to 1500 V RMS or 2120 V peak for 0.25 second. At higher device voltages it is not always possible to limit the fault voltage to 1500 V rms, so higher fault voltages may have to be tolerated.

The following tables show the typical Metrosil types that will be required, depending on relay current rating, REF voltage setting etc.

Metrosils for devices with a 1 Amp CT

The Metrosil units with 1 Amp CTs have been designed to comply with the following restrictions:

- The Metrosil current should be less than 30 mA rms.
- At the maximum secondary internal fault current the Metrosil should limit the voltage to 1500 V rms if possible.

The Metrosil units normally recommended for use with 1Amp CTs are as shown in the following table:

	Nominal Characteristic		Recommended Metrosil Type	
Device Voltage Setting	**C**	**β**	**Single Pole Relay**	**Triple Pole Relay**
Up to 125 V RMS	450	0.25	600A/S1/S256	600A/S3/1/S802
125 to 300 V RMS	900	0.25	600A/S1/S1088	600A/S3/1/S1195

Note:
Single pole Metrosil units are normally supplied without mounting brackets unless otherwise specified by the customer.

Metrosils for devices with a 5 Amp CT

These Metrosil units have been designed to comply with the following requirements:

- The Metrosil current should be less than 100 mA rms (the actual maximum currents passed by the devices shown below their type description.
- At the maximum secondary internal fault current the Metrosil should limit the voltage to 1500 V rms for 0.25secs. At the higher relay settings, it is not possible to limit the fault voltage to 1500 V rms so higher fault voltages have to be tolerated.

The Metrosil units normally recommended for use with 5 Amp CTs and single pole relays are as shown in the following table:

Secondary Internal Fault Current	Recommended Metrosil Types for Various Voltage Settings			
Amps RMS	Up to 200 V RMS	250 V RMS	275 V RMS	300 V RMS
50A	600A/S1/S1213 C = 540/640 35 mA RMS	600A/S1/S1214 C = 670/800 40 mA RMS	600A/S1/S1214 C =670/800 50 mA RMS	600A/S1/S1223 C = 740/870 50 mA RMS
100A	600A/S2/P/S1217 C = 470/540 70 mA RMS	600A/S2/P/S1215 C = 570/670 75 mA RMS	600A/S2/P/S1215 C =570/670 100 mA RMS	600A/S2/P/S1196 C =620/740 100 mA RMS
150A	600A/S3/P/S1219 C = 430/500 100 mA RMS	600A/S3/P/S1220 C = 520/620 100 mA RMS	600A/S3/P/S1221 C = 570/670 100 mA RMS	600A/S3/P/S1222 C =620/740 100 mA RMS

In some situations single disc assemblies may be acceptable, contact GE Vernova for detailed applications.

Note:
The Metrosils recommended for use with 5 Amp CTs can also be used with triple pole devices and consist of three single pole units mounted on the same central stud but electrically insulated from each other. To order these units please specify "Triple pole Metrosil type", followed by the single pole type reference. Metrosil for higher voltage settings and fault currents are available if required.

12.2.7 USE OF ANSI C-CLASS CTS

Where American/IEEE standards are used to specify CTs, the C class voltage rating can be used to determine the equivalent knee point voltage according to IEC. The equivalence formula is:

$$V_K = 1.05(C\ rating\ in\ volts) + 100R_{CT}$$

CHAPTER 13

MONITORING AND CONTROL

13.1 CHAPTER OVERVIEW

As well as providing a range of protection functions, the product includes comprehensive monitoring and control functionality.

This chapter contains the following sections:

13.2 EVENT RECORDS

GE Vernova devices record events in an event log. This allows you to establish the sequence of events that led up to a particular situation. For example, a change in a digital input signal or protection element output signal would cause an event record to be created and stored in the event log. This could be used to analyse how a particular power system condition was caused. These events are stored in the IED's non-volatile memory. Each event is time tagged.

The event records can be displayed on an IED's front panel but it is easier to view them through the settings application software. This can extract the events log from the device and store it as a single .evt file for analysis on a PC.

The event records are detailed in the *VIEW RECORDS* column. The first event (0) is always the latest event. After selecting the required event, you can scroll through the menus to obtain further details.

If viewing the event with the settings application software, simply open the extracted event file. All the events are displayed chronologically. Each event is summarised with a time stamp obtained from the ***Time & Date*** cell) and a short description relating to the event obtained from the ***Event Text*** cell). You can expand the details of the event by clicking on the **+** icon to the left of the time stamp.

The following table shows the correlation between the fields in the setting application software's event viewer and the cells in the menu database.

Field in Event Viewer	Equivalent cell in menu DB	Cell reference	User settable?
Left hand column header	VIEW RECORDS → Time & Date	01 03	No
Right hand column header	VIEW RECORDS → Event Text	01 04	No
Description	SYSTEM DATA → Description	00 04	Yes
Plant reference	SYSTEM DATA → Plant Reference	00 05	Yes
Model number	SYSTEM DATA → Model Number	00 06	No
Address	Displays the Courier address relating to the event	N/A	No
Event type	VIEW RECORDS → Menu Cell Ref	01 02	No
Event Value	VIEW RECORDS → Event Value	01 05	No
Evt Unique Id	VIEW RECORDS → Evt Unique ID	01 FE	No

The device is capable of storing up to 5000 time tagged event records.

In addition to the event log, there are two logs which contain duplicates of the last 10 maintenance records and the last 100 fault records. The purpose of this is to provide convenient access to the most recent fault and maintenance events.

13.2.1 EVENT TYPES

There are several different types of event:

- Opto-input events (Change of state of opto-input)
- Contact events (Change of state of output relay contact)
- Alarm events
- Fault record events
- Standard events
- Security events

Standard events are further sub-categorised internally to include different pieces of information. These are:

- Protection events (starts and trips)
- Maintenance record events
- Platform events

Note:
The first event in the list (event 0) is the most recent event to have occurred.

13.2.1.1 OPTO-INPUT EVENTS

If one or more of the opto-inputs has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all opto-inputs. You can tell which opto-input has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Logic Inputs #` where # is the batch number of the opto-inputs. This is '1', for the first batch of opto-inputs and '2' for the second batch of opto-inputs (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the opto-inputs, where the Least Significant Bit (LSB), on the right corresponds to the first opto-input `Input L1`.

The same information is also shown in the ***Opto I/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

13.2.1.2 CONTACT EVENTS

If one or more of the output relays (also known as output contacts) has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all output relays. You can tell which output relay has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Output Contacts #` where # is the batch number of the output relay contacts. This is '1', for the first batch of output contacts and '2' for the second batch of output contacts (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the output relays, where the LSB (on the right) corresponds to the first output contact `Output R1`.

The same information is also shown in the ***Relay O/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

13.2.1.3 ALARM EVENTS

The IED monitors itself on power up and continually thereafter. If it notices any problems, it will register an alarm event.

The description of this event type, as shown in the ***Event Text*** cell is cell dependent on the type of alarm and will be one of those shown in the following tables, followed by `OFF` or `ON`.

The event value shown in the ***Event Value*** cell for this type of event is a 32 bit binary string. There are one or more banks 32 bit registers, depending on the device model. These contain all the alarm types and their logic states (`ON` or `OFF`).

The same information is also shown in the ***Alarm Status (n)*** cells in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

13.2.1.4 FAULT RECORD EVENTS

An event record is created for every fault the IED detects. This is also known as a fault record.

The event type description shown in the ***Event Text*** cell for this type of event is always `Fault Recorded`.

The IED contains a separate register containing the latest fault records. This provides a convenient way of viewing the latest fault records and saves searching through the event log. You access these fault records using the ***Select Fault*** setting, where fault number 0 is the latest fault.

A fault record is triggered by the ***Fault REC TRIG*** signal DDB, which is assigned in the PSL. The fault recorder records the values of all parameters associated with the fault for the duration of the fault. These parameters are stored in separate Courier cells, which become visible depending on the type of fault.

The fault recorder stops recording only when:

The Start signal is reset AND the undercurrent is ON OR the Trip signal is reset, as shown below:

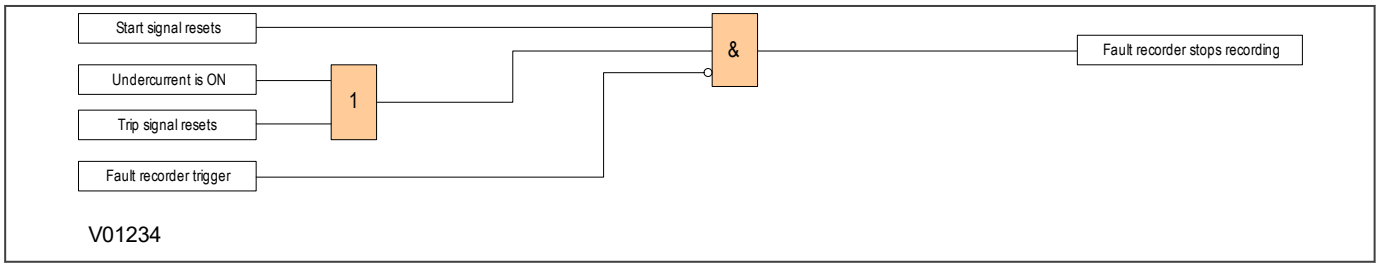


Figure 172: Fault recorder stop conditions

The event is logged as soon as the fault recorder stops. The time stamp assigned to the fault corresponds to the start of the fault. The timestamp assigned to the fault record event corresponds to the time when the fault recorder stops.

> *Note:*
> *We recommend that you do not set the triggering contact to latching. This is because if you use a latching contact, the fault record would not be generated until the contact has been fully reset.*

13.2.1.5 MAINTENANCE EVENTS

Internal failures detected by the self-test procedures are logged as maintenance records. Maintenance records are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is always `Maint Recorded`.

The ***Event Value*** cell also provides a unique binary code.

The IED contains a separate register containing the latest maintenance records. This provides a convenient way of viewing the latest maintenance records and saves searching through the event log. You access these fault records using the ***Select Maint*** setting.

The maintenance record has a number of extra menu cells relating to the maintenance event. These parameters are ***Maint Text***, ***Maint Type*** and ***Maint Data***. They contain details about the maintenance event selected with the ***Select Maint*** cell.

13.2.1.6 PROTECTION EVENTS

The IED logs protection starts and trips as individual events. Protection events are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is dependent on the protection event that occurred. Each time a protection event occurs, a DDB signal changes state. It is the name of this DDB signal followed by 'ON' or 'OFF' that appears in the ***Event Text*** cell.

The ***Event Value*** cell for this type of event is a 32 bit binary string representing the state of the relevant DDB signals. These binary strings can also be viewed in the *COMMISSION TESTS* column in the relevant DDB batch cells.

Not all DDB signals can generate an event. Those that can are listed in the *RECORD CONTROL* column. In this column, you can set which DDBs generate events.

13.2.1.7 SECURITY EVENTS

An event record is generated each time a setting that requires an access level is executed.

The event type description shown in the ***Event Text*** cell displays the type of change.

13.2.1.8 PLATFORM EVENTS

Platform events are special types of standard events.

The event type description shown in the ***Event Text*** cell displays the type of change.

13.3 DISTURBANCE RECORDER

The disturbance recorder feature allows you to record selected current and voltage inputs to the protection elements, together with selected digital signals. The digital signals may be inputs, outputs, or internal DDB signals. The disturbance records can be extracted using the disturbance record viewer in the settings application software. The disturbance record file can also be stored in the COMTRADE format. This allows the use of other packages to view the recorded data.

The integral disturbance recorder has an area of memory specifically set aside for storing disturbance records. The number of records that can be stored is dependent on the recording duration. The minimum duration is 0.1 s and the maximum duration is 10.5 s.

When the available memory is exhausted, the oldest records are overwritten by the newest ones.

Each disturbance record consists of a number of analogue data channels and digital data channels. The relevant CT and VT ratios for the analogue channels are also extracted to enable scaling to primary quantities.

The fault recording times are set by a combination of the ***Duration*** and ***Trigger Position*** cells. The ***Duration*** cell sets the overall recording time and the ***Trigger Position*** cell sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.

With the ***Trigger Mode*** set to *Single*, if further triggers occurs whilst a recording is taking place, the recorder will ignore the trigger. However, with the ***Trigger Mode*** set to *Extended*, the post trigger timer will be reset to zero, extending the recording time.

You can select any of the IED's analogue inputs as analogue channels to be recorded. You can also map any of the opto-inputs output contacts to the digital channels. In addition, you may also map a number of DDB signals such as Starts and LEDs to digital channels.

You may choose any of the digital channels to trigger the disturbance recorder on either a low to high or a high to low transition, via the ***Input Trigger*** cell. The default settings are such that any dedicated trip output contacts will trigger the recorder.

It is not possible to view the disturbance records locally via the front panel LCD. You must extract these using suitable setting application software such as MiCOM S1 Agile.

13.4 MEASUREMENTS

13.4.1 MEASURED QUANTITIES

The device measures directly and calculates a number of system quantities, which are updated every second. You can view these values in the relevant MEASUREMENT columns or with the Measurement Viewer in the settings application software. Depending on the model, the device may measure and display some or more of the following quantities:

- Measured and calculated analogue current and voltage values
- Power and energy quantities
- Peak, fixed and rolling demand values
- Frequency measurements
- Thermal measurements
- Teleprotection channel measurements

13.4.2 MEASUREMENT SETUP

You can define the way measurements are set up and displayed using the *MEASURE'T SETUP* column and the measurements are shown in the relevant MEASUREMENTS tables.

13.4.3 FAULT LOCATOR

Some models provide fault location functionality. It is possible to identify the fault location by measuring the fault voltage and current magnitude and phases and presenting this information to a Fault Locator function. The fault locator is triggered whenever a fault record is generated, and the subsequent fault location data is included as part of the fault record. This information is also displayed in the ***Fault Location*** cell in the *VIEW RECORDS* column. This cell will display the fault location in metres, miles ohms or percentage, depending on the chosen units in the ***Fault Location*** cell of the *MEASURE'T SETUP* column.

The Fault Locator uses pre-fault and post-fault analogue input signals to calculate the fault location. The result is included it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record.

When applied to parallel circuits, mutual flux coupling can alter the impedance seen by the fault locator. The coupling contains positive, negative and zero sequence components. In practise the positive and negative sequence coupling is insignificant. The effect on the fault locator of the zero sequence mutual coupling can be eliminated using the mutual compensation feature provided.

13.4.3.1 FAULT LOCATOR OPERATION

The 5th Generation fault locator uses an algorithmic method to provide a distance to fault location feature with metering capabilities. The data input to the algorithm is filtered using established digital signal processing techniques.

The data processed by the algorithm is first acquired by performing analogue to digital conversion on signals provided by the relays internal analogue bus and then performing the necessary calculations.

The metering values are continuously calculated, regularly updated and passed to the relays processor when requested.

Acquired data is written to a buffer until a fault condition is notified by the processor. This input buffer data is held pending the fault calculation and input data is redirected to an alternative buffer.

The fault calculation is initiated by a signal from the relay main processor. When the fault calculation is complete the output information is stored in non-volatile memory and made available to the processor for display on the relay front panel.

Where parallel circuits are hung on opposite sides of a route of towers, mutual flux coupling alters the impedance seen by the fault locator. In practice the positive and negative sequence coupling is insignificant and the effect on the fault locator of the zero sequence mutual coupling can be eliminated by using the mutual compensation feature provided.

It should be noted that in relays fitted with both a ***DEF*** element and a fault locator, the mutual compensation current input terminals are shared with the ***DEF*** zero sequence current polarising input. And so, ***DEF*** zero sequence current polarising cannot be used at the same time as fault locator mutual compensation.

The fault locator is optional on the underground cable version of the relay, where it is recommended that it is used for metering purposes only (see the Metering section, below) as fault location accuracy cannot be relied upon for this application.

13.4.3.2 EARTH FAULT BASIC THEORY

A two-machine equivalent circuit of a faulted power system is shown in the figure below:

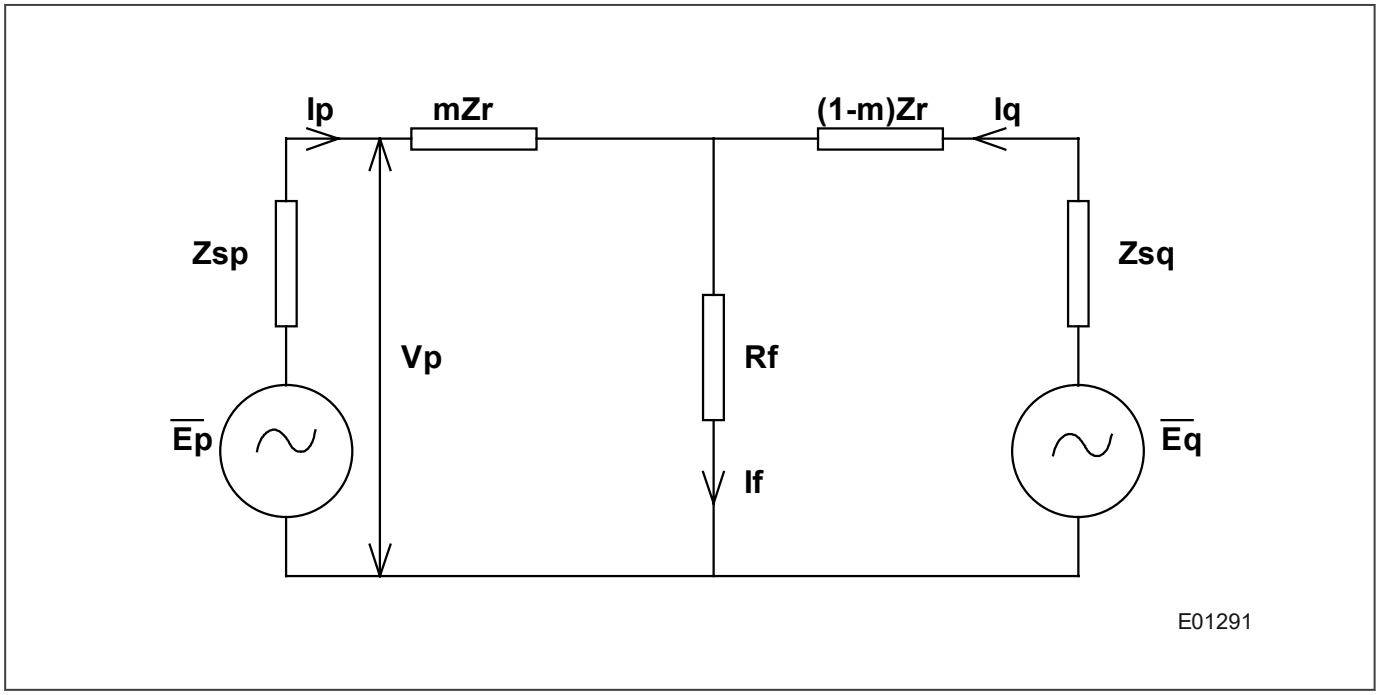


Figure 173: Two machine equivalent circuit

From the above figure:

$$Vp = mIpZr + IfRf$$

This equation shows that the calculation of m, the distance to fault, based on measurements of Vp and Ip at the local relay terminals is distorted by the IfRf term. This term is related to the current infeed from the remote terminal and cannot be readily measured. However its effect can be minimised as follows:

The real and imaginary components of these vectors (with respect to an arbitrary vector reference) vary with time as:

$$|Vp|[\cos(\omega t + s) + j\sin(\omega t + s)] = m|Zr|\,|Ip|\,[\cos(\omega t + e) + j\sin(\omega tt + e)] + Rf\,|If|\,[\cos(\omega t + d) + j\sin(\omega t + d)].$$

where:

d is the angle of the fault current.

s is the angle of Vp.

e is the angle of IpZr.

By evaluating equation *Vp = mIpZr + IfRf* at the instant in time when the fault current passes through zero and considering only the real components, then the Rf |If| term becomes zero i.e. t = ((π/2)-d)/ ω and the equation simplifies to:

$$|Vp|\cos(((\pi/2)-d) + s) = m\,|Zr|\,|Ip|\,\cos(((\pi/2)-d) + e)$$

Therefore, the fault location m can be calculated if the angle of the fault current d is known.

Estimating d the phase of the fault current If:

The fault vector If is obtained from an algorithm which uses superimposed currents, that is, the change of currents following the instant of fault.

Superimposed currents are indicated with an apostrophe (').

The sequence diagram for superimposed currents for an A-G fault is shown in the figure below:

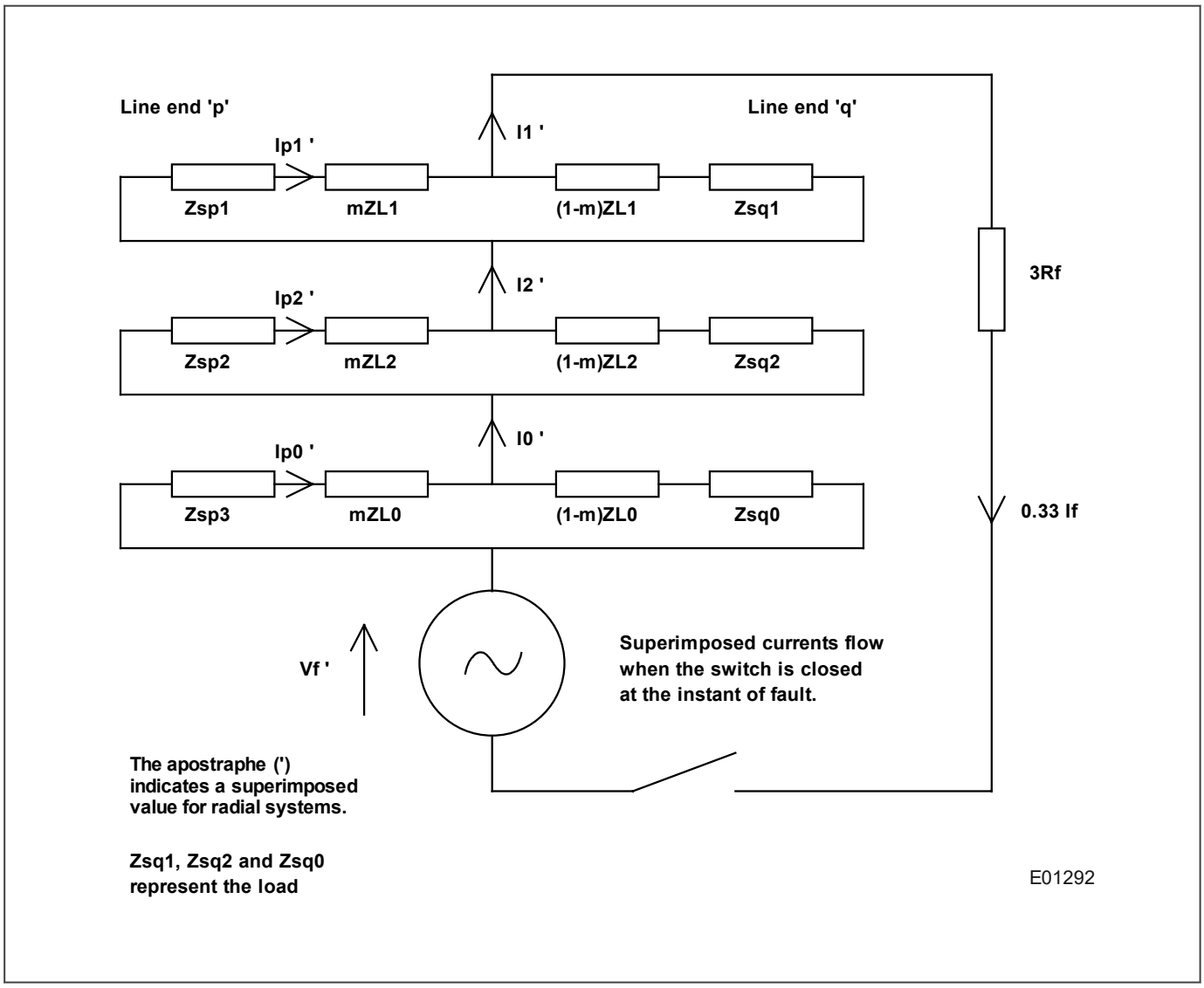


Figure 174: Superimposed symmetrical component sequence for A - N fault

For an A phase to earth fault:

$$0.33If = I1' = I2' = I0'$$

from which:

$$0.66If = I1' + I2'$$

$$= Ip1'D1 + Ip2'D2$$

where:

$$D1 = I1' / Ip1' \text{ and } D2 = I2' / Ip2'$$

and:

D2 approximately = D1 (assuming that the power system source and line positive and negative sequence impedances are approximately equal)

therefore:

$$0.66If = D1(Ip1' + Ip2')$$

also:

$$Ip' = Ip1' + Ip2' + Ip0'$$

therefore:

$$Ip1' + Ip2' = Ip' - Ip0'$$

from the equations above:

$$0.66If = D1\ (Ip' - Ip0')$$

Hence:

$$\text{angle } If = \text{angle } D1 + \text{angle } (Ip' - Ip0')$$

where:

D1 = A SCALAR factor - assuming that the power system is homogeneous

$$= (Zsp1 + Zl1 + Zsq1) / ((1-m)Zl1 + Zsq1)$$

The angle of D1 depends upon the fault position but for the purposes of this algorithm this angle is assumed to be zero.

Thus:

$$\text{angle } If = d = \text{angle } (Ip' - Ip0')$$

The equation above, shows that the phase angle of the fault current d can be estimated from the superimposed phase and neutral currents measured at the relay terminals.

therefore for an earth fault:

$$|If|(\cos(d) + j\sin(d))$$
$$= kD1(Ip'-Ip0')$$
$$= kD1[(Ia(fault) - Ia(prefault))$$
$$- 0.33(In(fault) - In(prefault))]$$

where:

k is a scalar factor and d is the required phase angle of If at the instant of time that the faulted vectors are calculated.

similarly, for a phase to phase fault:

$$|If|\ (\cos(d) + j\sin(d)) = kD1[(Ia(fault) - Ia(prefault))- (Ib(fault) - Ib(prefault))]$$

Thus, using the calculated pre-fault and faulted vectors the fault locator is able to calculate the angle of the fault current vector d at the instant of time that the faulted vectors are calculated.

13.4.3.3 DATA ACQUISITION AND BUFFER PROCESSING

The fault locator stores the sampled data within a 12 cycle cyclic buffer at a resolution of 48 samples per cycle. When the fault recorder is triggered the data in the buffer is frozen such that the buffer contains 6 cycles of pre-trigger data and 6 cycles of post-trigger data. Fault calculation commences shortly after this trigger point.

The trigger for the fault recorder is user selectable via the programmable scheme logic.

The fault locator can store data for up to four faults. This ensures that fault location can be calculated for all shots on a typical multiple reclose sequence.

13.4.3.4 FAULTED PHASE SELECTION

Phase selection is derived from the superimposed current phase selector.

Phase selection and fault location calculations can only be made if the current change exceeds 5% In.

13.4.3.5 FAULTED PHASE CALCULATION

The fault location calculation works by:

1. First obtaining the vectors
2. Selecting the faulted phase(s)
3. Estimating the phase of the fault current If for the faulted phase(s)
4. Solving the below equation for the fault location m at the instant of time where f = 0

$$Vp = mIpZr + IfRf$$

13.4.3.6 DISTANCE TO FAULT CALCULATION

Replica impedance Zr

The fault location calculation needs vectors derived from the line voltage (Vp) and from the relay's "replica impedance" voltage (IpZr) under fault conditions. The replica impedance is derived from the relay settings and is effectively set to the same value as the total line impedance. i.e.

$$Zr = Zline / \theta\ line + Zresidual / / \theta\ residual$$

This "replica impedance" is modified using the mutual compensation factor when the mutual compensation feature is used. i.e.

$$Zr = Zline / \theta\ line + Zresidual / / \theta\ residual + Zmutual / / \theta\ mutual$$

Where :

$$Zresidual = kZN*Zline$$
$$Zmutual = kZm*Zline$$

The fault location calculation

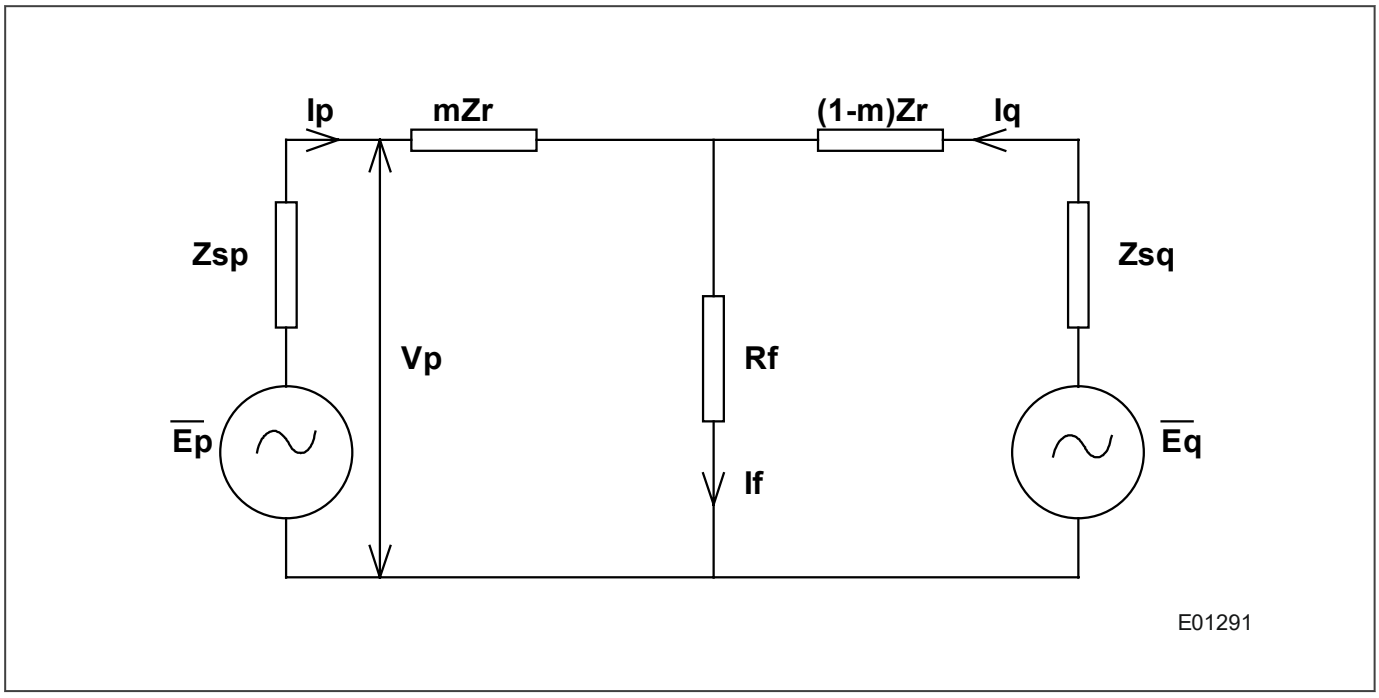


Figure 175: Two machine equivalent circuit

Fault location equation:

$$Vp = mIpZr + IfRf$$

Referring to the figure and equation, above.

The fault location calculation works by:

1. First obtaining the vectors to satisfy the above equation for the fault type specified by the phase selector.
2. Then estimating the phase of the fault current If.
3. Finally solving the above equation for the fault location m at the instant of time where If = 0.

Obtaining the vectors

Different sets of vectors are chosen depending on the type of fault identified by the phase selection algorithm. The calculation using fault location equation, above is applied for either a phase to earth fault or a phase to phase fault.

Thus, for a A phase to earth fault:

$$IpZr = Ia\ (Zline / \theta\ line) + In\ (Zresidual / / \theta\ residual)$$

and

$$Vp = VA$$

And for a A phase to B phase fault:

$$IpZr = Ia\ (\ Zline / \theta\ line\ ) - Ib\ (Zline / \theta\ line)$$

and

$$Vp = VA - VB$$

The calculation for an earth fault (A phase to earth fault equation, above) is modified when mutual compensation is used :

$$IpZr = Ia\ (Zline / \theta\ line) + In(Zresidual / / \theta\ residual\ ) + Im(Zmutual / / \theta\ mutual)$$

Solving the equation for the fault location

As the sine wave of If passes through zero, the instantaneous values of the sine waves Vp and □p can be used to solve the below equation for the fault location m. (The term IfRf being zero).

$$Vp = mIpZr + IfRf$$

This is determined by shifting the calculated vectors of Vp and IpZr by the angle (90° - angle of fault current) and then dividing the real component of Vp by the real component of IpZr. (See figure, below).

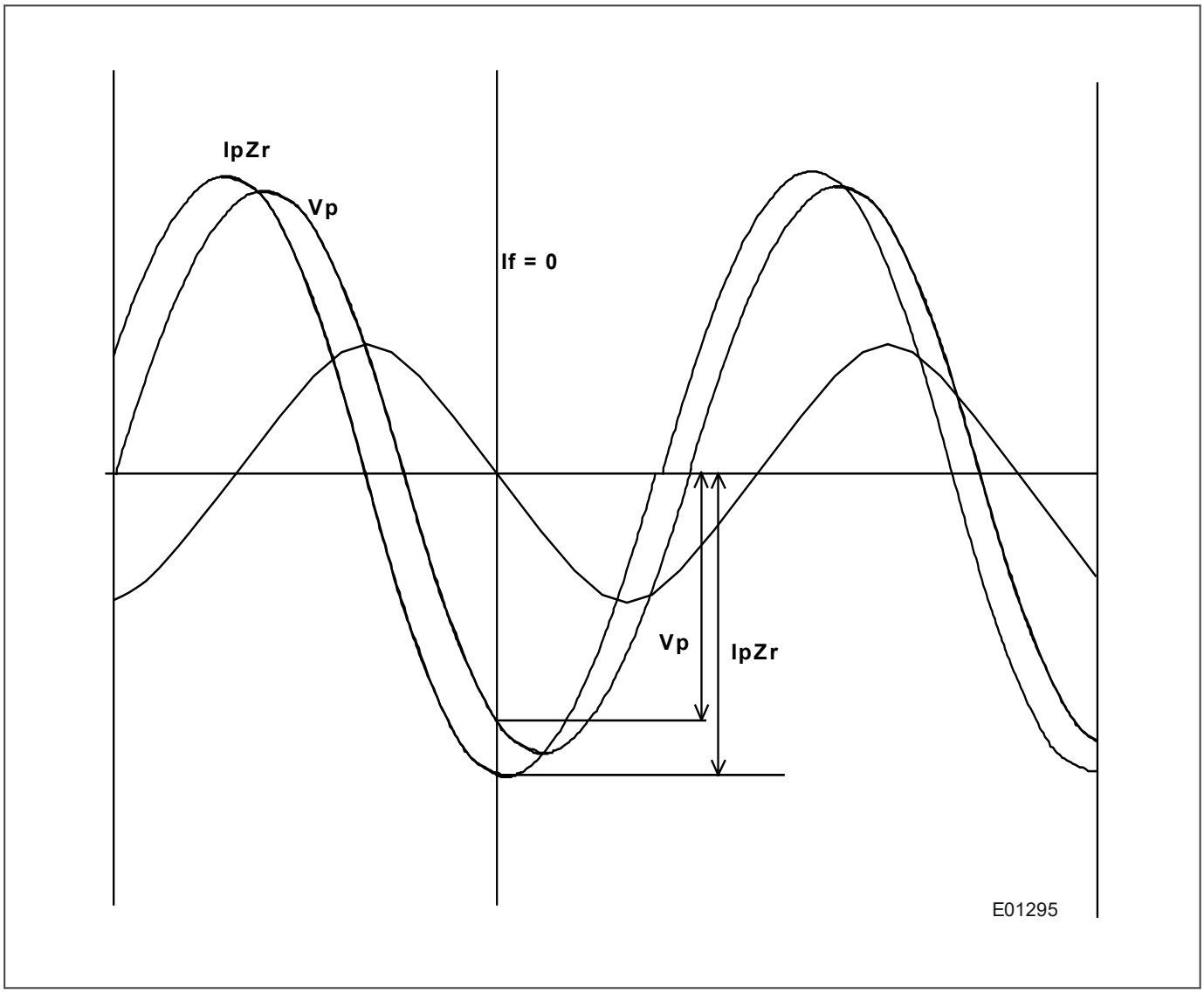


Figure 176: Fault locator selection of fault current zero

i.e.:

Phase advanced vector Vp

$$= |Vp| [\cos(s) + j\sin(s)] * [\sin(d) + j\cos(d)]$$

$$= |Vp| [-\sin(s-d) + j\cos(s-d)]$$

Phase advanced vector IpZr

$$= ||pZr| [\cos(e) + j\sin(e)] * [\sin(d) + j\cos(d)]$$

$$= ||pZr| [-\sin(e-d) + j\cos(e-d)]$$

Therefore, from equation 1:

$$m = Vp \div (Ip * Zr) \text{ at } If = 0$$

$$= Vp \sin(s-d)/(IpZr * \sin(e-d))$$

Where:

d = Angle of fault current If

s = Angle of Vp

e = Angle of IpZr

Thus, the relay evaluates m which is the fault location as a percentage of the fault locator line impedance setting and then calculates the output fault location by multiplying this by the line length setting. When calculated the fault location can be found in the fault record under the *VIEW RECORDS* column in the ***Fault Location*** cells. Distance to fault is available in kilometers, miles, impedance or percentage of line length.

13.4.3.7 MUTUAL COMPENSATION

Analysis of a ground fault on one circuit of a parallel over-head line shows that a fault locator positioned at one end of the faulty line will tend to over-reach while that at the other end will tend to under-reach. In cases of long lines with high mutual inductance, mutual zero sequence compensation can be used to improve the fault locator accuracy. The compensation is achieved by taking an input to the relay from the residual circuit of the current transformers in the parallel line.

The 5th Generation provides mutual compensation for both the fault locator function, AND the distance protection zones.

13.4.3.8 METERING

The metering calculations are continuously performed using the same fourier technique used by the fault locator. The results of these calculations are continuously updated and can be viewed using the relay user interface.

13.4.4 OPTO-INPUT TIME STAMPING

Each opto-input sample is time stamped within a tolerance of +/- 1 ms with respect to the Real Time Clock. These time stamps are used for the opto event logs and for the disturbance recording. The device needs to be synchronised accurately to an external clock source such as an IRIG-B signal or a master clock signal provided in the relevant data protocol.

For both the filtered and unfiltered opto-inputs, the time stamp of an opto-input change event is the sampling time at which the change of state occurred. If multiple opto-inputs change state at the same sampling interval, these state changes are reported as a single event.

13.5 CB CONDITION MONITORING

The device records various statistics related to each circuit breaker trip operation, allowing an accurate assessment of the circuit breaker condition to be determined. These statistics are available in the *CB CONDITION* column. The menu cells are register values only and cannot be set directly. They may be reset, however, during maintenance. The statistics monitored are:

- Total Current Broken: A register stores the total amount of current that the CB has broken is stored in an accumulator, giving at any time a measure of the total amount of current that the CB has broken since the value was last reset.
- Number of CB operations: A counter registers the number of CB trips that have been performed for each phase, giving at any time the total number of trips that the CB has performed since the value was last reset.
- CB Operate Time: A register stores the total amount of time the CB has transitioned from closed to open is stored in an accumulator, giving at any time a measure of the total time that the CB has spent tripping since the values was last reset.
- Excessive Fault Frequency: A counter registers the number of CB trips that have been performed for all phases, giving at any time the total number of trips performed since the value was last reset.

These statistics are available in the *CB CONDITION* column. The menu cells are register values only and cannot be set directly. They may be reset, however, during maintenance.

> *Note:*
> *When in Commissioning test mode the CB condition monitoring registers are not updated.*

Circuit breaker lockout, can be caused by the following circuit breaker condition monitoring functions:

- Maintenance lockout
- Excessive fault frequency lockout
- Broken current lockout

If the circuit breaker is locked out, the logic generates a lockout alarm

13.5.1 BROKEN CURRENT ACCUMULATOR

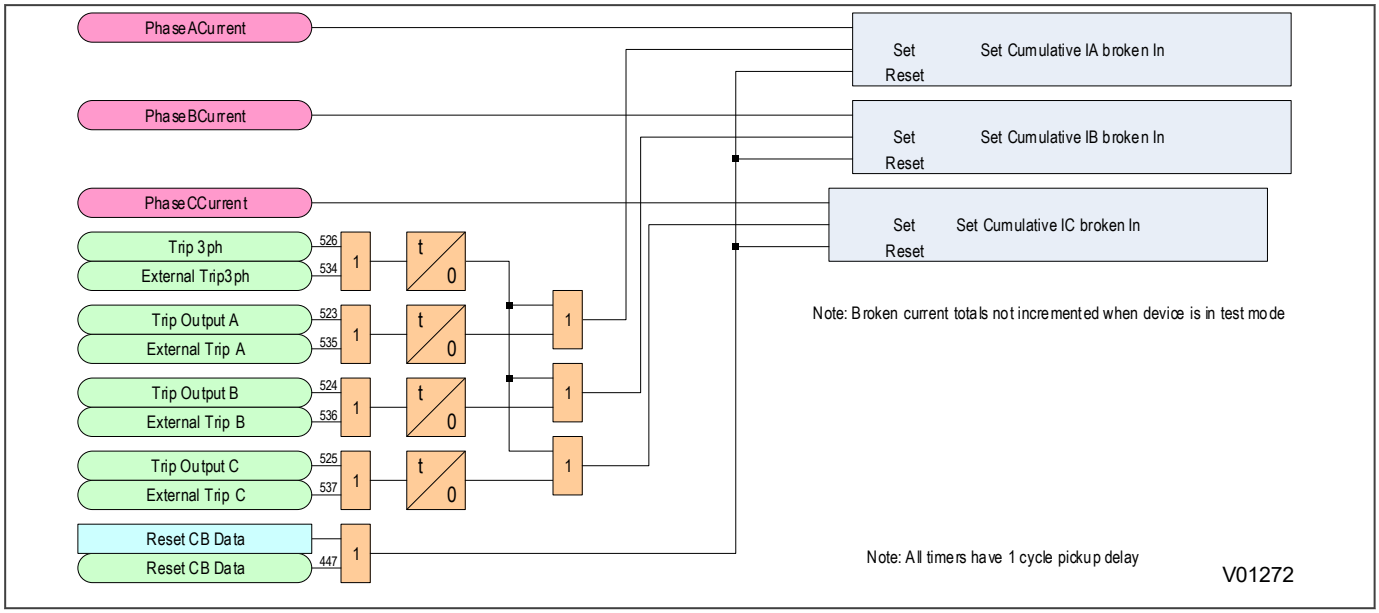


Figure 177: Broken Current Accumulator logic diagram

13.5.2 BROKEN CURRENT ACCUMULATOR

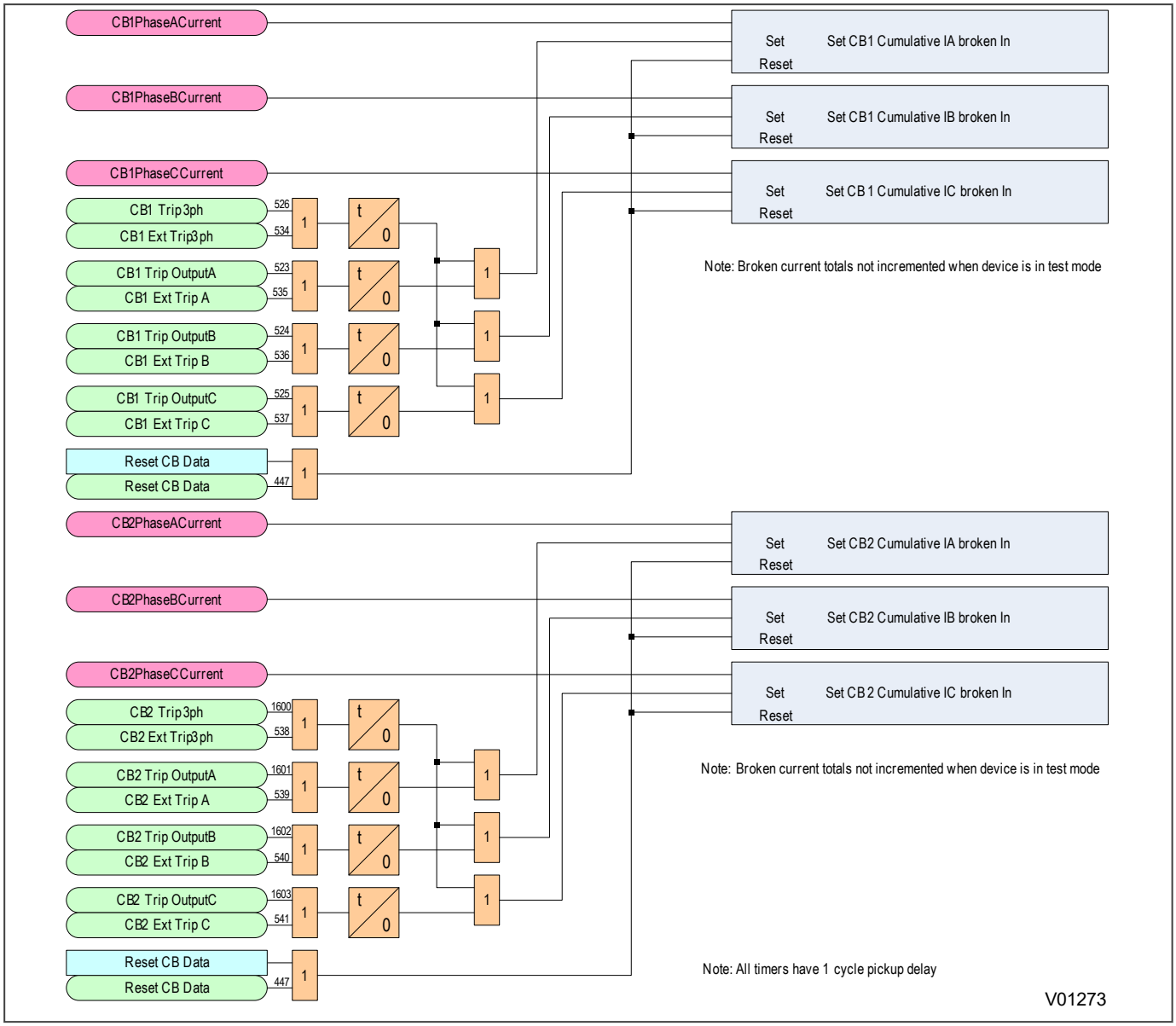


Figure 178: Broken Current Accumulator logic diagram

13.5.3 CB TRIP COUNTER

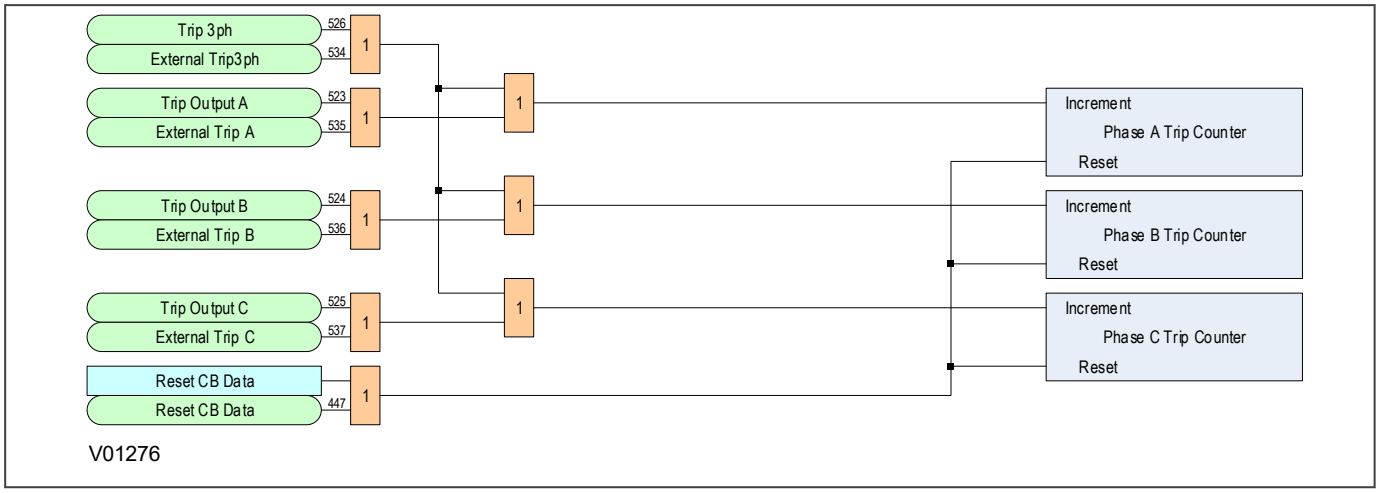


Figure 179: CB Trip Counter logic diagram

13.5.4 CB TRIP COUNTER

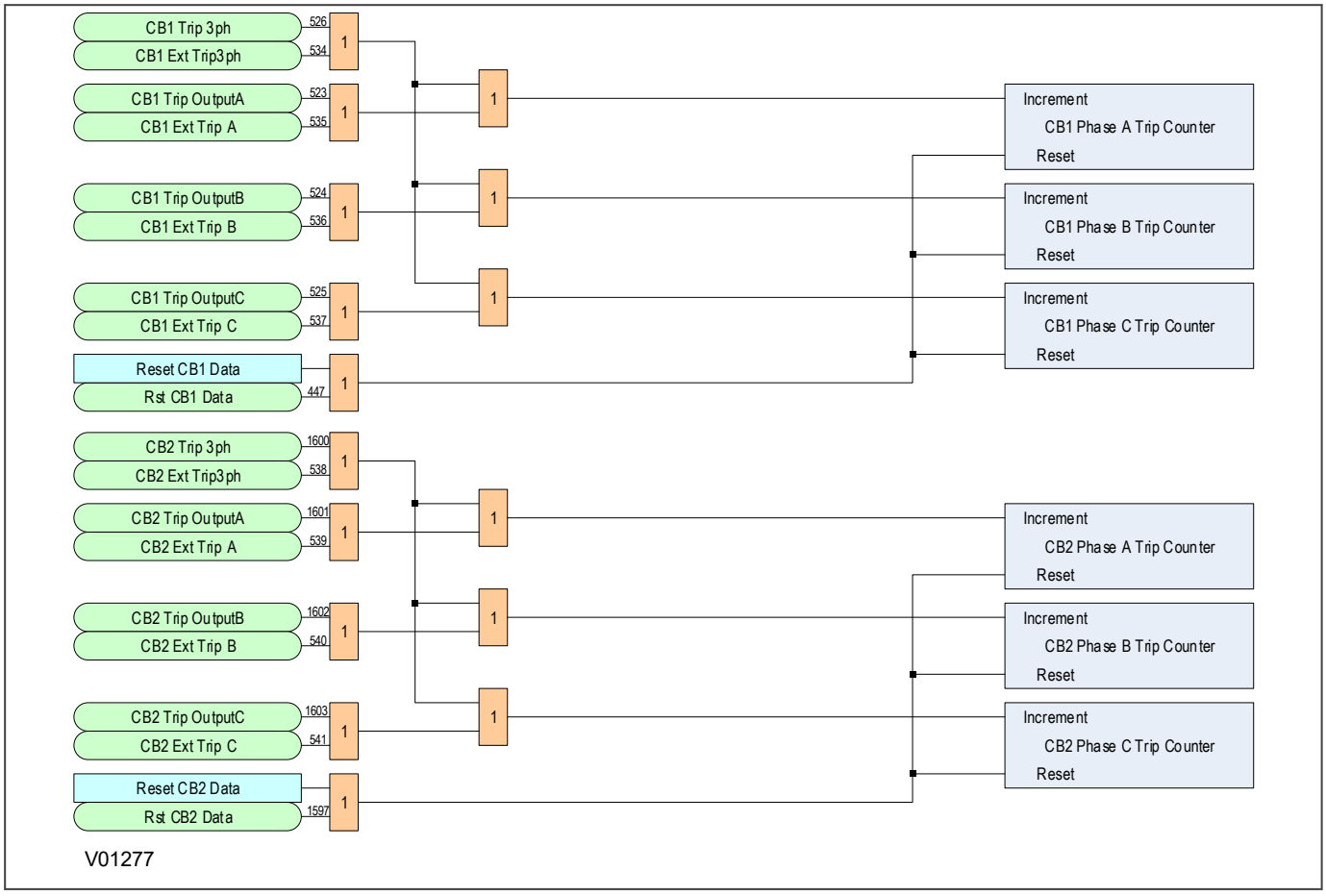


Figure 180: CB Trip Counter logic diagram

13.5.5 CB OPERATING TIME ACCUMULATOR

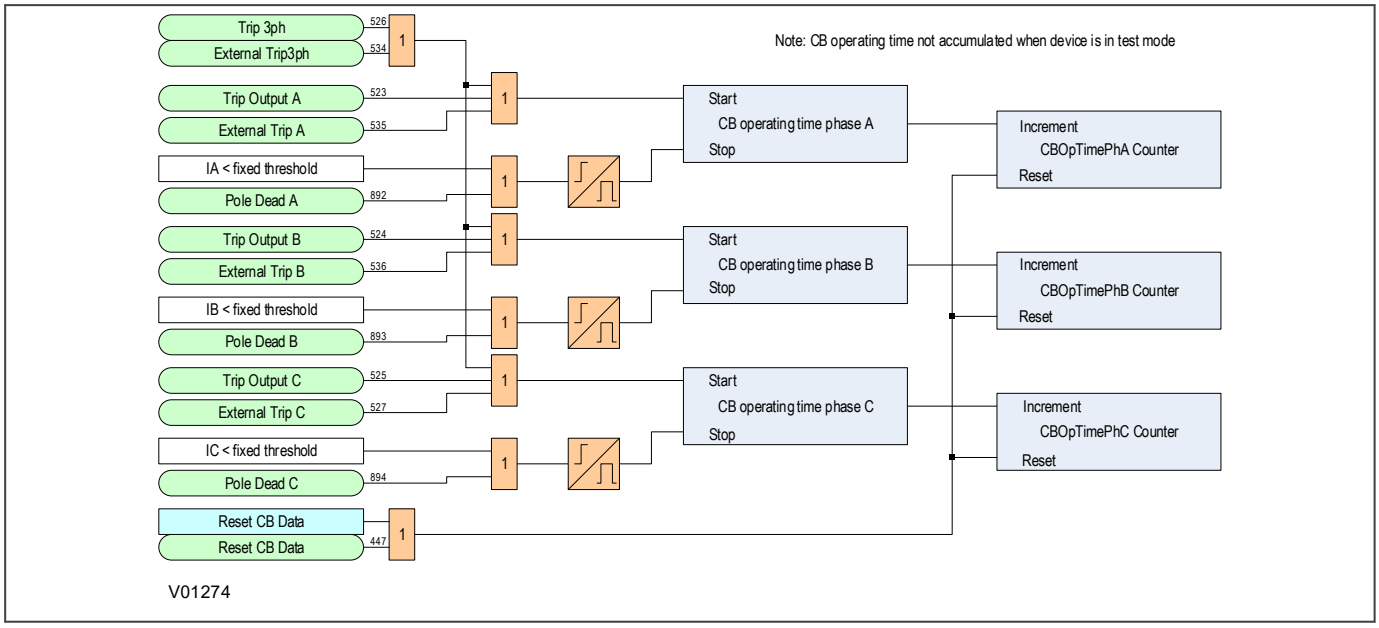


Figure 181: Operating Time Accumulator

13.5.6 CB OPERATING TIME ACCUMULATOR

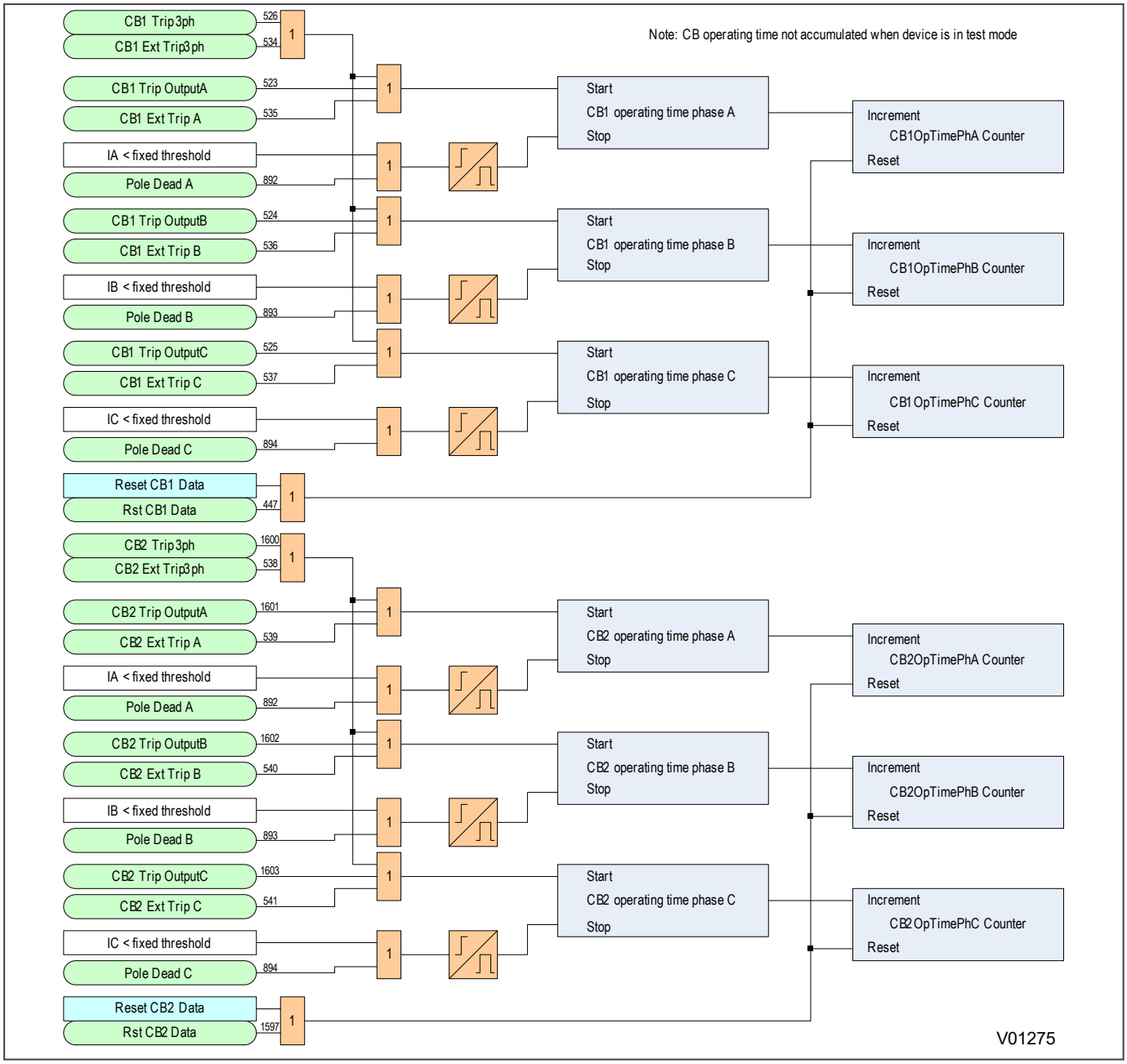


Figure 182: Operating Time Accumulator

13.5.7 EXCESSIVE FAULT FREQUENCY COUNTER

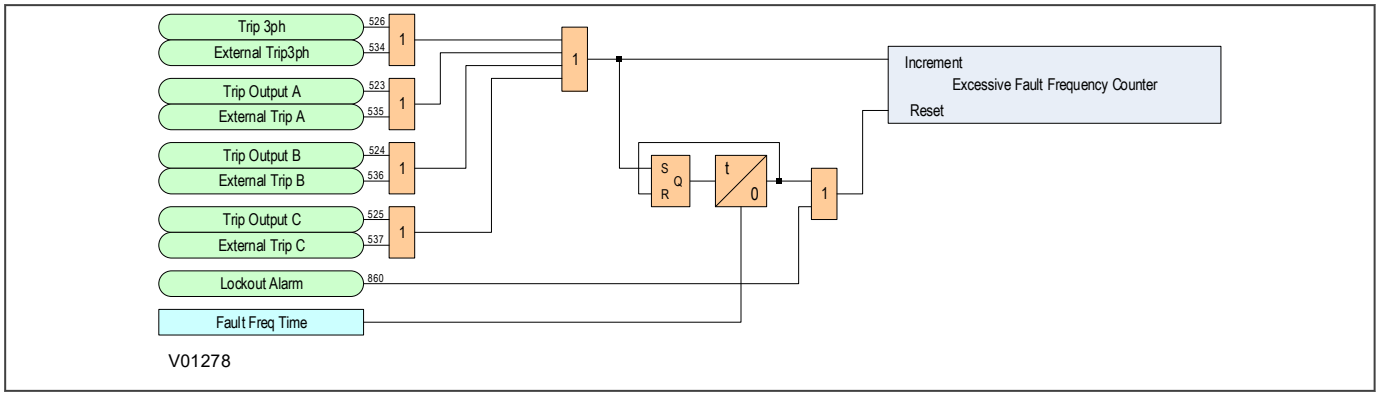


Figure 183: Excessive Fault Frequency logic diagram

13.5.8 EXCESSIVE FAULT FREQUENCY COUNTER

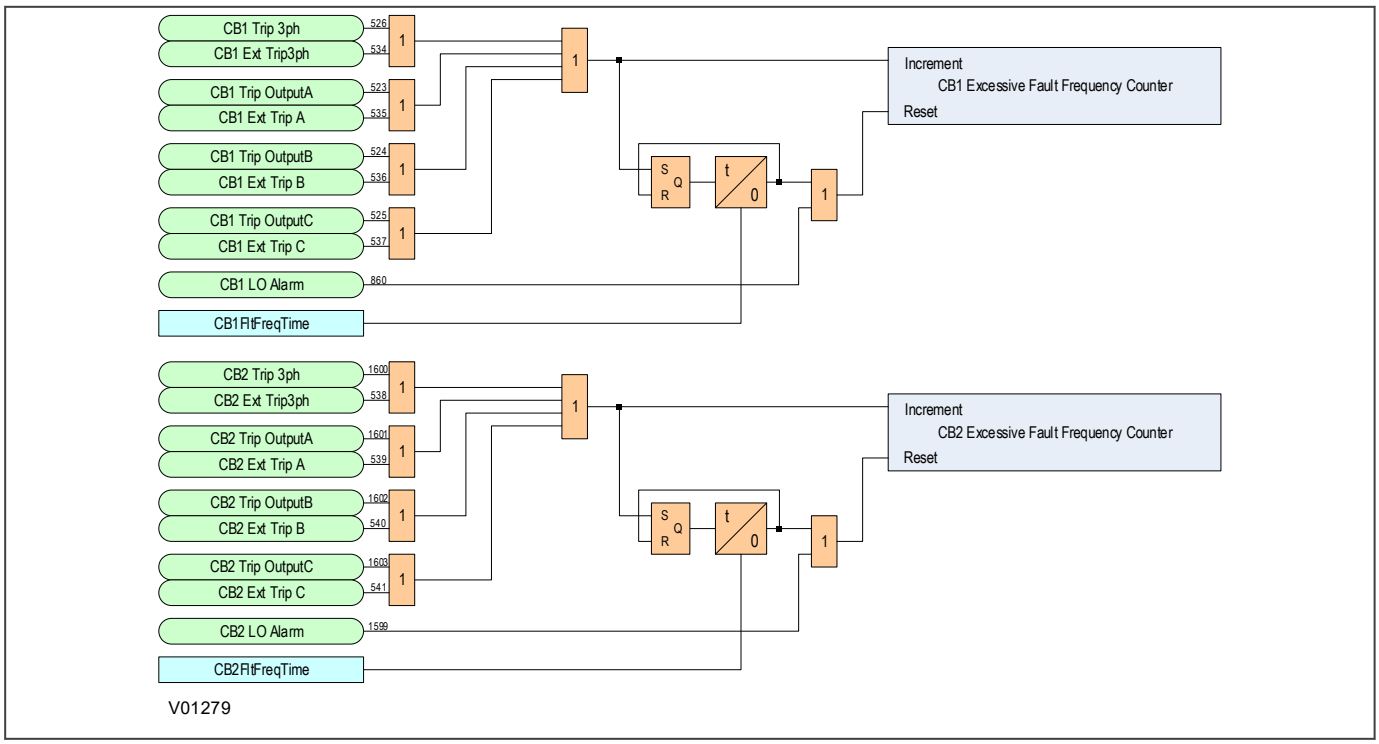


Figure 184: Excessive Fault Frequency logic diagram

13.5.9 RESET LOCKOUT ALARM

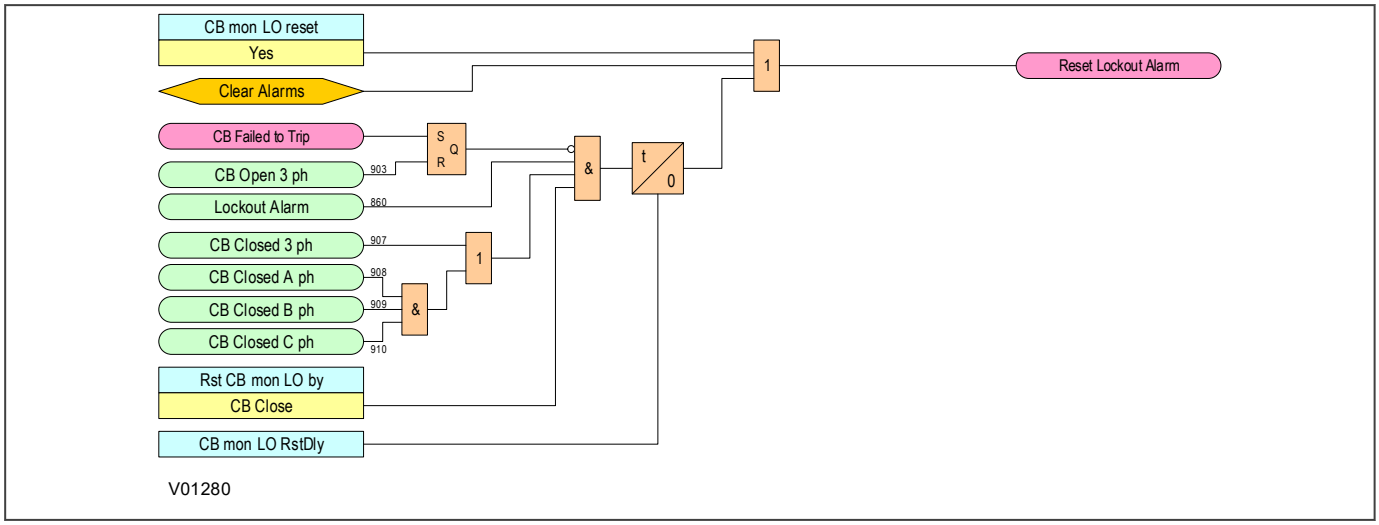


Figure 185: Reset Lockout Alarm logic diagram

13.5.10 RESET LOCKOUT ALARM

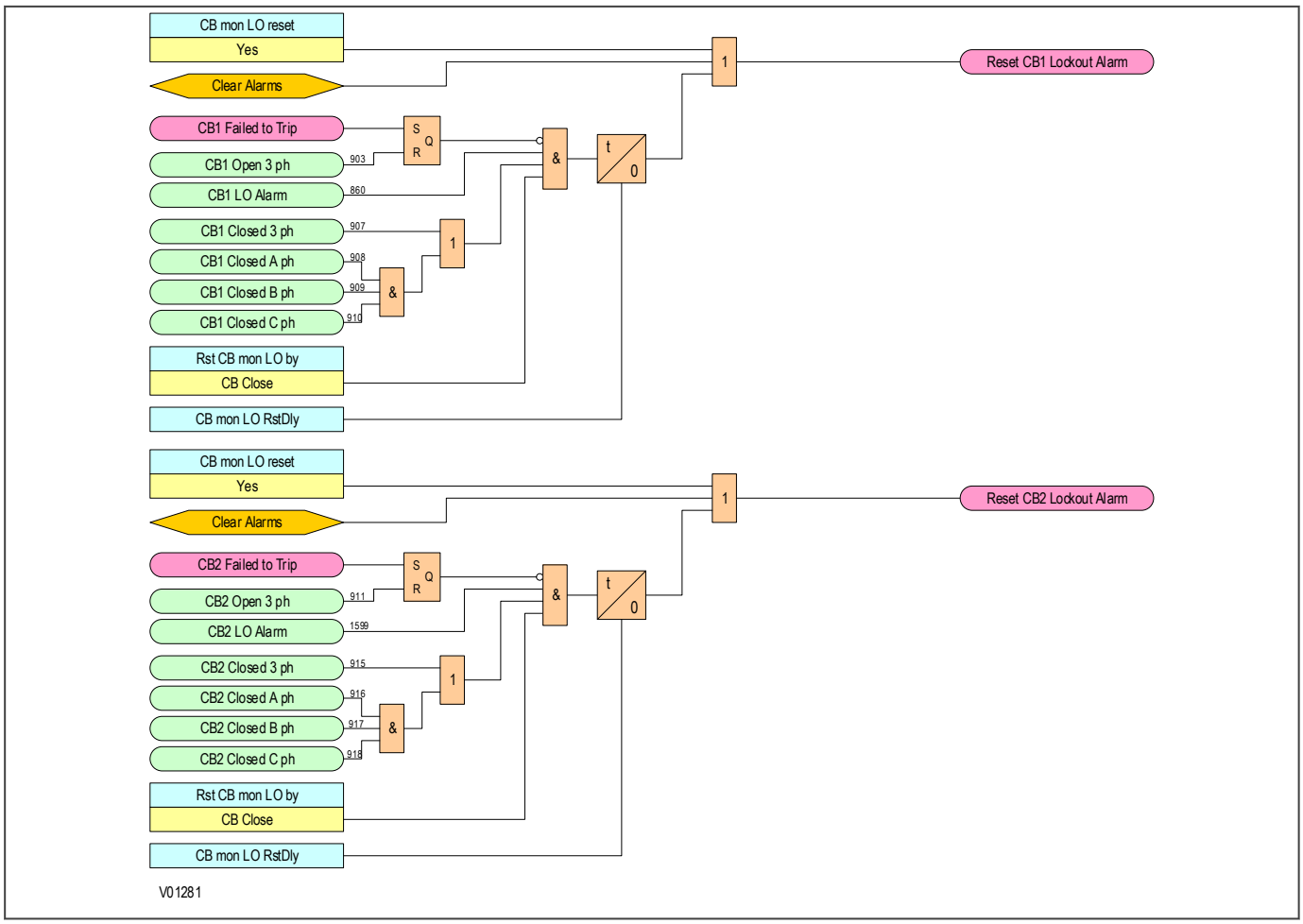


Figure 186: Reset Lockout Alarm logic diagram

13.5.11 CB CONDITION MONITORING LOGIC

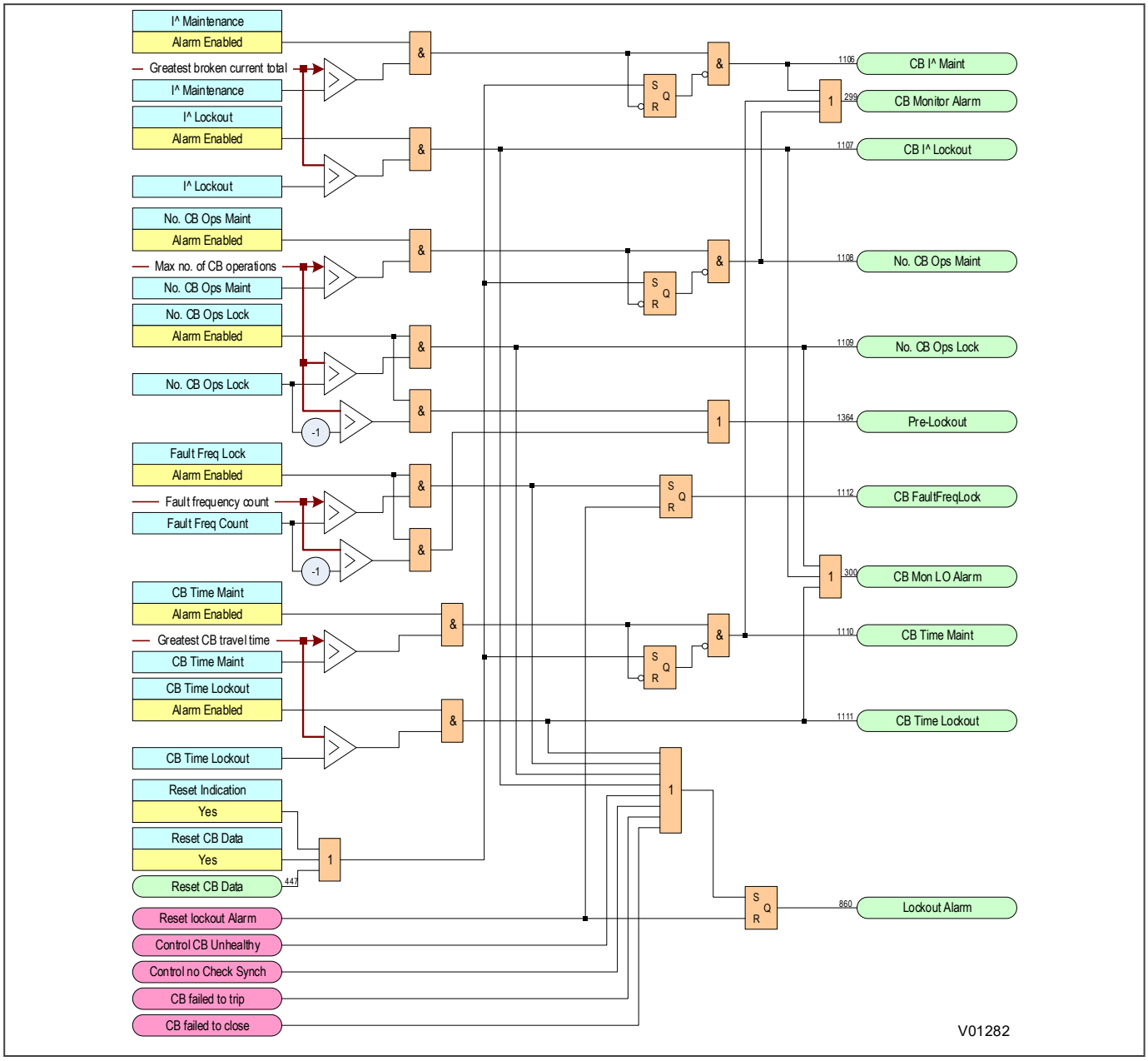


Figure 187: CB Condition Monitoring logic diagram

13.5.12 CB CONDITION MONITORING LOGIC

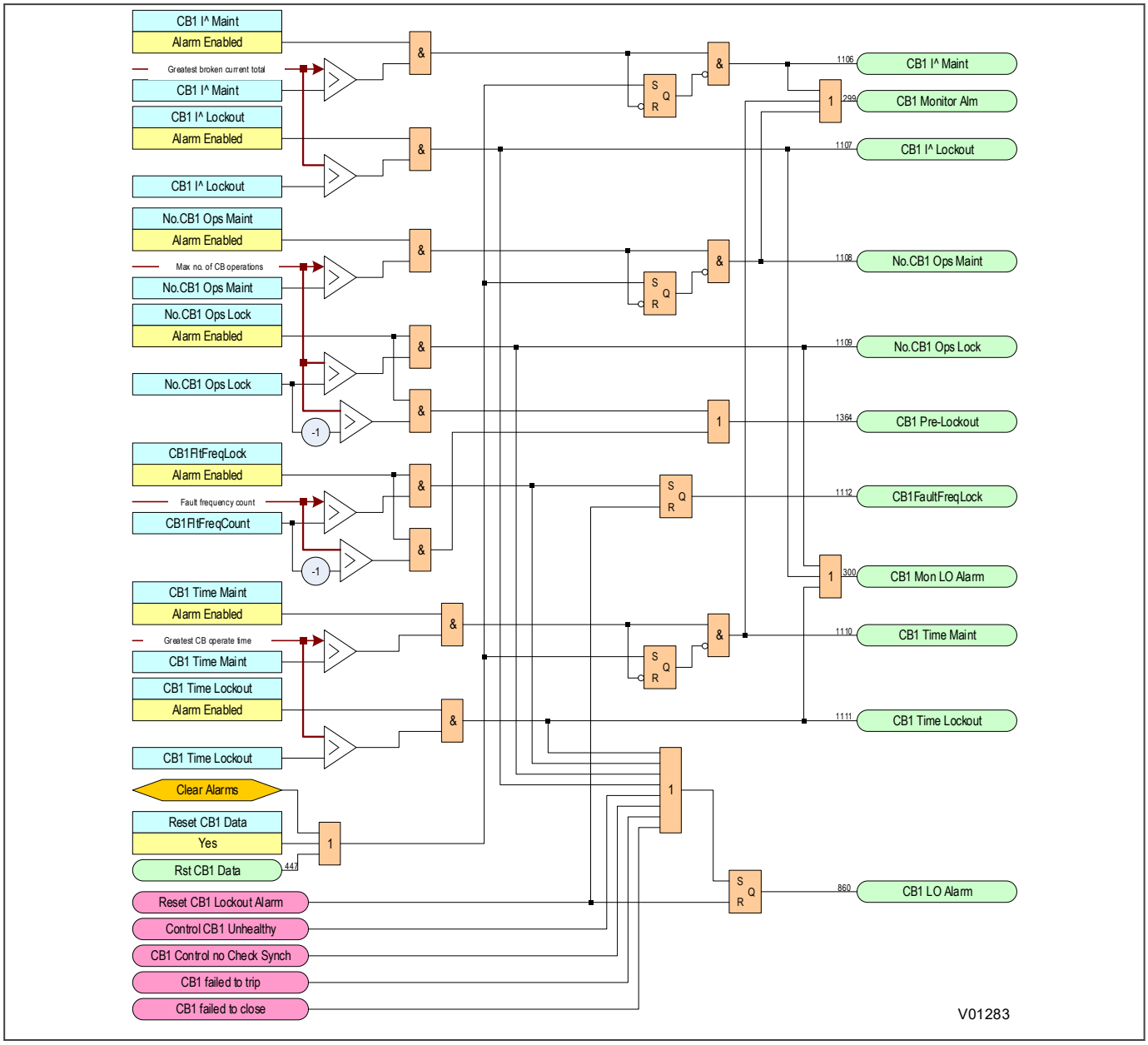


Figure 188: CB1 Condition Monitoring logic diagram

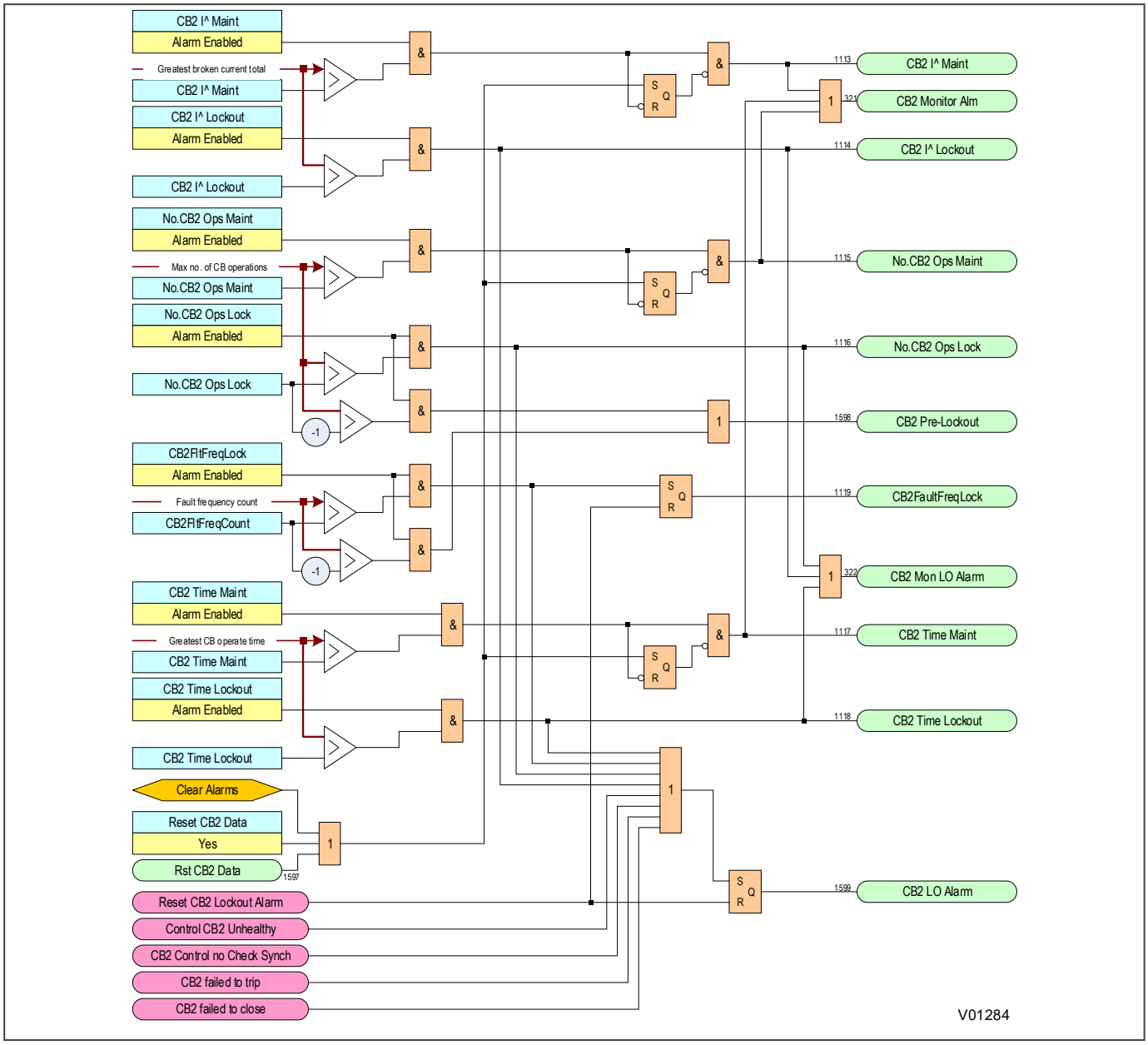


Figure 189: CB2 Condition Monitoring logic diagram

13.5.13 RESET CIRCUIT BREAKER LOCKOUT

Lockout conditions caused by the circuit breaker condition monitoring functions can be reset according to the condition of the ***Rst CB mon LO*** by setting found in the *CB CONTROL* column. There are two options; `CB Close` and `User interface`.

If set to `CB Close`, a timer setting, ***CB mon LO RstDly***, becomes visible. When the circuit breaker closes, the ***CB mon LO RstDly*** time starts. The lockout is reset when the timer expires.

If set to `User Interface` then a command, ***CB mon LO reset***, becomes visible. This command can be used to reset the lockout from a user interface.

An Autoreclose lockout generates an Autoreclose lockout alarm. Autoreclose lockout conditions can be reset by various commands and setting options found under the *CB CONTROL* column.

If ***Res LO by CB IS*** is set to *Enabled*, a lockout is reset if the circuit breaker is successfully closed manually. For this, the circuit breaker must remain closed long enough so that it enters the “In Service” state.

If ***Res LO by UI*** is set to *Enabled*, the circuit breaker lockout can be reset from a user interface using the reset circuit breaker lockout command in the *CB CONTROL* column.

If ***Res LO by NoAR*** is set to *Enabled*, the circuit breaker lockout can be reset by temporarily generating an ***AR disabled*** signal.

If ***Res LO by TDelay*** is set to *Enabled*, the circuit breaker lockout is automatically reset after a time delay set in the ***LO Reset Time*** setting.

If ***Res LO by ExtDDB*** is *Enabled*, the circuit breaker lockout can be reset by activation of an external input mapped in the PSL to the relevant reset lockout DDB signal.

13.5.13.1 RESET CB LOCKOUT LOGIC DIAGRAM

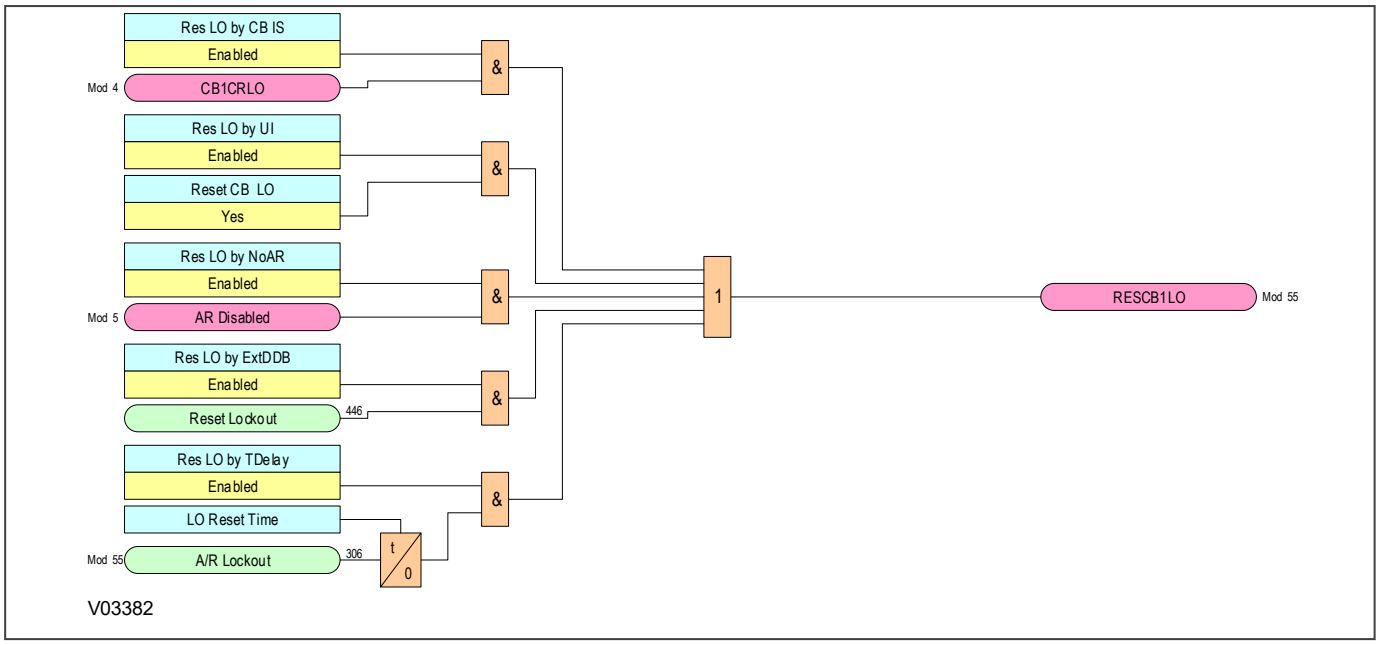


Figure 190: Reset Circuit Breaker Lockout Logic Diagram (Module 57)

13.5.13.2 RESET CB LOCKOUT LOGIC DIAGRAM

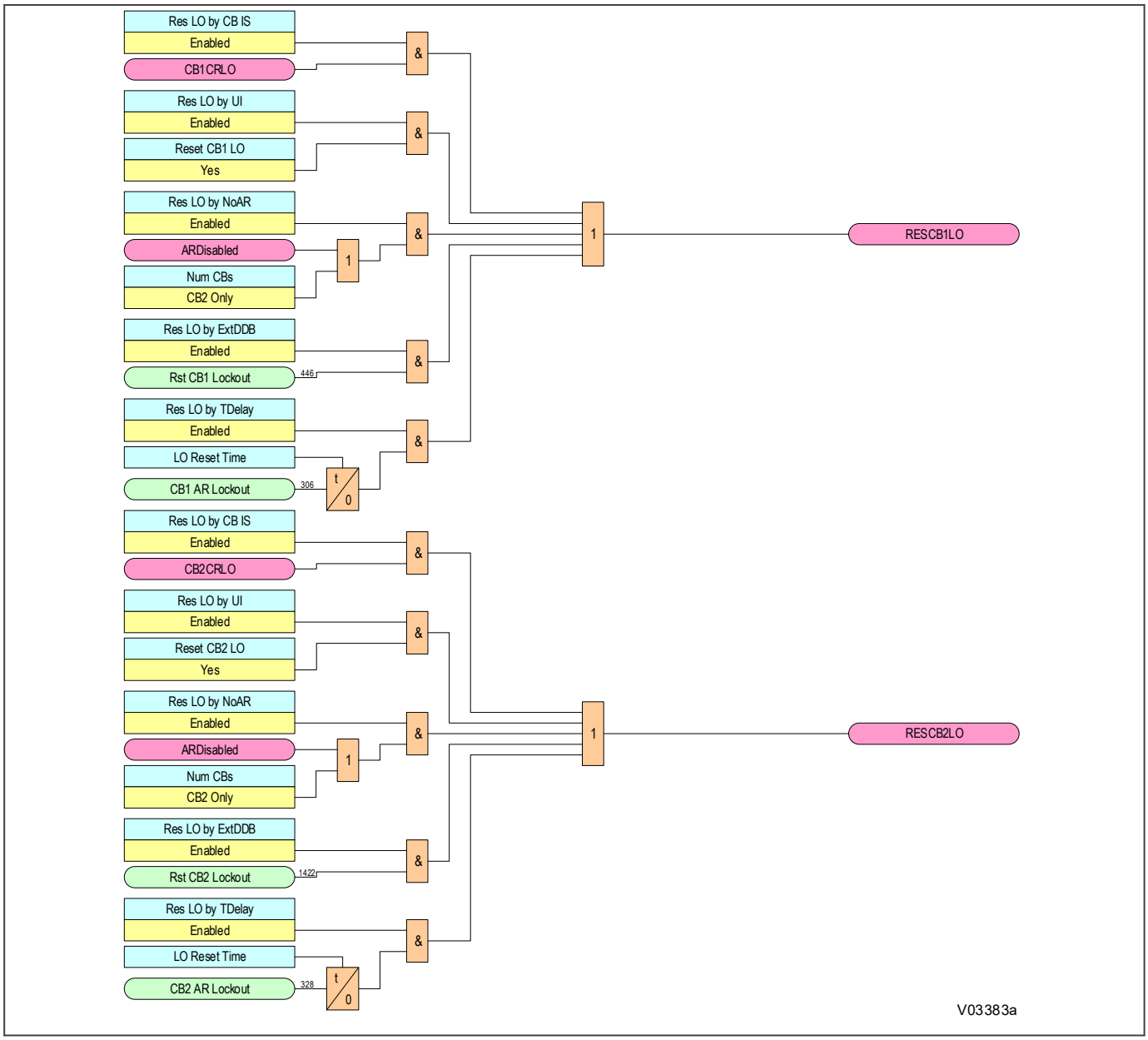


Figure 191: Reset Circuit Breaker Lockout Logic Diagram (Modules 57 & 58)

13.5.14 APPLICATION NOTES

13.5.14.1 SETTING THE THRESHOLDS FOR THE TOTAL BROKEN CURRENT

Where power lines use oil circuit breakers (OCBs), changing of the oil accounts for a significant proportion of the switchgear maintenance costs. Often, oil changes are performed after a fixed number of CB fault operations. However, this may result in premature maintenance where fault currents tend to be low, because oil degradation may be slower than would normally be expected. The Total Current Accumulator (I^ counter) cumulatively stores the total value of the current broken by the circuit breaker providing a more accurate assessment of the circuit breaker condition.

The dielectric withstand of the oil generally decreases as a function of I^2t, where 'I' is the broken fault current and 't' is the arcing time within the interrupter tank. The arcing time cannot be determined accurately, but is generally

dependent on the type of circuit breaker being used. Instead, you set a factor (***Broken I^***) with a value between 1 and 2, depending on the circuit breaker.

Most circuit breakers would have this value set to '2', but for some types of circuit breaker, especially those operating on higher voltage systems, a value of 2 may be too high. In such applications ***Broken I^*** may be set lower, typically 1.4 or 1.5.

The setting range for ***Broken I^*** is variable between 1.0 and 2.0 in 0.1 steps.

Note:
Any maintenance program must be fully compliant with the switchgear manufacturer's instructions.

13.5.14.2 SETTING THE THRESHOLDS FOR THE NUMBER OF OPERATIONS

Every circuit breaker operation results in some degree of wear for its components. Therefore routine maintenance, such as oiling of mechanisms, may be based on the number of operations. Suitable setting of the maintenance threshold will allow an alarm to be raised, indicating when preventative maintenance is due. Should maintenance not be carried out, the device can be set to lockout the autoreclose function on reaching a second operations threshold (***No. CB ops Lock***). This prevents further reclosure when the circuit breaker has not been maintained to the standard demanded by the switchgear manufacturer's maintenance instructions.

Some circuit breakers, such as oil circuit breakers (OCBs) can only perform a certain number of fault interruptions before requiring maintenance attention. This is because each fault interruption causes carbonising of the oil, degrading its dielectric properties. The maintenance alarm threshold (setting ***No. CB Ops Maint***) may be set to indicate the requirement for oil dielectric testing, or for more comprehensive maintenance. Again, the lockout threshold ***No. CB Ops Lock*** may be set to disable autoreclosure when repeated further fault interruptions could not be guaranteed. This minimises the risk of oil fires or explosion.

13.5.14.3 SETTING THE THRESHOLDS FOR THE OPERATING TIME

Slow CB operation indicates the need for mechanism maintenance. Alarm and lockout thresholds (***CB Time Maint*** and ***CB Time Lockout***) are provided to enforce this. They can be set in the range of 5 to 500 ms. This time relates to the interrupting time of the circuit breaker.

13.5.14.4 SETTING THE THRESHOLDS FOR EXCESSSIVE FAULT FREQUENCY

Persistent faults will generally cause autoreclose lockout, with subsequent maintenance attention. Intermittent faults such as clashing vegetation may repeat outside of any reclaim time, and the common cause might never be investigated. For this reason it is possible to set a frequent operations counter, which allows the number of operations ***Fault Freq Count*** over a set time period ***Fault Freq Time*** to be monitored. A separate alarm and lockout threshold can be set.

13.6 CB STATE MONITORING

CB State monitoring is used to verify the open or closed state of a circuit breaker. Most circuit breakers have auxiliary contacts through which they transmit their status (open or closed) to control equipment such as IEDs. These auxiliary contacts are known as:

- 52A for contacts that follow the state of the CB
- 52B for contacts that are in opposition to the state of the CB

This device can be set to monitor both of these types of circuit breaker state indication. If the state is unknown for some reason, an alarm can be raised.

Some CBs provide both sets of contacts. If this is the case, these contacts will normally be in opposite states. Should both sets of contacts be open, this would indicate one of the following conditions:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective
- CB is in isolated position

Should both sets of contacts be closed, only one of the following two conditions would apply:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective

If any of the above conditions exist, an alarm will be issued after a 5 s ***CB Status Time*** time delay. An output contact can be assigned to this function via the programmable scheme logic (PSL). The time delay is set to avoid unwanted operation during normal switching duties.

In the CB CONTROL column there is a setting called ***CB Status Input***. This cell can be set at one of the following four options:

- None
- 52A
- 52B
- Both 52A and 52B

Where `None` is selected no CB status is available. Where only 52A is used on its own then the device will assume a 52B signal opposite to the 52A signal. Circuit breaker status information will be available in this case but no discrepancy alarm will be available. The above is also true where only a 52B is used. If both 52A and 52B are used then status information will be available and in addition a discrepancy alarm will be possible, according to the following table:

Auxiliary Contact Position		CB State Detected	Action
52A	52B		
Open	Closed	Breaker open	Circuit breaker healthy
Closed	Open	Breaker closed	Circuit breaker healthy
Closed	Closed	CB failure	Alarm raised if the condition persists for greater than 5 s
Open	Open	State unknown	Alarm raised if the condition persists for greater than 5 s. ***CB State Detected*** becomes ***CB Failure***.

In the internal logic of the P40, the breaker position used in the algorithm is considered to be open when the **CB State Detected is Breaker Open**. In all other cases, the breaker position is considered to be closed. Therefore, during operation of the circuit breaker, if the condition '52A=52B=0' or '52A=52B=1' is encountered, the circuit breaker is considered to be closed.

The Circuit Breaker status can be monitored in the serial and Ethernet data protocols. For example, IEC 60870-5-103, DNP 3.0 and IEC 61850.

IEC 60870-5-103 protocol: The CB status can be monitored from individual private information numbers.

DNP 3.0 protocol: The CB status can be monitored from individual Binary Inputs.

IEC 61850 protocol: The CB status can be monitored in ‘XCBR’ Logical Node(s).

13.6.1 CB STATE MONITOR LOGIC DIAGRAM

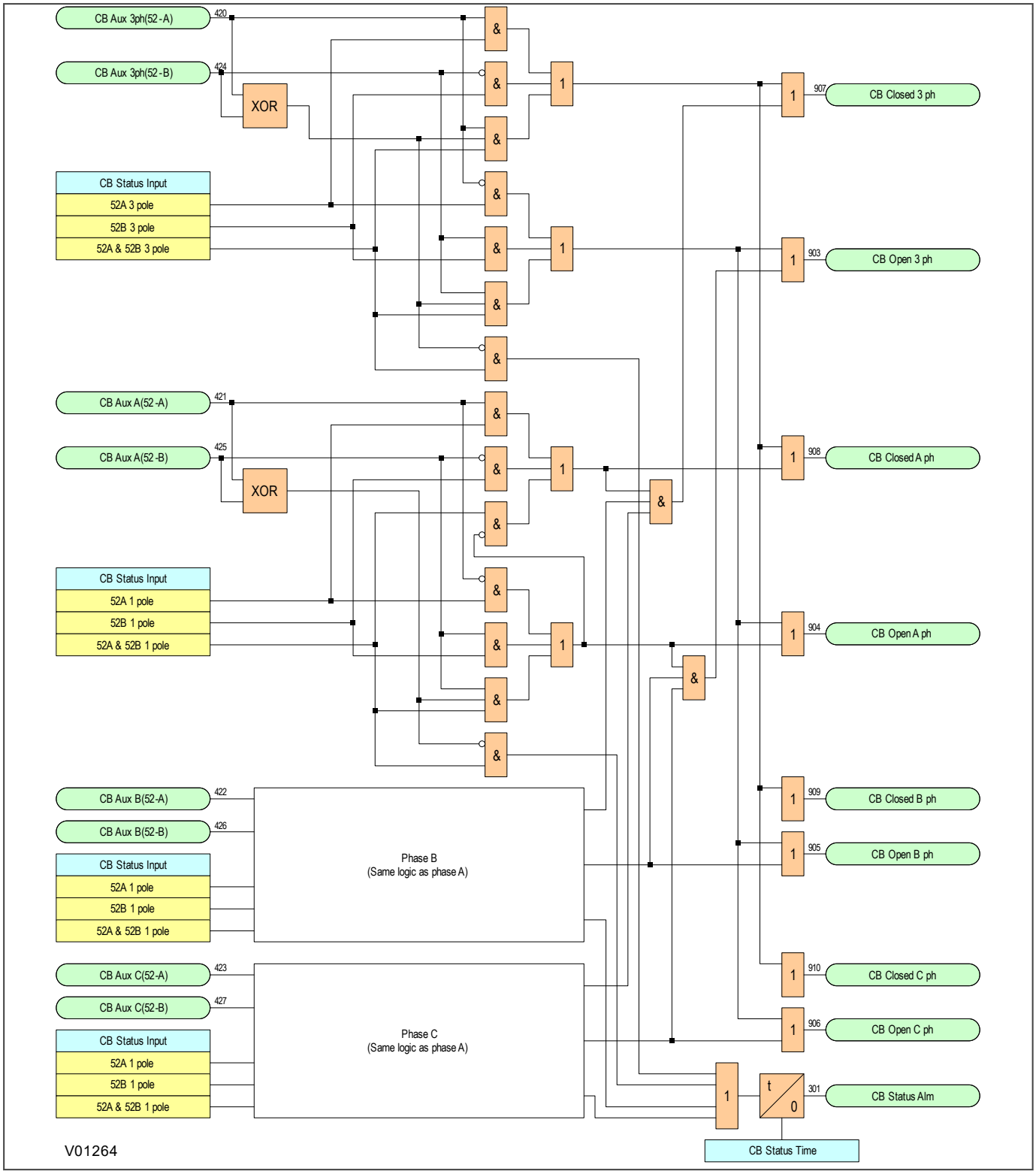


Figure 192: CB State Monitor logic diagram (Module 1)

13.6.2 CB STATE MONITOR

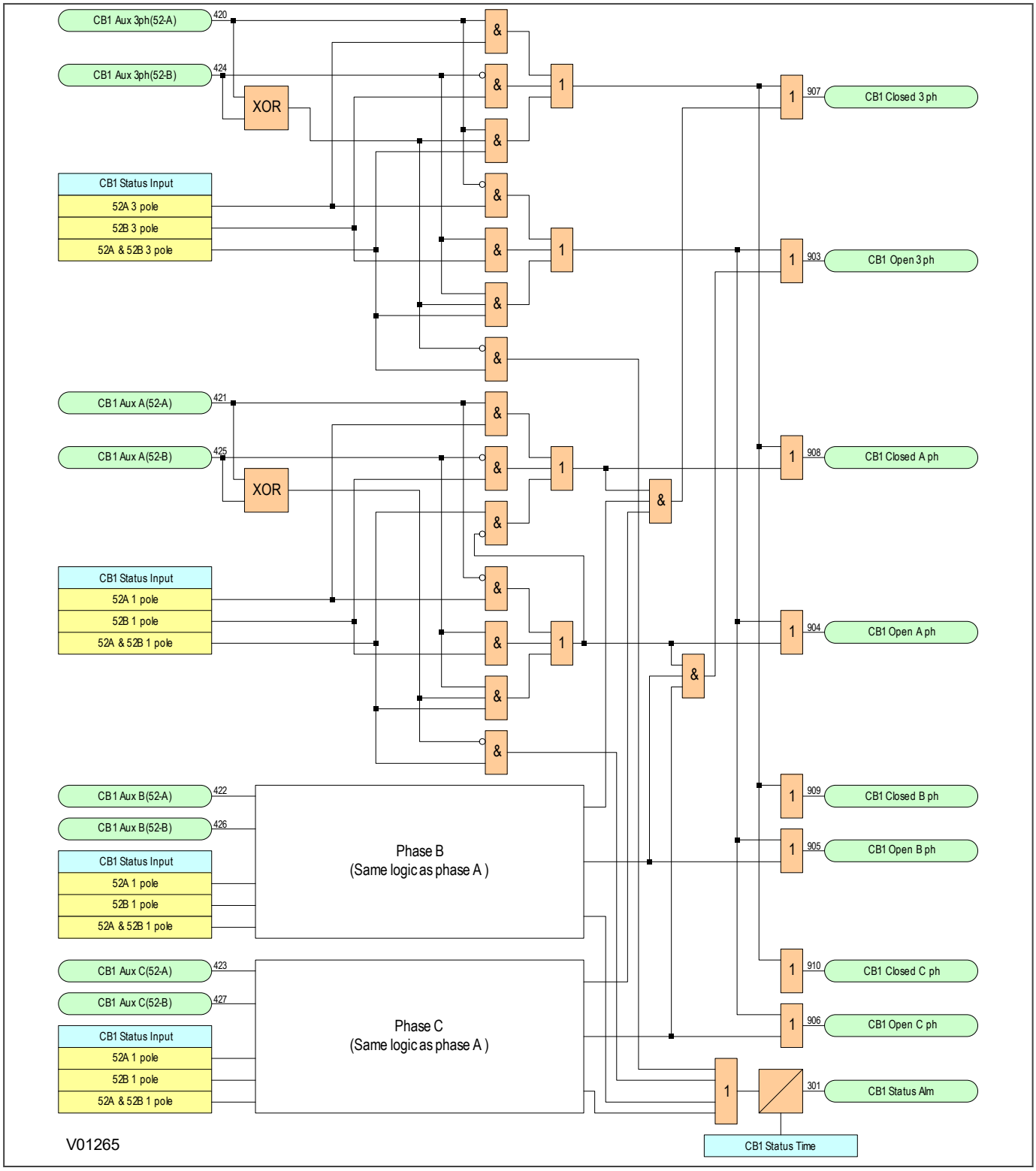


Figure 193: CB State logic diagram (Module 1)

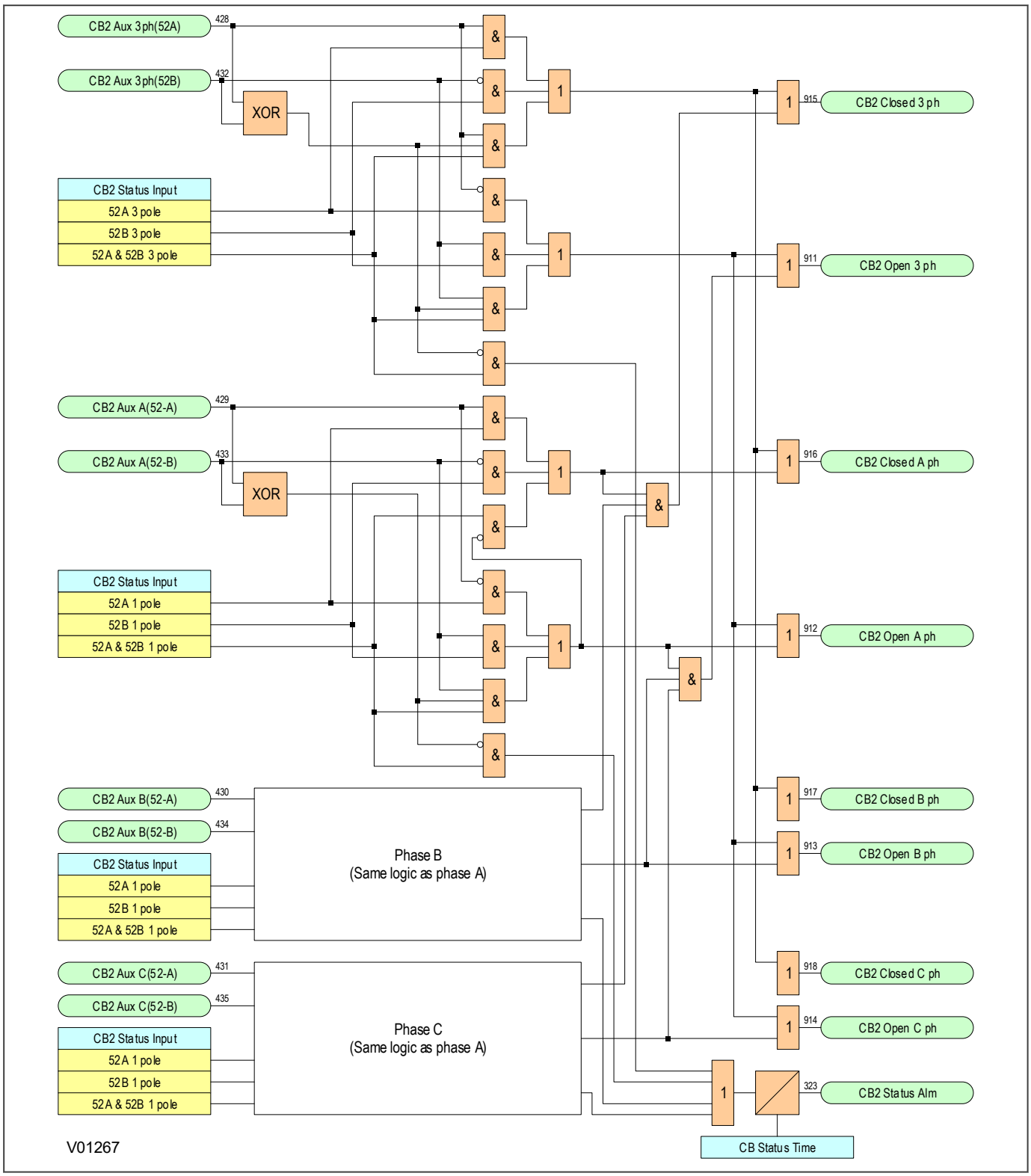


Figure 194: CB State logic diagram (Module 2)

13.7 CIRCUIT BREAKER CONTROL

Although some circuit breakers do not provide auxiliary contacts, most provide auxiliary contacts to reflect the state of the circuit breaker. These are:

- CBs with 52A contacts (where the auxiliary contact follows the state of the CB)
- CBs with 52B contacts (where the auxiliary contact is in the opposite state from the state of the CB)
- CBs with both 52A and 52B contacts

Circuit Breaker control is only possible if the circuit breaker in question provides auxiliary contacts. The ***CB Status Input*** cell in the *CB CONTROL* column must be set to the type of circuit breaker. If no CB auxiliary contacts are available then this cell should be set to `None`, and no CB control will be possible.

The ***CB control by*** cell is used to enable or disable local control options, remote control options, and combinations of both.

The output contact can be set to operate following a time delay defined by the setting ***Man Close Delay***. One reason for this delay is to give personnel time to safely move away from the circuit breaker following a CB close command.

The control close cycle can be cancelled at any time before the output contact operates by any appropriate trip signal, or by activating the ***Reset Close Dly*** DDB signal.

The length of the trip and close control pulses can be set via the ***Trip Pulse Time*** and **Close Pulse Time** settings respectively. These should be set long enough to ensure the breaker has completed its open or close cycle before the pulse has elapsed.

If an attempt to close the breaker is being made, and a protection trip signal is generated, the protection trip command overrides the close command.

The ***Reset Lockout by*** setting is used to enable or disable the resetting of lockout automatically from a manual close after the time set by ***Man Close RstDly***.

If the CB fails to respond to the control command (indicated by no change in the state of CB Status inputs) an alarm is generated after the relevant trip or close pulses have expired. These alarms can be viewed on the LCD display, remotely, or can be assigned to output contacts using the programmable scheme logic (PSL).

Note:
*The **CB Healthy Time** and **Sys Check time** set under this menu section are applicable to manual circuit breaker operations only. These settings are duplicated in the AUTORECLOSE menu for autoreclose applications.*

The ***Lockout Reset*** and ***Reset Lockout by*** settings are applicable to CB Lockouts associated with manual circuit breaker closure, CB Condition monitoring (Number of circuit breaker operations, for example) and autoreclose lockouts.

The device includes the following options for control of a single circuit breaker:

- The IED menu (local control)
- The CB Open/Close keys and the SLD on the graphical HMI
- The opto-inputs (local control)
- SCADA communication (remote control)

13.7.1 CB CONTROL USING THE IED MENU

You can control manual trips and closes with the ***CB Trip/Close*** command in the *SYSTEM DATA* column. This can be set to `No Operation`, `Trip`, or `Close` accordingly.

For this to work you have to set the ***CB control by*** cell to option 1 `Local`, option 3 `Local + Remote`, option 5 `Opto+Local`, option 7 `Opto+Local+Remote` or option 8 `L&R Key` in the *CB CONTROL* column.

13.7.2 SINGLE LINE DIAGRAM (SLD) VIEWER

The SLD menu displays the saved SLD on the graphical HMI screen. You can navigate to the SLD menu using the bottom Menu context keys or by using the quick launch menu on the Home page. The SLD is configured and uploaded into the IED using the S1 Agile configuration tool. Items of plant can be selected on the SLD screen using the navigation keypad.

13.7.2.1 CIRCUIT BREAKER CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the circuit breaker selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the ***CB Control by*** setting is selected, to option 1 `Local`, option 3 `Local+Remote`, option 5 `Opto+local`, option 7 `Opto+Rem+local` or option 8 `L/R Key` in the *CB CONTROL* column users are allowed to use the Trip and Close Key on the front panel to operate the CB.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***CB control by*** setting to `L/R Key`
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R Key LED is green and the REMOTE mode is selected. ***The L/R Key Status*** DDB status is stored in non-volatile memory, so that it's status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant which you require to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the Open or Close key to operate

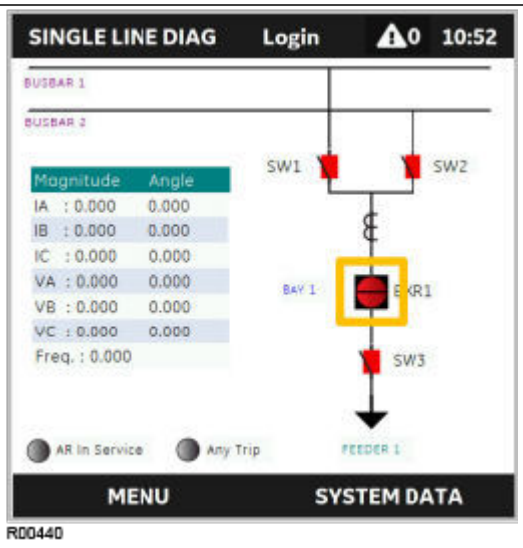


Figure 195: HMI SLD Display

For the Circuit Breaker Commands from HMI, additional checks are done:

If the CB is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "Control by" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "Control by" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "Control by" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - In Remote Control".

If the associated local DDB is set to local, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

13.7.3 CB CONTROL USING THE OPTO-INPUTS

Certain applications may require the use of push buttons or other external signals to control the various CB control operations. It is possible to connect such push buttons and signals to opto-inputs and map these to the relevant DDB signals.

For this to work, you have to set the ***CB control by*** cell to option 4 *opto*, option 5 *Opto+Local*, option 6 *Opto +Remote*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

13.7.4 REMOTE CB CONTROL

Remote CB control can be achieved from some of the serial and Ethernet data protocols, or by using the MiCOM S1 Agile settings application software.

For this to work, you have to set the ***CB control by*** cell to option 2 *Remote*, option 3 *Local+Remote*, option 6 *Opto+remote*, option 7 *Opto+Rem+local* or option 8 *L/R Key* in the *CB CONTROL* column.

We recommend that you allocate separate relay output contacts for remote CB control and protection tripping. This allows you to select the control outputs using a simple local/remote selector switch as shown below. Where this feature is not required the same output contact(s) can be used for both protection and remote tripping.

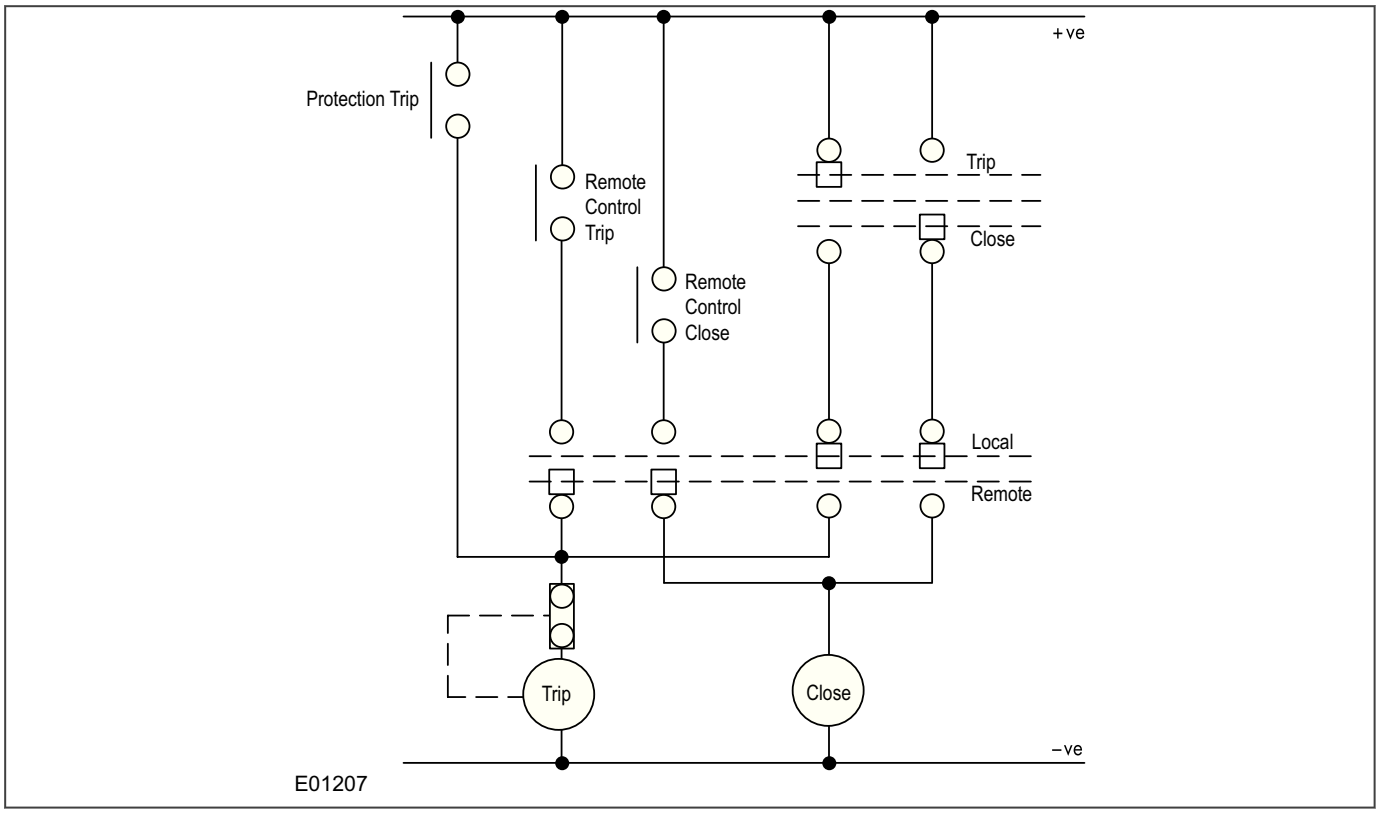


Figure 196: Remote Control of Circuit Breaker

DNP 3.0 protocol: The CB and switch positions can be controlled from Binary Outputs/Control Relay Output Blocks.

IEC 61850 protocol: The CB and switch positions can be controlled in the ‘CSWI’ Logical Node that is linked to the ‘XCBR’ Circuit Breaker Logical Node and 'XSWI' switch Logical Nodes. For Control Authority as per IEC 61850, it is necessary to select ***CB Control by*** cell as option 8 *L/R Key*.

13.7.5 CB HEALTHY CHECK

A CB Healthy check is available if required. This facility accepts an input to one of the opto-inputs to indicate that the breaker is capable of closing (e.g. that it is fully charged). A time delay can be set with the setting ***CB Healthy Time***. If the CB does not indicate a healthy condition within the time period following a Close command, the device will lockout and alarm.

13.7.6 SYNCHRONISATION CHECK

Where the check synchronism function is set, this can be enabled to supervise manual circuit breaker Close commands. A circuit breaker Close command will only be issued if the Check Synchronisation criteria are satisfied. A time delay can be set with the setting ***Sys Check time.*** If the Check Synchronisation criteria are not satisfied within the time period following a Close command the device will lockout and alarm.

13.7.7 CB CONTROL AR IMPLICATIONS

An ***Auto Close CB*** signal from the Auto-close logic bypasses the ***Man Close Delay*** time, and the ***CB Close*** output operates immediately to close the circuit breaker.

If Autoreclose is used it may be desirable to block its operation when performing a manual close. In general, the majority of faults following a manual closure are permanent faults and it is undesirable to allow automatic reclosure.

To ensure that Autoreclose is not initiated for a manual circuit breaker closure on to a pre-existing fault, the ***CB IS Time*** (circuit breaker in service time) setting in the *AUTORECLOSE* menu should be set for the desired time window. This setting ensures that Autoreclose initiation is inhibited for a period equal to setting ***CB IS Time*** following a manual circuit breaker closure. If a protection operation occurs during the inhibit period, Autoreclose is not initiated.

Following manual circuit breaker closure, if either a single phase or a three phase fault occur, the circuit breaker is tripped three phase, but Autoreclose is not locked out for this condition.

13.7.8 CB CONTROL LOGIC DIAGRAM

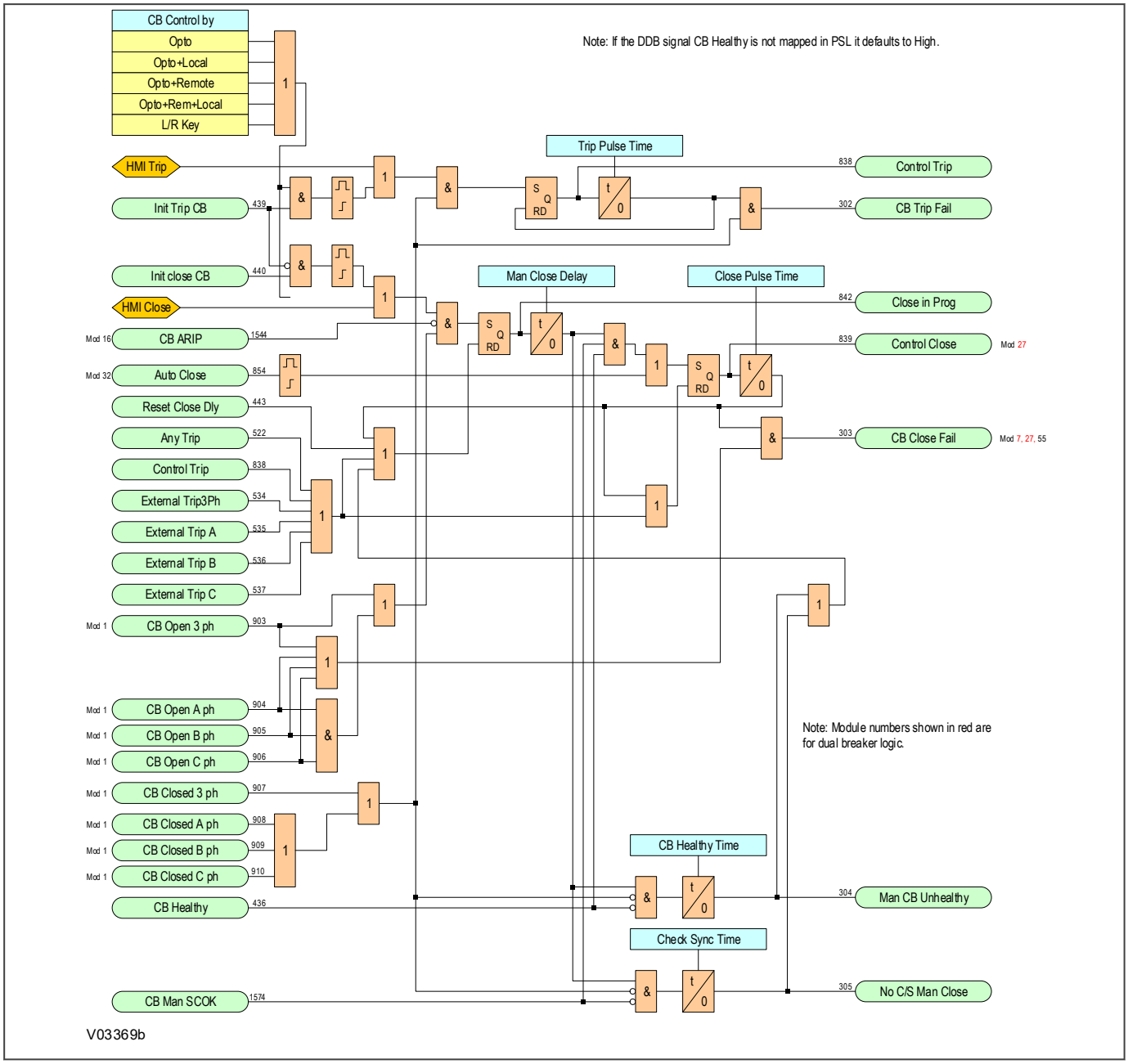


Figure 197: CB Control logic diagram (Module 43)

13.7.9 CB CONTROL LOGIC DIAGRAM

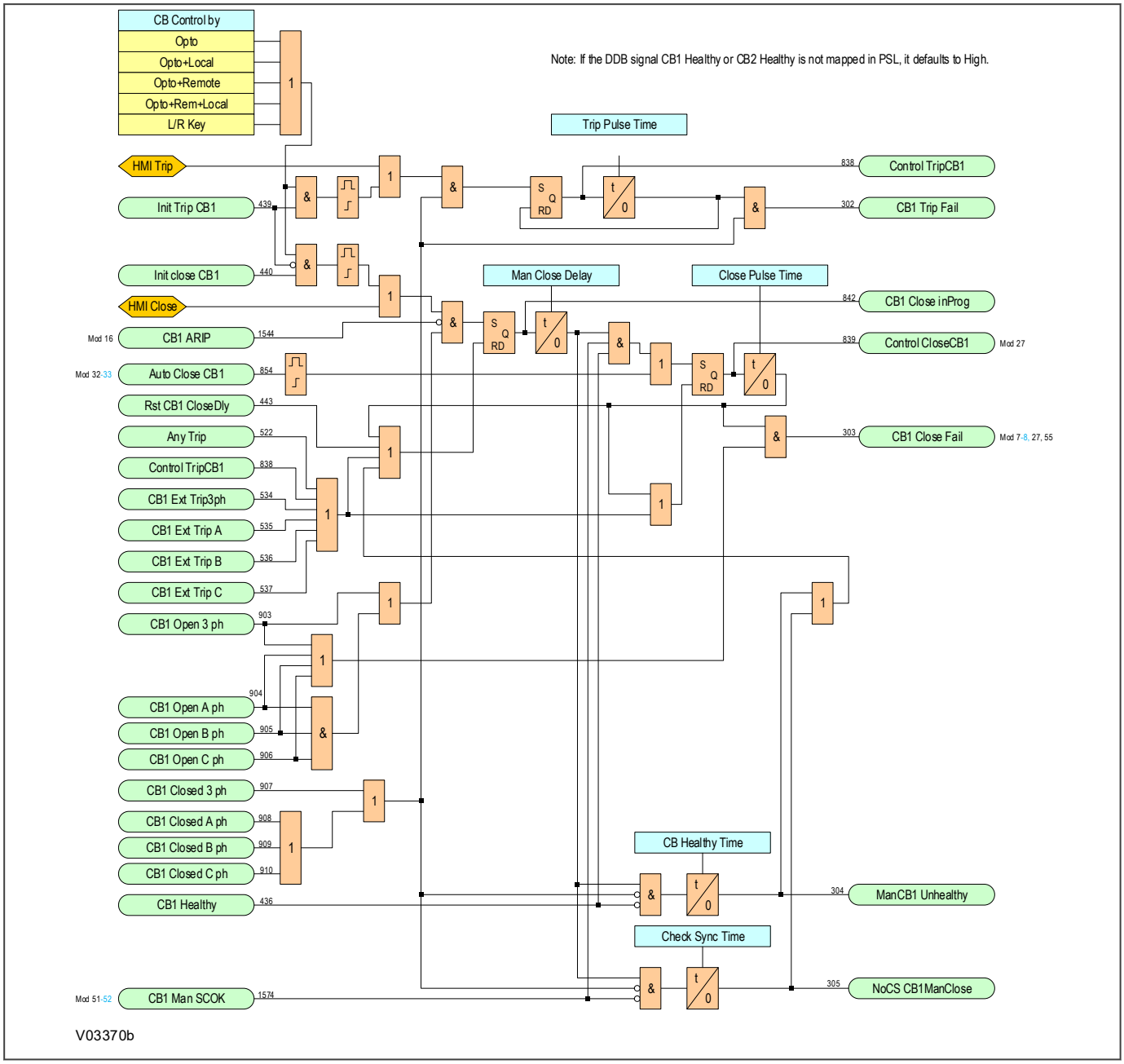


Figure 198: CB1 Control Logic (Module 43)

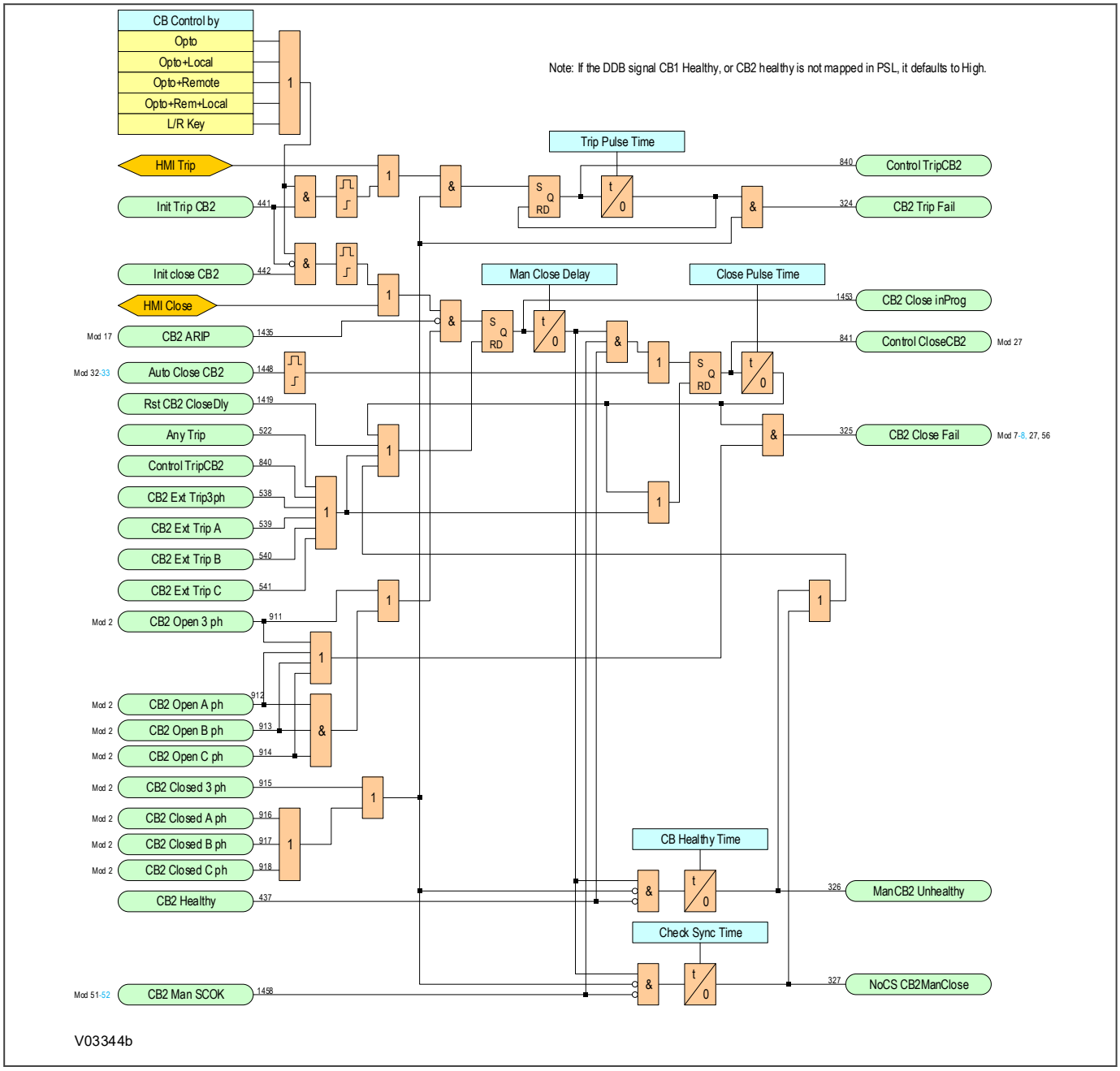


Figure 199: CB2 Control Logic (Module 44)

13.8 POLE DEAD FUNCTION

The Pole Dead Logic is used to determine and indicate that one or more phases of the line are not energised. A Pole Dead condition is determined either by measuring:

- the line currents and/or voltages, or
- by monitoring the status of the circuit breaker auxiliary contacts, as shown by dedicated DDB signals.

It can also be used to block operation of underfrequency and undervoltage elements where applicable.

13.8.1 POLE DEAD LOGIC

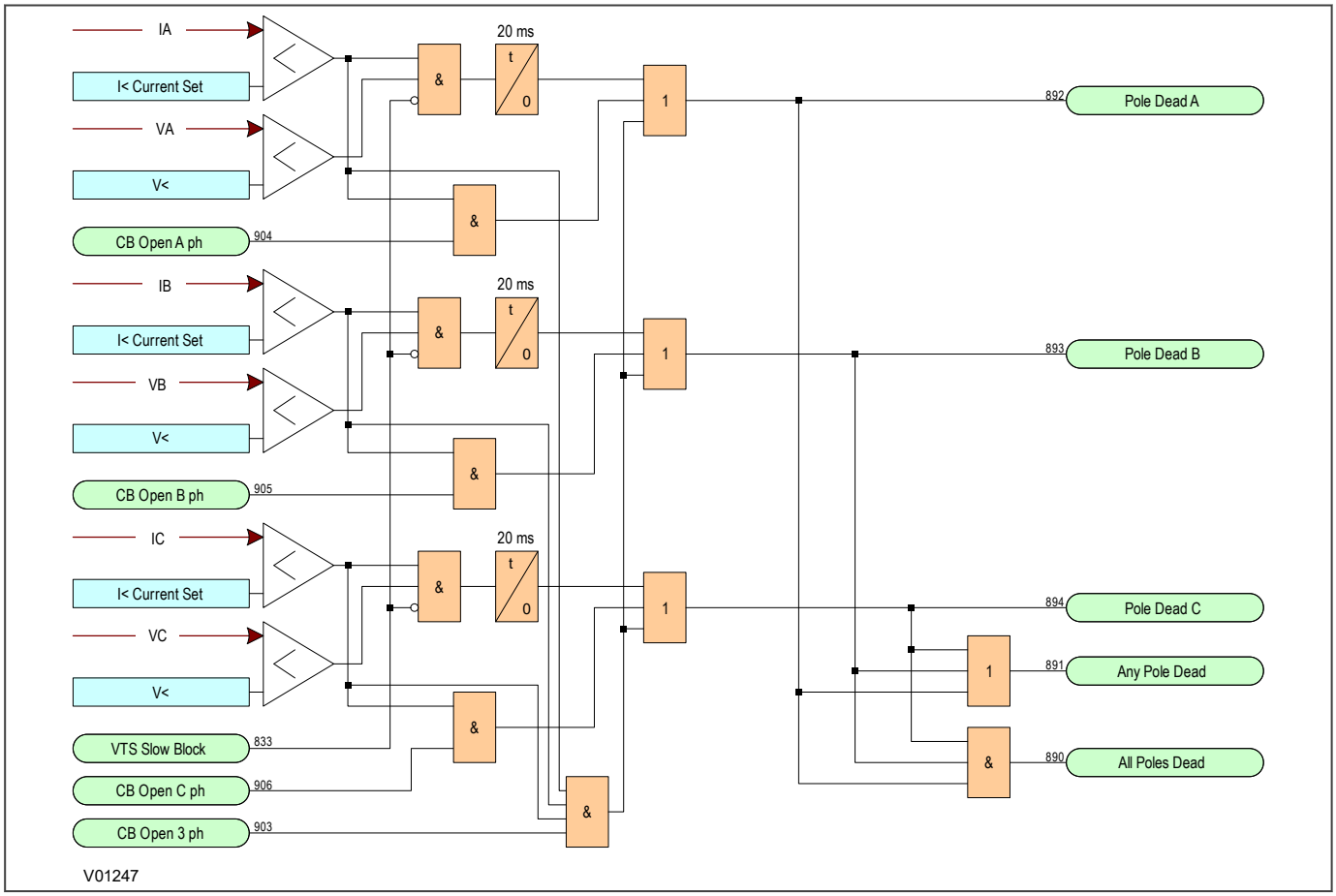


Figure 200: Pole Dead logic

If both the line current and voltage values fall below a certain threshold, or a CB Open condition is asserted from the state control logic, the device initiates a Pole Dead condition. The current and voltage thresholds can be set with the ***I< Current Set*** and the ***V< settings*** respectively, in the *CBFAIL&P.DEAD* column.

If one or more poles are dead, the device indicates which phase is dead and asserts the ***Any Pole Dead*** DDB signal. If all phases are dead the ***Any Pole Dead*** signal is accompanied by the ***All Poles Dead*** signal.

If the VT fails, a ***VTS Slow Block*** signal is taken from the VTS logic to block the Pole Dead indications that would be generated by the undervoltage and undercurrent thresholds.

Note:
If the VT is connected at the busbar side, auxiliary contacts (52a or 52b) must be connected to the IED for a correct pole dead indication.

13.8.2 POLE DEAD LOGIC

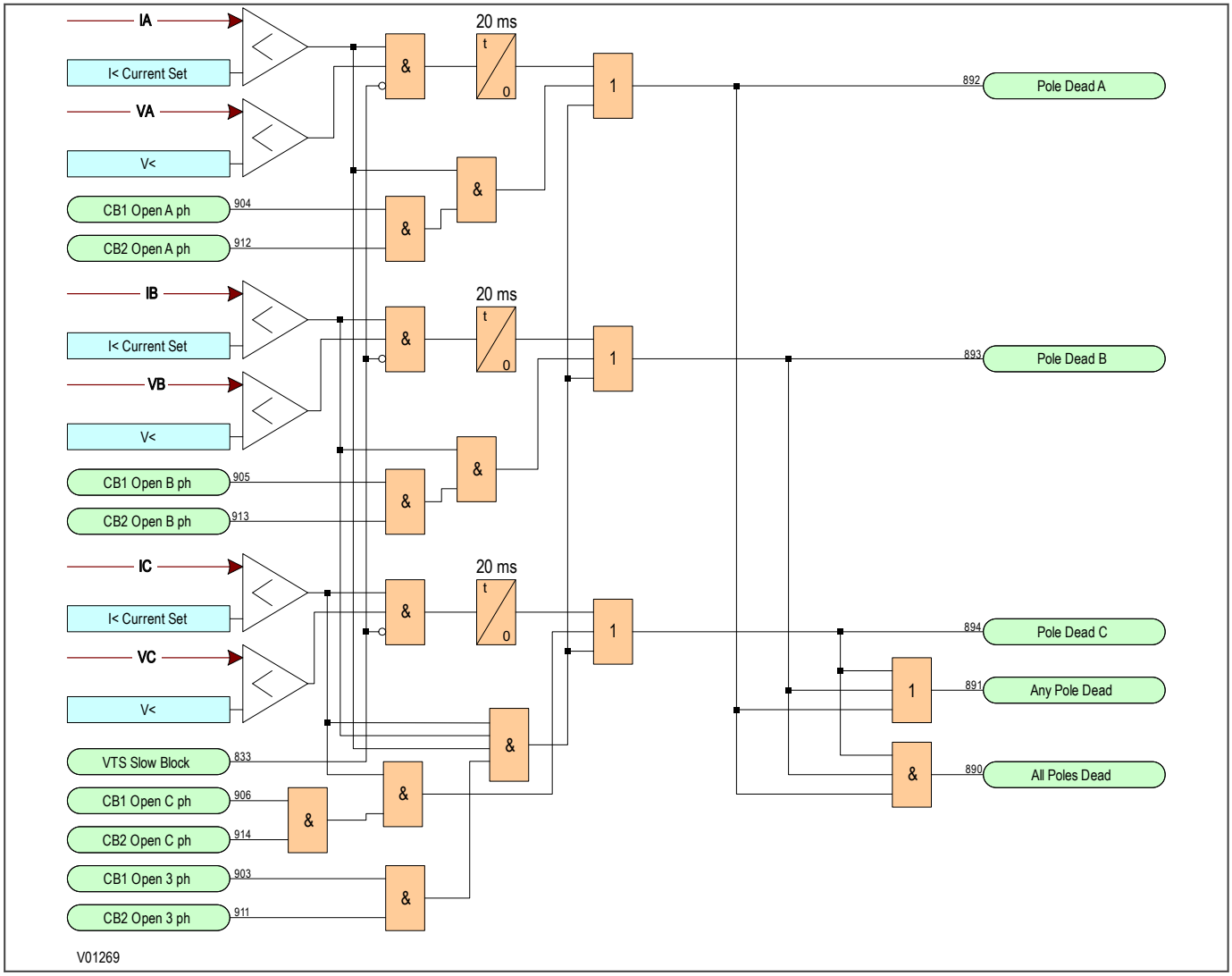


Figure 201: Pole Dead logic

If both the line current and voltage values fall below a certain threshold, or a CB Open condition is asserted from the state control logic, the device initiates a Pole Dead condition. The current and voltage thresholds can be set with the ***I< Current Set*** and the ***V< settings*** respectively, in the *CBFAIL&P.DEAD* column.

If one or more poles are dead, the device indicates which phase is dead and asserts the ***Any Pole Dead*** DDB signal. If all phases are dead the ***Any Pole Dead*** signal is accompanied by the ***All Poles Dead*** signal.

If the VT fails, a ***VTS Slow Block*** signal is taken from the VTS logic to block the Pole Dead indications that would be generated by the undervoltage and undercurrent thresholds.

Note:
If the VT is connected at the busbar side, auxiliary contacts (52a or 52b) must be connected to the IED for a correct pole dead indication.

13.9 SYSTEM CHECKS

In some situations it is possible for both "bus" and "line" sides of a circuit breaker to be live when a circuit breaker is open - for example at the ends of a feeder that has a power source at each end. Therefore, it is normally necessary to check that the network conditions on both sides are suitable, before closing the circuit breaker. This applies to both manual circuit breaker closing and autoreclosing. If a circuit breaker is closed when the line and bus voltages are both live, with a large phase angle, frequency or magnitude difference between them, the system could be subjected to an unacceptable shock, resulting in loss of stability, and possible damage to connected machines.

The System Checks functionality involves monitoring the voltages on both sides of a circuit breaker, and if both sides are live, performing a synchronisation check to determine whether any differences in voltage magnitude, phase angle or frequency are within permitted limits.

The pre-closing system conditions for a given circuit breaker depend on the system configuration, and for autoreclosing, on the selected autoreclose program. For example, on a feeder with delayed autoreclosing, the circuit breakers at the two line ends are normally arranged to close at different times. The first line end to close usually has a live bus and a dead line immediately before reclosing. The second line end circuit breaker now sees a live bus and a live line.

If there is a parallel connection between the ends of the tripped feeder the frequencies will be the same, but any increased impedance could cause the phase angle between the two voltages to increase. Therefore just before closing the second circuit breaker, it may be necessary to perform a synchronisation check, to ensure that the phase angle between the two voltages has not increased to a level that would cause unacceptable shock to the system when the circuit breaker closes.

If there are no parallel interconnections between the ends of the tripped feeder, the two systems could lose synchronism altogether and the frequency at one end could "slip" relative to the other end. In this situation, the second line end would require a synchronism check comprising both phase angle and slip frequency checks.

If the second line-end busbar has no power source other than the feeder that has tripped; the circuit breaker will see a live line and dead bus assuming the first circuit breaker has re-closed. When the second line end circuit breaker closes the bus will charge from the live line (dead bus charge).

13.9.1 SYSTEM CHECKS IMPLEMENTATION

The System Checks function provides *Live/Dead Voltage Monitoring*, two stages of *Check Synchronisation* and *System Split* indication.

The System Checks function is enabled or disabled by the ***System Checks*** setting in the *CONFIGURATION* column. If ***System Checks*** is disabled, the *SYSTEM CHECKS* menu becomes invisible, and a ***SysChks Inactive*** DDB signal is set.

The System Checks functionality can also be enabled or disabled by the ***System Checks*** setting in the *SYSTEM CHECKS* column. For the Systems Checks functionality to be enabled, both the ***System Checks*** setting in the *CONFIGURATION* column AND the ***System Checks*** setting in the *SYSTEM CHECKS* column must be enabled. For the System Checks functionality to be disabled, either the ***System Checks*** setting in the *CONFIGURATION* column OR the ***System Checks*** setting in the *SYSTEM CHECKS* column must be be enabled. In the latter case, the ***SysChks Inactive*** DDB signal is set.

The system Checks functionality can also be enabled or disabled individually for each circuit breaker by the ***System Checks CB1*** and ***System Checks CB2*** settings in the *SYSTEM CHECKS* column. For the Systems Checks functionality to be enabled, both the ***System Checks*** setting in the *CONFIGURATION* column AND the relevant setting (***System Checks CB1*** and/or ***System Checks CB2***) in the *SYSTEM CHECKS* column must be enabled. For the System Checks functionality to be disabled, either the ***System Checks*** setting in the *CONFIGURATION* column OR the relevant setting (***System Checks CB1*** and/or ***System Checks CB2***) in the *SYSTEM CHECKS* column must be be enabled. In the latter case, the ***SysChks Inactive*** DDB signal is set.

13.9.1.1 VT CONNECTIONS

The device provides inputs for a three-phase "Main VT" and at least one single-phase VT for check synchronisation. Depending on the primary system arrangement, the Main VT may be located on either the line-side of the busbar-side of the circuit breaker, with the Check Sync VT on the other. Normally, the Main VT is located on the line-side (as per the default setting), but this is not always the case. For this reason, a setting is provided where you can define this. This is the ***Main VT Location*** setting, which is found in the *CT AND VT RATIOS* column.

The Check Sync VT may be connected to one of the phase-to-phase voltages or phase-to-neutral voltages. This needs to be defined using the ***CS Input*** setting in the *CT AND VT RATIOS* column. Options are, A-B, B-C, C-A, A-N, B-N, or C-N.

13.9.1.2 VOLTAGE MONITORING

The settings in the *VOLTAGE MONITORS* sub-heading in the *SYSTEM CHECKS* column allow you to define the threshold at which a voltage is considered live, and a threshold at which the voltage is considered dead. These thresholds apply to both line and bus sides. If the measured voltage falls below the ***Dead Voltage*** setting, a DDB signal is generated (***Dead Bus***, or ***Dead Line***, depending on which side is being measured). If the measured voltage exceeds the ***Live Voltage*** setting, a DDB signal is generated (***Live Bus***, or ***Live Line***, depending on which side is being measured).

13.9.1.3 CHECK SYNCHRONISATION

The device provides two stages of Check Synchronisation. The first stage (CS1) is intended for use in synchronous systems. This means, where the frequencies and phase angles of both sides are compared and if the difference is within set limits, the circuit breaker is allowed to close. The second stage (CS2) is similar to stage, but has an additional adaptive setting. The second stage CS2 is intended for use in asynchronous systems, i.e. where the two sides are out of synchronism and one frequency is slipping continuously with respect to another. If the closing time of the circuit breaker is known, the CB Close command can be issued at a definite point in the cycle such that the CB closes at the point when both sides are in phase.

In situations where it is possible for the voltages on either side of a circuit breaker to be either synchronous or asynchronous, both CS1 and CS2 can be enabled to provide a CB Close signal if either set of permitted closing conditions is satisfied.

Each stage can also be set to inhibit circuit breaker closing if selected blocking conditions such as overvoltage, undervoltage or excessive voltage magnitude difference are detected. CS2 requires the phase angle difference to be decreasing in magnitude before permitting the circuit breaker to close. CS2 has an optional “Adaptive” closing feature, which issues the permissive close signal when the predicted phase angle difference immediately prior to the instant of circuit breaker main contacts closing (i.e. after CB Close time) is as close as practicable to zero.

Slip frequency is the rate of change of phase between each side of the circuit breaker, which is measured by the difference between the voltage signals on either side of the circuit breaker.

Having two system synchronism check stages available allows the circuit breaker closing to be enabled under different system conditions (for example, low slip / moderate phase angle, or moderate slip / small phase angle).

The settings specific to Check Synchronisation are found under the sub-heading *CHECK SYNC* in the *SYSTEM CHECKS* column. The only difference between the CS1 settings and the CS2 settings is that CS2 has a ***CS2 Adaptive*** setting for predictive closure of CB.

The settings specific to Check Synchronisation are found under the sub-heading *CHECK SYNC* in the *SYSTEM CHECKS* column. The only difference between the CS1 settings and the CS2 settings is that CS2 has settings for predictive closure of each CB (***CB1 CS2 Adaptive*** and ***CB2 CS2 Adaptive***).

13.9.1.4 CHECK SYNCRONISATION VECTOR DIAGRAM

The following vector diagram represents the conditions for the System Check functionality. The Dead Volts setting is represented as a circle around the origin whose radius is equal to the maximum voltage magnitude, whereby the voltage can be considered dead. The nominal line voltage magnitude is represented by a circle around the origin

whose radius is equal to the nominal line voltage magnitude. The minimum voltage magnitude at which the system can be considered as Live, is the magnitude difference between the bus and line voltages.

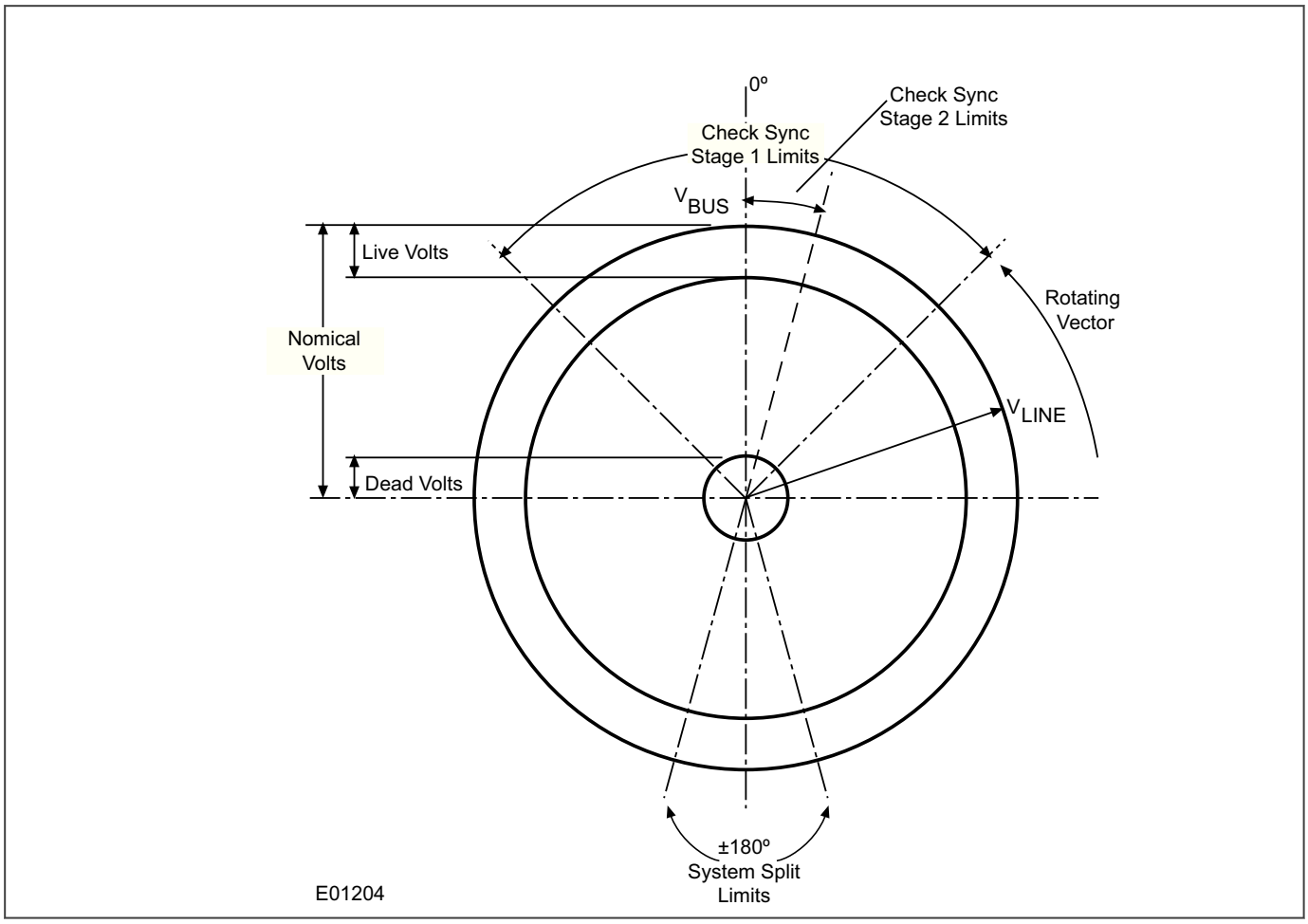


Figure 202: Check Synchronisation vector diagram

13.9.1.5 SYSTEM SPLIT

If the line side and bus side are of the same frequency (i.e. in synchronism) but have a large phase angle between them (180° +/- the set limits), the system is said to be 'Split'. If this is the case, the device will detect this and issue an alarm signal indicating this.

The settings specific to System Split functionality are found under the sub-heading *SYSTEM SPLIT* in the *SYSTEM CHECKS* column.

13.9.2 VOLTAGE MONITOR FOR CB CLOSURE

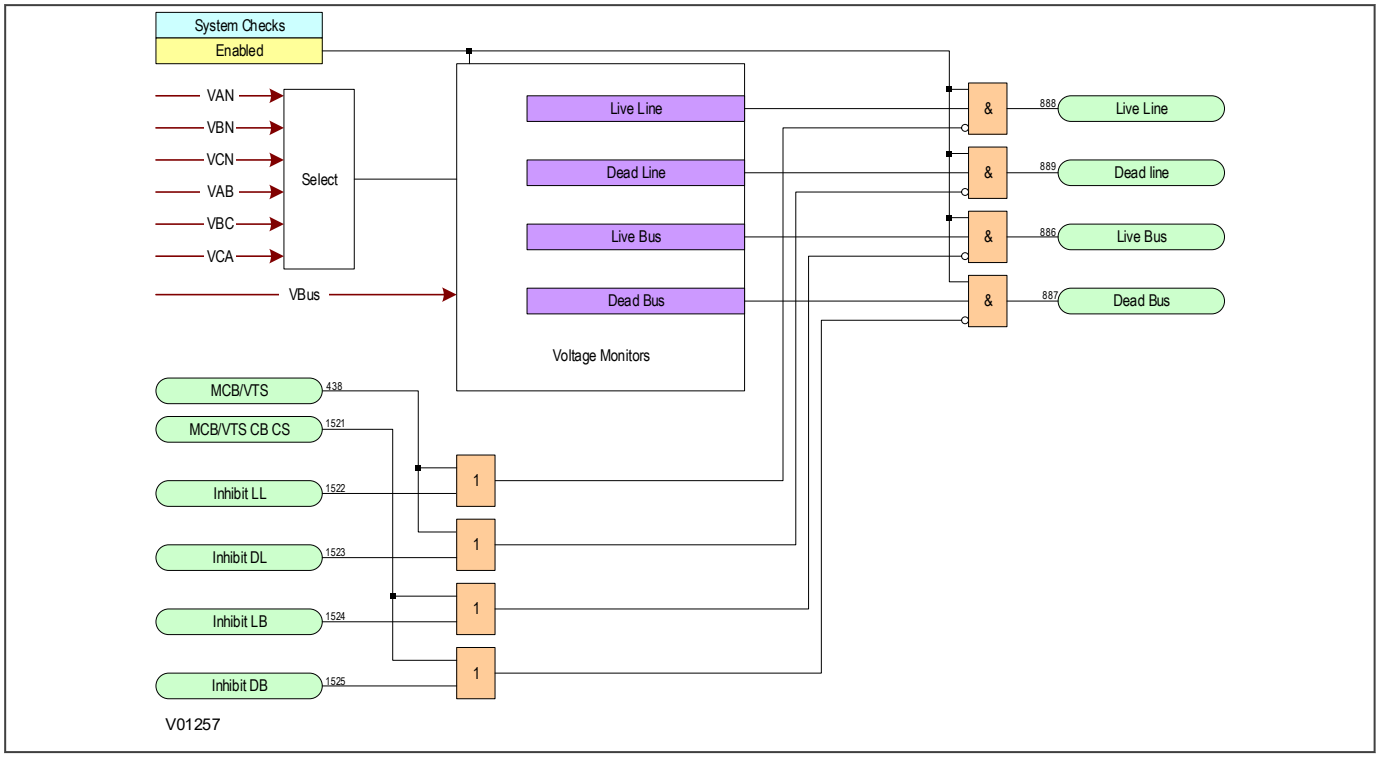


Figure 203: Voltage Monitor for CB Closure (Module 59)

13.9.3 VOLTAGE MONITOR FOR CB CLOSURE

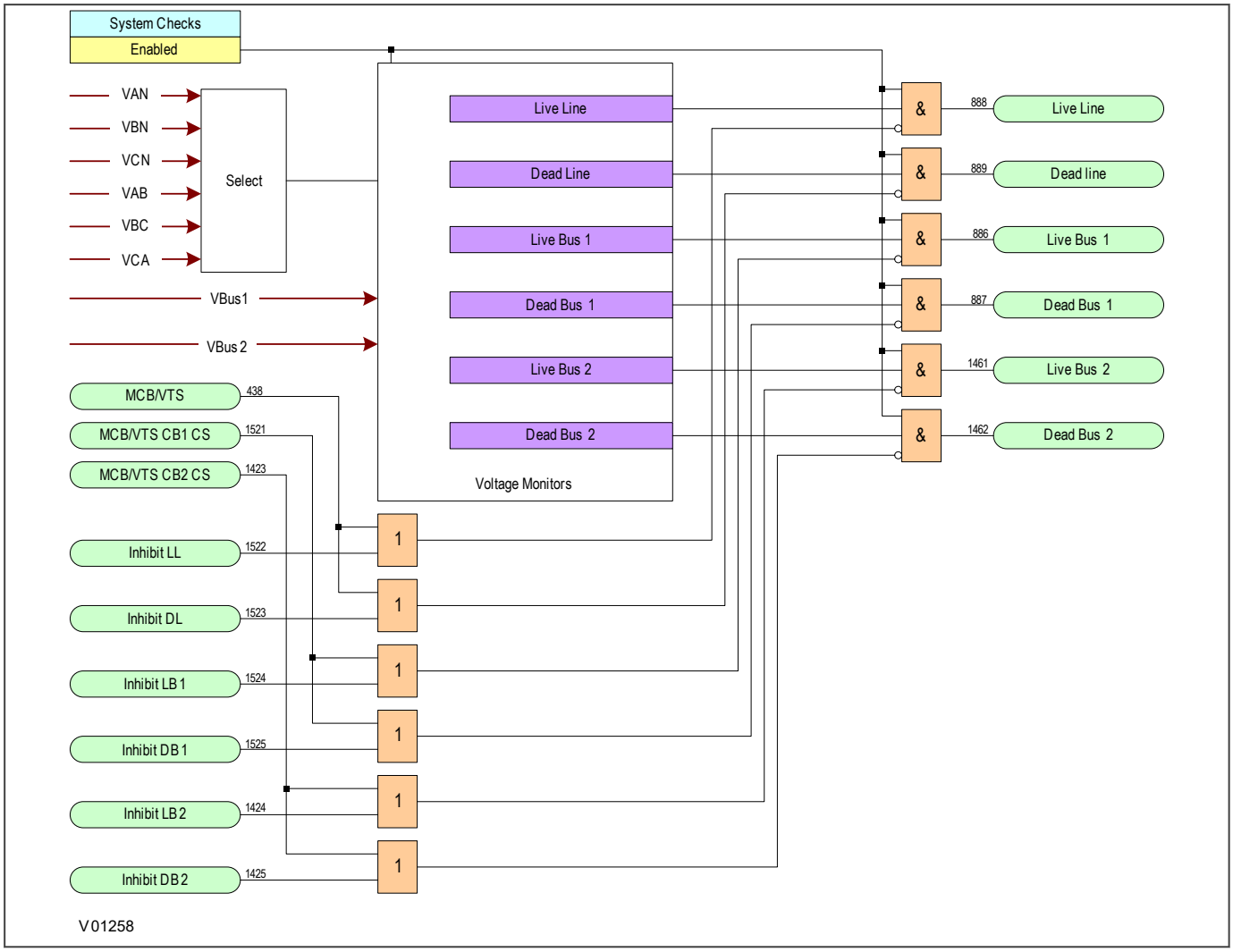


Figure 204: Voltage Monitor for CB Closure (Module 59)

13.9.4 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

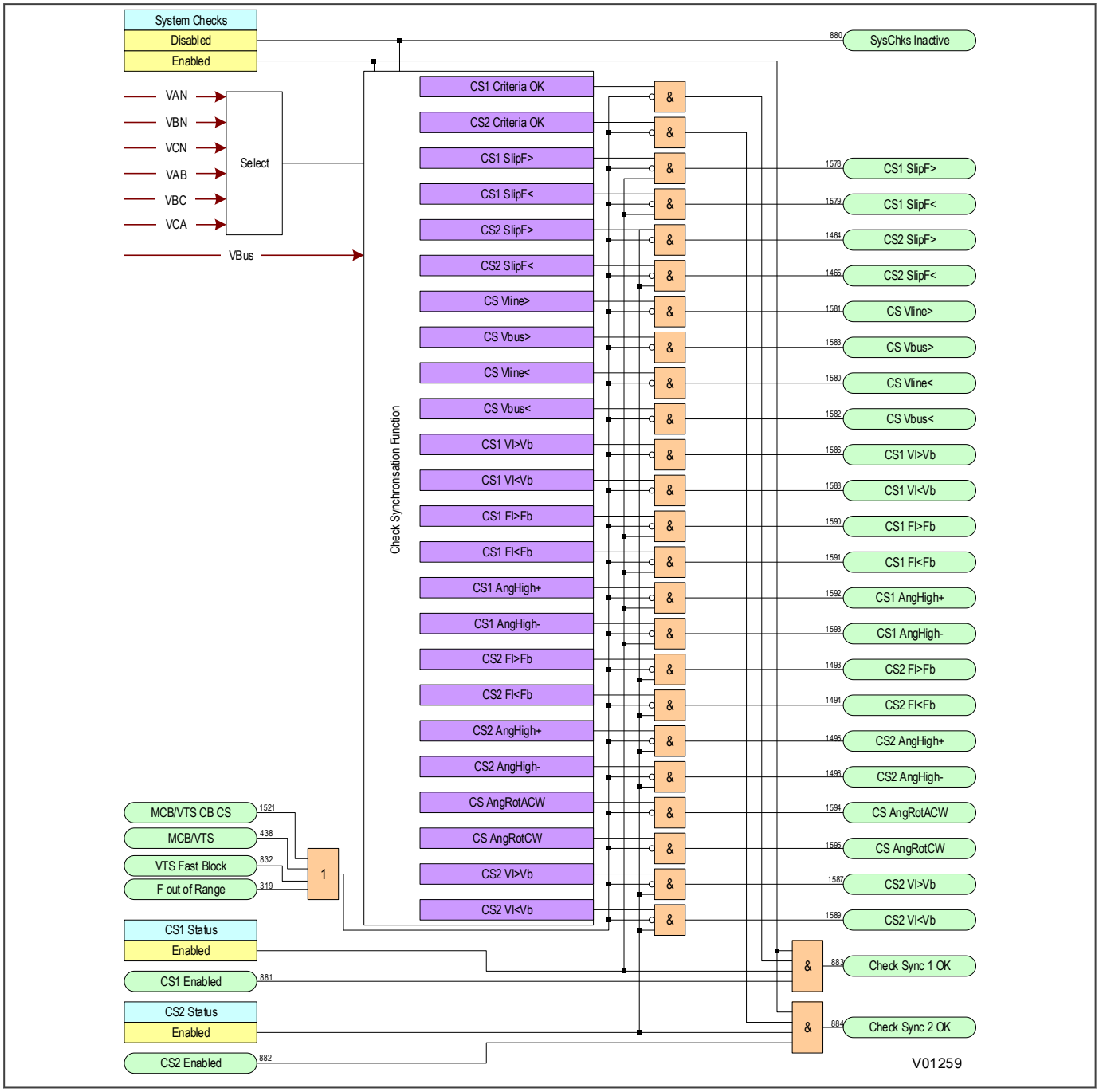


Figure 205: Check Synchronisation Monitor for CB closure (Module 60)

13.9.5 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

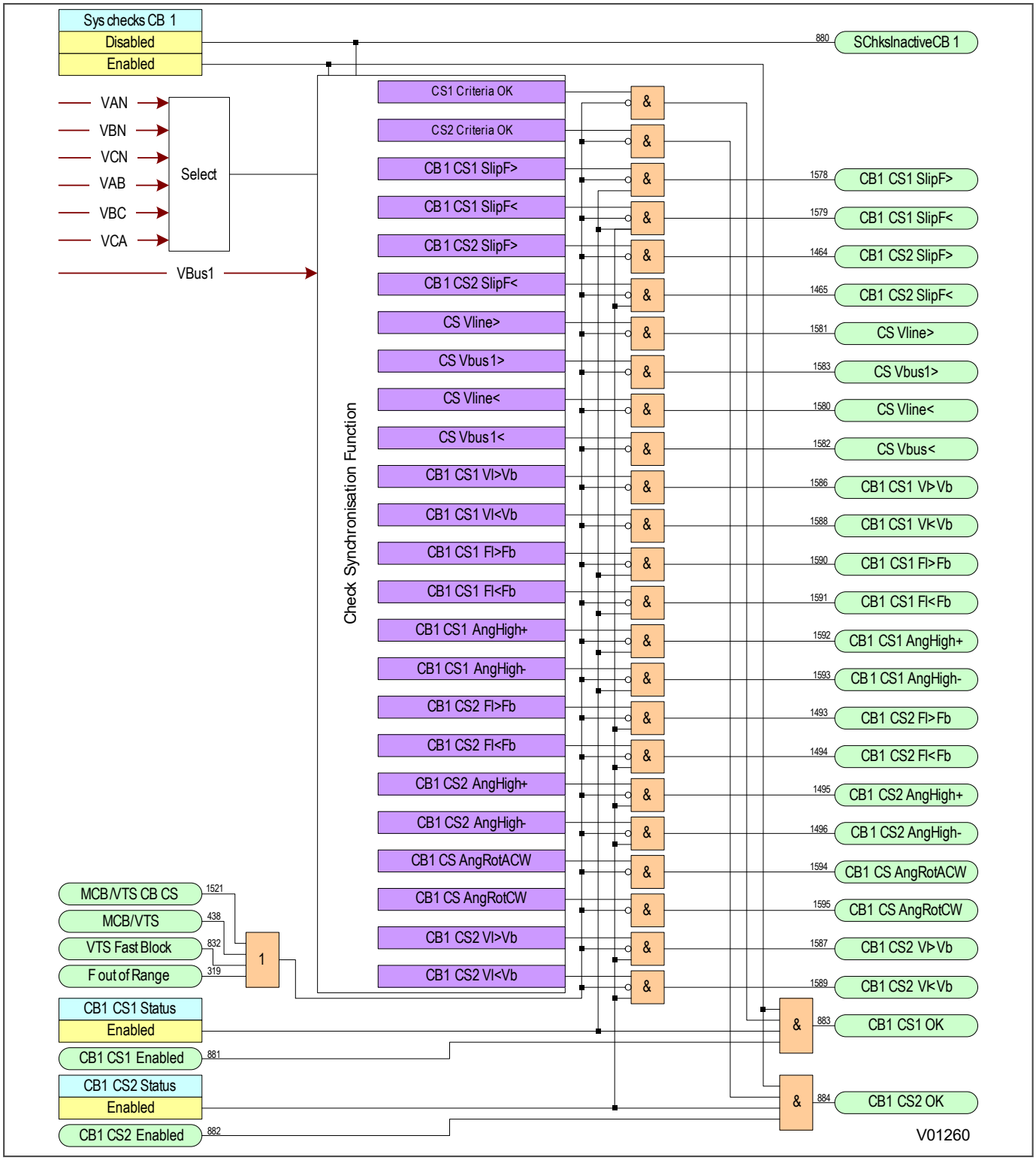


Figure 206: Check Synchronisation Monitor for CB1 closure (Module 60)

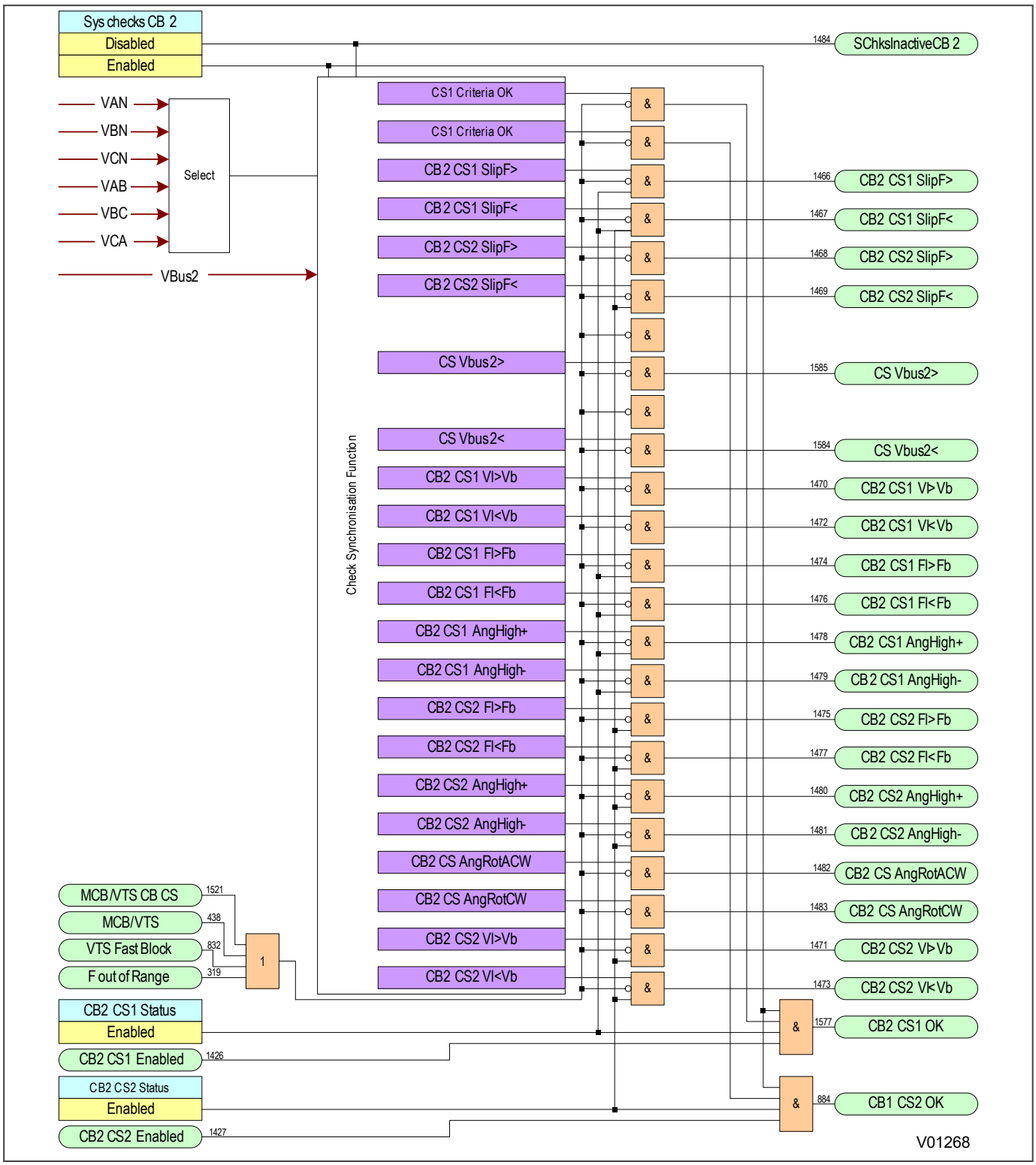


Figure 207: Check Synchronisation Monitor for CB2 closure (Module 61)

13.9.6 SYSTEM CHECK LOGIC

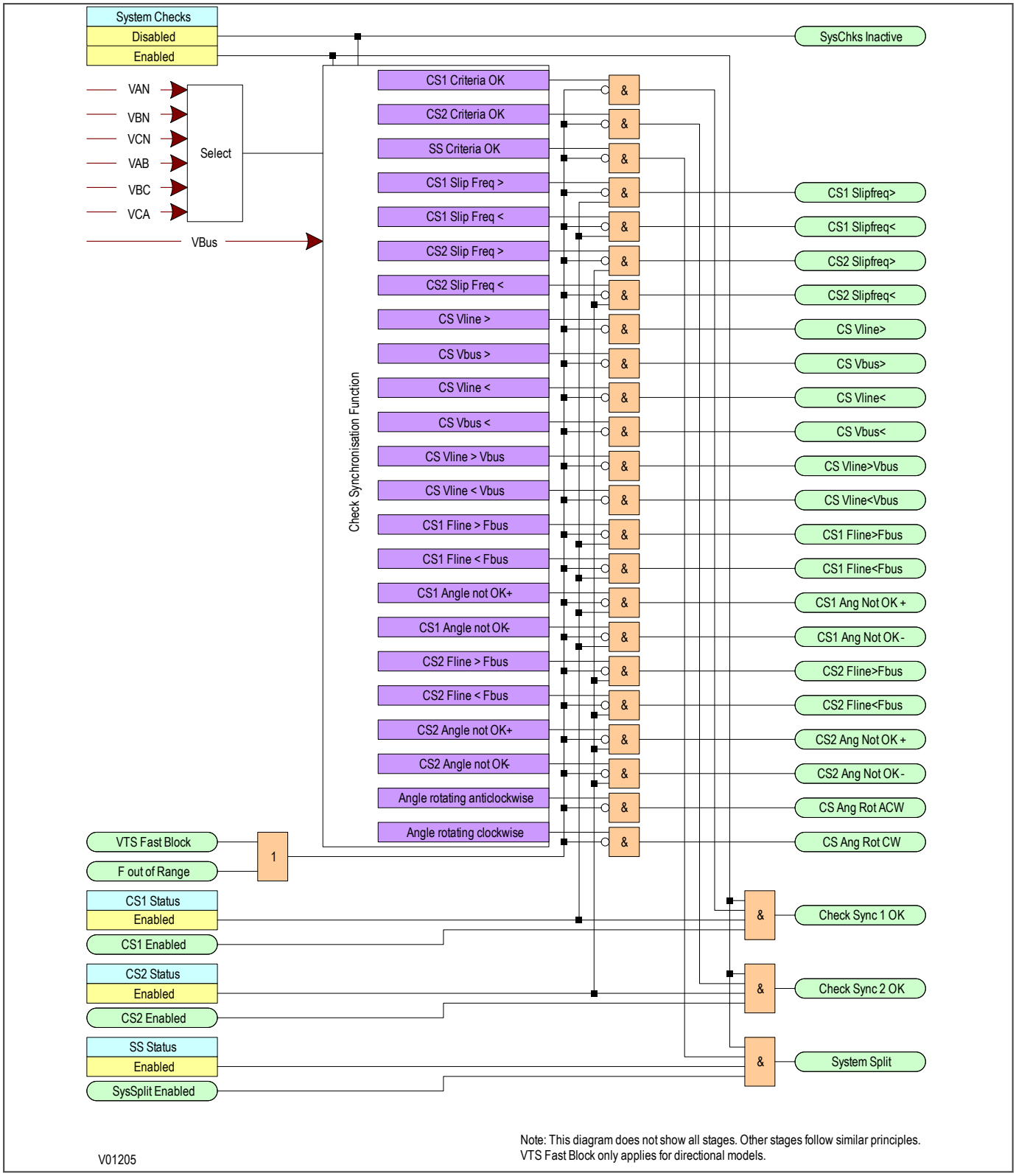


Figure 208: System Check logic

13.9.7 SYSTEM CHECK PSL

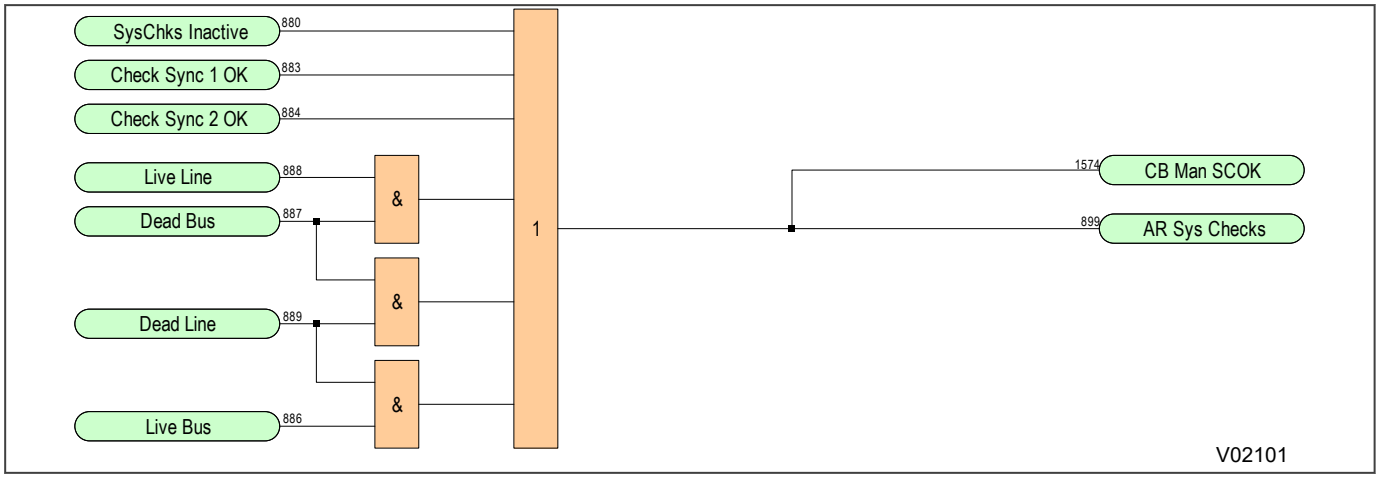


Figure 209: System Check PSL

13.9.8 APPLICATION NOTES

13.9.8.1 USE OF CHECK SYNC 2 AND SYSTEM SPLIT

Check Sync 2 (CS2) and System Split functions are included for situations where the maximum permitted slip frequency and phase angle for synchronism checks can change due to adverse system conditions. A typical application is on a closely interconnected system, where synchronism is normally retained when a feeder is tripped. But under some circumstances, with parallel interconnections out of service, the feeder ends can drift out of synchronism when the feeder is tripped. Depending on the system and machine characteristics, the conditions for safe circuit breaker closing could be, for example:

Condition 1: For synchronized systems, with zero or very small slip:

- Slip <50 mHz; phase angle <30°

Condition 2: For unsynchronized systems, with significant slip:

- Slip < 250 mHz; phase angle <10° and decreasing

By enabling both CS1 and CS2, the device can be configured to allow CB closure if either of the two conditions is detected.

For manual circuit breaker closing with synchronism check, some utilities might prefer to arrange the logic to check initially for condition 1 only. However, if a System Split is detected before the condition 1 parameters are satisfied, the device will switch to checking for condition 2 parameters instead, based on the assumption that a significant degree of slip must be present when system split conditions are detected. This can be arranged by suitable PSL logic, using the System Check DDB signals.

13.9.8.2 PREDICTIVE CLOSURE OF CIRCUIT BREAKER

The ***CS2 Adaptive*** setting compensates for the time taken to close the CB. When set to provide CB Close Time compensation, a predictive approach is used to close the circuit breaker ensuring that closing occurs at close to 0º therefore minimising the impact to the power system. The actual closing angle is subject to the constraints of the existing product architecture, i.e. the protection task runs twice per power system cycle, based on frequency tracking over the frequency range of 40 Hz to 65 Hz.

13.9.8.3 PREDICTIVE CLOSURE OF CIRCUIT BREAKERS

The ***CB1 CS2 Adaptive*** and ***CB1 CS2 Adaptive*** settings compensate for the time taken to close the CB. When set to provide CB Close Time compensation, a predictive approach is used to close the circuit breaker ensuring that closing occurs at close to 0º therefore minimising the impact to the power system. The actual closing angle is subject to the constraints of the existing product architecture, i.e. the protection task runs twice per power system cycle, based on frequency tracking over the frequency range of 40 Hz to 65 Hz.

13.9.8.4 VOLTAGE AND PHASE ANGLE CORRECTION

For the Check Synchronisation function, the device needs to convert measured secondary voltages into primary voltages. In some applications, VTs either side of the circuit breaker may have different VT Ratios. In such cases, a magnitude correction factor is required.

There are some applications where the main VT is on the HV side of a transformer and the Check Sync VT is on the LV side, or vice-versa. If the vector group of the transformer is not "0", the voltages are not in phase, so phase correction is also necessary.

The correction factors are as follows and are located in the *CT AND VT RATIOS* column:

- C/S V kSM, where kSM is the voltage correction factor.
- C/S Phase kSA, where kSA is the angle correction factor.

Assuming C/S input setting is A-N, then:

The line and bus voltage magnitudes are matched if $V_{a\ sec} = V_{cs\ sec}$ x C/S V kSA

The line and bus voltage angles are matched if $\angle V_{a\ sec} = \angle V_{cs\ sec}$ + C/S Phase kSA

The following application scenarios show where the voltage and angular correction factors are applied to match different VT ratios:

Scenario	Physical Ratios (ph-N Values)				Setting Ratios				CS Correction Factors	
	Main VT Ratio		CS VT Ratio		Main VT Ratio (ph-ph) Always		CS VT Ratio		kSM	kSA
	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)		
1	220/√3	110/√3	132/√3	100/√3	220	110	132	100	1.1	30º
2	220/√3	110/√3	220/√3	110	220	110	127	110	0.577	0º
3	220/√3	110/√3	220/√3	110/3	220	110	381	110	1.732	0º

13.10 SWITCH STATUS AND CONTROL

All P84 products support Switch Status and Control for up to 8 switchgear elements. This is available for IEC60870-5-103 and IEC61850 protocols. The device is able to monitor the status of and control up to eight switches. The types of switch that can be controlled are:

- Load Break switch
- Disconnector
- Earthing SwitchP84
- High Speed Earthing Switch

Consider the following feeder bay:

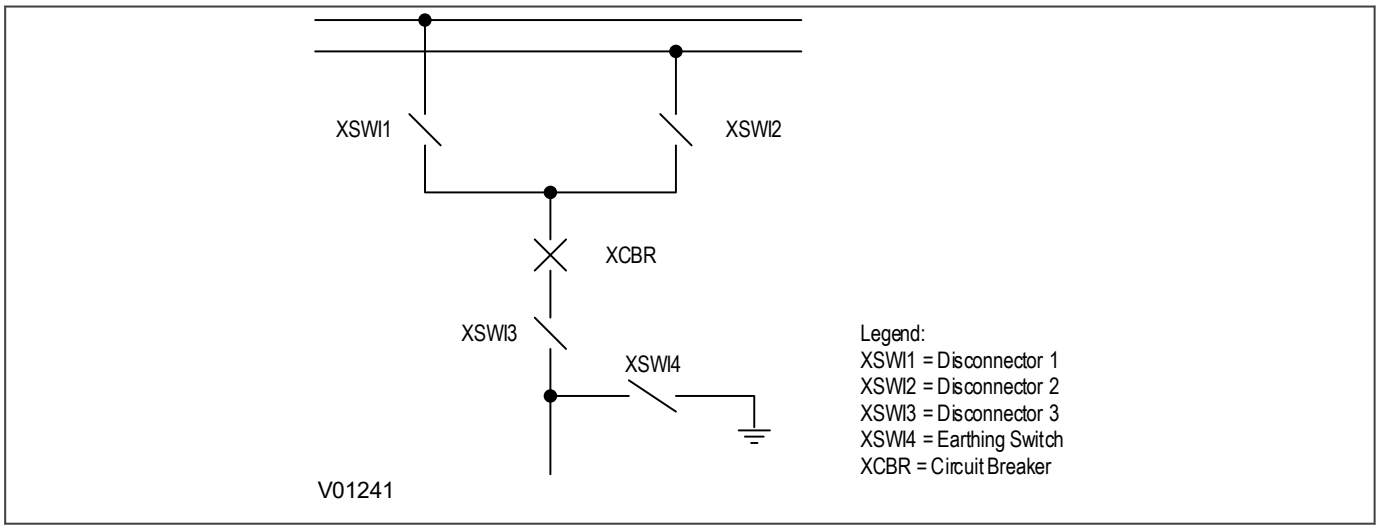


Figure 210: Representation of typical feeder bay

This bay shows four switches of the type LN XSWI and one circuit breaker of type LN XCBR. In this example, the switches XSWI1 – XSWI3 are disconnectors and XCSWI4 is an earthing switch.

For the device to be able to control the switches, the switches must provide auxiliary contacts to indicate the switch status. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers.

There are eight sets of settings in the *SWITCH CONTROL* column, which allow you to set up the Switch control, one set for each switch. These settings are as follows:

SWITCH1 Type

This setting defines the type of switch. It can be a load breaking switch, a disconnector, an earthing switch or a high speed earthing switch.

SWI1 Status Inpt

This setting defines the type of auxiliary contacts that will be used for the control logic. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers. "A" contacts match the status of the primary contacts, whilst "B" contacts are of the opposite polarity.

SWI1 Control by

This setting determines how the switch is to be controlled. This can be Local (using the device directly) remote (using a communications link), or both.

SWI1Trip/Close

This is a command t o directly trip or close the switch.

SWI1 Trp Puls T and ***SWI1 Cls Puls T***

These settings allow you to control the width of the open and close pulses.

SWI1 Sta Alrm T

This setting allows you to define the duration of wait timer before the relay raises a status alarm.

SWI1 Trp Fail T and ***SWI1 Cls Fail T***

These settings allow you to control the delay of the open and close alarms when the final switch status is not in line with expected status.

SWI1 Operations

This is a data cell, which displays the number of switch operations that have taken place. It is an accumulator, which you can reset using the ***Reset SWI1 Data*** setting

Reset SWI1 Data

This setting resets the switch monitoring data.

Note:
Settings for switch 1 are shown, but settings for all other switch elements are the same.

IEC 61850 protocol: The Switch position can be controlled in the 'CSWI' Logical Node that is linked to the 'XSWI' Switch Logical Node. For Control Authority as per IEC 61850, it is necessary to select ***SWx Control by*** cell as option 4 L/R Key.

13.10.1 SINGLE LINE DIAGRAM (SLD) VIEWER

The SLD menu displays the saved SLD on the graphical HMI screen. You can navigate to the SLD menu using the bottom Menu context keys or by using the quick launch menu on the Home page. The SLD is configured and uploaded into the IED using the S1 Agile configuration tool. Items of plant can be selected on the SLD screen using the navigation keypad.

13.10.2 SWITCH CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the switches selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the Switch Control by setting is selected to option 1 *LOCAL*, option 3 `Local+Remote` or option 4 `L/R Key` in the SWITCH CONTROL column, users are allowed to use the Open and Close Key on the front panel to operate the SWITCH.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***Switch Control by*** setting to `L/R Key`
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R Key LED is green and the REMOTE mode is selected. The **L/R Key Status** DDB status is stored in non-volatile memory, so that its status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant you want to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the OPEN or CLOSE key to operate

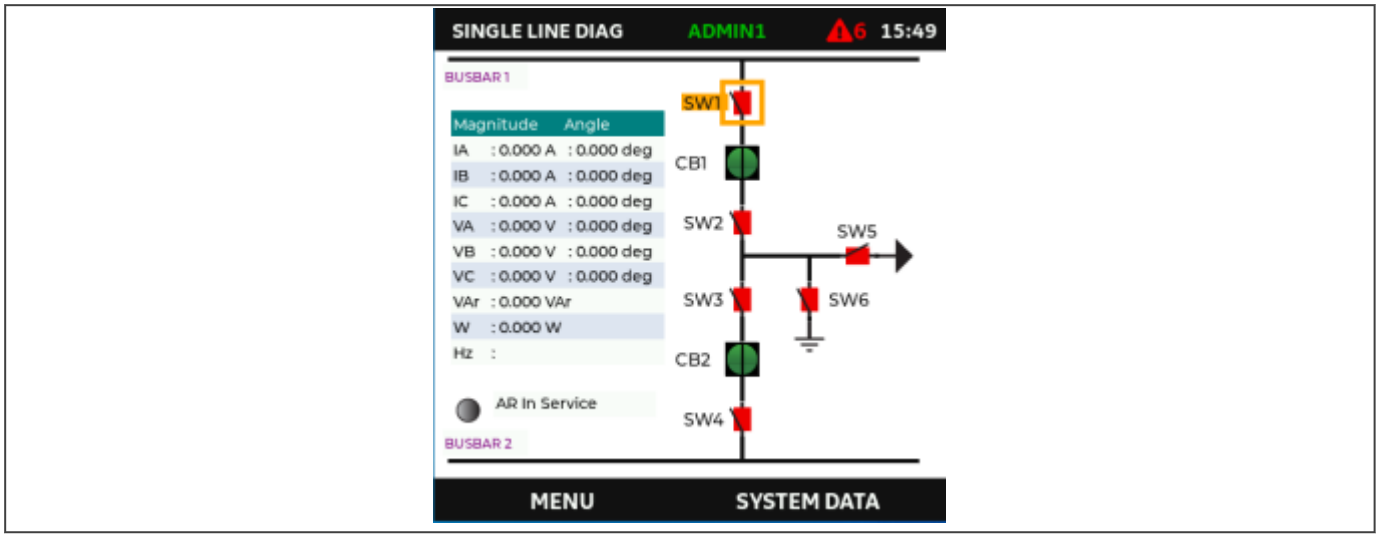


Figure 211: HMI SLD display

Figure 212: For the Switch Commands from HMI, these additional checks are done:

If the Switch is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "***Control by***" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - In Remote Control."

If the associated local DDB is set to local, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

13.10.3 SWITCH CONTROL LOGIC

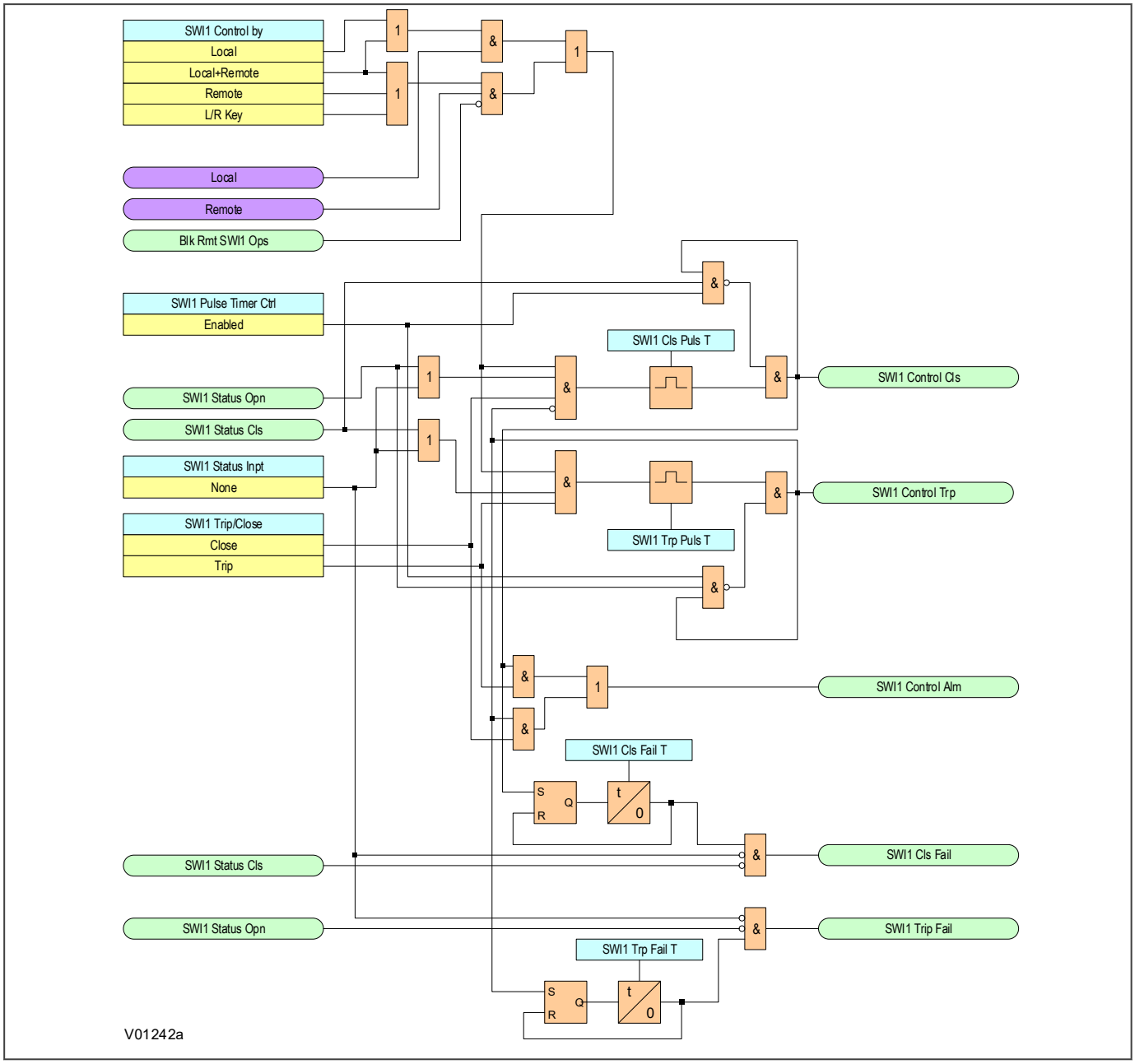


Figure 213: Switch control logic

13.10.4 SWITCH STATUS LOGIC

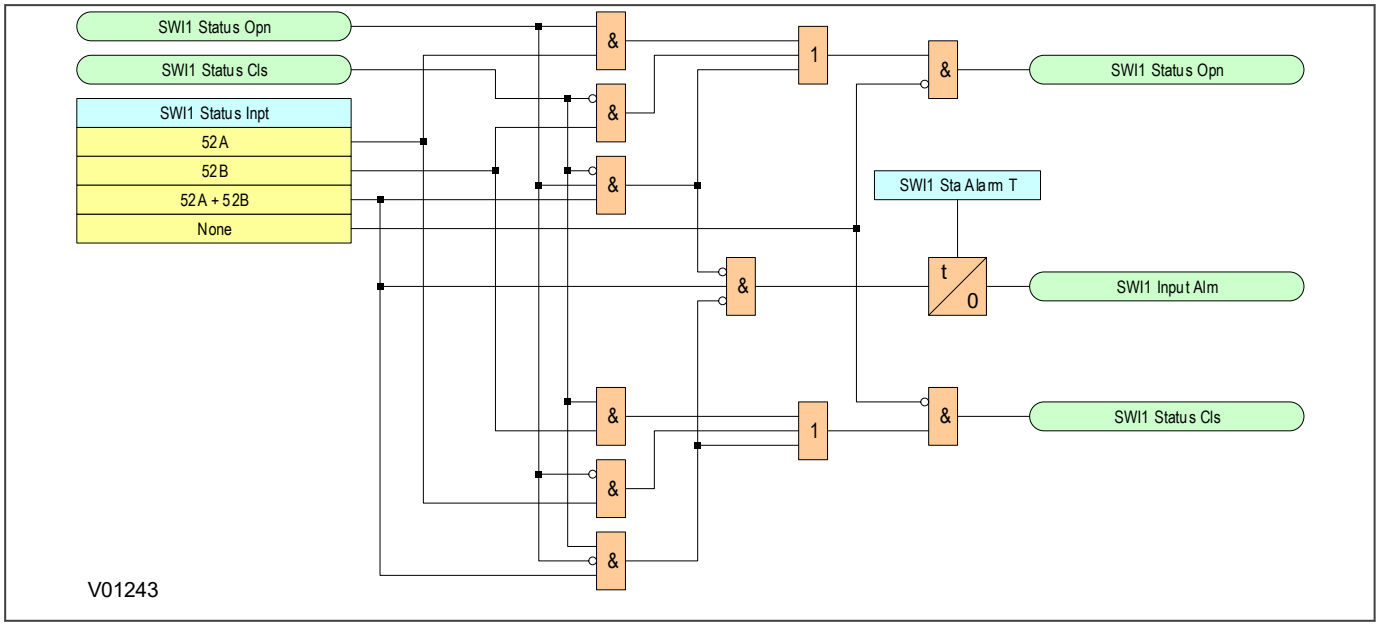


Figure 214: Switch status logic

13.11 TEST MODE

The behaviour of the IED is dependant on if it is in normal operation or in one of the Test Modes. This is reflected in some of the data that can be monitored and affects the allowed control operations, particularly using the IEC 61850 protocol.

The mode of operation is set using the ***IED Test Mode*** cell under the *COMMISSION TESTS* column. See the Commissioning Instructions chapter for more information.

When the IED is in either ***Test*** or ***Contacts Blocked*** mode, IEC 61850 status and measurement data will be transmitted with its quality parameter set to ***test***, so that the receiver understands that they have been issued by a device under test and can respond accordingly.

When the IED is in either ***Test*** or ***Contacts Blocked*** mode, the IED only responds to IEC 61850 MMS controls from the client with the 'test' flag set (with the exception of controls on System/LLN0.Mod).

You can select the mode of operation of the P40 IED by:

- Using the front panel HMI, with the setting ***IED Test Mode*** under the *COMMISSION TESTS* column
- Using an IEC 61850 MMS control service to ***System/LLN0.Mod***
- Using an opto-input via PSL with the signal ***Block Contacts***

The following table summarises the P40 IED behaviour under the different modes:

IED Test Mode Setting	IEC 61850 Mod	Result
Disabled	on	• Normal IED behaviour • IED only responds to incoming GOOSE and SV messages with quality q.test = false
Test	test	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are still active • IEC 61850 message outputs have 'quality' q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true
Contacts Blocked	test/blocked	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are disabled • IEC 61850 message outputs have quality q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true

Setting the Test or Contacts Blocked mode puts the whole IED into test mode. The IEC 61850 data object ***Beh*** in all Logical Nodes (except LPHD and any protection Logical Nodes that have Beh = 5 (off) due to the function being disabled) will be set to 3 (test) or 4 (test/blocked) as applicable.

13.12 IEC 61850 CONTROL AUTHORITY

Within the substation, control commands to the primary equipment, such as the breaker or disconnect/earth switches can be originated from one of four levels: Device, Bay, Station or Remote.

Device: Controls are issued manually at the device in the yard/GIS. Any commands from remote locations are not accepted. For this to happen the XCBR/XSWI.Loc object should be True. For P40 devices, the XCBR/XSWI.Loc is mapped to these DDBs:

DDB No.	DDB Name	Description
2186	LocKey Local	This DDB signal indicates that the IED is in local status
2187	SW1 Local	This DDB signal indicates that the switch 1 is in local status
2188	SW2 Local	This DDB signal indicates that the switch 2 is in local status
2189	SW3 Local	This DDB signal indicates that the switch 3 is in local status
2190	SW4 Local	This DDB signal indicates that the switch 4 is in local status
2191	SW5 Local	This DDB signal indicates that the switch 5 is in local status
2192	SW6 Local	This DDB signal indicates that the switch 6 is in local status
2193	SW7 Local	This DDB signal indicates that the switch 7 is in local status
2194	SW8 Local	This DDB signal indicates that the switch 8 is in local status
2195	CB1 Local	This DDB signal indicates that the CB1 is in local status
2196	CB2 Local	This DDB signal indicates that the CB2 is in local status
2197	CB3 Local	This DDB signal indicates that the CB3 is in local status
2198	CB4 Local	This DDB signal indicates that the CB4 is in local status
2199	CB5 Local	This DDB signal indicates that the CB4 is in local status

If the DDBs associated are not connected, the default is False which facilitates remote operations.

Bay: The commands are issued from the HMI of the P40. The P40 has a dedicated L/R Button for selection in the front face.

Key	Description	Function
	Local/Remote key	To select between local and remote operating modes.

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is Red and the Local mode is selected. When the DDB status is FALSE, the L/R Key LED is Green and the REMOTE mode is selected. The ***L/R Key Status*** DDB status is stored in non-volatile memory, so that its status is recovered after an IED power cycle.

Bay Level controls are possible from the HMI if the ***L/R Key Status*** is in Local. When L/R Key is in Local the IEC 61850 Signal, System\LLN0.Loc is set as True. When L/R Key is in Remote, and a control action is attempted, the User will be advised with a pop-up message of "Command Unavailable - in remote".

To facilitate integration of the IED into a wired Local/Remote control switch in a panel, an additional DDB L/R Key has been provided.

This is modelled into IEC 61850 System\LLN0.LocKey. The data object LocKey represents the status of a physical key switch and allows taking over the control authority, if the DDB is wired. If the DDB is used, and is set to 1, the IED Local/Remote (System\LLN0.Loc) automatically changes to Local. At this stage, it is not possible to change the

IED L/R Key to remote. If the DDB is set to 0, the IED L/R does not automatically change to Remote. If necessary, a user action is required to change the control authority to Remote.

Station/Remote: Station level commands are those originating from either the substation gateway or from the station HMI. Remote commands are from the remote Network Control Center (NCC).

The data object LocSta modelled in System\LLN0 shows the control authority at station level. If LocSta=True, control authority is at station level and control from remote is disabled. If LocSta=False, control commands are allowed from remote, e.g. network control center (NCC).

P40 devices also support the concept of Multiple Level Control authority. This is done via a dedicated datapoint in System\LLN0 known as MltLev. If true, authority control from multiple levels is allowed, otherwise no other control level is allowed.

Under certain operational conditions, such as during maintenance, it is necessary to block commands from one or more of these levels. The local/remote control feature (described in IEC 61850 7-4: Annex B) allows users to enable or disable control authority from one or more of the three levels, as illustrated in the tables below:

IEC 61850 commands originating from the various levels are differentiated using the Origin.OrCat attribute value in the IEC 61850 command.

If the control command is rejected by the P40 IED due to control authority check, the AddCause - Blocked-by-switching-hierarchy will be shown in the IEC 61850 Client.

Control Authority for Other Controllable Objects								
Device	**Switch**	**Bay Control**			**Manual Control at Front Panel**	**Command From**		
		Mode of Switching Authority for Local Control	**Local Control Behaviour**	**Control Authority at Station Level**		**OrCat**		
LLN0.Loc Key	**XCBR.Loc XWI.Loc**	**LLN0.Mlt Lev**	**CSWI.Loc**	**CSWI.Loc Sta**		**Bay**	**Station**	**Remote**
T	n.a.	F	n.a.	n.a.	AA	NA	NA	NA
F	T	F	T	n.a.	AA	NA	NA	NA
F	T	F	F	n.a.	NA	NA	NA	NA
F	F	F	T	n.a.	AA	NA	NA	NA
F	F	F	F	T	NA	NA	AA	NA
F	F	F	F	F	NA	NA	NA	AA
T	n.a.	T	n.a.	n.a.	AA	NA	NA	NA
F	T	T	T	n.a.	AA	NA	NA	NA
F	T	T	F	n.a.	NA	NA	NA	NA
F	F	T	T	n.a.	AA	NA	NA	NA
F	F	T	F	T	NA	AA	AA	NA
F	F	T	F	F	NA	AA	AA	AA

n.a. - Not Applicable
AA - Always Allowed
NA - Not Allowed

In addition to the CB/Switches, P40 devices follow the concept of Control Authority for other commands executed via IEC 61850. These include:

- Control Inputs
- Reset of Trip LED
- Enable/Disable of Protection, Check Sync and Auto Recloser
- Reset of demands and thermal measurements

Control Authority for Other Controllable Objects							
Device	**Bay Control**			**Manual Control at Front Panel**	**Command From**		
	Mode of Switching Authority for Local Control	**Local Control Behaviour**	**Control Authority at Station Level**		**OrCat**		
LLN0.Loc Key	**LLN0.Mlt Lev**	**LLN0.Loc**	**LLN0.Loc Sta**		**Bay**	**Station**	**Remote**
T	F	n.a.	n.a.	AA	NA	NA	NA
F	F	T	n.a.	AA	NA	NA	NA
F	F	F	T	AA	NA	AA	NA
F	F	F	F	AA	NA	NA	AA
T	T	n.a.	n.a.	AA	NA	NA	NA
F	T	T	n.a.	AA	NA	NA	NA
F	T	F	T	AA	AA	AA	NA
F	T	F	F	AA	AA	AA	AA
n.a. - Not Applicable AA - Always Allowed NA - Not Allowed							

IEC 61850 based control authority can be visualized from the P40 HMI.

This is under the COMMISSION TESTS Menu, under IEC 61850 Control Sub Menu:

Menu Text	Description	Min	Max	Default	Controllable
Multiple Level	Used to enable/disable the 'multi level control authority' feature for breaker/switch and other controls	Disabled	Enabled	Disabled	Yes
Station Level	Used to get control command of station authority from IEC 61850 Client	Disabled	Enabled	Disabled	No
Device Level	Used to show the IED local/remote status	Local	Remote	Local	No

Multiple Level Control Authority can be selected either via an IEC 61850 MMS Command or via selection from the menu item shown above.

Note:
The Control Authority only works if the Protocol is IEC 61850. For Legacy Protocols, the existing control mechanism remains.

Note:
For Control Authority for CB/Switches, it is mandatory to select the option of L/R for CB/Switches if IEC 61850 is used.

CHAPTER 14

SUPERVISION

14.1 CHAPTER OVERVIEW

This chapter describes the supervison functions.

This chapter contains the following sections:

14.2 VOLTAGE TRANSFORMER SUPERVISION

The Voltage Transformer Supervision (VTS) function is used to detect failure of the AC voltage inputs to the protection. This may be caused by voltage transformer faults, overloading, or faults on the wiring, which usually results in one or more of the voltage transformer fuses blowing.

If there is a failure of the AC voltage input, the IED could misinterpret this as a failure of the actual phase voltages on the power system, which could result in unnecessary tripping of a circuit breaker.

The VTS logic is designed to prevent such a situation by detecting voltage input failures, which are NOT caused by power system phase voltage failure, and automatically blocking associated voltage dependent protection elements. A time-delayed alarm output is available to warn of a VTS condition.

The following scenarios are possible with respect to the failure of the VT inputs.

- Loss of one or two-phase voltages
- Loss of all three-phase voltages under load conditions
- Absence of three-phase voltages upon line energisation

14.2.1 LOSS OF ONE OR TWO PHASE VOLTAGES

If the power system voltages are healthy, no Negative Phase Sequence (NPS) current will be present. If however, one or two of the AC voltage inputs are missing, there will be Negative Phase Sequence voltage present, even if the actual power system phase voltages are healthy. VTS works by detecting Negative Phase Sequence (NPS) voltage without the presence of Negative Phase Sequence current. So if there is NPS voltage present, but no NPS current, it is certain that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation. The use of negative sequence quantities ensures correct operation even where three-limb or V-connected VTs are used.

The Negative Sequence VTS Element is blocked by the ***Any Pole Dead*** DDB signal during ***SP AR Dead Time***. The resetting of the blocking signal is delayed by 240 ms after an ***Any Pole Dead*** condition disappears.

14.2.2 LOSS OF ALL THREE PHASE VOLTAGES

If all three voltage inputs are lost, there will be no Negative Phase Sequence quantities present, but the device will see that there is no voltage input. If this is caused by a power system failure, there will be a step change in the phase currents. However, if this is not caused by a power system failure, there will be no change in any of the phase currents. So if there is no measured voltage on any of the three phases and there is no change in any of the phase currents, this indicates that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation.

To avoid blocking VTS due to changing load condition, the superimposed current signal can only prevent operation of the VTS during the time window of 40 ms following the voltage collapse.

14.2.3 ABSENCE OF ALL THREE PHASE VOLTAGES ON LINE ENERGISATION

On line energisation there should be a change in the phase currents as a result of loading or line charging current. Under this condition we need an alternative method of detecting three-phase VT failure.

If there is no measured voltage on all three phases during line energisation, two conditions might apply:

- A three-phase VT failure
- A three-phase fault.

The first condition would require VTS to block the voltage-dependent functions.

In the second condition, voltage dependent functions should not be blocked, as tripping is required.

To differentiate between these two conditions an overcurrent level detector is used (***VTS I> Inhibit***). This prevents a VTS block from being issued in case of a genuine fault. This overcurrent level detector is only enabled for 240 ms following line energization (based on an ***All Poles Dead*** signal drop off). It must still be set below any three-phase fault along the line.

If the line is closed where a three-phase VT failure is present, the overcurrent detector will not operate and a VTS block will be applied. Closing onto a three-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

14.2.4 VTS IMPLEMENTATION

VTS is implemented in the *SUPERVISION* column of the relevant settings group.

The following settings are relevant for VT Supervision:

- ***VTS Mode***: determines the mode of operation (Measured + MCB, Measured Only, MCB Only)
- ***VTS Status***: determines whether the VTS Operate output will be a blocking output or an alarm indication only
- ***VTS Reset Mode***: determines whether the Reset is to be manual or automatic
- ***VTS Time Delay***: determines the operating time delay
- ***VTS I> Inhibit***: inhibits VTS operation in the case of a phase overcurrent fault
- ***VTS I2> Inhibit***: inhibits VTS operation in the case of a negative sequence overcurrent fault

For faults with I2 less than the setting ***VTS I2 Inhibit***, VTS will be active and block the associated functions if sufficient V2 is measured. VTS is only enabled during a live line condition (as indicated by the pole dead logic) to prevent operation under dead system conditions.

Thresholds

The negative sequence thresholds used by the element are:

- V2 = 10 V (fixed)
- I2 = 0.05 to 0.5 In settable (default 0.05 In).

The phase voltage level detectors are:

- Drop off = 10 V (fixed)
- Pickup = 30 V (fixed)

The sensitivity of the superimposed current elements is fixed at 0.1 In.

Fuse Fail

The device includes a setting (***VT Connected***) in the *CT AND VT RATIOS* column, which determines whether there are voltage transformers connected to it. If set to `No`, this setting has no effect.

If set to `No` it causes the VTS logic to set the ***VTS Slow Block*** and ***VTS Fast Block*** DDBs, but not raise any alarms. It also disables the VTS function. This prevents the pole dead logic working incorrectly if there is no voltage or current. It also blocks the distance, under voltage and other voltage-dependant functions. However, it does not affect the CB open part of the logic.

A VTS condition can be raised by a mini circuit breaker (MCB) status input, by internal logic using IED measurement, or both. The setting ***VTS Mode*** is used to select the method of indicating VT failure.

14.2.5 VTS LOGIC

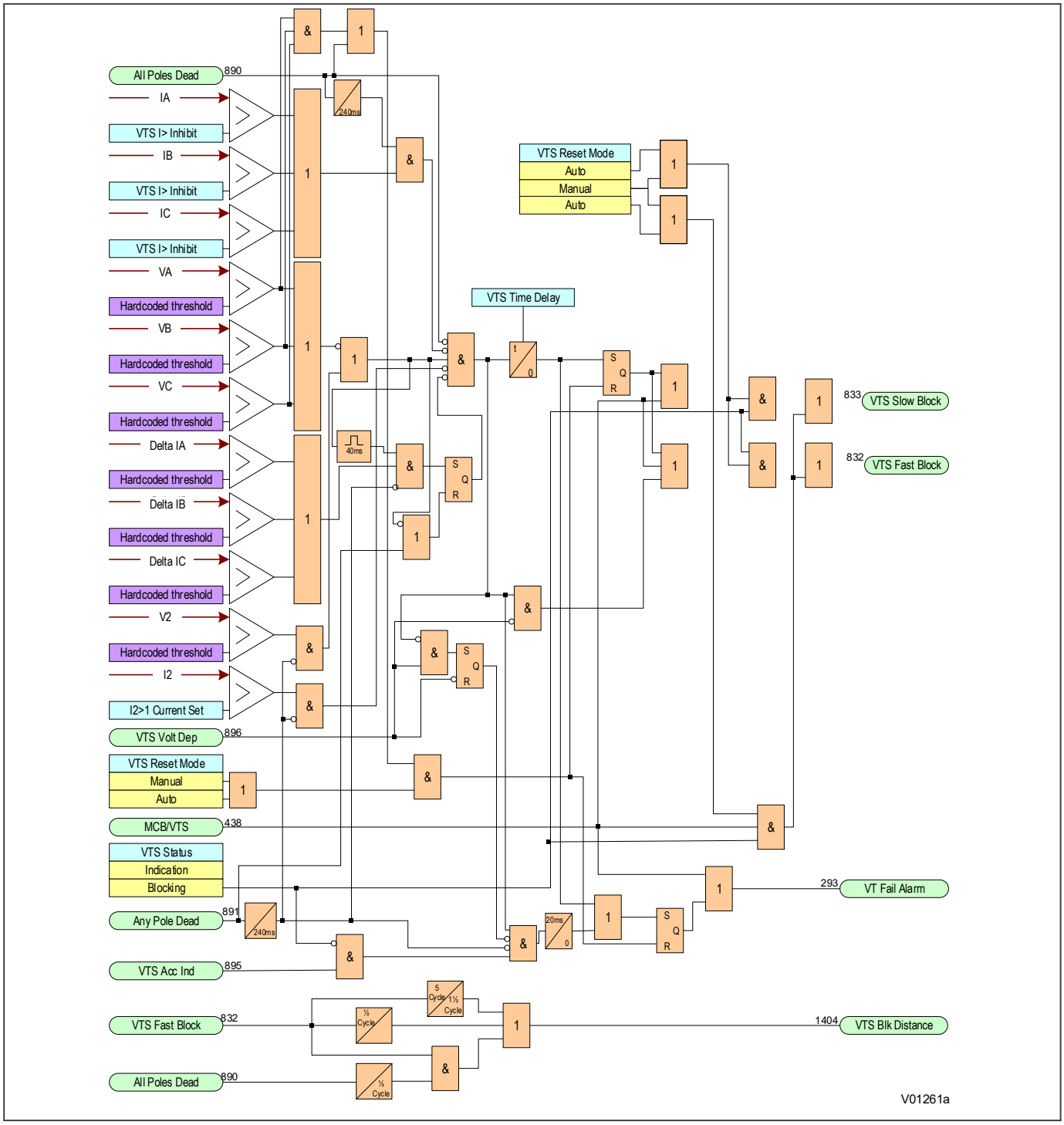


Figure 215: VTS logic

The IED may respond as follows, on operation of any VTS element:

- VTS set to provide alarm indication only
- Optional blocking of voltage-dependent protection elements
- Optional conversion of directional overcurrent elements to non-directional protection (by setting the relevant current protection status cells to `Enabled VTS`. In this case, the directional setting cells are automatically set to `non-directional`.)

The ***VTS I> Inhibit*** or ***VTS I2> Inhibit*** elements are used to override a VTS block if a fault occurs that could trigger the VTS logic. However, once the VTS block is set, subsequent system faults must not override the block. Therefore the VTS block is latched after a settable time delay (***VTS Time Delay***). Once the signal has latched, there are two methods of resetting. The first is manually using the front panel HMI, or remote communications (if the VTS condition has been removed). The second is in Auto mode, by restoring the 3 phase voltages above the phase level detector settings mentioned previously.

VTS Status can be set to `Disabled`, `Blocking` or `Indication`. If ***VTS Status*** is set to `Blocking`, a VTS condition will block operation of the relevant protection elements. In this case, a VTS indication is given after the ***VTS Time Delay*** has expired. If it is set to `Indication`, their is a risk of maloperation because protection elements are not blocked. In this case the VTS indication is given before the ***VTS Time Delay*** expires, if a trip signal is given (in this case a signal from the VTS acceleration logic is used as an input).

This scheme also operates correctly under very low load or even no load conditions. To achieve this, it uses a combination of time delayed signals derived from the DDB signals ***VTS Fast Block*** and ***All Poles Dead***, to generate the distance blocking DDB signal called ***VTS Blk Distance.***

Note:
*All non-distance voltage-dependent elements are blocked by the **VTS Fast Block** DDB.*

If a miniature circuit breaker (MCB) is used to protect the voltage transformer output circuits, MCB auxiliary contacts can be used to indicate a three-phase output disconnection. It is possible for the VTS logic to operate correctly without this input, but this facility has been provided to maintain compatibility with some practises. Energising an opto-isolated input assigned to the ***MCB/VTS*** provides the necessary block.

The VTS function is inhibited if:

- An ***All Poles Dead*** DDB signal is present
- Any phase overcurrent condition exists
- A Negative Phase Sequence current exists
- If the phase current changes over the period of 1 cycle

14.3 CURRENT TRANSFORMER SUPERVISION

The Current Transformer Supervision function (CTS) is used to detect failure of the AC current inputs to the protection. This may be caused by internal current transformer faults, overloading, or faults on the wiring. If there is a failure of the AC current input, the protection could misinterpret this as a failure of the actual phase currents on the power system, which could result in maloperation. Also, an open circuit in the AC current circuits can cause dangerous CT secondary voltages to be generated.

14.3.1 CTS IMPLEMENTATION

If the power system currents are healthy, no zero sequence voltage are derived. However, if one or more of the AC current inputs are missing, a zero sequence current would be derived, even if the actual power system phase currents are healthy. Standard CTS works by detecting a derived zero sequence current where there is no corresponding derived zero sequence voltage.

The voltage transformer connection used must be able to refer zero sequence voltages from the primary to the secondary side. Therefore, this element should only be enabled where the VT is of a five-limb construction, or comprises three single-phase units with the primary star point earthed.

The CTS function is implemented in the *SUPERVISION* column of the relevant settings group, under the sub-heading *CT SUPERVISION*.

The following settings are relevant for CT Supervision:

- ***CTS Status***: to disable or enable CTS
- ***CTS VN< Inhibit***: inhibits CTS if the zero sequence voltage exceeds this setting
- ***CTS IN> Set***: determines the level of zero sequence current
- ***CTS Time Delay***: determines the operating time delay

14.3.2 STANDARD CTS LOGIC

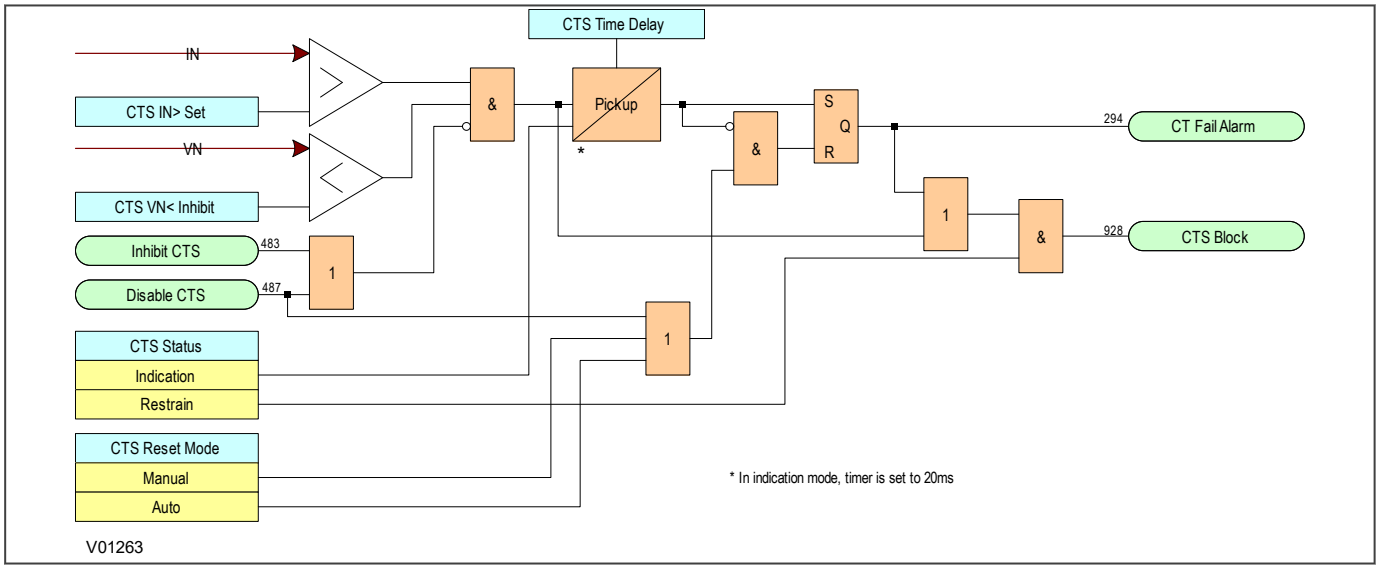


Figure 216: Standard CTS

14.3.3 CTS BLOCKING

Both the standard and differential CTS methods block protection elements operating from derived quantities, such as Broken conductor, derived earth fault and negative sequence overcurrent. Measured quantities such as DEF can be selectively blocked by designing an appropriate PSL scheme.

Differential CTS can be used to restrain the differential protection if required.

14.3.4 APPLICATION NOTES

14.3.4.1 SETTING GUIDELINES

The residual voltage setting, ***CTS VN< Inhibit*** and the residual current setting, ***CTS IN> Set***, should be set to avoid unwanted operation during healthy system conditions. For example:

- ***CTS VN< Inhibit*** should be set to 120% of the maximum steady state residual voltage.
- ***CTS IN> Set*** will typically be set below minimum load current.
- ***CTS Time Delay*** is generally set to 5 seconds.

Where the magnitude of residual voltage during an earth fault is unpredictable, the element can be disabled to prevent protection elements being blocked during fault conditions.

14.4 TRIP CIRCUIT SUPERVISION

In most protection schemes, the trip circuit extends beyond the IED enclosure and passes through components such as links, relay contacts, auxiliary switches and other terminal boards. Such complex arrangements may require dedicated schemes for their supervision.

There are two distinctly separate parts to the trip circuit; the trip path, and the trip coil. The trip path is the path between the IED enclosure and the CB cubicle. This path contains ancillary components such as cables, fuses and connectors. A break in this path is possible, so it is desirable to supervise this trip path and to raise an alarm if a break should appear in this path.

The trip coil itself is also part of the overall trip circuit, and it is also possible for the trip coil to develop an open-circuit fault.

This product supports a number of trip circuit supervision (TCS) schemes.

14.4.1 TRIP CIRCUIT SUPERVISION SCHEME 1

This scheme provides supervision of the trip coil with the CB open or closed, however, it does not provide supervision of the trip path whilst the breaker is open. The CB status can be monitored when a self-reset trip contact is used. However, this scheme is incompatible with latched trip contacts, as a latched contact will short out the opto-input for a time exceeding the recommended Delayed Drop-off (DDO) timer setting of 400 ms, and therefore does not support CB status monitoring. If you require CB status monitoring, further opto-inputs must be used.

Note:
A 52a CB auxiliary contact follows the CB position. A 52b auxiliary contact is the opposite.

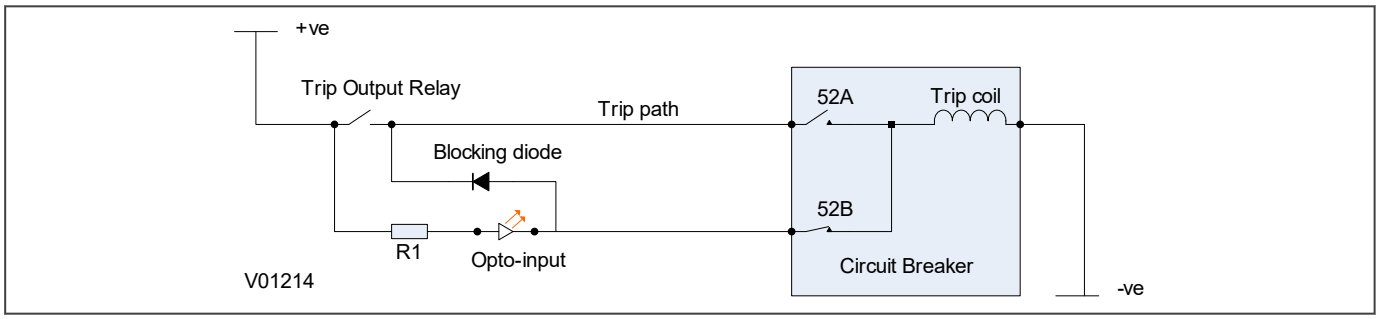


Figure 217: TCS Scheme 1

When the CB is closed, supervision current passes through the opto-input, blocking diode and trip coil. When the CB is open, supervision current flows through the opto-input and into the trip coil via the 52b auxiliary contact. This means that *Trip Coil* supervision is provided when the CB is either closed or open, however *Trip Path* supervision is only provided when the CB is closed. No supervision of the trip path is provided whilst the CB is open (pre-closing supervision). Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

14.4.1.1 RESISTOR VALUES

The supervision current is a lot less than the current required by the trip coil to trip a CB. The opto-input limits this supervision current to less than 10 mA. If the opto-input were to be short-circuited however, it could be possible for the supervision current to reach a level that could trip the CB. For this reason, a resistor R1 is often used to limit the current in the event of a short-circuited opto-input. This limits the current to less than 60mA. The table below shows the appropriate resistor value and voltage setting for this scheme.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 (ohms)
48/54	24/27	1.2k
110/125	48/54	2.7k
220/250	110/125	5.2k

Warning:
This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

14.4.1.2 PSL FOR TCS SCHEME 1

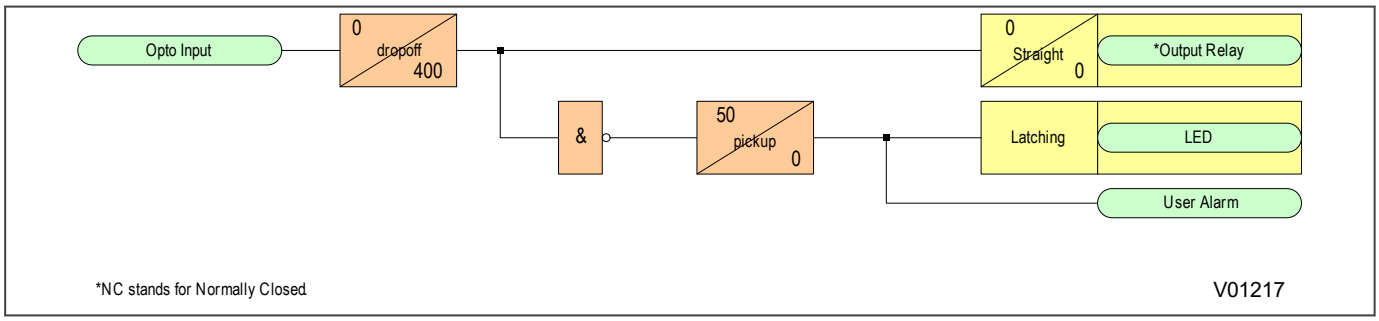


Figure 218: PSL for TCS Scheme 1

The opto-input can be used to drive a Normally Closed Output Relay, which in turn can be used to drive alarm equipment. The signal can also be inverted to drive a latching programmable LED and a user alarm DDB signal.

The DDO timer operates as soon as the opto-input is energised, but will take 400 ms to drop off/reset in the event of a trip circuit failure. The 400 ms delay prevents a false alarm due to voltage dips caused by faults in other circuits or during normal tripping operation when the opto-input is shorted by a self-reset trip contact. When the timer is operated the NC (normally closed) output relay opens and the LED and user alarms are reset.

The 50 ms delay on pick-up timer prevents false LED and user alarm indications during the power up time, following a voltage supply interruption.

14.4.2 TRIP CIRCUIT SUPERVISION SCHEME 2

This scheme provides supervision of the trip coil with the breaker open or closed but does not provide pre-closing supervision of the trip path. However, using two opto-inputs allows the IED to correctly monitor the circuit breaker status since they are connected in series with the CB auxiliary contacts. This is achieved by assigning one opto-input to the 52a contact and another opto-input to the 52b contact. Provided the ***CB Status*** setting in the *CB CONTROL* column is set to `Both 52A and 52B`, the IED will correctly monitor the status of the breaker. This scheme is also fully compatible with latched contacts as the supervision current will be maintained through the 52b contact when the trip contact is closed.

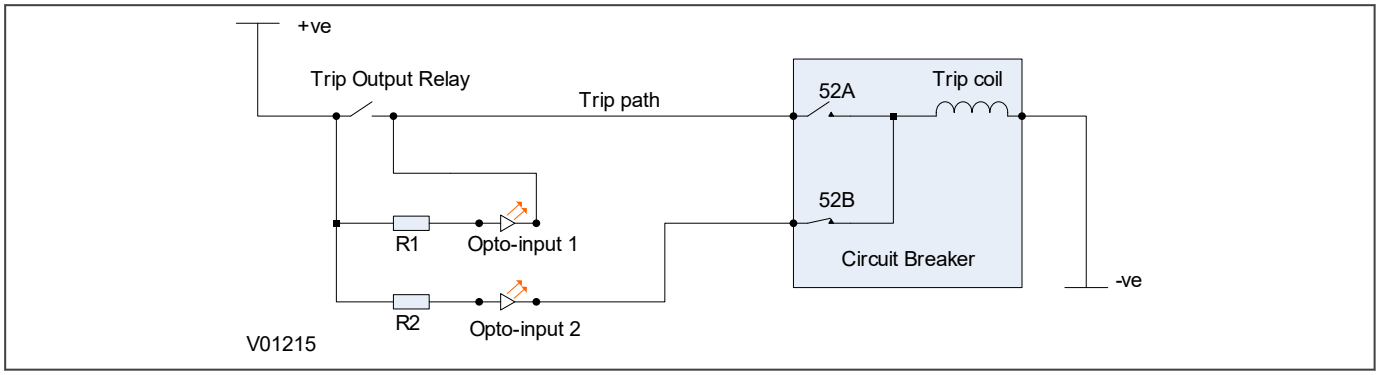


Figure 219: TCS Scheme 2

When the breaker is closed, supervision current passes through opto input 1 and the trip coil. When the breaker is open current flows through opto input 2 and the trip coil. No supervision of the trip path is provided whilst the breaker is open. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

14.4.2.1 RESISTOR VALUES

Optional resistors R1 and R2 can be added to prevent tripping of the CB if either opto-input is shorted. The table below shows the appropriate resistor value and voltage setting for this scheme.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 and R2 (ohms)
48/54	24/27	1.2k
110/125	48/54	2.7k
220/250	110/125	5.2k

Warning:
This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

14.4.2.2 PSL FOR TCS SCHEME 2

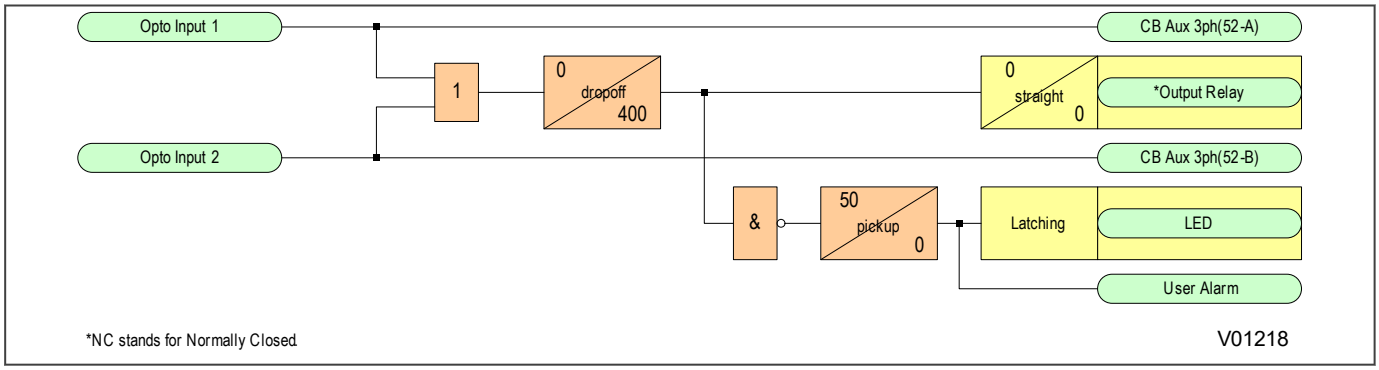


Figure 220: PSL for TCS Scheme 2

In TCS scheme 2, both opto-inputs must be low before a trip circuit fail alarm is given.

14.4.3 TRIP CIRCUIT SUPERVISION SCHEME 3

TCS Scheme 3 is designed to provide supervision of the trip coil with the breaker open or closed. It provides pre-closing supervision of the trip path. Since only one opto-input is used, this scheme is not compatible with latched trip contacts. If you require CB status monitoring, further opto-inputs must be used.

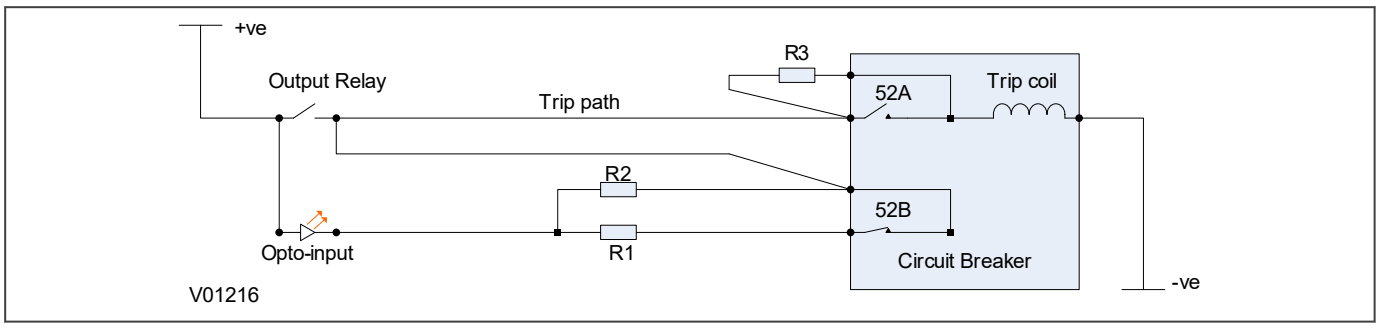


Figure 221: TCS Scheme 3

When the CB is closed, supervision current passes through the opto-input, resistor R2 and the trip coil. When the CB is open, current flows through the opto-input, resistors R1 and R2 (in parallel), resistor R3 and the trip coil. The supervision current is maintained through the trip path with the breaker in either state, therefore providing pre-closing supervision.

14.4.3.1 RESISTOR VALUES

Resistors R1 and R2 are used to prevent false tripping, if the opto-input is accidentally shorted. However, unlike the other two schemes. This scheme is dependent upon the position and value of these resistors. Removing them would result in incomplete trip circuit monitoring. The table below shows the resistor values and voltage settings required for satisfactory operation.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 & R2 (ohms)	Resistor R3 (ohms)
48/54	24/27	1.2k	600
110/250	48/54	2.7k	1.2k
220/250	110/125	5.0k	2.5k

Warning:
This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

14.4.3.2 PSL FOR TCS SCHEME 3

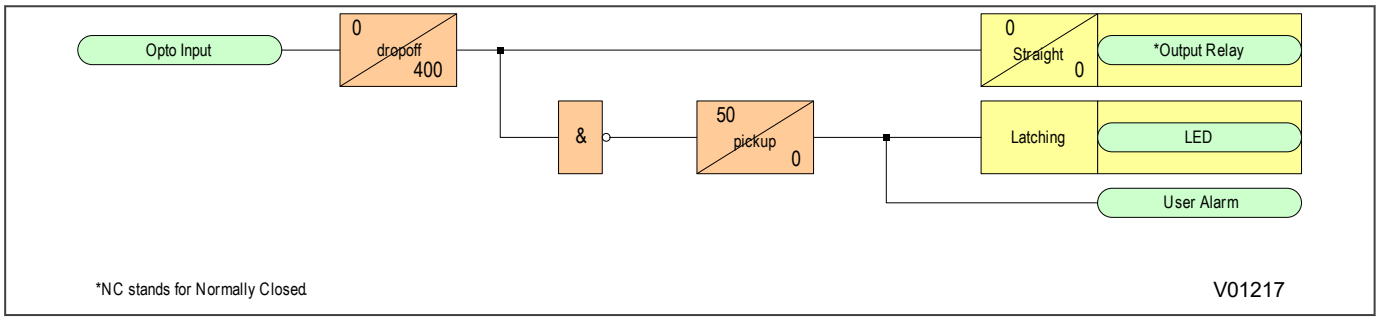


Figure 222: PSL for TCS Scheme 3

CHAPTER 15

DIGITAL I/O AND PSL CONFIGURATION

15.1 CHAPTER OVERVIEW

This chapter introduces the PSL (Programmable Scheme Logic) Editor, and describes the configuration of the digital inputs and outputs. It provides an outline of scheme logic concepts and the PSL Editor. This is followed by details about allocation of the digital inputs and outputs, which require the use of the PSL Editor. A separate "Settings Application Software" document is available that gives a comprehensive description of the PSL, but enough information is provided in this chapter to allow you to allocate the principal digital inputs and outputs.

This chapter contains the following sections:

15.2 CONFIGURING DIGITAL INPUTS AND OUTPUTS

Configuration of the digital inputs and outputs in this product is very flexible. You can use a combination of settings and programmable logic to customise them to your application. You can access some of the settings using the keypad on the front panel, but you will need a computer running the settings application software to fully interrogate and configure the properties of the digital inputs and outputs.

The settings application software includes an application called the PSL Editor (Programmable Scheme Logic Editor). The PSL Editor lets you allocate inputs and outputs according to your specific application. It also allows you to apply attributes to some of the signals such as a drop-off delay for an output contact.

In this product, digital inputs and outputs that are configurable are:

- Optically isolated digital inputs (opto-inputs). These can be used to monitor the status of associated plant.
- Output relays. These can be used for purposes such as initiating the tripping of circuit breakers, providing alarm signals, etc..
- Programmable LEDs. The number and colour of the programmable LEDs varies according to the particular product being applied.
- Function keys and associated LED indications. These are not provided on all products, but where they are, each function key has an associated tri-colour LED.
- IEC 61850 GOOSE inputs and outputs. These are only provided on products that have been specified for connection to an IEC61850 system, and the details of the GOOSE are presented in the documentation on IEC61850.

15.3 SCHEME LOGIC

The product is supplied with pre-loaded Fixed Scheme Logic (FSL) and Programmable Scheme Logic (PSL).

The Scheme Logic is a functional module within the IED, through which all mapping of inputs to outputs is handled. The scheme logic can be split into two parts; the Fixed Scheme Logic (FSL) and the Programmable Scheme Logic (PSL). It is built around a concept called the digital data bus (DDB). The DDB encompasses all of the digital signals (DDBs) which are used in the FSL and PSL. The DDBs included digital inputs, outputs, and internal signals.

The FSL is logic that has been hard-coded in the product. It is fundamental to correct interaction between various protection and/or control elements. It is fixed and cannot be changed.

The PSL gives you a facility to develop custom schemes to suit your application if the factory-programmed default PSL schemes do not meet your needs. Default PSL schemes are programmed before the product leaves the factory. These default PSL schemes have been designed to suit typical applications and if these schemes suit your requirements, you do not need to take any action. However, if you want to change the input-output mappings, or to implement custom scheme logic, you can change these, or create new PSL schemes using the PSL editor.

The PSL consists of components such as logic gates and timers, which combine and condition DDB signals.

The logic gates can be programmed to perform a range of different logic functions. The number of inputs to a logic gate are not limited. The timers can be used either to create a programmable delay or to condition the logic outputs. Output contacts and programmable LEDs have dedicated conditioners.

The PSL logic is event driven. Only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This minimises the amount of processing time used by the PSL ensuring industry leading performance.

The following diagram shows how the scheme logic interacts with the rest of the IED.

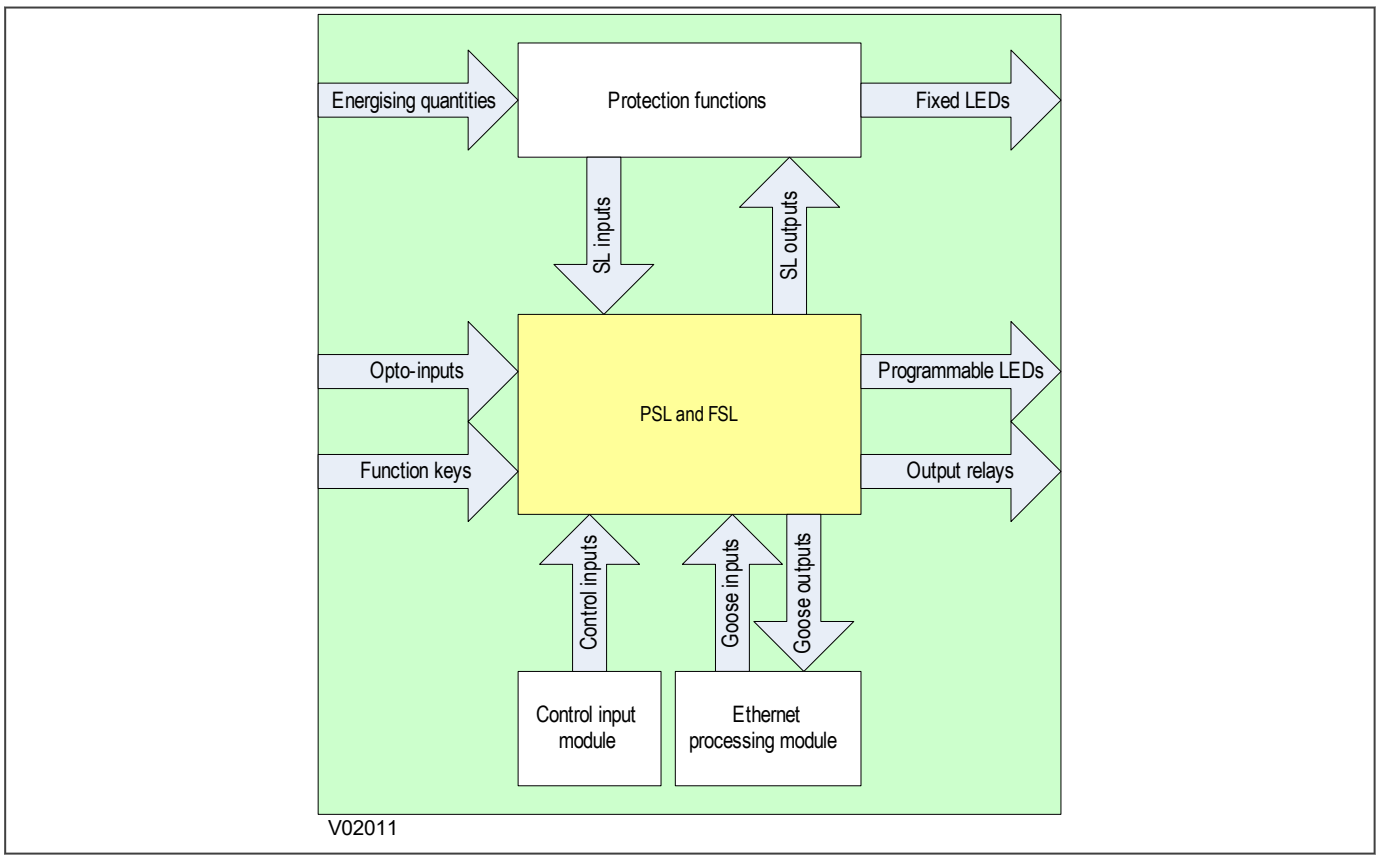


Figure 223: Scheme Logic Interfaces

15.3.1 PSL EDITOR

The Programmable Scheme Logic (PSL) is a module of programmable logic gates and timers in the IED, which can be used to create customised logic to qualify how the product manages its response to system conditions. The IED's digital inputs are combined with internally generated digital signals using logic gates, timers, and conditioners. The resultant signals are then mapped to digital outputs signals including output relays and LEDs.

The PSL Editor is a tool in the settings application software that allows you to create and edit scheme logic diagrams. You can use the default scheme logic which has been designed to suit most applications, but if it does not suit your application you can change it. If you create a different scheme logic with the software, you need to upload it to the device to apply it.

15.3.2 PSL SCHEMES

Your product is shipped with default scheme files. These can be used without modification for most applications, or you can choose to use them as a starting point to design your own scheme. You can also create a new scheme from scratch. To create a new scheme, or to modify an existing scheme, you will need to launch the settings application software. You then need to open an existing PSL file, or create a new one, for the particular product that you are using, and then open a PSL file. If you want to create a new PSL file, you should select **File** then **New** then **Blank scheme...** This action opens a default file appropriate for the device in question, but deletes the diagram components from the default file to leave an empty diagram with configuration information loaded. To open an existing file, or a default file, simply double-click on it.

15.3.3 PSL SCHEME VERSION CONTROL

To help you keep track of the PSL loaded into products, a version control feature is included. The user interface contains a *PSL DATA* column, which can be used to track PSL modifications. A total of 12 cells are contained in the *PSL DATA* column; 3 for each setting group.

Grp(n) PSL Ref: When downloading a PSL scheme to an IED, you will be prompted to enter the relevant group number and a reference identifier. The first 32 characters of the reference identifier are displayed in this cell. The horizontal cursor keys can scroll through the 32 characters as the LCD display only displays 16 characters.

Example:

```
Grp(n) PSL Ref
```

Date/time: This cell displays the date and time when the PSL scheme was downloaded to the IED.

Example:

```
18 Nov 2002
08:59:32.047
```

Grp(n) PSL ID: This cell displays a unique ID number for the downloaded PSL scheme.

Example:

```
Grp(n) PSL ID
ID - 2062813232
```

15.4 CONFIGURING THE OPTO-INPUTS

The number of optically isolated status inputs (opto-inputs) depends on the specific model supplied. The use of the inputs will depend on the application, and their allocation is defined in the programmable scheme logic (PSL). In addition to the PSL assignment, you also need to specify the expected input voltage. Generally, all opto-inputs will share the same input voltage range, but if different voltage ranges are being used, this device can accommodate them.

In the *OPTO CONFIG* column there is a global nominal voltage setting. If all opto-inputs are going to be energised from the same voltage range, you select the appropriate value in the setting. If you select `Custom` in the setting, then the cells ***Opto Input 1***, ***Opto Input 2***, etc. become visible. You use these cells to set the voltage ranges for each individual opto-input.

Within the *OPTO CONFIG* column there are also settings to control the filtering applied to the inputs, as well as the pick-up/drop-off characteristic.

The filter control setting provides a bit string with a bit associated with all opto-inputs. Setting the bit to '1' means that a half-cycle filter is applied to the inputs. This helps to prevent incorrect operation in the event of power system frequency interference on the wiring. Setting the field to '0' removes the filter and provides for faster operation.

The ***Characteristic*** setting is a single setting that applies to all the opto-inputs. It is used to set the pick-up/drop-off ratios of the input signals. As standard it is set to 80% pick-up and 60% drop-off, but you can change it to other available thresholds if that suits your operational requirements.

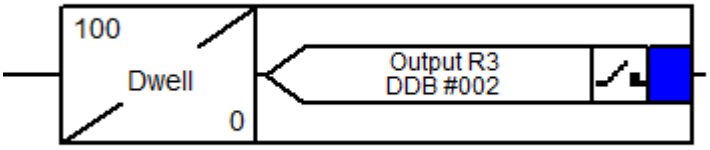
15.5 ASSIGNING THE OUTPUT RELAYS

Relay contact action is controlled using the PSL. DDB signals are mapped in the PSL and drive the output relays. The driving of an output relay is controlled by means of a relay output conditioner. Several choices are available for how output relay contacts are conditioned. For example, you can choose whether operation of an output relay contact is latched, has delay on pick-up, or has a delay on drop-off. You make this choice in the **Contact Properties** window associated with the output relay conditioner.

To map an output relay in the PSL you should use the Contact Conditioner button in the toolbar to import it. You then condition it according to your needs. The output of the conditioner respects the attributes you have assigned.

The toolbar button for a Contact Conditioner looks like this:

The PSL contribution that it delivers looks like this:



Note:
Contact Conditioners are only available if they have not all been used. In some default PSL schemes, all Contact Conditioners might have been used. If that is the case, and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the relay outputs. The button looks like this:

This is the "Contact Signal" button. It allows you to put replica instances of a conditioned output relay into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

15.6 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

15.6.1 TRIP LED LOGIC

When a trip occurs, the trip LED is illuminated. It is possible to reset this with a number of ways:

- Directly with a reset command (by pressing the Clear Key)
- With a reset logic input
- With self-resetting logic

You enable the automatic self-resetting with the ***Sys Fn Links*** cell in the *SYSTEM DATA* column. A '0' disables self resetting and a '1' enables self resetting.

The reset occurs when the circuit is reclosed and the ***Any Pole Dead*** signal has been reset for three seconds providing the ***Any Start*** signal is inactive. The reset is prevented if the ***Any Start*** signal is active after the breaker closes.

The Trip LED logic is as follows:

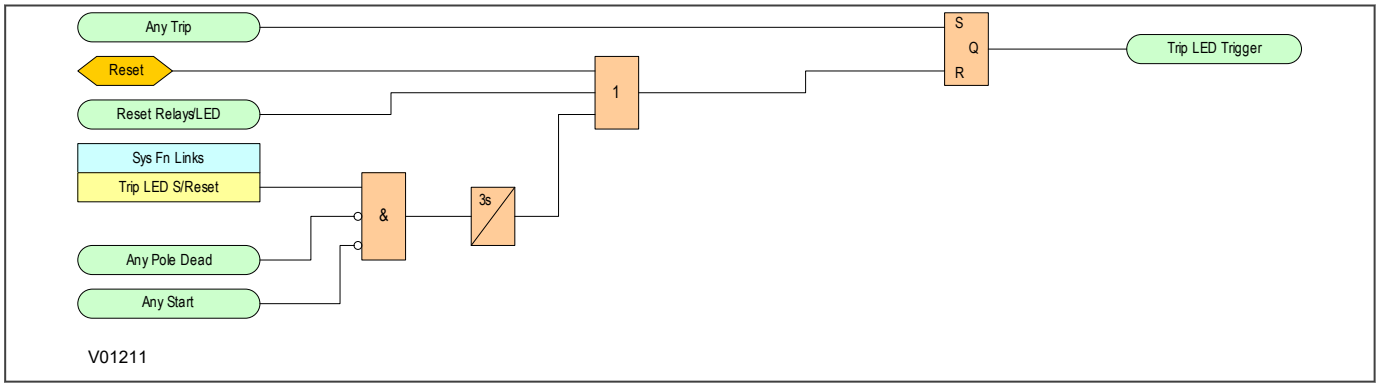


Figure 224: Trip LED logic

15.7 CONFIGURING PROGRAMMABLE LEDS

There are three types of programmable LED signals which vary according to the model being used. These are:

- Single-colour programmable LED. These are red when illuminated.
- Tri-colour programmable LED. These can be illuminated red, green, or amber.
- Tri-colour programmable LED associated with a Function Key. These can be illuminated red, green, or amber.

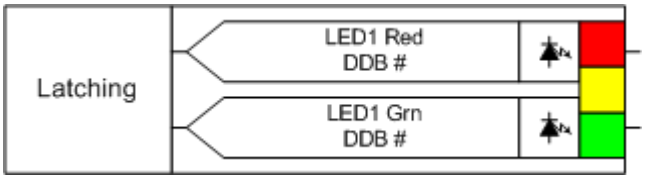
DDB signals are mapped in the PSL and used to illuminate the LEDs. For single-coloured programmable LEDs there is one DDB signal per LED. For tri-coloured LEDs there are two DDB signals associated with the LED. Asserting ***LED # Grn*** will illuminate the LED green. Asserting ***LED # Red*** will illuminate the LED red. Asserting both DDB signals will illuminate the LED amber.

The illumination of an LED is controlled by means of a conditioner. Using the conditioner, you can decide whether the LEDs reflect the real-time state of the DDB signals, or whether illumination is latched pending user intervention.

To map an LED in the PSL you should use the LED Conditioner button in the toolbar to import it. You then condition it according to your needs. The output(s) of the conditioner respect the attribute you have assigned.

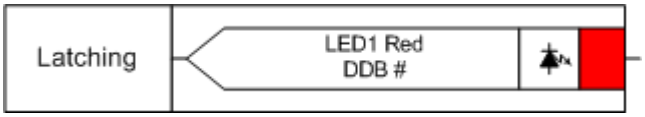
The toolbar button for a tri-colour LED looks like this:

The PSL contribution that it delivers looks like this:



The toolbar button for a single-colour LED looks like this:

The PSL contribution that it delivers looks like this.



Note:
LED Conditioners are only available if they have not all been used up, and in some default PSL schemes they might be. If that is the case and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the LEDs. For a tri-coloured LED the button looks like this:

For a single-colour LED it looks like this:

It is the "LED Signal" button. It allows you to put replica instances of a conditioned LED into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

Note:
All LED DDB signals are always shown in the PSL Editor. However, the actual number of LEDs depends on the device hardware. For example, if a small 20TE device has only 4 programmable LEDs, LEDs 5-8 will not take effect even if they are mapped in the PSL.

15.8 FUNCTION KEYS

For most models, a number of programmable function keys are available. This allows you to assign function keys to control functionality via the programmable scheme logic (PSL). Each function key is associated with a programmable tri-colour LED, which you can program to give the desired indication on activation of the function key.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are found in the *FUNCTION KEYS* column.

Each function key is associated with a DDB signal as shown in the DDB table. You can map these DDB signals to any function available in the PSL.

The ***Fn Key Status*** cell displays the status (energised or de-energised) of the function keys by means of a binary string, where each bit represents a function key starting with bit 0 for function key 1.

Each function key has three settings associated with it, as shown:

- ***Fn Key (n)***, which enables or disables the function key
- ***Fn Key (n) Mode***, which allows you to configure the key as toggled or normal
- ***Fn Key (n) label***, which allows you to define the function key text that is displayed

The ***Fn Key (n)*** cell is used to enable (unlock) or disable (unlock) the function key signals in PSL. The Lock setting has been provided to prevent further activation on subsequent key presses. This allows function keys that are set to `Toggled` mode and their DDB signal active 'high', to be locked in their active state therefore preventing any further key presses from deactivating the associated function. Locking a function key that is set to the "Normal" mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

When the ***Fn Key (n) Mode*** cell is set to `Toggle`, the function key DDB signal output will remain in the set state until a reset command is given. In the `Normal` mode, the function key DDB signal will remain energised for as long as the function key is pressed and will then reset automatically. In this mode, a minimum pulse duration can be programmed by adding a minimum pulse timer to the function key DDB output signal.

The ***Fn Key Label*** cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of all function keys are recorded in non-volatile memory. In case of auxiliary supply interruption their status will be maintained.

Note:
All function key DDB signals are always shown in the PSL Editor. However, the actual number of function keys depends on the device hardware. For example, if a small 20TE device has no function keys, the function key DDBs mapped in the PSL will not take effect.

15.9 CONTROL INPUTS

The control inputs are software switches, which can be set or reset locally or remotely. These inputs can be used to trigger any PSL function to which they are connected. There are three setting columns associated with the control inputs: *CONTROL INPUTS*, *CTRL I/P CONFIG* and *CTRL I/P LABELS*. These are listed in the Settings and Records appendix at the end of this manual.

15.10 USER ALARMS

User Alarms can be operated from an opto input or a control input using the PSL. They are useful for giving an alarm led and message on the LCD display, and an alarm indication via the communications of an external condition - for example: trip circuit supervision alarm, and temperature alarm etc. In the ***USER ALARMS*** menu, the ***Manual Reset*** 32 bit binary string (0 self-reset, 1 manual reset) can be used to set the operating mode of the user alarms to self or manual reset. The ***User Alarm 1-32*** labels in the ***USER ALARMS*** menu column are used to individually label each user alarm. The text is restricted to 16 characters.

CHAPTER 16

ELECTRICAL TELEPROTECTION

16.1 CHAPTER OVERVIEW

This chapter contains the following sections:

16.2 INTRODUCTION

Electrical Teleprotection is an optional feature that uses communications links to create protection schemes. It can be used to replace hard wiring between dedicated relay output contacts and digital input circuits. Two products equipped with electrical teleprotection can connect and exchange commands using a communication link. It is typically used to implement teleprotection schemes.

Using full duplex communications, eight binary command signals can be sent in each direction between connected products. The communication connection complies with the EIA(RS)232 standard. Ports may be connected directly, or using modems. Alternatively EIA(RS)232 converters can be used for connecting to other media such as optical fibres.

Communications statistics and diagnostics enable you to monitor the integrity of the communications link, and a loopback feature is available to help with testing.

16.3 TELEPROTECTION SCHEME PRINCIPLES

Teleprotection schemes use signalling to convey a trip command to remote circuit breakers to isolate circuits. Three types of teleprotection commands are commonly encountered:

- Direct Tripping
- Permissive Tripping
- Blocking Scheme

16.3.1 DIRECT TRIPPING

In direct tripping applications (often described by the generic term: “intertripping”), teleprotection signals are sent directly to a master trip device. Receipt of a command causes circuit breaker operation without any further qualification. Communication must be reliable and secure because any signal detected at the receiving end causes a trip of the circuit at that end. The communications system must be designed so that interference on the communication circuit does not cause spurious trips. If a spurious trip occurs, the primary system might be unnecessarily isolated.

16.3.2 PERMISSIVE TRIPPING

Permissive trip commands are monitored by a protection device. The circuit breaker is tripped when receipt of the command coincides with a ‘start’ condition being detected by the protection at the receiving. Requirements for the communications channel are less onerous than for direct tripping schemes, since receipt of an incorrect signal must coincide with a ‘start’ of the receiving end protection for a trip operation to take place. Permissive tripping is used to speed up tripping for faults occurring within a protected zone.

16.4 IMPLEMENTATION

Electrical InterMiCOM is configured using a combination of settings in the *INTERMICOM COMMS* column, settings in the *INTERMICOM CONF* column, and the programmable scheme logic (PSL).

The eight command signals are mapped to DDB signals within the product using the PSL.

Signals being sent to a remote terminal are referenced in the PSL as ***IM Output 1*** - ***IM Output 8***. Signals received from the remote terminal are referenced as ***IM Input 1*** - ***IM Input 8***.

Note:
As well as the optional Modem InterMiCOM, some products are available with a feature called InterMiCOM64 (IM64). The functionality and assignment of commands in InterMiCOM and InterMiCOM64 are similar, but they act independently and are configured independently.

16.5 CONFIGURATION

Electrical Teleprotection is compliant with IEC 60834-1:1999. For your application, you can customise individual command signals to the differing requirements of security, speed, and dependability as defined in this standard.

You customise the command signals using the ***IM# Cmd Type*** cell in the *INTERMICOM CONF* column.

Any command signal can be configured for:

- Direct intertripping by selecting 'Direct'. (this is the most secure signalling but incurs a time delay to deliver the security).
- Blocking applications by selecting 'Blocking'. (this is the fastest signalling)
- Permissive intertripping applications by selecting 'Permissive. (this is dependable signalling that balances speed and security)

You can also select to 'Disable' the command.

> *Note:*
> *When used in the context of a setting, '#' specifies which command signal (1-8) bit is being configured.*

To ensure that command signals are processed only by their intended recipient, the command signals are packaged into a message (sometimes referred to as a telegram) which contains an address field. A sending device sets a pattern in this field. A receiving device must be set to match this pattern in the address field before the commands will be acted upon. 10 patterns have been carefully chosen for maximum security. You need to choose which ones to use, and set them using the ***Source Address*** and ***Receive Address*** cells in the *INTERMICOM COMMS* column.

The value set in the ***Source Address*** of the transmitting device should match that set in the ***Receive Address*** of the receiving device. For example set ***Source Address*** to `1` at a local terminal and set ***Receive Address*** to `1` at the remote terminal.

The Source Address and Receive Address settings in the device should be set to different values to avoid false operation under inadvertent loopback conditions.

Where more than one pair of devices is likely to share a communication link, you should set each pair to use a different pair of address values.

Electrical InterMiCOM has been designed to be resilient to noise on communications links, but during severe noise conditions, the communication may fail. If this is the case, an alarm is raised and you can choose how the input signals are managed using the ***IM# FallBackMode*** cell in the *INTERMICOM CONF* column:

• If you choose `Latched`, the last valid command to be received can be maintained until a new valid message is received.

• If you choose `Default`, the signal will revert to a default value after the period defined in the ***IM# FrameSyncTim*** setting has expired. You choose the default value using the ***IM# DefaultValue*** setting.

Subsequent receipt of a full valid message will reset the alarm, and the new command signals will be used.

As well as the settings described above, you will need to assign input and output signals in the Programmable Scheme Logic (PSL). Use the 'Integral Tripping' buttons to create the logic you want to apply. A typical example is shown below.

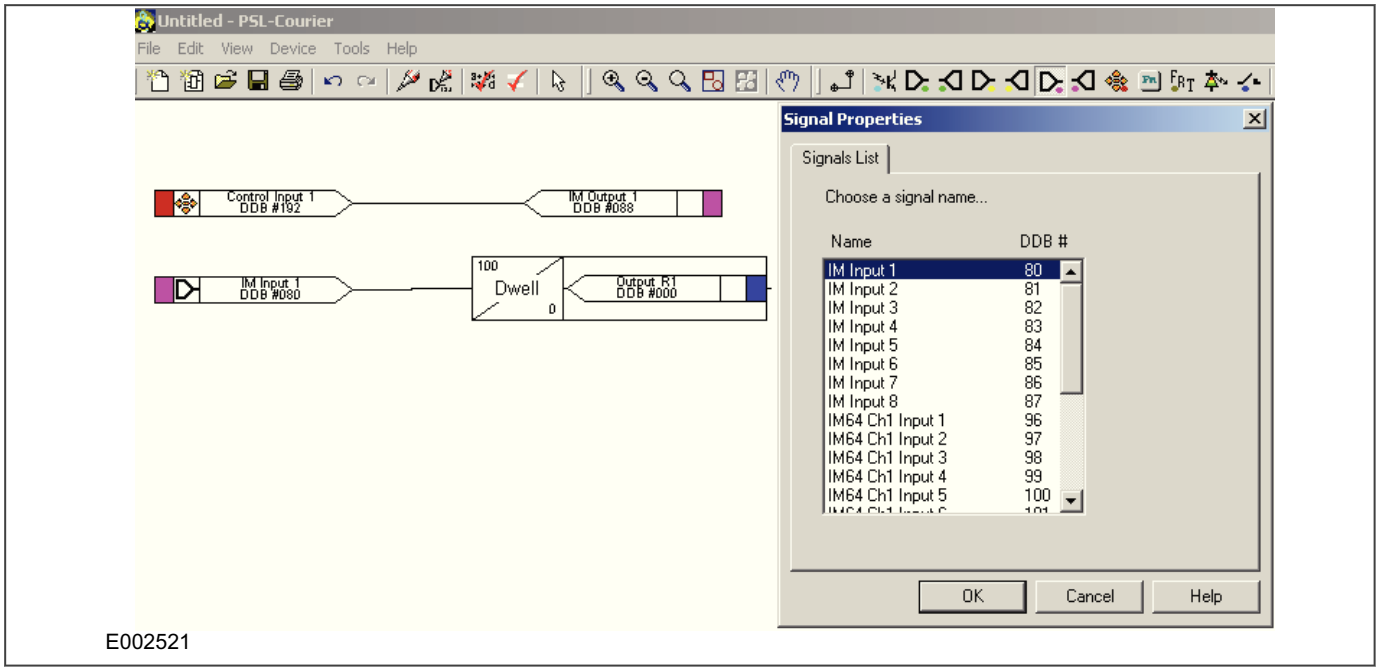


Figure 225: Example assignment of InterMiCOM signals within the PSL

Note:
When an Electrical InterMiCOM signal is sent from a local terminal, only the remote terminal will react to the command. The local terminal will only react to commands initiated at the remote terminal.

16.6 CONNECTING TO ELECTRICAL INTERMICOM

Electrical InterMiCOM uses EIA(RS)232 communication presented on a 9-pin 'D' type connector. The connector is labelled SK5 and is located at the bottom of the 2nd Rear communication board. The port is configured as standard DTE (Data Terminating Equipment).

16.6.1 SHORT DISTANCE

EIA(RS)232 is suitable for short distance connections only - less than 15m. Where this limitation is not a problem, direct connection between devices is possible. For this case, inter-device connections should be made as shown below the figure below.

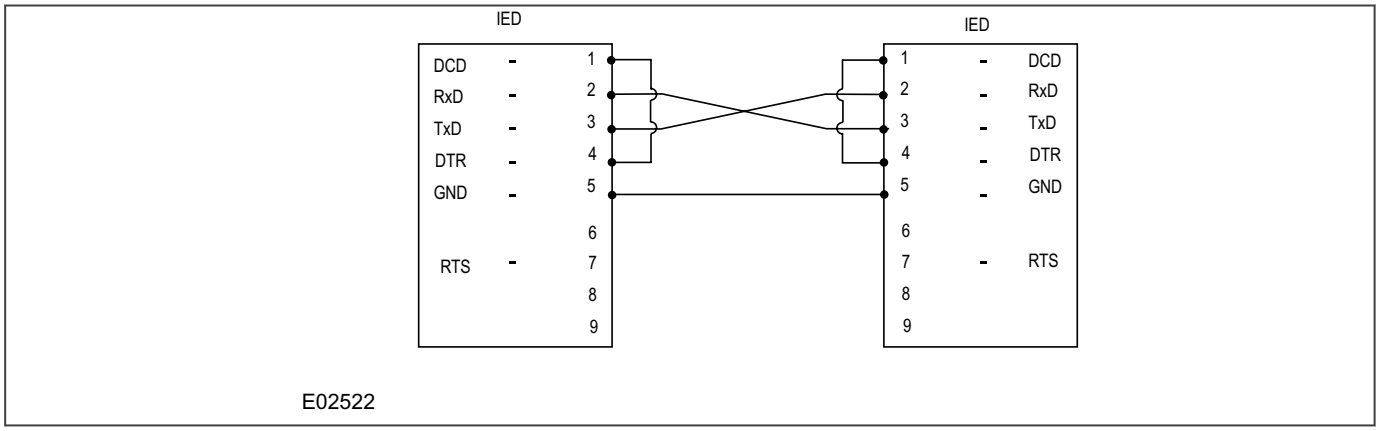


Figure 226: Direct connection

For direct connection, the maximum baud rate can generally be used.

16.6.2 LONG DISTANCE

EIA(RS)232 is suitable for short distance connections only - less than 15m. Where this limitation is a problem, direct connection between devices is not possible. For this case, inter-device connections should be made as shown below the figure below.

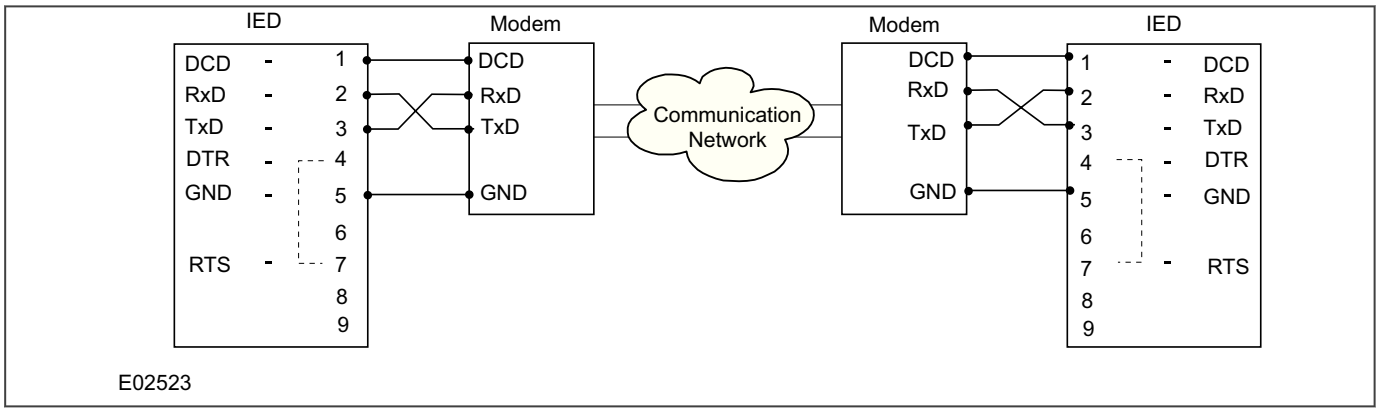


Figure 227: Indirect connection using modems

This type of connection should be used when connecting to devices that have the ability to control the DCD line. The baud rate should be chosen to be suitable for the communications network. If the Modem does not support the DCD function, the DCD terminal on the IED should be connected to the DTR terminal.

16.7 APPLICATION NOTES

Electrical InterMiCOM settings are contained within two columns; *INTERMICOM COMMS* and *INTERMICOM CONF*. The *INTERMICOM COMMS* column contains all the settings needed to configure the communications, as well as the channel statistics and diagnostic facilities. The *INTERMICOM CONF* column sets the mode of each command signal and defines how they operate in case of signalling failure.

Short metallic direct connections and connections using fire-optic converters will generally be set to have the highest signalling speed of 19200b/s. Due to this high signalling rate, the difference in operating time between the direct, permissive, and blocking type signals is small. This means you can select the most secure signalling command type ('Direct' intertrip) for all commands. You do this with the ***IM# Cmd Type*** settings. For these applications you should set the ***IM# Fallback Mode*** to `Default`. You should also set a minimal intentional delay by setting ***IM# FrameSyncTim*** to 10 msecs. This ensures that whenever two consecutive corrupt messages are received, the command will immediately revert to the default value until a new valid message is received.

For applications that use Modem and/or multiplexed connections, the trade-off between speed, security, and dependability is more critical. Choosing the fastest baud rate (data rate) to achieve maximum speed may appear attractive, but this is likely to increase the cost of the telecommunications equipment. Also, telecommunication services operating at high data rates are more prone to interference and suffer from longer re-synchronisation times following periods of disruption. Taking into account these factors we recommend a maximum baud rate setting of 9600 bps. As baud rates decrease, communications become more robust with fewer interruptions, but overall signalling times increase.

At slower baud rates, the choice of signalling mode becomes significant. You should also consider what happens during periods of noise when message structure and content can be lost.

- In 'Blocking' mode, the likelihood of receiving a command in a noisy environment is high. In this case, we recommend you set ***IM# Fallback Mode*** to `Default`, with a reasonably long ***IM# FrameSyncTim*** setting. Set ***IM# DefaultValue*** to '1'. This provides a substitute for a received blocking signal, applying a failsafe for blocking schemes.
- In 'Direct' mode, the likelihood of receiving commands in a noisy environment is small. In this case, we recommend you set ***IM# Fallback Mode*** to `Default` with a short ***IM# FrameSyncTim*** setting. Set ***IM# DefaultValue*** to '0'. This means that if a corrupt message is received, InterMiCOM will use the default value. This provides a substitute for the intertrip signal not being received, applying a failsafe for direct intertripping schemes.
- In 'Permissive' mode, the likelihood of receiving a valid command under noisy communications conditions is somwhere between that of the 'Blocking' mode and the 'Direct' intertrip mode. In this case, we recommended you set ***IM# Fallback Mode*** to `Latched`.

The table below presents recommended ***IM# FrameSyncTim*** settings for the different signalling modes and baud rates:

	Minimum Recommended "IM# FrameSyncTim" Setting			
Baud Rate	**Direct Intertrip Mode**	**Blocking Mode**	**Minimum Setting (ms)**	**Maximum Setting (ms)**
600	100	250	100	1500
1200	50	130	50	1500
2400	30	70	30	1500
4800	20	40	20	1500
9600	10	20	10	1500
19200	10	10	10	1500

Note:
As we have recommended Latched operation, the table does not contain recommendations for 'Permissive' mode. However, if you do select 'Default' mode, you should set ***IM# FrameSyncTim*** *greater than those listed above. If you set* ***IM# FrameSyncTim*** *lower than the minimum setting listed above, the device could interpret a valid change in a message as a corrupted message.*

We recommend a setting of 25% for the communications failure alarm.

CHAPTER 17

COMMUNICATIONS

17.1 CHAPTER OVERVIEW

This product supports Substation Automation System (SAS), and Supervisory Control and Data Acquisition (SCADA) communication through multiple interfaces and a choice of data protocols.

All products support rugged serial communications for SCADA and SAS applications. Optionally, any product can support Ethernet communications for IEC 61850, cyber security and remote access, either through a single port or industry-standard redundant ports.

This chapter contains the following sections:

17.2 COMMUNICATION INTERFACES

The products have a number of standard and optional communication interfaces. The standard and optional hardware and protocols are summarised below:

Port	Availability	Physical Interface	Use	Data Protocols
Front	Standard	USB Type B	Local settings	Courier
Rear Port 1 (RP1 copper)	Standard	RS232/RS485/K-Bus	SCADA Remote settings	Courier, IEC 60870-5-103, DNP3.0
Rear Port 1 (RP1 fibre)	Optional	Fibre	SCADA Remote settings	Courier, IEC 60870-5-103, DNP3.0
Rear Port 2 (RP2)	Optional	RS232/RS485/K-Bus	SCADA Remote settings	SK4: Courier only SK5: InterMiCOM only
Ethernet	Optional	Ethernet	IEC 61850 Remote settings	IEC 61850, Courier Tunnel

Note:
Optional communications boards are always fitted into slot A. It is only possible to fit one optional communications board, therefore RP2 and Ethernet communications are mutually exclusive, except for ZN0098005, where both Ethernet and serial protocols are supported.
On RP1, any one of the data protocols can be selected at one time, from the COMMUNICATIONS Menu (it is no longer necessary to select one as a product order option).

17.3 SERIAL COMMUNICATION

The physical layer standards that are used for serial communications for SCADA purposes are:

- EIA(RS)485 (often abbreviated to RS485)
- K-Bus (a proprietary customization of RS485)

USB is used for local communication with the IED (for transferring settings and downloading firmware updates).

RS485 is similar to RS232 but for longer distances and it allows daisy-chaining and multi-dropping of IEDs.

K-Bus is a proprietary protocol quite similar to RS485, but it cannot be mixed on the same link as RS485. Unlike RS485, K-Bus signals applied across two terminals are not polarised.

It is important to note that these are not data protocols. They only describe the physical characteristics required for two devices to communicate with each other.

For a description of the K-Bus standard see K-Bus and GE Vernova's K-Bus interface guide reference R6509.

A full description of the RS485 is available in the published standard.

17.3.1 USB FRONT PORT

The USB interface uses the proprietary Courier protocol for local communication with the MiCOM S1 Agile settings application software.

This is intended for temporary local connection and is not suitable for permanent connection. This interface uses a fixed baud rate of 19200 bps, 11-bit frame (8 data bits, 1 start bit, 1 stop bit, even parity bit), and a fixed device address of '1'.

The USB interface is a Type B connector. Normally a Type A to Type B USB cable will be required to communicate between MiCOM S1 Agile and the IED.

17.3.2 EIA(RS)485 BUS

The RS485 two-wire connection provides a half-duplex, fully isolated serial connection to the IED. The connection is polarized but there is no agreed definition of which terminal is which. If the master is unable to communicate with the product, and the communication parameters match, then it is possible that the two-wire connection is reversed.

The RS485 bus must be terminated at each end with 120 Ω 0.5 W terminating resistors between the signal wires.

The RS485 standard requires that each device be directly connected to the actual bus. Stubs and tees are forbidden. Loop bus and Star topologies are not part of the RS485 standard and are also forbidden.

Two-core screened twisted pair cable should be used. The final cable specification is dependent on the application, although a multi-strand 0.5 mm^2 per core is normally adequate. The total cable length must not exceed 1000 m. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The RS485 signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product’s chassis. This is for both safety and noise reasons.

It may be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to turn from receive mode to transmit mode. This may be because the master is waiting in receive mode, in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequently not responding. Symptoms of this are; poor response times (due to retries), increasing message error counts, erratic communications, and in the worst case, complete failure to communicate.

17.3.2.1 EIA(RS)485 BIASING REQUIREMENTS

Biasing requires that the signal lines be weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean to prevent noise being injected.

Note:
Some devices may be able to provide the bus bias, in which case external components would not be required.

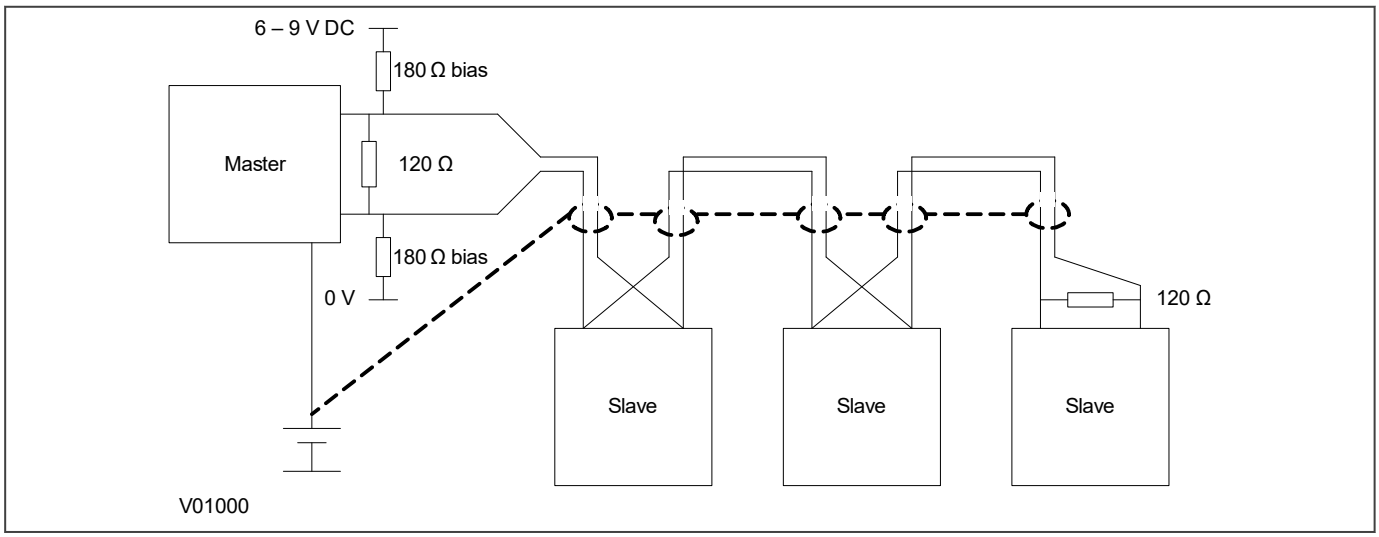


Figure 228: RS485 biasing circuit

Warning:
It is extremely important that the 120 Ω termination resistors are fitted. Otherwise the bias voltage may be excessive and may damage the devices connected to the bus.

17.3.3 K-BUS

K-Bus is a robust signalling method based on RS485 voltage levels. K-Bus incorporates message framing, based on a 64 kbps synchronous HDLC protocol with FM0 modulation to increase speed and security.

The rear interface is used to provide a permanent connection for K-Bus, which allows multi-drop connection.

A K-Bus spur consists of up to 32 IEDs connected together in a multi-drop arrangement using twisted pair wiring. The K-Bus twisted pair connection is non-polarised.

It is not possible to use a standard EIA(RS)232 to EIA(RS)485 converter to convert IEC 60870-5 FT1.2 frames to K-Bus. A protocol converter, namely the KITZ101 or KITZ102, must be used for this purpose. Please consult GE Vernova for information regarding the specification and supply of KITZ devices. The following figure demonstrates a typical K-Bus connection.

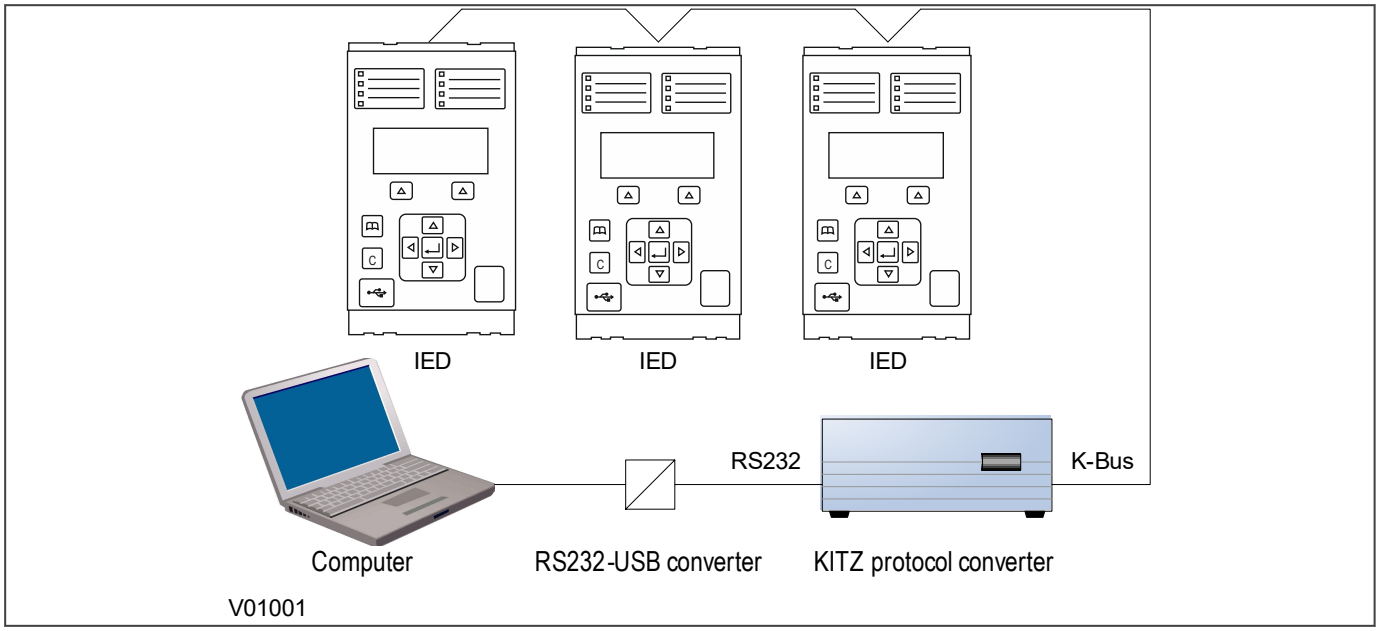


Figure 229: Remote communication using K-Bus

Note:
An RS232-USB converter is only needed if the local computer does not provide an RS232 port.

Further information about K-Bus is available in the publication R6509: K-Bus Interface Guide, which is available on request.

17.4 ETHERNET BOARD VERSIONS

Each board combines Ethernet communications, with universal IRIG-B timing functionality. There is a choice of embedded protocols for the Ethernet communications, and one option that also includes support for serial protocols.

Board variants

Board	Part No.	Compatible With
One LC duplex Ethernet port with universal IRIG-B and IEEE1588 and one RJ45 Maintenance/Engineering Port	ZN0098 001	Ethernet network, no native redundancy.
Two RJ45 duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two copper pairs), with on-board universal IRIG-B and IEEE 1588 and one RJ45 Maintenance/engineering port	ZN0098 002	Any PRP, HSR, RSTP or standard Ethernet network
Two LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with on-board universal IRIG-B and IEEE 1588 and one RJ45 Maintenance/engineering port	ZN0098 003	Any PRP, HSR, RSTP or standard Ethernet network
Two LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with serial fibre ST ports with on-board universal IRIG-B and IEEE 1588 and one RJ45 Maintenance/ engineering port	ZN0098 005	Any PRP, HSR, RSTP or standard Ethernet network. On the serial interface Courier, IEC 60870-5-103, DNP3

When using any of the redundant Ethernet boards on an IED, the final product will have two MAC addresses and will require two IP addresses, one for the maintenance port (NP1) for management purposes, and one for the IED station bus communications (NP2). Both of these are set using the IED Configurator tool of MiCOM S1 Agile release 3.1 or later.

All Ethernet connections are made with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (LC connector). The boards support IEC 61850 over Ethernet.

17.5 BOARD CONNECTIONS

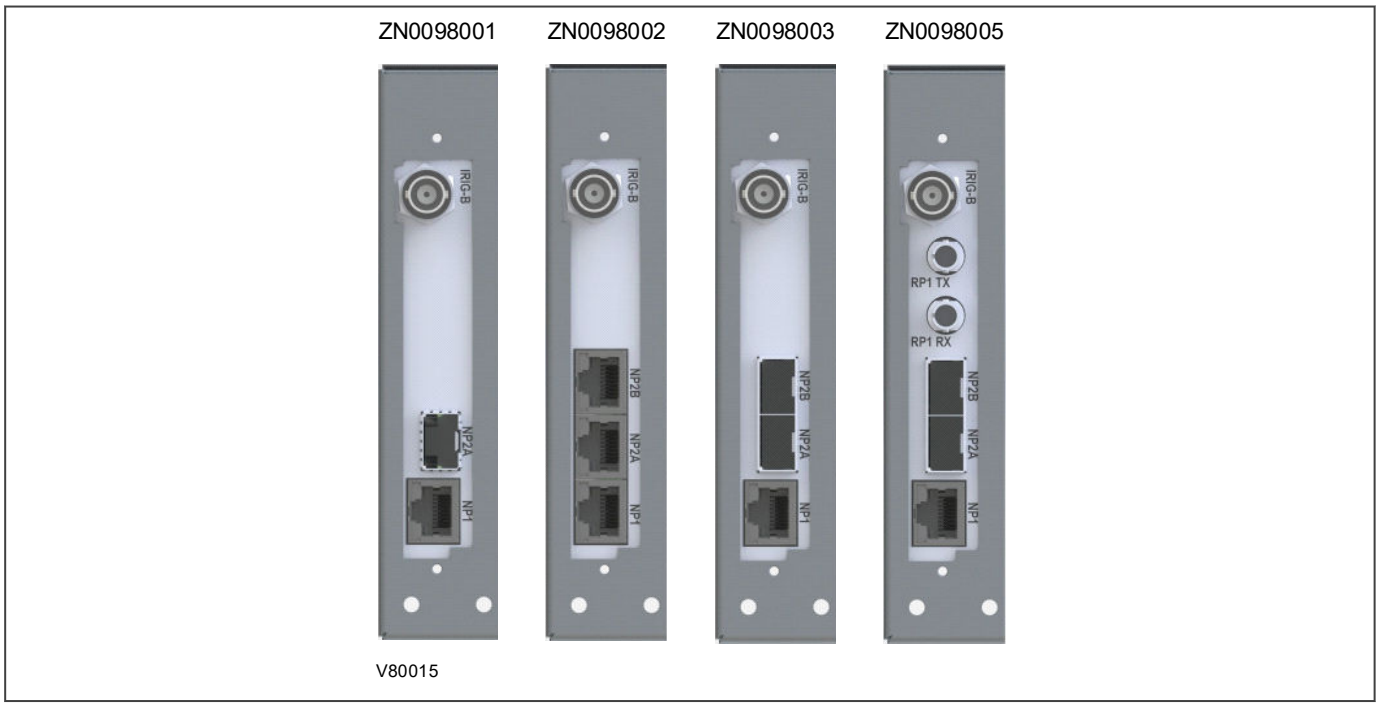


Figure 230: Board connectors

IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

RJ45 Connector (NP1, NP2A and NP2B optional)

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

LC Optical Fibre Connectors (NP2A and NP2B optional)

Connector	SFP
A	TX
B	RX

Optical Fibre Connectors (ST only on part ZN0098005)

Connector	Serial Courier, IEC 60870-5-103, DNP3
RP1	TX
RP1	RX

17.6 ETHERNET CONFIGURATION

All configuration for both the monitoring/engineering port and the station bus port is done in **IED Configurator**.

The monitoring/engineering port is named "Network Port 1" and the redundant IEC 61850 station bus port is named "Network Port 2".

Network Port 1 (NP1) and Network Port 2 (NP2) have independent IP address and subnet configuration parameters, as detailed in the sub-section below. These parameters can be configured in IED Configurator, or optionally from the Front Panel UI.

The IP addresses can be in the range 0.0.0.0 to 223.255.255.255. This means it can be configured as either a Class A, B or C address.

Class	Address Range
A	0.0.0.0 to 127.255.255.255
B	128.0.0.0 to 191.255.255.255
C	192.0.0.0 to 223.255.255.255

The NP1 and NP2 IP addresses must not be configured in the same subnet.

The primary and secondary server IP addresses for RADIUS, syslog and SNMP must also be in these ranges.

17.6.1 NETWORK CONFIGURATION

To set the IP address of the monitoring/engineering port:

1. From the main window click the **Communications** section.
2. Navigate to the Network Port 1.
3. Enter the required IP address, network mask and gateway.
4. The media is not configurable for the engineering port, as they are always RJ45 copper ports.

To set the IP address of the station bus port:

1. From the main window click the **Communications** section.
2. Navigate to the Network Port 2.
3. Enter the required IP address, network mask and gateway.
4. In the Network Port 2 General configuration section, the redundancy options become available.
5. If the board supports redundancy, choose the redundant protocol desired (Failover, RSTP, PRP and HSR).
6. Each protocol has its own protocol specific settings, covered in each protocol's section.
7. The media is not configurable for the station bus port, as they are always enabled according to the ordering code. The media section is available for legacy boards only.

17.6.2 PRP CONFIGURATION

To view or configure the PRP Parameters:

1. Set the redundancy mode to **PRP**.
   - **Multicast Address:** Use this field to configure the multicast destination address. All DANPs in the network must be configured to operate with the same multicast address for the purpose of network supervision.
   - **Life Check Interval:** This defines how often a node sends a PRP_Supervision frame. All DANPs shall be configured with the same Life Check Interval.

17.6.3 HSR CONFIGURATION

To view or configure the HSR Parameters:

Set the redundancy mode to HSR.

- **Multicast Address:** Use this field to configure the multicast destination address. All DANPs in the network must be configured to operate with the same multicast address for the purpose of network supervision.
- **Life Check Interval**: This defines how often a node sends an HSR Supervision frame. All DANPs shall be configured with the same Life Check Interval.

17.6.4 RSTP CONFIGURATION

To view or configure the RSTP Parameters:

Set the redundancy mode to **RSTP**.

Parameter	Default value (second)	Minimum value (second)	Maximum value (second)
Bridge Max Age	20	6	40
Bridge Hello Time	2	1	10
Bridge Forward Delay	15	4	30
Bridge Priority	32768	0	61440

17.6.5 FAILOVER CONFIGURATION

To view or configure the Failover Parameters:

1. Set the redundancy mode to **Failover**.
   - Port A and Port B radio button allows to select your main port for the Failover. The name of the port in the board is also shown.
   - The Failover time defines how long it takes for the redundancy switch over to trigger. The minimum value is 2s.

17.6.6 SNTP IP ADDRESS CONFIGURATION

To configure the SNTP server IP address:

1. From the main window click the **SNTP** button.
2. The General configuration allows to set the frequency of the polling of the SNTP server. It also has a check-box **IED is a clock source** to configure the IED to be a SNTP server itself, to retransmit its date and time.
3. Under External Server 1 and 2, set the IP address of the SNTP server.

17.7 REDUNDANCY PROTOCOLS

REB variants for each of the following protocols are available:

- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- RSTP (Rapid Spanning Tree Protocol)
- Failover

PRP and HSR are open standard, so their implementation is compatible with any standard PRP or HSR device respectively. PRP and HSR provides "bumpless" redundancy. RSTP is also an open standard, so its implementation is compatible with any standard RSTP devices. RSTP provides redundancy, however, it is not "bumpless", the standard instead utilises a loop free topology that is recalculated when a device fails, and does not forward messages during recalculation.

17.7.1 PARALLEL REDUNDANCY PROTOCOL (PRP)

Power system companies have traditionally used proprietary protocols for redundant communications. This is because standardized protocols could not meet the requirements for real-time systems. Even a short loss of connectivity may result in loss of functionality.

However, Parallel Redundancy Protocol (PRP) uses the IEC 62439 standard in Dual Star Topology networks, designed for IEDs from different manufacturers to operate with each other in a substation redundant-Ethernet network. PRP provides bumpless redundancy for real-time systems and is the standard for double Star-topology networks in substations.

17.7.1.1 PRP NETWORKS

Redundant networks usually rely on the network’s ability to reconfigure if there is a failure. However, PRP uses two independent networks in parallel.

PRP implements the redundancy functions in the end nodes rather than in network elements. This is one major difference to RSTP. An end node is attached to two similar LANs of any topology which operate in parallel.

The sending node replicates each frame and transmits them over both networks. The receiving node processes the frame that arrives first and discards the duplicate. Therefore there is no distinction between the working and backup path. The receiving node checks that all frames arrive in sequence and that frames are correctly received on both ports.

The PRP layer manages this replicate and discard function, and hides the two networks from the upper layers. This scheme works without reconfiguration and switchover, so it stays available ensuring no data loss.

There should be no common point of failure between the two LANs. Therefore they are not powered by the same source and cannot be connected directly together. They are identical in protocol at the MAC level but may differ in performance and topology. Both LANs must be on the same subnet so all IP addresses must be unique.

17.7.1.2 NETWORK ELEMENTS

A PRP compatible device has two ports that operate in parallel. Each port is connected to a separate LAN. In the IEC 62439 standard, these devices are called DANP (Doubly Attached Node running PRP). A DAN has two ports, one MAC address and one IP address.

A Single Attached Node (SAN) is a non-critical node attached to only one LAN. SANs that need to communicate with each other must be on the same LAN.

The following diagram shows an example of a PRP network. The Doubly Attached Nodes DANP 1 and DANP 2 have full node redundancy. The Singly Attached Nodes SAN 1 and SAN 4 do not have any redundancy. Singly attached nodes can be connected to both LANs using a Redundancy Box (RedBox). The RedBox converts a singly attached node into a doubly attached node. Devices such as PCs with one network board, printers, and IEDs with

one network board are singly attached nodes. A SAN behind a RedBox appears like a DAN so is called a Virtual DAN (VDAN).

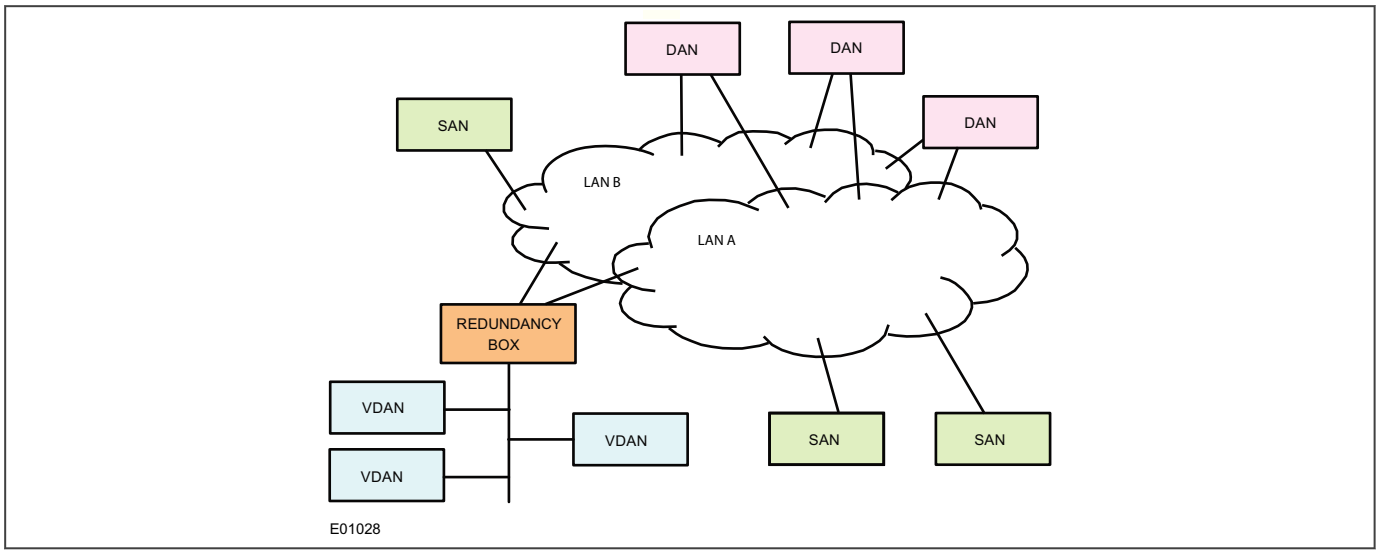


Figure 231: Example PRP redundant network

In a DAN, both ports share the same MAC address so it does not affect the way devices talk to each other in an Ethernet network (Address Resolution Protocol at layer 2). Every data frame is seen by both ports.

When a DAN sends a frame of data, the frame is duplicated on both ports and therefore on both LAN segments. This provides a redundant path for the data frame if one of the segments fails. Under normal conditions, both LAN segments are working and each port receives identical frames. There are two ways of handling this: Duplicate Accept and Duplicate Discard.

The GE Vernova RedBox is the H49 switch. This is compatible with any other vendor's PRP device.

17.7.2 HIGH-AVAILABILITY SEAMLESS REDUNDANCY (HSR)

HSR is standardized in IEC 62439-3 (clause 5) for use in ring topology networks. Similar to PRP, HSR provides bumpless redundancy and meets the most demanding needs of substation automation. HSR has become the reference standard for ring-topology networks in the substation environment. The HSR implementation of the redundancy Ethernet board (REB) is compatible with any standard HSR device.

HSR works on the premise that each device connected in the ring is a doubly attached node running HSR (referred to as DANH). Similar to PRP, singly attached nodes such as printers are connected via Ethernet Redundancy Boxes (RedBox).

17.7.2.1 HSR MULTICAST TOPOLOGY

When a DANH is sending a multicast frame, the frame (C frame) is duplicated (A frame and B frame), and each duplicate frame A/B is tagged with the destination MAC address and the sequence number. The frames A and B differ only in their sequence number, which is used to identify one frame from the other. Each frame is sent to the network via a separate port. The destination DANH receives two identical frames, removes the HSR tag of the first frame received and passes this (frame D) on for processing. The other duplicate frame is discarded. The nodes forward frames from one port to the other unless it was the node that injected it into the ring.

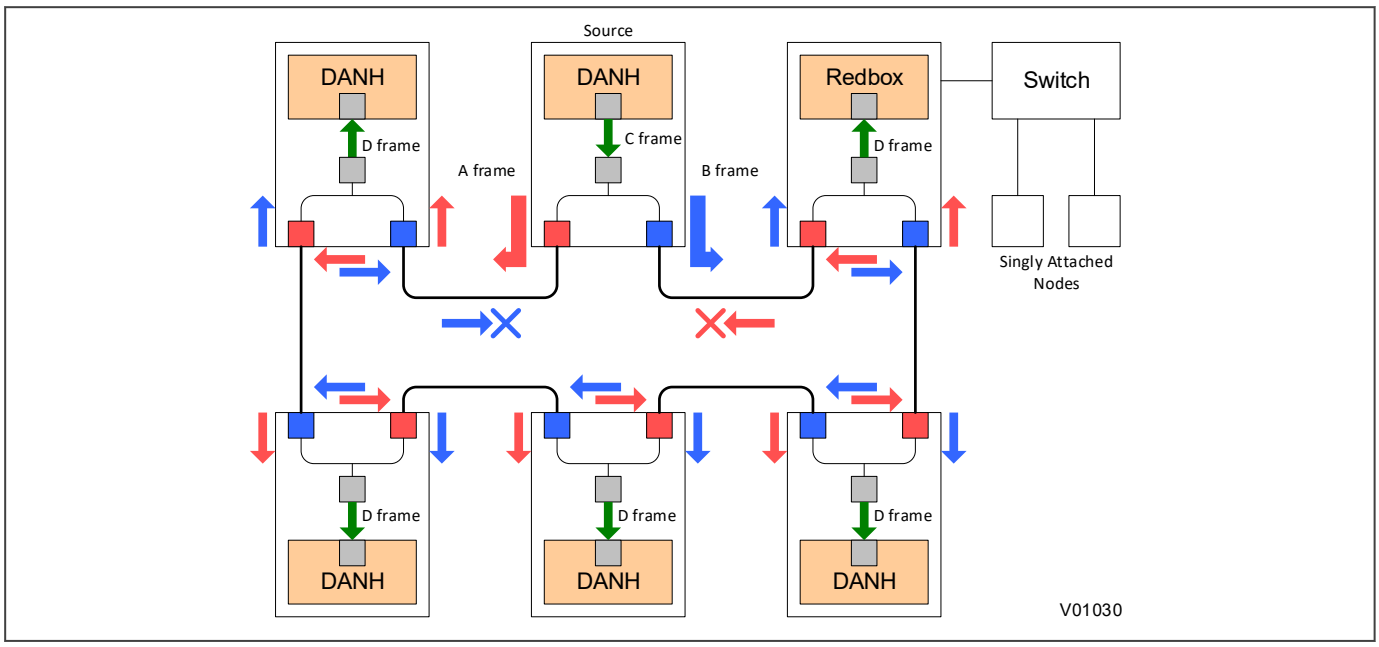


Figure 232: HSR multicast topology

Only about half of the network bandwidth is available in HSR for multicast or broadcast frames because both duplicate frames A & B circulate the full ring.

17.7.2.2 HSR UNICAST TOPOLOGY

With unicast frames, there is just one destination and the frames are sent to that destination alone. All non-recipient devices simply pass the frames on. They do not process them in any way. In other words, D frames are produced only for the receiving DANH. This is illustrated below.

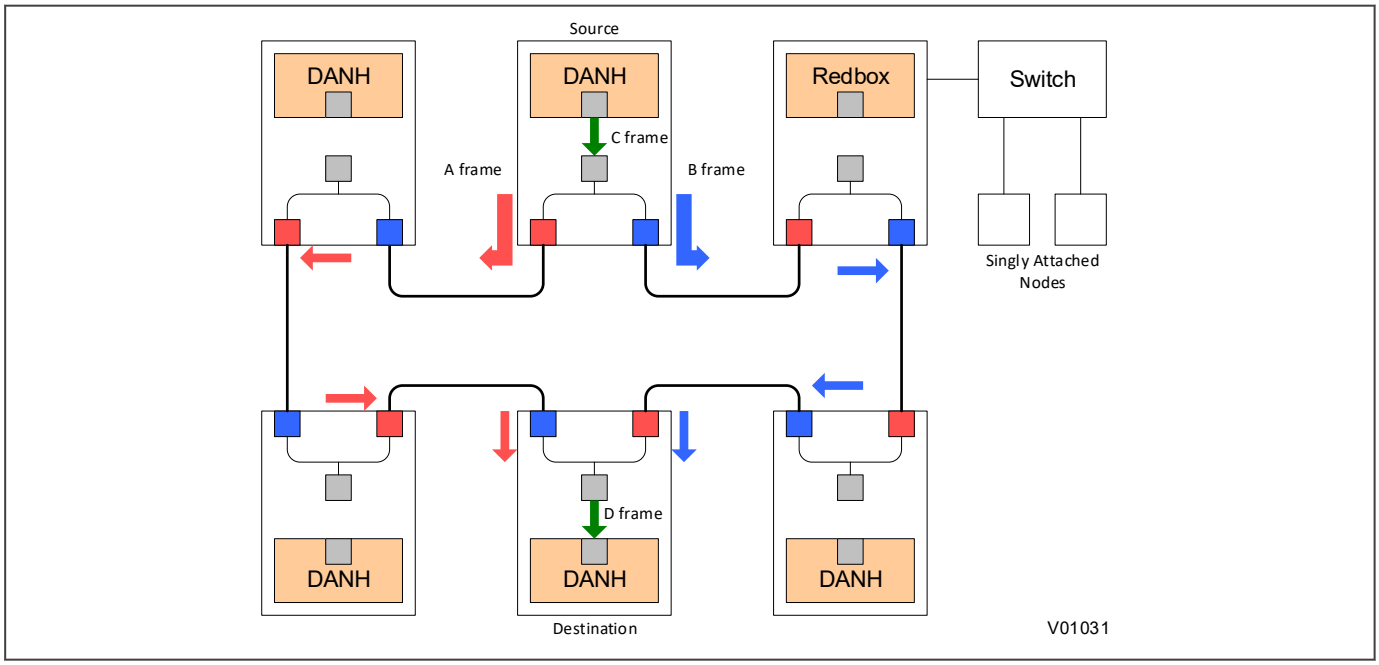


Figure 233: HSR unicast topology

For unicast frames, the whole bandwidth is available as both frames A & B stop at the destination node.

17.7.2.3 HSR APPLICATION IN THE SUBSTATION

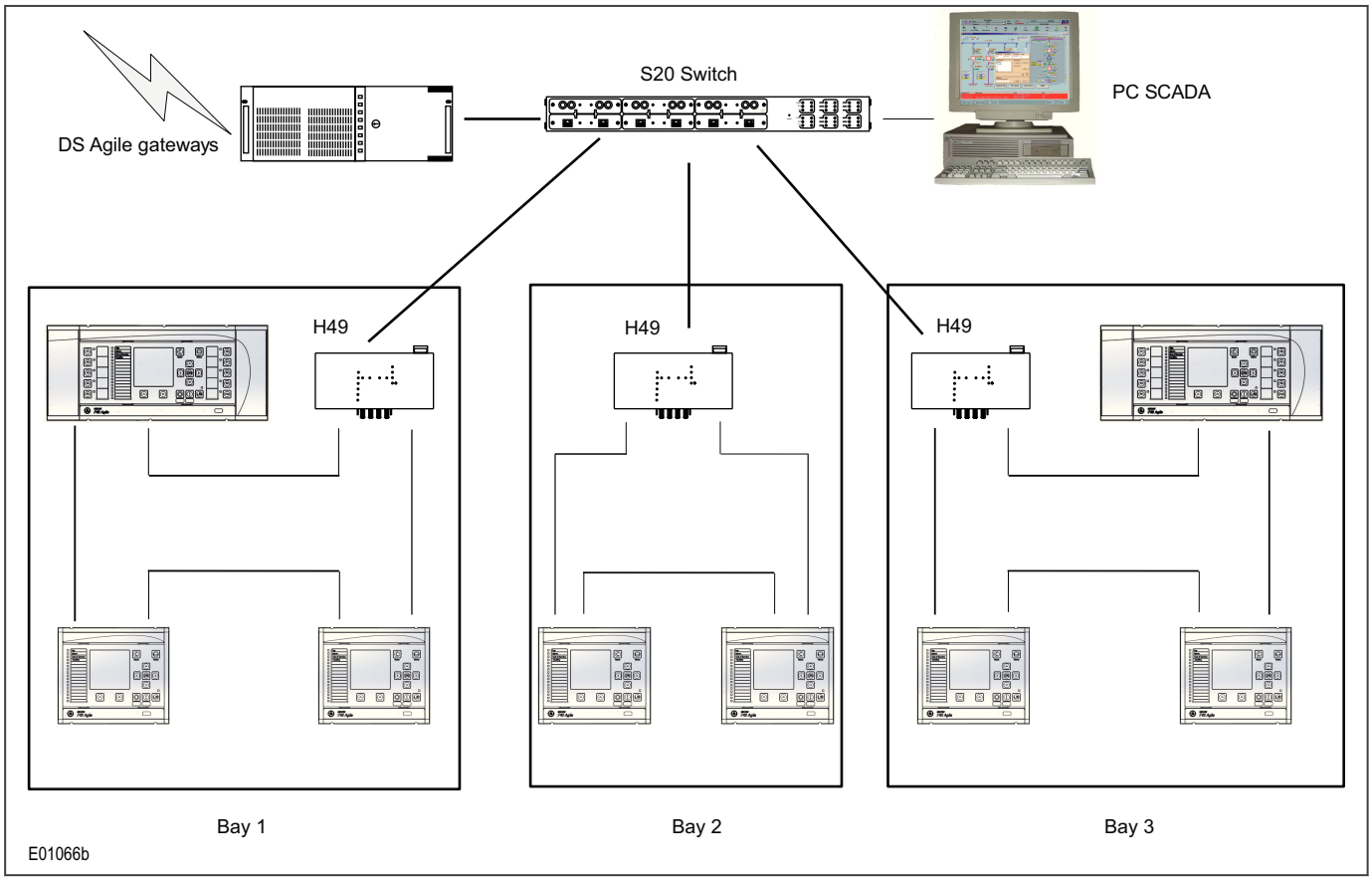


Figure 234: HSR application in the substation

17.7.3 RAPID SPANNING TREE PROTOCOL (RSTP)

RSTP is a standard used to quickly reconnect a network fault by finding an alternative path, allowing loop-free network topology. Although RSTP can recover network faults quickly, the fault recovery time depends on the number of devices and the topology. The recovery time also depends on the time taken by the devices to determine the root bridge and compute the port roles (discarding, learning, forwarding). The devices do this by exchanging Bridge Protocol Data Units (BPDUs) containing information about bridge IDs and root path costs. See the IEEE 802.1D 2004 standard for further information.

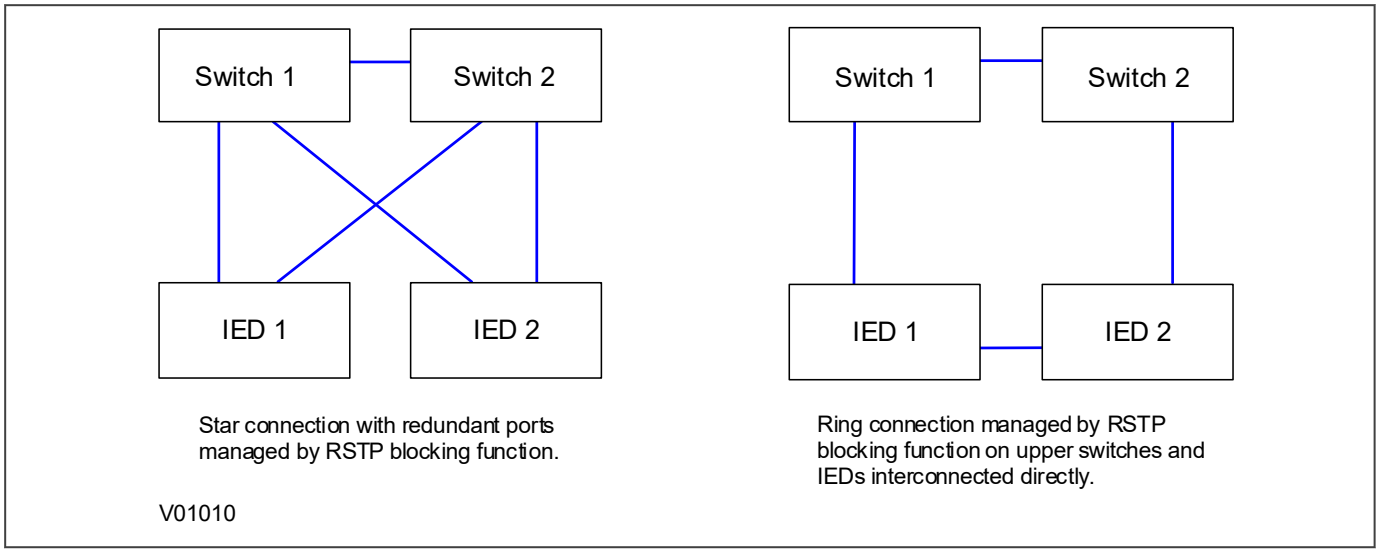


Figure 235: IED attached to redundant Ethernet star or ring circuit

The RSTP solution is based on open standards. It is therefore compatible with other Manufacturers' IEDs that use the RSTP protocol. The RSTP recovery time is typically 300 ms but it increases with network size, therefore cannot achieve the desired bumpless redundancy.

To ensure optimal performance of the protocol, make sure that one of the Ethernet switches is always the root of the RSTP topology.

17.7.4 FAILOVER

Failover is a simple redundancy mechanism that is not tied to any protocol. It works by selecting a main port and a switching time that can be as low as 2 seconds. When the main port link fails, the redundant port becomes physically active. At no point are both ports physically active, which means it can be used on any redundant or non-redundant network.

17.8 SIMPLE NETWORK MANAGEMENT PROTOCOL (SNMP)

Simple Network Management Protocol (SNMP) is a network protocol designed to manage devices in an IP network. SNMP uses a Management Information Base (MIB) that contains information about parameters to supervise. The MIB format is a tree structure, with each node in the tree identified by a numerical Object Identifier (OID). Each OID identifies a variable that can be read or set using SNMP with the appropriate software. The information in the MIB is standardised.

Each system in a network (workstation, server, router, bridge, etc.) maintains a MIB that reflects the status of the managed resources on that system, such as the version of the software running on the device, the IP address assigned to a port or interface, the amount of free hard drive space, or the number of open files. The MIB does not contain static data, but is instead an object-oriented, dynamic database that provides a logical collection of managed object definitions. The MIB defines the data type of each managed object and describes the object.

The SNMP-related branches of the MIB tree are located in the internet branch, which contains two main types of branches:

- Public branches (mgmt=2), which are defined by the Internet Engineering Task Force (IETF).
- Private branches (private=4), which are assigned by the Internet Assigned Numbers Authority (IANA). These are defined by the companies and organizations to which these branches are assigned.

The following figure shows the structure of the SNMP MIB tree. There are no limits on the width and depth of the MIB tree.

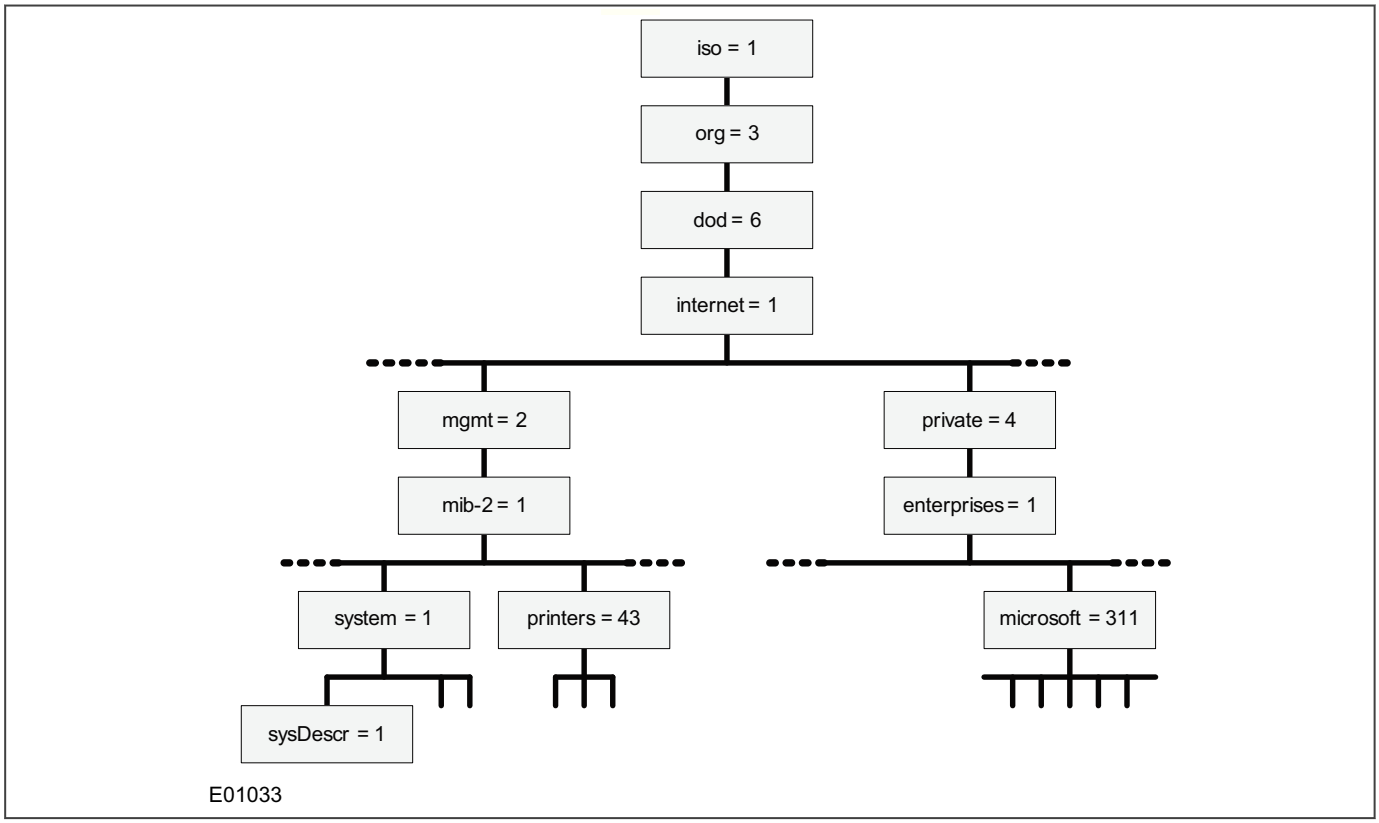


Figure 236: SNMP MIB tree

The top four levels of the hierarchy are fixed. These are:

- International Standards Organization (iso)
- Organization (org)
- Department of Defence (dod)
- Internet

Management (mgmt) is the main public branch. It defines network management parameters common to devices from all vendors. Underneath the Management branch is MIB-II (mib-2), and beneath this are branches for common management functions such as system management, printers, host resources, and interfaces.

The private branch of the MIB tree contains branches for large organizations, organized under the enterprises branch. This is not applicable to GE Vernova.

17.8.1 SNMP MIBS COMPATIBLE WITH THE IED

Our IED supports four different MIBs, all available for download on the GE website:

- IEC-62439-3-MIB: Standard PRP/HSR MIB.
- RMON-MIB: Standard Remote Monitoring MIB.
- GE-PX4X-MIB.mib: Private MIB that contains all the information specific to the relay. For example, model and serial number.
- GE-GRID-MIB.mib: Private MIB that only contains manufacturer information.

The information within the MIBs can be read using a simple text app like Notepad, or the MIB can be explored using an MIB Browser.

The private branch of the MIB tree contains branches for large organizations, organized under the enterprises branch. This is not applicable to GE Vernova.

17.8.2 NEW SNMP SYSTEM OBJECTS

The following elements have been added to the SNMP structure to more accurately describe the new functionalities added in the Ethernet boards:

17.8.2.1 NEW SNMP TRAPS

Changes in the Physical link statuses (Up or Down status) of NP1, NP2A, NP2B ethernet ports will be reported as SNMP traps.

The objects for these link statuses are added in MIB (GE-PX4X-MIB.mib). Below are the IDs for Network Port link objects:

- **np1Link**: 1.3.6.1.4.1.55461.1.6.1
- **np2ALink**: 1.3.6.1.4.1.55461.1.6.2
- **np2Blink**: 1.3.6.1.4.1.55461.1.6.3

17.8.2.2 NEW SNMP OBJECTS

The following objects have been added to MIB (GE-PX4X-MIB.mib) to add more visibility to the behaviour of the Ethernet board.

- **np2Redundancy:** .1.3.6.1.4.1.55461.1.6.4, represents active redundancy protocol set in the device.
- **rstpRootIdentifier**: .1.3.6.1.4.1.55461.1.6.5, represents RSTP Rot Bridge Identifier. It is a combination of Root bridge's priority and its MAC address.
- **rstpTimeSinceTopoChange**: .1.3.6.1.4.1.55461.1.6.6, represents the time elapsed since last RSTP topology change.
- **rstpTopoChangeCount**: .1.3.6.1.4.1.55461.1.6.7, represents RSTP topology change count.

17.8.3 SNMP ALARM ENHANCEMENT

An SNMP alarm is triggered by the relay when a security event occurs, if SNMP trap destination IP is configured in the settings.

17.8.3.1 SNMP ALARM FORMAT

The format of the SNMP trap/alarm for security events consists of three parts as described below.

"Event Description, Username, Interface".

Event Description: Short description of the alarm, same as the description present in Security event.

Username: User associated with the event, provided only when Username is available for the Security event.

Interface: Interface on which Security event has occurred, same as the interface information present in Security event.

17.8.3.2 LIST OF SNMP ALARMS

No.	Security Events	SNMP Trap Text
1	SECUR_EVT_PW_SET_NON_COMPLIANT	User Password change failed - policy check failed
2	SECUR_EVT_PW_MODIFIED	User password changed successfully
3	SECUR_EVT_PW_ENTRY_NOW_BLOCKED	User locked - wrong credentials
4	SECUR_EVT_PW_ENTRY_UNBLOCKED	User unlocked
5	SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	Log-in attempt when user is locked
6	SECUR_EVT_INVALID_PW_ENTERED	Log-in failed - wrong credentials
7	SECUR_EVT_PW_TIMED_OUT	Log-in failed - credentials expired
8	SECUR_EVT_RECOVERY_PW_ENTERED	Recovery password entered
9	SECUR_EVT_IED_SEC_CODE_READ	Security Code read
10	SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	Security Code Timer expired
11	SECUR_EVT_PORT_DISABLED	Port Disabled
12	SECUR_EVT_PORT_ENABLED	Port Enabled
13	SECUR_EVT_PSL_SETTINGS_DOWNLOADED	PSL Settings downloaded to device
14	SECUR_EVT_DNP_SETTINGS_DOWNLOADED	DNP Settings downloaded to device
15	SECUR_EVT_61850_CONFIG_DOWNLOADED	IEC61850 Config downloaded to device
16	SECUR_EVT_USER_CURVES_DOWNLOADED	User Curves downloaded to device
17	SECUR_EVT_SETTING_GRP_DOWNLOADED	Setting Group downloaded to device
18	SECUR_EVT_DR_SETTINGS_DOWNLOADED	DR Settings downloaded to device
19	SECUR_EVT_PSL_SETTINGS_UPLOADED	PSL Settings uploaded from device
20	SECUR_EVT_DNP_SETTINGS_UPLOADED	DNP Settings uploaded from device
21	SECUR_EVT_61850_CONFIG_UPLOADED	IEC61850 Config uploaded from device
22	SECUR_EVT_USER_CURVES_UPLOADED	User Curves uploaded from device
23	SECUR_EVT_PSL_CONFIG_UPLOADED	PSL Config uploaded from device
24	SECUR_EVT_SETTINGS_UPLOADED	Settings uploaded from device
25	SECUR_EVT_CS_SETTINGS_CHANGED	Control & Support settings changed

No.	Security Events	SNMP Trap Text
26	SECUR_EVT_DR_SETTINGS_CHANGED	Disturbance Record Settings changed
27	SECUR_EVT_SETTING_GROUP_CHANGED	Setting Group changed
28	SECUR_EVT_DEFAULT_SETTINGS_RESTORED	Default Settings restored
29	SECUR_EVT_DEFAULT_USRCURVE_RESTORED	Default User Curve restored
30	SECUR_EVT_POWER_ON	Device Powered On
31	SECUR_EVT_RADIUS_UNAVAIL	RADIUS server not available
32	SECUR_EVT_SESSION_LIMIT	Active user sessions limit reached
33	SECUR_EVT_SLD_FILE_DOWNLOADED	SLD File downloaded to device
34	SECUR_EVT_SLD_FILE_UPLOADED	SLD File uploaded from device
35	SECUR_EVT_RBAC_LOGIN	Log-in successful
36	SECUR_EVT_RBAC_LOGOUT	Log-out (user logged out)
37	Bypass mode Activated	Bypass Mode Activated
38	Bypass mode Deactivated	Bypass Mode Deactivated
39	RADIUS Secret Key changed	RADIUS Secret Key changed
40	SECUR_EVT_SEC_SETTINGS_RESTORED	Security settings restored
41	Switch to Golden Image	Device switching to Firmware update mode
42	Fallback to Device Authentication	Fallback to Device Authentication
43	User logged out due to inactivity timeout.	Log-out by user inactivity (timeout)
44	Security events upload	Security Events uploaded from device
45	SSH Passcode change	SSH pass code change
46	SSH Client Authentication Fail	Failed client authentication
47	SSH Client Authentication Success	Successful client authentication
48	New User added	User account created successfully
49	User deleted	User account deleted successfully
50	User role change	Permission changed successfully
51	User name change	User renamed successfully

17.9 DATA PROTOCOLS

The products support a wide range of protocols to make them applicable to many industries and applications. The exact data protocols supported by a particular product depend on its chosen application, but the following table gives a list of the data protocols that are typically available.

DATA PROTOCOLS

Data Protocol	Layer 1 Interface	Description
Courier	USB, K-Bus, RS232, RS485, Ethernet	Standard for SCADA communications developed by GE Vernova.
IEC 60870-5-103	RS485	IEC standard for SCADA communications
DNP 3.0	RS485	Standard for SCADA communications
IEC 61850	Ethernet	IEC standard for substation automation. Facilitates interoperability.

The relationship of these protocols to the lower-level physical layer protocols are as follows:

Data Protocols	IEC 60870-5-103 DNP3.0 Courier	IEC 61850 Courier	Courier	Courier	Courier
Data Link Layer	EIA(RS)485	Ethernet	EIA(RS)232	K-Bus	USB
Physical Layer	Copper or Optical Fibre				USB Type B

The product supports switchable serial communication data protocol on the Rear Port 1 (RP1) interface (it is no longer necessary to select the protocol as a product order option). This setting cell is ***RP1 Protocol*** in the *COMMUNICATIONS* column. For example, the product can now be configured to provide IEC 61850 on the Ethernet interface and DNP3.0 on the serial port concurrently.

17.9.1 COURIER

This section should provide sufficient detail to enable understanding of the Courier protocol at a level required by most users. For situations where the level of information contained in this manual is insufficient, further publications (R6511 and R6512) containing in-depth details about the protocol and its use, are available on request.

Courier is a GE Vernova proprietary communication protocol. Courier uses a standard set of commands to access a database of settings and data in the IED. This allows a master to communicate with a number of slave devices. The application-specific elements are contained in the database rather than in the commands used to interrogate it, meaning that the master station does not need to be preconfigured. Courier also provides a sequence of event (SOE) and disturbance record extraction mechanism.

17.9.1.1 PHYSICAL CONNECTION AND LINK LAYER

Courier can be used with four physical layer protocols: USB, K-Bus, EIA(RS)232 or EIA(RS)485.

Several connection options are available for Courier

- The front USB port (for connection to Settings application software on, for example, a laptop)
- Rear Port 1 (RP1) - for permanent SCADA connection via serial RS485 or K-Bus
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via serial optical fibre
- Optional Rear Port 2 (RP2) - for permanent SCADA connection via serial RS485, K-Bus, or RS232

Optional Ethernet board (NIC) - for remote communication with the S1 Agile settings application software across an Ethernet network.

For either of the serial rear ports, both the IED address and baud rate can be selected using the front panel menu or by the settings application software.

Note:
*Changing the **RP2 Port Config** setting (K-Bus, EIA(RS)232) requires the IED to be rebooted, for the change to become effective.*

17.9.1.2 COURIER DATABASE

The Courier database is two-dimensional and resembles a table. Each cell in the database is referenced by a row and column address. Both the column and the row can take a range from 0 to 255 (0000 to FFFF Hexadecimal. Addresses in the database are specified as hexadecimal values, for example, 0A02 is column 0A row 02. Associated settings or data are part of the same column. Row zero of the column has a text string to identify the contents of the column and to act as a column heading.

The product-specific menu databases contain the complete database definition.

17.9.1.3 SETTINGS CATEGORIES

There are two main categories of settings in protection IEDs:

- Control and support settings
- Protection settings

With the exception of the Disturbance Recorder settings, changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to the Protection settings and the Disturbance Recorder settings are stored in ‘scratchpad’ memory and are not immediately implemented. These need to be committed by writing to the ***Save Changes*** cell in the *CONFIGURATION* column.

17.9.1.4 SETTING CHANGES

Courier provides two mechanisms for making setting changes. Either method can be used for editing any of the settings in the database.

Method 1

This uses a combination of three commands to perform a settings change:

First, enter Setting mode: This checks that the cell is settable and returns the limits.

1. Preload Setting: This places a new value into the cell. This value is echoed to ensure that setting corruption has not taken place. The validity of the setting is not checked by this action.
2. Execute Setting: This confirms the setting change. If the change is valid, a positive response is returned. If the setting change fails, an error response is returned.
3. Abort Setting: This command can be used to abandon the setting change.

This is the most secure method. It is ideally suited to on-line editors because the setting limits are extracted before the setting change is made. However, this method can be slow if many settings are being changed because three commands are required for each change.

Method 2

The Set Value command can be used to change a setting directly. The response to this command is either a positive confirm or an error code to indicate the nature of a failure. This command can be used to implement a setting more rapidly than the previous method; however the limits are not extracted. This method is therefore most suitable for off-line setting editors such as MiCOM S1 Agile, or for issuing preconfigured control commands.

17.9.1.5 EVENT EXTRACTION

You can extract events either automatically (rear serial port only) or manually (either serial port). For automatic extraction, all events are extracted in sequential order using the Courier event mechanism. This includes fault and maintenance data if appropriate. The manual approach allows you to select events, faults, or maintenance data as desired.

17.9.1.5.1 AUTOMATIC EVENT RECORD EXTRACTION

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported through the rear Courier port.

When new event information is created, the ***Event*** bit is set in the ***Status*** byte. This indicates to the Master device that event information is available. The oldest, non-extracted event can be extracted from the IED using the ***Send Event*** command. The IED responds with the event data.

Once an event has been extracted, the ***Accept Event*** command can be used to confirm that the event has been successfully extracted. When all events have been extracted, the ***Event*** bit is reset. If there are more events still to be extracted, the next event can be accessed using the ***Send Event*** command as before.

17.9.1.5.2 MANUAL EVENT RECORD EXTRACTION

The *VIEW RECORDS* column (location 01) is used for manual viewing of event, fault, and maintenance records. The contents of this column depend on the nature of the record selected. You can select events by event number and directly select a fault or maintenance record by number.

Event Record Selection ('Select Event' cell: 0101)

This cell can be set the number of stored events. For simple event records (Type 0), cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3), the remainder of the column contains the additional information.

Fault Record Selection ('Select Fault' cell: 0106)

This cell can be used to select a fault record directly, using a value between 0 and 99 to select one of up to a hundred stored fault records. (0 is the most recent fault and 99 is the oldest). The column then contains the details of the fault record selected.

Maintenance Record Selection ('Select Maint' cell: 01F0)

This cell can be used to select a maintenance record using a value between 0 and 9. This cell operates in a similar way to the fault record selection.

If this column is used to extract event information, the number associated with a particular record changes when a new event or fault occurs.

Event Types

The IED generates events under certain circumstances such as:

- Change of state of output contact
- Change of state of opto-input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out

Event Record Format

The IED returns the following fields when the Send Event command is invoked:

- Cell reference
- Time stamp
- Cell text
- Cell value

The Menu Database contains tables of possible events, and shows how the contents of the above fields are interpreted. Fault and Maintenance records return a Courier Type 3 event, which contains the above fields plus two additional fields:

- Event extraction column
- Event number

These events contain additional information, which is extracted from the IED using column B4. Row 01 contains a ***Select Record*** setting that allows the fault or maintenance record to be selected. This setting should be set to the event number value returned in the record. The extended data can be extracted from the IED by uploading the text and data from the column.

17.9.1.6 DISTURBANCE RECORD EXTRACTION

The stored disturbance records are accessible through the Courier interface. The records are extracted using column (B4).

The ***Select Record*** cell can be used to select the record to be extracted. Record 0 is the oldest non-extracted record. Older records which have already been extracted are assigned positive values, while younger records are assigned negative values. To help automatic extraction through the rear port, the IED sets the ***Disturbance*** bit of the ***Status*** byte, whenever there are non-extracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from the ***Trigger Time*** cell (B402). The disturbance record can be extracted using the block transfer mechanism from cell B40B and saved in the COMTRADE format. The settings application software software automatically does this.

17.9.1.7 PROGRAMMABLE SCHEME LOGIC SETTINGS

The programmable scheme logic (PSL) settings can be uploaded from and downloaded to the IED using the block transfer mechanism.

The following cells are used to perform the extraction:

- ***Domain*** cell (B204): Used to select either PSL settings (upload or download) or PSL configuration data (upload only)
- ***Sub-Domain*** cell (B208): Used to select the Protection Setting Group to be uploaded or downloaded.
- ***Version*** cell (B20C): Used on a download to check the compatibility of the file to be downloaded.
- ***Transfer Mode*** cell (B21C): Used to set up the transfer process.
- ***Data Transfer*** cell (B120): Used to perform upload or download.

The PSL settings can be uploaded and downloaded to and from the IED using this mechanism. The settings application software must be used to edit the settings. It also performs checks on the validity of the settings before they are transferred to the IED.

17.9.1.8 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the Courier protocol. The device will correct for the transmission delay. The time synchronization message may be sent as either a global command or to any individual IED address. If the time synchronization message is sent to an individual address, then the device will respond with a confirm message. If sent as a global command, the (same) command must be sent twice. A time

synchronization Courier event will be generated/produced whether the time-synchronization message is sent as a global command or to any individual IED address.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

17.9.1.9 COURIER CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the chosen communication protocol – in this case `Courier`.
4. Move down to the next cell (***RP1 Address***). This cell controls the address of the RP1 port on the device. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. Courier uses an integer number between 1 and 254 for the Relay Address. It is set to 255 by default, which has to be changed. It is important that no two IEDs share the same address.
5. Move down to the next cell (***RP1 InactivTimer***). This cell controls the inactivity timer. The inactivity timer controls how long the IED waits without receiving any messages on the rear port before revoking any password access that was enabled and discarding any changes. For the rear port this can be set between 1 and 30 minutes.
6. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).
7. Move down to the next cell (***RP1 Card Status***). This cell is not settable. It displays the status of the chosen physical layer protocol for RP1.
8. Move down to the next cell (***RP1 Port Config***). This cell controls the type of serial connection. Select between K-Bus or RS485.
9. If using EIA(RS)485, the next cell (***RP1 Comms Mode***) selects the communication mode. The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity. If using K-Bus this cell will not appear.
10. If using EIA(RS)485, the next cell down controls the baud rate. Three baud rates are supported; 9600, 19200 and 38400. If using K-Bus this cell will not appear as the baud rate is fixed at 64 kbps.

17.9.2 IEC 60870-5-103

The specification IEC 60870-5-103 (Telecontrol Equipment and Systems Part 5 Section 103: Transmission Protocols), defines the use of standards IEC 60870-5-1 to IEC 60870-5-5, which were designed for communication with protection equipment.

This section describes how the IEC 60870-5-103 standard is applied to the Px40 platform. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 60870-5-103 standard.

This section should provide sufficient detail to enable understanding of the standard at a level required by most users.

The IEC 60870-5-103 interface is a master/slave interface with the device as the slave device. The device conforms to compatibility level 2, as defined in the IEC 60870-5-103.standard.

The following IEC 60870-5-103 facilities are supported by this interface:

- Initialization (reset)
- Time synchronization
- Event record extraction

- General interrogation
- Cyclic measurements
- General commands
- Disturbance record extraction
- Private codes

17.9.2.1 PHYSICAL CONNECTION AND LINK LAYER

Two connection options are available for IEC 60870-5-103:

- Rear Port 1 (RP1) - for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via optical fibre

If the optional fibre optic port is fitted, a menu item appears in which the active port can be selected. However, the selection is only effective following the next power up.

The IED address and baud rate can be selected using the front panel menu or by the settings application software.

17.9.2.2 INITIALISATION

Whenever the device has been powered up, or if the communication parameters have been changed a reset command is required to initialize the communications. The device will respond to either of the two reset commands; Reset CU or Reset FCB (Communication Unit or Frame Count Bit). The difference between the two commands is that the Reset CU command will clear any unsent messages in the transmit buffer, whereas the Reset FCB command does not delete any messages.

The device will respond to the reset command with an identification message ASDU 5. The Cause of Transmission (COT) of this response will be either Reset CU or Reset FCB depending on the nature of the reset command. The content of ASDU 5 is described in the IEC 60870-5-103 section of the Menu Database, available from GE Vernova separately if required.

In addition to the above identification message, it will also produce a power up event.

17.9.2.3 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the IEC 60870-5-103 protocol. The device will correct for the transmission delay as specified in IEC 60870-5-103. If the time synchronization message is sent as a send/confirm message then the device will respond with a confirm message. A time synchronization Class 1 event will be generated/produced whether the time-synchronization message is sent as a send confirm or a broadcast (send/no reply) message.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the IEC 60870-5-103 interface. An attempt to set the time via the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

17.9.2.4 CONFIGURABLE IEC 60870-5-103 SIGNAL LIST

From Software Version 91 onwards, there is a setting cell which allows the IEC 60870-5-103 private range signals to be selected and de-selected from IEC 60870-5-103 communication.

The IEC 60870-5-103 standard (compatible range) signals, that are provided according to the relay type and implementation, are always enabled. These signals cannot be disabled.

This setting cell is ***Config Mode*** in the *PROTOCOL CFG* column.

There are two settings associated with this cell. These are:

Setting	Description
Fixed	In this mode, the IED behaviour for IEC 60870-5-103 protocol is identical to pre-Software Version 91 IEDs. All the implemented signals (IEC 60870-5-103 compatible range and private range signals) are enabled for IEC 60870-5-103 communication. The COT behaviour will be according to the device IEC 60870-5-103 profile. This mode is provided for backward compatibility. This is the default setting.
Std+UserConfig	In this mode, the user can select which IEC 60870-5-103 private range signals are enabled for IEC 60870-5-103 communication. The selection is done using DDB mask setting cells in the *PROTOCOL CFG* column. The DDB mask value controls only the signal selection (enabled or disabled) for IEC 60870-5-103 communication. It does not modify the COT behaviour of the signals. The COT behaviour of the private range signals will be according to the device IEC 60870-5-103 profile. By default, only IEC 60870-5-103 standard signals are enabled. All private range signals are disabled.

When the ***Config Mode*** cell is set to `Std+UserConfig`, the DDB masks become visible in the *PROTOCOL CFG* column. These masks function in a similar way to the DDB masks in the *RECORD CONTROL* column. Editing these masks controls the DDB signals that are enabled for communication of the equivalent IEC 60870-5-103 private range signal, as listed in the IEC 60870-5-103 profile in the Menu Database.

Within these masks, only individual DDBs that are equivalent to IEC 60870-5-103 private range signals are editable. By default, all of the individual DDBs that are equivalent to IEC 60870-5-103 private range signals are set to 0 (zero), that is disabled for communication. Setting any individual DDB to 1 (one), enables the equivalent IEC 60870-5-103 private range signal for communication.

Within these masks, individual DDBs that are either equivalent to IEC 60870-5-103 standard range signals, or do not have any equivalent IEC 60870-5-103 private range signal, are not editable.

17.9.2.5 SPONTANEOUS EVENTS

Events are categorized using the following information:

- Function type
- Information Number

The IEC 60870-5-103 profile in the Menu Database contains a complete listing of all events produced by the device.

From Software Version 91 onwards, the IEC 60870-5-103 private range signals can be individually selected for spontaneous communication, by settting the ***Config Mode*** cell to `Std+UserConfig`, and configuring the DDB masks as required.

17.9.2.6 GENERAL INTERROGATION (GI)

The GI request can be used to read the status of the device, the function numbers, and information numbers that will be returned during the GI cycle. These are shown in the IEC 60870-5-103 profile in the Menu Database.

From Software Version 91 onwards, the IEC 60870-5-103 private range signals can be individually selected for GI reporting, by setting the ***Config Mode*** cell to `Std+UserConfig`, and configuring the DDB masks as required.

17.9.2.7 CYCLIC MEASUREMENTS

The device will produce measured values using ASDU 9 on a cyclical basis, this can be read from the device using a Class 2 poll (note ADSU 3 is not used). The rate at which the device produces new measured values can be controlled using the measurement period setting. This setting can be edited from the front panel menu or using MiCOM S1 Agile. It is active immediately following a change.

The device transmits its measurands with maximum value of 2.4 times the rated value of the measurement.

17.9.2.8 COMMANDS

A list of the supported commands is contained in the Menu Database. The device will respond to other commands with an ASDU 1, with a cause of transmission (COT) indicating ‘negative acknowledgement’.

17.9.2.9 TEST MODE

It is possible to disable the device output contacts to allow secondary injection testing to be performed using either the front panel menu or the front serial port. The IEC 60870-5-103 standard interprets this as ‘test mode’. An event will be produced to indicate both entry to and exit from test mode. Spontaneous events and cyclic measured data transmitted whilst the device is in test mode will have a COT of ‘test mode’.

17.9.2.10 DISTURBANCE RECORDS

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC 60870-5-103.

> *Note:*
> *IEC 60870-5-103 only supports up to 8 records.*

17.9.2.11 COMMAND/MONITOR BLOCKING

The device supports a facility to block messages in the monitor direction (data from the device) and also in the command direction (data to the device). Messages can be blocked in the monitor and command directions using one of the two following methods

- The menu command ***RP1 CS103Blcking*** in the *COMMUNICATIONS* column
- The DDB signals Monitor Blocked and Command Blocked

17.9.2.12 IEC 60870-5-103 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the chosen communication protocol – in this case `IEC 60870-5-103`.
4. Move down to the next cell (***RP1 Address***). This cell controls the IEC 60870-5-103 address of the IED. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. IEC 60870-5-103 uses an integer number between 0 and 254 for the address. It is important that no two IEDs have the same IEC 60870 5 103 address. The IEC 60870-5-103 address is then used by the master station to communicate with the IED.
5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Two baud rates are supported by the IED, `9600 bits/s` and `19200 bits/s`. Make sure that the baud rate selected on the IED is the same as that set on the master station.
6. Move down to the next cell (***RP1 Meas Period***). The next cell down controls the period between IEC 60870-5-103 measurements. The IEC 60870-5-103 protocol allows the IED to supply measurements at regular intervals. The interval between measurements is controlled by this cell, and can be set between 1 and 60 seconds.
7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).
8. The next cell down (***RP1 CS103Blcking***) can be used for monitor or command blocking.
9. There are three settings associated with this cell; these are:

Setting	Description
Disabled	No blocking selected.
Monitor Blocking	When the monitor blocking DDB Signal is active high, either by energising an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the device returns a "Termination of general interrogation" message to the master station.
Command Blocking	When the command blocking DDB signal is active high, either by energising an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the device returns a "negative acknowledgement of command" message to the master station.

17.9.3 DNP 3.0

This section describes how the DNP 3.0 standard is applied in the product. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the DNP 3.0 standard.

The descriptions given here are intended to accompany the device profile document that is included in the Menu Database document. The DNP 3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP 3.0 implementation. This is the standard format DNP 3.0 document that specifies which objects; variations and qualifiers are supported. The device profile document also specifies what data is available from the device using DNP 3.0. The IED operates as a DNP 3.0 slave and supports subset level 2, as described in the DNP 3.0 standard, plus some of the features from level 3.

The DNP 3.0 protocol is defined and administered by the DNP Users Group. For further information on DNP 3.0 and the protocol specifications, please see the DNP website (www.dnp.org).

17.9.3.1 PHYSICAL CONNECTION AND LINK LAYER

DNP 3.0 can be used with EIA(RS)485.

Several connection options are available for DNP 3.0

- Rear Port 1 (RP1) - for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via optical fibre

The baud rate can be selected using the front panel menu or by the settings application software.

When using a serial interface, the data format is: 1 start bit, 8 data bits, 1 stop bit and optional configurable parity bit.

17.9.3.2 OBJECT 1 BINARY INPUTS

Object 1, binary inputs, contains information describing the state of signals in the IED, which mostly form part of the digital data bus (DDB). In general these include the state of the output contacts and opto-inputs, alarm signals, and protection start and trip signals. The ‘DDB number’ column in the device profile document provides the DDB numbers for the DNP 3.0 point data. These can be used to cross-reference to the DDB definition list. See the relevant Menu Database document. The binary input points can also be read as change events using Object 2 and Object 60 for class 1-3 event data.

Note:
For the DNP Events to be transmitted it is mandatory to have the corresponding DDBs of the Configured Point Index to be included in the Courier Event Record. The RECORD CONTROL Menu lists all the DDBs, and the mask settings control their inclusion/exclusion as a Courier Event.

17.9.3.3 OBJECT 10 BINARY OUTPUTS

Object 10, binary outputs, contains commands that can be operated using DNP 3.0. Therefore the points accept commands of type pulse on (null, trip, close) and latch on/off as detailed in the device profile in the relevant Menu Database document, and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

There is an additional image of the Control Inputs. Described as Alias Control Inputs, they reflect the state of the Control Input, but with a dynamic nature.

- If the Control Input DDB signal is already SET and a new DNP SET command is sent to the Control Input, the Control Input DDB signal goes momentarily to RESET and then back to SET.
- If the Control Input DDB signal is already RESET and a new DNP RESET command is sent to the Control Input, the Control Input DDB signal goes momentarily to SET and then back to RESET.

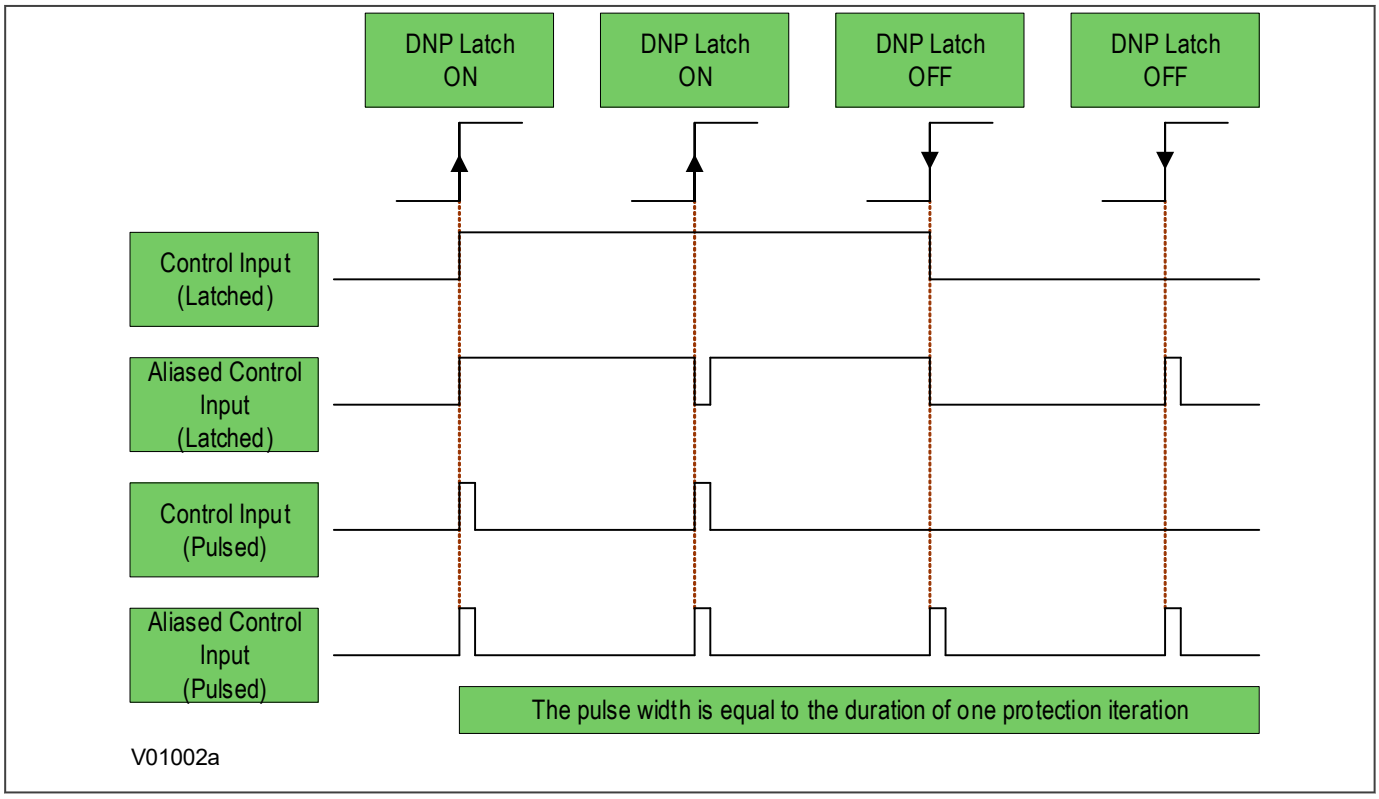


Figure 237: Control input behaviour

Many of the IED's functions are configurable so some of the Object 10 commands described in the following sections may not be available. A read from Object 10 reports the point as off-line and an operate command to Object 12 generates an error response.

Examples of Object 10 points that maybe reported as off-line are:

- Activate setting groups: Ensure setting groups are enabled
- CB trip/close: Ensure remote CB control is enabled
- Reset NPS thermal: Ensure NPS thermal protection is enabled
- Reset thermal O/L: Ensure thermal overload protection is enabled
- Reset RTD flags: Ensure RTD Inputs is enabled
- Control inputs: Ensure control inputs are enabled

17.9.3.4 OBJECT 20 BINARY COUNTERS

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from Object 20, or as a 'frozen' value from Object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding Object 21 frozen counter. The freeze and clear function resets the Object 20 running counter to zero after freezing its value.

Binary counter and frozen counter change event values are available for reporting from Object 22 and Object 23 respectively. Counter change events (Object 22) only report the most recent change, so the maximum number of events supported is the same as the total number of counters. Frozen counter change events (Object 23) are generated whenever a freeze operation is performed and a change has occurred since the previous freeze command. The frozen counter event queues store the points for up to two freeze operations.

17.9.3.5 OBJECT 30 ANALOGUE INPUT

Object 30, analogue inputs, contains information from the IED's measurements columns in the menu. All object 30 points can be reported as 16 or 32-bit integer values with flag, 16 or 32-bit integer values without flag, as well as short floating point values.

Analogue values can be reported to the master station as primary, secondary or normalized values (which takes into account the IED's CT and VT ratios), and this is settable in the *COMMUNICATIONS* column in the IED. Corresponding deadband settings can be displayed in terms of a primary, secondary or normalized value. Deadband point values can be reported and written using Object 34 variations.

The deadband is the setting used to determine whether a change event should be generated for each point. The change events can be read using Object 32 or Object 60. These events are generated for any point which has a value changed by more than the deadband setting since the last time the data value was reported.

Any analogue measurement that is unavailable when it is read is reported as offline. For example, the frequency would be offline if the current and voltage frequency is outside the tracking range of the IED. All Object 30 points are reported as secondary values in DNP 3.0 (with respect to CT and VT ratios).

17.9.3.6 OBJECT 40 ANALOGUE OUTPUT

The conversion to fixed-point format requires the use of a scaling factor, which is configurable for the various types of data within the IED such as current, voltage, and phase angle. All Object 40 points report the integer scaling values and Object 41 is available to configure integer scaling quantities.

17.9.3.7 OBJECT 50 TIME SYNCHRONISATION

Function codes 1 (read) and 2 (write) are supported for Object 50 (time and date) variation 1. The DNP Need Time function (the duration of time waited before requesting another time sync from the master) is supported, and is configurable in the range 1 - 30 minutes.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

17.9.3.8 DNP3 DEVICE PROFILE

This section describes the specific implementation of DNP version 3.0 within GE Vernova MiCOM P40 Agile IEDs for both compact and modular ranges.

The devices use the DNP 3.0 Slave Source Code Library version 3 from Triangle MicroWorks Inc.

This document, in conjunction with the DNP 3.0 Basic 4 Document Set, and the DNP Subset Definitions Document, provides complete information on how to communicate with the devices using the DNP 3.0 protocol.

This implementation of DNP 3.0 is fully compliant with DNP 3.0 Subset Definition Level 2. It also contains many Subset Level 3 and above features.

17.9.3.8.1 DNP3 DEVICE PROFILE TABLE

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a “Document”, it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a "Document", it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

DNP 3.0 Device Profile Document	
Vendor Name:	GE Vernova
Device Name:	MiCOM P40Agile Protection Relays - compact and modular range
Models Covered:	All models
Highest DNP Level Supported*: * This is the highest DNP level FULLY supported. Parts of level 3 are also supported	For Requests: Level 2 For Responses: Level 2
Device Function:	Slave
Notable objects, functions, and/or qualifiers supported in addition to the highest DNP levels supported (the complete list is described in the DNP 3.0 Implementation Table): For static (non-change event) object requests, request qualifier codes 00 and 01 (start-stop), 07 and 08 (limited quantity), and 17 and 28 (index) are supported in addition to the request qualifier code 06 (no range (all points)) Static object requests sent with qualifiers 00, 01, 06, 07, or 08 will be responded with qualifiers 00 or 01 Static object requests sent with qualifiers 17 or 28 will be responded with qualifiers 17 or 28 For change-event object requests, qualifiers 17 or 28 are always responded 16-bit and 32-bit analogue change events with time may be requested The read function code for Object 50 (time and date) variation 1 is supported Analogue Input Deadbands, Object 34, variations 1 through 3, are supported Floating Point Analogue Output Status and Output Block Objects 40 and 41 are supported Sequential file transfer, Object 70, variations 2 through 7, are supported Device Attribute Object 0 is supported	
Maximum Data Link Frame Size (octets):	Transmitted: 292 Received: 292
Maximum Application Fragment Size (octets)	Transmitted: Configurable (100 to 2048). Default 2048 Received: 249
Maximum Data Link Retries:	Fixed at 2
Maximum Application Layer Retries:	None
Requires Data Link Layer Confirmation:	Configurable to Never or Always
Requires Application Layer Confirmation:	When reporting event data (Slave devices only) When sending multi-fragment responses (Slave devices only)
Timeouts while waiting for:	
Data Link Confirm:	Configurable
Complete Application Fragment:	None
Application Confirm:	Configurable
Complete Application Response:	None
Others:	
Data Link Confirm Timeout:	Configurable from 0 (Disabled) to 120s, default 10s.
Application Confirm Timeout:	Configurable from 1 to 120s, default 2s.

DNP 3.0 Device Profile Document	
Select/Operate Arm Timeout:	Configurable from 1 to 10s, default 10s.
Need Time Interval (Set IIN1-4):	Configurable from 1 to 30, default 10min.
Application File Timeout	60 s
Analog Change Event Scan Period:	Fixed at 0.5s
Counter Change Event Scan Period	Fixed at 0.5s
Frozen Counter Change Event Scan Period	Fixed at 1s
Maximum Delay Measurement Error:	2.5 ms
Time Base Drift Over a 10-minute Interval:	7 ms
Sends/Executes Control Operations:	
Write Binary Outputs:	Never
Select/Operate:	Always
Direct Operate:	Always
Direct Operate - No Ack:	Always
Count > 1	Never
Pulse On	Always
Pulse Off	Sometimes
Latch On	Always
Latch Off	Always
Queue	Never
Clear Queue	Never
Note: Paired Control points will accept Pulse On/Trip and Pulse On/Close, but only single point will accept the Pulse Off control command.	
Reports Binary Input Change Events when no specific variation requested:	Configurable to send one or the other
Reports time-tagged Binary Input Change Events when no specific variation requested:	Binary input change with time
Sends Unsolicited Responses:	Never
Sends Static Data in Unsolicited Responses:	Never No other options are permitted
Default Counter Object/Variation:	Configurable, Point-by-point list attached Default object: 20 Default variation: 1
Counters Roll Over at:	32 bits
Sends multi-fragment responses:	Yes
Sequential File Transfer Support:	
Append File Mode	No
Custom Status Code Strings	No
Permissions Field	Yes
File Events Assigned to Class	No
File Events Send Immediately	Yes
Multiple Blocks in a Fragment	No
Max Number of Files Open	1

17.9.3.8.2 DNP3 IMPLEMENTATION TABLE

The implementation table provides a list of objects, variations and control codes supported by the device:

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
1	0	Binary Input (Variation 0 is used to request default variation)	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
1	1 (default - see note 1)	Binary Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
1	2	Binary Input with Flag	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
2	0	Binary Input Change - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
2	1	Binary Input Change without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
2	2	Binary Input Change with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
10	0	Binary Output Status - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
10	2 (default - see note 1)	Binary Output Status	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
12	1	Control Relay Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28	(index)	129	response		echo of request
20	0	Binary Counter - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
			7 8 9 10	(freeze) (freeze noack) (freeze clear) (frz. cl. Noack)	00, 01 06 07, 08	(start-stop) (no range, or all) (limited qty)				
20	1	32-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	2	16-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	5 (default - see note 1)	32-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	6	16-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	0	Frozen Counter - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
21	1	32-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
21	2	16-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	5	32-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 1)
21	6	16-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) 17, 28 (index - see note 1)
21	9 (default - see note 1)	32-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	10	16-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
`22	0	Counter Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
22	1 (default - see note 1)	32-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	2	16-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	5	32-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	6	16-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	0	Frozen Counter Event (Variation 0 is used to request default variation)	1	(read)	06 07, 08	(no range, or all) (limited qty)				
23	1 (default - see note 1)	32-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	2	16-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	5	32-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	6	16-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
30	0	Analog Input - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
30	1	32-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	2	16-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	3 (default - see note 1)	32-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	4	16-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	5	Short floating point	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
32	0	Analog Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
32	1 (default - see note 1)	32-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	2	16-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	3	32-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	4	16-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	5	Short floating point Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	7	Short floating point Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
34	0	Analog Input Deadband (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
34	1	16 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
34	2 (default - see note 1)	32 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
34	3	Short Floating Point Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
40	0	Analog Output Status (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
40	1 (default - see note 1)	32-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
40	2	16-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
40	3	Short Floating Point Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
41	1	32-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request
41	2	16-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
41	3	Short Floating Point Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 27, 28	(index)	129	response		echo of request
50	1 (default - see note 1)	Time and Date	1	(read)	07	(limited qty = 1)	129	response	07	(limited qty = 1)
			2	(write)	07	(limited qty = 1)				
60	0	Not defined								
60	1	Class 0 Data	1	(read)	06	(no range, or all)				
60	2	Class 1 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
60	3	Class 2 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
60	4	Class 3 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
70	0	File Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
70	2	File Authentication	29	(authenticate)	5b	(free-format)	129	response		5B (free-format)
70	3	File Command	25 27	(open) (delete)	5b	(free-format)				
70	4	File Command Status	26 30	(close) (abort)	5b	(free-format)	129	response		5B (free-format)
70	5	File Transfer	1	(read)	5b	(free-format)	129	response		5B (free-format)
70	6	File Transfer Status					129	response		5B (free-format)
70	7	File Descriptor	28	(get file info)	5b	(free-format)	129	response		5B (free-format)
80	1	Internal Indications	1	(read)	00, 01	(start-stop)	129	response	00, 01	(start-stop)
		No Object (function code only)	13	(cold restart)						
		No Object (function code only)	14	(warm restart)						
		No Object (function code only)	23	(delay meas.)						

Note:
A Default variation refers to the variation responded to when variation 0 is requested and/or in class 0, 1, 2, or 3 scans.

Note:
For static (non-change-event) objects, qualifiers 17 or 28 are only responded to when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded to with qualifiers 00 or 01. For change-event objects, qualifiers 17 or 28 are always responded to.

17.9.3.8.3 DNP3 INTERNAL INDICATIONS

The following table lists the DNP3.0 Internal Indications (IIN) and identifies those that are supported by the device.

The IIN form an information element used to convey the internal states and diagnostic results of a device. This information can be used by a receiving station to perform error recovery or other suitable functions. The IIN is a two-octet field that follows the function code in all responses from the device. When a request cannot be processed due to formatting errors or the requested data is not available, the IIN is always returned with the appropriate bits set.

Bit	Indication	Description	Supported
Octet 1			
0	All stations message received	Set when a request is received with the destination address of the all stations address (6553510). It is cleared after the next response (even if a response to a global request is required). This IIN is used to let the master station know that a "broadcast" message was received by the relay.	Yes
1	Class 1 data available	Set when data that has been configured as Class 1 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
2	Class 2 data available	Set when data that has been configured as Class 2 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
3	Class 3 data available	Set when data that has been configured as Class 3 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
4	Time-synchronisation required	The relay requires time synchronization from the master station (using the Time and Date object). This IIN is cleared once the time has been synchronised. It can also be cleared by explicitly writing a 0 into this bit of the Internal Indication object.	Yes
5	Local	Set when some or all of the relays digital output points (Object 10/12) are in the Local state. That is, the relays control outputs are NOT accessible through the DNP protocol. This IIN is clear when the relay is in the Remote state. That is, the relays control outputs are fully accessible through the DNP protocol.	No
6	Device in trouble	Set when an abnormal condition exists in the relay. This IIN is only used when the state cannot be described by a combination of one or more of the other IIN bits.	No
7	Device restart	Set when the device software application restarts. This IIN is cleared when the master station explicitly writes a 0 into this bit of the Internal Indications object.	Yes
Octet 2			
0	Function code not implemented	The received function code is not implemented within the relay.	Yes
1	Requested object(s) unknown	The relay does not have the specified objects or there are no objects assigned to the requested class. This IIN should be used for debugging purposes and usually indicates a mismatch in device profiles or configuration problems.	Yes
2	Out of range	Parameters in the qualifier, range or data fields are not valid or out of range. This is a 'catch-all' for application request formatting errors. It should only be used for debugging purposes. This IIN usually indicates configuration problems.	Yes
3	Buffer overflow	Event buffer(s), or other application buffers, have overflowed. The master station should attempt to recover as much data as possible and indicate to the user that there may be lost data. The appropriate error recovery procedures should be initiated by the user.	Yes

Bit	Indication	Description	Supported
4	Already executing	The received request was understood but the requested operation is already executing.	
5	Bad configuration	Set to indicate that the current configuration in the relay is corrupt. The master station may download another configuration to the relay.	Yes
6	Reserved	Always returned as zero.	
7	Reserved	Always returned as zero.	

17.9.3.8.4 DNP3 RESPONSE STATUS CODES

When the device processes Control Relay Output Block (Object 12) requests, it returns a set of status codes; one for each point contained within the original request. The complete list of codes appears in the following table:

Code Number	Identifier Name	Description
0	Success	The received request has been accepted, initiated, or queued.
1	Timeout	The request has not been accepted because the 'operate' message was received after the arm timer (Select Before Operate) timed out. The arm timer was started when the select operation for the same point was received.
2	No select	The request has not been accepted because no previous matching 'select' request exists. (An 'operate' message was sent to activate an output that was not previously armed with a matching 'select' message).
3	Format error	The request has not been accepted because there were formatting errors in the control request ('select', 'operate', or 'direct operate').
4	Not supported	The request has not been accepted because a control operation is not supported for this point.
5	Already active	The request has not been accepted because the control queue is full or the point is already active.
6	Hardware error	The request has not been accepted because of control hardware problems.
7	Local	The request has not been accepted because local access is in progress.
8	Too many operations	The request has not been accepted because too many operations have been requested.
9	Not authorized	The request has not been accepted because of insufficient authorisation.
127	Undefined	The request not been accepted because of some other undefined reason.

Note:
Code numbers 10 through to 126 are reserved for future use.

17.9.3.8.5 DNP3 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the chosen communication protocol – in this case `DNP3.0`.
4. Move down to the next cell (***RP1 Address***). This cell controls the DNP3.0 address of the IED. Up to 32 IEDs can be connected to one spur, therefore it is necessary for each IED to have a unique address so that messages from the master control station are accepted by only one IED. DNP3.0 uses a decimal number between 1 and 65519 for the Relay Address. It is important that no two IEDs have the same address.

5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Six baud rates are supported by the IED 1200 bps, 2400 bps, 4800 bps, 9600 bps, 19200 bps and 38400 bps. Make sure that the baud rate selected on the IED is the same as that set on the master station.
6. Move down to the next cell (***RP1 Parity***). This cell controls the parity format used in the data frames. The parity can be set to be one of `None`, `Odd` or `Even`. Make sure that the parity format selected on the IED is the same as that set on the master station.
7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).
8. Move down to the next cell (***RP1 Time Sync***). This cell affects the time synchronisation request from the master by the IED. It can be set to `enabled` or `disabled`. If enabled it allows the DNP3.0 master to synchronise the time on the IED.

17.9.3.8.5.1 DNP3 CONFIGURATOR

A PC support package for DNP3.0 is available as part of the supplied settings application software (MiCOM S1 Agile) to allow configuration of the device's DNP3.0 response. The configuration data is uploaded from the device to the PC in a block of compressed format data and downloaded in a similar manner after modification. The new DNP3.0 configuration takes effect after the download is complete. To restore the default configuration at any time, from the *CONFIGURATION* column, select the ***Restore Defaults*** cell then select `All Settings`.

In MiCOM S1 Agile, the DNP3.0 data is shown in three main folders, one folder each for the point configuration, integer scaling and default variation (data format). The point configuration also includes screens for binary inputs, binary outputs, counters and analogue input configuration.

If the device supports DNP Over Ethernet, the configuration related settings are done in the folder **DNP Over Ethernet**.

17.9.4 IEC 61850

This section describes how the IEC 61850 standard is applied to GE Vernova products. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 61850 standard.

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions within a substation, and additionally provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security that is so essential in substations today.

There are two editions of most parts of the IEC 61850 standard; edition 1 and edition 2. This product supports IEC 61850 edition 2 only.

17.9.4.1 BENEFITS OF IEC 61850

The standard provides:

- Standardised models for IEDs and other equipment within the substation
- Standardised communication services (the methods used to access and exchange data)
- Standardised formats for configuration files
- Peer-to-peer communication

The standard adheres to the requirements laid out by the ISO OSI model and therefore provides complete vendor interoperability and flexibility on the transmission types and protocols used. This includes mapping of data onto

Ethernet, which is becoming more and more widely used in substations, in favour of RS485. Using Ethernet in the substation offers many advantages, most significantly including:

- Ethernet allows high-speed data rates (currently 100 Mbps, rather than tens of kbps or less used by most serial protocols)
- Ethernet provides the possibility to have multiple clients
- Ethernet is an open standard in every-day use
- There is a wide range of Ethernet-compatible products that may be used to supplement the LAN installation (hubs, bridges, switches)

17.9.4.2 IEC 61850 INTEROPERABILITY

A major benefit of IEC 61850 is interoperability. IEC 61850 standardizes the data model of substation IEDs, which allows interoperability between products from multiple vendors.

An IEC 61850-compliant device may be interoperable, but this does not mean it is interchangeable. You cannot simply replace a product from one vendor with that of another without reconfiguration. However, the terminology is pre-defined and anyone with prior knowledge of IEC 61850 should be able to integrate a new device very quickly without having to map all of the new data. IEC 61850 brings improved substation communications and interoperability to the end user, at a lower cost.

17.9.4.3 THE IEC 61850 DATA MODEL

The data model of any IEC 61850 IED can be viewed as a hierarchy of information, whose nomenclature and categorization is defined and standardized in the IEC 61850 specification.

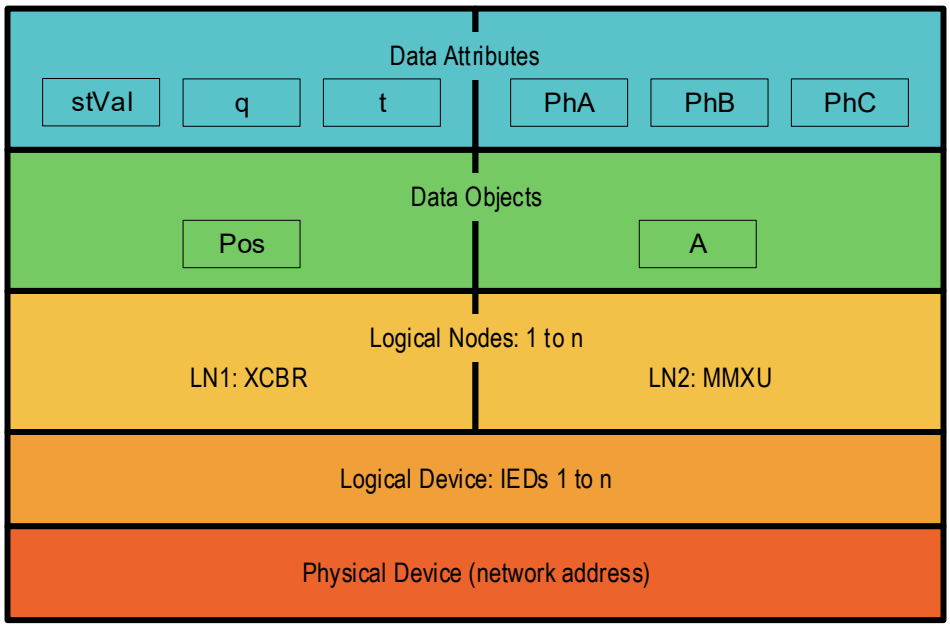


Figure 238: Data model layers in IEC 61850

The levels of this hierarchy can be described as follows:

Data Frame format

Layer	Description
Physical Device	Identifies the actual IED within a system. Typically the device's name or IP address can be used (for example Feeder_1 or 10.0.0.2.
Logical Device	Identifies groups of related Logical Nodes within the Physical Device. For the MiCOM IEDs, multiple Logical Devices exist, for System (root LD) and various Control, Measurements, Protection, and Records LDs.
Wrapper/Logical Node Instance	Identifies the major functional areas within the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name suffixed by an instance number. For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2).
Data Object	This next layer is used to identify the type of data you will be presented with. For example, Pos (position) of Logical Node type XCBR.
Data Attribute	This is the actual data (measurement value, status, description, etc.). For example, stVal (status value) indicating actual position of circuit breaker for Data Object type Pos of Logical Node type XCBR.

17.9.4.4 IEC 61850 IN MICOM IEDS

IEC 61850 is implemented by use of a separate Ethernet board. This Ethernet board manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection functions.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 client (or master), for example a bay computer (MiCOM C264)
- An HMI
- An MMS browser, with which the full data model can be retrieved from the IED, without any prior knowledge of the IED

The IEC 61850 compatible interface standard provides capability for the following:

- Read access to measurements
- Refresh of all measurements at a standard rate.
- Generation of non-buffered and buffered multi-client reports on change of status or measurement
- SNTP time synchronization over an Ethernet link. (This is used to synchronize the IED's internal real time clock.
- GOOSE peer-to-peer communication
- Disturbance record extraction by IEC 61850 MMS file transfer. The record is extracted as an ASCII format COMTRADE file
- Controls (Direct and Select Before Operate)

Note:
Setting changes are not supported in the current IEC 61850 implementation. Currently these setting changes are carried out using the settings application software.

17.9.4.5 IEC 61850 DATA MODEL IMPLEMENTATION

The data model naming adopted in the IEDs has been standardised for consistency. The Logical Nodes are allocated under Logical Devices, as appropriate.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available as a separate document.

17.9.4.6 IEC 61850 COMMUNICATION SERVICES IMPLEMENTATION

The IEC 61850 communication services which are implemented in the IEDs are described in the Protocol Implementation Conformance Statement (PICS) document, which is available as a separate document.

17.9.4.7 IEC 61850 PEER-TO-PEER (GOOSE) COMMUNICATIONS

The implementation of IEC 61850 Generic Object Oriented Substation Event (GOOSE) enables faster communication between IEDs offering the possibility for a fast and reliable system-wide distribution of input and output data values. The GOOSE model uses multicast services to deliver event information. Multicast messaging means that messages are sent to selected devices on the network. The receiving devices can specifically accept frames from certain devices and discard frames from the other devices. It is also known as a publisher-subscriber system. When a device detects a change in one of its monitored status points it publishes a new message. Any device that is interested in the information subscribes to the data it contains.

17.9.4.8 GOOSE MESSAGE VALIDATION

Whenever a new GOOSE message is received its validity is checked before the dataset is decoded and used to update the Programmable Scheme Logic. As part of the validation process a check is made for state and sequence number anomalies. If an anomaly is detected, the 'out-of-order' GOOSE message is discarded. When a message is discarded the last valid message remains active until a new valid GOOSE message is received or its validity period (TAL) expires.

Out-of-order GOOSE message indicators and reporting are provided to the subscriber via the IEC61850 LGOS logical node.

17.9.4.9 MAPPING GOOSE MESSAGES TO VIRTUAL INPUTS

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the virtual inputs within the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

An IED can subscribe to all GOOSE messages but only the following data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2
- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

17.9.4.10 IEC 61850 GOOSE CONFIGURATION

All GOOSE configuration is performed using the IEC 61850 Configurator tool available in the MiCOM S1 Agile software application.

All GOOSE publishing configuration can be found under the **GOOSE Publishing** tab in the configuration editor window. All GOOSE subscription configuration parameters are under the **External Binding** tab in the configuration editor window.

Settings to enable GOOSE signalling and to apply Test Mode are available using the HMI.

17.9.4.11 ETHERNET FUNCTIONALITY

IEC 61850 **Associations** are unique and made between the client and server. If Ethernet connectivity is lost for any reason, the associations are lost, and will need to be re-established by the client. The IED has a **TCP_KEEPALIVE** function to monitor each association, and terminate any which are no longer active.

The IED allows the re-establishment of associations without disruption of its operation, even after its power has been removed. As the IED acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost, and reports requested by connected clients are reset. The client must re-enable these when it next creates the new association to the IED.

17.9.4.12 IEC 61850 CONFIGURATION

To configure the device for IEC 61850, it is recommended to use the IEC 61850 IED Configurator, which is part of the settings application software. You can also configure it with the HMI. To configure IEC61850 edition 2 using the HMI, you must first enable the IP From HMI setting, after which you can set the media (copper or fibre), IP address, subnet mask and gateway address.

IEC 61850 allows IEDs to be directly configured from a configuration file. The IED's system configuration capabilities are determined from an IED Capability Description file (ICD), supplied with the product. By using ICD files from the products to be installed, you can design, configure and test (using simulation tools), a substation's entire protection scheme before the products are installed into the substation.

To help with this process, the settings application software provides an IEC 61850 Configurator tool, which allows the pre-configured IEC 61850 configuration file to be imported and transferred to the IED. As well as this, you can manually create configuration files for all products, based on their original IED capability description (ICD file).

Other features include:

- The extraction of configuration data for viewing and editing.
- A sophisticated error checking sequence to validate the configuration data before sending to the IED.

Note:
Some configuration data is available in the IEC61850 CONFIG. column, allowing read-only access to basic configuration data.

17.9.4.12.1 IEC 61850 CONFIGURATION BANKS

There are two configuration banks:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the IED is automatically stored in the inactive configuration bank, therefore not immediately affecting the current configuration.

Following an upgrade, the IEC 61850 Configurator tool can be used to transmit a command, which authorises activation of the new configuration contained in the inactive configuration bank. This is done by switching the active and inactive configuration banks. The capability of switching the configuration banks is also available using the *IEC61850 CONFIG.* column of the HMI.

The SCL Name and Revision attributes of both configuration banks are available in the *IEC61850 CONFIG.* column of the HMI.

17.9.4.12.2 IEC 61850 NETWORK CONNECTIVITY

Configuration of the IP parameters and SNTP (Simple Network Time Protocol) time synchronisation parameters is performed by the IEC 61850 Configurator tool. If these parameters are not available using an SCL (Substation Configuration Language) file, they must be configured manually.

Every IP address on the Local Area Network must be unique. Duplicate IP addresses result in conflict and must be avoided. Most IEDs check for a conflict on every IP configuration change and at power up and they raise an alarm if an IP conflict is detected.

The IED can be configured to accept data from other networks using the ***Gateway*** setting. If multiple networks are used, the IP addresses must be unique across networks.

17.9.4.13 IEC 61850 EDITION 2

Many parts of the IEC 61850 standard have now been released as the second edition. This offers some significant enhancements including:

- Improved interoperability
- Many new logical nodes
- Better defined testing; it is now possible to perform off-line testing and simulation of functions

Edition 2 implementation requires use of version 3.8 of the IEC 61850 configurator, which is installed with version 2.0.1 of MiCOM S1 Agile.

17.9.4.13.1 BACKWARD COMPATIBILITY

IEC61850 System - Backward compatibility

An Edition 1 IED can operate with an Edition 2 IEC 61850 system, provided that the Edition 1 IEDs do not subscribe to GOOSE messages with data objects or data attributes which are only available in Edition 2.

The following figure explains this concept:

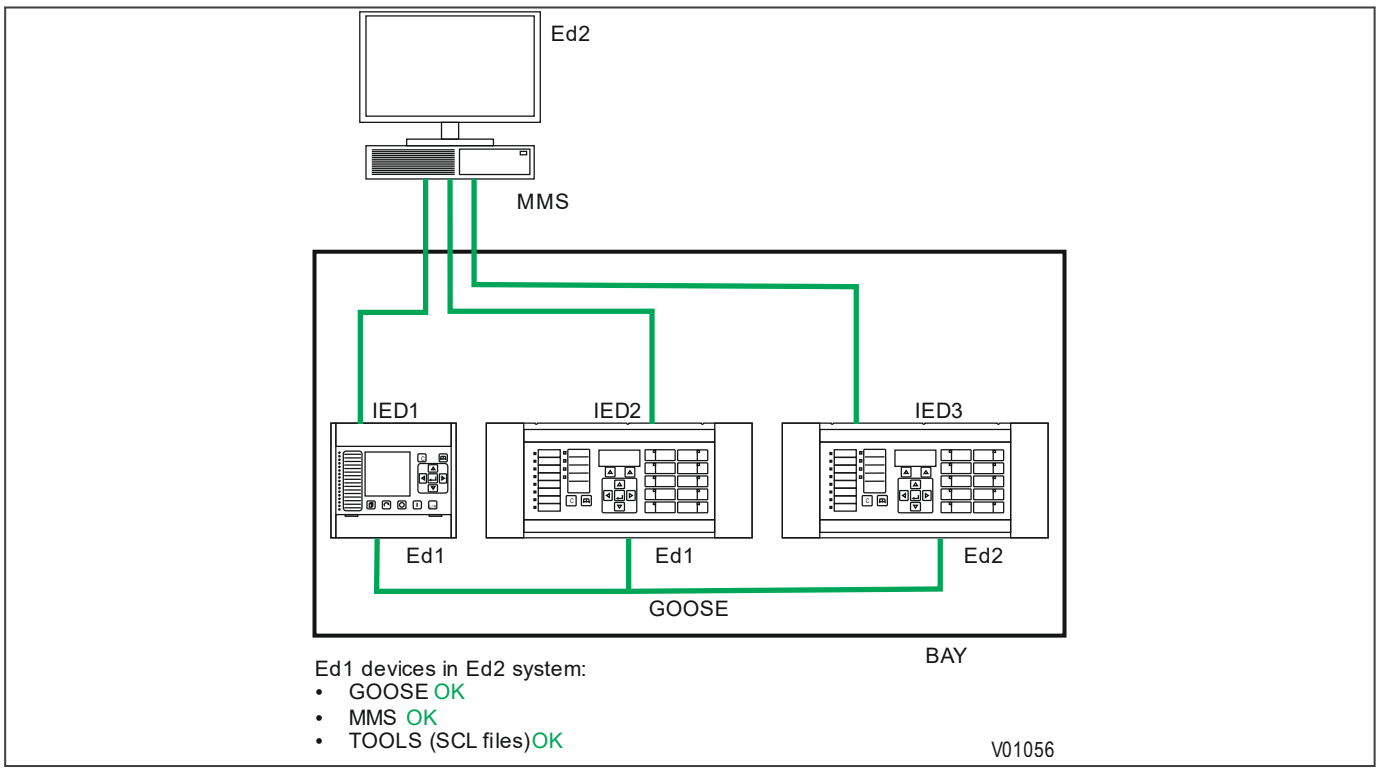


Figure 239: Edition 2 system - backward compatibility

An Edition 2 IED cannot normally operate within an Edition 1 IEC 61850 system. An Edition 2 IED can work for GOOSE messaging in a mixed system, providing the client is compatible with Edition 2.

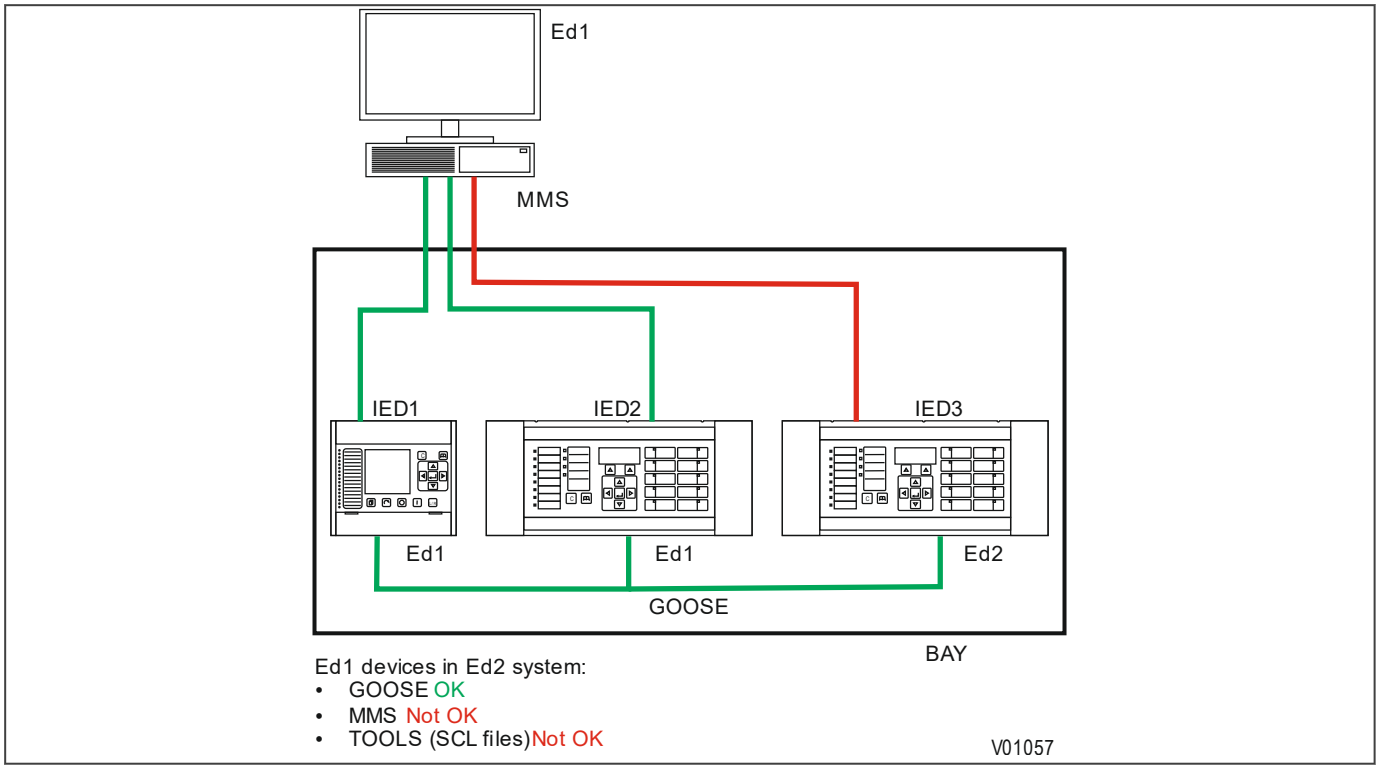


Figure 240: Edition 1 system - forward compatibility issues

17.9.4.13.2 EDITION-2 COMMON DATA CLASSES

The following common data classes (CDCs) are new to Edition 2 and therefore should not be used in GOOSE control blocks in mixed Edition 1 and Edition 2 systems

- Histogram (HST)
- Visible string status (VSS)
- Object reference setting (ORG)
- Controllable enumerated status (ENC)
- Controllable analogue process value (APC)
- Binary controlled analogue process value (BAC)
- Enumerated status setting (ENG)
- Time setting group (TSG)
- Currency setting group (CUG)
- Visible string setting (VSG)
- Curve shape setting (CSG)

Of these, only ENS and ENC types are available from a MiCOM P40 IED when publishing GOOSE messages, so Data Objects using these Common Data Classes should not be published in mixed Edition 1 and Edition 2 systems.

For compatibility between Edition 1 and Edition 2 IEDs, SCL files using SCL schema version "2.1" must be used. For a purely Edition 2 system, use the schema version "2007B4".

17.9.5 READ ONLY MODE

With IEC 61850 and Ethernet/Internet communication capabilities, security has become an important issue. For this reason, all relevant GE Vernova IEDs have been adapted to comply with the latest cyber-security standards.

In addition to this, a facility is provided which allows you to enable or disable the communication interfaces. This feature is available for products using Courier, IEC 60870-5-103, or IEC 61850.

17.9.5.1 IEC 60870-5-103 PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with IEC 60870-5-103, the following commands are blocked at the interface:

- Write parameters (=change setting) (private ASDUs)
- General Commands (ASDU20), namely:
  - INF16 auto-recloser on/off
  - INF19 LED reset
  - Private INFs (for example: CB open/close, Control Inputs)

The following commands are still allowed:

- Poll Class 1 (Read spontaneous events)
- Poll Class 2 (Read measurands)
- GI sequence (ASDU7 'Start GI', Poll Class 1)
- Transmission of Disturbance Records sequence (ASDU24, ASDU25, Poll Class 1)
- Time Synchronisation (ASDU6)
- General Commands (ASDU20), namely:
  - INF23 activate characteristic 1
  - INF24 activate characteristic 2
  - INF25 activate characteristic 3
  - INF26 activate characteristic 4

Note:
For IEC 60870-5-103, Read Only Mode function is different from the existing Command block feature.

17.9.5.2 COURIER PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with Courier, the following commands are blocked at the interface:

- Write settings
- All controls, including:
  - Reset Indication (Trip LED)
  - Operate Control Inputs
  - CB operations
  - Auto-reclose operations
  - Reset demands
  - Clear event/fault/maintenance/disturbance records
  - Test LEDs & contacts

The following commands are still allowed:

- Read settings, statuses, measurands
- Read records (event, fault, disturbance)
- Time Synchronisation
- Change active setting group

17.9.5.3 IEC 61850 PROTOCOL BLOCKING

If Read-Only Mode is enabled for the Ethernet interfacing with IEC 61850, the following commands are blocked at the interface:

- All controls, including:
  - Enable/disable protection
  - Operate Control Inputs
  - CB operations (Close/Trip, Lock)
  - Reset LEDs

The following commands are still allowed:

- Read statuses, measurands
- Generate reports
- Extract disturbance records
- Time synchronisation
- Change active setting group

17.9.5.4 READ-ONLY SETTINGS

The following settings are available for enabling or disabling Read Only Mode.

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

17.9.5.5 READ-ONLY DDB SIGNALS

The remote read only mode is also available in the PSL using three dedicated DDB signals:

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

Using the PSL, these signals can be activated by opto-inputs, Control Inputs and function keys if required.

17.10 TIME SYNCHRONISATION

In modern protection schemes it is necessary to synchronise the IED's real time clock so that events from different devices can be time stamped and placed in chronological order. This is achieved in various ways depending on the chosen options and communication protocols.

- Using the IRIG-B input (if fitted)
- Using the SNTP time protocol (for Ethernet IEC 61850 versions)
- Using IEEE 1588 Precision Time Protocol (PTP)
- By using the time synchronisation functionality inherent in the data protocols

The time synchronisation sources can be configured in a priority order using the Primary Source and Secondary Source cells in the DATE AND TIME column. If the Primary source becomes unavailable, the Secondary source will be used, if available.

17.10.1 IRIG-B

IRIG stands for Inter Range Instrumentation Group, which is a standards body responsible for standardising different time code formats. There are several different formats starting with IRIG-A, followed by IRIG-B and so on. The letter after the "IRIG" specifies the resolution of the time signal in pulses per second (PPS). IRIG-B, the one which we use has a resolution of 100 PPS. IRIG-B is used when accurate time-stamping is required.

The following diagram shows a typical GPS time-synchronised substation application. The satellite RF signal is picked up by a satellite dish and passed on to receiver. The receiver receives the signal and converts it into time signal suitable for the substation network. IEDs in the substation use this signal to govern their internal clocks and event recorders.

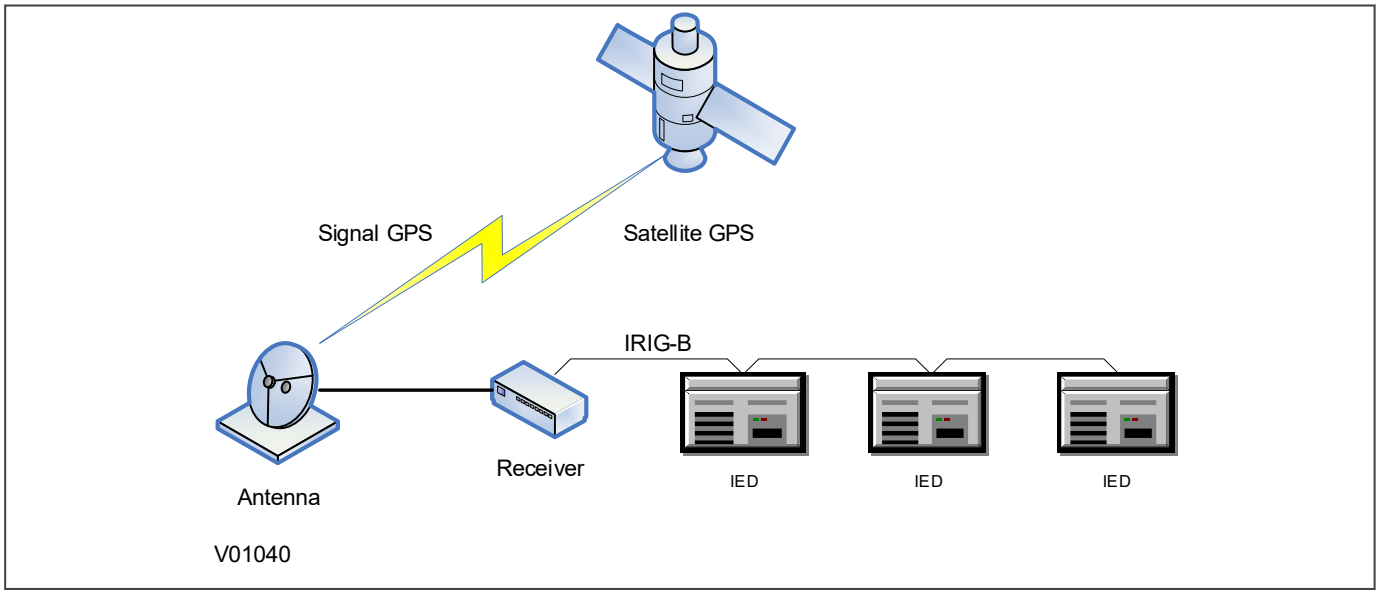


Figure 241: GPS satellite timing signal

The IRIG-B time code signal is a sequence of one second time frames. Each frame is split up into ten 100 mS slots as follows:

- Time-slot 1: Seconds
- Time-slot 2: Minutes

- Time-slot 3: Hours
- Time-slot 4: Days
- Time-slot 5 and 6: Control functions
- Time-slots 7 to 10: Straight binary time of day

The first four time-slots define the time in BCD (Binary Coded Decimal). Time-slots 5 and 6 are used for control functions, which control deletion commands and allow different data groupings within the synchronisation strings. Time-slots 7-10 define the time in SBS (Straight Binary Second of day).

17.10.1.1 IRIG-B IMPLEMENTATION

Depending on the chosen hardware options, the product can be equipped with an IRIG-B input for time synchronisation purposes. The IRIG-B interface is implemented either on a dedicated board, or together with other communication functionality such as Ethernet. The IRIG-B connection is presented by a connector is a BNC connector. IRIG-B signals are usually presented as an RF-modulated signal. The boards support universal IRIG-B, which means they accept demodulated or modulated IRIG-B.

To set the device to use IRIG-B, use the setting ***IRIG-B Sync*** cell in the *DATE AND TIME* column.

The IRIG-B status can be viewed in the ***IRIG-B Status*** cell in the *DATE AND TIME* column.

17.10.2 SNTP

SNTP is used to synchronise the clocks of computer systems over packet-switched, variable-latency data networks, such as IP. SNTP can be used as the time synchronisation method for models using IEC 61850 over Ethernet. A time synchronisation accuracy of within 5 ms is possible.

The device is synchronised by the main SNTP server. This is achieved by entering the IP address of the SNTP server into the IED using the IEC 61850 Configurator software described in the settings application software manual. A second server is also configured with a different IP address for backup purposes.

This function issues an alarm when there is a loss of time synchronisation on the SNTP server. This could be because there is no response or no valid clock signal.

The HMI menu does not contain any configurable settings relating to SNTP, as the only way to configure it is using the IEC 61850 Configurator. However it is possible to view some parameters in the *COMMUNICATIONS* column under the sub-heading SNTP parameters. Here you can view the SNTP server addresses and the SNTP poll rate in the cells ***SNTP Server 1***, ***SNTP Server 2*** and ***SNTP Poll rate*** respectively.

The SNTP time synchronisation status is displayed in the ***SNTP Status*** cell in the *DATE AND TIME* column.

17.10.2.1 LOSS OF SNTP SERVER SIGNAL ALARM

This function issues an alarm when there is a loss of time synchronization on the SNTP server. It is issued when the SNTP sever has not detected a valid time synchronisation response within its 5 second window. This is because there is no response or no valid clock. The alarm is mapped to IEC 61850.

17.10.3 IEEE 1588 PRECISION TIME PROTOCOL

The MiCOM P40 modular products support IEEE 1588 Precision Time Protocol (PTP) as a slave-only clock. MiCOM relays are profile unaware, which means that they will accept synchronisation from any PTP profile. Power Utility Profile (IEC 61850-9-3) is specifically designed to perform well for substation related applications, with PMU applications needing the most stringent requirements.

PTP can be used to replace or supplement IRIG-B and SNTP time synchronisation so that the IED can be synchronised using Ethernet messages from the substation LAN without any additional physical connections being required.

A dedicated DDB signal (***PTP Failure***) is provided to indicate failure of PTP.

17.10.3.1 ACCURACY AND DELAY CALCULATION

A time synchronisation accuracy of within 3 ms is possible. Both peer-to-peer or end-to-end mode delay measurement can be used.In peer-to-peer mode, delays are measured between each link in the network and are compensated for. This provides greater accuracy, but requires that every device between the Grand Master and Slaves supports the peer-to-peer delay measurement.

In end-to-end mode, delays are only measured between each Grand Master and Slave. The advantage of this mode is that the requirements for the switches on the network are lower; they do not need to independently calculate delays. The main disadvantage is that more inaccuracy is introduced, because the method assumes that forward and reverse delays are always the same, which may not always be correct.

When using end-to-end mode, the IED can be connected in a ring or line topology using RSTP or Self Healing Protocol without any additional Transparent Clocks. But because the IED is a slave-only device, additional inaccuracy is introduced. The additional error will be less than 1ms for a network of eight devices.

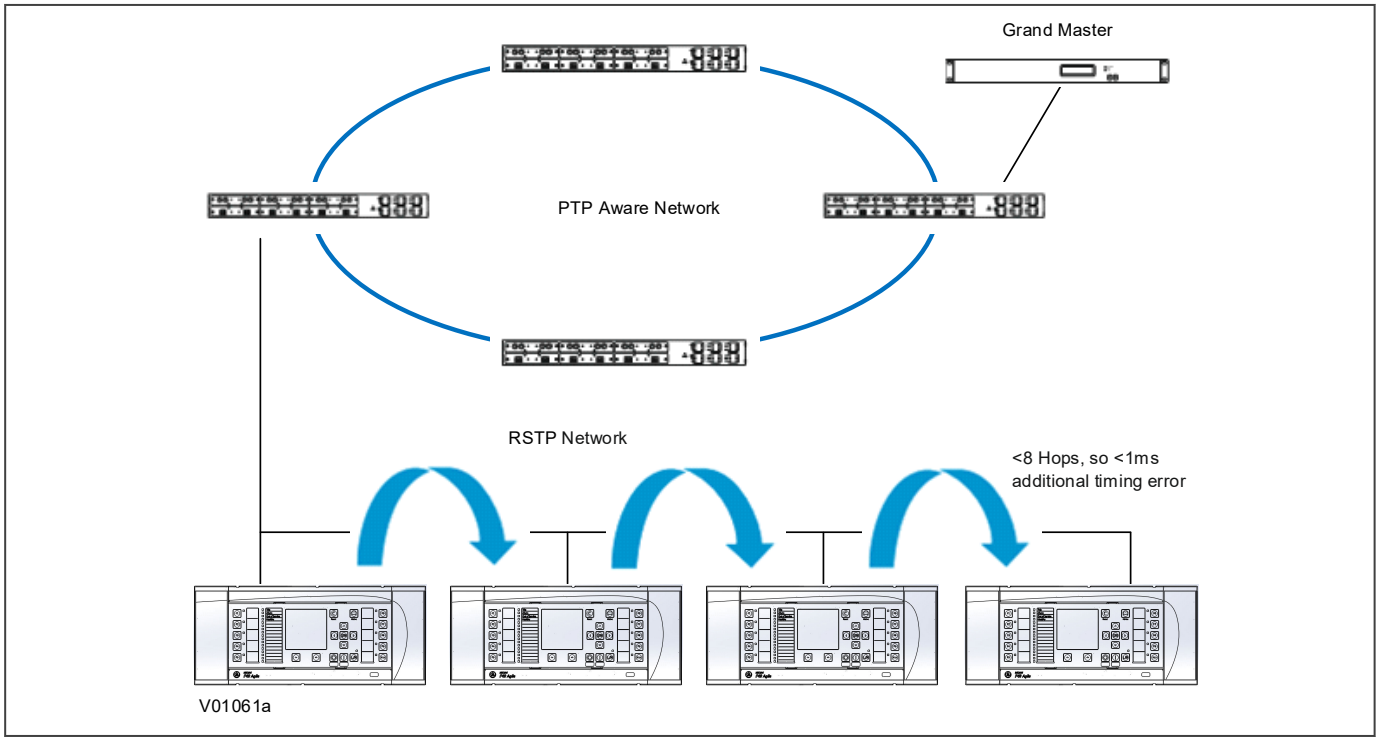


Figure 242: Timing error using ring or line topology

17.10.3.2 PTP DOMAINS

PTP traffic can be segregated into different domains using Boundary Clocks. These allow different PTP clocks to share the same network while maintaining independent synchronisation within each grouped set.

The PTP domain number can be configured in MiCOM P40 modular products the using the ***Domain Number*** cell in the *DATE AND TIME* column. The domain number needs to be configured to match the domain of the local network.

17.10.4 TIME SYNCHRONISATION USING THE COMMUNICATION PROTOCOLS

All communication protocols have in-built time synchronisation mechanisms. If an external time synchronisation mechanism such as IRIG-B, SNTP, or IEEE 1588 PTP is not used to synchronise the devices, the time synchronisation mechanism within the relevant serial protocol is used. The real time is usually defined in the master station and communicated to the relevant IEDs via one of the rear serial ports using the chosen protocol. It is also possible to define the time locally using settings in the *DATE AND TIME* column.

The time synchronisation for each protocol is described in the relevant protocol description section.

CHAPTER 18

CYBER-SECURITY

18.1 DISCLAIMER

GE Vernova Grid Automation products are digital devices designed to be installed and operated in utility substations & industrial plant environments and connected to secure private networks. GE Vernova IEDs should not be connected to the public internet.

GE Vernova strongly recommends that users protect their digital devices using a defense-in-depth strategy which will protect their products, their network, their systems and interfaces against cyber security threats. This includes, but is not limited to, placing digital devices inside the control system network security perimeter, deploying and maintaining access controls, monitoring and intrusion detection, security awareness training, security policies, network segmentation and firewalls installation, strong and active password management, data encryption, antivirus and other mitigating applicable technologies.

GE Vernova IEDs are available with standard features, and in some products additional optional software options, which provide cyber security mechanisms to help users protect against cyber security intrusion. GE Vernova strongly recommends using all available cyber security options.

For additional details and recommendations on how to protect the GE Vernova IEDs, please see Cyber Security sections of the manuals. GE Vernova Grid Automation may also provide additional instructions and recommendations to users from time to time relating to IED and cyber security threats or vulnerabilities.

It is the users' sole responsibility to make sure that all GE Vernova Grid Automation IEDs are installed and operated considering its cyber security capabilities, security context, and the instructions and recommendations provided to the user relating to GE Vernova. Users assume all risks and liability associated with damages or losses incurred in connection with any and all cyber security incidences.

IT IS THE SOLE RESPONSIBILITY OF THE USER TO SECURE THEIR NETWORK AND ASSOCIATED DEVICES AGAINST CYBER SECURITY INTRUSIONS OR ATTACKS. GE VERNOVA GRID AUTOMATION AND ITS AFFILIATES ARE NOT LIABLE FOR ANY DAMAGES AND/OR LOSSES ARISING FROM OR RELATED TO SUCH SECURITY INTRUSION OR ATTACKS.

18.2 OVERVIEW

In the past, substation networks were traditionally isolated and the protocols and data formats used to transfer information between devices were often proprietary.

For these reasons, the substation environment was very secure against cyber-attacks. The terms used for this inherent type of security are:

- Security by isolation (if the substation network is not connected to the outside world, it cannot be accessed from the outside world).
- Security by obscurity (if the formats and protocols are proprietary, it is very difficult to interpret them).

However, note that these are not recognised defences against attackers.

The increasing sophistication of protection schemes, coupled with the advancement of technology and the desire for vendor interoperability, has resulted in standardisation of networks and data interchange within substations. Today, devices within substations use standardised protocols for communication. Furthermore, substations can be interconnected with open networks, such as the internet or corporate-wide networks, which use standardised protocols for communication. This introduces a major security risk making the grid vulnerable to cyber-attacks, which could in turn lead to major electrical outages.

Clearly, there is now a need to secure communication and equipment within substation environments. This chapter describes the security measures that have been put in place for our range of Intelligent Electronic Devices (IEDs).

Note:
Cyber-security compatible devices do not enforce NERC compliance, they merely facilitate it. It is the responsibility of the user to ensure that compliance is adhered to as and when necessary.

This chapter contains the following sections:

18.3 THE NEED FOR CYBER-SECURITY

Cyber-security provides protection against unauthorised disclosure, transfer, modification, or destruction of information or information systems, whether accidental or intentional. To achieve this, there are several security requirements:

- Confidentiality (preventing unauthorised access to information)
- Integrity (preventing unauthorised modification)
- Availability/Authentication (preventing the denial of service and assuring authorised access to information)
- Non-repudiation (preventing the denial of an action that took place)
- Traceability/Detection (monitoring and logging of activity to detect intrusion and analyse incidents)

The threats to cyber-security may be unintentional (e.g. natural disasters, human error), or intentional (e.g. cyber-attacks by hackers).

Good cyber-security can be achieved with a range of measures, such as closing down vulnerability loopholes, implementing adequate security processes and procedures and providing technology to help achieve this.

Examples of vulnerabilities are:

- Indiscretions by personnel (users keep passwords on their computer)
- Bad practice (users do not change default passwords, or everyone uses the same password to access all substation equipment)
- Bypassing of controls (users turn off security measures)
- Inadequate technology (substation is not firewalled)

Examples of availability issues are:

- Equipment overload, resulting in reduced or no performance
- Expiry of a certificate preventing access to equipment

To help tackle these issues, standards organisations have produced various standards. Compliance with these standards significantly reduces the threats associated with lack of cyber-security.

18.4 STANDARDS

There are several standards, which apply to substation cyber-security. The standards currently applicable to Grid Automation Systems and IEDs are NERC and IEEE1686.

Standard	Country	Description
NERC CIP (North American Electric Reliability Corporation)	USA	Framework for the protection of the grid critical Cyber Assets
BDEW (German Association of Energy and Water Industries)	Germany	Requirements for Secure Control and Telecommunication Systems
ANSI ISA 99	USA	ICS oriented then Relevant for EPU completing existing standard and identifying new topics such as patch management
IEEE 1686	International	International Standard for substation IED cyber-security capabilities
IEC 62351	International	Power systems management and associated information exchange - Data and communications security
IEC 62443	International	Security for industrial automation and control systems
ISO/IEC 27002	International	Framework for the protection of the grid critical Cyber Assets
NIST SP800-53 (National Institute of Standards and Technology)	USA	Complete framework for SCADA SP800-82and ICS cyber-security
CPNI Guidelines (Centre for the Protection of National Infrastructure)	UK	Clear and valuable good practices for Process Control and SCADA security

18.4.1 NERC COMPLIANCE

The North American Electric Reliability Corporation (NERC) created a set of standards for the protection of critical infrastructure. These are known as the CIP standards (Critical Infrastructure Protection). These were introduced to ensure the protection of 'Critical Cyber Assets', which control or have an influence on the reliability of North America’s electricity generation and distribution systems.

These standards have been compulsory in the USA for several years now. Compliance auditing started in June 2007, and utilities face extremely heavy fines for non-compliance.

NERC CIP standards

CIP Standard	Description
CIP-002 Critical Cyber Assets	Define and document the Critical Assets and the Critical Cyber Assets
CIP-003 Security Management Controls	Define and document the Security Management Controls required to protect the Critical Cyber Assets
CIP-004 Personnel and Training	Define and Document Personnel handling and training required protecting Critical Cyber Assets
CIP-005 Electronic Security	Define and document logical security perimeters where Critical Cyber Assets reside. Define and document measures to control access points and monitor electronic access
CIP-006 Physical Security	Define and document Physical Security Perimeters within which Critical Cyber Assets reside

CIP Standard	Description
CIP-007 Systems Security Management	Define and document system test procedures, account and password management, security patch management, system vulnerability, system logging, change control and configuration required for all Critical Cyber Assets
CIP-008 Incident Reporting and Response Planning	Define and document procedures necessary when Cyber-security Incidents relating to Critical Cyber Assets are identified
CIP-009 Recovery Plans	Define and document Recovery plans for Critical Cyber Assets

18.4.1.1 CIP 002

CIP 002 concerns itself with the identification of:

- Critical assets, such as overhead lines and transformers
- Critical cyber assets, such as IEDs that use routable protocols to communicate outside or inside the Electronic Security Perimeter; or are accessible by dial-up

Power Utility Responsibilities	GE Vernova's Contribution
Create the list of the assets	We can help the power utilities to create this asset register automatically. We can provide audits to list the Cyber assets

18.4.1.2 CIP 003

CIP 003 requires the implementation of a cyber-security policy, with associated documentation, which demonstrates the management's commitment and ability to secure its Critical Cyber Assets.

The standard also requires change control practices whereby all entity or vendor-related changes to hardware and software components are documented and maintained.

Power Utility Responsibilities	GE Vernova's Contribution
To create a cyber-security policy	We can help the power utilities to have access control to its critical assets by providing centralized Access control. We can help the customer with its change control by providing a section in the documentation where it describes changes affecting the hardware and software.

18.4.1.3 CIP 004

CIP 004 requires that personnel with authorized cyber access or authorized physical access to Critical Cyber Assets, (including contractors and service vendors), have an appropriate level of training.

Power Utility Responsibilities	GE Vernova's Contribution
To provide appropriate training of its personnel	We can provide cyber-security training

18.4.1.4 CIP 005

CIP 005 requires the establishment of an Electronic Security Perimeter (ESP), which provides:

- The disabling of ports and services that are not required
- Permanent monitoring and access to logs (24x7x365)
- Vulnerability Assessments (yearly at a minimum)
- Documentation of Network Changes

Power Utility Responsibilities	GE Vernova's Contribution
To monitor access to the ESP To perform the vulnerability assessments To document network changes	To disable all ports not used in the IED To monitor and record all access to the IED

18.4.1.5 CIP 006

CIP 006 states that Physical Security controls, providing perimeter monitoring and logging along with robust access controls, must be implemented and documented. All cyber assets used for Physical Security are considered critical and should be treated as such:

Power Utility Responsibilities	GE Vernova's Contribution
Provide physical security controls and perimeter monitoring Ensure that people who have access to critical cyber assets don’t have criminal records	GE Vernova cannot provide additional help with this aspect

18.4.1.6 CIP 007

CIP 007 covers the following points:

- Test procedures
- Ports and services
- Security patch management
- Antivirus
- Account management
- Monitoring

Power Utility Responsibilities	GE Vernova's Contribution
To provide an incident response team and have appropriate processes in place	Test procedures, we can provide advice and help on testing. Ports and services, our devices can disable unused ports and services Security patch management, we can provide assistance Antivirus, we can provide advise and assistance Account management, we can provide advice and assistance Monitoring, our equipment monitors and logs access

18.4.1.7 CIP 008

CIP 008 requires that an incident response plan be developed, including the definition of an incident response team, their responsibilities and associated procedures.

Power Utility Responsibilities	GE Vernova's Contribution
To provide an incident response team and have appropriate processes in place.	GE Vernova cannot provide additional help with this aspect.

18.4.1.8 CIP 009

CIP 009 states that a disaster recovery plan should be created and tested with annual drills.

Power Utility Responsibilities	GE Vernova's Contribution
To implement a recovery plan	To provide guidelines on recovery plans and backup/restore documentation

18.4.2 IEEE 1686-2013

IEEE 1686-2013 is an IEEE Standard for substation IEDs' cyber-security capabilities. It proposes practical and achievable mechanisms to achieve secure operations.

The following features described in this standard apply:

- Passwords are 8 characters long and can contain upper-case, lower-case, numeric and special characters.
- Passwords are never displayed or transmitted to a user.
- IED functions and features are assigned to different password levels. The assignment is fixed.
- The audit trail is recorded, listing events in the order in which they occur, held in a circular buffer.
- Records contain all defined fields from the standard and record all defined function event types where the function is supported.
- No password defeat mechanism exists. Instead a secure recovery password scheme is implemented.
- Unused ports (physical and logical) may be disabled.

18.5 CYBER-SECURITY IMPLEMENTATION

GE Vernova IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

MiCOM 5th Generation P40 products provide enhanced security through the following features:

- An Authentication, Authorization, Accounting (AAA) Remote Authentication Dial-In User Service (RADIUS) client that is managed centrally, enables user attribution, provides accounting of all user activities, and uses secure standards based on strong cryptography for authentication and credential protection. In other words, this option uses a RADIUS.
- Server for user authentication. There is provision for both remote (RADIUS) and local (device) authentication.
- A Role-Based Access Control (RBAC) system in line with IEC 62351-8:2020 that provides a permission model that allows access to the device operations and configurations based on specific roles and individual user accounts configured on the AAA server.
- Security event reporting through both proprietary security event log (separate from the main events file) and the Syslog and SNMP protocols for supporting Security Information Event Management (SIEM) systems for centralised cybersecurity monitoring.
- Encryption of passwords - stored within the IED, in network messages between the MiCOM S1 Agile software and the IED, and in network messages between the RADIUS server and the IED (subject to the RADIUS server configuration).
- Secure firmware upgrade process.

18.5.1 INITIAL SETUP: DEFAULT USERNAMES AND DEFAULT PASSWORDS

The requirements for initial setup of the IED for cyber-security and RBAC will depend on:

1. which interfaces, if any, the cyber-security is required,
2. the intended authentication method, as defined in the setting ***Auth. Method*** in *SECURITY CONFIG* column (see the Authentication Methods section).

When the authentication method is configured as `Device Only`, there are four pre-defined profiles.

User Name	Default Password	IEC 62351-8 Roles
ADMIN1	ChangeMe1#	SECADM
RBACMNT1	ChangeMe2#	RBACMNT
ENGG1	ChangeMe3#	ENGINEER
VIEWER1	ChangeMe4#	VIEWER

During the first logon, it is Mandatory to change the Default Passwords, and the IED or MiCOM S1 Agile software will prompt the user to change it. The new password must comply with the strength defined by the Password Policy setting, detailed in the ***Password Policy*** section of this chapter.

When the authentication method is configured as ‘Server + Device’, and authentication using RADIUS is required, users must be set up on the RADIUS server (see the RADIUS users section). These users are separate from the pre-defined Device users. RADIUS server information must be configured in the IED to connect to the RADIUS server(s) for Server authentication (see the RADIUS server settings section). It is recommended that the RADIUS shared secret be changed from the default (see the RADIUS client-server validation section).

18.6 ROLES AND PERMISSIONS

18.6.1 ROLES

The P40 Agile products supports all the mandatory pre-defined roles as per IEC 62351-8:2020.

IEC 62351-8 Roles	Value
VIEWER	0
OPERATOR	1
ENGINEER	2
INSTALLER	3
SECADM	4
SECAUD	5
RBACMNT	6

Individual user accounts can be configured to have one or more of these roles.

- VIEWER: Can view all values and settings
- OPERATOR: Can view values and perform control operations
- ENGINEER: Can view values, and change settings of the device
- INSTALLER: Specific role required to perform firmware updates
- SECADM: Security Administrator - Can edit/modify Users and roles and configure security settings
- SECAUD: Security Auditor - Can view Security Log files
- RBACMNT: RBAC Management can change role to permission assignment

Only one role of one type is allowed to be logged in at a time from any interface. For example, one Operator can be logged in but not a second Operator at the same time from any other interface. This prevents subsets of settings from being changed at the same time.

18.6.2 PERMISSIONS

Authentication and authorization are two different processes. An authenticated user cannot perform any action on the IED unless a privilege has been explicitly granted to them. This is the concept of “least privileges” access.

Privileges must be granted to users through roles. A role is a collection of privileges, and roles are granted to users. It is possible to have multiple roles for a user. The privilege/role matrix is stored on the IED. This is known as Role-Based-Access Control (RBAC).

On successful user authentication, the IED will load the user’s role list. If the user’s role changes, the user must logout and log back in to exercise his/her privileges.

The table below shows the predefined permissions assignment for the predefined Roles according to IEC 62351-8:2020

Value	Role Name (revision = 1)	Permission										
		LISTOBJECTS	READVALUES	DATASET	REPORTING	FILEREAD	FILEWRITE	FILEMNGT	CONTROL	CONFIG	SETTINGGROUP	SECURITY
<0>	VIEWER	C	C		X	C_1						

Value	Role Name (revision = 1)	Permission										
		LISTOBJECTS	READVALUES	DATASET	REPORTING	FILEREAD	FILEWRITE	FILEMNGT	CONTROL	CONFIG	SETTINGGROUP	SECURITY
<1>	OPERATOR	X	X		X	C_1			X		X	
<2>	ENGINEER	X	X	X	X	X_1	X_1	X_1		X	X	
<3>	INSTALLER	X	X		X	X_2	X_2			X	X	
<4>	SECADM	X	X	X		X_4	X_4	X_4		X		X
<5>	SECAUD	X	X		X	X_3						
<6>	RBACMNT	X	X		X			X_4		X		
<7 ...32767>	Reserved	For future use of IEC defined roles.										
<-32768 .. -1>	Private	Defined by external agreement. Not guaranteed to be inoperable.										

C = Conditional read access, clarification of specific data objects may be necessary (e.g., VIEWER may not access security settings, but process values)
C_1 = Conditional read access to files of filetype data
X_1 = Access to files of type data and config
X_2 = Access to files of type config and firmware (updates)
X_3 = Access to files of type audit log
X_4 = Access to files of type security (config)

The table below shows the predefined permissions description according to IEC 62351-8:2020

Permission	Description
LISTOBJECTS	Allows the subject/role to discover what objects are present within an IED by presenting the type and ID of those objects. If this permission is granted to a subject/role, the object for which the READVALUES permission has not been granted are not readable. This permission basically relates to all objects defined in IEC 61850 and allows a query on the existence of the data objects.
READVALUES	Allows the subject/role to obtain the values for all or some objects that are present within an IED in addition to the type and ID. This permission basically relates to all objects defined in IEC 61850 that provide a value and allows a read action on the actual values of the data objects.
DATASET	Allows the subject/role to have full service access (e.g., createDataSet, deleteDataSet) for both persistent and non-persistent DataSets.
REPORTING	Allows the subject/role to use buffered reporting as well as unbuffered reporting. Reporting relates to buffered and unbuffered report control blocks of a logical node.
FILEREAD	Allows the subject/role to perform read actions on file objects.
FILEWRITE	Allows the subject/role to perform write actions on file objects. This permission includes the FILEREAD permission.
CONTROL (group)	Allows the subject/role to perform control operations on all or some controllable objects that are present within an IED. Control services are for instance select or operate and relate to data objects defined in IEC 61850.
CONFIG	Allows the subject/role to locally or remotely configure all or some objects that are present within an IED. This relates to data attributes of the IEC 61850 functional constraints CF, DC and SP.
SETTINGGROUP	Allows the subject/role to remotely configure SettingGroup control block. For example, this relates to the switching between different configured SettingGroups. SettingGroups also contains the IEC 61850 functional constraints SE.
FILEMNGT	Allows the subject/role to delete existing files on the IEDS.
SECURITY	Allows the subject/role to perform actions on all security related data objects, reportings, logs or files.

Specific product related permissions are listed in the tables below. Roles are mapped to Access Level definitions: A cross indicates that specific actions can be done by a user with the role allocated.

Extract Files	Role Name							
File Type	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Setting				X	X	X	X	X
PSL				X	X			
MCL (IEC 61850)				X	X			
DNP3				X	X			
SLD				X	X			
Events (operational)		X	X	X				
Security Events							X	
Disturbance Records		X	X	X				

Sending Files	Role Name							
File Type	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Setting				X	X	X		
PSL				X	X			
MCL (IEC 61850)				X	X			
DNP3				X	X			
SLD				X	X			
Menu Text				X	X			

18.7 USER AUTHENTICATION

18.7.1 AUTHENTICATION METHODS

The IED supports Bypass (no authentication), Device authentication and Server authentication.

Authentication Method	Description	User Interface
Bypass Auth.	IED does not provide security, any user (Local) can access the IED without logging in. IED does not validate user and password. In this case, there is no need to enter user name and password to login. Bypass can not be enabled on Rear Port 1, Rear Port 2 and Ethernet Ports.	Front Panel UI Front Port (USB port) (Local interfaces only)
Device Only	IED allows role access using local authentication.	Front Panel UI Front Port (USB port) Rear Port 1 Rear Port 2 Network Port 1 Network Port 2
Server + Device	IED uses RADIUS server authentication to validate the user first. And it allows fallback to device authentication if the RADIUS server(s) are unavailable.	Front Panel UI Front Port (USB port) Rear Port 1 Rear Port 2 Network Port 1 Network Port 2

If ***Bypass Auth.*** is enabled, the IED ignores the ***Auth. Method*** setting.

The ***Auth. Method*** setting offers the following options for user authentication:

- *Server + Device* (This is the default setting for IEDs with NIC (Ethernet Board) fitted)
- *Device Only* (This is the default setting for IEDs without NIC (Ethernet Board) fitted)

Only users with a SECADM role may change the ***Auth. Method*** setting. If the SECADM user changes it, the role remains logged in. Only when the user logs-out is their access-level revoked.

18.7.2 BYPASS

In ***Bypass Auth.*** mode, the IED does not provide user authentication - any user can login. IED does not validate user and password. The bypass security feature provides an easier access, with no authentication and encryption for situations when this is considered safe. Only users with SECADM role can enable Bypass mode.

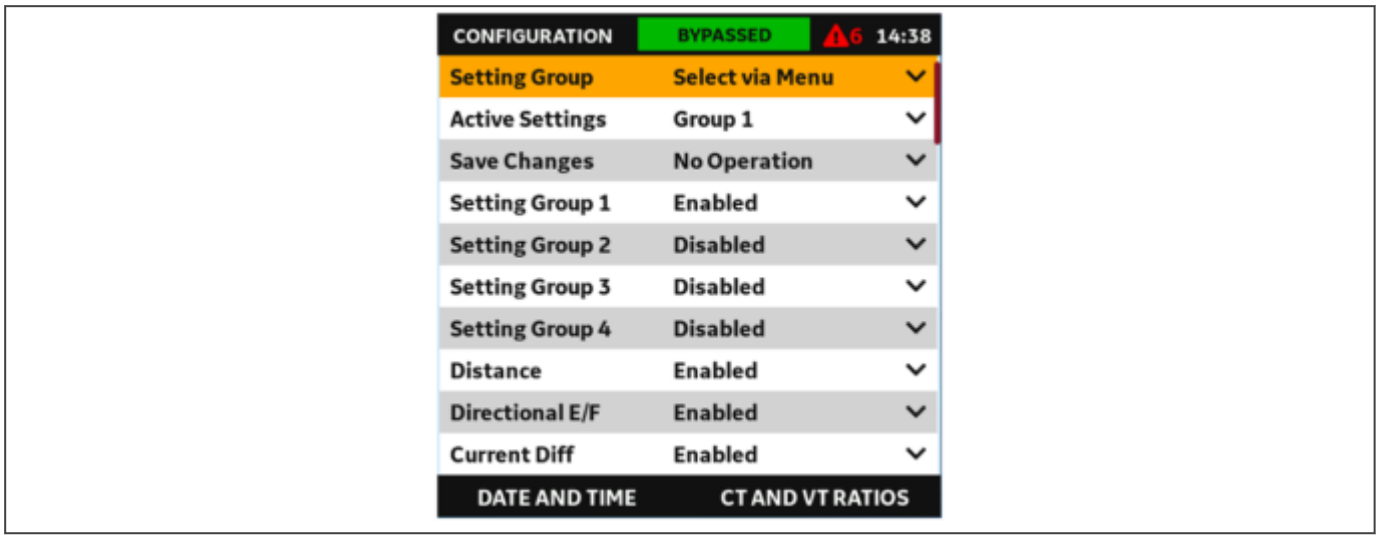
There are three modes for authentication bypass:

1. *Disabled* - no interfaces in ***Bypass Auth.*** mode (normal authentication is active)
2. *Local* - Bypass authentication when using Front Port and Front Panel
3. *Front Panel* - will bypass authentication Front Panel User Interface

Bypass authentication for Bypass mode:	Front Port	Front Panel UI
Disabled		
Local	X	X
Front Panel		X

The DDB signal ***Security Bypass*** is available to indicate that the IED is in ***Bypass Auth.*** mode.

The Front Panel UI will display "BYPASSED" at the top of the screen to indicate that the IED is in ***Bypass Auth***. mode.



18.7.3 LOGIN

A user can only login through the following methods:

- Front Panel User Interface
- Using MiCOM S1 Agile, connected to either the Front Port, Rear Port 1 or 2, or Ethernet Network Port 1 or 2.

18.7.3.1 FRONT PANEL LOGIN

Front panel User Interface supports both Device authentication and Server authentication. The P40 gives the user the option to enter the user credentials via UI panel. To access the Login window, select the Login text in the top banner using the arrow keys.

R80008

For both Device authentication or Server authentication, the user can enter any valid username and password combination. For ease of typing, it is preferable to do login using MiCOM S1 Agile.

After successful log in, a confirmation message is displayed, showing the logged in username at the top of the screen. For example:

R80010

18.7.3.2 LOGIN FAILED

When Authentication fails, a failure message is displayed:

18.7.3.3 OTHER LOGIN PROMPTS

For cases where the bypass is disabled and the user attempts an action which requires a user login, the Login Window appears after the error message. This is applicable while changing any setting values or pressing buttons which require user management - the Function Key, for example.

18.7.3.4 MICOM S1 LOGIN

When the user attempts to login, MiCOM S1 Agile will prompt the user with a login dialog box that contains a username and password entry fields. For both Device authentication or Server authentication, the user can enter any valid combination of username and password.

18.7.3.4.1 WARNING BANNER

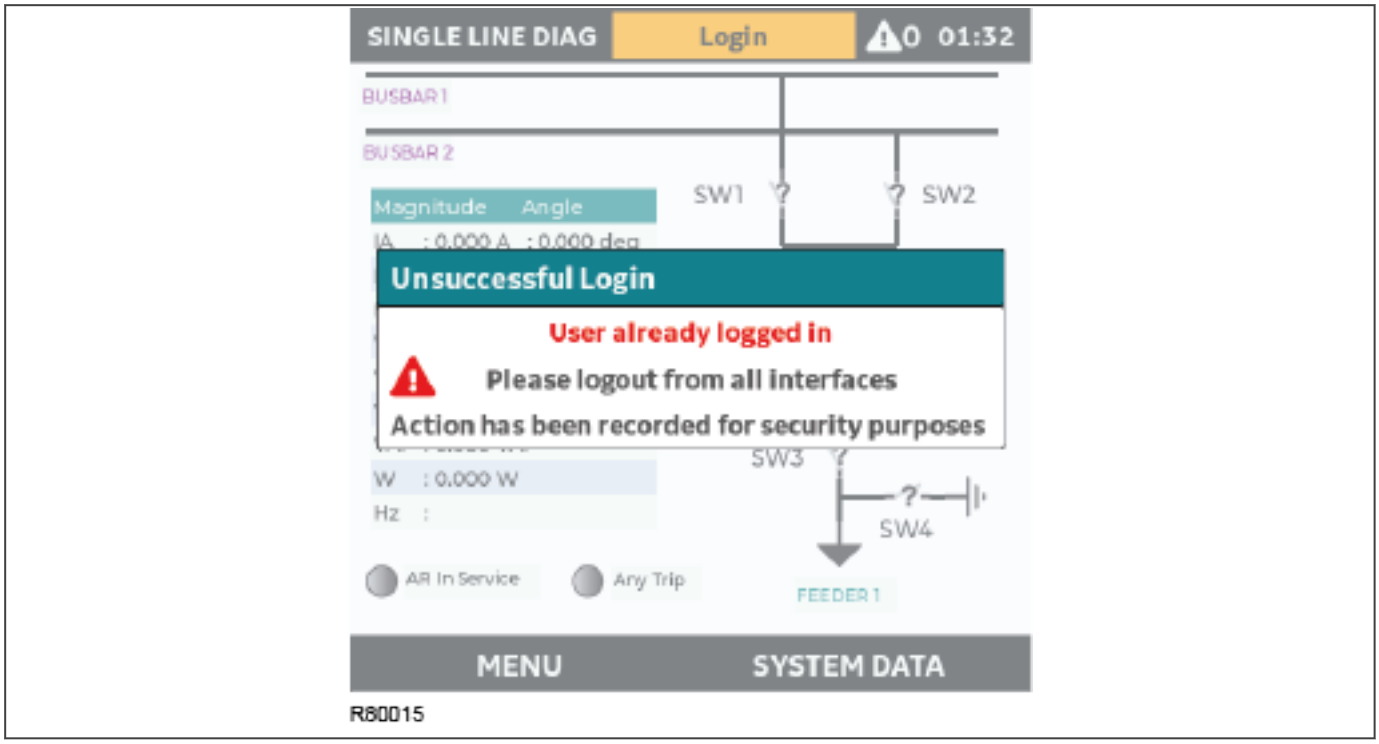
After successful authentication and authorisation to access the IED, MiCOM S1 Agile will display a security warning banner to the user.

If **I Agree** is selected, the integrated authentication and authorisation is completed. Selecting **I Disagree** causes the program to close and the login user to logout.

For S1 Agile authentication, this is a pop-up dialog that the user must click to acknowledge.

18.7.4 USER SESSIONS

Only one role of one type is allowed to be logged in at a time from any interface. If the role has been logged in from one interface, an attempt to login the same role will result in a message being displayed, as below.



Open sessions will be automatically closed by the IED after a configurable session timeout.

The inactivity timer configuration setting defines the period of time that the IED waits in idleness before a logged in user is automatically logged out.

If there is any data change that does not commit to IED, the data change is discarded when user logged out. If there is any access that does not finish, the access will fail when user logged out. Front panel will display the default page when user reaches the defined inactivity time.

If the keypad is inactive for configured UI inactivity timer, the user logout message is displayed and the front panel user interface reverts to the Viewer access level.

The following settings are available in the ***SECURITY CONFIG*** column to support configurable inactivity timers.

- ***FP InactivTimer***
- ***UI InactivTimer***
- ***NIC Tunl Timeout***

Setting Name	Description	Min	Max	Default	Units	User Role Required
Attempts Limit	Number of failed authentications before the device blocks subsequent authentication attempts for the lockout period. A value of 0 means Lockout is disabled.	0 (lockout disabled)	99	3	-	SECADM
Lockout Period	The period of time in seconds a user is prevented from logging in, after being locked out.	1	5940	30	sec	SECADM
FP InactivTimer	FP Inactivity Timer is the time of idleness on Front Port before a logged in user is automatically logged out and revert the access level to the viewer role	0 (no Inactivity Timeout)	30	10	min	SECADM
UI InactivTimer	UI Inactivity Timer is the time of idleness on Front Panel before a logged in user is automatically logged out and revert the access level to the viewer role	0 (no Inactivity Timeout)	30	10	min	SECADM

Setting Name	Description	Min	Max	Default	Units	User Role Required
NIC Tunl Timeout	NIC Tunl Timeout is the time of idleness on Ethernet Port (NIC) before a logged in user is automatically logged out and revert the access level to the viewer role	1	30	5	min	SECADM

The recommended settings for ***Attempts Limit*** is *3* and ***Lockout Period*** is *30 sec* to discourage brute force attacks. If the Lockout period is too large, anybody can lockout Device users.

The following settings are available in the *COMMUNICATIONS* column to configure the inactivity timers for rear serial ports:

- ***KBUS InactTmr*** for RP1, if Courier Protocol is selected
- ***RP2 InactivTimer*** for RP2

18.7.5 USER LOCKING POLICY

A local user locking policy is implemented for Device access:

- This user locking policy applies to both Device users.
- The account is unlocked at the first successful login after the ***Lockout Period***
- If the user consecutively fails to login at the configured number of ***Attempts Limit***, the user account will be locked for the configured ***Lockout Period***

Each user account records how long it has been locked if the account is locked.

Each user account records how many times it has consecutively failed to login. User account failed times include all interfaces login attempts. For example, if the ***Attempts Limit*** setting is *3* and the operator failed to login from front panel 2 times, and they changed to login from the Courier interface, but failed again, then the Operator would be locked out.

When the IED is powered on, these ***Attempts Limit*** counter resets to zero.

When the user account exceeds the ***Attempts Limit*** it is locked for ***Lockout period***, at that time ***Attempt limit*** resets to zero.

The locked user account will be unlocked automatically, after the configured “Lockout Period” is expired.

If the locked account attempts to login the IED from the Front Panel, the unsuccessful login attempt screen is displayed.

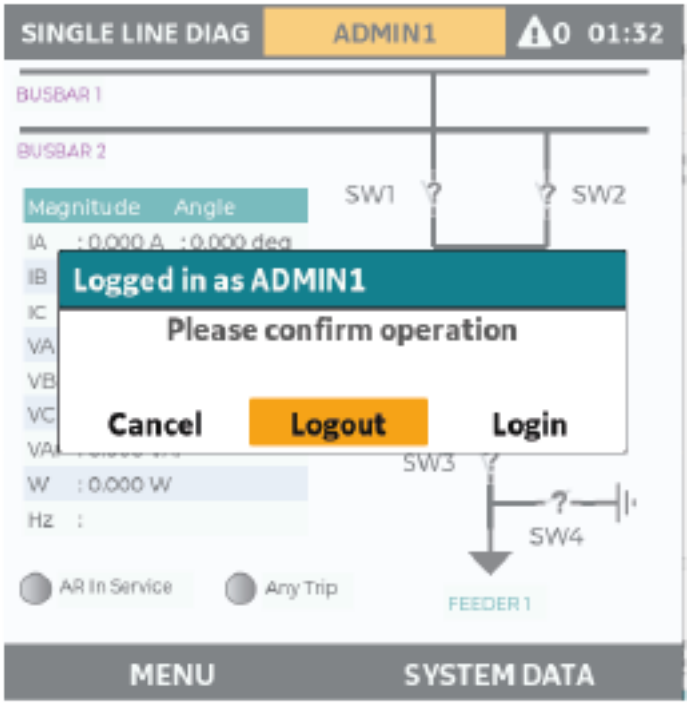
18.7.6 LOGOUT

Each user should ***Log out*** after reading or configuring the IED.

The user can only log out from the front panel, if they logged in from the front panel. If the user logged in from S1 Agile, they have to logout from S1 Agile.

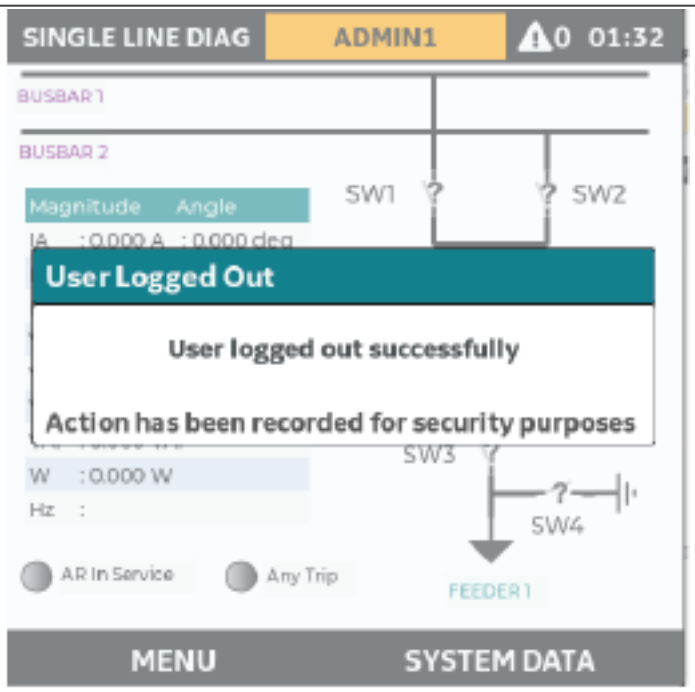
18.7.6.1 FRONT PANEL LOGOUT

Go to the top of the banner and select the current logged in User. You may be prompted to log out with the following display:



R80013

If you confirm, the following screen is displayed for 2 seconds and then the action will be recorded in the security events file:



R80014

If you decide not to log out (i.e. you cancel), the logout screen would be cancelled.

18.7.6.2 MICOM S1 LOGOUT

Right-click on the device name in the System Explorer panel in MiCOM S1 Agile and select Log Off.

In the Log Off confirmation dialog, click Yes. The action will be recorded in the security events file.

18.7.7 PASSWORD POLICY

Cyber-security requires strong passwords and validation for NERC compliance. The IED will enforce one of two levels of password strength according to the ***Password Policy*** setting.

The NERC password complexity policy requires an alpha-numeric password (for all accesses, front panel, and network/local port) that meets the following **mandatory** requirements:

1. Passwords cannot contain the user's account name or parts of the user's full name that exceed two consecutive characters.
2. Passwords must be at least eight characters in length, but not exceed 16 characters in length.

Strict passwords rules must contain characters from all four categories as shown below:

a. English uppercase characters (A through Z).
b. English lowercase characters (a through z).
c. Numeric (digits 0 through 9).
d. Special non-alphanumeric characters (such as @,!,#,{, but not limited to only those)

Normal password rules: Any 3 out of 4 conditions as in strict password rules.

For Device authentication, the IED will enforce that configured passwords meet these requirements. The user can select which policies are required by selecting either Strict or Normal in the Password Policy setting under DEVICE RBAC.

Setting Name	Description	Min	Max	Default	Units	User Role Required
Password Policy	Selection of whether strict or normal rules apply for device authentication password policy	Normal	Strict	Strict	-	SECADM

For Server authentication, the password complexity and user locking policy is defined in the external RADIUS server.

18.7.8 PASSWORD EXPIRY

For Device authentication users, it is possible to select a configurable time (in days) for the password to be changed by the user.

Under *DEVICE RBAC* Settings, select ***Password Expiry*** to be Enabled. The setting of ***Disabled*** disables the password expiry check by the IED. If enabled, Max Password Age can be selected, this is in the range of days.

Setting Name	Description	Min	Max	Default	Units	User Role Required
Password Expiry	Selection of whether Password Expiry is enforced by the IED for device authentication	Disabled	Enabled	Enabled	-	SECADM
Max Password Age	Period in days if Password Expiry is enabled, the device passwords need to be changed	30	730	180	days	SECADM

When the Max Password Age has been reached and if the user attempts to login using the front panel UI, the following window will be shown.

R80011

The user will be presented with a screen to save the new password.

R80012

18.7.9 CHANGE PASSWORD

All the Device users will need to change the default password at the first logon.

The initial password change can be done either from the front panel User Interface, or from MiCOM S1 Agile using the **Change/Set Password** option in the **Supervise Device** dialog box.

Any further password change can only be done from MiCOM S1 Agile using the **Change/Set Password** option in the **Supervise Device** dialog box.

Users with SECADM and RBACMNT roles can change the password of any user. Users with other roles can change only their own password.

Caution:
It is recommended that user passwords are changed periodically.

18.7.10 RADIUS AUTHENTICATION

When the ***Auth. Method*** setting is configured as *Server + Device*, a user must log in with a username and password that has been predefined on the RADIUS server.

This log in can be performed from any interface, as described in the Login section. The IED will authenticate the user to the active RADIUS server, over the Ethernet connection.

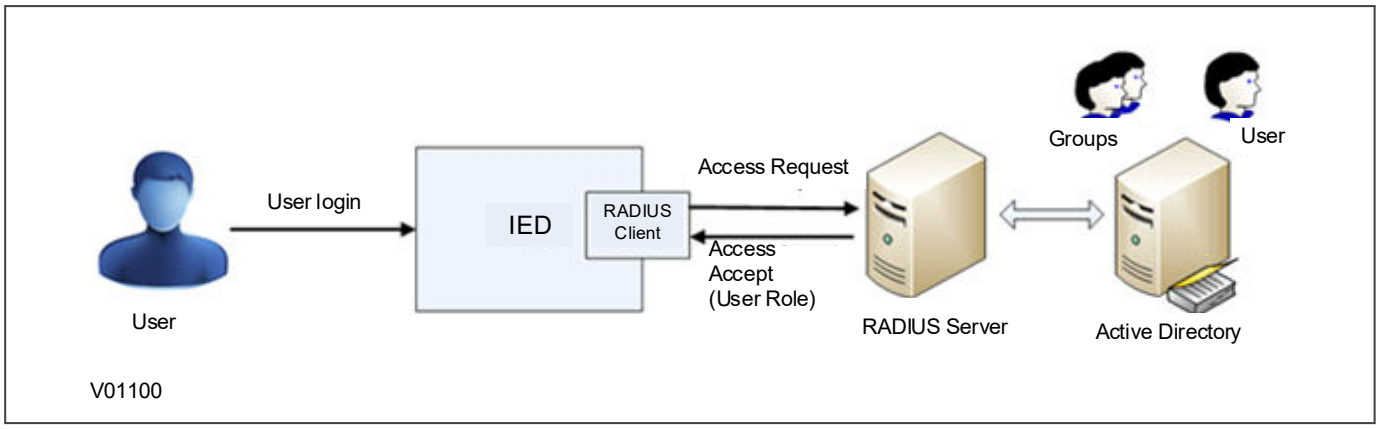


Figure 243: RADIUS server/client communication

18.7.10.1 RADIUS USERS

For Server authentication, RADIUS users and passwords are created in the RADIUS server (in the Active Directory), not in the IED.

The username must be from the ASCII Subset of 32 to 122 which includes upper and lower case letters, digits and several special characters.

Each RADIUS user must have a password that meets the password policy of the Active Directory (not the password policy of the P40) and have one of the supported roles assigned in the Active Directory.

The number of RADIUS users is not limited by the IED.

RADIUS password changes are done in the Active Directory (after password expiration).

18.7.10.2 RADIUS CLIENT

Two RADIUS servers are supported by the IED in the configuration for redundancy. The IED will try each in sequence until one responds.

The IED will first try server 1 up to the configured number of retries, leaving a request timeout between each request. If, after this point there is still no valid answer from server 1, the IED will switch to server 2 and repeat for up to the configured number of retries.

If the number of retries for the second server is exceeded the IED will fallback to Device authentication. A **RADIUS Server unavailable** security event is also logged under this condition.

The RADIUS implementation supports the following authentication protocols:

- EAP-TTLS-MSCHAP2
- PAP
- EAP-PEAP-MSCHAP2
- PAP EAP-TTLS-PAP (Default)

The RADIUS implementation queries the Role ID vendor attribute and establish the logged in user security context with that role.

RADIUS Config.	Value
Vendor ID	2910
Vendor Attribute	1
Standard Values	
VIEWER	0
OPERATOR	1
ENGINEER	2
INSTALLER	3
SECADM	4
SECAUD	5
RBACMNT	6

18.7.10.3 RADIUS SERVER SETTINGS

The following RADIUS server information must be configured in the IED to connect to the RADIUS server(s) for Server authentication.

Setting Name	Description	Min	Max	Default	Units	User Role Required
RADIUS Pri IP	IP address of Server 1. Default value indicates no Primary RADIUS server is configured, and so RADIUS is disabled.	0.0.0.0	255.255.255.255	0.0.0.0	-	SECADM
RADIUS Sec IP	IP address of Server 2. Default value indicates no Secondary RADIUS server is configured	0.0.0.0	255.255.255.255	0.0.0.0	-	SECADM
RADIUS Auth Port	RADIUS authentication port	1	65535	1812	-	SECADM
RADIUS Security	Authentication protocol to be used by RADIUS server	EAP-TTLS-MSCHAP2 PAP EAP-PEAP-MSCHAP2 PAP EAP-TTLS-PAP		PAP EAP-TTLS-PAP	-	SECADM
RADIUS Timeout	Timeout in seconds between re-transmission requests	1	900	2	sec	SECADM
RADIUS Retries	Number of retries before giving up	1	99	10	-	SECADM
RADIUS Secret	Shared Secret used in authentication. It is only displayed as asterisks.	1 character	64 characters	ChangeMe1#	-	SECADM

Setting Name	Description	Min	Max	Default	Units	User Role Required
RADIUS NAS ID	NAS-Identifier for RADIUS	1 character	20 characters	MiCOM P40	-	SECADM

The data cell ***RADIUS Status*** indicates the status of the currently-selected RADIUS server. This will display either `Disabled`, `Server OK`, or `Failed`.

18.7.10.4 RADIUS ACCOUNTING

RADIUS accounting is not supported by the IED. The user can achieve accounting through syslog (see the SYSLOG section).

18.7.10.5 RADIUS CLIENT-SERVER VALIDATION

Client-server validation is achieved using a shared secret. The IED must be configured with the ***RADIUS Secret*** setting to match the shared secret configured in the RADIUS server. It is recommended (but not enforced) that this setting meets the P40 password requirements. The device supports RADIUS secret of 1-64 characters.

MiCOM S1 Agile provides an option to save ***RADIUS Secret*** to the device. This can be achieved by logging to the device with a SECADM profile and accessing Supervise Device -> ***RADIUS Secret***.

Note:
It is recommended that the shared secret be changed from the default before using RADIUS authentication.

The IED does not support exchange of CA certificates. The RADIUS server may send a certificate but the IED will not verify it.

18.7.11 RECOVERY

18.7.11.1 RESTORE TO LOCAL FACTORY DEFAULT

The ***Restore Defaults*** setting is available to facilitate NERC CIP compliance requirements for decommissioning critical cyber devices. Only the **Administrator** role can change this setting.

The ***Restore Defaults*** setting under the *CONFIGURATION* column is used to restore a setting group to factory default settings.

0 = `No Operation`

1 = `All Settings`

2 = `Setting Group 1`

3 = `Setting Group 2`

4 = `Setting Group 3`

5 = `Setting Group 4`

To restore the default values to the settings in any setting group, set the ***Restore Defaults*** setting to the relevant Group number. Alternatively, it is possible to set the ***Restore Defaults*** setting to `All Settings` to restore the default values to all the IEDs settings, not only one setting group.

Note:
Restoring defaults to all settings includes the rear communication port settings, which may result in communication via the rear port being disrupted if the new (default) settings do not match those of the master station.

Data (events, DR, fault records, protection counters etc) is left untouched. When decommissioning critical cyber IEDs, users may want to clear all data and events as well.

18.7.11.2 PASSWORD RESET PROCEDURE

If you mislay a devices password (if Administrator forgets their password), the passwords can be reset to default using a recovery password. To obtain the recovery password you must contact the Contact Centre and supply the Serial Number and the security code. The Contact Centre will use these items to generate a Recovery Password.

The security code is a 16-character string of uppercase characters. It is a read-only parameter. The device generates its own security code randomly. A new code is generated under the following conditions:

- On power up
- Whenever settings are set back to default
- On expiry of validity timer (see below)
- When the recovery password is entered

This reset procedure can be only accomplished through front panel exclusively and cannot be done over any other interface. As soon as the security code is displayed on the front panel User Interface, a validity timer is started. This validity timer is set to 72 hours and is not configurable. This provides enough time for the Contact Centre to manually generate and send a recovery password. The Service Level Agreement (SLA) for recovery password generation is one working day, so 72 hours is sufficient time, even allowing for closure of the Contact Centre over weekends and bank holidays.

The procedure is:

The security code is displayed on confirmation. The validity timer is then started. The security code can only be read from the front panel.

This reset procedure can be only accomplished through front panel exclusively and cannot be done over the Ethernet/serial port, but only when physically present in front of the IED. In the event of losing all passwords (if the Administrator forgets their password) the user could reset the IED to default passwords, following the procedure below:

1. User navigates to ***Security Code*** cell in *SECURITY CONFIG* column
2. To prevent accidental reading of the IED ***Security Code***, the cell will initially display a warning message:

```
PRESS ENTER TO
READ SEC. CODE
```

3. Press Enter to read the ***Security Code***.
4. User sends an email to the Contact Centre providing the full IED serial number and displayed ***Security Code***, using a recognisable corporate email account
5. Contact Centre emails the user with the Recovery Password. The recovery password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once – for password recovery.
6. User logs in with the username **ADMINISTRATOR** and the recovery password in to the ***Password*** setting in *SYSTEM DATA* column.
7. Then IED will prompt

```
RESET PASSWORD?
ENTER or CLEAR
```

8. Press Enter to continue the reset procedure
9. If the recovery password successfully validates, the default passwords are restored for each access level for Device authentication.
10. Change ***Auth. Method*** setting to `Server + Device` if applicable.

Note:
Restoring passwords to defaults does not affect any other settings and does not provoke reboot of the IED. The protection and control functions of the IED are always maintained.

18.7.11.3 ACCESS LEVEL DDBS

The current level of access for each interface is available for use in the Programmable Scheme Logic (PSL) as these DDB signals:

- ***HMI Access Lvl 1***
- ***HMI Access Lvl 2***
- ***FPort AccessLvl1***
- ***FPort AccessLvl2***
- ***RPrt1 AccessLvl1***
- ***RPrt1 AccessLvl2***
- ***RPrt2 AccessLvl1***
- ***RPrt2 AccessLvl2***

Each pair of DDB signals indicates the access level as follows:

- Level 1 off, Level 2 off = 0
- Level 1 on, Level 2 off = 1
- Level 1 off, Level 2 on = 2
- Level 1 on, Level 2 on = 3

KEY:

HMI = Human Machine Interface

(Front Panel User Interface)

FPort = Front Port

RPrt = Rear Port

Lvl = Level

18.7.12 PORT HARDENING: PHYSICAL PORTS

It is possible to disable unused physical ports. Enabling/Disabling of physical ports can be done either via the Front Panel or by sending the modified settings to the IED. These settings are under the PORT HARDENING: PHYSICAL PORTS Section of SECURITY CONFIG column. A user with SECADM role is needed to perform this action. This action cannot be done via the Supervise Device dialog box using MiCOM S1 Agile.

The following ports can be disabled, depending on the model.

- Front Port (***Front Port*** setting)
- Rear Port 1 (***Rear Port 1*** setting)
- Rear Port 2 (***Rear Port 2*** setting)
- Ethernet Network Port 1 (***Network Port 1*** Setting)
- Ethernet Network Port 2 (***Network Port 2*** Setting)

18.7.13 PORT HARDENING: LOGICAL PORTS (PROTOCOLS)

It is possible to disable unused logical ports. Enabling/Disabling of logical ports can be done either via the Front Panel or via sending the modified settings to the IED. These settings are under the PORT HARDENING: LOGICAL PORTS Section of the SECURITY CONFIG column. A user with SECADM role is needed to perform this action, This action cannot be done via the Supervise Device dialog box using MiCOM S1 Agile.

The following NIC protocols can be disabled:

- Courier Tunnel (for S1 Agile remote connection over Ethernet)
- IEC 61850
- SNTP
- PTP
- SNMP
- RADIUS
- SYSLOG

18.7.14 SERVICE (PROTOCOL) MAPPING: ETHERNET NETWORK PORTS 1 AND 2

This section details which of the Ethernet protocols are available on each of Network Port 1 and Network Port 2, and whether these are configurable or fixed mappings. Settings for the configurable service mappings are under the PORT HARDENING: SERVICE MAP section of the *SECURITY CONFIG* column.

Service	Network Port 1	Network Port 2	Fixed/Configurable	Setting
IEC 61850	No	Yes	Fixed to NP2.	
SNTP	No	Yes	Fixed to NP2.	
PTP	No	Yes	Fixed to NP2.	
SSH (for S1 Agile)	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	Courier Tunnel
SNMP	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	SNMP
RADIUS	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	RADIUS
Syslog	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	SYSLOG

18.7.15 SUPERVISE DEVICE DIALOG BOX

Supervise Device	Role Name							
	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Active Group			X	X	X			
Reset Cell			X					
Breakers			X					
Device Address				X	X	X		
Date and Time			X	X	X			
Bypass Options						X		

Supervise Device	Role Name							
	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Active MCL Bank				X	X			
Device User Management						X		X
Own Password Change		X	X	X	X	X	X	X
RADIUS Secret						X		
SNMP Security						X		
Clear Records				X				
Restore Defaults				X	X			
Restore Security Settings						X		
SSH Client Passcode						X		

18.7.16 SECURE FIRMWARE UPGRADE

IEC 62351-8:2020 has defined a specific INSTALLER Role which can do firmware upgrades on the IEDs. The default users in the Device Authentication does not have any users with the INSTALLER Role. If a requirement exists to upgrade the Firmware of the IED, then the following mandatory steps must be taken before starting the firmware update:

- Using MiCOM S1 Agile, create a new user having the INSTALLER Role
- Using MiCOM S1 Agile, log into the device using the user having the INSTALLER Role. Change the default password
- Use the Firmware Download Tool and log into the IED, using the newly created user and changed password
- Once these steps are done, the firmware update process can continue.

The device supports Secure Firmware Update. The firmware files are checked for validity prior to updating of the IED. The main steps in the secure firmware update process are as follows:

- The ‘PX40 Download and Calibration’ firmware tool opens the secure firmware ZIP file and extracts its contents [Compressed Images and Signatures].
- The ‘PX40 Download and Calibration’ firmware tool transfers the firmware files [Compressed Images and Signatures] to IED Main CPU Board.
- IED validates the Compressed Images and extracts them.
- After successful validation, only then will the settings be cleared.
- In case of validation failure, IED will display the ERROR CODE and after that, the user can reboot the relay to its previous state.
- IED updates it Main CPU Board, Co-processor Board and Ethernet Board storage and verifies it.
- Finally, the Main CPU Board initiates an IED reboot.

Key steps in this process will be logged in the security events - see the Security Event Management section of this chapter for further details.

Any firmware upgrade should be organised through the GE Vernova Grid Automation After Sales Service departments, or a regional Local Service Centre. The firmware upgrade should normally be performed by GE Vernova personnel, or by suitably prepared and competent persons after instruction from GE Vernova personnel. A separate MiCOM P40 firmware download procedure guide is available.

Note:
It is not possible to update the firmware on the IED which is under Bypass mode.

Note:
During the firmware update, only the security events file is retained - all other configuration and record files are erased during a firmware upgrade.

18.8 SNMP CONFIGURATION

You configure the SNMP interface using the HMI panel or using the SNMP Security option in the Supervise Device dialog box by a user with SECADM role. Two different versions are available; SNMPv2c and SNMPv3:

To enable the SNMP interface:

1. Select the SECURITY CONFIG column and scroll to the SNMP PARAMETERS heading
2. You can select either v2C, V3 or both. Selecting None will disable the main processor SNMP interface.

SNMP Trap Configuration

SNMP traps allow for unsolicited reporting between the IED and up to two SNMP managers with unique IP addresses. The device MIB details what information can be reported using Traps. To configure the SNMP Traps:

1. Move down to the cell ***Trap Dest. IP 1*** and enter the IP address of the first destination SNMP manager. Setting this cell to `0.0.0.0` disables the first Trap interface.
2. Move down to the cell ***Trap Dest. IP 2*** and enter the IP address of the second destination SNMP manager. Setting this cell to `0.0.0.0` disables the Second Trap interface.

SNMP V3 Security Configuration

SNMPv3 provides a higher level of security via authentication and privacy protocols. The IED adopts a secure SNMPv3 implementation with a user-based security model (USM).

Authentication is used to check the identity of users, privacy allows for encryption of SNMP messages. Both are optional, however you must enable authentication in order to enable privacy. To configure these security options:

1. If SNMPv3 has been enabled, set the ***Security Level*** setting. There are three levels; without authentication and without privacy (`noAuthNoPriv`), with authentication but without privacy (`authNoPriv`), and with authentication and with privacy (`authPriv`).
2. If Authentication is enabled, use the ***Auth Protocol*** setting to select the authentication type. There are two options: `HMAC-MD5-96` or `HMAC-SHA-96`.
3. Using the ***Auth Password*** setting, enter the password (up to 20 characters) to be used by the IED for authentication.
4. Using the ***Auth Protocol*** setting, select one of the two available mechanisms for encryption of messages to be used by the IED (CBC-DES or CFB-AES128).
5. If privacy is enabled, use the ***Encrypt Password*** setting to set the encryption password (up to 20 characters) that will be used by the IED for encryption.

> *Note:*
> *When setting the SNMP browser for RBAC compatible relays, the Context Name should be 'px4x'.*

SNMP V2C Security Configuration

SNMPv2c implements authentication between the master and agent using a parameter called the ***Community Name***. This is effectively the password but it is not encrypted during transmission (this makes it inappropriate for some scenarios in which case version 3 should be used instead). To configure the SNMP 2c security:

1. If SNMPv2c has been enabled, use the ***Community Name*** setting to set the password that will be used by the IED and SNMP manager for authentication. This may be between one and 8 characters.

18.9 RETURNING THE IED TO FACTORY

MiCOM P40 5th Generation products provide enhanced security, and there is no mechanism to bypass the implemented user management. In the event that the IED is returned to the factory for repair or technical analysis, to facilitate the Engineers gaining access to the configuration and stored records in the IED, it is proposed that the IED is returned to the factory with one of the following options:

- Bypass enabled on the front port
- A new user with all Roles is created and left with a default password. If the details of this user are passed to the factory, the IED can be logged in after changing the default password. If the newly created user's password has been modified, it will be required that the modified password is provided

18.10 SECURITY EVENT MANAGEMENT

To implement NERC-compliant cyber-security, a range of security events are logged by the IED in three separate methods:

- In the Security Events file (security audit log) - a Courier events file that can be extracted and viewed by MiCOM S1 Agile
- As syslog events
- As SNMP events (traps)

18.10.1 SECURITY EVENTS: COURIER

The P40 supports the IEC 62351-14 format of security event messages. These are logged into a separate security audio log file named "Security events" that can be extracted and viewed by MiCOM S1 Agile, in addition to the operational events file. The maximum number of security events is 2048.

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
SECUR_EVT_PW_SET_NON_COMPLIANT	62443-AUDIT_LOG	Info	USER_PW_CHANGE_FAIL_POLICY	IEC 62351-14:1.31	User Password change failed - policy check failed	
SECUR_EVT_PW_MODIFIED	62443-CONFIG_CHANGE	Notice	USER_PW_CHANGE_OK	IEC 62351-14:1.25	User password changed successfully	Interface
SECUR_EVT_PW_ENTRY_NOW_BLOCKED	62443-ACCESS_CONTROL	Notice	LOCK_USER_WRONG_CR	IEC 62351-14:1.7	User locked - Wrong credentials	Interface
SECUR_EVT_PW_ENTRY_UNBLOCKED	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-001	User unlocked	Interface
SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-002	Log-in attempt when user is locked	Interface
SECUR_EVT_INVALID_PW_ENTERED	62443-ACCESS_CONTROL	Notice	LOGIN_FAIL_WRONG_ CR	IEC 62351-14:1.3	Log-in failed - Wrong credentials	Interface
SECUR_EVT_PW_TIMED_OUT	62443-ACCESS_CONTROL	error	LOGIN_FAIL_CRED_EXPIRE	IEC 62351-14:1.4	Log-in failed - credentials expired.	Interface
SECUR_EVT_RECOVERY_PW_ENTERED	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-004	Recovery password entered	Interface
SECUR_EVT_IED_SEC_CODE_READ	62443-AUDIT_LOG	Info	-	2910-MiCP40-005	Security Code read	Interface
SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	62443-AUDIT_LOG	Info	-	2910-MiCP40-006	Security Code Timer expired	Interface
SECUR_EVT_PORT_DISABLED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-007	Port Disabled	Interface
SECUR_EVT_PORT_ENABLED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-008	Port Enabled	Interface, Port number

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
SECUR_EVT_PSL_ SETTINGS_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-009	PSL Settings downloaded to device	Interface, Port number
SECUR_EVT_DNP_ SETTINGS_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-010	DNP Settings downloaded to device	Interface, Group number
SECUR_EVT_TRACE_ DATA_DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-011	TRACE Data downloaded to device	Interface
SECUR_EVT_61850_ CONFIG_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-012	IEC61850 Config downloaded to device	Interface
SECUR_EVT_USER_ CURVES_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-013	User Curves downloaded to device	Interface
SECUR_EVT_SETTING_GRP_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-014	Setting Group downloaded to device	Interface, Curve number
SECUR_EVT_DR_ SETTINGS_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-015	DR Settings downloaded to device	Interface, Group number
SECUR_EVT_PSL_ SETTINGS_ UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-016	PSL Settings uploaded from device	Interface
SECUR_EVT_DNP_ SETTINGS_ UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-017	DNP Settings uploaded from device	Interface, Group number
SECUR_EVT_TRACE_ DATA_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-018	TRACE Data uploaded from device	Interface
SECUR_EVT_61850_ CONFIG_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-019	IEC61850 Config uploaded from device	Interface
SECUR_EVT_USER_ CURVES_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-020	User Curves uploaded from device	Interface
SECUR_EVT_PSL_ CONFIG_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-021	PSL Config uploaded from device	Interface, Curve number
SECUR_EVT_ SETTINGS_ UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-022	Settings uploaded from device	Interface, Group number
SECUR_EVT_CS_ SETTINGS_CHANGED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-023	Control & Support settings changed	Interface
SECUR_EVT_DR_ SETTINGS_CHANGED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-024	Disturbance Record Settings changed	Interface
SECUR_EVT_ SETTING_GROUP_ CHANGED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-025	Setting Group changed	Interface

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
SECUR_EVT_ DEFAULT_SETTINGS_ RESTORED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-026	Default Settings restored	Interface, Group number
SECUR_EVT_ DEFAULT_USRCURVE_ RESTORED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-027	Default User Curve restored	Interface
SECUR_EVT_POWER_ON	62443-CONTROL_SYSTEM	Notice	-	2910-MiCP40-028	Device Powered On	Interface, Curve number
SECUR_EVT_RADIUS_UNAVAIL	62443-AUDIT_LOG	warning	RBAC_NO_RADIUS	IEC 62351-8:1.3	RADIUS server not available	Interface
SECUR_EVT_ SESSION_LIMIT	62443-AUDIT_LOG	Notice	-	2910-MiCP40-030	Active user sessions limit reached	Interface
SECUR_EVT_SLD_ FILE_DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-031	SLD File downloaded to device	Interface
SECUR_EVT_SLD_ FILE_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-032	SLD File uploaded from device	Interface
SECUR_EVT_RBAC_ LOGIN	62443-ACCESS_CONTROL	Notice	LOGIN_OK	IEC-62351-14:1.1	Log-in successful	Interface
SECUR_EVT_RBAC_ LOGOUT	62443-ACCESS_CONTROL	Notice	LOGOUT_USER	IEC 62351-14:1.8	Log-out (user logged out)	Interface
Bypass mode Activated	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-033	Bypass Mode Activated	Interface
Bypass mode Deactivated	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-034	Bypass Mode Deactivated	Interface
SECUR_EVT_RADIUS_KEY_CHANGED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-044	RADIUS Secret Key changed	Interface
SECUR_SEC_ SETTINGS_ RESTORED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-041	Security settings restored	Interface
Switch to Golden Image	62443-AUDIT_LOG	Notice	-	2910-MiCP40-045	Device switching to Firmware update mode	Interface
FIRMWARE_ VALIDATION_ SUCCESS	62443-AUDIT_LOG	Notice	-	2910-MiCP40-035	Firmware Digital Signature check successful	Interface
FIRMWARE_ VALIDATION_FAIL	62443-AUDIT_LOG	warning	-	2910-MiCP40-036	Firmware Digital Signature check failed	Interface
Firmware update process started	62443-AUDIT_LOG	Notice	-	2910-MiCP40-046	Firmware update initiated	Interface

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
Fail to receive firmware files	62443-AUDIT_LOG	Warning	-	2910-MiCP40-047	Firmware files transfer failed	Interface
Fail to update firmware	62443-AUDIT_LOG	Warning	-	2910-MiCP40-048	Firmware update failed	Interface
Firmware update process success	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-049	Firmware update successful	Interface, Previous FW version, Latest FW version
Serial&Model number update success	62443-AUDIT_LOG	Notice	-	2910-MiCP40-050	Serial/Model number update successful	
Serial&Model number update fail	62443-AUDIT_LOG	Warning	-	2910-MiCP40-051	Serial/Model number update failed	Interface
NP1 MAC update success	62443-AUDIT_LOG	Notice	-	2910-MiCP40-052	NP1 MAC address update successful	Interface
NP1 MAC update fail	62443-AUDIT_LOG	Warning	-	2910-MiCP40-053	NP1 MAC address update failed	Interface
NP2 MAC update success	62443-AUDIT_LOG	Notice	-	2910-MiCP40-054	NP2 MAC address update successful	Interface
NP2 MAC update fail	62443-AUDIT_LOG	Warning	-	2910-MiCP40-055	NP2 MAC address update failed	Interface
Fallback to Device Authentication	62443-ACCESS_CONTROL	Warning	-	2910-MiCP40-056	Fallback to Device Authentication	Interface
User logged out due to inactivity timeout	62443-ACCESS_CONTROL	Notice	LOGOUT_TIMEOUT	IEC 62351-14:1.9	Log-out by user inactivity (timeout).	Interface
Security events upload	62443-AUDIT_LOG	Notice	-	2910-MiCP40-042	Security Events uploaded from device	Interface
SSH Passcode change	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-057	SSH pass code change	Interface
SSH Client Authentication Fail	62443-ACCESS_CONTROL	Warning	-	2910-MiCP40-059	Failed client authentication	Interface
SSH Client Authentication Success	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-058	Successful client authentication	Interface
New User added	62443-CONFIG_CHANGE	Notice	USER_ACCNT_CREATE_OK	IEC 62351-14:2.15	User account created successfully.	Interface

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
User deleted	62443-CONFIG_CHANGE	Notice	USER_ACCNT_DEL_OK	IEC 62351-14:2.21	User account deleted successfully.	Interface
User role change	62443-CONFIG_CHANGE	Notice	USER_PERMISSION_CHANGE_OK	IEC 62351-14:2.11	Permission changed successfully.	Interface
User name change	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-060	User renamed successfully	Interface

Where the Interface values in "Extra Info" parameter are: "UI", "FP", "RP1", "RP2", "NET", "HMI".

18.10.2 SECURITY EVENTS: SYSLOG

Security events are also logged to a remote server and are based on Syslog [RFC 5424].

All login and logout attempts from local and central authentication, whether successful or failed, are logged. The contents of each successful or failed, login and logout security event include a specific username.

The security log cannot be cleared by any of the available roles.

The contents of each login and/or logout security event include the relevant interface. The following interfaces are supported:

Interface	Abbr.
Front Port	FP
Rear Port 1	RP1
Rear Port 2	RP2
Network Port 1 or 2	NET
Front Panel	UI

The following events are available to be logged to the syslog server:

Security Event	SNMP Trap Text
SECUR_EVT_PW_SET_NON_COMPLIANT	User Password change failed - policy check failed
SECUR_EVT_PW_MODIFIED	User password changed successfully
SECUR_EVT_PW_ENTRY_NOW_BLOCKED	User locked – Wrong credentials
SECUR_EVT_PW_ENTRY_UNBLOCKED	User unlocked
SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	Log-in attempt when user is locked
SECUR_EVT_INVALID_PW_ENTERED	Log-in failed - Wrong credentials
SECUR_EVT_PW_TIMED_OUT	Log-in failed - credentials expired.
SECUR_EVT_RECOVERY_PW_ENTERED	Recovery password entered
SECUR_EVT_IED_SEC_CODE_READ	Security Code read

Security Event	SNMP Trap Text
SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	Security Code Timer expired
SECUR_EVT_PORT_DISABLED	Port Disabled
SECUR_EVT_PORT_ENABLED	Port Enabled
SECUR_EVT_PSL_SETTINGS_DOWNLOADED	PSL Settings downloaded to device
SECUR_EVT_DNP_SETTINGS_DOWNLOADED	DNP Settings downloaded to device
SECUR_EVT_61850_CONFIG_DOWNLOADED	IEC61850 Config downloaded to device
SECUR_EVT_USER_CURVES_DOWNLOADED	User Curves downloaded to device
SECUR_EVT_SETTING_GRP_DOWNLOADED	Setting Group downloaded to device
SECUR_EVT_DR_SETTINGS_DOWNLOADED	DR Settings downloaded to device
SECUR_EVT_PSL_SETTINGS_UPLOADED	PSL Settings uploaded from device
SECUR_EVT_DNP_SETTINGS_UPLOADED	DNP Settings uploaded from device
SECUR_EVT_61850_CONFIG_UPLOADED	IEC61850 Config uploaded from device
SECUR_EVT_USER_CURVES_UPLOADED	User Curves uploaded from device
SECUR_EVT_PSL_CONFIG_UPLOADED	PSL Config uploaded from device
SECUR_EVT_SETTINGS_UPLOADED	Settings uploaded from device
SECUR_EVT_CS_SETTINGS_CHANGED	Control & Support settings changed
SECUR_EVT_DR_SETTINGS_CHANGED	Disturbance Record Settings changed
SECUR_EVT_SETTING_GROUP_CHANGED	Setting Group changed
SECUR_EVT_DEFAULT_SETTINGS_RESTORED	Default Settings restored
SECUR_EVT_DEFAULT_USRCURVE_RESTORED	Default User Curve restored
SECUR_EVT_RADIUS_UNAVAIL	RADIUS server not available
SECUR_EVT_SESSION_LIMIT	Active user sessions limit reached
SECUR_EVT_SLD_FILE_DOWNLOADED	SLD File downloaded to device
SECUR_EVT_SLD_FILE_UPLOADED	SLD File uploaded from device
SECUR_EVT_RBAC_LOGIN	Log-in successful
SECUR_EVT_RBAC_LOGOUT	Log-out (user logged out)
Bypass mode Activated	Bypass Mode Activated
Bypass mode Deactivated	Bypass Mode Deactivated

Security Event	SNMP Trap Text
RADIUS Secret Key changed	RADIUS Secret Key changed
SECUR_EVT_SEC_SETTINGS_RESTORED	Security settings restored
Switch to Golden Image	Device switching to Firmware update mode
Fallback to Device Authentication	Fallback to Device Authentication
User logged out due to inactivity timeout.	Log-out by user inactivity (timeout)
Security events upload	Security Events uploaded from device
SSH Passcode change	SSH pass code change
SSH Client Authentication Fail	Failed client authentication
SSH Client Authentication Success	Successful client authentication
New User added	User account created successfully.
User deleted	User account deleted successfully.
User role change	Permission changed successfully.

18.10.3 SYSLOG CLIENT

The IED supports security event reporting through the Syslog protocol for supporting Security Information Event Management (SIEM) systems for centralized cyber security Monitoring over UDP protocol.

The IED is a Syslog client that supports two Syslog servers. The following settings are available in the *SECURITY CONFIG.* column.

Setting Name	Description	Min	Max	Default	Units	User Role Required
SysLog Pri IP	The IP address of the target Syslog server (Primary)	0.0.0.0	223.255.255.254	0.0.0.0	-	SECADM
SysLog Sec IP	The IP address of the target Syslog server (Secondary)	0.0.0.0	223.255.255.254	0.0.0.0	-	SECADM
SysLog Port	The UDP port number of the target Syslog server	1	65535	514	-	SECADM

18.10.4 SYSLOG FUNCTIONALITY

P40 supports IEC 62351-14 based cyber security event monitoring and is based on Syslog [RFC 5424].

Sample Syslog messages are shown below:

Event	Access Method	Syslog Message (As from Syslog Server)
IED Powered On	UI	5492, 2024-06-12T19:18:28.982Z, 423991K, GE_RE_P543_____AB0_o, MiCP40_POWER_ON, 2910-MiCP40-028, notice, IECCTRLSYS, Device Powered On, UI
ADMIN1 Log-in successful	FP	5523, 2024-06-12T20:04:26.851Z, 423991K, GE_RE_P543_____AB0_o, LOGIN_OK, IEC 62351-14:1.1, notice, IECACCCTRL, ADMIN1, SECAM, Log-in successful, FP

Event	Access Method	Syslog Message (As from Syslog Server)
SSH Successful client authentication (S1 Agile)	NET	5460, 2024-06-12T18:04:45.359Z, 423991J, GE_RE_P546_____AB0_o, MiCP40_SSH_CLIENT_AUTH_SUCCESS, 2910-MiCP40-058, notice, IECACCCTRL, Successful client authentication, NET
Firmware update successful	FP	5476, 2024-06-12T19:18:19.004Z, 423991K, GE_RE_P543_____AB0_o, MiCP40_FW_UPDATE_SUCCESS, 2910-MiCP40-049, notice, IECCONFCHG, Firmware update successful, FP, P546_____AB0_o to P543_____AB0_o

18.10.5 SECURITY EVENTS: SNMP

Security events can also be sent as SNMP traps to a remote SNMP server. These traps are supported in both V2c and V3 versions of SNMP. For further information related to the full SNMP interface in P40, refer to the SNMP section in the COMMUNICATIONS chapter.

The format of the SNMP traps for security events consists of three parts as described below:

"Event Description, Username, Interface"

- Event Description: Short description of the alarm, same as the description present in Security event.
- Username: User associated with the event, provided only when Username is available for the Security event.
- Interface: Interface on which Security event has occurred, same as the interface information present in Security event.

The following events are available to be logged to the SNMP server:

Security Event	SNMP Trap Text
SECUR_EVT_PW_SET_NON_COMPLIANT	User Password change failed - policy check failed
SECUR_EVT_PW_MODIFIED	User password changed successfully
SECUR_EVT_PW_ENTRY_NOW_BLOCKED	User locked – Wrong credentials
SECUR_EVT_PW_ENTRY_UNBLOCKED	User unlocked
SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	Log-in attempt when user is locked
SECUR_EVT_INVALID_PW_ENTERED	Log-in failed - Wrong credentials
SECUR_EVT_PW_TIMED_OUT	Log-in failed - credentials expired.
SECUR_EVT_RECOVERY_PW_ENTERED	Recovery password entered
SECUR_EVT_IED_SEC_CODE_READ	Security Code read
SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	Security Code Timer expired
SECUR_EVT_PORT_DISABLED	Port Disabled
SECUR_EVT_PORT_ENABLED	Port Enabled
SECUR_EVT_PSL_SETTINGS_DOWNLOADED	PSL Settings downloaded to device
SECUR_EVT_DNP_SETTINGS_DOWNLOADED	DNP Settings downloaded to device
SECUR_EVT_61850_CONFIG_DOWNLOADED	IEC61850 Config downloaded to device
SECUR_EVT_USER_CURVES_DOWNLOADED	User Curves downloaded to device

Security Event	SNMP Trap Text
SECUR_EVT_SETTING_GRP_DOWNLOADED	Setting Group downloaded to device
SECUR_EVT_DR_SETTINGS_DOWNLOADED	DR Settings downloaded to device
SECUR_EVT_PSL_SETTINGS_UPLOADED	PSL Settings uploaded from device
SECUR_EVT_DNP_SETTINGS_UPLOADED	DNP Settings uploaded from device
SECUR_EVT_61850_CONFIG_UPLOADED	IEC61850 Config uploaded from device
SECUR_EVT_USER_CURVES_UPLOADED	User Curves uploaded from device
SECUR_EVT_PSL_CONFIG_UPLOADED	PSL Config uploaded from device
SECUR_EVT_SETTINGS_UPLOADED	Settings uploaded from device
SECUR_EVT_CS_SETTINGS_CHANGED	Control & Support settings changed
SECUR_EVT_DR_SETTINGS_CHANGED	Disturbance Record Settings changed
SECUR_EVT_SETTING_GROUP_CHANGED	Setting Group changed
SECUR_EVT_DEFAULT_SETTINGS_RESTORED	Default Settings restored
SECUR_EVT_DEFAULT_USRCURVE_RESTORED	Default User Curve restored
SECUR_EVT_POWER_ON	Device Powered On
SECUR_EVT_RADIUS_UNAVAIL	RADIUS server not available
SECUR_EVT_SESSION_LIMIT	Active user sessions limit reached
SECUR_EVT_SLD_FILE_DOWNLOADED	SLD File downloaded to device
SECUR_EVT_SLD_FILE_UPLOADED	SLD File uploaded from device
SECUR_EVT_RBAC_LOGIN	Log-in successful
SECUR_EVT_RBAC_LOGOUT	Log-out (user logged out)
Bypass mode Activated	Bypass Mode Activated
Bypass mode Deactivated	Bypass Mode Deactivated
RADIUS Secret Key changed	RADIUS Secret Key changed
SECUR_EVT_SEC_SETTINGS_RESTORED	Security settings restored
Switch to Golden Image	Device switching to Firmware update mode
Fallback to Device Authentication	Fallback to Device Authentication
User logged out due to inactivity timeout.	Log-out by user inactivity (timeout)
Security events upload	Security Events uploaded from device

Security Event	SNMP Trap Text
SSH Passcode change	SSH pass code change
SSH Client Authentication Fail	Failed client authentication
SSH Client Authentication Success	Successful client authentication
New User added	User account created successfully.
User deleted	User account deleted successfully.
User role change	Permission changed successfully.

CHAPTER 19

INSTALLATION

19.1 CHAPTER OVERVIEW

This chapter provides information about installing the product.

This chapter contains the following sections:

19.2 HANDLING THE GOODS

Our products are of robust construction but require careful treatment before installation on site. This section discusses the requirements for receiving and unpacking the goods, as well as associated considerations regarding product care and personal safety.

Caution:
Before lifting or moving the equipment you should be familiar with the Safety Information chapter of this manual.

19.2.1 RECEIPT OF THE GOODS

On receipt, ensure the correct product has been delivered. Unpack the product immediately to ensure there has been no external damage in transit. If the product has been damaged, make a claim to the transport contractor and notify us promptly.

For products not intended for immediate installation, repack them in their original delivery packaging.

19.2.2 UNPACKING THE GOODS

When unpacking and installing the product, take care not to damage any of the parts and make sure that additional components are not accidentally left in the packing or lost. Do not discard any CDROMs or technical documentation (where included). These should accompany the unit to its destination substation and put in a dedicated place.

The site should be well lit to aid inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies where installation is being carried out at the same time as construction work.

19.2.3 STORING THE GOODS

If the unit is not installed immediately, store it in a place free from dust and moisture in its original packaging. Keep any dehumidifier bags included in the packing. The dehumidifier crystals lose their efficiency if the bag is exposed to ambient conditions. Restore the crystals before replacing it in the carton. Ideally regeneration should be carried out in a ventilating, circulating oven at about 115°C. Bags should be placed on flat racks and spaced to allow circulation around them. The time taken for regeneration will depend on the size of the bag. If a ventilating, circulating oven is not available, when using an ordinary oven, open the door on a regular basis to let out the steam given off by the regenerating silica gel.

On subsequent unpacking, make sure that any dust on the carton does not fall inside. Avoid storing in locations of high humidity. In locations of high humidity the packaging may become impregnated with moisture and the dehumidifier crystals will lose their efficiency.

The device can be stored between –25º to +70ºC for unlimited periods or between -40°C to + 85°C for up to 96 hours (see technical specifications).

To avoid deterioration of electrolytic capacitors, power up units that are stored in a de-energised state once a year, for one hour continuously.

19.2.4 DISMANTLING THE GOODS

If you need to dismantle the device, always observe standard ESD (Electrostatic Discharge) precautions. The minimum precautions to be followed are as follows:

- Use an antistatic wrist band earthed to a suitable earthing point.
- Avoid touching the electronic components and PCBs.

19.3 MOUNTING THE DEVICE

The products are dispatched either individually or as part of a panel or rack assembly.

Individual products are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centres.

The products are designed so the fixing holes in the mounting flanges are only accessible when the access covers are open.

If you use a P991 or MMLG test block with the product, when viewed from the front, position the test block on the right-hand side of the associated product. This minimises the wiring between the product and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

19.3.1 FLUSH PANEL MOUNTING

Panel-mounted devices are flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

Caution:
Do not use conventional self-tapping screws, because they have larger heads and could damage the faceplate.

Alternatively, you can use tapped holes if the panel has a minimum thickness of 2.5 mm.

For applications where the product needs to be semi-projection or projection mounted, a range of collars are available.

If several products are mounted in a single cut-out in the panel, mechanically group them horizontally or vertically into rigid assemblies before mounting in the panel.

Caution:
Do not fasten products with pop rivets because this makes them difficult to remove if repair becomes necessary.

19.3.2 RACK MOUNTING

Panel-mounted variants can also be rack mounted using single-tier rack frames (our part number FX0021 001), as shown in the figure below. These frames are designed with dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483 mm (19 inch) rack this enables combinations of case widths up to a total equivalent of size 80TE to be mounted side by side.

The two horizontal rails of the rack frame have holes drilled at approximately 26 mm intervals. Attach the products by their mounting flanges using M4 Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

Caution:
Risk of damage to the front cover molding. Do not use conventional self-tapping screws, including those supplied for mounting MiDOS products because they have slightly larger heads.

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

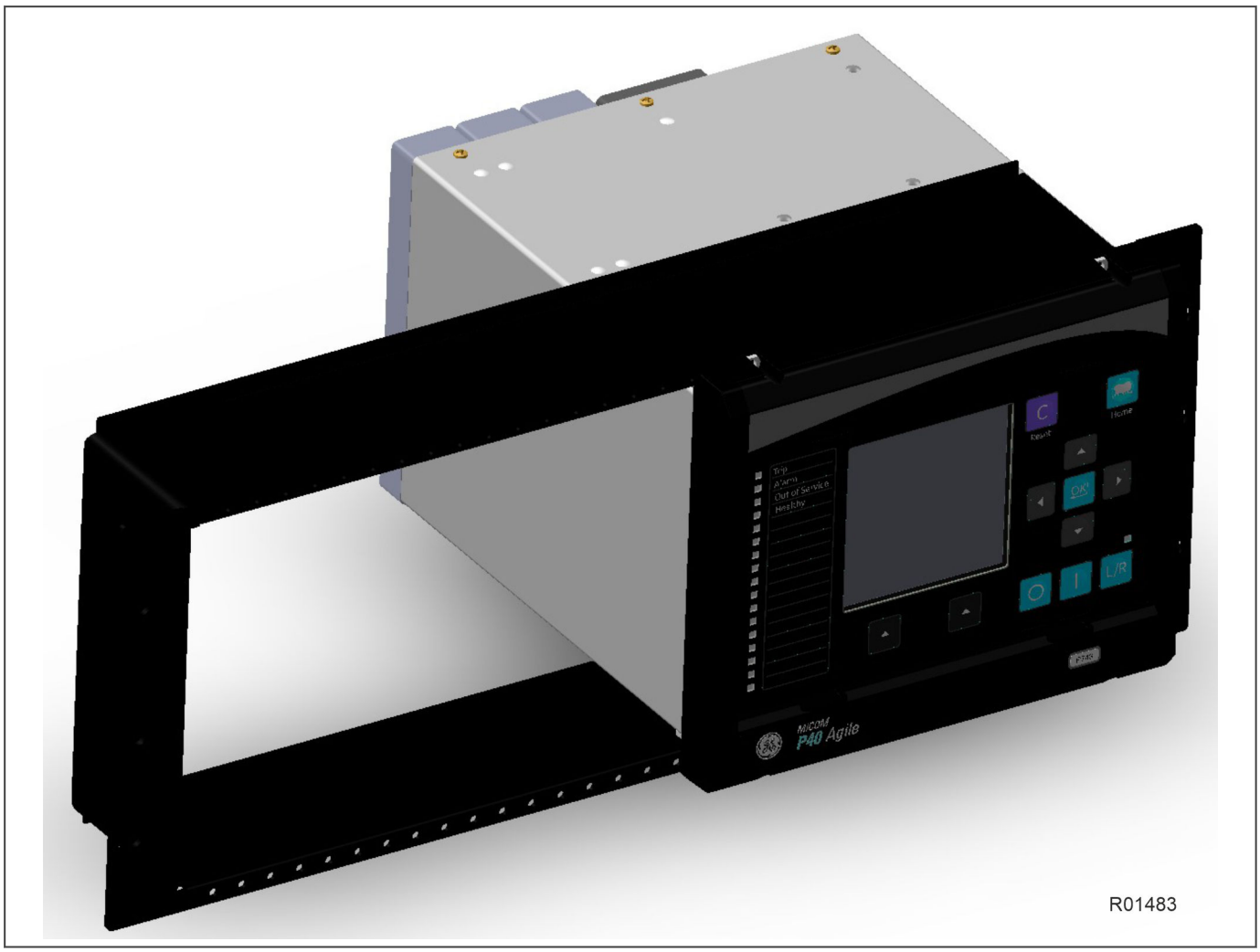


Figure 244: Rack mounting of products

Products can be mechanically grouped into single tier (4U) or multi-tier arrangements using the rack frame. This enables schemes using products from different product ranges to be pre-wired together before mounting.

Use blanking plates to fill any empty spaces. The spaces may be used for installing future products or because the total size is less than 80TE on any tier. Blanking plates can also be used to mount ancillary components. The part numbers are as follows:

Case size summation	Blanking plate part number
5TE	GJ2028 001
10TE	GJ2028 002
20TE	GJ2028 004
40TE	GJ2028 008
60TE	GJ2028 012

19.3.3 REFURBISHMENT SOLUTIONS

A major advantage of the 5th Generation MiCOM 5th Generation IEDs is the ease in which you can refurbish older P841 generation devices. The P40 5th Generation 5th Generation IEDs retain form, fit and function compatibility, compared to older P841 generations, while delivering the latest platform and software and maintains pin to pin refurbishment compatibility. This allows easy upgrade of the protection system with minimum impact, resulting in

only a few minutes of downtime. To begin the upgrade for a legacy P841 IED to the latest 5th Generation 5th Generation:

- Take the order code (CORTEC) of the older relay being removed, typically a blue case relay
- Translate to today's latest GE Vernova MiCOM model, adding Ethernet options if required
- Order the new 5th Generation P40 relay
- Use the S1 Agile toolsuite to extract and convert the settings and logic
- Detach the medium duty terminal blocks from your old device, making sure you leave the wiring attached. It is recommended the CT/VT terminal blocks on the new IED are used during refurbishment
- Attach the medium duty terminal blocks and wiring from your old device to the new IED and connect the CT/VT wiring to the original terminal blocks of the new IED
- Download your converted files
- Test, then return circuit to service

Please contact us for assistance.

19.4 CABLES AND CONNECTORS

This section describes the type of wiring and connections that should be used when installing the device. For pin-out details please refer to the Hardware Design chapter or the wiring diagrams.

Caution:
Before carrying out any work on the equipment you should be familiar with the Safety Section and the ratings on the equipment's rating label.

19.4.1 TERMINAL BLOCKS

The device may use one or more of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, relay outputs and rear communications port
- MiDOS terminal blocks for CT and VT circuits
- RTD/CLIO terminal block for connection to analogue transducers

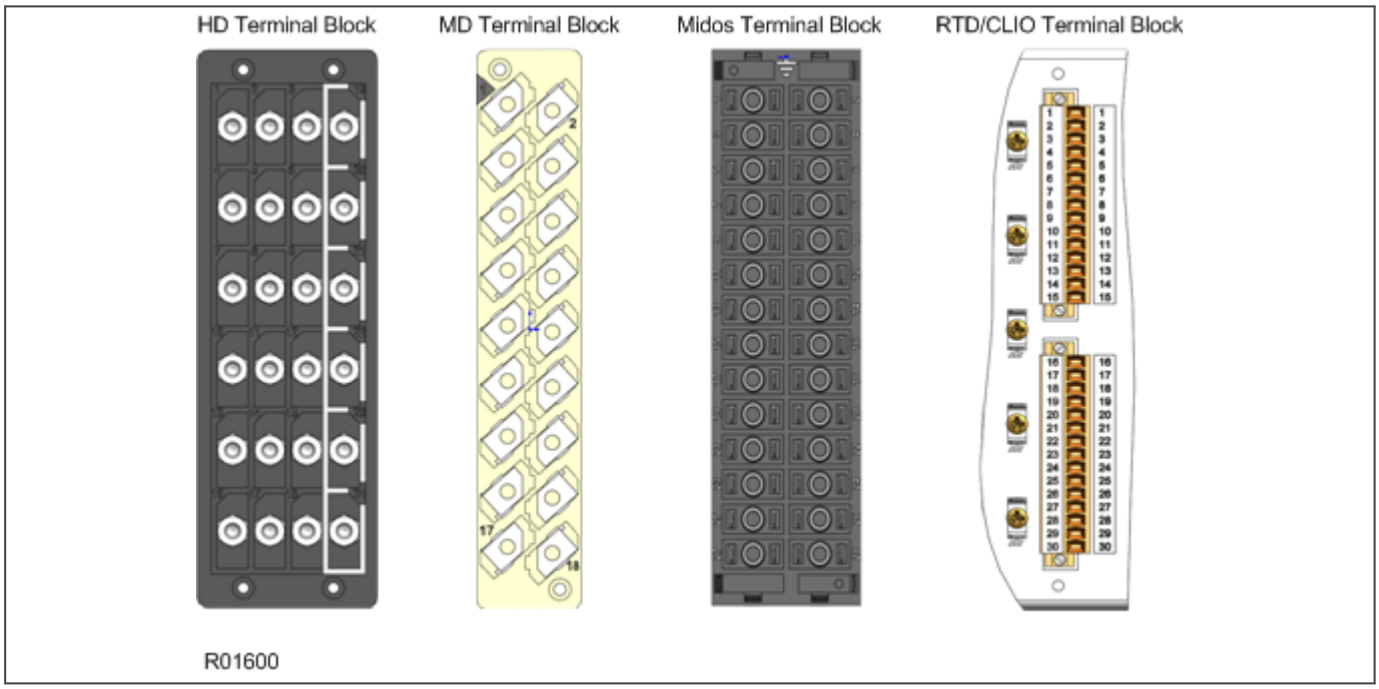


Figure 245: Terminal block types

MiCOM products are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per terminal.

If required, M4 90° crimp ring terminals can be supplied in three different sizes depending on wire size. Each type is available in bags of 100.

Part number	Wire size	Insulation color
ZB9124 901	0.25 - 1.65 mm^2 (22 – 16 AWG)	Red
ZB9124 900	1.04 - 2.63 mm^2 (16 – 14 AWG)	Blue

Note:
IP2x shields and side cover panels may be fitted to provide IP20 ingress protection for MiCOM terminal blocks. The shields and covers can be attached during installation or retrofitted to upgrade existing installations. The shields are supplied with four language fitting instructions, publication number: IP2x-TM-4L-n (where n is the current issue number). For more information, contact your local sales office or our worldwide Contact Centre.

19.4.2 POWER SUPPLY CONNECTIONS

These should be wired with 1.5 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

Caution:
Protect the auxiliary power supply wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

19.4.3 EARTH CONNNECTION

Every device must be connected to the cubicle earthing bar using the M4 earth terminal.

Use a wire size of at least 2.5 mm^2 terminated with a ring terminal.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm^2 using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm^2 per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

Note:
To prevent any possibility of electrolytic action between brass or copper ground conductors and the rear panel of the product, precautions should be taken to isolate them from one another. This could be achieved in several ways, including placing a nickel-plated or insulating washer between the conductor and the product case, or using tinned ring terminals.

19.4.4 CURRENT TRANSFORMERS

Current transformers would generally be wired with 2.5 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm^2 using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm^2 per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

Caution:
Current transformer circuits must never be fused.

Note:
If there are CTs present, spring-loaded shorting contacts ensure that the terminals into which the CTs connect are shorted before the CT contacts are broken.

Note:
For 5A CT secondaries, we recommend using 2 x 2.5 mm^2 PVC insulated multi-stranded copper wire.

19.4.5 VOLTAGE TRANSFORMER CONNECTIONS

Voltage transformers should be wired with 2.5 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

19.4.6 WATCHDOG CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

19.4.7 EIA(RS)485 AND K-BUS CONNECTIONS

For connecting the EIA(RS485) / K-Bus ports, use 2-core screened cable with a maximum total length of 1000 m or 200 nF total cable capacitance.

To guarantee the performance specifications, you must ensure continuity of the screen, when daisy chaining the connections.

Two-core screened twisted pair cable should be used. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The K-Bus signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product’s chassis. This is for both safety and noise reasons.

A typical cable specification would be:

- Each core: 16/0.2 mm^2 copper conductors, PVC insulated
- Nominal conductor area: 0.5 mm^2 per core
- Screen: Overall braid, PVC sheathed

19.4.8 IRIG-B CONNECTION

The IRIG-B input and BNC connector have a characteristic impedance of 50 ohms. We recommend that connections between the IRIG-B equipment and the product are made using coaxial cable of type RG59LSF with a halogen free, fire retardant sheath.

19.4.9 OPTO-INPUT CONNECTIONS

These should be wired with 1 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Each opto-input has a selectable preset ½ cycle filter. This makes the input immune to noise induced on the wiring. This can, however slow down the response. If you need to switch off the ½ cycle filter, either use double pole switching on the input, or screened twisted cable on the input circuit.

Caution:
Protect the opto-inputs and their wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

19.4.10 OUTPUT RELAY CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

19.4.11 ETHERNET METALLIC CONNECTIONS

If the device has a metallic Ethernet connection, it can be connected to either a 10Base-T or a 100Base-TX Ethernet hub. Due to noise sensitivity, we recommend this type of connection only for short distance connections, ideally where the products and hubs are in the same cubicle. For increased noise immunity, CAT 6 (category 6) STP (shielded twisted pair) cable and connectors can be used.

The connector for the Ethernet port is a shielded RJ-45. The pin-out is as follows:

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

19.4.12 ETHERNET FIBRE CONNECTIONS

We recommend the use of fibre-optic connections for permanent connections in a substation environment. The 100 Mbps fibre optic port uses type LC connectors (one for Tx and one for Rx), compatible with 50/125 µm or 62.5/125 µm multimode fibres at 1300 nm wavelength.

19.4.13 USB CONNECTION

The IED has a type B USB socket inside the bottom compartment. A standard USB printer cable (type A one end, type B the other end) can be used to connect a local PC to the IED. This cable is the same as that used for connecting a printer to a PC.

19.4.14 GPS FIBRE CONNECTION

Some products use a GPS 1 PPS timing signal. If applicable, this is connected to a fibre-optic port on the coprocessor board in slot B. The fibre-optic port uses an ST type connector, compatible with fibre multimode 50/125 µm or 62.5/125 µm – 850 nm.

19.4.15 FIBRE COMMUNICATION CONNECTIONS

The fibre optic port consists of one or two channels using ST type connectors (one for Tx and one for Rx). The type of fibre used depends on the option selected.

850 nm and 1300 nm multimode systems use 50/125 µm or 62.5/125 µm multimode fibres. 1300 nm and 1550 nm single mode systems use 9/125 µm single mode fibres.

19.5 CASE DIMENSIONS

Not all products are available in all case sizes.

19.5.1 CASE DIMENSIONS 40TE

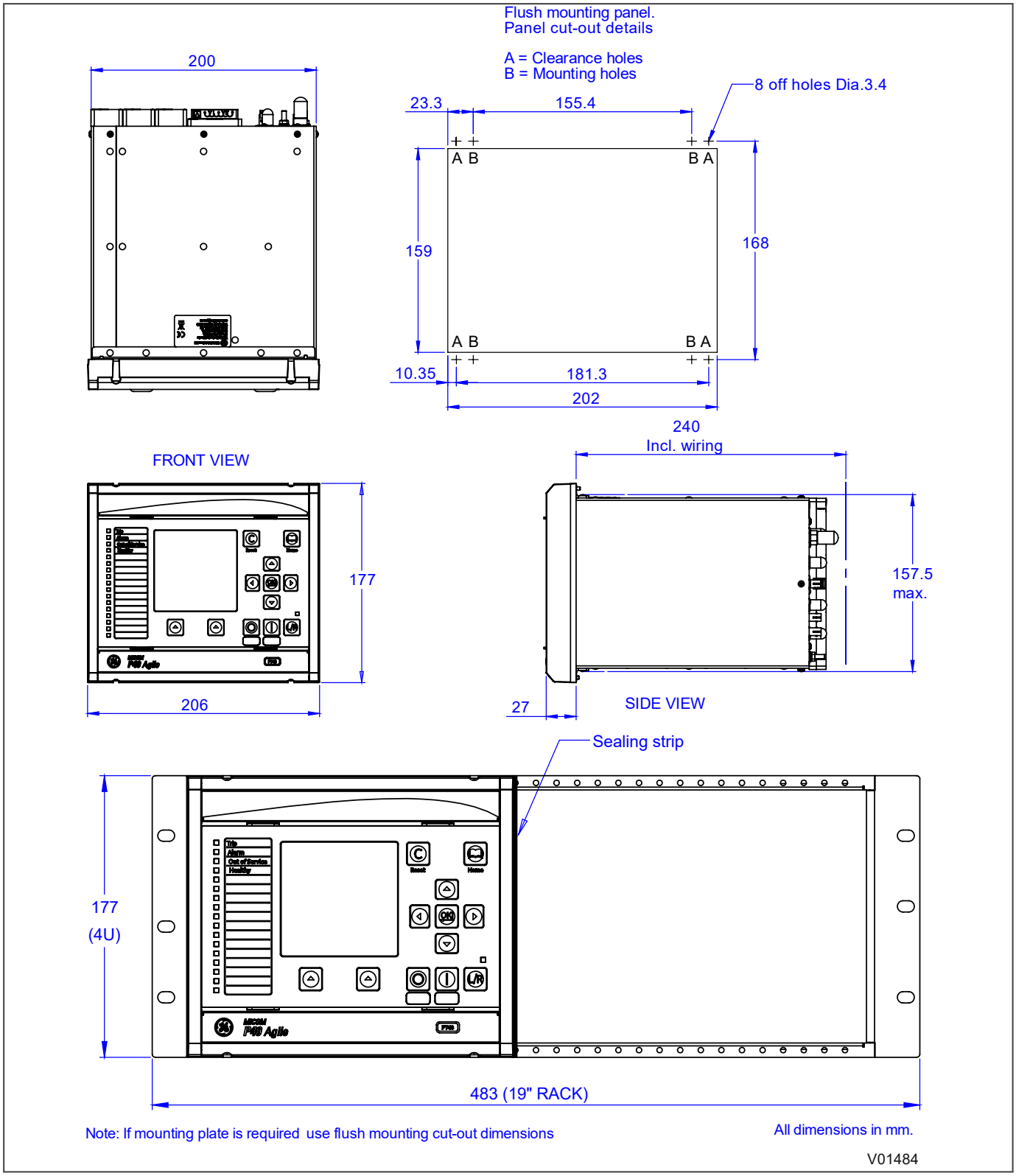


Figure 246: 40TE case dimensions

19.5.2 CASE DIMENSIONS 60TE

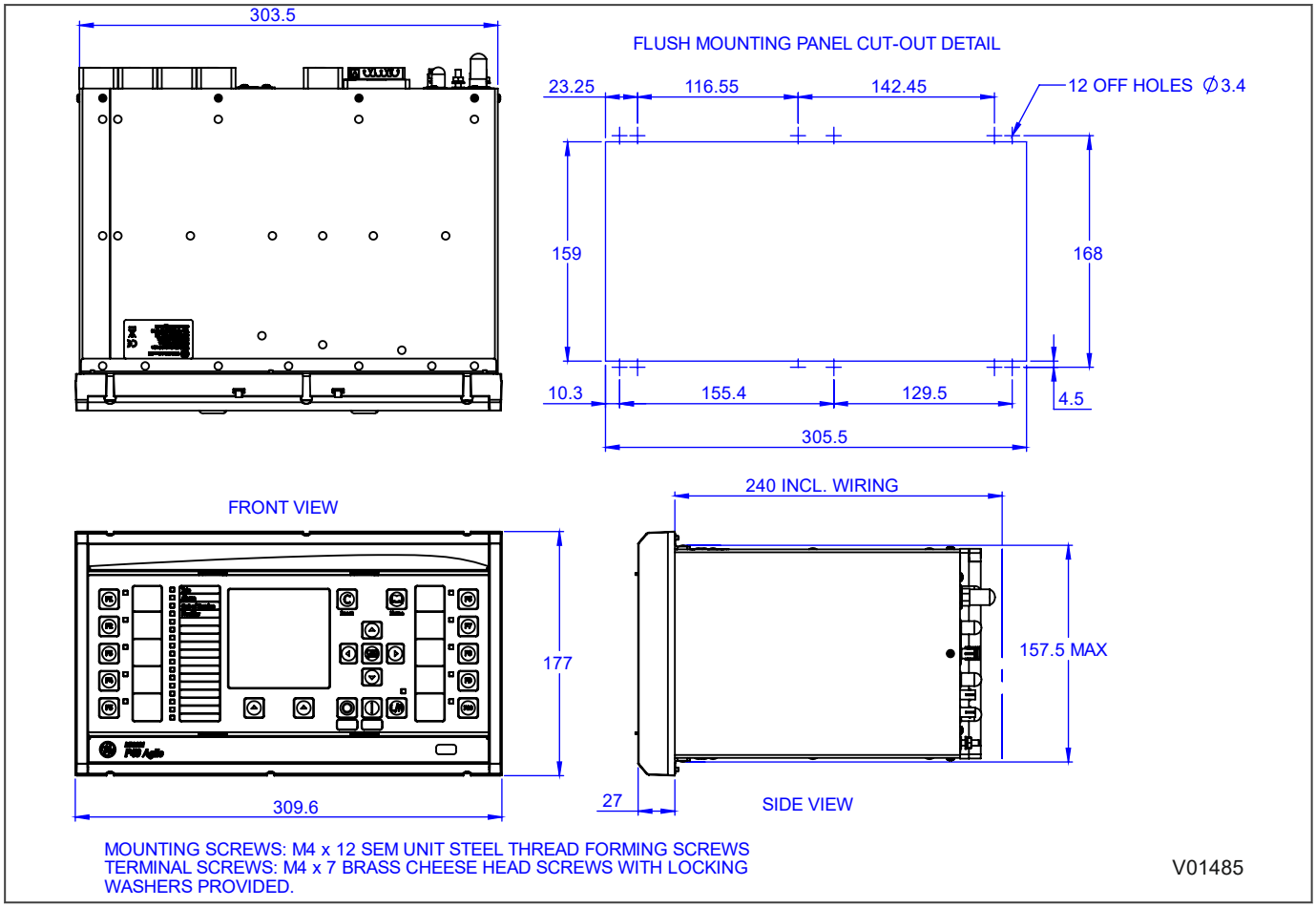


Figure 247: 60TE case dimensions

19.5.3 CASE DIMENSIONS 80TE

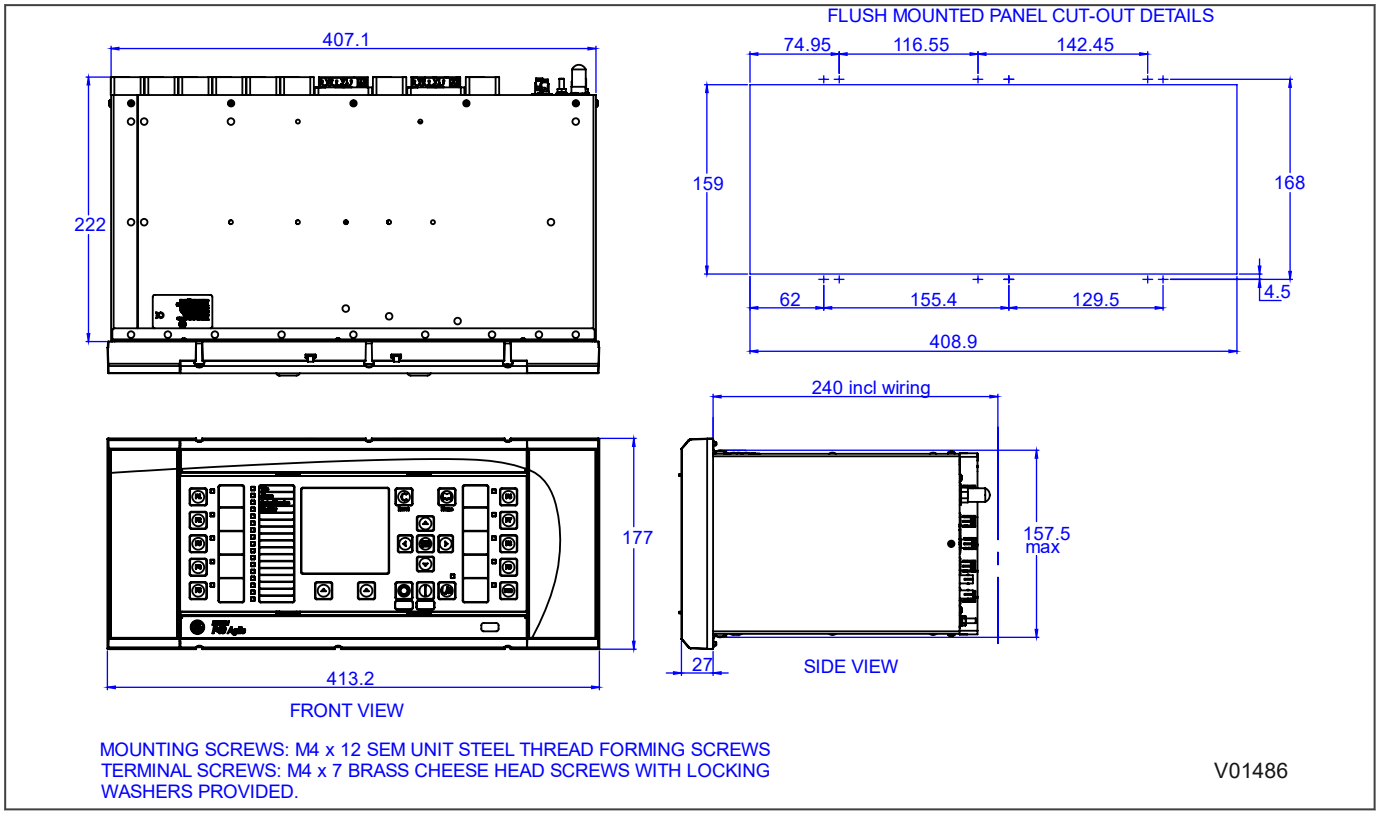


Figure 248: 80TE case dimensions

CHAPTER 20

COMMISSIONING INSTRUCTIONS

20.1 CHAPTER OVERVIEW

This chapter contains the following sections:

20.2 GENERAL GUIDELINES

GE Vernova IEDs are self-checking devices and will raise an alarm in the unlikely event of a failure. This is why the commissioning tests are less extensive than those for non-numeric electronic devices or electro-mechanical relays.

To commission the devices, you (the commissioning engineer) do not need to test every function. You need only verify that the hardware is functioning correctly and that the application-specific software settings have been applied. You can check the settings by extracting them using the settings application software, or by means of the front panel interface (HMI panel).

The menu language is user-selectable, so you can change it for commissioning purposes if required.

Note:
Remember to restore the language setting to the customer's preferred language on completion.

Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or Safety Guide SFTY/4LM as well as the ratings on the equipment's rating label.

Warning:
With the exception of the CT shorting contacts check, do not disassemble the device during commissioning.

20.3 COMMISSIONING TEST MENU

The IED provides several test facilities under the *COMMISSION TESTS* menu heading. There are menu cells that allow you to monitor the status of the opto-inputs, output relay contacts, internal Digital Data Bus (DDB) signals and user-programmable LEDs. This section describes these commissioning test facilities.

20.3.1 OPTO I/P STATUS CELL (OPTO-INPUT STATUS)

This cell can be used to monitor the status of the opto-inputs while they are sequentially energised with a suitable DC voltage. The cell is a binary string that displays the status of the opto-inputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each logic input.

20.3.2 RELAY O/P STATUS CELL (RELAY OUTPUT STATUS)

This cell can be used to monitor the status of the relay outputs. The cell is a binary string that displays the status of the relay outputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each relay output.

The cell indicates the status of the output relays when the IED is in service. You can check for relay damage by comparing the status of the output contacts with their associated bits.

Note:
*When the **Test Mode** cell is set to `Contacts Blocked`, the relay output status indicates which contacts would operate if the IED was in-service. It does not show the actual status of the output relays, as they are blocked.*

20.3.3 TEST PORT STATUS CELL

This cell displays the status of the DDB signals that have been allocated in the ***Monitor Bit*** cells. If you move the cursor along the binary numbers, the corresponding DDB signal text string is displayed for each monitor bit.

By using this cell with suitable monitor bit settings, the state of the DDB signals can be displayed as various operating conditions or sequences are applied to the IED. This allows you to test the Programmable Scheme Logic (PSL).

20.3.4 MONITOR BIT 1 TO 8 CELLS

The eight Monitor Bit cells allows you to select eight DDB signals that can be observed in the Test Port Status cell or downloaded via the front port.

Each Monitor Bit cell can be assigned to a particular DDB signal. You set it by entering the required DDB signal number from the list of available DDB signals.

The pins of the monitor/download port used for monitor bits are as follows:

Monitor Bit	1	2	3	4	5	6	7	8
Monitor/Download Port Pin	11	12	15	13	20	21	23	24

The signal ground is available on pins 18, 19, 22 and 25.

Caution:
The monitor/download port is not electrically isolated against induced voltages on the communications channel. It should therefore only be used for local communications.

20.3.5 TEST MODE CELL

This cell allows you to perform secondary injection testing. It also lets you test the output contacts directly by applying menu-controlled test signals.

To go into test mode, select the `Test Mode` option in the ***Test Mode*** cell. This takes the IED out of service causing an alarm condition to be recorded and the ***Out of Service*** LED to illuminate. This also freezes any information stored in the *CB CONDITION* column. In IEC 60870-5-103 protocol versions, it changes the Cause of Transmission (COT) to Test Mode. In IEC 61850 protocol, it changes the quality test flag to q.test = true. See section 10.1 for further detail of IEC 61850 test mode.

In Test Mode, the output contacts are still active. To disable the output contacts you must select the `Contacts Blocked` option.

Once testing is complete, return the device back into service by setting the ***Test Mode*** Cell back to `Disabled`.

Caution:
When the cell is in Test Mode, the Scheme Logic still drives the output relays, which could result in tripping of circuit breakers. To avoid this, set the *Test Mode* cell to `Contacts Blocked`.

Note:
`Test mode` and `Contacts Blocked` mode can also be selected by energising an opto-input mapped to the Test Mode signal, and the Contact Block signal respectively.

20.3.6 TEST PATTERN CELL

The ***Test Pattern*** cell is used to select the output relay contacts to be tested when the ***Contact Test*** cell is set to `Apply Test`. The cell has a binary string with one bit for each user-configurable output contact, which can be set to '1' to operate the output and '0' to not operate it.

20.3.7 CONTACT TEST CELL

When the `Apply Test` command in this cell is issued, the contacts set for operation change state. Once the test has been applied, the command text on the LCD will change to ***No Operation*** and the contacts will remain in the Test state until reset by issuing the `Remove Test` command. The command text on the LCD will show ***No Operation*** after the `Remove Test` command has been issued.

Note:
*When the **Test Mode** cell is set to `Contacts Blocked` the **Relay O/P Status** cell does not show the current status of the output relays and therefore cannot be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.*

20.3.8 TEST LEDS CELL

When the `Apply Test` command in this cell is issued, the user-programmable LEDs illuminate for approximately 2 seconds before switching off, and the command text on the LCD reverts to ***No Operation***.

20.3.9 TEST AUTORECLOSE CELL

Where the IED provides an auto-reclose function, this cell will be available for testing the sequence of circuit breaker trip and auto-reclose cycles.

The *Trip 3 Pole* option in the ***Test Autoreclose*** cell causes the device to perform the first three phase trip/ reclose cycle so that associated output contacts can be checked for operation at the correct times during the cycle. Once the trip output has operated the command text will revert to *No Operation* whilst the rest of the auto-reclose cycle is performed. To test subsequent three-phase autoreclose cycles, you repeat the *Trip 3 Pole* command. You can also test the single phases with *Trip Pole A*, *Trip Pole B* and *Trip Pole C*.

Note:
The default settings for the programmable scheme logic has the AR Trip Test signals mapped to the Trip Input signals. If the programmable scheme logic has been changed, it is essential that these signals retain this mapping for the Test Autoreclose facility to work.

20.3.10 STATIC TEST MODE

Static Test Mode can be set to *Enabled* or *Disabled*. When the Static Test mode is enabled it allows injection test that don't support dynamic switching to be used to commission and test the device.

Dynamic secondary injection test sets are able to accurately mimic real power system faults. The test sets mimic an instantaneous fault “shot”, with the real rate of rise of current, and the decaying DC exponential component. Dynamic injection test sets are available, which cater for all three phases, providing a six signal set of analogue inputs: Va, Vb, Vc, Ia, Ib, Ic. Such injection test sets can be used with the device, with no special testing limitations.

Static test sets, also known as Static Simulators, may not properly provide or simulate:

- A healthy pre-fault voltage
- A real fault shot (instead a gradually varying current or voltage would be used)
- The rate of rise of current and DC components
- A complete set of three-phase analogue inputs
- Real dynamic step changes in current and voltage.

Some of the protection in this product is based on delta techniques which recognise step changes in actual power system quantities. Because these may not be produced by static test sets,, certain functions are can be disabled or bypassed to allow injection testing with static test sets. Enabling the ***Static Test Mode*** option does this..

For the tests, the delta directional line is replaced by a conventional distance directional line. Extra filtering of distance comparators is used so the filtering slows to use a fixed one cycle window. Memory polarising is replaced by cross-polarising from unfaulted phases.

Note:
Trip times may be up to ½ cycle longer when tested in the static mode, due to the nature of the test voltage and current, and the slower filtering. This is normal, and perfectly acceptable.

20.3.11 LOOPBACK MODE

Loopback Mode can be used to test InterMiCOM^{64} signalling.

Note:
If the cell is set to Internal, only the IED software is checked. If the cell is set to External, both the software and hardware are checked.

When the device is switched into Loopback Mode, it automatically uses generic addresses 0-0. It responds as if it is connected to a remote device. The sent and received IM^{64} signals continue to be routed to and from the signals defined in the programmable logic.

Note:
Loopback mode can also be selected by energising an opto-input mapped to the Loopback signal.

20.3.12 IM64 TEST PATTERN

This cell is used with the ***IM64 Test Mode*** cell to set a 16-bit pattern (8 bits per channel), which is transmitted whenever the ***IM64 Test Mode*** cell is set to `Enabled`. The ***IM64 TestPattern*** cell has a binary string with one bit for each user-defined Inter-MiCOM command. These can be set to '1' to operate the IM64 output under test conditions and '0' for no operation.

20.3.13 IM64 TEST MODE

When the `Enable` command in this cell is issued, the InterMiCOM^{64} commands change to reflect the state of the values set in the ***IM64 TestPattern*** cell. If the cell is set to Disabled, the InterMiCOM^{64} commands reflect the state of the signals generated by the protection and control functions.

20.3.14 RED AND GREEN LED STATUS CELLS

These cells contain binary strings that indicate which of the user-programmable red and green LEDs are illuminated when accessing from a remote location. A '1' indicates that a particular LED is illuminated.

Note:
*When the status in both **Red LED Status** and **Green LED Status** cells is '1', this indicates the LEDs illumination is yellow.*

20.4 COMMISSIONING EQUIPMENT

Specialist test equipment is required to commission this product. We recognise three classes of equipment for commissioning :

- Recommended
- Essential
- Advisory

Recommended equipment constitutes equipment that is both necessary, and sufficient, to verify correct performance of the principal protection functions.

Essential equipment represents the minimum necessary to check that the product includes the basic expected protection functions and that they operate within limits.

Advisory equipment represents equipment that is needed to verify satisfactory operation of features that may be unused, or supplementary, or which may, for example, be integral to a distributed control/automation scheme. Operation of such features may, perhaps, be more appropriately verified as part of a customer defined commissioning requirement, or as part of a system-level commissioning regime.

20.4.1 RECOMMENDED COMMISSIONING EQUIPMENT

The minimum recommended equipment is a multifunctional three-phase AC current and voltage injection test set featuring :

- Controlled three-phase AC current and voltage sources,
- Transient (dynamic) switching between pre-fault and post-fault conditions (to generate delta conditions),
- Dynamic impedance state sequencer (capable of sequencing through 4 impedance states),
- Integrated or separate variable DC supply (0 - 250 V)
- Integrated or separate AC and DC measurement capabilities (0-440V AC, 0-250V DC)
- Integrated and/or separate timer,
- Integrated and/or separate test switches.

In addition, you will need :

- A portable computer, installed with appropriate software to liaise with the equipment under test (EUT). Typically this software will be proprietary to the product's manufacturer (for example MiCOM S1 Agile).
- Suitable electrical test leads.
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- Continuity tester
- Verified application-specific settings files

20.4.2 ESSENTIAL COMMISSIONING EQUIPMENT

As an absolute minimum, the following equipment is required:

- AC current source coupled with AC voltage source
- Variable DC supply (0 - 250V)
- Multimeter capable of measuring AC and DC current and voltage (0-440V AC, 0-250V DC)
- Timer
- Test switches
- Suitable electrical test leads
- Continuity tester

20.4.3 ADVISORY TEST EQUIPMENT

Advisory test equipment may be required for extended commissioning procedures:

- Current clamp meter
- Multi-finger test plug:
  - P992 for test block type P991
  - MMLB for test block type MMLG blocks
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- KITZ K-Bus - EIA(RS)232 protocol converter for testing EIA(RS)485 K-Bus port
- EIA(RS)485 to EIA(RS)232 converter for testing EIA(RS)485 Courier/MODBUS/IEC60870-5-103/DNP3 port
- A portable printer (for printing a setting record from the portable PC) and or writeable, detachable memory device
- Phase angle meter
- Phase rotation meter
- Fibre-optic power meter.
- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 µm or 62.5µm terminated with BFOC (ST) 2.5 connectors for testing the fibre-optic RP1 port

20.5 PRODUCT CHECKS

These product checks are designed to ensure that the device has not been physically damaged prior to commissioning, is functioning correctly and that all input quantity measurements are within the stated tolerances.

If the application-specific settings have been applied to the IED prior to commissioning, you should make a copy of the settings. This will allow you to restore them at a later date if necessary. This can be done by:

- Obtaining a setting file from the customer.
- Extracting the settings from the IED itself, using a portable PC with appropriate setting software.

If the customer has changed the password that prevents unauthorised changes to some of the settings, either the revised password should be provided, or the original password restored before testing.

Note:
If the password has been lost, a recovery password can be obtained from GE Vernova.

20.5.1 PRODUCT CHECKS WITH THE IED DE-ENERGISED

Warning:
The following group of tests should be carried out without the auxiliary supply being applied to the IED and, if applicable, with the trip circuit isolated.

The current and voltage transformer connections must be isolated from the IED for these checks. If a P991 test block is provided, the required isolation can be achieved by inserting test plug type P992. This open circuits all wiring routed through the test block.

Before inserting the test plug, you should check the scheme diagram to ensure that this will not cause damage or a safety hazard (the test block may, for example, be associated with protection current transformer circuits). The sockets in the test plug, which correspond to the current transformer secondary windings, must be linked before the test plug is inserted into the test block.

Warning:
Never open-circuit the secondary circuit of a current transformer since the high voltage produced may be lethal and could damage insulation.

If a test block is not provided, the voltage transformer supply to the IED should be isolated by means of the panel links or connecting blocks. The line current transformers should be short-circuited and disconnected from the IED terminals. Where means of isolating the auxiliary supply and trip circuit (for example isolation links, fuses and MCB) are provided, these should be used. If this is not possible, the wiring to these circuits must be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

20.5.1.1 VISUAL INSPECTION

Warning:
Check the rating information under the top access cover on the front of the IED.

Warning:
Check that the IED being tested is correct for the line or circuit.

Warning:
Record the circuit reference and system details.

Warning:
Check the CT secondary current rating and record the CT tap which is in use.

Carefully examine the IED to see that no physical damage has occurred since installation.

Ensure that the case earthing connections (bottom left-hand corner at the rear of the IED case) are used to connect the IED to a local earth bar using an adequate conductor.

20.5.1.2 CURRENT TRANSFORMER SHORTING CONTACTS

Check the current transformer shorting contacts to ensure that they close when the heavy-duty terminal block is disconnected from the current input board.

The heavy-duty terminal blocks are fastened to the rear panel using four crosshead screws. These are located two at the top and two at the bottom.

Note:
Use a magnetic bladed screwdriver to minimise the risk of the screws being left in the terminal block or lost.

Pull the terminal block away from the rear of the case and check with a continuity tester that all the shorting switches being used are closed.

20.5.1.3 INSULATION

Insulation resistance tests are only necessary during commissioning if explicitly requested.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a DC voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the IED.

20.5.1.4 EXTERNAL WIRING

Caution:
Check that the external wiring is correct according to the relevant IED and scheme diagrams. Ensure that phasing/phase rotation appears to be as expected.

20.5.1.5 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states:

Terminals	Contact State with Product De-energised
11 - 12 on power supply board	Closed
13 - 14 on power supply board	Open

20.5.1.6 POWER SUPPLY

Depending on its nominal supply rating, the IED can be operated from either a DC only or an AC/DC auxiliary supply. The incoming voltage must be within the operating range specified below.

Without energising the IED measure the auxiliary supply to ensure it is within the operating range.

Nominal supply rating DC	Nominal Supply Rating AC RMS	DC Operating Range	AC Operating Range
24 - 54 V	N/A	19 to 65 V	N/A
48 - 125 V	30 - 100 V	37 to 150 V	24 - 110 V
110 - 250 V	100 - 240 V	87 to 300 V	80 to 265 V

Note:
The IED can withstand an AC ripple of up to 15% of the upper rated voltage on the DC auxiliary supply.

Warning:
Do not energise the IED or interface unit using the battery charger with the battery disconnected as this can irreparably damage the power supply circuitry.

Caution:
Energise the IED only if the auxiliary supply is within the specified operating ranges. If a test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the IED.

20.5.2 PXXX_CI_PRODUCTCHECKSENERGISED

Warning:
The current and voltage transformer connections must remain isolated from the IED for these checks. The trip circuit should also remain isolated to prevent accidental operation of the associated circuit breaker.

The following group of tests verifies that the IED hardware and software is functioning correctly and should be carried out with the supply applied to the IED.

20.5.2.1 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states when energised and healthy.

Terminals	Contact State with Product Energised
11 - 12 on power supply board	Open
13 - 14 on power supply board	Closed

20.5.2.2 TEST GRAPHICAL HMI

The Graphical HMI is designed to operate in a wide range of substation ambient temperatures. For this purpose, the IEDs have an ***LCD Brightness*** setting. The brightness is factory pre-set, but it may be necessary to adjust the contrast to give the best in-service display.

To change the contrast, you can increment or decrement the ***LCD Brightness*** cell in the *CONFIGURATION* column.

Caution:
Before applying a brightness setting, make sure that it will not make the display so light or dark that the menu text becomes unreadable. It is possible to restore the visibility of a display by downloading a setting file, and setting the LCD Brightness within the typical range of 7 - 11.

20.5.2.3 DATE AND TIME

The date and time is stored in memory, which is backed up by a supercapacitor.

The method for setting the date and time depends on whether an IRIG-B signal is being used or not. The IRIG-B signal will override the time, day and month settings, but not the initial year setting. For this reason, you must ensure you set the correct year, even if the device is using IRIG-B to maintain the internal clock.

You set the Date and Time by one of the following methods:

- Using the front panel to set the ***Date and Time*** cells respectively
- By sending a courier command to the ***Date/Time*** cell (Courier reference 0801)

Note:
If the auxiliary supply fails, the time and date will be maintained by the supercapacitor. Therefore, when the auxiliary supply is restored, you should not have to set the time and date again. To test this, remove the IRIG-B signal, and then remove the auxiliary supply. Leave the device de-energised for approximately 30 seconds. On re energisation, the time should be correct.

When using IRIG-B to maintain the clock, the IED must first be connected to the satellite clock equipment (usually an RT430), which should be energised and functioning.

1. Set the IRIG-B Sync cell in the *DATE AND TIME* column to `Enabled`.
2. Ensure the IED is receiving the IRIG-B signal by checking that cell IRIG-B Status reads `Active`.
3. Once the IRIG-B signal is active, adjust the time offset of the universal co coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.
4. Check that the time, date and month are correct in the Date/Time cell. The IRIG-B signal does not contain the current year so it will need to be set manually in this cell.
5. Reconnect the IRIG-B signal.

If the time and date is not being maintained by an IRIG-B signal, ensure that the IRIG-B Sync cell in the *DATE AND TIME* column is set to `Disabled`.

1. Set the date and time to the correct local time and date using Date/Time cell or using the serial protocol.

20.5.2.4 TEST LEDS

On power-up, all LEDs should first flash yellow. Following this, the green "Healthy" LED should illuminate indicating that the device is healthy.

The IED's non-volatile memory stores the states of the alarm, the trip, and the user-programmable LED indicators (if configured to latch). These indicators may also illuminate when the auxiliary supply is applied.

If any of these LEDs are ON then they should be reset before proceeding with further testing. If the LEDs successfully reset (the LED goes off), no testing is needed for that LED because it is obviously operational.

20.5.2.5 TEST ALARM AND OUT-OF-SERVICE LEDS

The alarm and out of service LEDs can be tested using the *COMMISSION TESTS* menu column.

1. Set the ***Test Mode*** cell to `Contacts Blocked`.
2. Check that the out of service LED illuminates continuously and the alarm LED flashes.

It is not necessary to return the ***Test Mode*** cell to `Disabled` at this stage because the test mode will be required for later tests.

20.5.2.6 TEST TRIP LED

The trip LED can be tested by initiating a manual circuit breaker trip. However, the trip LED will operate during the setting checks performed later. Therefore no further testing of the trip LED is required at this stage.

20.5.2.7 TEST USER-PROGRAMMABLE LEDS

To test these LEDs, set the Test LEDs cell to `Apply Test`. Check that all user-programmable LEDs illuminate.

20.5.2.8 TEST FIELD VOLTAGE SUPPLY

The IED generates a field voltage of nominally 48 V that can be used to energise the opto-inputs (alternatively the substation battery may be used).

1. Measure the field voltage across the terminals 7 and 9 of the power supply terminal block
2. Check that the field voltage is within the range 40 V to 60 V when no load is connected and that the polarity is correct.
3. Repeat for terminals 8 and 10.

20.5.2.9 TEST OPTO-INPUTS

This test checks that all the opto-inputs on the IED are functioning correctly.

The opto-inputs should be energised one at a time. For terminal numbers, please see the external connection diagrams in the "Wiring Diagrams" chapter. Ensuring correct polarity, connect the supply voltage to the appropriate terminals for the input being tested.

The status of each opto-input can be viewed using either the ***Opto I/P Status*** cell in the *SYSTEM DATA* column, or the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column.

A '1' indicates an energised input and a '0' indicates a de-energised input. When each opto-input is energised, one of the characters on the bottom line of the display changes to indicate the new state of the input.

20.5.2.10 TEST OUTPUT RELAYS

This test checks that all the output relays are functioning correctly.

1. Ensure that the IED is still in test mode by viewing the ***Test Mode*** cell in the *COMMISSION TESTS* column. Ensure that it is set to `Contacts Blocked`.
2. The output relays should be energised one at a time. To select output relay 1 for testing, set the Test Pattern cell as appropriate.
3. Connect a continuity tester across the terminals corresponding to output relay 1 as shown in the external connection diagram.
4. To operate the output relay set the Contact Test cell to `Apply Test`.
5. Check the operation with the continuity tester.

6. Measure the resistance of the contacts in the closed state.
7. Reset the output relay by setting the Contact Test cell to `Remove Test`.
8. Repeat the test for the remaining output relays.
9. Return the IED to service by setting the Test Mode cell in the *COMMISSION TESTS* menu to `Disabled`.

20.5.2.11 TEST SERIAL COMMUNICATION PORT RP1

You need only perform this test if the IED is to be accessed from a remote location with a permanent serial connection to the communications port. The scope of this test does not extend to verifying operation with connected equipment beyond any supplied protocol converter. It verifies operation of the rear communication port (and if applicable the protocol converter) and varies according to the protocol fitted.

20.5.2.11.1 CHECK PHYSICAL CONNECTIVITY

The rear communication port RP1 is presented on terminals 16, 17 and 18 of the power supply terminal block. Screened twisted pair cable is used to make a connection to the port. The cable screen should be connected to pin 16 and pins 17 and 18 are for the communication signal:

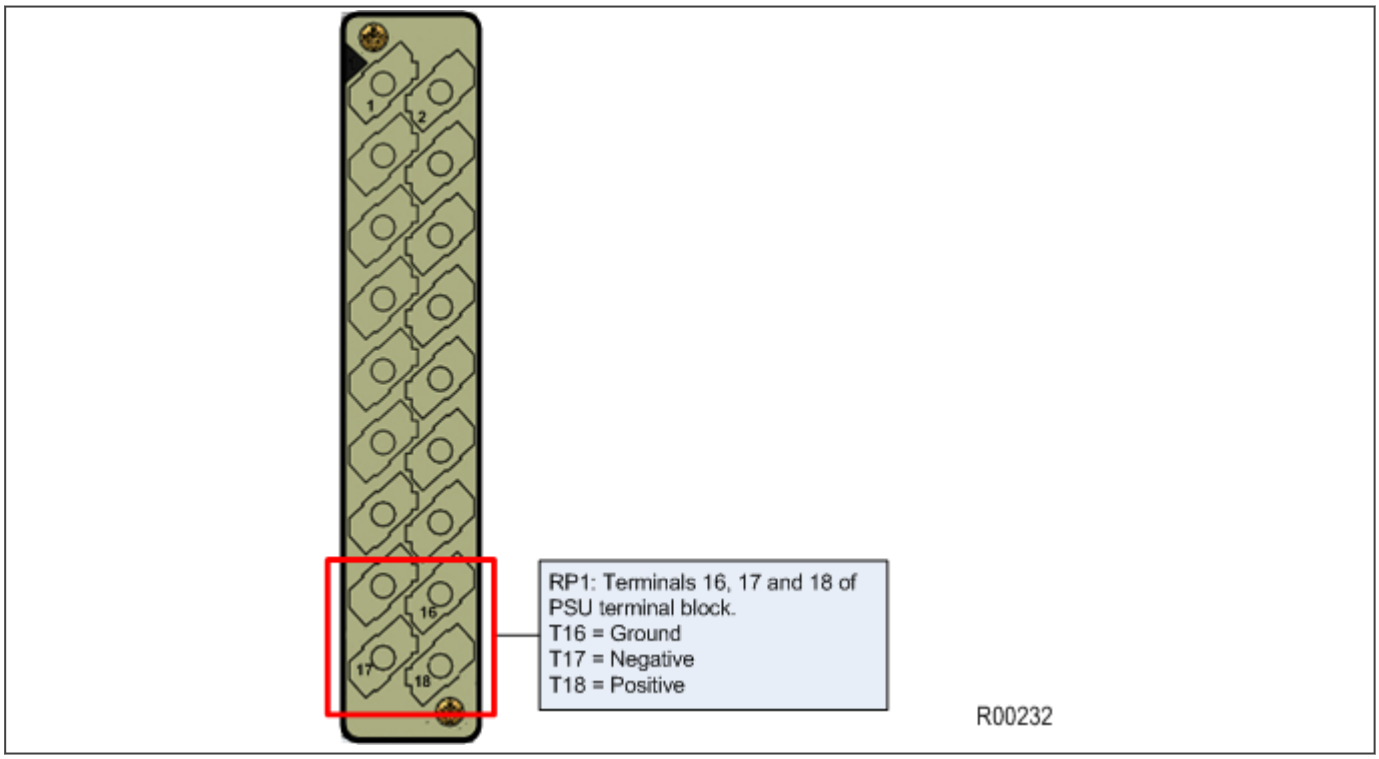


Figure 249: RP1 physical connection

For K-Bus applications, pins 17 and 18 are not polarity sensitive and it does not matter which way round the wires are connected. EIA(RS)485 is polarity sensitive, so you must ensure the wires are connected the correct way round (pin 18 is positive, pin 17 is negative).

If K-Bus is being used, a Kitz protocol converter (KITZ101, KITZ102 OR KITZ201) will have been installed to convert the K-Bus signals into RS232. Likewise, if RS485 is being used, an RS485-RS232 converter will have been installed. In the case where a protocol converter is being used, a laptop PC running appropriate software (such as MiCOM S1 Agile) can be connected to the incoming side of the protocol converter. An example for K-bus to RS232 conversion is shown below. RS485 to RS232 would follow the same principle, only using a RS485-RS232 converter. Most modern laptops have USB ports, so it is likely you will also require a RS232 to USB converter too.

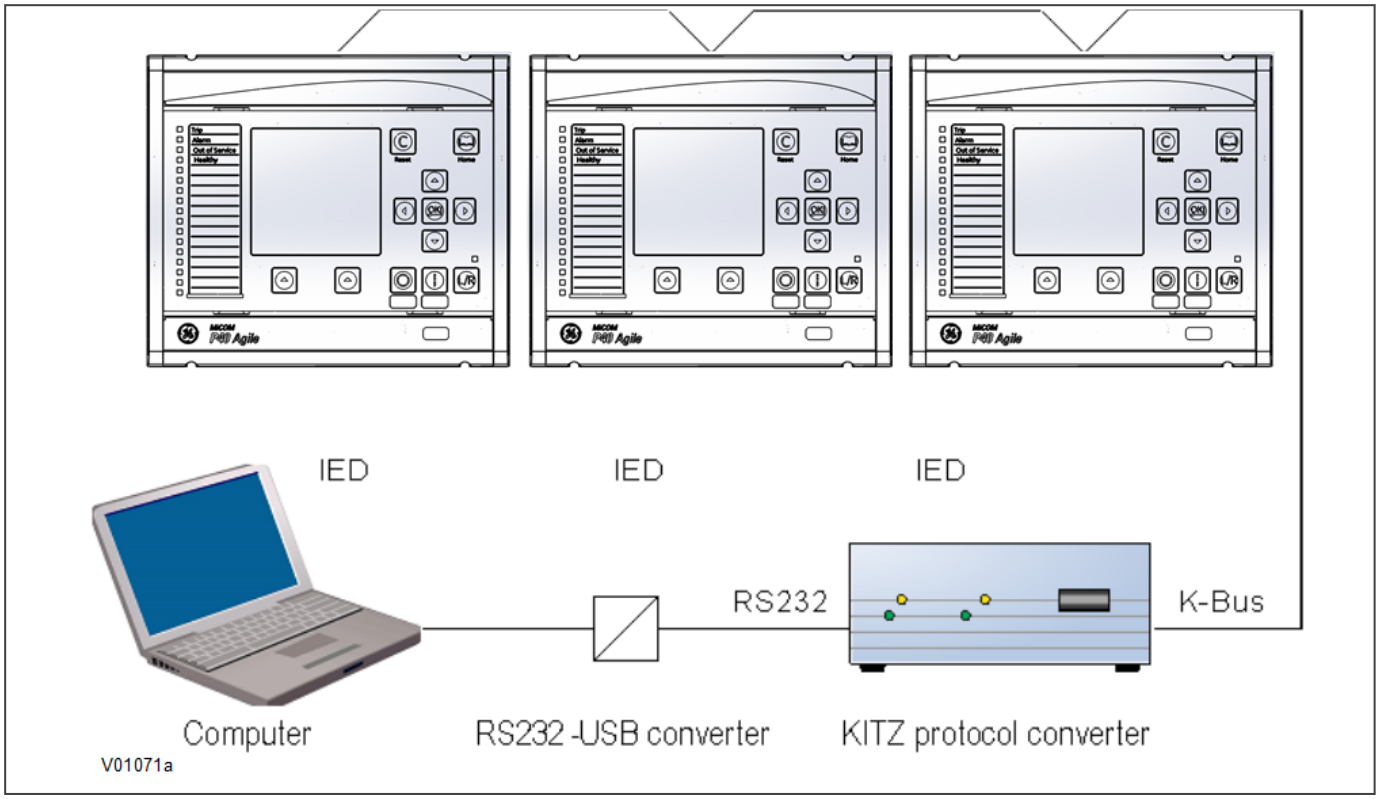


Figure 250: Remote communication using K-bus

Fibre Connection

Some models have an optional fibre optic communications port fitted (on a separate communications board). The communications port to be used is selected by setting the Physical Link cell in the *COMMUNICATIONS* column, the values being `Copper` or `K-Bus` for the RS485/K-bus port and `Fibre Optic` for the fibre optic port.

20.5.2.11.2 CHECK LOGICAL CONNECTIVITY

The logical connectivity depends on the chosen data protocol, but the principles of testing remain the same for all protocol variants:

1. Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter.
2. For Courier models, ensure that you have set the correct RP1 address
3. Check that communications can be established with this IED using the portable PC/Master Station.

20.5.2.12 TEST SERIAL COMMUNICATION PORT RP2

RP2 is an optional second serial port board providing additional serial connectivity. It provides two 9-pin D-type serial port connectors SK4 and SK5. Both ports are configured as DTE (Date Terminal Equipment) ports. That means they can be connected to communications equipment such as a modem with a straight-through cable.

SK4 can be configured as an EIA(RS232), EIA(RS485), or K-Bus connection for Courier protocol only, whilst SK5 is fixed to EIA(RS)232 for InterMiCOM signalling only.

It is not the intention of this test to verify the operation of the complete communication link between the IED and the remote location, just the IED's rear communication port and, if applicable, the protocol converter.

The only checks that need to be made are as follows:

1. Set the ***RP2 Port Config*** cell in the *COMMUNICATIONS* column to the required physical protocol; (K-Bus, EIA(RS)485, or EIA(RS)232.
2. Set the IED's Courier address to the correct value (it must be between 1 and 254).

20.5.2.13 TEST ETHERNET COMMUNICATION

For products that employ Ethernet communications, we recommend that testing be limited to a visual check that the correct ports are fitted and that there is no sign of physical damage.

If there is no board fitted or the board is faulty, a NIC link alarm will be raised (providing this option has been set in the ***NIC Link Report*** cell in the *COMMUNICATIONS* column).

20.5.3 SECONDARY INJECTION TESTS

Secondary injection testing is carried out to verify the integrity of the VT and CT readings. All devices leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required, you must set this in the Frequency cell in the *SYSTEM DATA* column.

The PMU must be installed and connected to a 1pps fibre optic synchronising signal and a demodulated IRIG-B signal, provided by a device such as a REASON RT430.

Connect the current and voltage outputs of the test set to the appropriate terminals of the first voltage and current channel and apply nominal voltage and current with the current lagging the voltage by 90 degrees.

20.5.3.1 TEST CURRENT INPUTS

This test verifies that the current measurement inputs are configured correctly.

1. Using secondary injection test equipment such as an Omicron, apply and measure nominal rated current to each CT in turn.
2. Check its magnitude using a multi-meter or test set readout. Check this value against the value displayed on the HMI panel (usually in *MEASUREMENTS 1* column).
3. Record the displayed value. The measured current values will either be in primary or secondary Amperes. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be equal to the applied current multiplied by the corresponding current transformer ratio (set in the *CT AND VT RATIOS* column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied current.

> *Note:*
> *If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.*

The measurement accuracy of the IED is +/- 1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

20.5.3.2 TEST VOLTAGE INPUTS

This test verifies that the voltage measurement inputs are configured correctly.

1. Using secondary injection test equipment, apply and measure the rated voltage to each voltage transformer input in turn.
2. Check its magnitude using a multimeter or test set readout. Check this value against the value displayed on the HMI panel (usually in *MEASUREMENTS 1* column).
3. Record the value displayed. The measured voltage values will either be in primary or secondary Volts. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be equal to the applied voltage multiplied by the corresponding voltage transformer ratio (set in the *CT AND VT RATIOS* column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied voltage.

Note:
If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.

The measurement accuracy of the IED is +/- 1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

20.6 ELECTRICAL INTERMICOM COMMUNICATION LOOPBACK

If the IED is used in a scheme with standard InterMiCOM communication (Electrical Teleprotection), you need to configure a loopback for testing purposes.

20.6.1 SETTING UP THE LOOPBACK

The communication path may include various connectors and signal converters before leaving the substation. We therefore advise making the loopback as close as possible to where the communication link leaves the substation. This way, as much of the wiring as possible and all associated communication signal converters are included in the test.

1. Set *CONFIGURATION* > ***InterMiCOM*** to `Enabled`.
2. Set *INTERMICOM COMMS* > ***Ch Statistics*** and ***Ch Diagnostics*** to `Visible`.
3. Check that *INTERMICOM COMMS* > ***IM H/W Status*** displays OK. This means the InterMiCOM hardware is fitted and initialised.

20.6.2 LOOPBACK TEST

INTERMICOM COMMS > ***Loopback Mode*** allows you to test the InterMiCOM channel. In normal service it must be disabled. *INTERMICOM COMMS* > ***Loopback Status*** shows the status of the InterMiCOM loopback mode.

Note:
If INTERMICOM COMMS > ***Loopback Mode*** *is set to* `Internal`*, only the internal software of the device is checked. This is useful for testing functionality if no communications connections are made. Use the 'External' setting during commissioning because it checks both the software and hardware. When the IED is switched into either Internal or External Loopback Mode it automatically inhibits InterMiCOM messages to the PSL by setting all eight InterMiCOM message command states to zero.*

Set *INTERMICOM COMMS* > ***Loopback Mode*** to `External` and form a communications loopback by connecting the transmit signal (pin 2) to the receive signal (pin 3).

Note:
The DCD signal must be held high (by connecting pin 1 to pin 4) if the connected equipment does not support DCD.

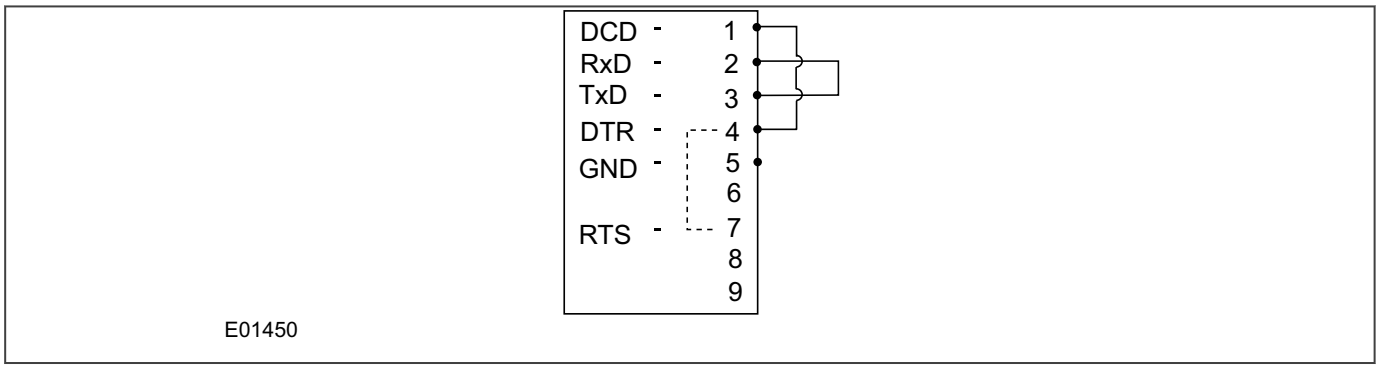


Figure 251: InterMicom loopback testing

The loopback mode is shown on the front panel by an Alarm LED and the message IM Loopback on the LCD.

Check that all connections are correct and the software is working correctly.

Check that *INTERMICOM COMMS* > ***Loopback Status*** shows OK.

20.6.2.1 INTERMICOM COMMAND BITS

To test the InterMiCOM command bits, go to the *INTERMICOM COMMS* column and do the following:

1. Enter any test pattern in the ***Test Pattern*** cell in the by scrolling through and changing selected bits between 1 and 0. The entered pattern is transmitted through the loopback.
2. Check that the ***IM Output Status*** cell matches the applied Test Pattern.
3. Check that all 8 bits in the ***IM Input Status*** cell are zero.

20.6.2.2 INTERMICOM CHANNEL DIAGNOSTICS

Check that the following cells in the *INTERMICOM COMMS* column all read **OK**.

- ***Data CD Status***
- ***FrameSync Status***
- ***Message Status***
- ***Channel Status***

20.6.2.3 SIMULATING A CHANNEL FAILURE

1. Simulate a failure of the communications link by breaking a connection and checking that some of these cells show **Fail**.
2. Restore the communications loopback and ensure that the four diagnostic cells display **OK.**

> *Note:*
> *Some or all of these cells show **Fail** depending on the communications configuration and the way the link has failed.*

20.7 SETTING CHECKS

The setting checks ensure that all of the application-specific settings (both the IED's function and Programmable Scheme Logic settings) have been correctly applied.

> *Note:*
> *If applicable, the trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.*

20.7.1 APPLY APPLICATION-SPECIFIC SETTINGS

There are two different methods of applying the settings to the IED

- Transferring settings to the IED from a pre-prepared setting file using MiCOM S1 Agile
- Enter the settings manually using the IED's front panel HMI

20.7.1.1 TRANSFERRING SETTINGS FROM A SETTINGS FILE

This is the preferred method for transferring function settings. It is much faster and there is a lower margin for error.

1. Connect a PC running the Settings Application Software to the IED's front port, or a rear Ethernet port. Alternatively connect to the rear Courier communications port, using a KITZ protocol converter if necessary.
2. Power on the IED
3. Enter the IP address of the device if it is Ethernet enabled
4. Right-click the appropriate device name in the System Explorer pane and select **Send**
5. In the **Send to** dialog select the setting files and click **Send**

> *Note:*
> *The device name may not already exist in the system shown in **System Explorer**. In this case, perform a **Quick Connect** to the IED, then manually add the settings file to the device name in the system. Refer to the Settings Application Software help for details of how to do this.*

20.7.1.2 ENTERING SETTINGS USING THE HMI

1. Starting at the default display, press the Down cursor key to show the first column heading.
2. Use the horizontal cursor keys to select the required column heading.
3. Use the vertical cursor keys to view the setting data in the column.
4. To return to the column header, either press the Up cursor key for a second or so, or press the **Cancel** key once. It is only possible to move across columns at the column heading level.
5. To return to the default display, press the Up cursor key or the Cancel key from any of the column headings. If you use the auto-repeat function of the Up cursor key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
6. To change the value of a setting, go to the relevant cell in the menu, then press the **Enter** key to change the cell value. A flashing cursor on the LCD shows that the value can be changed. You may be prompted for a password first.
7. To change the setting value, press the vertical cursor keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the left and right cursor keys.

8. Press the **Enter** key to confirm the new setting value or the **Clear** key to discard it. The new setting is automatically discarded if it is not confirmed within 15 seconds.
9. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used. When all required changes have been entered, return to the column heading level and press the down cursor key. Before returning to the default display, the following prompt appears.

```
Update settings?
ENTER or CLEAR
```

10. Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.

Note:
If the menu time-out occurs before the setting changes have been confirmed, the setting values are also discarded.
Control and support settings are updated immediately after they are entered, without the Update settings prompt.
It is not possible to change the PSL using the IED's front panel HMI.

Caution:
Where the installation needs application-specific PSL, the relevant .psl files, must be transferred to the IED, for each and every setting group that will be used. If you do not do this, the factory default PSL will still be resident. This may have severe operational and safety consequences.

20.8 IEC 61850 EDITION 2 TESTING

20.8.1 USING IEC 61850 EDITION 2 TEST MODES

In a conventional substation, functionality typically resides in a single device. It is usually easy to physically isolate these functions, as the hardwired connects can simply be removed. Within a digital substation architecture however, functions may be distributed across many devices. This makes isolation of these functions difficult, because there are no physical wires that can be disconnected on an Ethernet network. Logical isolation of the various functions is therefore necessary.

With IEDs that support IEC 61850 Edition 2, it is possible to use a test mode to conduct online testing. The advantages of this are as follows:

- The IED can be placed into test mode, to allow testing the IED using test input signals, and with all protection functions and output contacts active.
- The IED can be placed into test/blocked mode, to allow testing the IED using test input signals, and with all protection functions active but output contacts disabled.
- GOOSE message outputs are tagged so that receiving devices can recognise they are test signals.
- An IED receiving simulated GOOSE or Sampled Value messages from test devices can differentiate these from normal process messages, and respond appropriately.

20.8.1.1 IED TEST MODE BEHAVIOUR

IEC 61850 Edition 2 defines how the IED responds to test messages in the IED test modes, and whether the relay output contacts are activated or not.

You can select the mode of operation of the P40 IED by:

- Using the front panel HMI, with the setting ***IED Test Mode*** under the *COMMISSION TESTS* column.
- Using an IEC 61850 MMS control service to ***System/LLN0.Mod***
- Using an opto-input via PSL with the signal ***Block Contacts***

The following table summarises the P40 IED behaviour under the different modes:

IED Test Mode Setting	IEC 61850 Mod	Result
Disabled	on	• Normal IED behaviour • IED only responds to incoming GOOSE and SV messages with quality q.test = false
Test	test	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are still active • IEC 61850 message outputs have 'quality' q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true
Contacts Blocked	test/blocked	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are disabled • IEC 61850 message outputs have quality q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true

Setting the Test or Contacts Blocked mode puts the whole IED into test mode. The IEC 61850 data object ***Beh*** in all Logical Nodes (except LPHD and any protection Logical Nodes that have Beh = 5 (off) due to the function being disabled) will be set to 3 (test) or 4 (test/blocked) as applicable.

20.8.2 SIMULATED INPUT BEHAVIOUR

Simulated GOOSE messages and sampled value streams can be used during testing.

The ***Subscriber Sim*** setting in the *COMMISSION TESTS* column controls whether a device listens to simulated signals or to real ones. An IEC 61850 control service to System/LPHD.Sim can also be used to change this value.

The device may be presented with both real signals and test signals. An internal state machine is used to control how the device switches between signals:

- The IED will continue subscribing to the 'real' GOOSE1 (in green) until it receives the first simulated GOOSE 1 (in red). This will initiate subscription changeover.
- After changeover to this new state, the IED will continue to subscribe to the simulated GOOSE 1 message (in red). Even if this simulated GOOSE 1 message disappears, the real GOOSE 1 message (in green) will still not be processed. This means all Virtual Inputs derived from the GOOSE 1 message will go to their default state.
- The only way to bring the IED out of this state is to set the ***Subscriber Sim*** setting back to False. The IED will then immediately stop processing the simulated messages and start processing real messages again.
- During above steps, IED1 will continuously process the real GOOSE 2 and GOOSE 3 messages as normal because it has not received any simulated messages for these that would initiate a changeover.

The process is represented in the following figure:

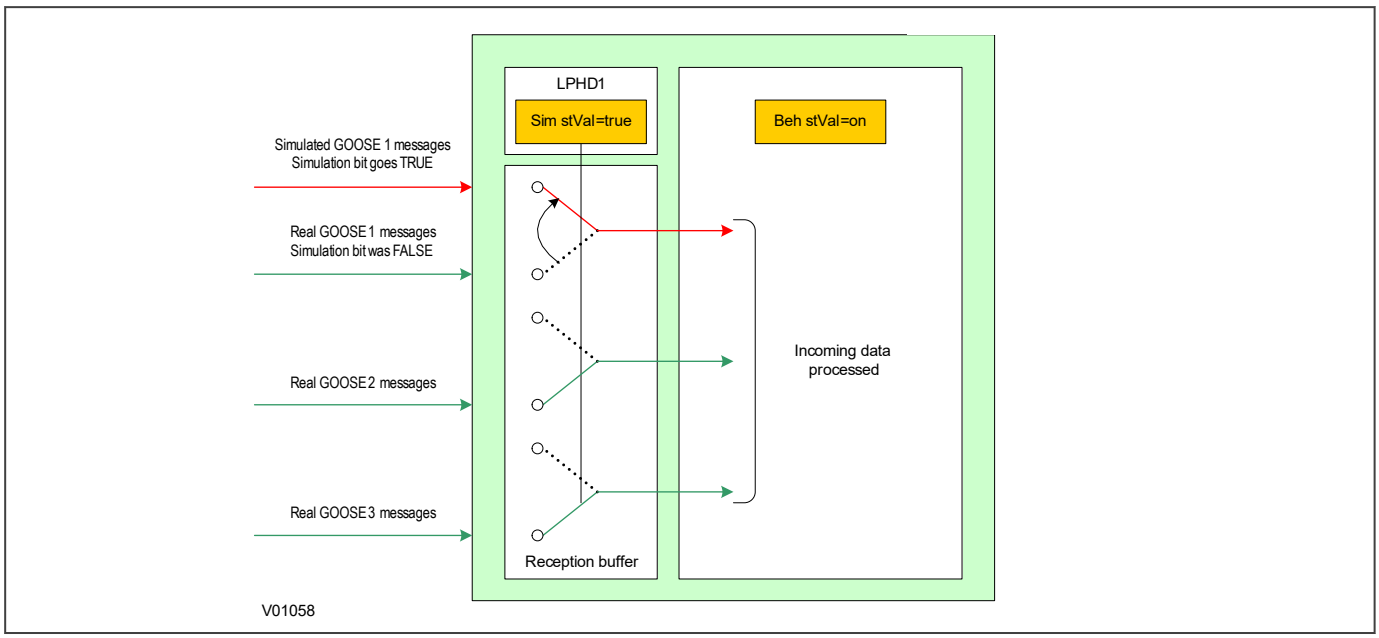


Figure 252: Simulated input behaviour

20.8.3 TESTING EXAMPLES

These examples show how you test the IED with and without simulated values. Depending on the IED Test Mode, it may respond by operating plant (for example by tripping the circuit breaker) or it may not operate plant.

20.8.3.1 TEST PROCEDURE FOR REAL VALUES

This procedure is for testing with real values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/eh***, and check that it shows `Test-blocked`
3. Set device into Simulation Listening Mode
   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Disabled`
4. Inject real signals using a test device connected to the merging units. The device will continue to listen to 'real' GOOSE messages and ignore simulated messages received.
5. Verify function based on test signal outputs
   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

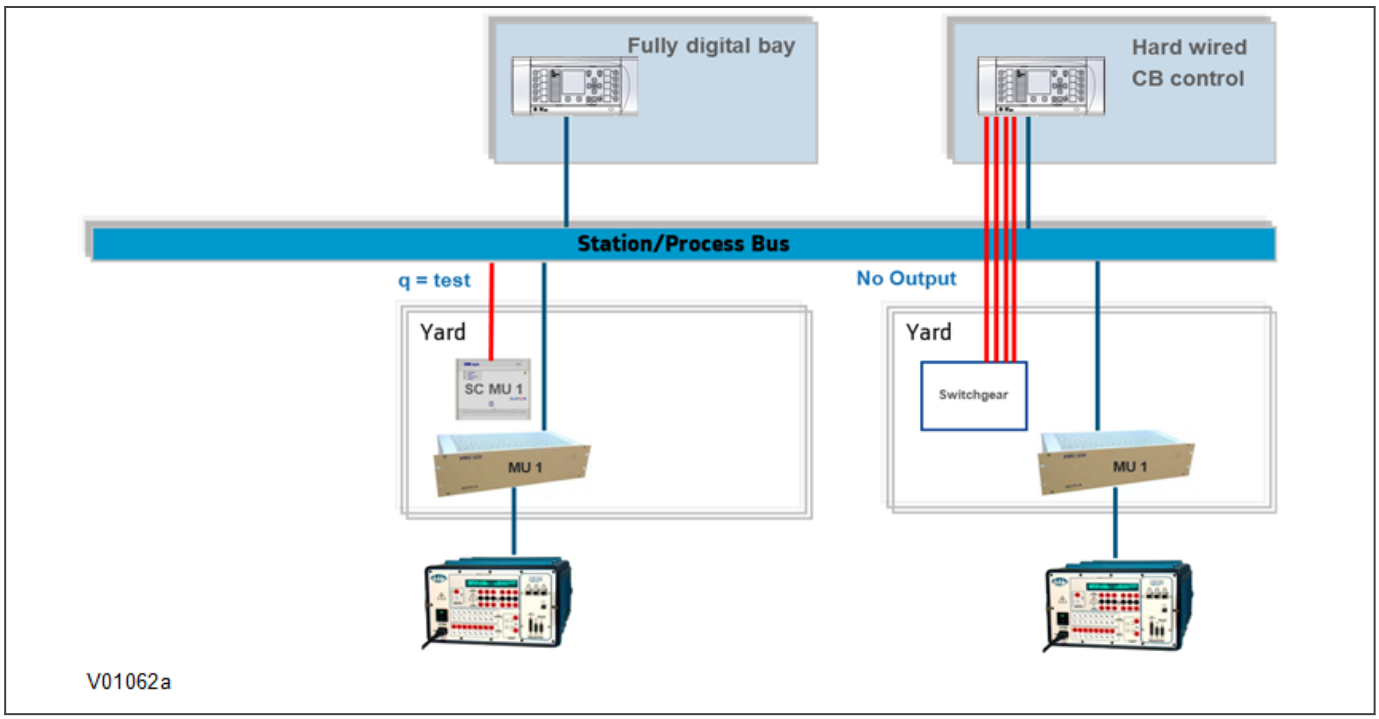


Figure 253: Test example 1

20.8.3.2 TEST PROCEDURE FOR SIMULATED VALUES - NO PLANT

This procedure is for testing with simulated values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `test-blocked`

3. Set device into Simulation Listening Mode

   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Enabled`

4. Inject simulated signals using a test device connected to the Ethernet network. The device will continue to listen to 'real' GOOSE messages until a simulated message is received. Once the simulated messages are received, the corresponding 'real' messages are ignored until the device is taken out of test mode. Each message is treated separately, but sampled values are considered as a single message.

5. Verify function based on test signal outputs

   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

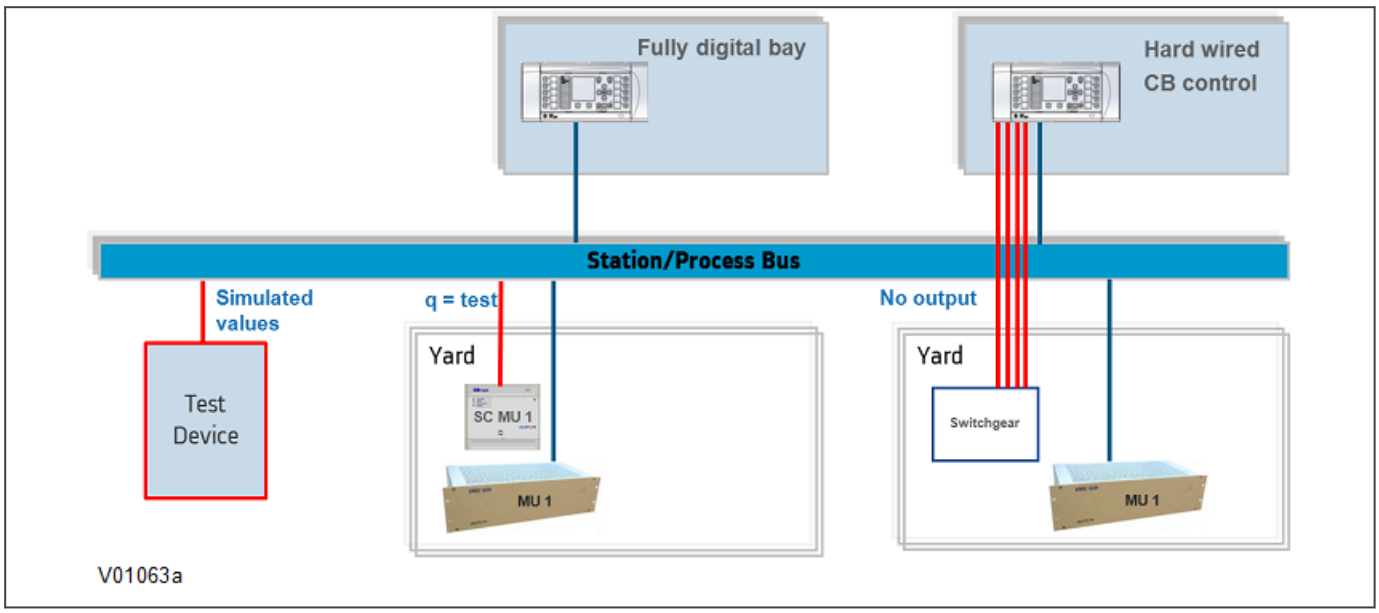


Figure 254: Test example 2

20.8.3.3 TEST PROCEDURE FOR SIMULATED VALUES - WITH PLANT

This procedure is for testing with simulated values with operating plant.

1. Set device into 'Contacts Blocked' Mode

   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Test`

2. Confirm new behaviour has been enabled

   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `Test`

3. Set device into Simulation Listening Mode

   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Enabled`

4. Inject simulated signals using a test device connected to the Ethernet network.

   The device will continue to listen to 'real' GOOSE messages until a simulated message is received. Once the simulated messages are received, the corresponding 'real' messages are ignored until the device is taken out of IED test mode. Each message is treated separately, but sampled values are considered as a single message.

5. Verify function based on test signal outputs.

   Binary outputs (e.g. CB trips) will operate as normal. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram:

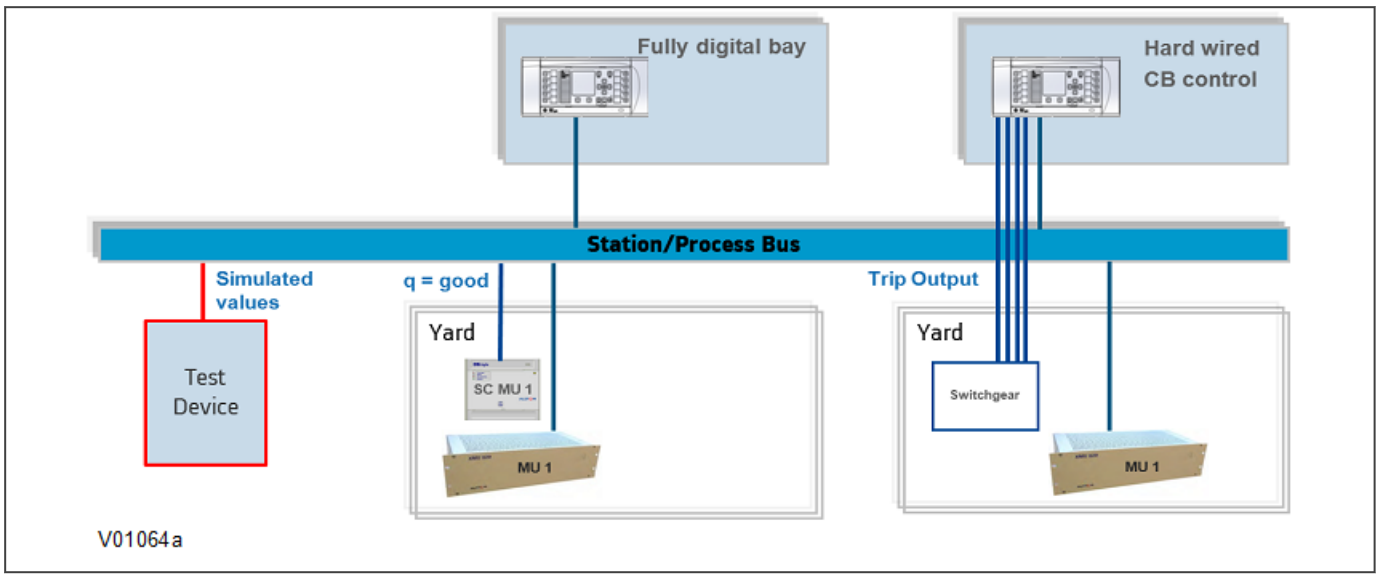


Figure 255: Test example 3

20.8.3.4 CONTACT TEST

The ***Apply Test*** command in this cell is used to change the state of the contacts set for operation.

If the device has been put into 'Contact Blocked' mode using an input signal (via the ***Block Contacts*** DDB signal) then the ***Apply Test*** command will not execute. This is to prevent a device that has been blocked by an external process having its contacts operated by a local operator using the HMI.

If the ***Block Contacts*** DDB is not set and the ***Apply Test*** command in this cell is issued, contacts change state and the command text on the LCD changes to `No Operation`. The contacts remain in the Test state until reset by issuing the ***Remove Test*** command. The command text on the LCD shows `No Operation` after the ***Remove Test*** command has been issued.

> *Note:*
> *When the **IED Test Mode** cell is set to Contacts Blocked, the **Relay O/P Status** cell does not show the current status of the output relays so cannot be used to confirm operation of the output relays. Therefore it is necessary to monitor the state of each contact in turn.*

20.9 PROTECTION TIMING CHECKS

There is no need to check every protection function. Only one protection function needs to be checked as the purpose is to verify the timing on the processor is functioning correctly.

20.9.1 OVERCURRENT CHECK

If the overcurrent protection function is being used, test the overcurrent protection for stage 1.

1. Check for any possible dependency conditions and simulate as appropriate.
2. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
3. Make a note of which elements need to be re-enabled after testing.
4. Connect the test circuit.
5. Perform the test.
6. Check the operating time.

20.9.2 CONNECTING THE TEST CIRCUIT

1. Use the PSL to determine which output relay will operate when an overcurrent trip occurs.
2. Use the output relay assigned to ***Trip Output A***.
3. Use the PSL to map the protection stage under test directly to an output relay.

> *Note:*
> *If using the default PSL, use output relay 3 as this is already mapped to the DDB signal* ***Trip Command Out****.*

4. Connect the output relay so that its operation will trip the test set and stop the timer.
5. Connect the current output of the test set to the A-phase current transformer input.

   If the ***I>1 Directional*** cell in the *OVERCURRENT* column is set to `Directional Fwd`, the current should flow out of terminal 2. If set to `Directional Rev`, it should flow into terminal 2.

   If the ***I>1 Directional*** cell in the *OVERCURRENT* column has been set to `Directional Fwd` or `Directional Rev`, the rated voltage should be applied to terminals 20 and 21.
6. Ensure that the timer starts when the current is applied.

> *Note:*
> *If the timer does not stop when the current is applied and stage 1 has been set for directional operation, the connections may be incorrect for the direction of operation set. Try again with the current connections reversed.*

20.9.3 PERFORMING THE TEST

1. Ensure that the timer is reset.
2. Apply a current of twice the setting shown in the ***I>1 Current Set*** cell in the *OVERCURRENT* column.
3. Note the time displayed when the timer stops.
4. Check that the red trip LED has illuminated.

20.9.4 CHECK THE OPERATING TIME

Check that the operating time recorded by the timer is within the range shown below.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

Characteristic	Operating Time at Twice Current Setting and Time Multiplier/Time Dial Setting of 1.0	
	Nominal (seconds)	Range (seconds)
DT	I>1 Time Delay setting	Setting ±2%
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	24.67 - 28.67
UK LT Inverse	120.00	114.00 - 126.00
IEEE M Inverse	3.8	3.61 - 4.0
IEEE V Inverse	7.03	6.68 - 7.38
IEEE E Inverse	9.50	9.02 - 9.97
US Inverse	2.16	2.05 - 2.27
US ST Inverse	12.12	11.51 - 12.73

Note:
With the exception of the definite time characteristic, the operating times given are for a Time Multiplier Setting (TMS) or Time Dial Setting (TDS) of 1. For other values of TMS or TDS, the values need to be modified accordingly.
For definite time and inverse characteristics there is an additional delay of up to 0.02 second and 0.08 second respectively. You may need to add this the IED's acceptable range of operating times.

Caution:
On completion of the tests, you must restore all settings to customer specifications.

20.10 SYSTEM CHECK AND CHECK SYNCHRONISM

This function performs a comparison between the line voltage and the bus voltage.

There are two voltage inputs to compare:

- one from the voltage transformer input from the line side of the circuit breaker (Main VT)
- one from the VT on the bus side of the circuit breaker (CS VT).

In most cases the line VT input is three phase, whereas the bus VTs are single phase.

The bus VT inputs are normally single phase so the system voltage checks are made on single phases and the VT may be connected to either a phase-to-phase or phase to neutral voltage.

For these reasons, the IED has to be programmed with the appropriate connection. The ***CS Input*** setting in the *CT AND VT RATIOS* column can be set to A-N, B-N, C-N, A-B, B-C or C-A according to the application.

The single-phase bus VT inputs each have associated phase shift and voltage magnitude compensation settings to compensate for healthy voltage angle and magnitude differences between the check sync VT input and the selected main VT reference phase. These are:

- ***CS VT Ph Shift*** and ***CS VT Mag***

Any voltage measurements or comparisons using bus VT inputs are made using the compensated values.

Each circuit breaker controlled can have two stages of check synchronism enabled according to the settings:

- ***System Checks***, ***CS1 Status*** and ***CS2 Status***

When the system voltage check conditions are satisfied, the relevant DDB signals are asserted high as follows:

- DDB (883): Check Sync 1 OK
- DDB (884): Check Sync 2 OK

These DDB signals should be mapped to the monitor/download port and used to indicate that the system check synchronism condition has been satisfied.

20.10.1 SYSTEM CHECK AND CHECK SYNCHRONISM

This function performs a comparison between the line voltage and the bus voltage.

For a single circuit breaker application, there are two voltage inputs to compare:

- one from the voltage transformer input from the line side of the circuit breaker (Main VT)
- one from the VT on the bus side of the circuit breaker (CS VT).

For a dual circuit breaker installation (breaker-and-a-half switch or mesh/ring bus), three VT inputs are required:

- one from the common point of the two circuit breakers, identified as the line (Main VT)
- one from the bus side of CB1 (CB1 CS VT)
- one from the bus side of CB2 (CB2 CS VT)

In most cases the line VT input is three phase, whereas the bus VTs are single phase.

The bus VT inputs are normally single phase so the system voltage checks are made on single phases and the VT may be connected to either a phase-to-phase or phase to neutral voltage.

For these reasons, the IED has to be programmed with the appropriate connection. The ***CS Input*** setting in the *CT AND VT RATIOS* column can be set to A-N, B-N, C-N, A-B, B-C or C-A according to the application.

The single-phase bus VT inputs each have associated phase shift and voltage magnitude compensation settings to compensate for healthy voltage angle and magnitude differences between the check sync VT input and the selected main VT reference phase. These are:

- ***CB1 CS VT PhShft***, ***CB1 CS VT Mag***, ***CB2 CS VT PhShft***, ***CB2 CS VT Mag***

Any voltage measurements or comparisons using bus VT inputs are made using the compensated values.

Each circuit breaker controlled can have two stages of check synchronism enabled according to the settings:

- ***Sys Checks CB1***, ***CB1 CS1 Status***, ***CB1 CS2 Status***, ***Sys Checks CB2***, ***CB2 CS1 Status***, ***CB1 CS2 Status***

When the system voltage check conditions are satisfied, the relevant DDB signals are asserted high as follows:

- DDB (883): ***CB1 CS1 OK***
- DDB (884): ***CB1 CS2 OK***
- DDB (1577): ***CB2 CS1 OK***
- DDB (1463): ***CB2 CS2 OK***

These DDB signals should be mapped to the monitor/download port and used to indicate that the system check synchronism condition has been satisfied.

20.10.2 CHECK SYNCHRONISM PASS

1. Taking note of the check synchronism settings, identify the appropriate VT input terminals and inject voltage signals that should satisfy the system voltage check synchronism criteria.
2. Check that the DDB signals are asserted high.

20.10.3 CHECK SYNCHRONISM FAIL

1. Change the voltage signals so that the criteria are not satisfied
2. Check that the appropriate DDB signals are driven low

20.11 CHECK TRIP AND AUTORECLOSE CYCLE

If the auto-reclose function is being used, the circuit breaker trip and auto reclose cycle can be tested automatically by using the application-specific settings.

To test the trip and close operation without operating the breaker, the following conditions must be satisfied:

- The ***CB Healthy*** DDB signal should either not be mapped, or if it is mapped it must be asserted high.
- The CB status inputs (52A, etc.) should either not be mapped, or if they are mapped they should be activated to mimic the circuit breaker operation.
- Some models can be configured for single-pole tripping. If configured for single pole tripping, either set *CT/VT RATIO* > ***VT Connected*** to `No`, or apply appropriate voltage signals to prevent the pole dead logic from converting to 3-pole tripping.

1. To test the first three-phase auto-reclose cycle, set *COMMISSION TESTS* > ***Test Autoreclose*** to `Trip 3 Pole`. The IED performs a trip/reclose cycle.
2. Repeat this operation to test the subsequent three-phase auto-reclose cycles.
3. Check all output relays (used for such as circuit breaker tripping and closing, or blocking other devices) operate at the correct times during the trip/close cycle.

Check the auto-reclose cycles for single phase trip conditions one at a time by sequentially setting *COMMISSION TESTS* > ***Test Autoreclose*** to `Trip Pole A`, `Trip Pole B` and `Trip Pole C`.

20.12 ONLOAD CHECKS

Warning:
Onload checks are potentially very dangerous and may only be carried out by qualified and authorised personnel.

Onload checks can only be carried out if there are no restrictions preventing the energisation of the plant, and the other devices in the group have already been commissioned.

Remove all test leads and temporary shorting links, then replace any external wiring that has been removed to allow testing.

Warning:
If any external wiring has been disconnected for the commissioning process, replace it in accordance with the relevant external connection or scheme diagram.

20.12.1 CONFIRM VOLTAGE CONNECTIONS

1. Using a multimeter, measure the voltage transformer secondary voltages to ensure they are correctly rated.
2. Check that the system phase rotation is correct using a phase rotation meter.
3. Compare the values of the secondary phase voltages with the measured voltage magnitude values, which can be found in the *MEASUREMENTS 1* menu column.

Cell in MEASUREMENTS 1 Column	Corresponding VT Ratio in CT/VT RATIOS Column
VAB MAGNITUDE *VBC MAGNITUDE* *VCA MAGNITUDE* *VAN MAGNITUDE* *VBN MAGNITUDE* *VCN MAGNITUDE*	Main VT Primary / Main VT Sec'y
C/S Voltage Mag	CS VT Primary / CS VT Secondary

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

20.12.2 CONFIRM CURRENT CONNECTIONS

1. Measure the current transformer secondary values for each input either by:
   a. reading from the device's HMI panel (providing it has first been verified by a secondary injection test)
   b. using a current clamp meter
2. Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of power flow by contacting the system control centre.
3. Ensure the current flowing in the neutral circuit of the current transformers is negligible.

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

20.12.3 ON-LOAD DIRECTIONAL TEST

This test ensures that directional overcurrent and fault locator functions have the correct forward/reverse response to fault and load conditions. For this test you must first know the actual direction of power flow on the system. If you do not already know this you must determine it using adjacent instrumentation or protection already in-service.

- For load current flowing in the Forward direction (power export to the remote line end), the ***A Phase Watts*** cell in the *MEASUREMENTS 2* column should show positive power signing.
- For load current flowing in the Reverse direction (power import from the remote line end), the ***A Phase Watts*** cell in the *MEASUREMENTS 2* column should show negative power signing.

Note:
*This check applies only for Measurement Modes 0 (default), and 2. This should be checked in the MEASURE'T SETUP column (**Measurement Mode** = 0 or 2). If measurement modes 1 or 3 are used, the expected power flow signing would be opposite to that shown above.*

In the event of any uncertainty, check the phase angle of the phase currents with respect to their phase voltage.

20.13 FINAL CHECKS

1. Remove all test leads and temporary shorting leads.
2. If you have had to disconnect any of the external wiring in order to perform the wiring verification tests, replace all wiring, fuses and links in accordance with the relevant external connection or scheme diagram.
3. The settings applied should be carefully checked against the required application-specific settings to ensure that they are correct, and have not been mistakenly altered during testing.
4. Ensure that all protection elements required have been set to `Enabled` in the *CONFIGURATION* column.
5. Ensure that the IED has been restored to service by checking that the ***Test Mode*** cell in the *COMMISSION TESTS* column is set to `Disabled`.
6. If the IED is in a new installation or the circuit breaker has just been maintained, the circuit breaker maintenance and current counters should be zero. These counters can be reset using the ***Reset All Values*** cell. If the required access level is not active, the device will prompt for a password to be entered so that the setting change can be made.
7. If the menu language has been changed to allow accurate testing it should be restored to the customer's preferred language.
8. If a P991/MMLG test block is installed, remove the P992/MMLB test plug and replace the cover so that the protection is put into service.
9. Ensure that all event records, fault records, disturbance records, alarms and LEDs and communications statistics have been reset.

Note:
Remember to restore the language setting to the customer's preferred language on completion.

CHAPTER 21

MAINTENANCE AND TROUBLESHOOTING

21.1 CHAPTER OVERVIEW

The Maintenance and Troubleshooting chapter provides details of how to maintain and troubleshoot products based on the Px4x and P40Agile platforms. Always follow the warning signs in this chapter. Failure to do so may result injury or defective equipment.

Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

The troubleshooting part of the chapter allows an error condition on the IED to be identified so that appropriate corrective action can be taken.

If the device develops a fault, it is usually possible to identify which module needs replacing. It is not possible to perform an on-site repair to a faulty module.

If you return a faulty unit or module to the manufacturer or one of their approved service centres, you should include a completed copy of the Repair or Modification Return Authorization (RMA) form.

This chapter contains the following sections:

21.2 MAINTENANCE

21.2.1 MAINTENANCE CHECKS

In view of the critical nature of the application, GE Vernova products should be checked at regular intervals to confirm they are operating correctly. GE Vernova products are designed for a life in excess of 20 years.

The devices are self-supervising and so require less maintenance than earlier designs of protection devices. Most problems will result in an alarm, indicating that remedial action should be taken. However, some periodic tests should be carried out to ensure that they are functioning correctly and that the external wiring is intact. It is the responsibility of the customer to define the interval between maintenance periods. If your organisation has a Preventative Maintenance Policy, the recommended product checks should be included in the regular program. Maintenance periods depend on many factors, such as:

- The operating environment
- The accessibility of the site
- The amount of available manpower
- The importance of the installation in the power system
- The consequences of failure

Although some functionality checks can be performed from a remote location, these are predominantly restricted to checking that the unit is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. For this reason, maintenance checks should also be performed locally at the substation.

Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

21.2.1.1 ALARMS

First check the alarm status LED to see if any alarm conditions exist. If so, press the Read key repeatedly to step through the alarms.

After dealing with any problems, clear the alarms. This will clear the relevant LEDs.

21.2.1.2 OPTO-ISOLATORS

Check the opto-inputs by repeating the commissioning test detailed in the Commissioning chapter.

21.2.1.3 OUTPUT RELAYS

Check the output relays by repeating the commissioning test detailed in the Commissioning chapter.

21.2.1.4 MEASUREMENT ACCURACY

If the power system is energised, the measured values can be compared with known system values to check that they are in the expected range. If they are within a set range, this indicates that the A/D conversion and the calculations are being performed correctly. Suitable test methods can be found in Commissioning chapter.

Alternatively, the measured values can be checked against known values injected into the device using the test block, (if fitted) or injected directly into the device's terminals. Suitable test methods can be found in the Commissioning chapter. These tests will prove the calibration accuracy is being maintained.

21.2.2 REPLACING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, you can replace either the complete device or just the faulty PCB, identified by the in-built diagnostic software.

If possible you should replace the complete device, as this reduces the chance of damage due to electrostatic discharge and also eliminates the risk of fitting an incompatible replacement PCB. However, we understand it may be difficult to remove an installed product and you may be forced to replace the faulty PCB on-site. The case and rear terminal blocks are designed to allow removal of the complete device, without disconnecting the scheme wiring.

Caution:
Replacing PCBs requires the correct on-site environment (clean and dry) as well as suitably trained personnel.

Caution:
If the repair is not performed by an approved service centre, the warranty will be invalidated.

Caution:
Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label. This should ensure that no damage is caused by incorrect handling of the electronic components.

Warning:
Before working at the rear of the device, isolate all voltage and current supplying it.

Note:
The current transformer inputs are equipped with integral shorting switches which will close for safety reasons, when the terminal block is removed.

To replace the complete device:

1. Carefully disconnect the cables not connected to the terminal blocks (e.g. IRIG-B, fibre optic cables, earth), as appropriate, from the rear of the device.
2. Remove the terminal block screws using a magnetic screwdriver to minimise the risk of losing the screws or leaving them in the terminal block.
3. Without exerting excessive force or damaging the scheme wiring, pull the terminal blocks away from their internal connectors.
4. Remove the terminal block screws that fasten the device to the panel and rack. These are the screws with the larger diameter heads that are accessible when the access covers are fitted and open.
5. Withdraw the device from the panel and rack. Take care, as the device will be heavy due to the internal transformers.
6. To reinstall the device, follow the above instructions in reverse, ensuring that each terminal block is relocated in the correct position and the chassis ground, IRIG-B and fibre optic connections are replaced. The terminal blocks are labelled alphabetically with 'A' on the left hand side when viewed from the rear.

Once the device has been reinstalled, it should be re-commissioned as set out in the Commissioning chapter.

Caution:
If the top and bottom access covers have been removed, some more screws with smaller diameter heads are made accessible. Do NOT remove these screws, as they secure the front panel to the device.

Note:
There are four possible types of terminal block: RTD/CLIO input, heavy duty, medium duty, and MiDOS. The terminal blocks are fastened to the rear panel with slotted or cross-head screws depending on the type of terminal block. Not all terminal block types are present on all products.

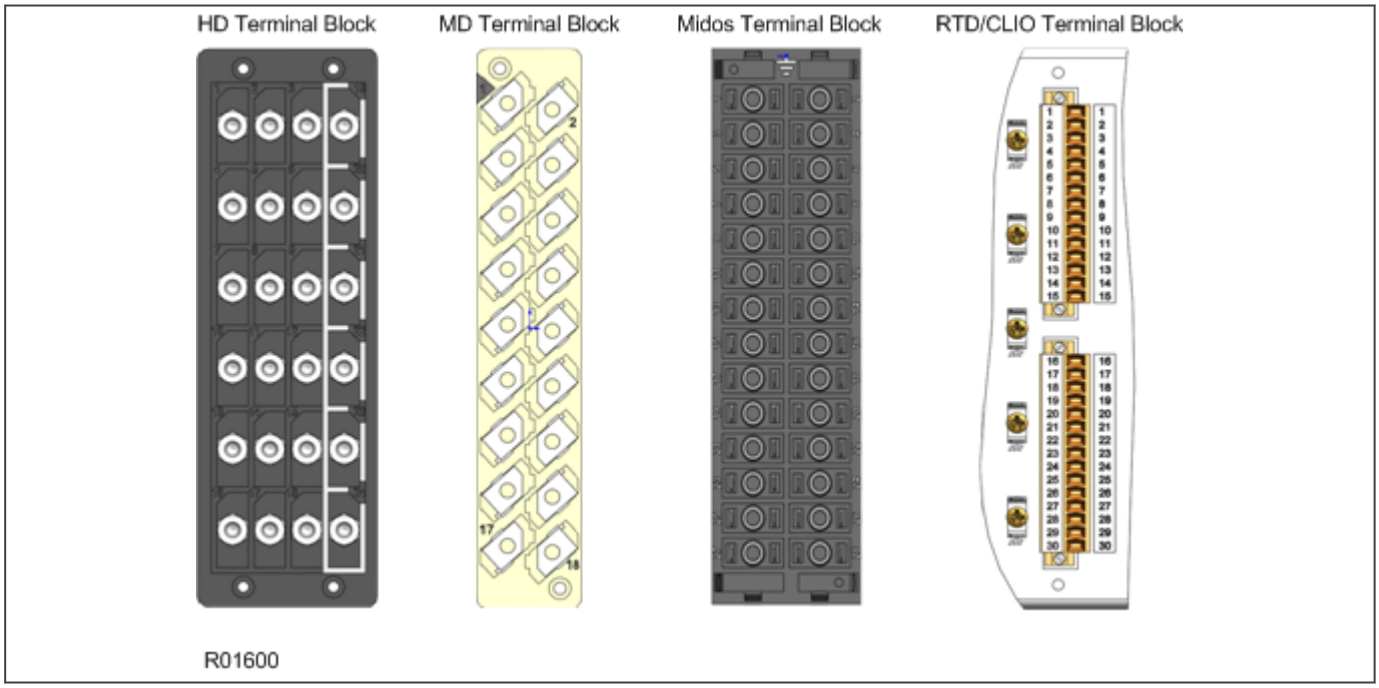


Figure 256: Possible terminal block types

21.2.3 REPAIRING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, either the complete unit or just the faulty PCB, identified by the in-built diagnostic software, should be replaced.

Replacement of printed circuit boards and other internal components must be undertaken by approved Service Centres. Failure to obtain the authorization of after-sales engineers prior to commencing work may invalidate the product warranty.

We recommend that you entrust any repairs to Automation Support teams, which are available world-wide.

21.2.4 REMOVING THE FRONT PANEL

Warning:
Before removing the front panel to replace a PCB, you must first remove the auxiliary power supply and wait 5 seconds for the internal capacitors to discharge. You should also isolate voltage and current transformer connections and trip circuit.

Caution:
Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.

To remove the front panel:

1. Open the top and bottom access covers. You must open the hinged access covers by more than 90° before they can be removed.
2. If fitted, remove the transparent secondary front cover.
3. Apply outward pressure to the middle of the access covers to bow them and disengage the hinge lug, so the access cover can be removed. The screws that fasten the front panel to the case are now accessible.
4. Undo and remove the screws. The 40TE case has four cross-head screws fastening the front panel to the case, one in each corner, in recessed holes. The 60TE/80TE cases have an additional two screws, one midway along each of the top and bottom edges of the front plate.
5. When the screws have been removed, pull the complete front panel forward to separate it from the metal case. The front panel is connected to the rest of the circuitry by a 64-way ribbon cable.
6. The ribbon cable is fastened to the front panel using an IDC connector; a socket on the cable and a plug with locking latches on the front panel. Gently push the two locking latches outwards which eject the connector socket slightly. Remove the socket from the plug to disconnect the front panel.

Caution:
Do not remove the screws with the larger diameter heads which are accessible when the access covers are fitted and open. These screws hold the relay in its mounting (panel or cubicle).

Caution:
The internal circuitry is now exposed and is not protected against electrostatic discharge and dust ingress. Therefore ESD precautions and clean working conditions must be maintained at all times.

21.2.5 REPLACING PCBS

1. To replace any of the PCBs, first remove the front panel.
2. Once the front panel has been removed, the PCBs are accessible. The numbers above the case outline identify the guide slot reference for each printed circuit board. Each printed circuit board has a label stating the corresponding guide slot number to ensure correct relocation after removal. To serve as a reminder of the slot numbering there is a label on the rear of the front panel metallic screen.
3. Remove the 64-way ribbon cable from the PCB that needs replacing
4. Remove the PCB in accordance with the board-specific instructions detailed later in this section.

Note:
To ensure compatibility, always replace a faulty PCB with one of an identical part number.

21.2.5.1 REPLACING THE MAIN PROCESSOR BOARD

The main processor board is situated in the front panel. This board contains application-specific settings in its non-volatile memory. You may wish to take a backup copy of these settings. This could save time in the re-commissioning process.

To replace the main processor board:

1. Remove front panel.
2. Place the front panel with the user interface face down and remove the six screws from the metallic screen, as shown in the figure below. Remove the metal plate.
3. Remove the screws that hold the main processor board in position.
4. Carefully disconnect the ribbon cable. Take care as this could easily be damaged by excessive twisting.
5. Replace the main processor board
6. Reassemble the front panel using the reverse procedure. Make sure the ribbon cable is reconnected to the main processor board and that all eight screws are refitted.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, carry out the standard commissioning procedure as defined in the Commissioning chapter.

Note:
After replacing the main processor board, all the settings required for the application need to be re-entered. This may be done either manually or by downloading a settings file.

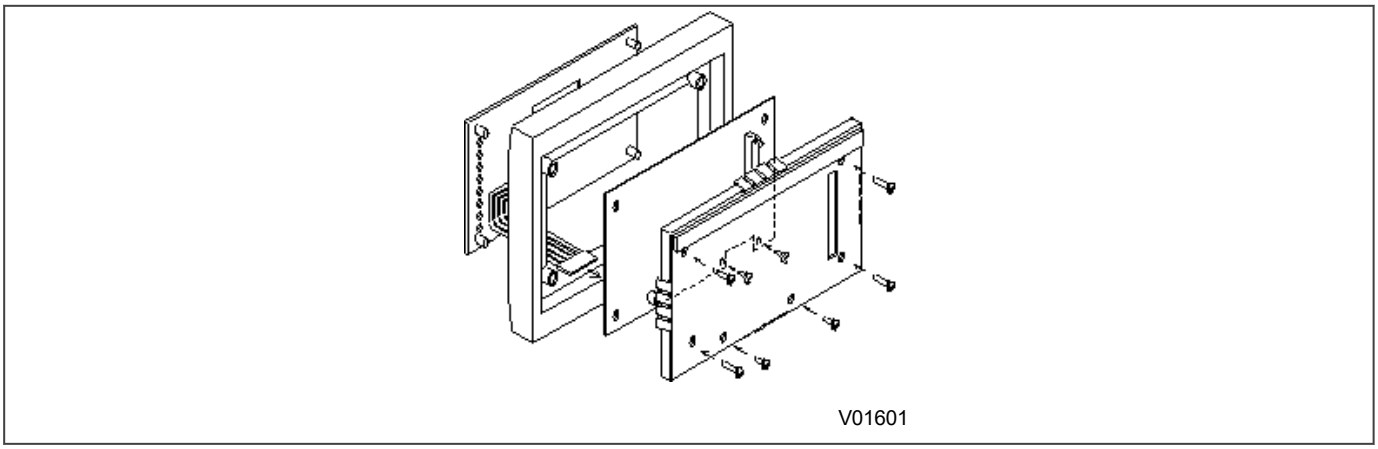


Figure 257: Front panel assembly

21.2.5.2 REPLACEMENT OF COMMUNICATIONS BOARDS

Most products will have at least one communications board of some sort fitted. There are several different boards available offering various functionality, depending on the application. Some products may even be fitted with two boards of different types.

To replace a faulty communications board:

1. Remove front panel.
2. Disconnect all connections at the rear.
3. The board is secured in the relay case by two screws, one at the top and another at the bottom. Remove these screws carefully as they are not captive in the rear panel.
4. Gently pull the communications board forward and out of the case.
5. Before fitting the replacement PCB check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.

6. Fit the replacement PCB carefully into the correct slot. Make sure it is pushed fully back and that the securing screws are refitted.
7. Reconnect all connections at the rear.
8. Refit the front panel.
9. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
10. Once the unit has been reassembled, commission it according to the Commissioning chapter.

21.2.5.3 REPLACEMENT OF THE INPUT MODULE

Depending on the product, the input module consists of two or three boards fastened together and is contained within a metal housing. One board contains the transformers and one contains the analogue to digital conversion and processing electronics. Some devices have an additional auxiliary transformer contained on a third board.

To replace an input module:

1. Remove front panel.
2. The module is secured in the case by two screws on its right-hand side, accessible from the front, as shown below. Move these screws carefully as they are not captive in the front plate of the module.
3. On the right-hand side of the module there is a small metal tab which brings out a handle (on some modules there is also a tab on the left). Grasp the handle(s) and pull the module firmly forward, away from the rear terminal blocks. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
4. Remove the module from the case. The module may be heavy, because it contains the input voltage and current transformers.
5. Slot in the replacement module and push it fully back onto the rear terminal blocks. To check that the module is fully inserted, make sure the v-shaped cut-out in the bottom plate of the case is fully visible.
6. Refit the securing screws.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, commission it according to the Commissioning chapter.

Caution:
With non-mounted IEDs, the case needs to be held firmly while the module is withdrawn. Withdraw the input module with care as it suddenly comes loose once the friction of the terminal blocks is overcome.

Note:
If individual boards within the input module are replaced, recalibration will be necessary. We therefore recommend replacement of the complete module to avoid on-site recalibration.

21.2.5.4 REPLACEMENT OF THE POWER SUPPLY BOARD

Caution:
Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.

The power supply board is fastened to an output relay board with push fit nylon pillars. This doubled-up board is secured on the extreme left hand side, looking from the front of the unit.

1. Remove front panel.
2. Pull the power supply module forward, away from the rear terminal blocks and out of the case. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
3. Separate the boards by pulling them apart carefully. The power supply board is the one with two large electrolytic capacitors.
4. Before reassembling the module, check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label
5. Reassemble the module with a replacement PCB. Push the inter-board connectors firmly together. Fit the four push fit nylon pillars securely in their respective holes in each PCB.
6. Slot the power supply module back into the housing. Push it fully back onto the rear terminal blocks.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, commission it according to the Commissioning chapter.

21.2.5.5 REPLACEMENT OF THE I/O BOARDS

There are several different types of I/O boards, which can be used, depending on the product and application. Some boards have opto-inputs, some have relay outputs and others have a mixture of both.

1. Remove front panel.
2. Gently pull the board forward and out of the case
3. If replacing the I/O board, make sure the setting of the link above IDC connector on the replacement board is the same as the one being replaced.
4. Before fitting the replacement board check the number on the round label next to the front edge of the board matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.
5. Carefully slide the replacement board into the appropriate slot, ensuring that it is pushed fully back onto the rear terminal blocks.
6. Refit the front panel.
7. Refit and close the access covers then press at the hinge assistance T-pieces so they click back into the front panel moulding.
8. Once the unit has been reassembled, commission it according to the Commissioning chapter.

21.2.6 RECALIBRATION

Recalibration is not needed when a PCB is replaced, unless it is one of the boards in the input module. If any of the boards in the input module is replaced, the unit must be recalibrated.

Although recalibration is needed when a board inside the input module is replaced, it is not needed if the input module is replaced in its entirety.

Although it is possible to carry out recalibration on site, this requires special test equipment and software. We therefore recommend that the work be carried out by the manufacturer, or entrusted to an approved service centre.

21.2.7 SUPERCAPACITOR DISCHARGED

The supercapacitor maintains charge for two weeks with the IED de-energised. When first energising the IED after this time there may be a ***SuperCap Alarm*** due to the supercapacitor voltage dropping below a pre-defined

threshold. The ***SuperCap Alarm*** will clear after approximately 30 minutes of IED being energised, and once cleared there will be enough charge in the supercapacitor to maintain the RTC.

Note:
The Real Time Clock will be reset if the supercapacitor is fully discharged.

21.2.8 CLEANING

Warning:
Before cleaning the device, ensure that all AC and DC supplies and transformer connections are isolated, to prevent any chance of an electric shock while cleaning.

Only clean the equipment with a lint-free cloth dampened with clean water. Do not use detergents, solvents or abrasive cleaners as they may damage the product's surfaces and leave a conductive residue.

21.3 TROUBLESHOOTING

21.3.1 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the 'Healthy' LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the 'Healthy' LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

21.3.2 POWER-UP ERRORS

If the IED does not appear to power up, use the following to determine whether the fault is in the external wiring, auxiliary fuse, IED power supply module or IED front panel.

Test	Check	Action
1	Measure the auxiliary voltage on terminals 1 and 2. Verify the voltage level and polarity against the rating label on the front. Terminal 1 is –dc, 2 is +dc	If the auxiliary voltage is correct, go to test 2. Otherwise check the wiring and fuses in the auxiliary supply.
2	Check the LEDs and LCD backlight switch on at power-up. Also check the N/O (normally open) watchdog contact for closing.	If the LEDs and LCD backlight switch on, or the contact closes and no error code is displayed, the error is probably on the main processor board in the front panel. If the LEDs and LCD backlight do not switch on and the contact does not close, go to test 3.
3	Check the output (nominally 48 V DC).	If there is no field voltage, the fault is probably in the IED power supply module.

21.3.3 ERROR MESSAGE OR CODE ON POWER-UP

The IED performs a self-test during power-up. If it detects an error, a message appears on the LCD and the power-up sequence stops. If the error occurs when the IED application software is running, a maintenance record is created and the device reboots.

Test	Check	Action
1	Is an error message or code permanently displayed during power up?	If the IED locks up and displays an error code permanently, go to test 2. If the IED prompts for user input, go to test 4. If the IED reboots automatically, go to test 5.
2	Record displayed error, and then remove and re-apply IED auxiliary supply.	Record whether the same error code is displayed when the IED is rebooted. If no error code is displayed, contact the local service centre stating the error code and IED information. If the same code is displayed, go to test 3.

Test	Check	Action
3	Error Code Identification The following text messages (in English) are displayed if a fundamental problem is detected, preventing the system from booting: Bus Fail – address lines SRAM Fail – data lines FLASH Fail format error FLASH Fail checksum Code Verify Fail The following hex error codes relate to errors detected in specific IED modules:	These messages indicate that a problem has been detected on the IED's main processor board in the front panel.
3.1	0c140005/0c0d0000	Input Module (including opto-isolated inputs)
3.2	0c140006/0c0e0000	Output IED boards
3.3	The last four digits provide details on the actual error.	Other error codes relate to hardware or software problems on the main processor board. Contact General Electric with details of the problem for a full analysis.
4	The IED displays a message for corrupt settings and prompts for the default values to be restored for the affected settings.	The power-up tests have detected corrupted IED settings. Restore the default settings to allow the power-up to complete, and then reapply the application-specific settings.
5	The IED resets when the power-up is complete. A record error code is displayed	Error 0x0E080000, programmable scheme logic error due to excessive execution time. If the IED powers up successfully, check the programmable logic for feedback paths. Other error codes relate to software errors on the main processor board.

21.3.4 OUT OF SERVICE LED ON AT POWER-UP

Test	Check	Action	
1	Using the IED menu, confirm the Commission Test or Test Mode setting is Enabled. If it is not Enabled, go to test 2.	If the setting is Enabled, disable the test mode and make sure the Out of Service LED is OFF.	
2	Select the *VIEW RECORDS* column then view the last maintenance record from the menu.	Check for the H/W Verify Fail maintenance record. This indicates a discrepancy between the IED model number and the hardware. Examine the ***Maint Data***; cell. This indicates the causes of the failure using bit fields: Bit Meaning	
		0	The application type field in the model number does not match the software ID
		1	The application field in the model number does not match the software ID
		2	The variant 1 field in the model number does not match the software ID
		3	The variant 2 field in the model number does not match the software ID
		4	The protocol field in the model number does not match the software ID

Test	Check	Action	
		5	The language field in the model number does not match the software ID
		6	The VT type field in the model number is incorrect (110 V VTs fitted)
		7	The VT type field in the model number is incorrect (440 V VTs fitted)
		8	The VT type field in the model number is incorrect (no VTs fitted)

21.3.5 ERROR CODE DURING OPERATION

The IED performs continuous self-checking. If the IED detects an error it displays an error message, logs a maintenance record and after a short delay resets itself. A permanent problem (for example due to a hardware fault) is usually detected in the power-up sequence. In this case the IED displays an error code and halts. If the problem was transient, the IED reboots correctly and continues operation. By examining the maintenance record logged, the nature of the detected fault can be determined.

21.3.6 MAL-OPERATION DURING TESTING

21.3.6.1 FAILURE OF OUTPUT CONTACTS

An apparent failure of the relay output contacts can be caused by the configuration. Perform the following tests to identify the real cause of the failure. The self-tests verify that the coils of the output relay contacts have been energized. An error is displayed if there is a fault in the output relay board.

Test	Check	Action
1	Is the Out of Service LED ON?	If this LED is ON, the relay may be in test mode or the protection has been disabled due to a hardware verify error.
2	Examine the Contact status in the Commissioning section of the menu.	If the relevant bits of the contact status are operated, go to test 4; if not, go to test 3.
3	Examine the fault record or use the test port to check the protection element is operating correctly.	If the protection element does not operate, check the test is correctly applied. If the protection element operates, check the programmable logic to make sure the protection element is correctly mapped to the contacts.
4	Using the Commissioning or Test mode function, apply a test pattern to the relevant relay output contacts. Consult the correct external connection diagram and use a continuity tester at the rear of the relay to check the relay output contacts operate.	If the output relay operates, the problem must be in the external wiring to the relay. If the output relay does not operate the output relay contacts may have failed (the self-tests verify that the relay coil is being energized). Ensure the closed resistance is not too high for the continuity tester to detect.

21.3.6.2 FAILURE OF OPTO-INPUTS

The opto-isolated inputs are mapped onto the IED's internal DDB signals using the programmable scheme logic. If an input is not recognised by the scheme logic, use the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column to check whether the problem is in the opto-input itself, or the mapping of its signal to the scheme logic functions.

If the device does not correctly read the opto-input state, test the applied signal. Verify the connections to the opto-input using the wiring diagram and the nominal voltage settings in the *OPTO CONFIG* column. To do this:

1. Select the nominal voltage for all opto-inputs by selecting one of the five standard ratings in the ***Global Nominal V*** cell.
2. Select `Custom` to set each opto-input individually to a nominal voltage.
3. Using a voltmeter, check that the voltage on its input terminals is greater than the minimum pick-up level (See the Technical Specifications chapter for opto pick-up levels).

If the signal is correctly applied, this indicates failure of an opto-input, which may be situated on standalone opto-input board, or on an opto-input board that is part of the input module. Separate opto-input boards can simply be replaced. If, however, the faulty opto-input board is part of the input module, the complete input module should be replaced. This is because the analogue input module cannot be individually replaced without dismantling the module and recalibration of the IED.

21.3.6.3 INCORRECT ANALOGUE SIGNALS

If the measured analogue quantities do not seem correct, use the measurement function to determine the type of problem. The measurements can be configured in primary or secondary terms.

1. Compare the displayed measured values with the actual magnitudes at the terminals.
2. Check the correct terminals are used.
3. Check the CT and VT ratios set are correct.
4. Check the phase displacement to confirm the inputs are correctly connected.

21.3.7 PSL EDITOR TROUBLESHOOTING

A failure to open a connection could be due to one or more of the following:

- The IED address is not valid (this address is always 1 for the front port)
- Password in not valid
- Communication set-up (COM port, Baud rate, or Framing) is not correct
- Transaction values are not suitable for the IED or the type of connection
- The connection cable is not wired correctly or broken
- The option switches on any protocol converter used may be incorrectly set

21.3.7.1 DIAGRAM RECONSTRUCTION

Although a scheme can be extracted from an IED, a facility is provided to recover a scheme if the original file is unobtainable.

A recovered scheme is logically correct but much of the original graphical information is lost. Many signals are drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B. Any annotation added to the original diagram such as titles and notes are lost.

Sometimes a gate type does not appear as expected. For example, a single-input AND gate in the original scheme appears as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 also appear as OR gates

21.3.7.2 PSL VERSION CHECK

The PSL is saved with a version reference, time stamp and CRC check (Cyclic Redundancy Check). This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

21.3.8 REPAIR AND MODIFICATION PROCEDURE

Please follow these steps to return an Automation product to us:

1. Get the Repair and Modification Return Authorization (RMA) form
   An electronic version of the RMA form is available from the following:
   contact.centre@ge.com
2. Fill in the RMA form
   Fill in only the white part of the form.
   Please ensure that all fields marked **(M)** are completed such as:
   - Equipment model
   - Model No. and Serial No.
   - Description of failure or modification required (please be specific)
   - Value for customs (in case the product requires export)
   - Delivery and invoice addresses
   - Contact details
3. Send the RMA form to your local contact
   For a list of local service contacts worldwide, email us at:
   contact.centre@ge.com
4. The local service contact provides the shipping information
   Your local service contact provides you with all the information needed to ship the product:
   - Pricing details
   - RMA number
   - Repair centre address

   If required, an acceptance of the quote must be delivered before going to the next stage.
5. Send the product to the repair centre
   - Address the shipment to the repair centre specified by your local contact
   - Make sure all items are packaged in an anti-static bag and foam protection
   - Make sure a copy of the import invoice is attached with the returned unit
   - Make sure a copy of the RMA form is attached with the returned unit
   - E-mail or fax a copy of the import invoice and airway bill document to your local contact.

CHAPTER 22

TECHNICAL SPECIFICATIONS

22.1 CHAPTER OVERVIEW

This chapter describes the technical specifications of the product.

This chapter contains the following sections:

22.2 INTERFACES

22.2.1 GRAPHICAL HMI

Graphical HMI	
Screen size	4.0" diagonal
Display format	480 x 480 Dots
Number of colour	16.7M
Dimensions	77 mm (H) x 80 mm (V) x 2.3 mm (D)
Active area	71.86 mm (H) x 70.18 mm (V)
Display mode	Transmissive/normally black
Viewing direction	All round
Backlight type	LED, white
Operating temperature	-30°C ~ + 85°C
Storage temperature	-40°C ~ + 90°C

22.2.2 FRONT USB PORT

Front USB port	
Use	For local connection to laptop for configuration purposes and firmware downloads
Connector	USB type B
Isolation	Isolation to ELV level
Constraints	Maximum cable length 5 m

22.2.3 REAR SERIAL PORT 1

Rear serial port 1 (RP1)	
Use	For SCADA communications (multi-drop)
Standard	EIA(RS)485, K-bus
Connector	General purpose block, M4 screws (2 wire)
Cable	Screened twisted pair (STP)
Supported Protocols *	Courier, IEC-60870-5-103, DNP3.0
Isolation	Isolation to SELV level
Constraints	Maximum cable length 1000 m

22.2.4 FIBRE REAR SERIAL PORT 1

Optional fibre rear serial port (RP1)	
Main Use	Serial SCADA communications over fibre
Connector	IEC 874-10 BFOC 2.5 –(ST®) (1 each for Tx and Rx)
Fibre type	Multimode 50/125 µm or 62.5/125 µm
Supported Protocols	Courier, IEC870-5-103, DNP 3.0
Wavelength	850 nm

22.2.5 REAR SERIAL PORT 2

Optional rear serial port (RP2)	
Use	For SCADA communications (multi-drop)
Standard	EIA(RS)485, K-bus, EIA(RS)232
Designation	SK4
Connector	9 pin D-type female connector
Cable	Screened twisted pair (STP)
Supported Protocols	Courier
Isolation	Isolation to SELV level
Constraints	Maximum cable length 1000 m for RS485 and K-bus, 15 m for RS232

22.2.6 OPTIONAL REAR SERIAL PORT (SK5)

Optional rear serial port for teleprotection	
Use	For teleprotection in distance products
Standard	EIA(RS)232
Designation	SK5
Connector	9 pin D-type female connector
Cable	Screened twisted pair (STP)
Supported Protocols	InterMiCOM (IM)
Isolation	Isolation to SELV level
Constraints	Maximum cable length 15 m

22.2.7 IRIG-B (DEMODULATED)

IRIG-B Interface (Demodulated)	
Use	External clock synchronisation signal
Standard	IRIG 200-98 format B00X
Connector	BNC
Cable type	50 ohm coaxial
Isolation	Isolation to SELV level
Input signal	TTL level
Input impedance	10 k ohm at dc
Accuracy	+/- 1 ms

22.2.8 IRIG-B (MODULATED)

IRIG-B Interface (Modulated)	
Use	External clock synchronisation signal
Standard	IRIG 200-98 format B12X
Connector	BNC
Cable type	50 ohm coaxial
Isolation	Isolation to SELV level

IRIG-B Interface (Modulated)	
Input signal	peak to peak, 200 mV to 20 mV
Input impedance	6 k ohm at 1000 Hz
Accuracy	+/- 1 ms

22.2.9 REAR ETHERNET PORT COPPER

Rear Ethernet Port Using CAT 5/6/7 Wiring	
Main Use	Substation Ethernet communications
Standard	IEEE 802.3 10BaseT/100BaseTX
Connector	RJ45
Cable type	Screened twisted pair (STP)
Isolation	1.5 kV
Supported Protocols	Courier (tunnelled), IEC 61850, PTP, SNTP, SNMP, RADIUS, syslog
Redundancy Protocols Supported	PRP (Parallel Redundancy Protocol) HSR (High-availability Seamless Redundancy) RSTP (Rapid Spanning Tree Protocol) Failover
Constraints	Maximum cable length 100 m

22.2.10 REAR ETHERNET PORT FIBRE

Rear Ethernet Port Using Fibre-optic Cabling	
Main Use	Substation Ethernet communications
Connector	IEC 874-10 BFOC 2.5 - (LC®) (1 each for Tx and Rx)
Standard	IEEE 802.3 100 BaseFX
Fibre type	Multimode 50/125 µm (OM2 or OM3) or 62.5/125 µm (OM1)
Supported Protocols	Courier (tunnelled), IEC 61850, PTP, SNTP, SNMP, RADIUS, syslog
Redundancy Protocols Supported	PRP (Parallel Redundancy Protocol) HSR (High-availability Seamless Redundancy) RSTP (Rapid Spanning Tree Protocol) Failover
Wavelength	1310 nm

22.2.10.1 100 BASE FX RECEIVER CHARACTERISTICS

Parameter	Sym	Min.	Typ.	Max.	Unit
Input Optical Power Minimum at Window Edge	PIN Min. (W)	-31.0		-12.0	dBm avg.
Input Optical Power Minimum at Eye Center	PIN Min. (C)		-34.5	-31.8	Bm avg.
Input Optical Power Maximum	PIN Max.	-14	-11.8		dBm avg.

Conditions: TA = 0°C to 70°C

22.2.10.2 100 BASE FX TRANSMITTER CHARACTERISTICS

Parameter	Sym	Min.	Typ.	Max.	Unit
Output Optical Power BOL 62.5/125 µm NA = 0.275 Fibre EOL	PO	-20	-17.0	-14.0	dBm avg.
Output Optical Power BOL 50/125 µm NA = 0.20 Fibre EOL	PO	-24.0	-21.0	-17.0	dBm avg.
Optical Extinction Ratio	ER	10			dB
Output Optical Power at Logic "0" State	$P_{O(off)}$			-45	dBm avg.

Conditions: TA = 0°C to 70°C

22.3 PROTECTION FUNCTIONS

22.3.1 AUTORECLOSE AND CHECK SYNYCHRONISM

Accuracy	
Timers	+/- 20 ms or 2%, whichever is greater

22.3.2 PHASE OVERCURRENT PROTECTION

Accuracy	
IDMT pick-up	1.05 x Setting +/-5%
DT pick-up	Setting +/-5%
Drop-off (IDMT and DT)	0.98 x setting +/-5%
IDMT operate	+/-5% of expected operating time or 40 ms, whichever is greater*
IEEE reset	+/-5% or 40 ms, whichever is greater**
DT operate time	+/-2% of setting or 40 ms, whichever is greater (Non Directional)** +/-2% of setting or 60 ms, whichever is greater (Directional)
DT reset	Setting +/-5%
Repeatability	<5%
Characteristic UK	IEC 60255-151: 2009
Characteristic US	IEEE C37.112 1996

Note:
**Reference conditions: TMS = 1, TD = 7, I> = 1A, operating range = 2-20In*
***Reference conditions: Injected value is 2 x pick-up value.*

22.3.2.1 TRANSIENT OVERREACH AND OVERSHOOT

Additional tolerance due to increasing X/R ratios	+/-5% over the X/R ratio of 1 to 90
Overshoot of overcurrent elements	< 30 ms

22.3.2.2 PHASE OVERCURRENT DIRECTIONAL PARAMETERS

Accuracy	
Directional boundary pickup (RCA +/-90%)	+/-2°
Directional boundary hysteresis	< 2°
Directional boundary repeatability	<2%

22.3.3 EARTH FAULT PROTECTION

Accuracy	
IDMT pick-up	1.05 x Setting +/-5%
DT pick-up	Setting +/-5%, or 20 mA, whichever is greater

Accuracy	
Drop-off (IDMT and DT)	0.95 x setting +/-5%
IDMT Operate	+/- 5% or 60 ms, whichever is greater (1.05 - 2) Is +/- 5% or 40 ms, whichever is greater (2 - 20) Is
IEEE reset	+/-10% or 40 ms, whichever is greater
Repeatability	< 5%
DT operate	+/- 2% or 70 ms, whichever is greater (1.05 - 2) Is +/- 2% or 55 ms, whichever is greater (2 - 20) Is
DT reset	+/- 5% or 50 ms, whichever is greater

22.3.3.1 EARTH FAULT DIRECTIONAL PARAMETERS

Zero Sequence Polarising accuracy	
Directional boundary pick-up (RCA +/- 90°)	+/-2°
Hysteresis	<3°
VN> pick-up	Setting+/-10%
VN> drop-off	0.9 x Setting +/-10%

Negative Sequence Polarising accuracy	
Directional boundary pick-up (RCA +/- 90°)	+/-2°
Hysteresis	<3°
VN2> pick-up	Setting+/-10%
VN2> drop-off	0.9 x Setting +/-10%
IN2> pick-up	Setting+/-10%
IN2> drop-off	0.9 x Setting +/-10%

22.3.4 SENSITIVE EARTH FAULT PROTECTION

IDMT pick-up	1.05 x Setting +/-5%
DT Pick-up	Setting +/- 5%
Drop-off (IDMT + DT)	0.95 x Setting +/-5%
IDMT operate	+/- 5% or 70 ms, whichever is greater (1.05 - 2) Is +/- 5% or 70 ms, whichever is greater (2 - 20) Is
DT operate	+/- 2% or 70 ms, whichever is greater (1.05 - 2) Is +/- 2% or 50 ms, whichever is greater (2 - 20) Is
DT reset	Setting +/- 5% or 50 ms, whichever is greater
Repeatability	< 5%

Note:
SEF claims apply to SEF input currents of no more than 2 x In. For input ranges above 2 x In, the claim is not supported.

22.3.4.1 SENSITIVE EARTH FAULT PROTECTION DIRECTIONAL ELEMENT

Wattmetric SEF	
Pick-up P = 0 W	ISEF > +/-5% or 5 mA
Pick-up P > 0 W	P > +/-5%
Drop-off P = 0 W	0.95 x ISEF> +/- 5% or 5 mA
Drop-off P > 0 W	0.9 x P> +/- 5% or 5 mA
Boundary accuracy	+/-5% with hysteresis < 1°
Repeatability	< 1%

22.3.5 HIGH IMPEDANCE RESTRICTED EARTH FAULT PROTECTION

High Impedance and Low Impedance	
Pick-up	Setting formula +/- 5%
Drop-off	0.8 x Setting formula +/-5%
Operating time	< 60 ms
High set pick-up	Setting +/- 10%
High set operating time	< 30 ms
Repeatability	< 5%

22.3.6 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

IDMT pick-up	1.05 x Setting +/-5%
DT pick-up	Setting +/- 5%
Drop-off (IDMT and DT)	0.95 x Setting +/-5%
IDMT operate	+/- 5% or 40 ms, whichever is greater
DT operate	+/- 2% or 60 ms, whichever is greater
DT Reset	Setting +/- 5%

22.3.6.1 NPSOC DIRECTIONAL PARAMETERS

Directional boundary pick-up (RCA +/-90%)	+/-2°
Directional boundary hysteresis	< 1°
Directional boundary repeatability	< 1%

22.3.7 CIRCUIT BREAKER FAIL AND UNDERCURRENT PROTECTION

I< Pick-up	Setting +/- 10% or 0.025 In, whichever is greater
I< Drop-off	Setting +/- 5% or 20 mA, whichever is greater
Operate time	< 12 ms
Timers	+/- 2% or 20 ms, whichever is greater

Reset time	< 15 ms

22.3.8 BROKEN CONDUCTOR PROTECTION

Pick-up	Setting +/- 2.5%
Drop-off	0.95 x Setting +/- 2.5%
DT operate	+/- 2% or 40 ms, whichever is greater
Reset time	<30 ms

22.3.9 THERMAL OVERLOAD PROTECTION

Thermal alarm pick-up	Calculated trip time +/- 10%
Thermal overload pick-up	Calculated trip time +/- 10%
Cooling time accuracy	+/- 15% of theoretical
Repeatability	<5%

Note:
Operating time measured with applied current of 20% above thermal setting.

22.4 PERFORMANCE OF VOLTAGE PROTECTION FUNCTIONS

22.4.1 OVERVOLTAGE PROTECTION

Pick-up (DT)	Setting +/- 1%
Pick-up (IDMT)	1.02 x Setting +/- 2%
Drop-off (DT and IDMT)	0.98 x Setting +/-2%
DT operate	+/- 2% or 40 ms, whichever is greater
IDMT operate	+/- 2% or 40 ms, whichever is greater
Reset	< 75 ms
Repeatability	< 1%

22.4.2 UNDERVOLTAGE PROTECTION

Pick-up (DT)	Setting +/-5%
Pick-up (IDMT)	0.98 x Setting +/-2%
Drop-off (DT and IDMT)	1.02 x Setting +/-2%
DT operate	+/- 2% or 40 ms, whichever is greater
IDMT operate	+/- 2% or 40 ms, whichever is greater
Reset	< 35 ms
Repeatability	< 1%

22.4.3 RESIDUAL OVERVOLTAGE PROTECTION

Pick-up (DT)	Setting +/- 5%
Pick-up (IDMT)	1.05 x Setting +/- 5%
Drop-off (DT and IDMT)	0.95 x Setting +/-5%
DT operate	+/- 2% or 20 ms, whichever is greater
IDMT operate	+/- 5% or 60 ms, whichever is greater
Instantaneous operation	< 50 ms
Reset	< 35 ms
Repeatability	< 10%

22.4.4 COMPENSATED OVERVOLTAGE PROTECTION

Pick-up (DT)	Setting +/- 1%
Pick-up (IDMT)	1.02 x Setting +/- 2%
Drop-off (DT and IDMT)	(1-(**Cp V Hysteresis** setting))* setting +/- 2%
DT operate	+/- 2% or 40 ms, whichever is greater
IDMT operate	+/- 2% or 40 ms, whichever is greater

Reset	< 75 ms
Repeatability	< 1%

22.4.5 VOLTAGE MONITOR

Live Voltage Accuracy	
Pick-up	Setting +/-3% or +/- 0.1 V, whichever is greater
Drop-off	(0.98 x setting) +/-3% or +/- 0.1 V, whichever is greater
Repeatability	< 1%

Dead Voltage Accuracy	
Pick-up	Setting +/-3% or +/- 0.1 V, whichever is greater
Drop-off	(1.02 x setting) +/-3% or +/- 0.1 V, whichever is greater
Repeatability	< 1%

Diff Voltage Accuracy	
Pick-up	Setting +/-3% or +/- 0.1 V, whichever is greater
Drop-off	(0.98 x setting) +/-3% or +/- 0.1 V, whichever is greater
Repeatability	< 1%

Overvoltage Accuracy	
Pick-up	Setting +/-3% or +/- 0.1 V, whichever is greater
Drop-off	(0.98 x setting) +/-3% or +/- 0.1 V, whichever is greater
Repeatability	< 1%

Undervoltage Accuracy	
Pick-up	Setting +/-3% or +/- 0.1 V, whichever is greater
Drop-off	(1.02 x setting) +/-3% or +/- 0.1 V, whichever is greater
Repeatability	< 1%

22.4.6 CHECK SYNCHRONISATION

Accuracy (CS1/CS2)	
Phase Angle	
Pick-up	(Setting-2°) ±1° *
Drop-off	(Setting-1°) ±1° *
Repeatability	<1%
Slip Frequency	
Pick-up	Setting ±0.01 Hz
Drop-off	(0.95 x Setting) ±0.01 Hz
Repeatability	<1%
Slip Timer	

Accuracy (CS1/CS2)	
Timers	+/- 1% or 40 ms, whichever is greater
Reset Time	<30 ms
Repeatability	<10 ms

Note:
** **CS VT Ph Shift** setting = 0°*

22.4.7 SYSTEM SPLIT

SS Phase Angle Accuracy	
Pick-up	(Setting + 2°) +/- 1°
Drop-off	(Setting + 1°) +/- 1°
Repeatability	< 1%

SS Undervoltage Accuracy	
Pick-up	Setting +/- 3 %
Drop-off	1.02 x setting
Repeatability	< 1%

SS Timer	
Timers	Setting +/- 1% or 40 ms, whichever is greater
Reset time	< 30 ms
Repeatability	< 10 ms

22.5 PERFORMANCE OF FREQUENCY PROTECTION FUNCTIONS

22.5.1 OVERFREQUENCY PROTECTION

Accuracy	
Pick-up	Setting +/- 10 mHz
Drop-off	Setting -20 mHz +/- 10 mHz
Operating timer	+/- 2% or 50 ms, whichever is greater

Operating and Reset time	
Operating time (Fs/Ff ratio less than 2)	<125 ms
Operating time (Fs/Ff ratio between 2 and 30)	<150 ms
Operating time (Fs/Ff ratio greater than 30)	<200 ms
Reset time	<200 ms

Reference conditions: Tested using step changed in frequency with Freq. Av Cycles setting = 0 and no intentional time delay.

Fs = start frequency – frequency setting

Ff = frequency setting – end frequency

22.5.2 UNDERFREQUENCY PROTECTION

Accuracy	
Pick-up	Setting +/- 10 mHz
Drop-off	Setting + 20 mHz +/- 10 mHz
Operating timer	+/- 2% or 50 ms, whichever is greater

Operating and Reset time	
Operating time (Fs/Ff ratio less than 2)	<100 ms
Operating time (Fs/Ff ratio between 2 and 6)	<160 ms
Operating time (Fs/Ff ratio greater than 6)	<230 ms
Reset time	<200 ms

Reference conditions: Tested using step changed in frequency with Freq. Av Cycles setting = 0 and no intentional time delay.

Fs = start frequency – frequency setting

Ff = frequency setting – end frequency

22.5.3 INDEPENDENT RATE OF CHANGE OF FREQUENCY PROTECTION

Accuracy	
Pick-up (df/dt)	Setting +/- 50 mHz
Operating timer	+/- 2% or 50 ms, whichever is greater

Operating	
For 6 Cycles: Operating time (for ramps 1.5 x setting and greater)	<300 ms
For 12 Cycles: Operating time (for ramps 1.5 x setting and greater)	<500 ms

Reference Conditions: Tested with df/dt Average Cycles = 6 and 12 for df/dt settings greater than 0.1 Hz/s, and no intentional time delay.

22.6 POWER PROTECTION FUNCTIONS

22.6.1 OVERPOWER/UNDERPOWER PROTECTION

Pick-up	Setting +/- 10%
Reverse/Overpower Drop-off	0.95 x Setting +/- 10%
Low forward power Drop-off	1.05 x Setting +/- 10%
Angle variation pick-up	+/- 2°
Angle variation drop-off	+/- 2.5°
Operating time	+/- 2% or 50 ms, whichever is greater
Repeatability	< 5%
Disengagement time	<50 ms
tRESET	+/- 5%
Instantaneous operating time	< 50 ms

22.7 MONITORING, CONTROL AND SUPERVISION

22.7.1 VOLTAGE TRANSFORMER SUPERVISION

Fast block operation, loss of 1 and 2 phases	<1 cycle
Fast Block operation, loss of 3 phases	<1.5 cycle
Time delay	+/- 2% or 30 ms, whichever is greater

22.7.2 STANDARD CURRENT TRANSFORMER SUPERVISION

IN> Pick-up	Setting +/- 5%
VN< Pick-up	Setting +/- 5%
IN> Drop-off	0.9 x setting +/- 5%
VN< Drop-off	1.05 x setting +/-5% or 1 V, whichever is greater
Time delay operation	Setting +/-2% or 20 ms, whichever is greater
CTS block operation	< 1 cycle
CTS reset	< 35 ms

22.7.3 DIFFERENTIAL CURRENT TRANSFORMER SUPERVISION

Accuracy	
I1> Pick-up	Setting +/- 5%
I1> Drop-off	0.9 x setting +/- 5%
I2/I1> Pick-up	Setting +/- 5%
I2/I1> Drop-off	0.9 x setting +/-5%
I2/I1>> Pick-up	Setting +/- 5%
I2/I1 >> Drop-off	0.9 x setting +/-5%
Time delay operation	Setting +/-2% or 20 ms, whichever is greater
CTS block diff operation	< 1 cycle
CTS reset	< 35 ms

22.7.4 CB STATE AND CONDITION MONITORING

Accuracy	
Timers	+/- 40 ms or 2%, whichever is greater
Broken current accuracy	+/- 5%
Reset time	< 30 ms

22.7.5 PSL TIMERS

Output conditioner timer	Setting ±2% or 50 ms, whichever is greater
Dwell conditioner timer	Setting ±2% or 50 ms, whichever is greater
Pulse conditioner timer	Setting ±2% or 50 ms, whichever is greater

22.8 MEASUREMENTS AND RECORDING

22.8.1 GENERAL

General Measurement Accuracy	
General measurement accuracy	Typically +/- 1%, but +/- 0.5% between 0.2 - 2 In/Vn
Phase	0° to 360° +/- 0.5%
Current (0.05 to 3 In)	+/- 1.0% of reading, or 4mA (1A input), or 20mA (5A input)
Voltage (0.05 to 2 Vn)	+/- 1.0% of reading
Frequency (45 to 65 Hz)	+/- 0.025 Hz
Power (W) (0.2 to 2 Vn and 0.05 to 3 In)	+/- 5.0% of reading at unity power factor
Reactive power (Vars) (0.2 to 2 Vn and 0.05 to 3 In)	+/- 5.0% of reading at zero power factor
Apparent power (VA) (0.2 to 2 Vn and 0.05 to 3 In)	+/- 5.0% of reading
Energy (Wh) (0.2 to 2 Vn and 0.2 to 3 In)	+/- 5.0% of reading at unity power factor
Energy (Varh) (0.2 to 2 Vn and 0.2 to 3In)	+/- 5.0% of reading at zero power factor

22.8.2 DISTURBANCE RECORDS

Disturbance Records Measurement Accuracy	
Minimum record duration	0.1 s
Maximum record duration	10.5 s
Minimum number of records at 10.5 seconds	100
Magnitude and relative phases accuracy	+/- 5% of applied quantities
Duration accuracy	+/- 2%
Trigger position accuracy	+/- 2% (minimum Trigger 100 ms)

22.8.3 EVENT, FAULT AND MAINTENANCE RECORDS

Event, Fault & Maintenance Records	
Record location	Flash memory
Viewing method	Front panel display or Settings Application Software
Extraction method	Extracted via USB, RP1, RP2, NIC (Ethernet) port
Number of event records	Up to 5000 time tagged event records (newest overwrites oldest)
Number of fault records	Up to 100
Number of maintenance records	Up to 10
Event time stamp resolution	1 ms

22.8.4 FAULT LOCATOR

Accuracy	
Fault Location	+/- 2% of line length Reference conditions: solid fault applied on line

22.9 RATINGS

22.9.1 AC MEASURING INPUTS

AC Measuring Inputs	
Nominal frequency	50 Hz or 60 Hz (settable)
Operating range	45 to 65 Hz
Phase rotation	ABC or CBA

22.9.2 CURRENT TRANSFORMER INPUTS

AC Current Inputs	
Nominal current (In)	1A or 5A
Nominal burden per phase	< 0.2 VA at In
AC current thermal withstand (5A input)	20 A (continuous operation) 150 A (for 10 s) 500 A (for 1 s)
AC current thermal withstand (1A input)	4 A (continuous operation) 30 A (for 10 s) 100 A (for 1 s)
Linearity	Standard: Linear up to 64 × In (non-offset AC current) Sensitive: Linear up to 2 × In (non-offset AC current)

22.9.3 VOLTAGE TRANSFORMER INPUTS

AC Voltage Inputs		
Version	100 V to 120 V (ph-ph)	380 V to 480 V (ph-ph)
Nominal burden per VT input *1	< 0.003 VA @ Vn (ph-n); Vn < 120/Ö3 V (ph-n) < 0.01 VA @ Vn (ph-n); Vn < 240/Ö3 V (ph-n)	< 0.02 VA @ Vn (ph-n); Vn < 440/3Ö V (ph-n) < 0.07 VA @ Vn (ph-n); Vn < 880/3Ö V (ph-n)
Linearity for each VT input	Linear up to 200 Vac rms	Linear up to 800 Vac rms
Continuous rating for each VT input	240 Vac rms	880 Vac rms
10 seconds rating for each VT input	312 Vac rms	1144 Vac rms

Note:
*Reference Conditions: *1 = Overfrequency operating range 50/60 Hz and over temperature range 20° +/- 5° C.*

22.9.4 AUXILIARY SUPPLY VOLTAGE

Nominal operating range	CORTEC option (DC only) 24 to 48 V DC CORTEC option (rated for AC or DC operation) 48 to 110 V DC 40 to 100 V AC rms CORTEC option (rated for AC or DC operation) 110 to 250 V DC 100 to 240 V AC rms
Maximum operating range	CORTEC option (DC only) 19 to 65 V DC CORTEC option (rated for AC or DC operation) 37 to 150 V DC 32 to 110 V AC rms CORTEC option (rated for AC or DC operation) 87 to 300 V DC 80 to 265 V AC rms
Frequency range for AC supply	45 to 65 Hz
Ripple	<15% for a DC supply (compliant with IEC 60255-26:2013)
Power up time	< 11 seconds

22.9.5 NOMINAL BURDEN

Quiescent burden	11.2 W or 22 VA
2nd rear communications port	1.25 W or 2.5 VA
Each relay output burden	0.13 W or 0.25 VA per output relay
Each opto-input burden (24 – 27 V)	0.065 W or 0.13 VA max
Each opto-input burden (30 – 34 V)	0.065 W or 0.13 VA max
Each opto-input burden (48 – 54 V)	0.125 W or 0.25 VA max
Each opto-input burden (110 – 125 V)	0.36 W or 0.72 VA max
Each opto-input burden (220 – 250 V)	0.9 W or 1.8 VA max

22.9.6 POWER SUPPLY INTERRUPTION

Standard	IEC 60255-26:2013 (DC and AC)
24-48V DC SUPPLY 100% interruption without de-energising	20 ms at 24 V (half and full load) 50 ms at 36 V (half and full load) 100 ms at 48 V (half and full load)
48-110V DC SUPPLY 100% interruption without de-energising	20 ms at 37V (half and full load) 50 ms at 60 V (half and full load) 100 ms at 72 V (half load) 100 ms at 85 V (full load) 200 ms at 110 V (half and full load)

110-250V DC SUPPLY 100% interruption without de-energising	20 ms at 87 V (half load) 50 ms at 110 V (half load) 50 ms at 98 V (full load) 100 ms at 160 V (half load) 100 ms at 135 V (full load) 200 ms at 210 V (half load) 200 ms at 174 V (full load)
40-100V AC SUPPLY 100% voltage dip without de-energising	50 ms at 32 V (half load) 10 ms at 32 V (full load)
100-240V AC SUPPLY 100% voltage dip without de-energising	50 ms at 80 V (full and half load)

Note:
Maximum loading = all inputs/outputs energised.

Note:
Quiescent or 1/2 loading = 1/2 of all inputs/outputs energised.

22.9.7 SUPERCAPACITOR

Discharge time	>14 days

22.10 INPUT/OUTPUT CONNECTIONS

22.10.1 ISOLATED DIGITAL INPUTS

Opto-isolated digital inputs (opto-inputs)	
Compliance	ESI 48-4
Rated nominal voltage	24 to 250 V dc
Operating range	19 to 265 V dc
Withstand	300 V dc
Recognition time with half-cycle ac immunity filter removed	< 2 ms
Recognition time with filter on	< 12 ms

22.10.1.1 NOMINAL PICKUP AND RESET THRESHOLDS

Nominal battery voltage	Logic levels: 60-80% DO/PU	Logic Levels: 50-70% DO/PU
24/27 V	Logic 0 < 16.2V, Logic 1 > 19.2V	Logic 0 <12V, Logic 1 > 16.8V
30/34	Logic 0 < 20.4V, Logic 1 > 24V	Logic 0 < 15V, Logic 1 > 21V
48/54	Logic 0 < 32.4V, Logic 1 > 38.4V	Logic 0 < 24V, Logic 1 > 33.6V
110/125	Logic 0 < 75V, Logic 1 > 88V	Logic 0 < 55.V, Logic 1 > 77V
220/250	Logic 0 < 150V, Logic 1 > 176V	Logic 0 < 110V, Logic 1 > 154V

Note:
Filter is required to make the opto-inputs immune to induced AC voltages.

22.10.2 STANDARD OUTPUT CONTACTS

Compliance	In accordance with IEC 60255-1:2009
Use	General purpose relay outputs for signalling, tripping and alarming
Rated voltage	300 V
Maximum continuous current	10 A
Short duration withstand carry	30 A for 3 s 250 A for 30 ms
Make and break, dc resistive	50 W
Make and break, dc inductive	62.5 W (L/R = 50 ms)
Make and break, ac resistive	2500 VA resistive (cos phi = unity)
Make and break, ac inductive	2500 VA inductive (cos phi = 0.7)
Make and carry, dc resistive	30 A for 3 s, 10000 operations (subject to a maximum load of 7500W))
Make, carry and break, dc resistive	4 A for 1.5 s, 10000 operations (subject to the above limit for make and break, dc resistive load)
Make, carry and break, dc inductive	0.5 A for 1 s, 10000 operations (subject to the above limit for make and break, dc inductive load)
Make, carry and break ac resistive	30 A for 200 ms, 2000 operations (subject to the above limits)

Make, carry and break ac inductive	10 A for 1.5 s, 10000 operations (subject to the above limits)
Loaded contact	10000 operations min.
Unloaded contact	100000 operations min.
Operate time	< 5 ms
Reset time	< 10 ms

22.10.3 HIGH BREAK OUTPUT CONTACTS

Compliance	In accordance with IEC 60255-1:2009
Use	For applications requiring high rupture capacity
Rated voltage	300 V
Maximum continuous current	10 A DC
Short duration withstand carry	30 A DC for 3 s 250 A for 30 ms
Make and break, dc resistive	7500 W
Make and break, dc inductive	2500 W (L/R = 50 ms)
Make and carry, dc resistive	30 A for 3 s, 10000 operations (subject to the above limits)
Make, carry and break, dc resistive	30 A for 3 s, 5000 operations (subject to the above limit for make and break, dc resistive load) 30 A for 200 ms, 10000 operations (subject to the above limit for make and break, dc resistive load)
Make, carry and break, dc inductive	10 A for 40 ms, 10000 operations (subject to the above limit for make and break, dc inductive load) 10 A for 20 ms (250V, 4 shots per second, subject to the above limit for make and break, dc inductive load)
Loaded contact	10,000 operations minimum.
Unloaded contact	100,000 operations minimum.
Operate time	< 0.2 ms
Reset time	< 8 ms
MOV Protection	Maximum voltage 330 V DC

22.10.4 WATCHDOG CONTACTS

Use	Non-programmable contacts for relay healthy/relay fail indication
Breaking capacity, dc resistive	30 W
Breaking capacity, dc inductive	15 W (L/R = 40 ms)
Breaking capacity, ac inductive	375 VA inductive (cos phi = 0.7)

22.11 MECHANICAL SPECIFICATIONS

22.11.1 PHYSICAL PARAMETERS

Case Types*	40TE 60TE 80TE
Weight (40TE case)	7 kg – 8 kg (depending on chosen options)
Weight (60TE case)	9 kg – 12 kg (depending on chosen options)
Weight (80TE case)	13 kg - 16 kg (depending on chosen options)
Dimensions in mm (w x h x l) (40TE case)	W: 206.0 mm H: 177.0 mm D: 243.1 mm
Dimensions in mm (w x h x l) (60TE case)	W: 309.6 mm H: 177.0 mm D: 243.1 mm
Dimensions in mm (w x h x l) (80TE case)	W 413.2 mm H 177.0 mm D 243.1 mm
Mounting	Panel, rack, or retrofit

Note:
**Case size is product dependent.*

22.11.2 ENCLOSURE PROTECTION

Against dust and dripping water (front face)	IP52 as per IEC 60529:1989/A2:2013
Protection against dust (whole case)	IP50 as per IEC 60529:1989/A2:2013
Protection for sides of the case (safety)	IP30 as per IEC 60529:1989/A2:2013
Protection for rear of the case (safety)	IP10 as per IEC 60529:1989/A2:2013

22.11.3 MECHANICAL ROBUSTNESS

Vibration test per EN 60255-21-1:1998	Response: class 2, Endurance: class 2
Shock and bump immunity per EN 60255-21-2:1988	Shock response: class 2, Shock withstand: class 1, Bump withstand: class 1
Seismic test per EN 60255-21-3: 1993	Class 2

22.11.4 TRANSIT PACKAGING PERFORMANCE

Primary packaging carton protection	ISTA 1C
Vibration tests	3 orientations, 7 Hz, amplitude 5.3 mm, acceleration 1.05g
Drop tests	10 drops from 610 mm height on multiple carton faces, edges and corners

22.12 TYPE TESTS

22.12.1 INSULATION

Compliance	IEC 60255-27: 2013
Insulation resistance	> 100 M ohm at 500 V DC (Using only electronic/brushless insulation tester)

22.12.2 CREEPAGE DISTANCES AND CLEARANCES

Compliance	IEC 60255-27: 2013
Pollution degree	3
Overvoltage category	III
Impulse test voltage (not RJ45)	5 kV
Impulse test voltage (RJ45)	1 kV

22.12.3 HIGH VOLTAGE (DIELECTRIC) WITHSTAND

IEC Compliance	IEC 60255-27: 2013
Between all independent circuits	2 kV ac rms for 1 minute
Between independent circuits and protective earth conductor terminal	2 kV ac rms for 1 minute
Between all case terminals and the case earth	2 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute
Across open contacts of changeover output relays	1 kV ac rms for 1 minute
Between all RJ45 contacts and protective earth	1 kV ac rms for 1 minute
Between all screw-type EIA(RS)485 contacts and protective earth	1 kV ac rms for 1 minute
ANSI/IEEE Compliance	ANSI/IEEE C37.90-2005
Across open contacts of normally open output relays	1.5 kV ac rms for 1 minute
Across open contacts of normally open changeover output relays	1 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute

22.12.4 IMPULSE VOLTAGE WITHSTAND TEST

Compliance	IEC 60255-27: 2013
Between all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between terminals of all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between all independent circuits and protective earth conductor terminal	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J

Note:
Exceptions are communications ports and normally-open output contacts, where applicable.

22.13 ENVIRONMENTAL CONDITIONS

22.13.1 AMBIENT TEMPERATURE RANGE

Compliance	IEC 60255-27: 2013
Test Method	IEC 60068-2-1:2007 and IEC 60068-2-2 2007
Operating temperature range	-25°C to +55°C (continuous)
Storage and transit temperature range	-25°C to +70°C (continuous)

22.13.2 TEMPERATURE ENDURANCE TEST

Temperature Endurance Test	
Test Method	IEC 60068-2-1: 2007 and 60068-2-2: 2007
Operating temperature range	-40°C (96 hours) +70°C (96 hours)
Storage and transit temperature range	-40°C (96 hours) +70°C (96 hours)

22.13.3 AMBIENT HUMIDITY RANGE

Compliance	IEC 60068-2-78: 2012 and IEC 60068-2-30: 2005
Durability	56 days at 93% relative humidity and +40°C
Damp heat cyclic	six (12 + 12) hour cycles, 93% RH, +25 to +55°C

22.13.4 CORROSIVE ENVIRONMENTS

Compliance, Industrial corrosive environment/poor environmental control	IEC 60068-2-42: 2003, IEC 60068-2-43: 2003, IEC 60068-2-52: 1996
Sulphur Dioxide, IEC 60068-2-42: 2003	21 days exposure to elevated concentrations (25ppm) of SO_2 at 75% relative humidity and +25°C
Hydrogen Sulphide, IEC 60068-2-43: 2003	21 days exposure to elevated concentrations (10ppm) of H_2S at 75% relative humidity and +25°C
Salt mist, IEC 60068-2-52: 1996	7 days, KB severity 3

22.14 ELECTROMAGNETIC COMPATIBILITY

22.14.1 1 MHZ BURST HIGH FREQUENCY DISTURBANCE TEST

Compliance	IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Differential test voltage (level 3)	1.0 kV

22.14.2 DAMPED OSCILLATORY TEST

Compliance	EN61000-4-18: 2011: Level 3, 100 kHz and 1 MHz. Level 4: 3 MHz, 10 MHz and 30 MHz, IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Common-mode test voltage (level 4)	4.0 kV
Differential mode test voltage	1.0 kV

22.14.3 IMMUNITY TO ELECTROSTATIC DISCHARGE

Compliance	IEC 60255-26:2013, IEC 61000-4-2:2009
Class 4 Condition	15 kV discharge in air to user interface, display, and exposed metalwork
Class 3 Condition	8 kV discharge in air to all communication ports

22.14.4 ELECTRICAL FAST TRANSIENT OR BURST REQUIREMENTS

Compliance	IEC 60255-26:2013, IEC 61000-4-4:2012
Applied to communication inputs	Amplitude: 2 kV, burst frequency 5 kHz and 100 KHz (level 4)
Applied to power supply and all other inputs except for communication inputs	Amplitude: 4 kV, burst frequency 5 kHz and 100 KHz (level 4)

22.14.5 SURGE WITHSTAND CAPABILITY

Compliance	IEEE/ANSI C37.90.1: 2012
Condition 1	4 kV fast transient and 2.5 kV oscillatory applied common mode and differential mode to opto inputs, output relays, CTs, VTs, power supply
Condition 2	4 kV fast transient and 2.5 kV oscillatory applied common mode to communications, IRIG-B

22.14.6 SURGE IMMUNITY TEST

Compliance	IEC 60255-26:2013, IEC 61000-4-5:2014+AMD1:2017
Pulse duration	Time to half-value: 1.2/50 µs
Between all groups and protective earth conductor terminal	Amplitude 4 kV
Between terminals of each group (excluding communications ports, where applicable)	Amplitude 2 kV

22.14.7 IMMUNITY TO RADIATED ELECTROMAGNETIC ENERGY

Compliance	IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010
Frequency band	80 MHz to 3.0 GHz
Spot tests at	80, 160, 380, 450, 900, 1850, 2150 MHz
Test field strength	10 V/m
Test using AM	1 kHz @ 80%
Compliance	IEEE/ANSI C37.90.2: 2004
Frequency band	80 MHz to 1 GHz
Spot tests at	80, 160, 380, 450 MHz
Waveform	1 kHz @ 80% am and pulse modulated
Field strength	35 V/m

22.14.8 RADIATED IMMUNITY FROM DIGITAL COMMUNICATIONS

Compliance	IEC 61000-4-3:2006 + A2:2010
Frequency bands	800 to 960 MHz, 1.4 to 2.0 GHz
Test field strength	30 V/m
Test using AM	1 kHz / 80%

22.14.9 RADIATED IMMUNITY FROM DIGITAL RADIO TELEPHONES

Compliance	IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010
Frequency bands	900 MHz and 1.89 GHz
Test field strength	10 V/m

22.14.10 IMMUNITY TO CONDUCTED DISTURBANCES INDUCED BY RADIO FREQUENCY FIELDS

Compliance	IEC 60255-26:2013, IEC 61000-4-6:2013 Level 3
Frequency bands	150 kHz to 80 MHz

Test disturbance voltage	10 V rms
Test using AM	1 kHz @ 80%
Spot tests	27 MHz and 68 MHz

22.14.11 MAGNETIC FIELD IMMUNITY

Compliance	IEC 61000-4-8:2009 Level 5 IEC 61000-4-9:2016 Level 5 IEC 61000-4-10:2016 Level 5
IEC 61000-4-8 test	100 A/m applied continuously, 1000 A/m applied for 3 s
IEC 61000-4-9 test	1000 A/m applied in all planes
IEC 61000-4-10 test	100 A/m applied in all planes at 100 kHz/1 MHz with a burst duration of 2 seconds

22.14.12 CONDUCTED EMISSIONS

Compliance	IEC 60255-26:2013, EN 55032: 2015+A1:2020
Power supply test 1	0.15 - 0.5 MHz, 79 dBµV (quasi peak) 66 dBµV (average)
Power supply test 2	0.5 – 30 MHz, 73 dBµV (quasi peak) 60 dBµV (average)
RJ45 test 1 (where applicable)	0.15 - 0.5 MHz, 97 dBµV (quasi peak) 84 dBµV (average)
RJ45 test 2 (where applicable)	0.5 – 30 MHz, 87 dBµV (quasi peak) 74 dBµV (average)

22.14.13 RADIATED EMISSIONS

Compliance	IEC 60255-26:2013
Test 1	30 – 230 MHz, 40 dBµV/m at 10 m measurement distance
Test 2	230 – 1 GHz, 47 dBµV/m at 10 m measurement distance
Test 3	1 – 2 GHz, 76 dBµV/m at 10 m measurement distance

22.14.14 POWER FREQUENCY

Compliance	IEC 60255-26:2013
Opto-inputs (Compliance is achieved using the opto-input filter)	300 V common-mode (Class A) 150 V differential mode (Class A)

Note:
Compliance is achieved using the opto-input filter.

22.15 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.

CE

22.15.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

22.15.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

22.15.3 R&TTE COMPLIANCE: 2014/53/EU

Radio and Telecommunications Terminal Equipment (R&TTE) directive 2014/53/EU.

Conformity is demonstrated by compliance to both the EMC directive and the Low Voltage directive, to zero volts.

22.15.4 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.

c UL us

APPENDIX A

ORDERING OPTIONS

CORTEC Order Code Matrix		1-3	4	5	6	7	8	9	10	11	12-13	14	15
Multi-Functional Line Terminal with Autoreclose/Check Syncronising		P84	1								**		
Model A: Single Breaker Application													
Model B: Breaker and a Half or Dual Breaker Appplication													
Nominal Auxiliary Supply Voltage													
24-54 Vdc				7									
48-125 Vdc (40-100 Vac)				8									
110-250 Vdc (100-240 Vac)				9									
CT and VT Ratings	Hardware Opt. Compatibility												
Model A: Autoreclose for one CB Dual rated CT(1/5A :100-120V)	All				1								
Model B: Autoreclose for one/two CB Dual rated CT(1/5A :100-120V)	All				3								
IEC 61850-9-2LE Redundant Sampled Analogue Values Ethernet - process bus model *	Options R, S, T only				C								
Hardware Options													
Standard - 1 x RS485 rear serial communications port provided with all ordering options (Courier, -103, DNP3 ready)						1							
With additional IRIG-B (Modulated)						2							
With additional IRIG-B (Modulated) & Serial Fibre Optic comms						4							
With 2nd Courier protocol Rear Port + IRIG-B modulated *						F							
Redundant Ethernet PRP/HSR/RSTP/Failover: 2 multi-mode fibre ports + Modulated/Un-Modulated IRIG-B *						R							
Redundant Ethernet PRP/HSR/RSTP/Failover: 2 copper ports RJ45 + Modulated/Un-Modulated IRIG-B *						S							
Single and Redundant Ethernet Failover: 1 copper port RJ45 + 1 multi-mode fibre port + Modulated/Un-Modulated IRIG-B *						T							
Single Ethernet 1 LC Duplex port + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port **						U							
Redundant Ethernet PRP/HSR/RSTP/Failover 2 LC Duplex port + IEC870-103 Serial Fibre ST ports + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port **						V							
Redundant Ethernet PRP/HSR/RSTP/Failover 2 RJ45 + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port **						W							
Redundant Ethernet PRP/HSR/RSTP/Failover 2 LC Duplex ports + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port **						Y							
*** only available with SW AA**													
**** only available with SW AB**													
Input/Output Options	Case Size Compatibility												
8 inputs, 7 outputs	40TE, 60TE						A						
8 inputs, 8 outputs	40TE, 60TE						B						
8 inputs, 14 outputs	60TE						C						
12 inputs, 12 outputs	60TE						E						
16 inputs, 14 outputs	60TE						G						
16 inputs, 16 outputs	60TE						H						
16 inputs, 16 outputs + 4 High-Speed High-Break	60TE P841A only, 80TE						J						
16 inputs, 21 outputs	60TE P841A only, 80TE						K						
16 inputs, 24 outputs	P841A only 60TE, 80TE						L						
20 inputs, 20 outputs **	P841A only 60TE, 80TE						P						
24 inputs, 16 outputs **	P841A only 60TE, 80TE						S						
24 inputs, 16 outputs + 8 High-Speed High-Break	80TE						T						
24 inputs, 24 outputs **	80TE						U						
24 inputs, 32 outputs	80TE						V						
28 inputs, 43 outputs	P841A only - 80TE						Y						
32 inputs, 24 outputs **	80TE						1						
32 inputs, 32 outputs	P841A only - 80TE						2						
40 inputs, 24 outputs	P841A only - 80TE						4						
40 inputs, 32 outputs **	P841A only - 80TE						5						
Product Specific Options													
Standard Version								A					
Case Size and Mounting	Product Compatibility												
80TE Case - Flush/Panel Mounting with Harsh Env. Coating, with USB Port and 10 Function Keys	P841A, P841B								S				
80TE Case - 19" Rack Mounting with Harsh Env. Coating, with USB Port and 10 Function Keys 40TE	P841A, P841B								T				
Case - Flush/Panel Mounting with Harsh Env. Coating, with USB Port, without Function Keys 60TE	P841A. P841B with IEC 61850-9-2LE								U				
Case - Flush/Panel Mounting with Harsh Env. Coating, with USB Port and 10 Function Keys	P841A, P841B								V				
Product Features													
Single Breaker										A			
Breaker and a Half or Dual Breaker Appplication										B			
Software Version													
Major Version - please Visit Online store to select											**		
Customer-Specific Additions Standard													
version												0	
Customer-specific configuration/options												A	
Hardware Version													
5th Generation Hardware, Graphical Colour HMI with High Performance Processing													Q

APPENDIX B

SETTINGS AND SIGNALS

Tables, containing a full list of settings for each model, are provided in a separate Excel file attached as an embedded resource. To access the spreadsheet file, click on the button below.

Note:
An Open File dialogue box may open with a warning message about potential harm from programs, macros or viruses. The file supplied does not contain any harmful content, and may be safely opened.

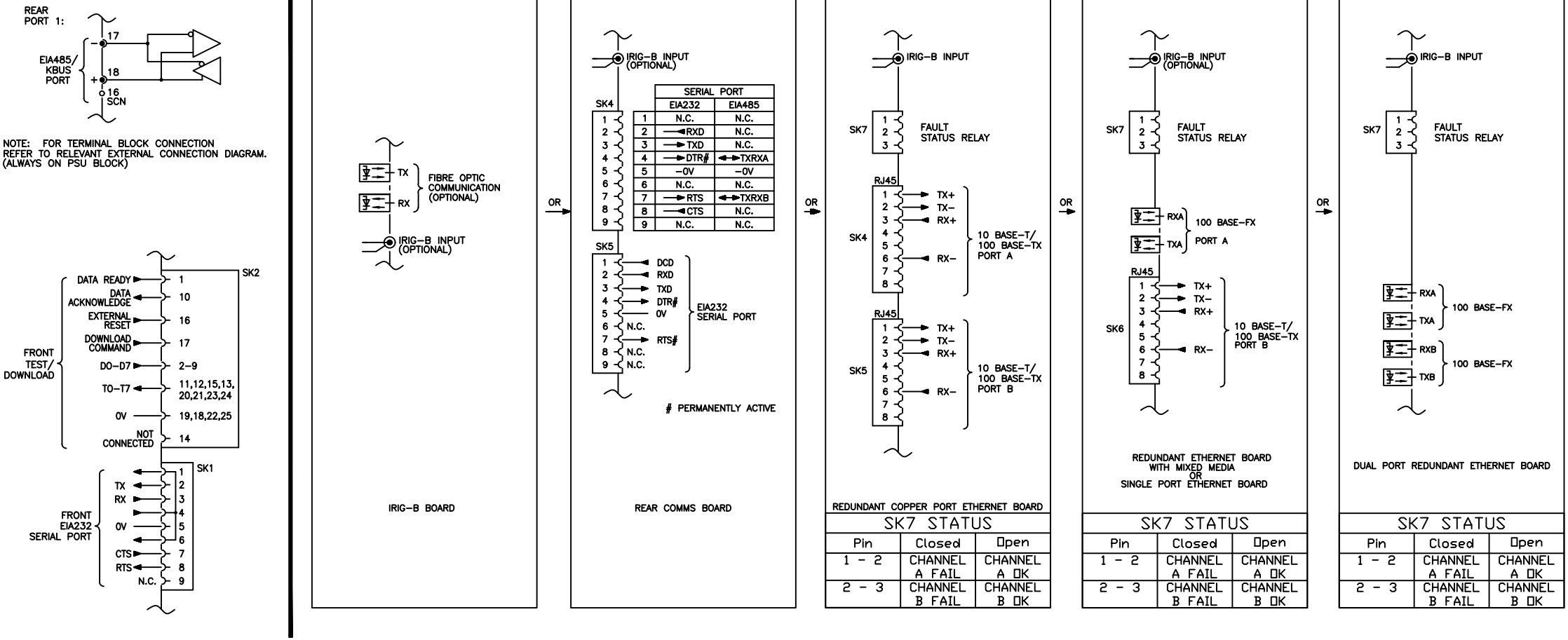
Settings and Signals

APPENDIX C

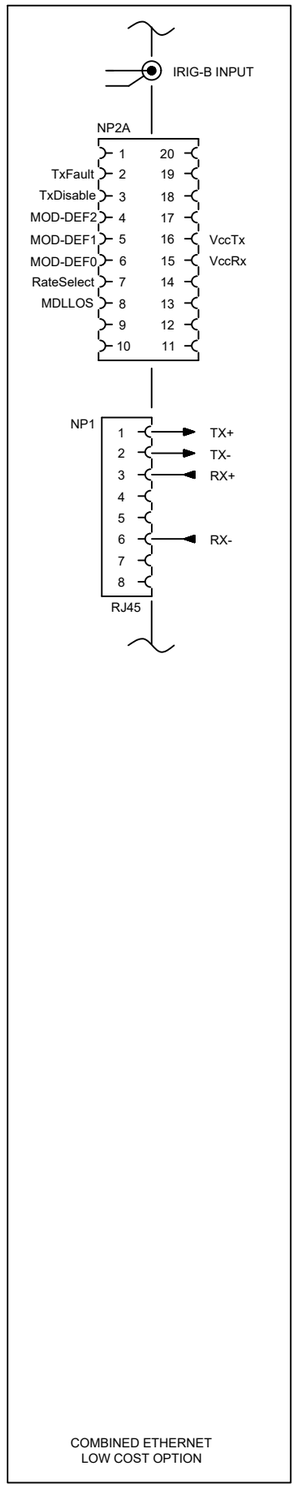
WIRING DIAGRAMS

Model	CORTEC Option*	Input/Output Options and Case Size Compatibility	Drawing-Sheet	Issue
All	-	Comms Options MiCOM Px40 Platform	10Px4001-1 10Px4001-2	N A
P841	I/O Option A	8 Inputs, 7 Outputs (40TE)	10P84140-1	A
	I/O Option A	8 Inputs, 7 Outputs (60TE)	10P84112-1	A
	I/O Option B	8 Inputs, 8 Outputs (40TE)	10P84141-1	C
	I/O Option B	8 Inputs, 8 Outputs (60TE)	10P84113-1	A
	I/O Option B	8 Inputs, 8 Outputs (60TE)	10P84156-1	C
	I/O Option C	8 Inputs, 14 Outputs (60TE)	10P84114-1	A
	I/O Option C	8 Inputs, 14 Outputs (60TE)	10P84157-1	C
	I/O Option E	12 Inputs, 12 Outputs (60TE)	10P84115-1	A
	I/O Option E	12 Inputs, 12 Outputs (60TE)	10P84158-1	C
	I/O Option G	16 Inputs, 14 Outputs (60TE)	10P84116-1	C
	I/O Option G	16 Inputs, 14 Outputs (60TE)	10P84159-1	C
	I/O Option H	16 Inputs, 16 Outputs (60TE)	10P84117-1	A
	I/O Option H	16 Inputs, 16 Outputs (60TE)	10P84160-1	C
	I/O Option J	16 Inputs, 16 Outputs + 4 High-Speed High-Break (60TE)	10P84118-1	A
	I/O Option J	16 Inputs, 16 Outputs + 4 High-Speed High-Break (80TE)	10P84142-1	A
	I/O Option J	16 Inputs, 16 Outputs + 4 High-Speed High-Break (80TE)	10P84147-1	A
	I/O Option K	16 Inputs, 21 Outputs (60TE)	10P84119-1	A
	I/O Option K	16 Inputs, 21 Outputs (80TE)	10P84143-1	A
	I/O Option K	16 Inputs, 21 Outputs (80TE)	10P84148-1	A
	I/O Option L	16 Inputs, 24 Outputs (60TE)	10P84120-1	A
	I/O Option P	20 Inputs, 20 Outputs (60TE)	10P84195-1	A
	I/O Option P	20 Inputs, 20 Outputs (80TE)	10P84176-1	A
	I/O Option P	20 Inputs, 20 Outputs (80TE)	10P84185-1	A
	I/O Option S	24 Inputs, 16 Outputs (60TE)	10P84198-1	A
	I/O Option S	24 Inputs, 16 Outputs (80TE)	10P84187-1	A
	I/O Option T	24 Inputs, 16 Outputs + 8 High-Speed High-Break (80TE)	10P84145-1	A
	I/O Option T	24 Inputs, 16 Outputs + 8 High-Speed High-Break (80TE)	10P84150-1	A
	I/O Option U	24 Inputs, 24 Outputs (80TE)	10P84179-1	A
	I/O Option U	24 Inputs, 24 Outputs (80TE)	10P84188-1	A
	I/O Option V	24 Inputs, 32 Outputs (80TE)	10P84146-1	B
	I/O Option V	24 Inputs, 32 Outputs (80TE)	10P84151-1	A
	I/O Option Y	28 Inputs, 43 Outputs (80TE)	10P84154-1	B
	I/O Option 1	32 Inputs, 24 Outputs (80TE)	10P84181-1	A
	I/O Option 1	32 Inputs, 24 Outputs (80TE)	10P84190-1	A
	I/O Option 2	32 Inputs, 32 Outputs (80TE)	10P84152-1	A
	I/O Option 4	40 Inputs, 24 Outputs (80TE)	10P84153-1	A
	I/O Option 5	40 Inputs, 32 Outputs (80TE)	10P84191-1	A

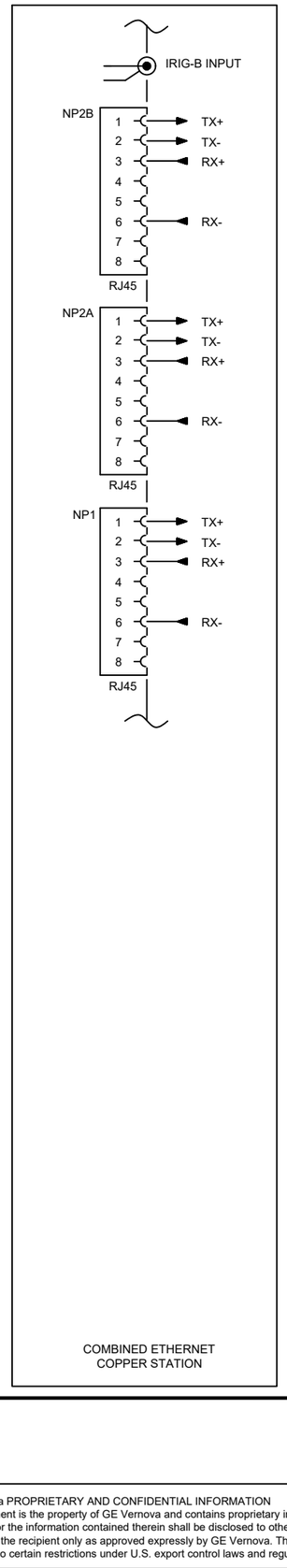
* When selecting the applicable wiring diagram(s), refer to the appropriate model CORTEC.



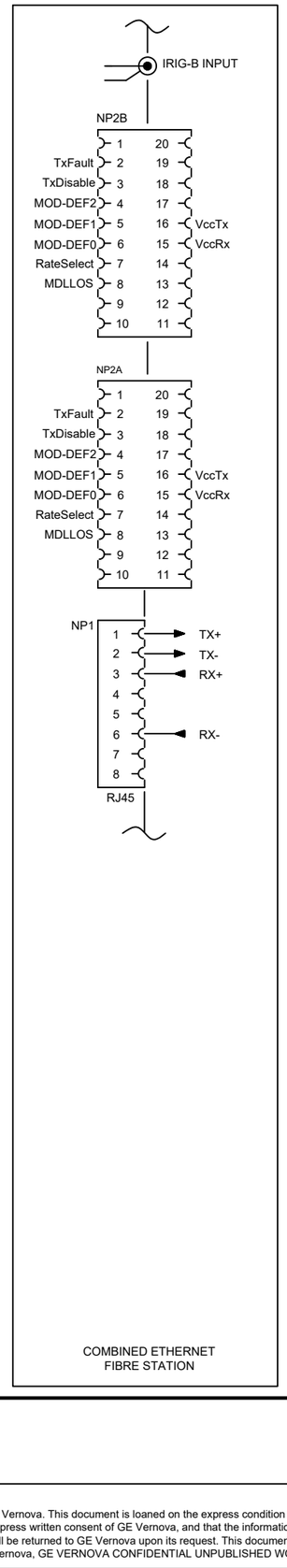
Issue: N	Revision: SHEET 2 ADDED. CID008142.		Title: EXTERNAL CONNECTION DIAGRAM: COMMS OPTIONS MICOM Px40 PLATFORM	
Date: 17/07/2024	Name: S WOOTTON	GE Vernova PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova and contains proprietary information of GE Vernova. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE Vernova, and that the information shall be used by the recipient only as approved expressly by GE Vernova. This document shall be returned to GE Vernova upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE Vernova, GE VERNOVA CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10PX4001	Sht: 1 Next Sht: 2
Date:	Chkd:			GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.



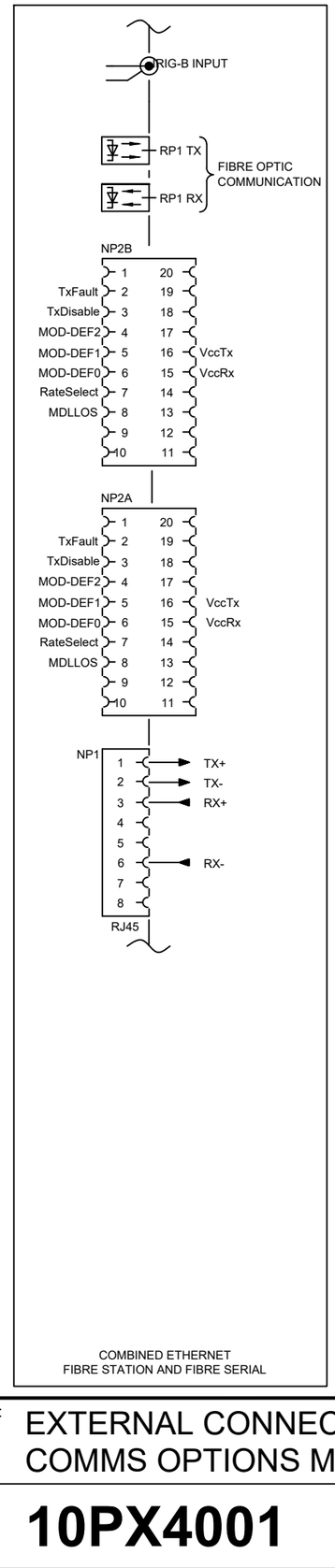
COMBINED ETHERNET
LOW COST OPTION



COMBINED ETHERNET
COPPER STATION

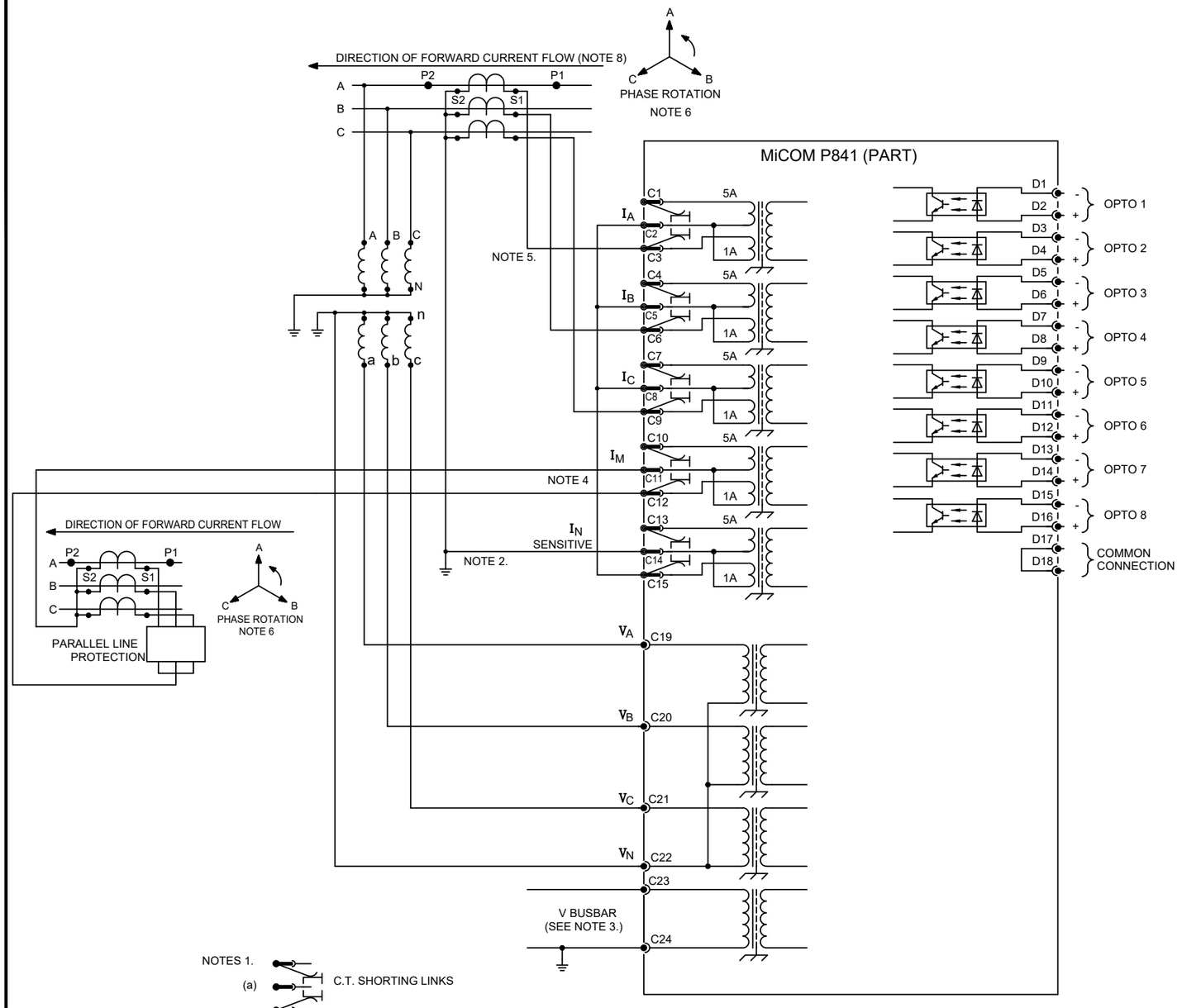


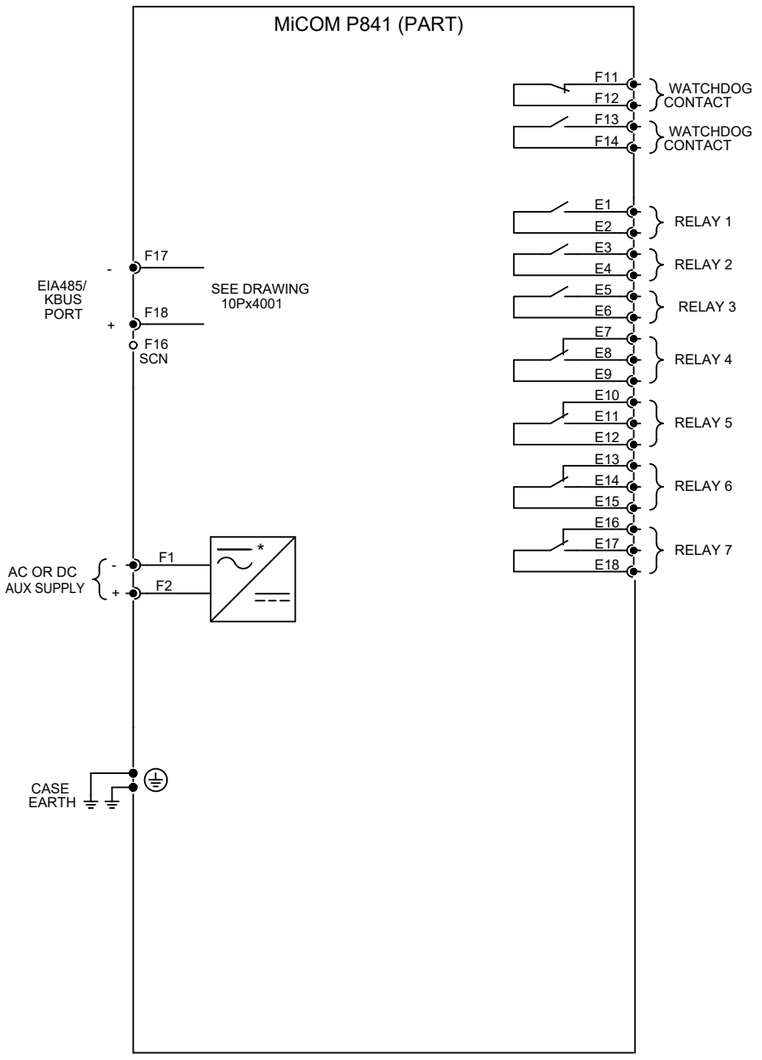
COMBINED ETHERNET
FIBRE STATION



COMBINED ETHERNET
FIBRE STATION AND FIBRE SERIAL

Issue: A	Revision: INITIAL ISSUE. CID008142		Title: EXTERNAL CONNECTION DIAGRAM COMMS OPTIONS MICOM Px40		
Date: 27/06/2024	Name: S WOOTTON		Drg No: 10PX4001	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

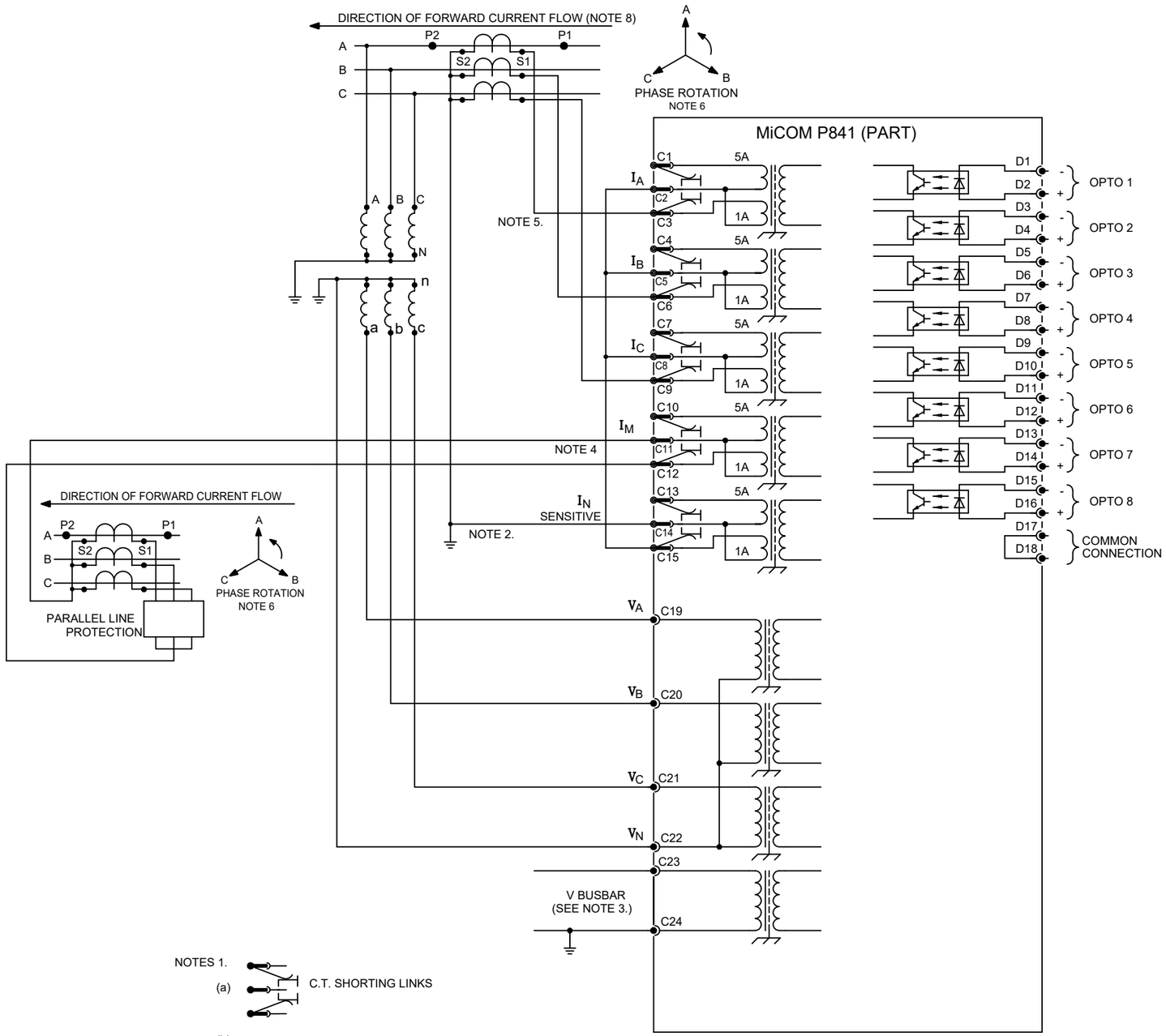
50 OHM BNC CONNECTOR

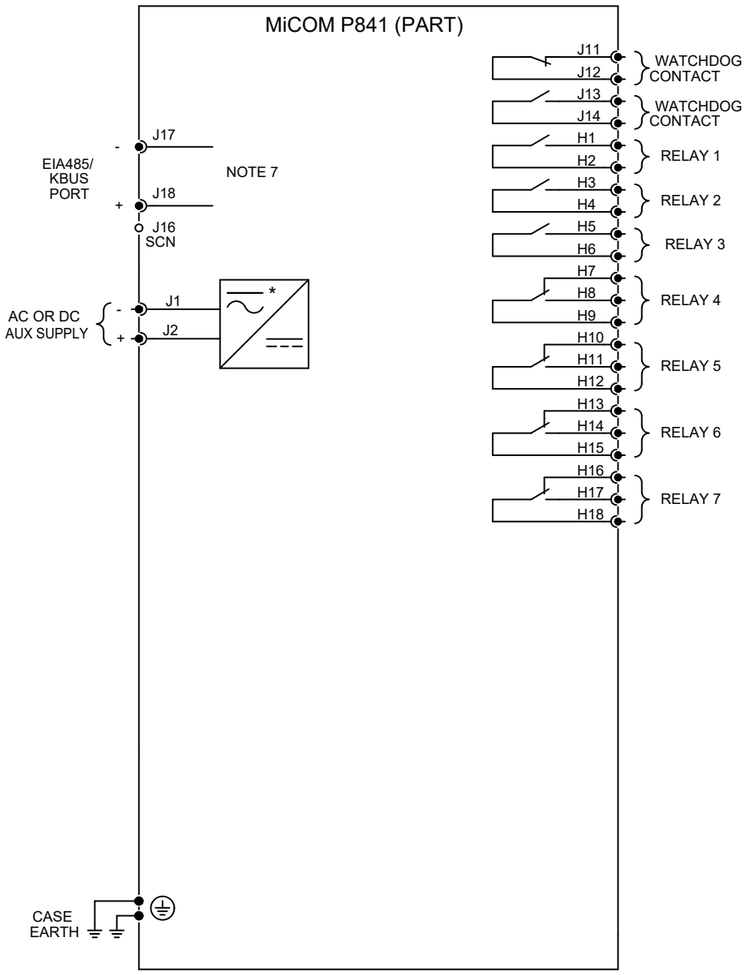
9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008091. CURRENT DIFF CONNECTIONS REMOVED. ADDED IN ERROR		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE 40TE 8I/7O		
Date: 30/11/2023	Name: S WOOTTON		Drg No: 10P84140	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

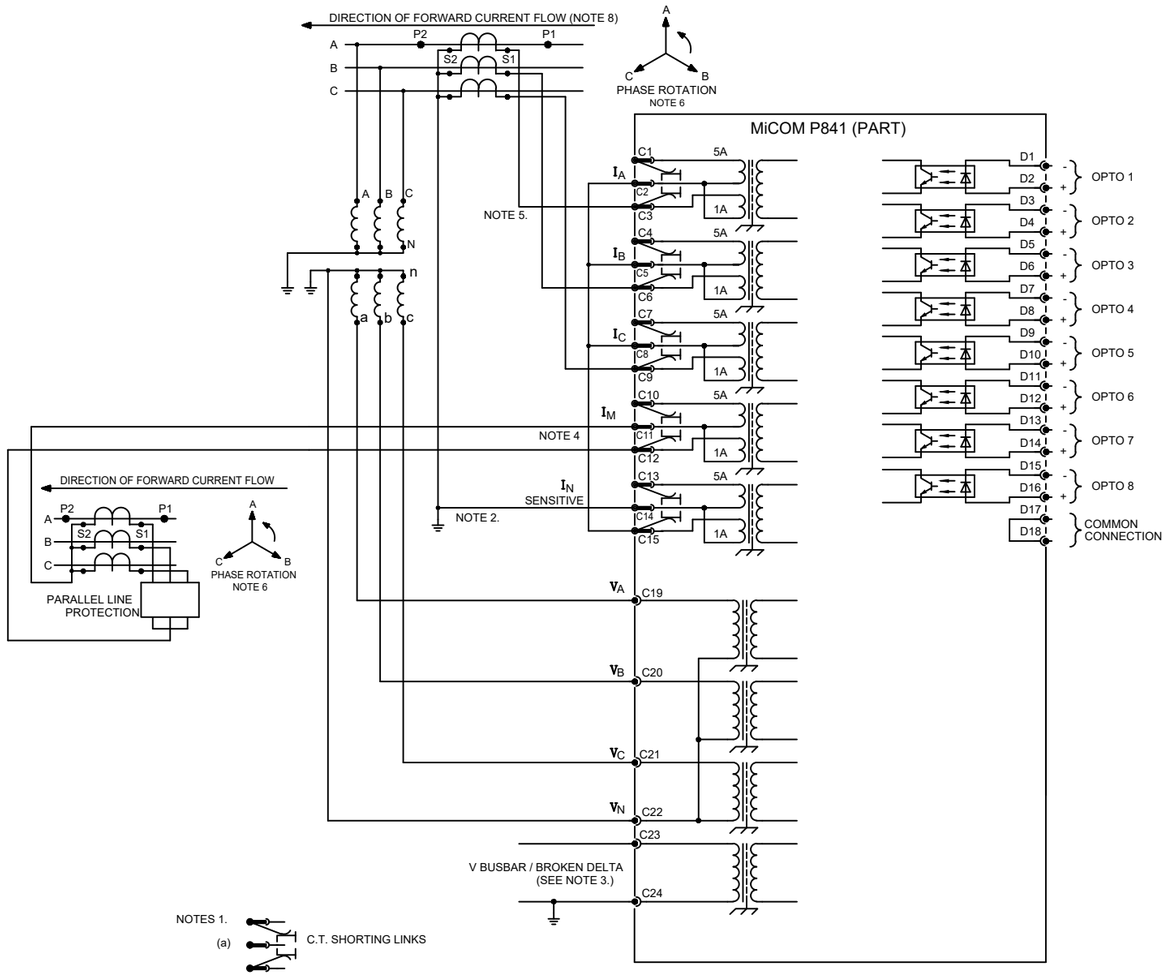
(b) PIN TERMINAL (P.C.B. TYPE)

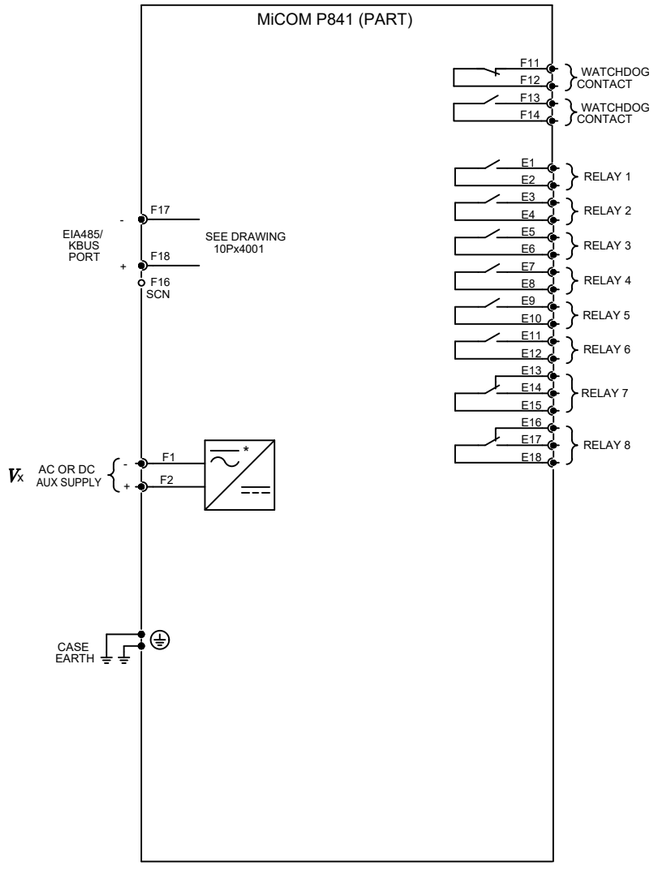
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Revision: CID008091. CURRENT DIFF CONNECTIONS REMOVED. ADDED IN ERROR		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 8I/7O		
Date: 18/08/2022	Name: S WOOTTON		Drg No: **10P84112**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

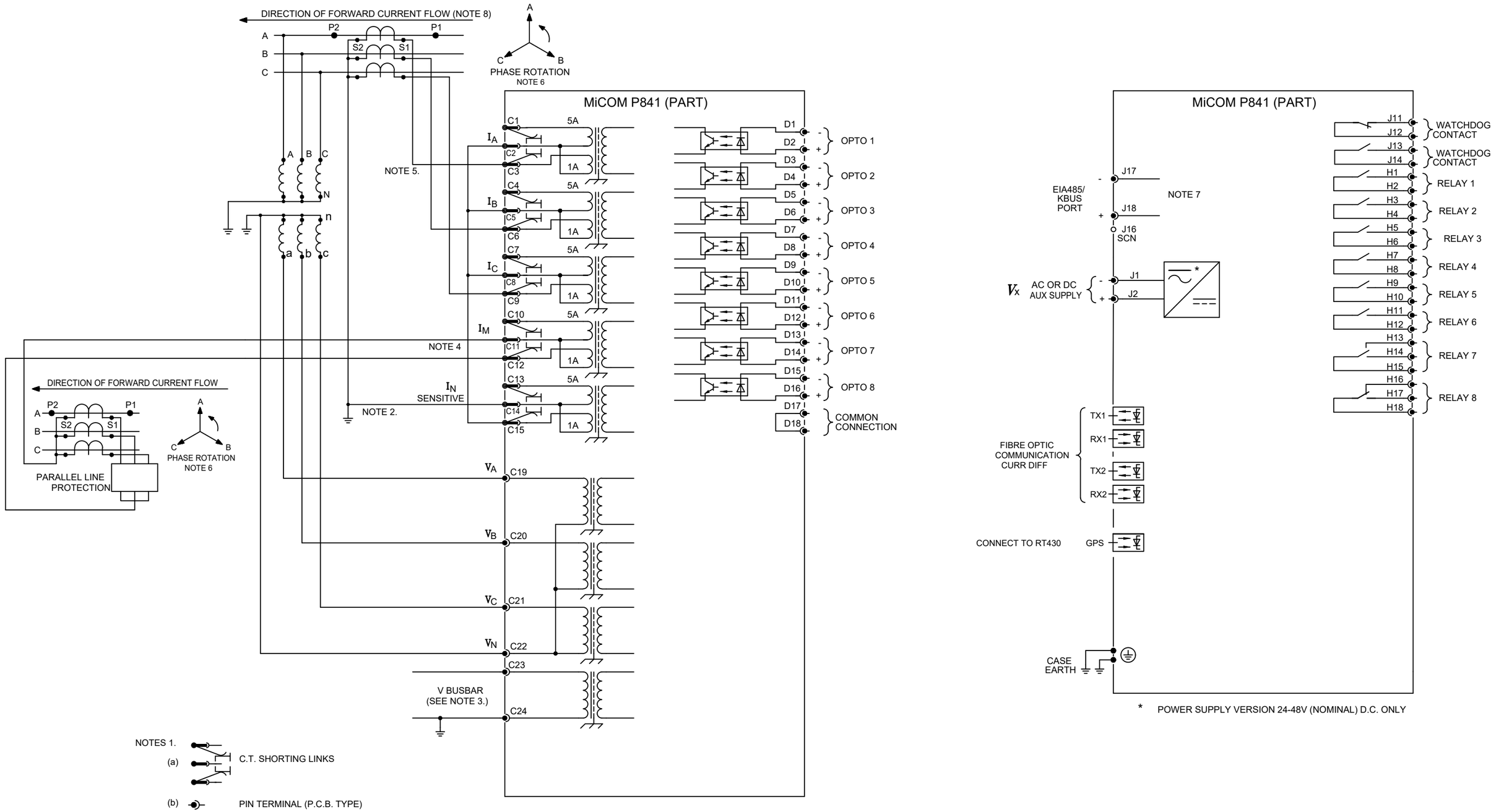
9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. 4TH/5TH VT BASED ON MODEL NUMBER CAN BE SELECTED FOR BROKEN DELTA ONCE SYSTEM CHECK IS DISABLED IN CONFIGURATION TAB.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: C	Revision: CID008444. Added information about Broken Delta		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (40TE) 8I/8O		
Date: 12/07/2024	Name: J.HUTCHINS		Drg No: 10P84141	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

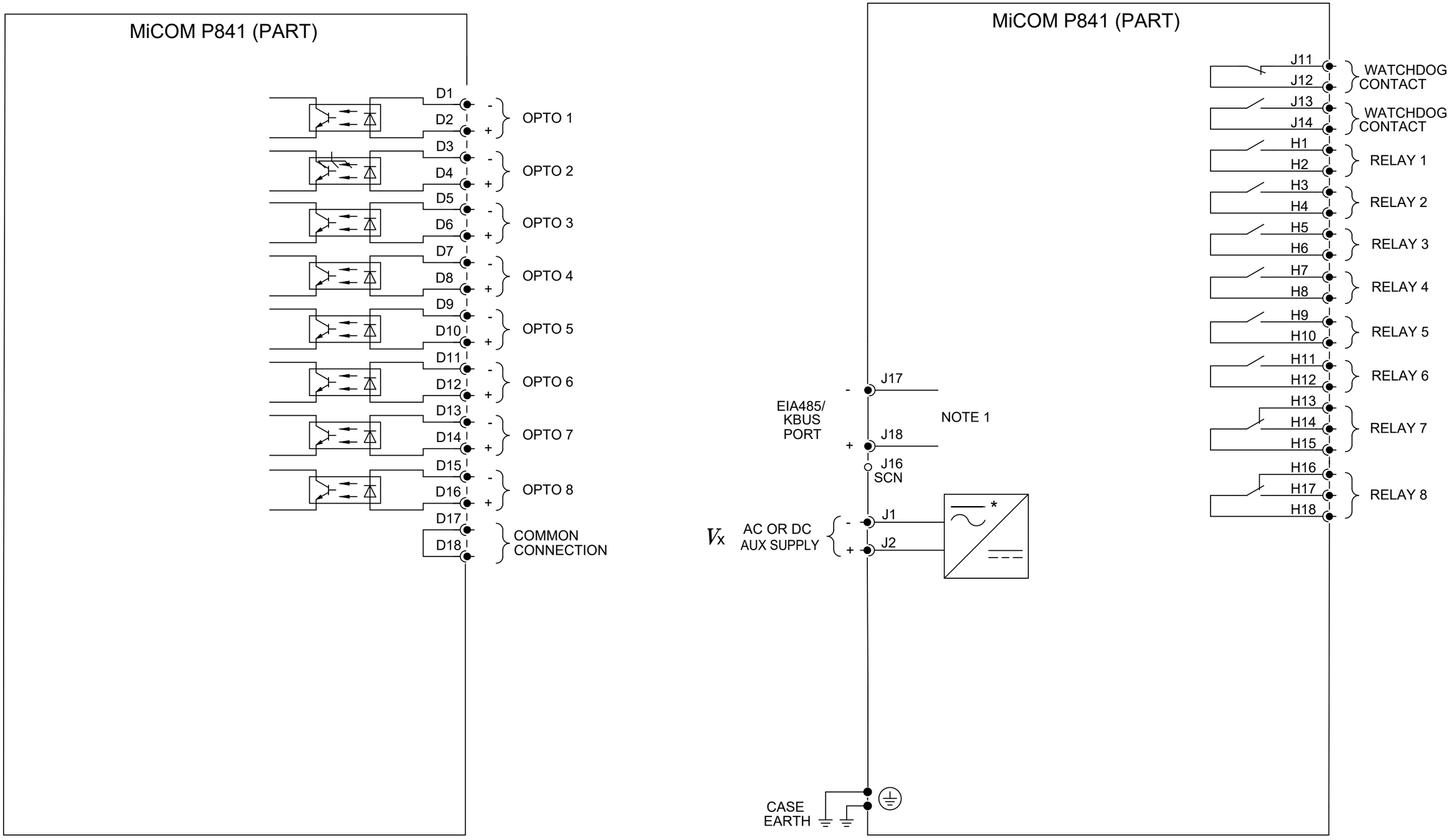
(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

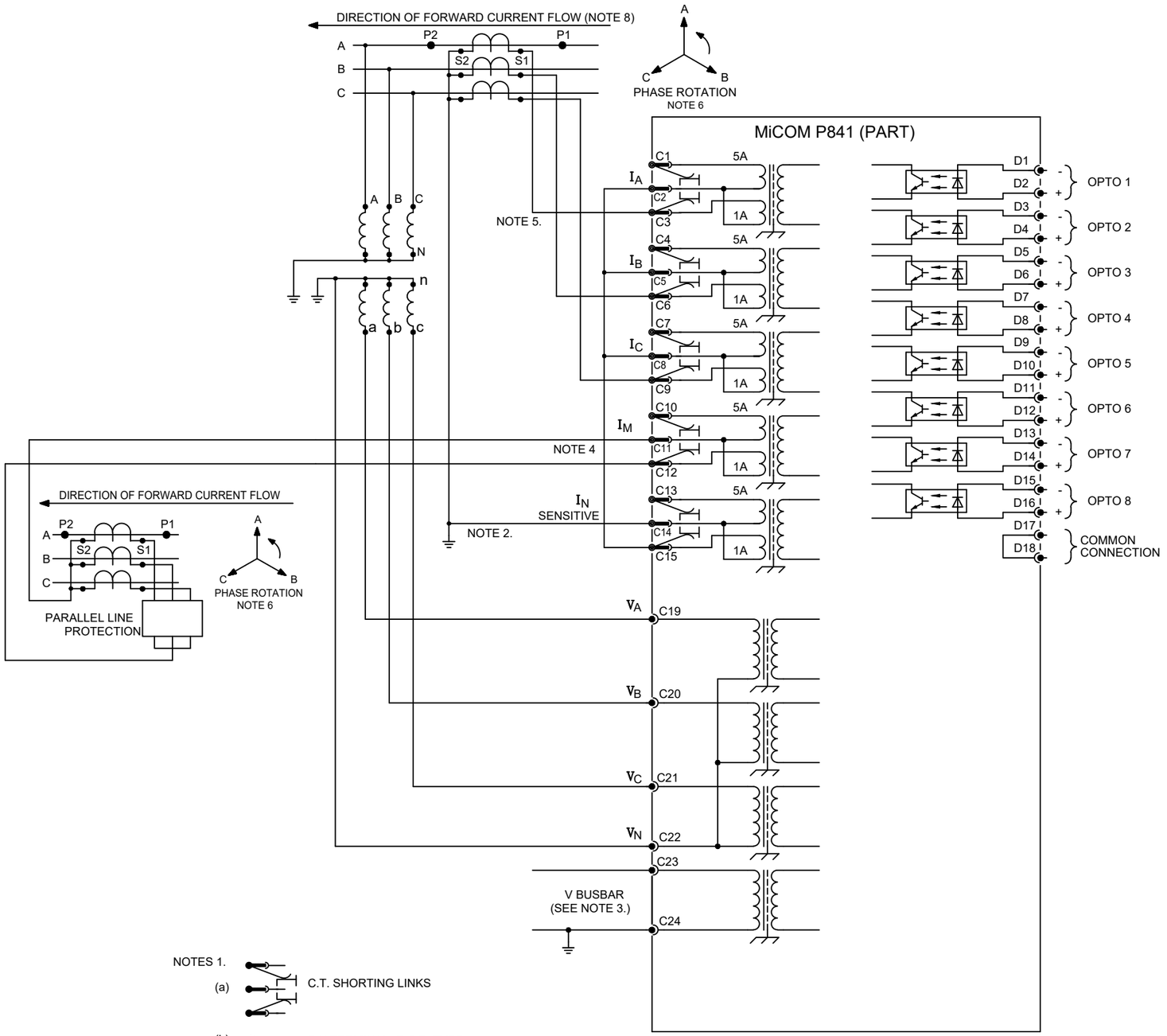
Issue: A	Revision: CID007390. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 8I/80		
Date: 18/08/2022	Name: S WOOTTON		Drg No: 10P84113	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	

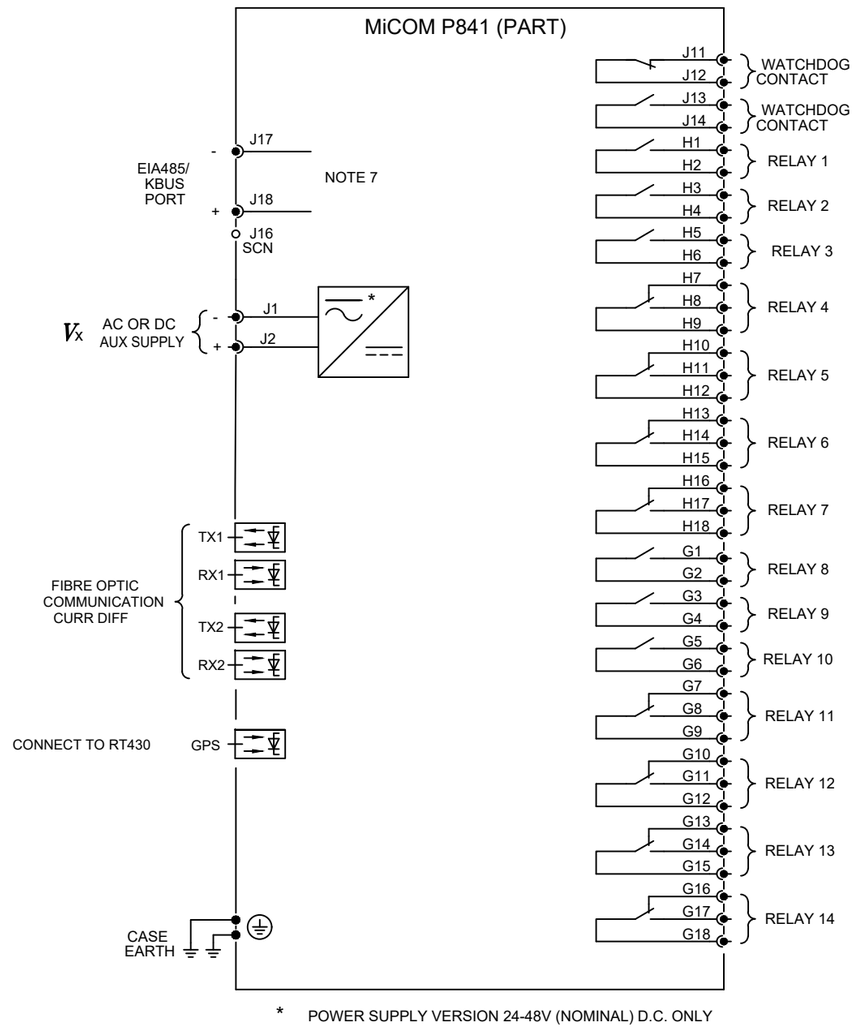


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
SEE 10P84199 FOR POWER SYSTEM CONNECTIONS

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE) ⊸

Issue: C	Revision: CID008455. NOTE REGARDING POWER SYSTEM CONNECTIONS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 8I/8O		
Date: 23/07/2024	Name: S WOOTTON		Drg No: 10P84156	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

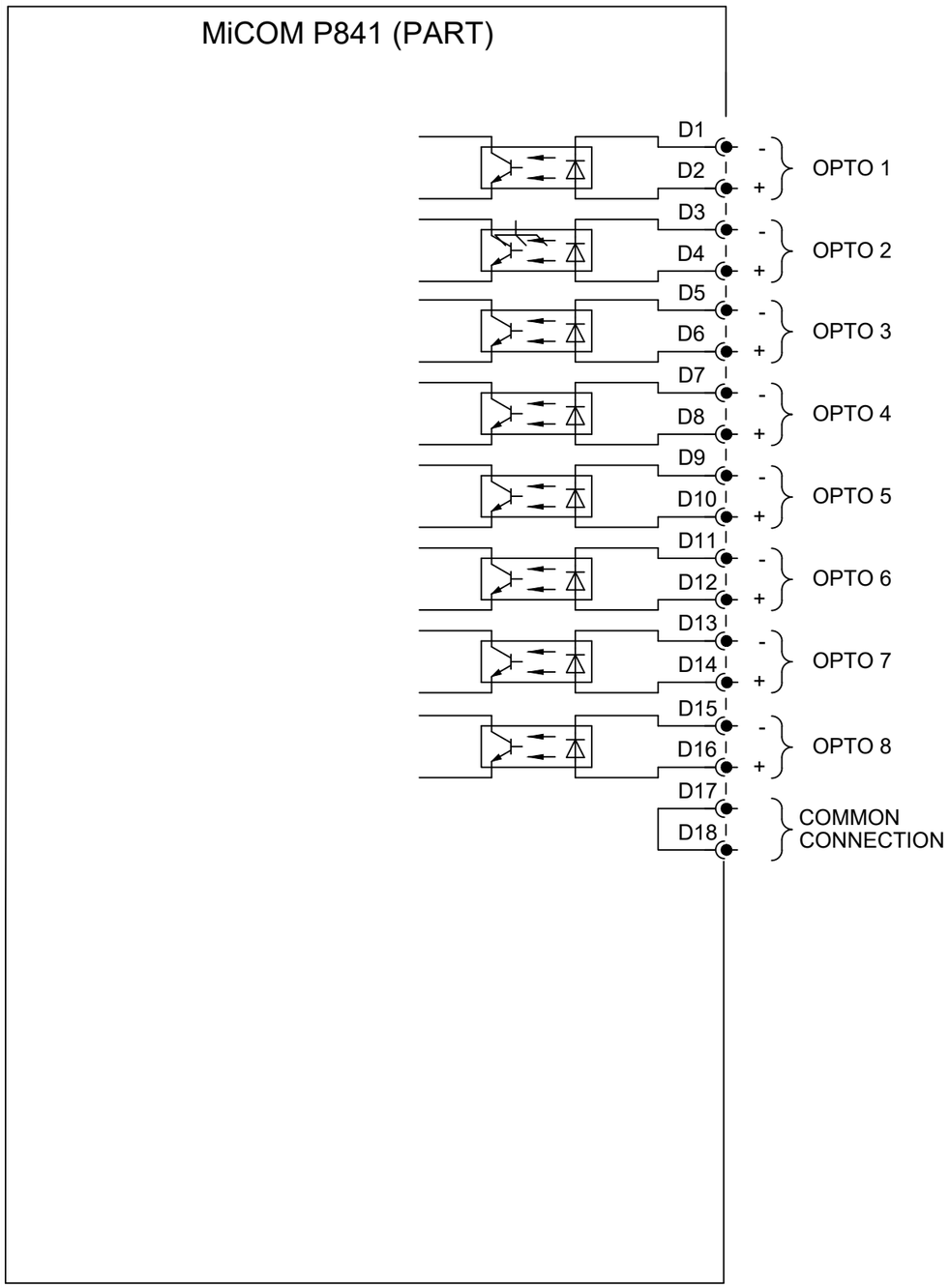
(b) PIN TERMINAL (P.C.B. TYPE)

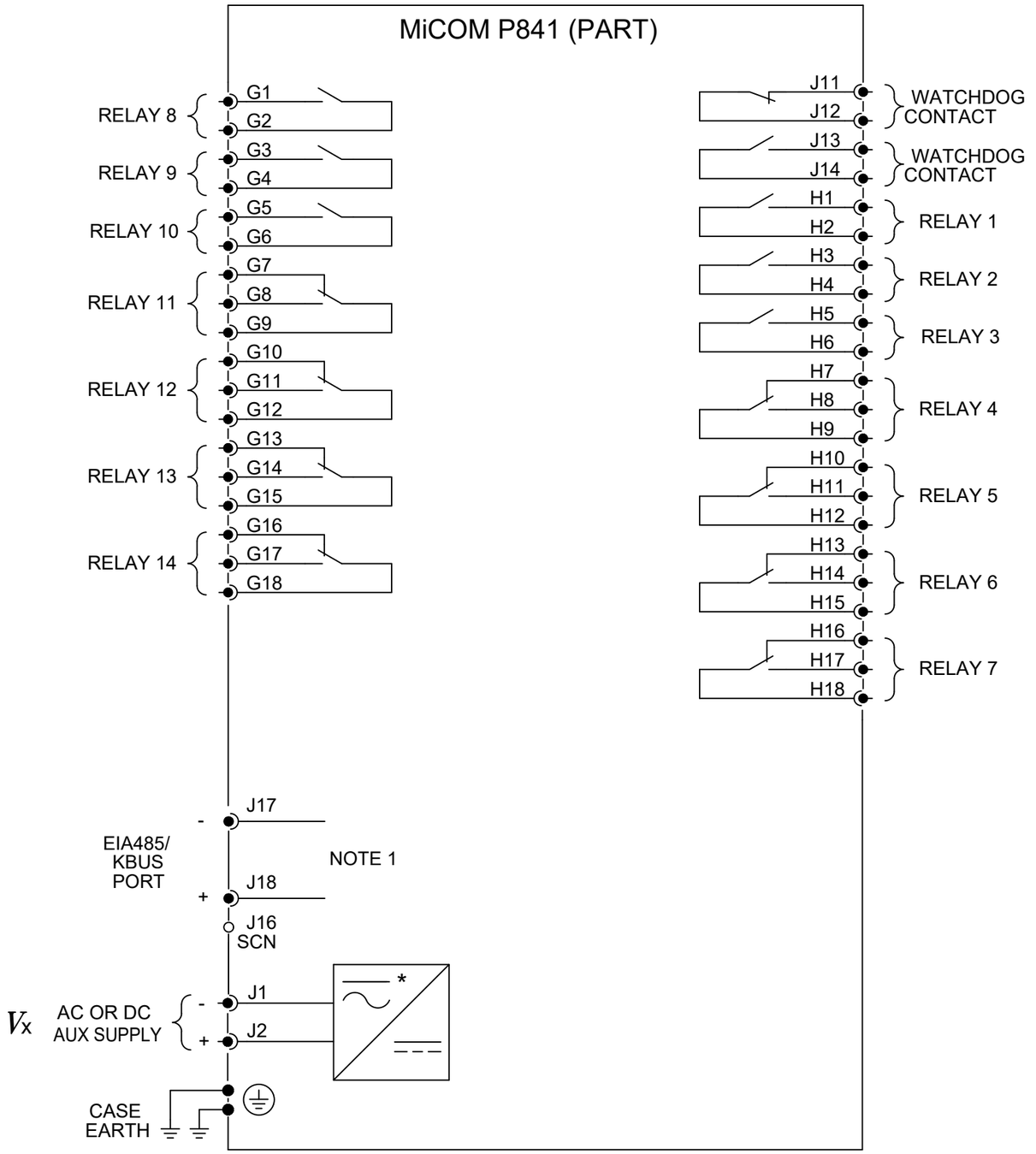
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: A	Revision: CID007390. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 8I/14O		
Date: 18/08/2020	Name: S WOOTTON		Drg No: **10P84114**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	

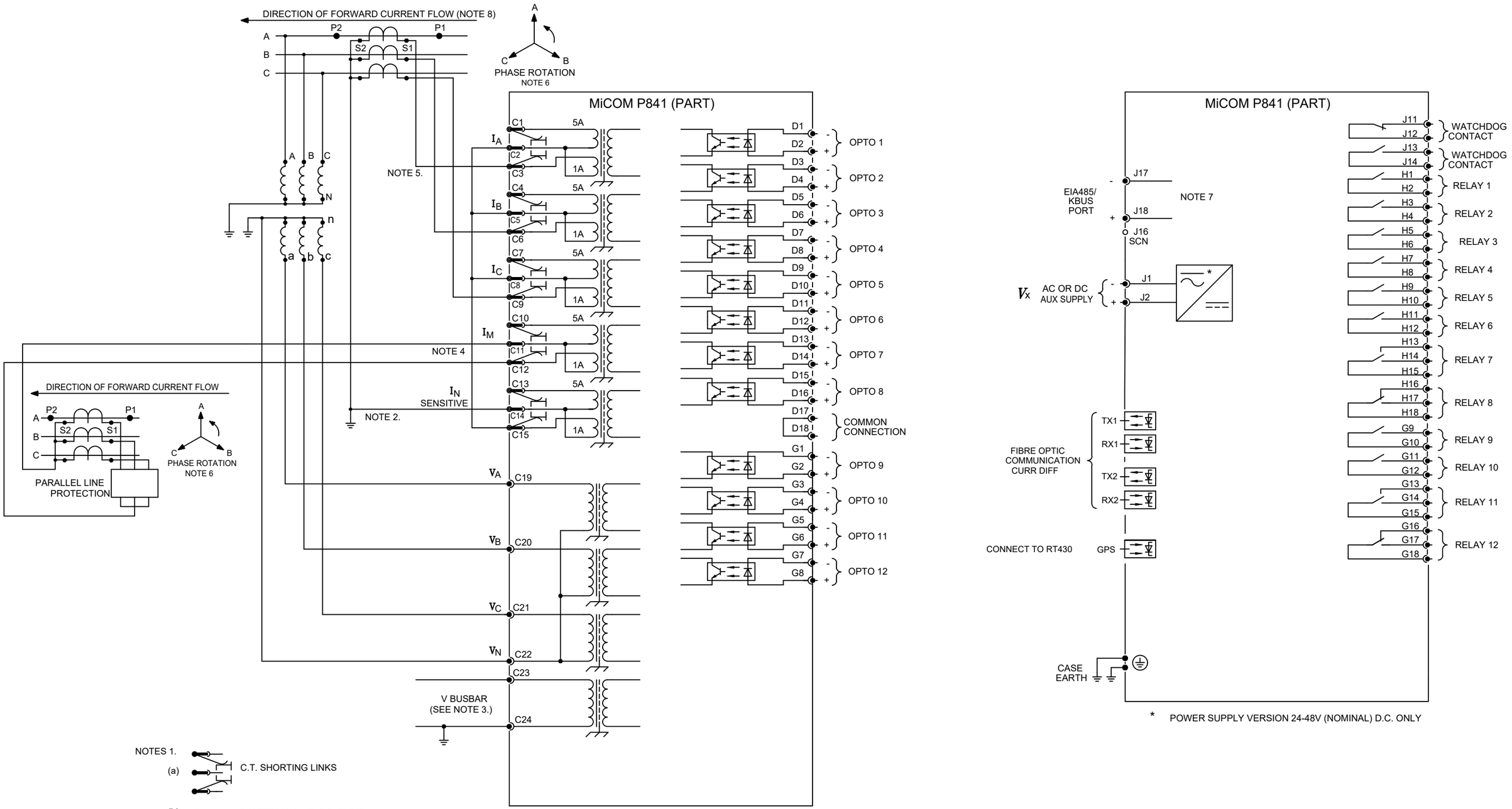




* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
SEE 10P84199 FOR POWER SYSTEM CONNECTIONS.

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE) –●–

Issue: C	Revision: CID008455. NOTE REGARDING POWER SYSTEM CONNECTIONS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 8I/14O		
Date: 23/07/2024	Name: S WOOTTON		Drg No: 10P84157	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

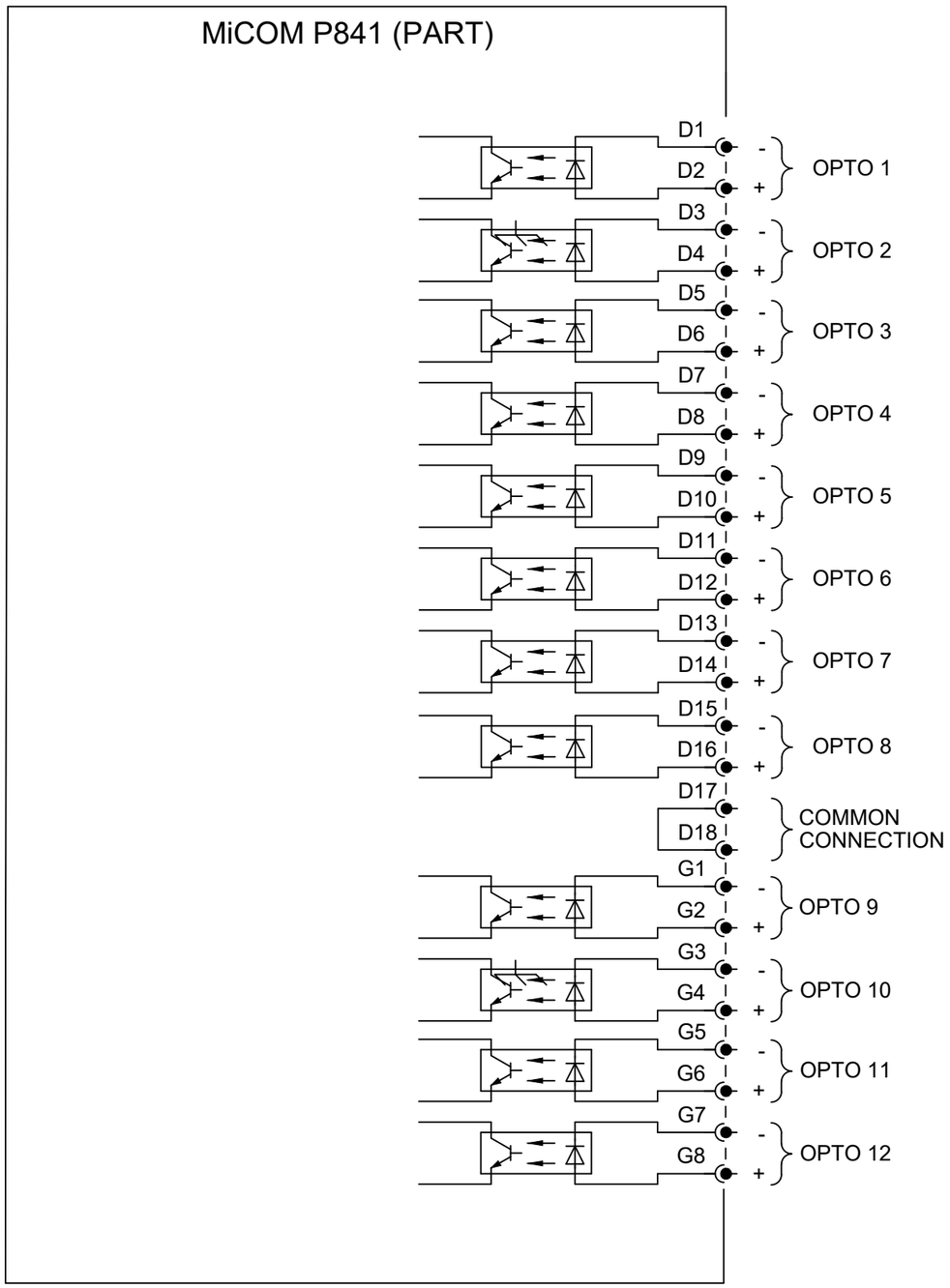
(b) PIN TERMINAL (P.C.B. TYPE)

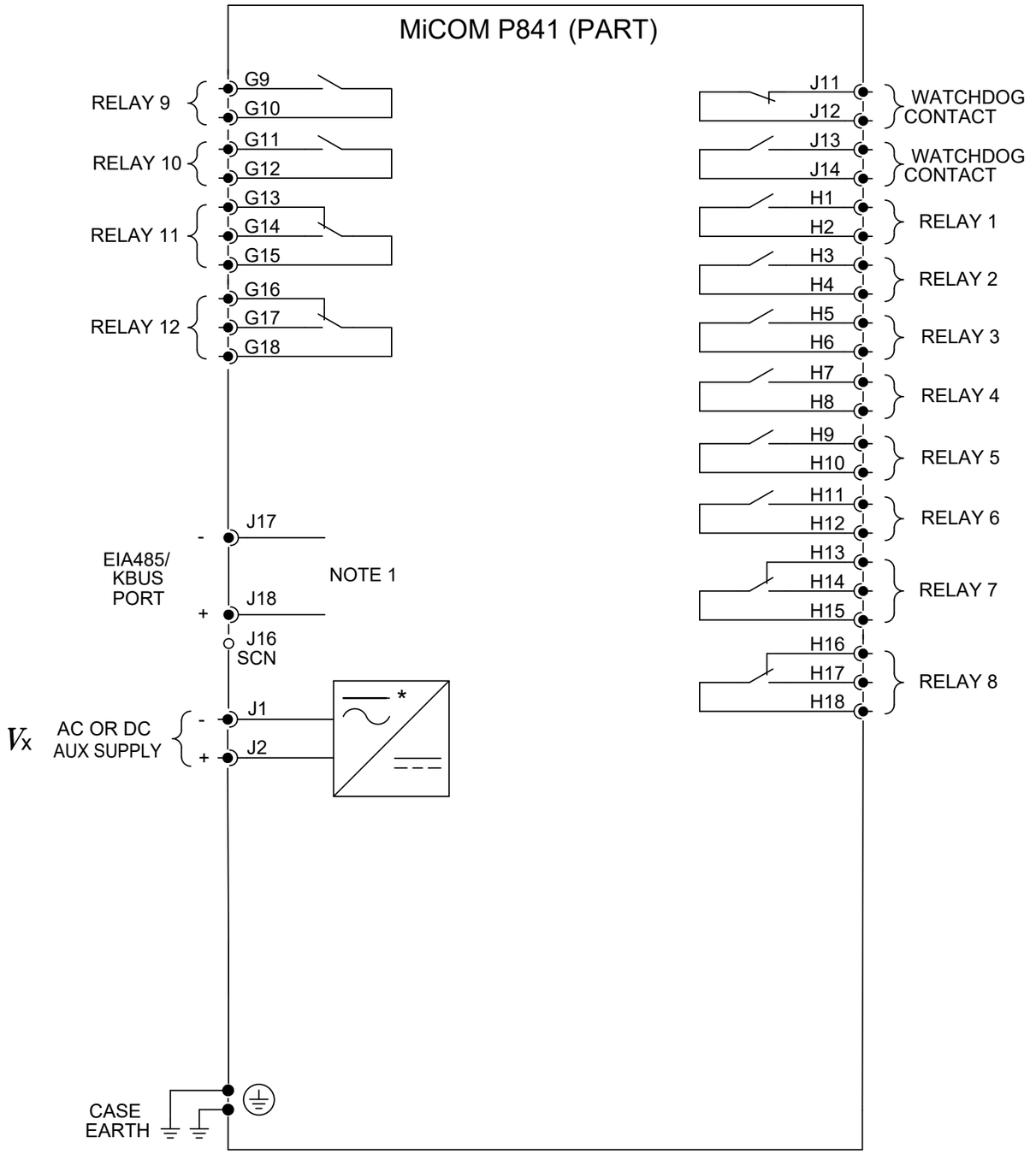
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: A	Revision: CID007390. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 12I/12O		
Date: 18/08/2022	Name: S WOOTTON		Drg No: 10P84115	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	

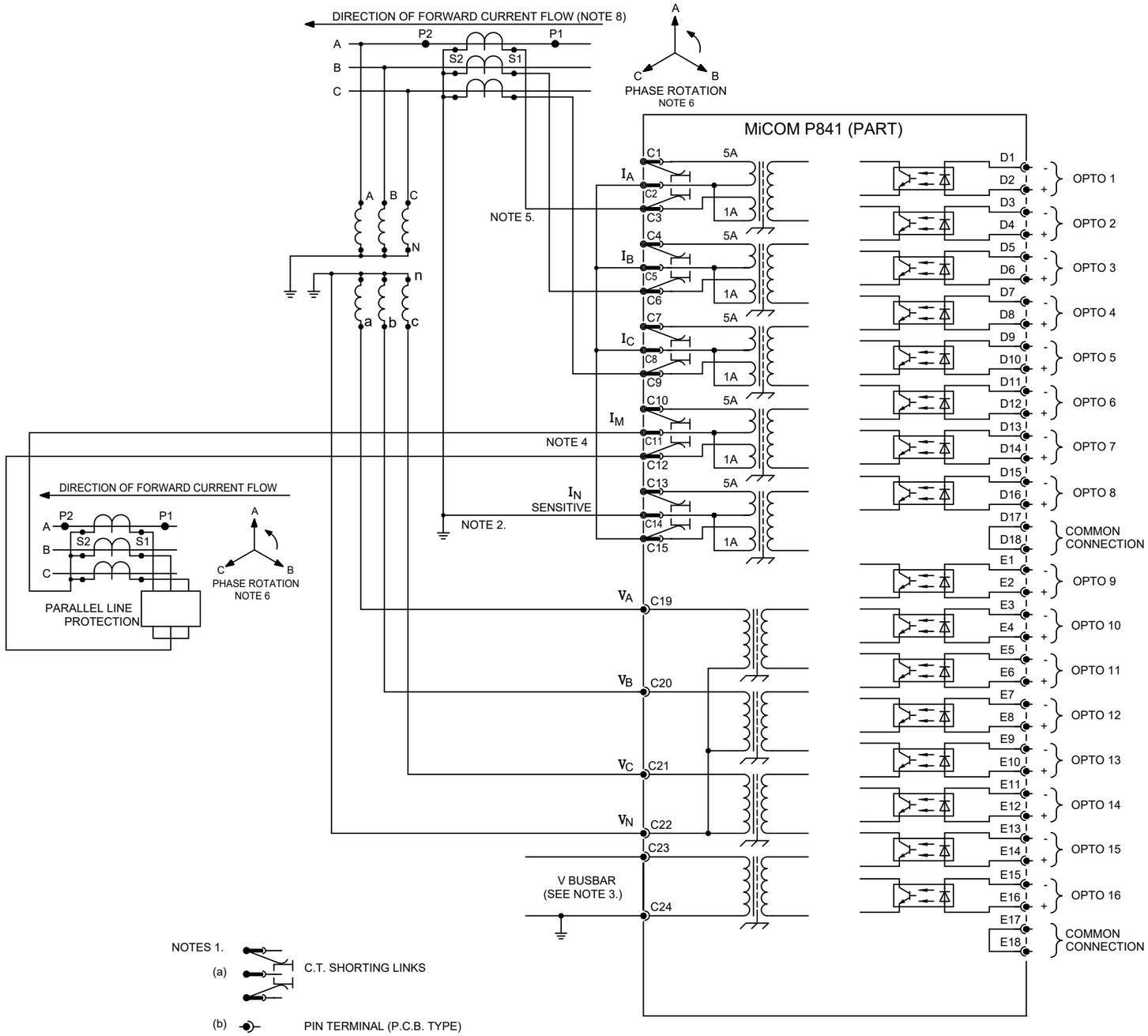


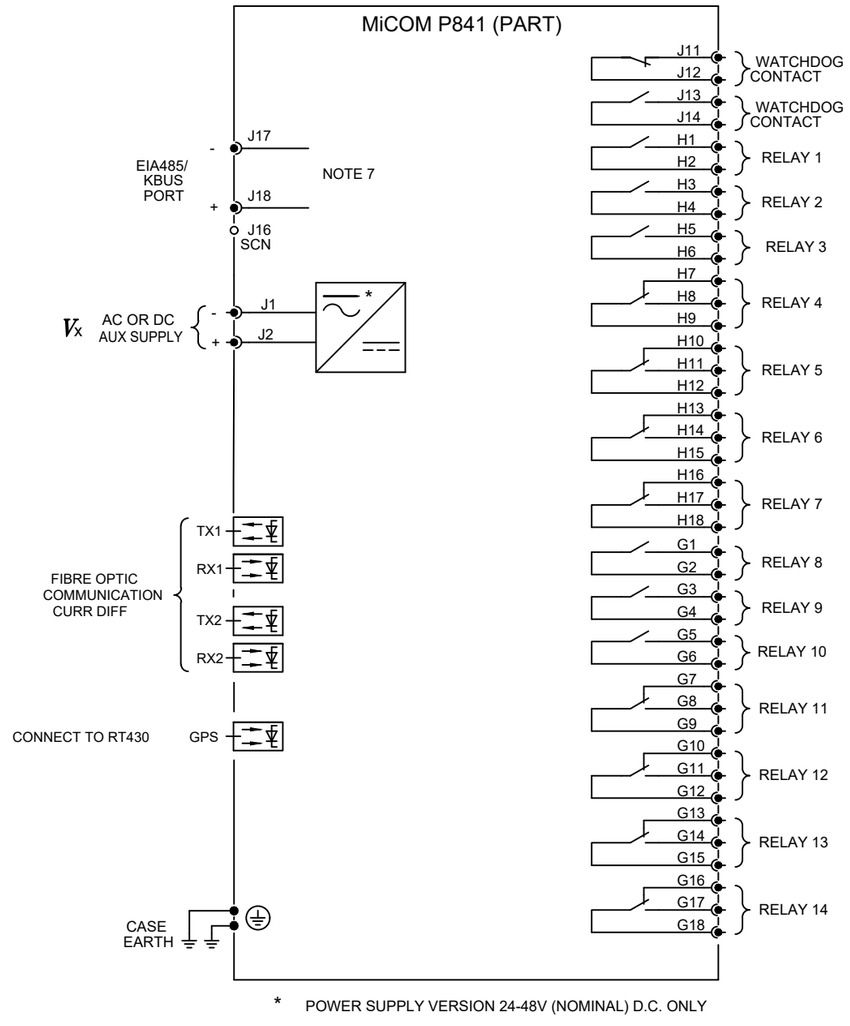


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
SEE 10P84199 FOR POWER SYSTEM CONNECTIONS.

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE) ⊸

Issue: C	Revision: CID008455. NOTE REGARDING POWER SYSTEM CONNECTIONS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 12I/12O		
Date: 23/07/2024	Name: S WOOTTON		Drg No: 10P84158	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

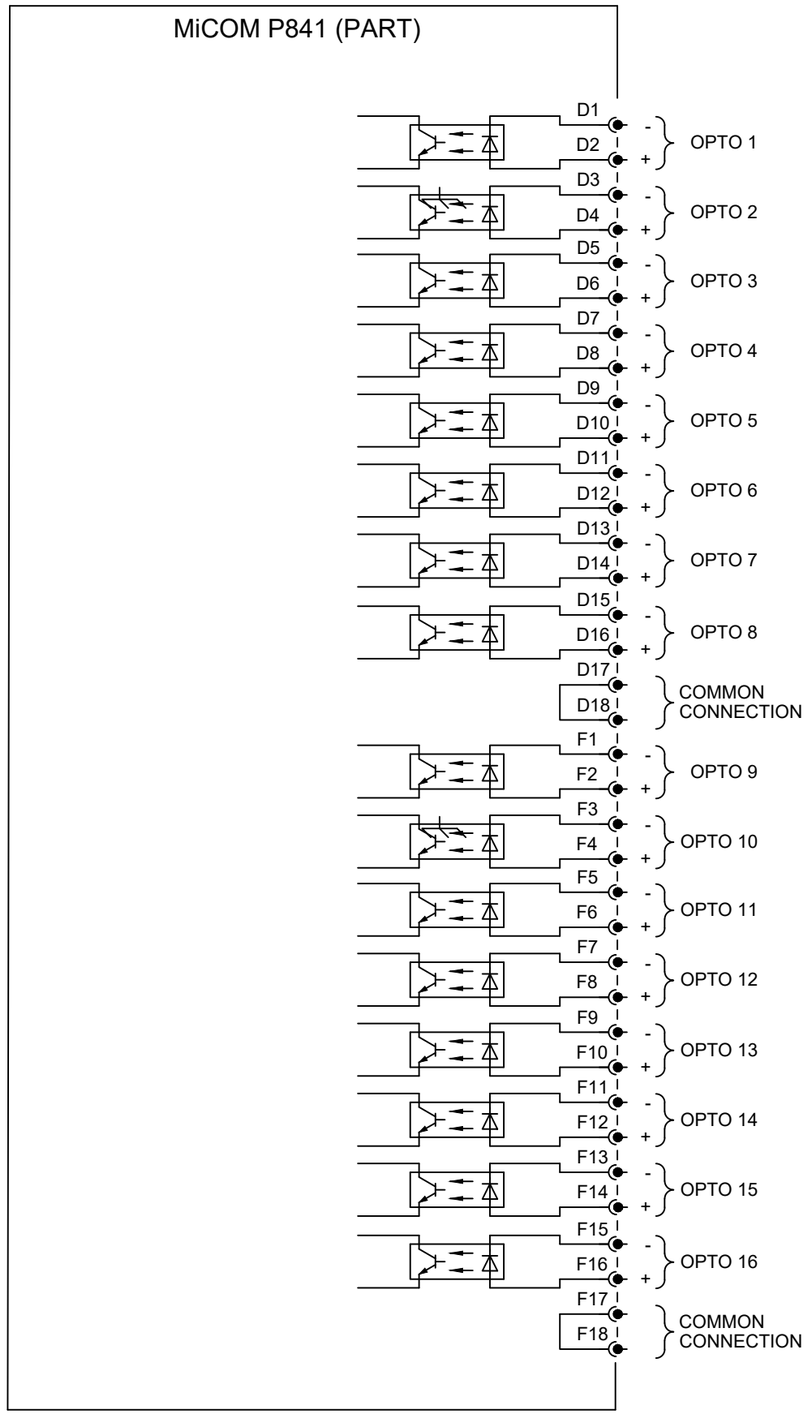
(b) PIN TERMINAL (P.C.B. TYPE)

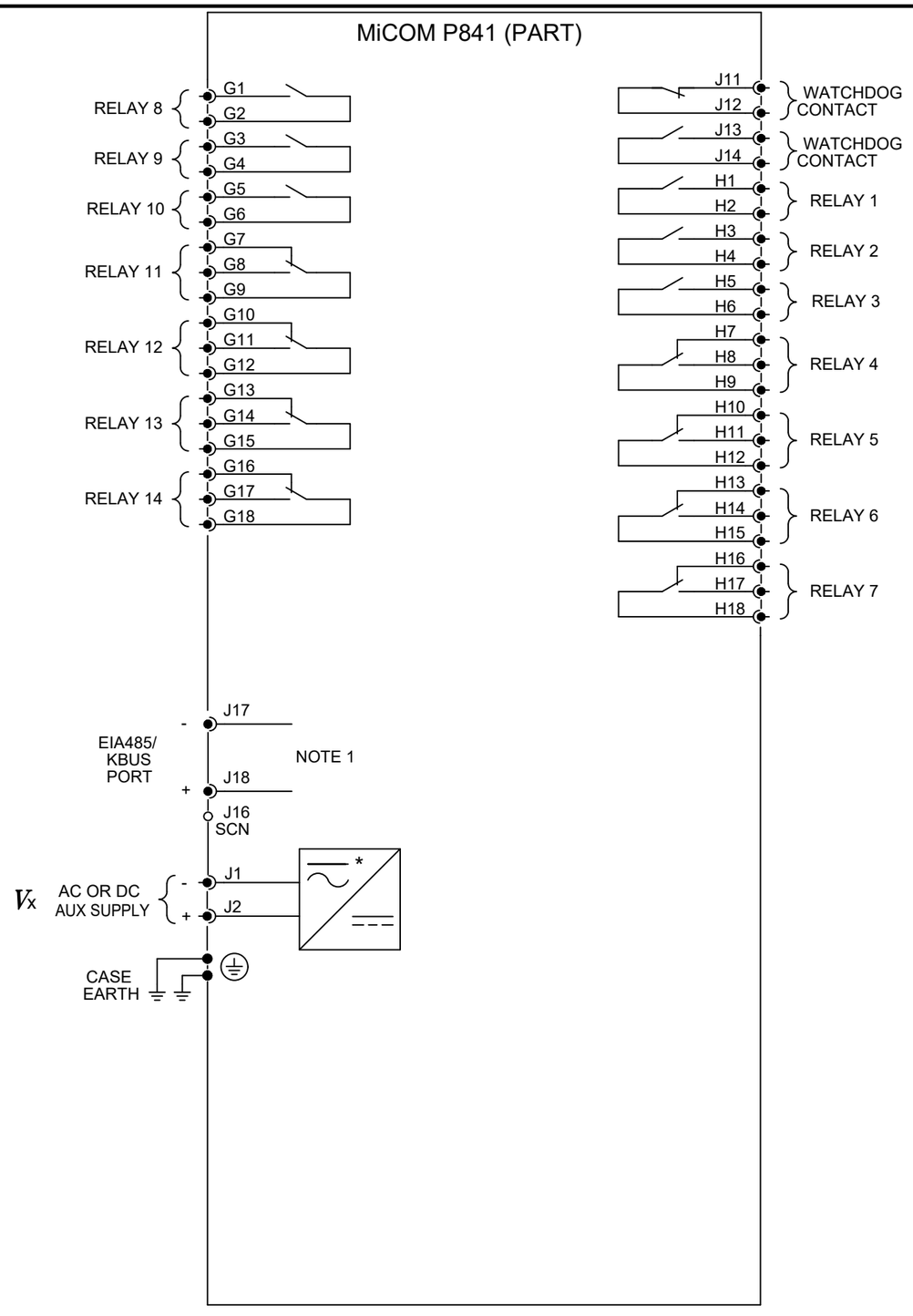
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: A	Revision: CID007390. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 16I/14O		
Date: 18/08/2022	Name: S WOOTTON		Drg No: **10P84116**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	

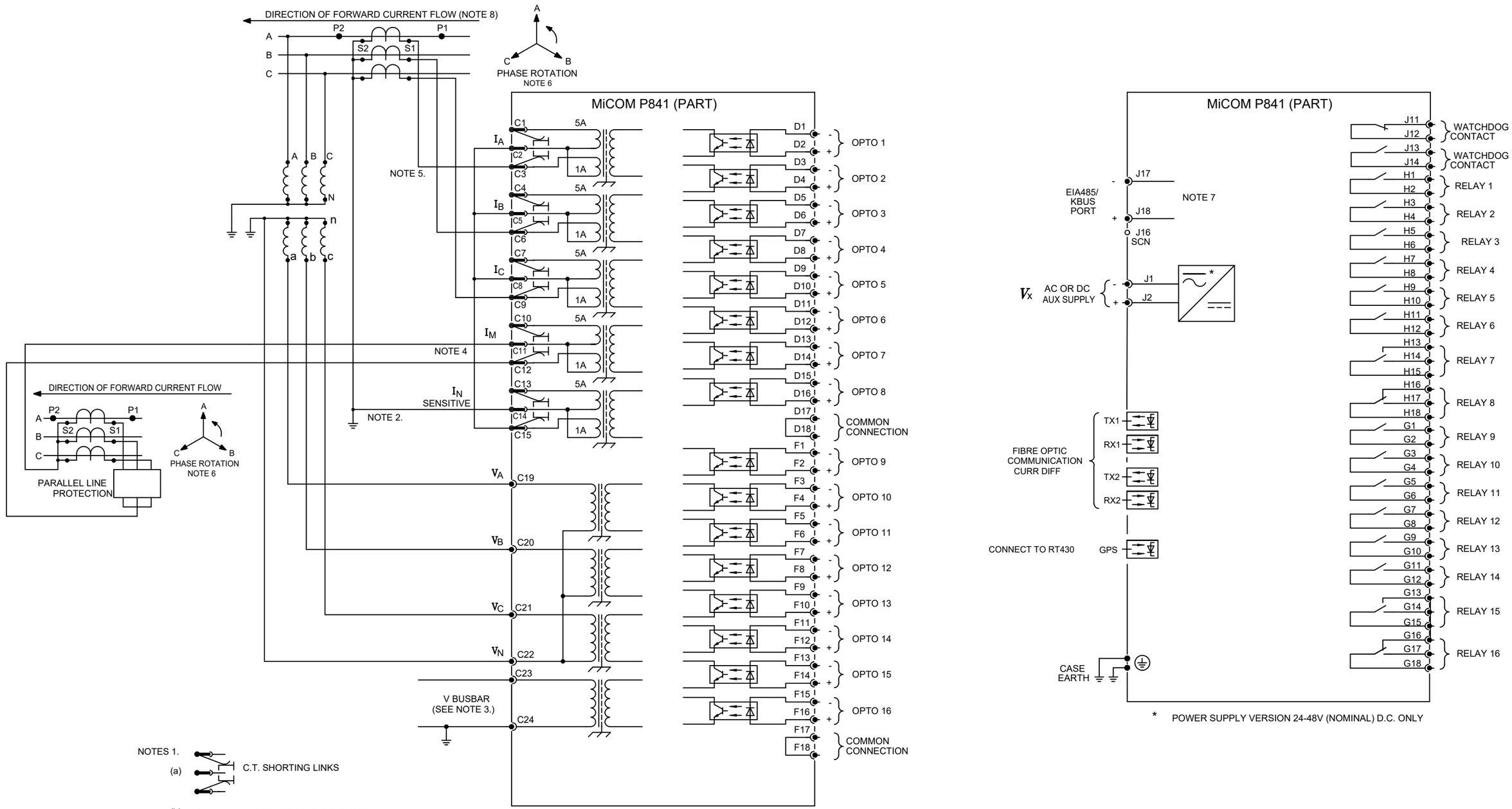




* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
SEE 10P84199 FOR POWER SYSTEM CONNECTIONS

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: C	Revision: CID008455. NOTE REGARDING POWER SYSTEM CONNECTIONS ADDED		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 16I/14O		
Date: 23/07/2024	Name: S WOOTTON		Drg No: **10P84159**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.

3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.

4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.

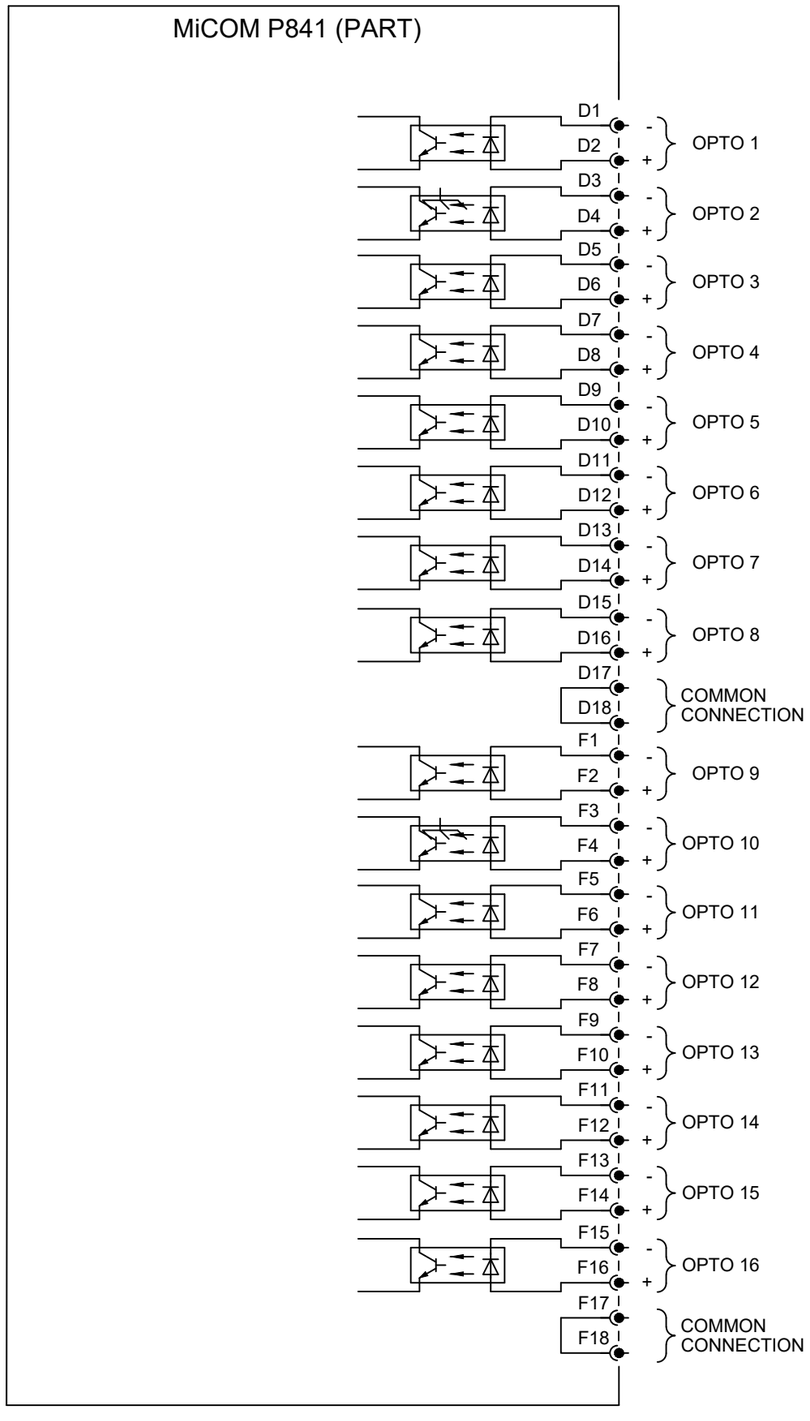
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.

6. REVERSE PHASE ROTATION IS ALSO SUPPORTED

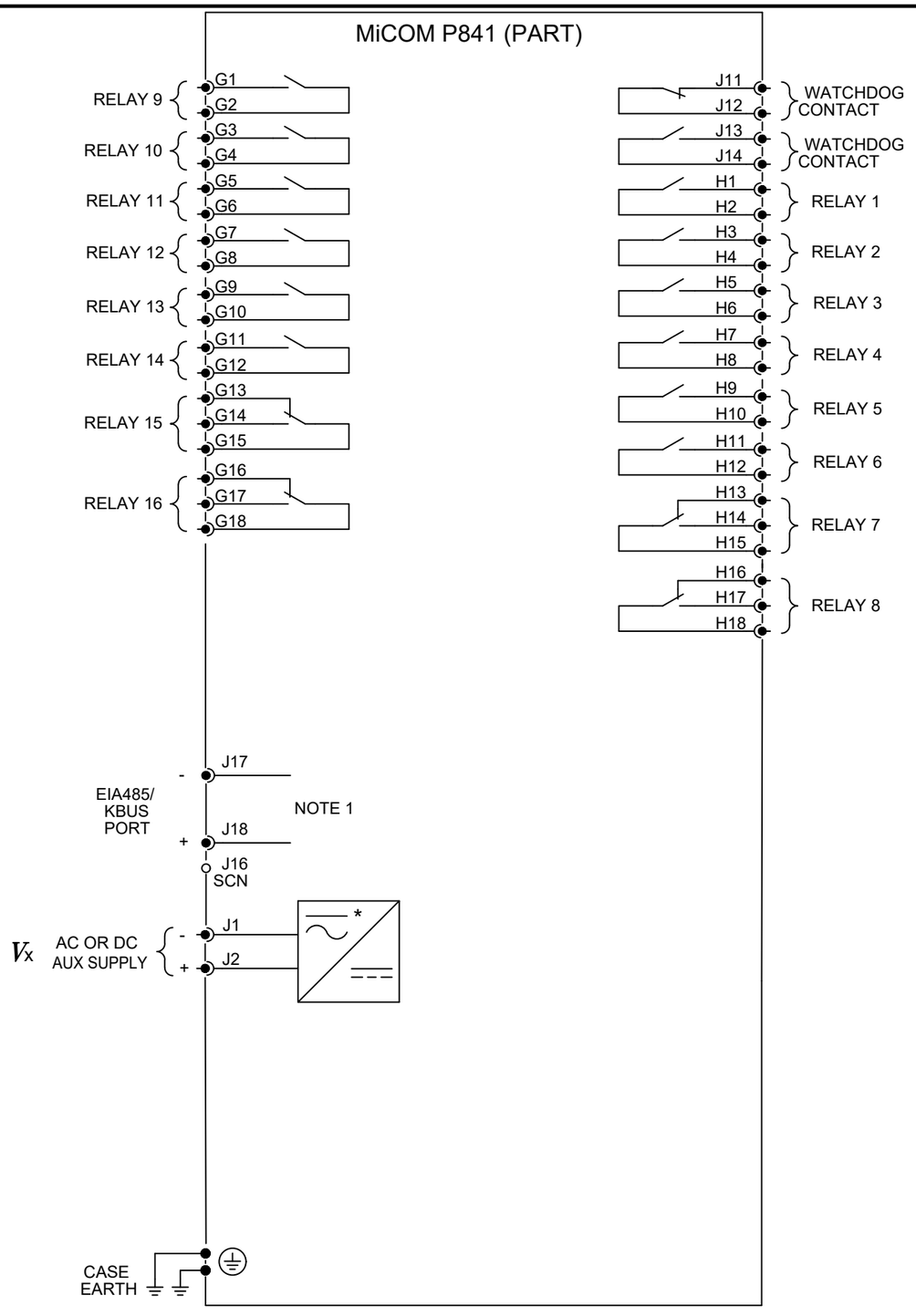
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: A	Revision: CID007390. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 16I/16O		
Date: 18/08/2022	Name: S WOOTTON		Drg No: 10P84117	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	

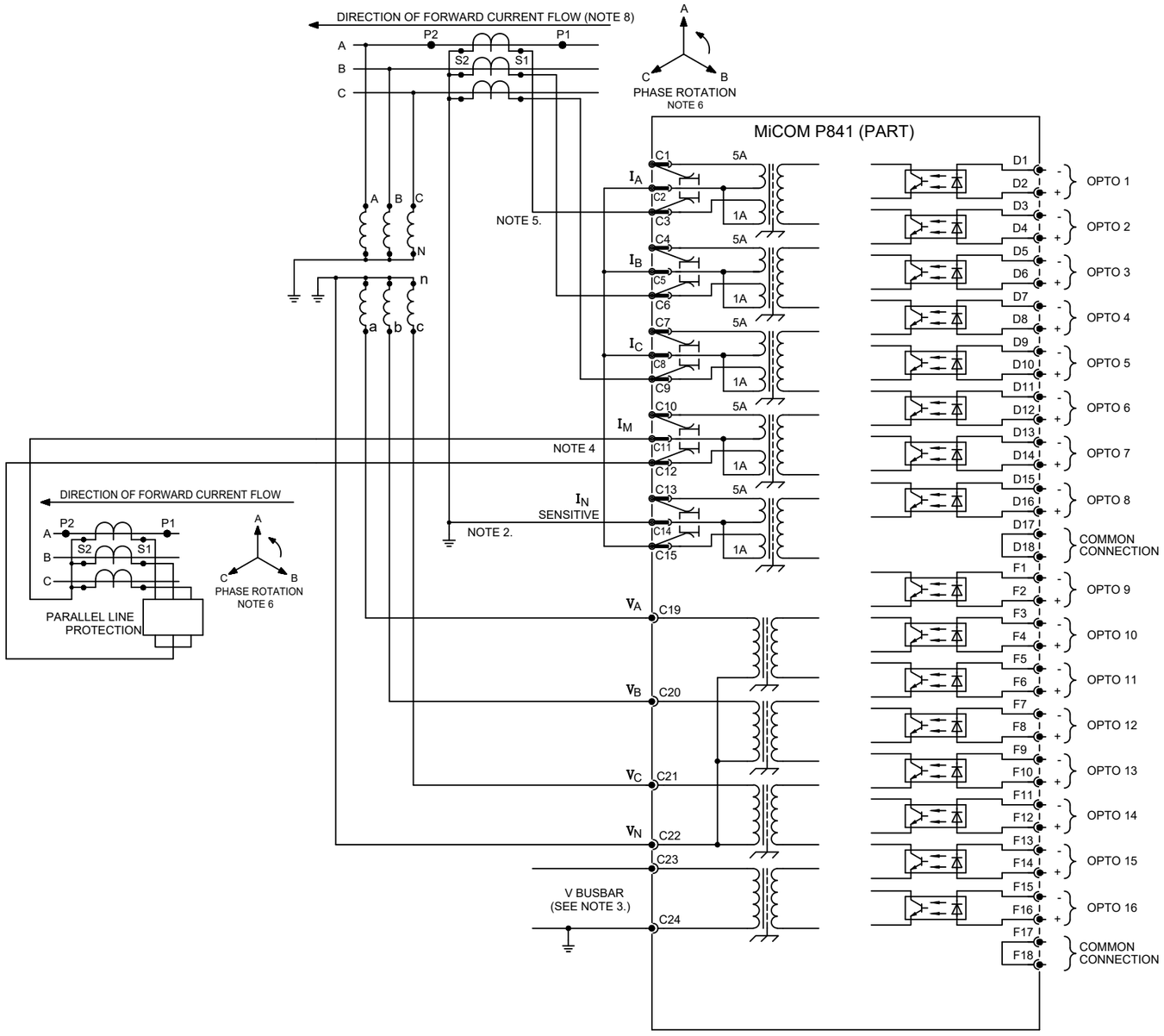


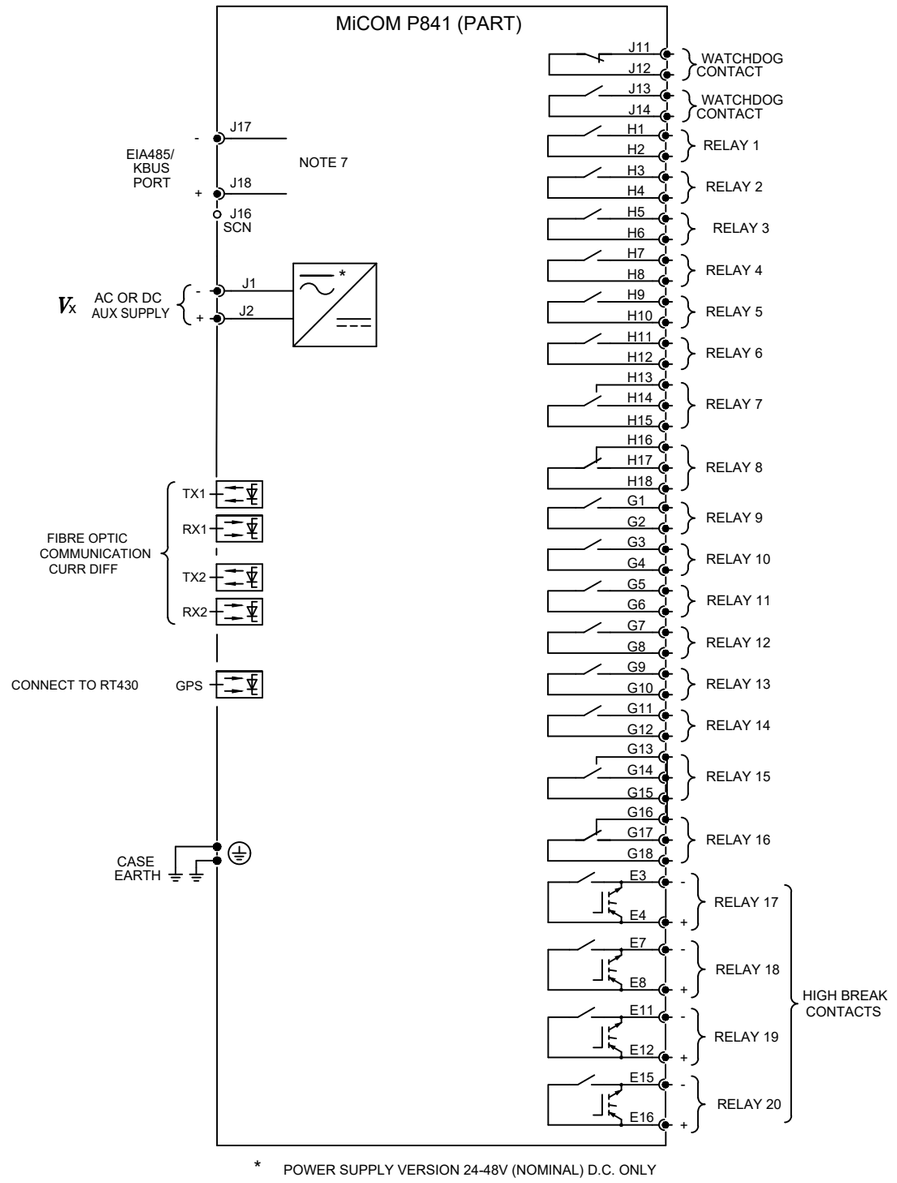
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
SEE 10P84199 FOR POWER SYSTEM CONNECTIONS



1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: C	Revision: CID008455. NOTE REGARDING POWER SYSTEM CONNECTIONS ADDED		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 16I/16O		
Date: 23/07/2024	Name: S WOOTTON		Drg No: 10P84160	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: A	Revision: CID007390. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 16I/16O + 4 HIGH SPEED HIGH BREAK RELAYS	
Date: 19/08/2022	Name: S WOOTTON		Drg No: 10P84118	Sht: 1
Date:	Chkd: S SWAIN			Next Sht: -

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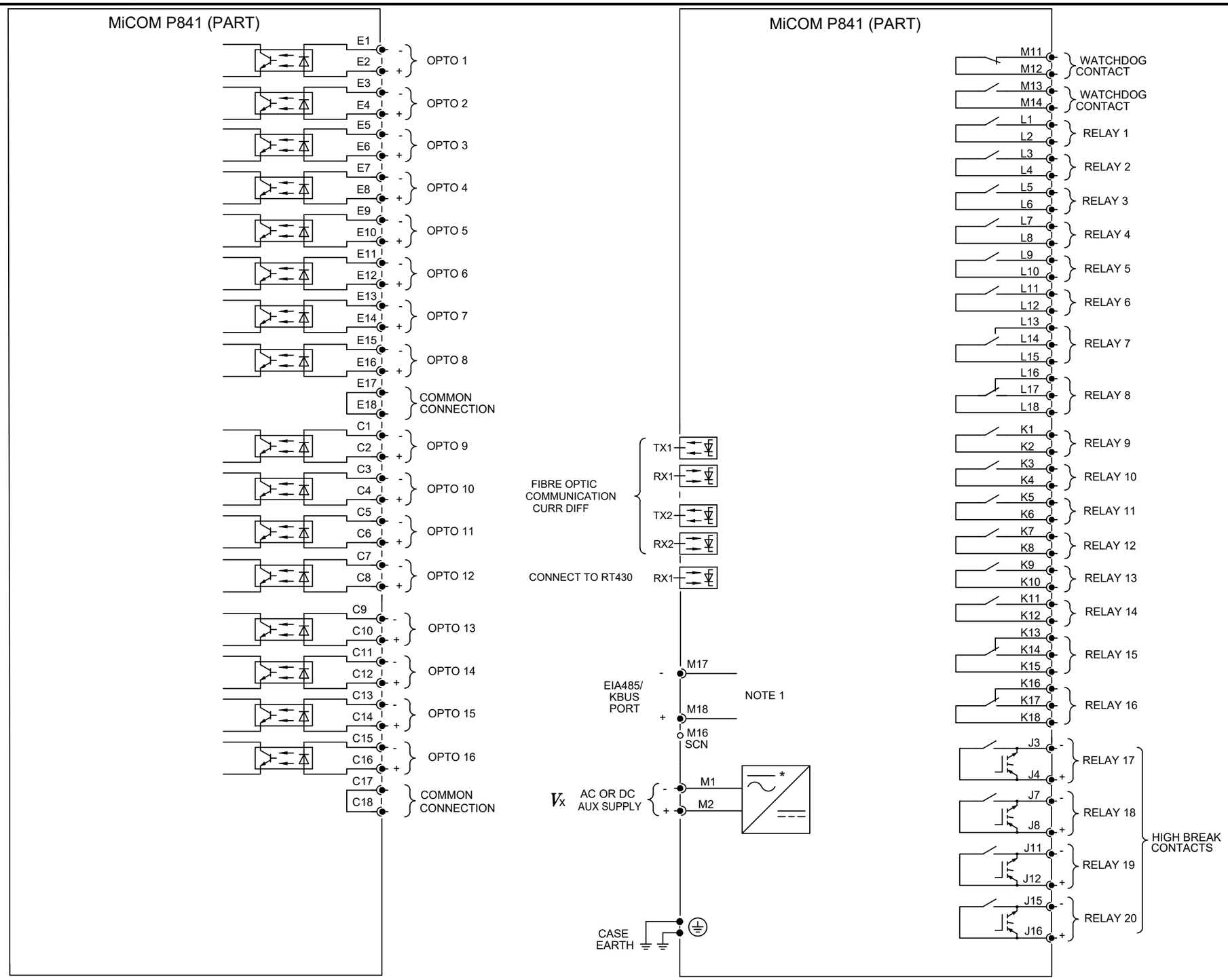
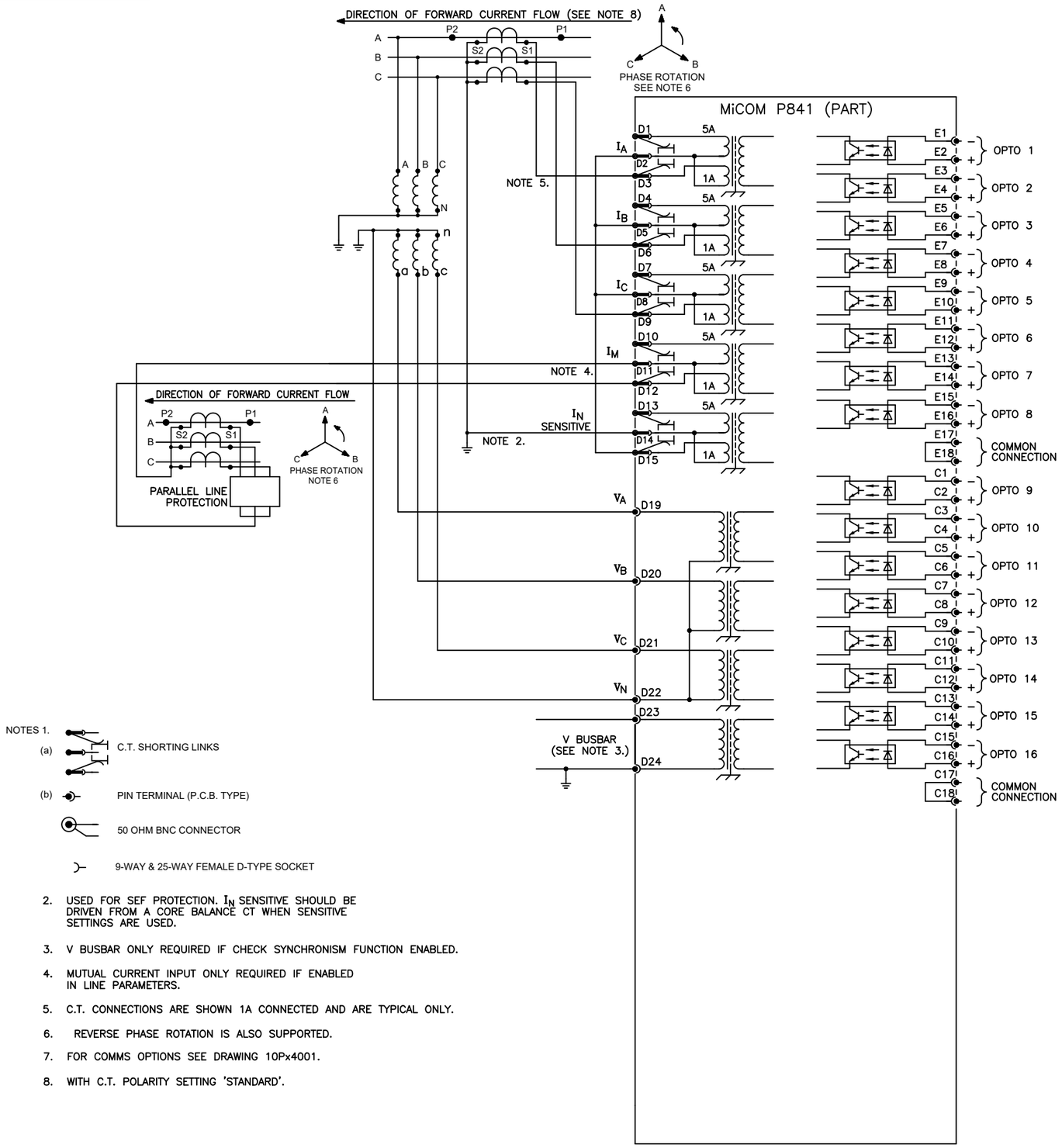


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: A	Revision: CID007390. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 16I/16O + 4 HIGH SPEED HIGH BREAK RELAYS		
Date: 31/08/2022	Name: S WOOTTON		Drg No: 10P84142	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	



NOTES 1.

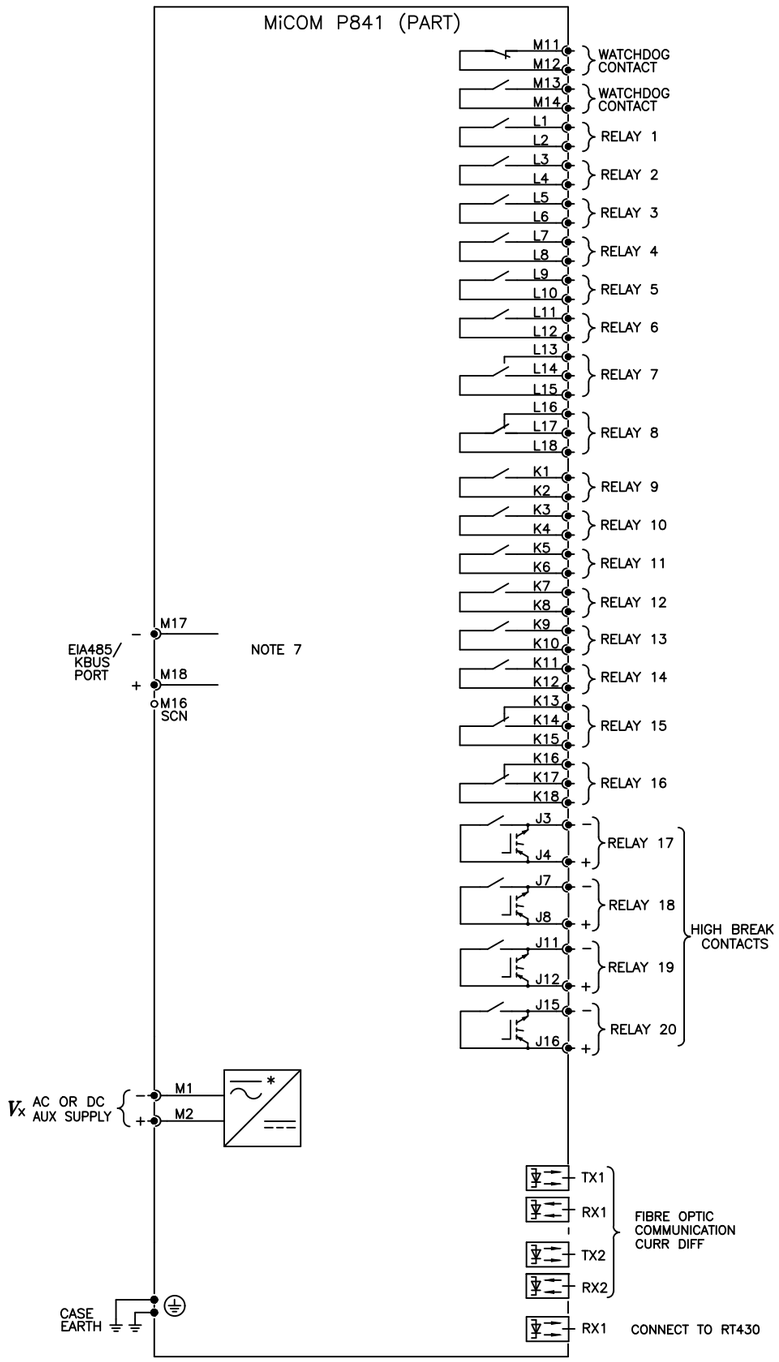
(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.



* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

Issue: A	Revision: CID007472. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 16I/16O + 4 HIGH SPEED HIGH BREAK RELAYS	
Date: 20/10/2022	Name: S WOOTTON		Drg No: 10P84147	Sht: 1
Date:	Chkd:			Next Sht: -

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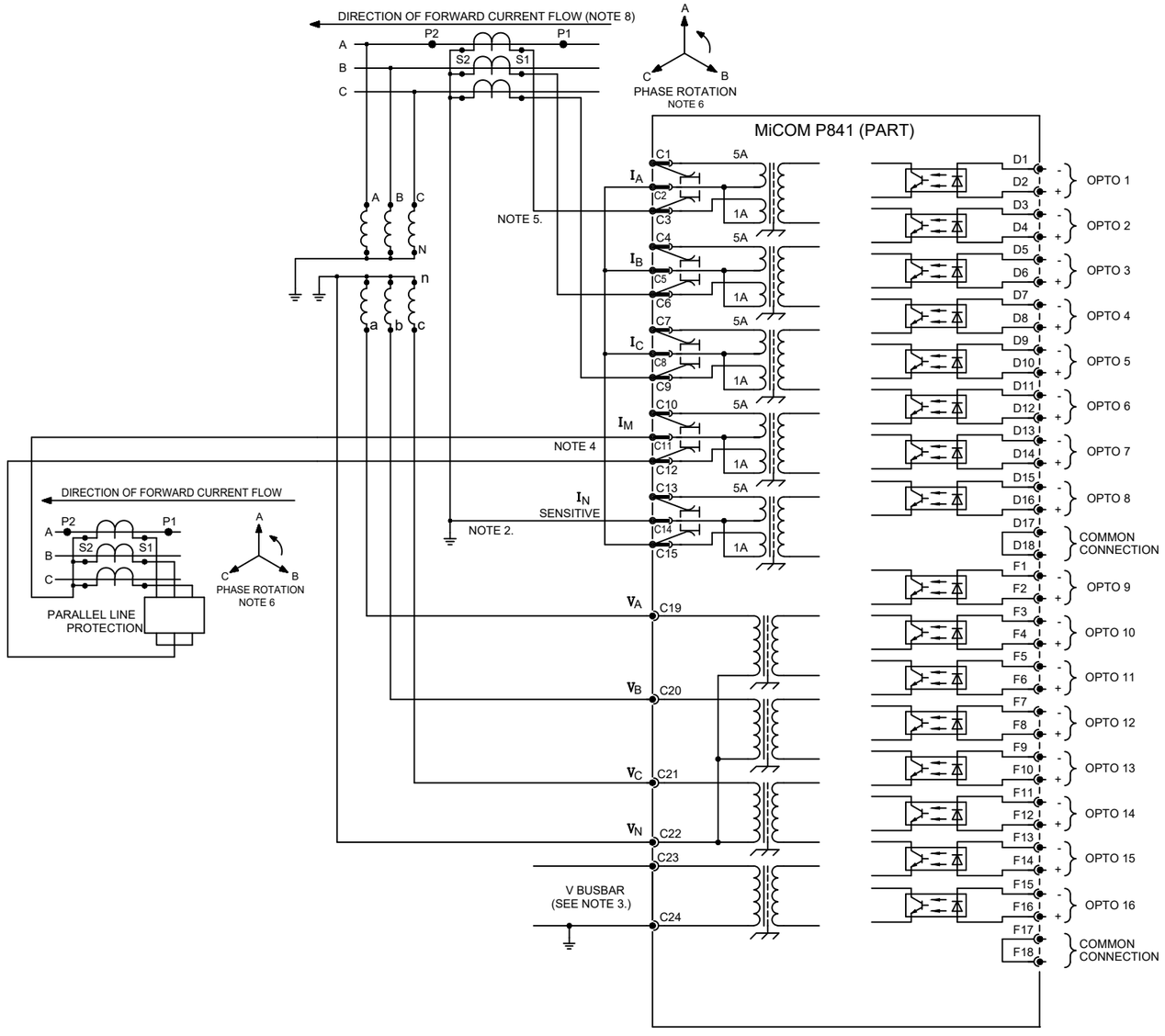


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.

3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.

4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.

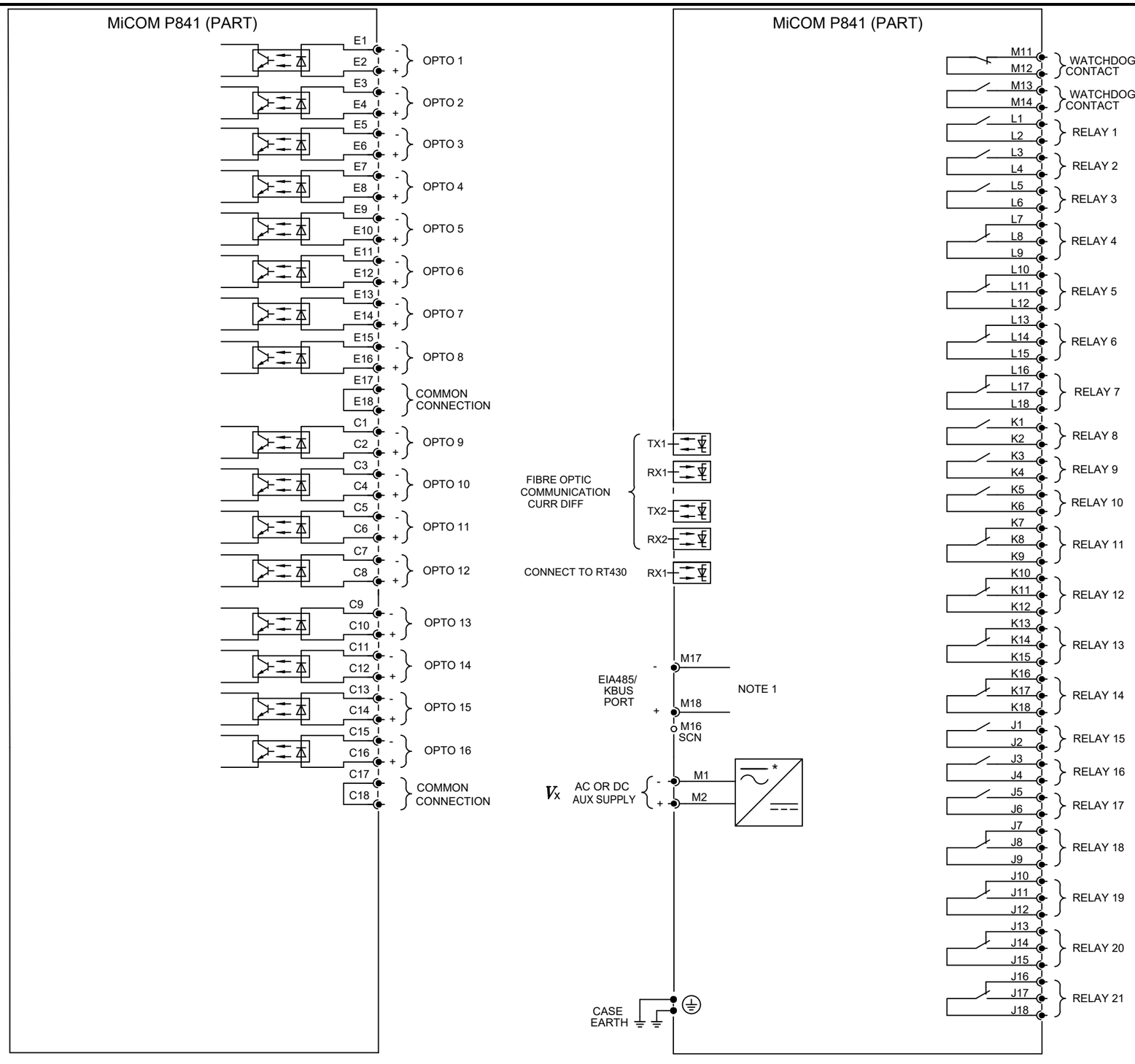
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.

6. REVERSE PHASE ROTATION IS ALSO SUPPORTED

7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

8. WITH C.T. POLARITY SETTING 'STANDARD'.

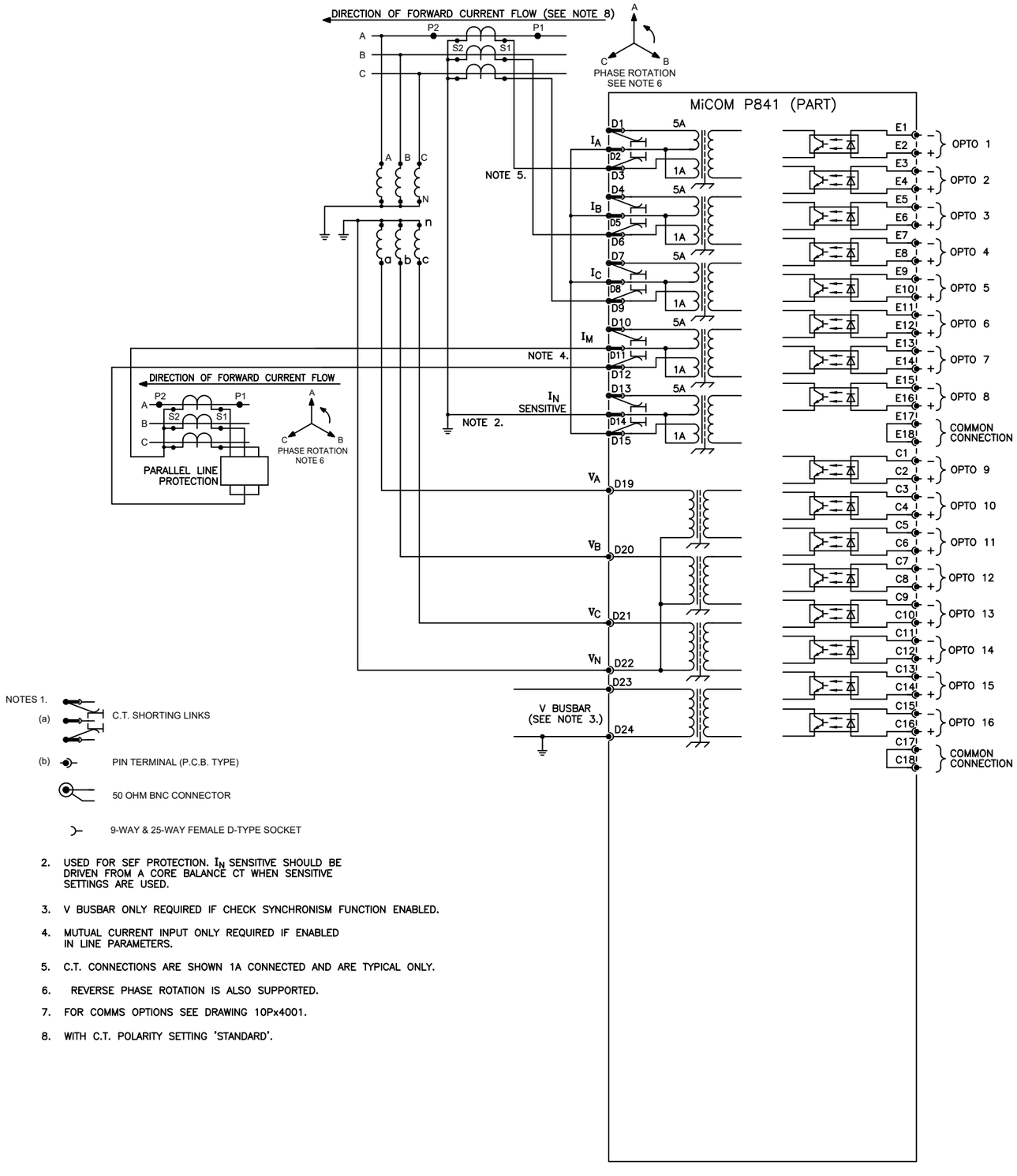
Issue: A	Revision: CID007390, INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 16I/21O		
Date: 19/08/2022	Name: S WOOTTON		Drg No: 10P84119	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	

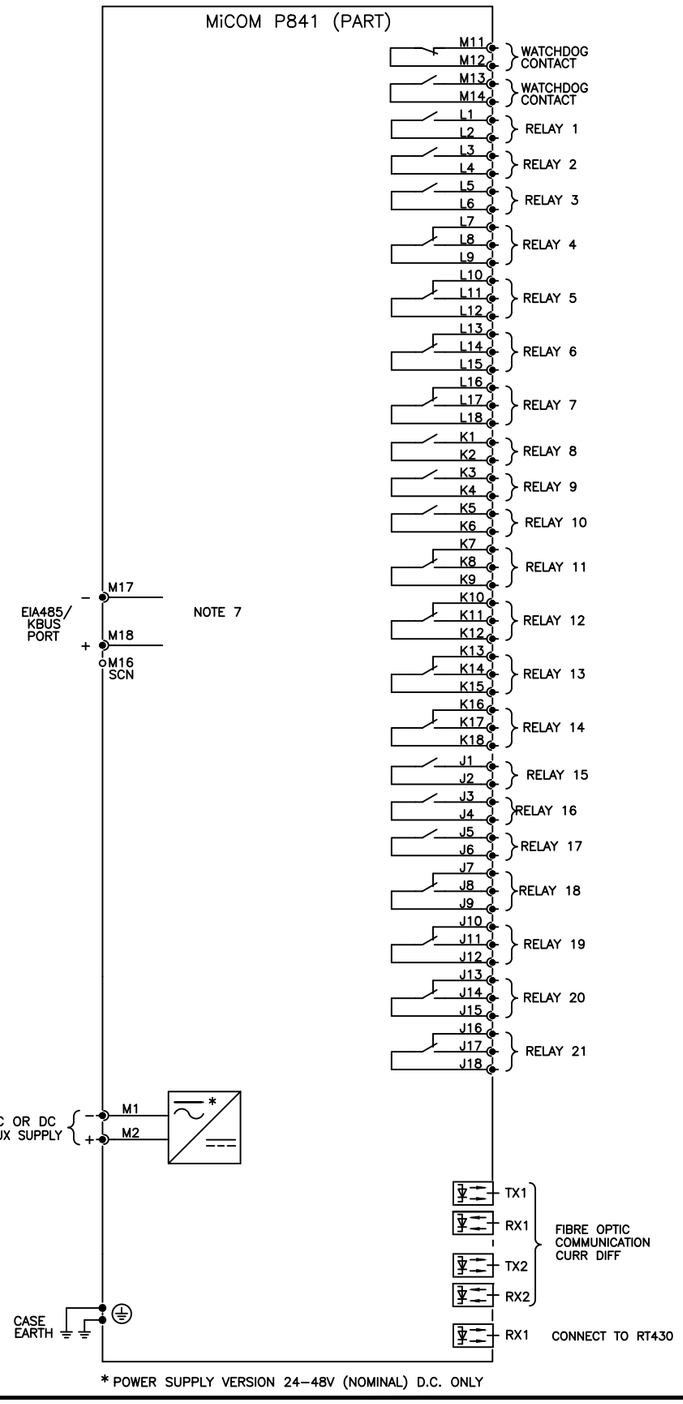


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: A	Revision: CID007390. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 16I/21O		
Date: 31/08/2022	Name: S WOOTTON		Drg No: **10P84143**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

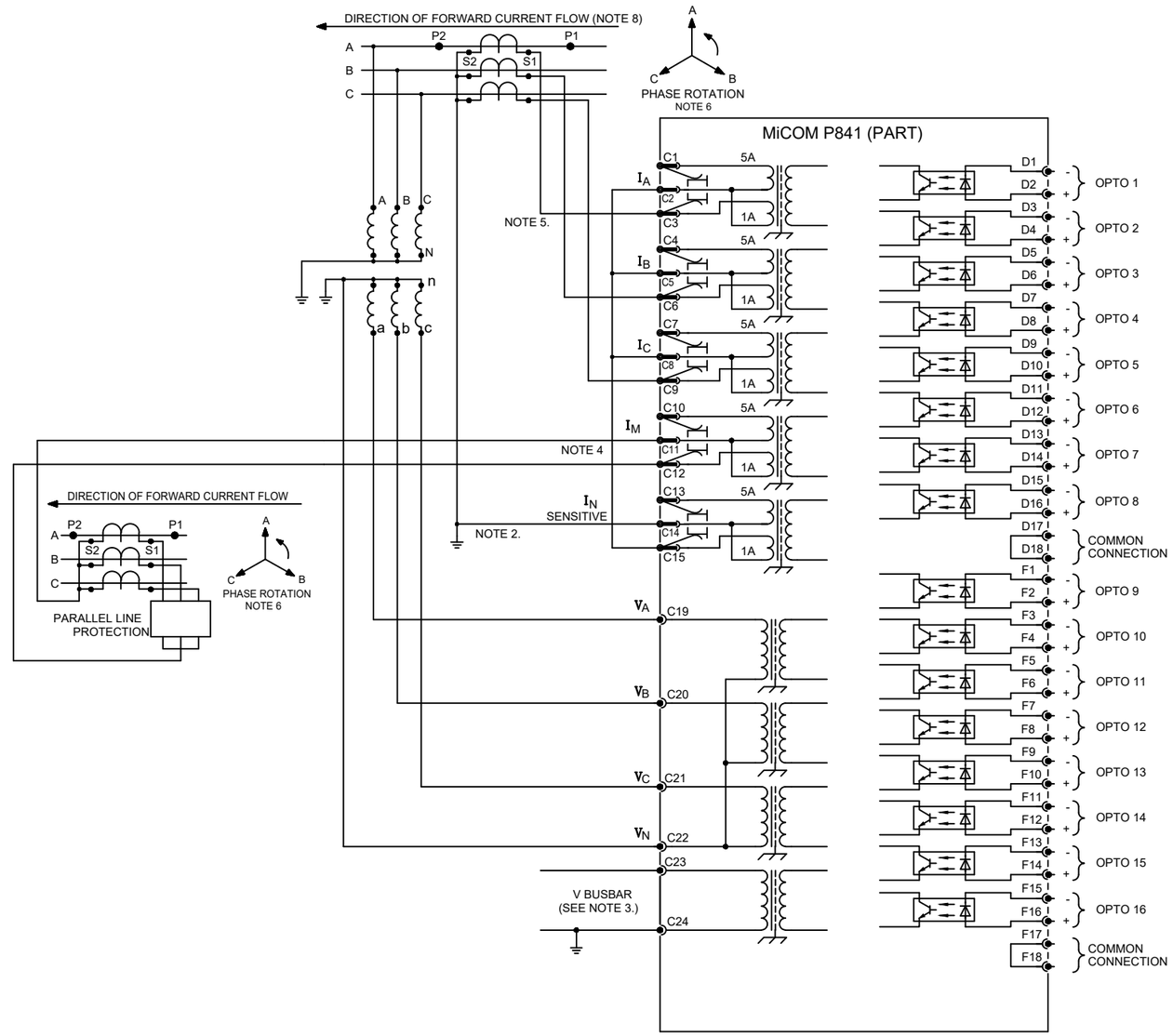
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

Issue: A	Revision: CID007472. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 16I/21O		
Date: 20/10/2022	Name: S WOOTTON		Drg No: 10P84148	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

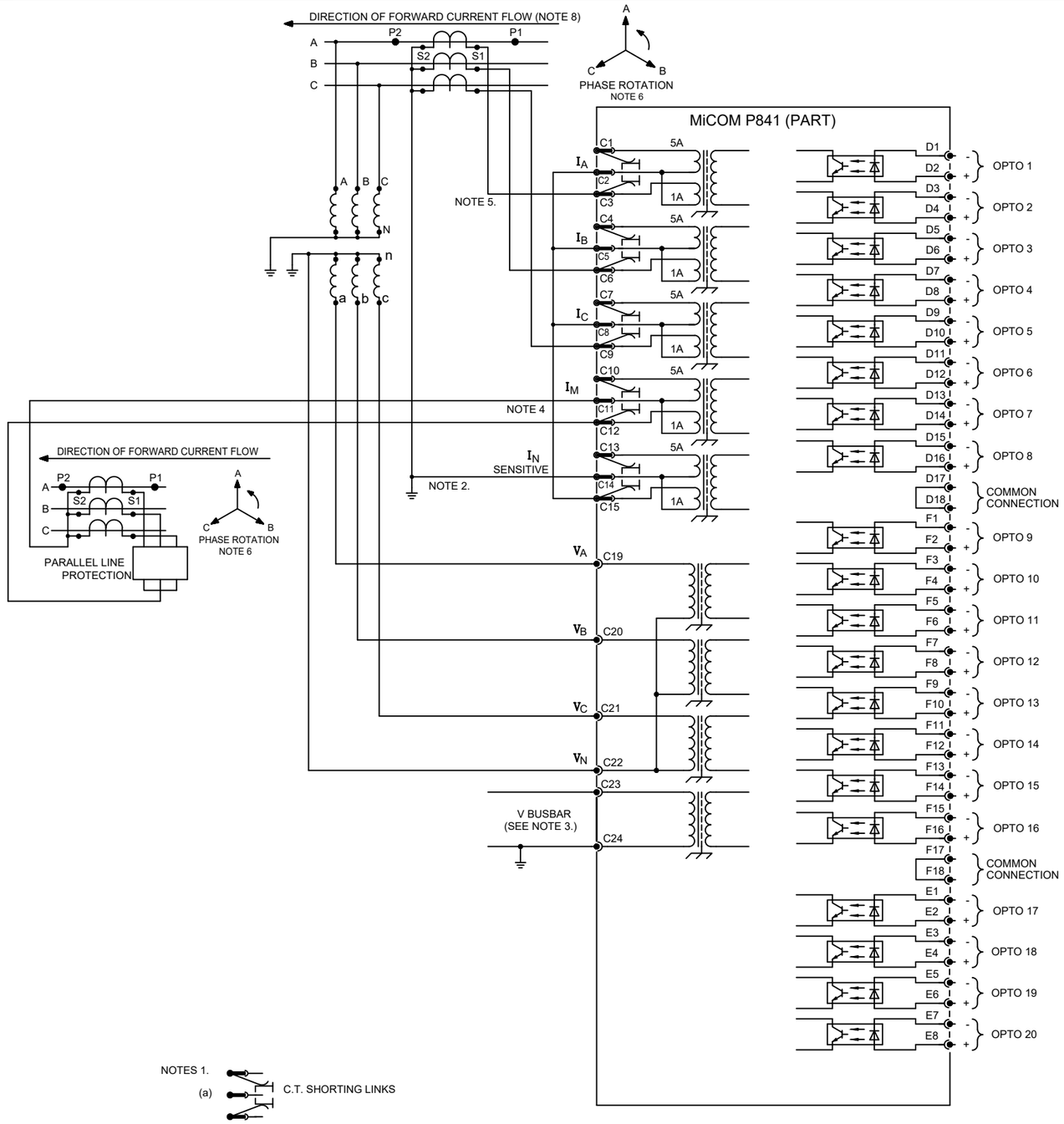
50 OHM BNC CONNECTOR

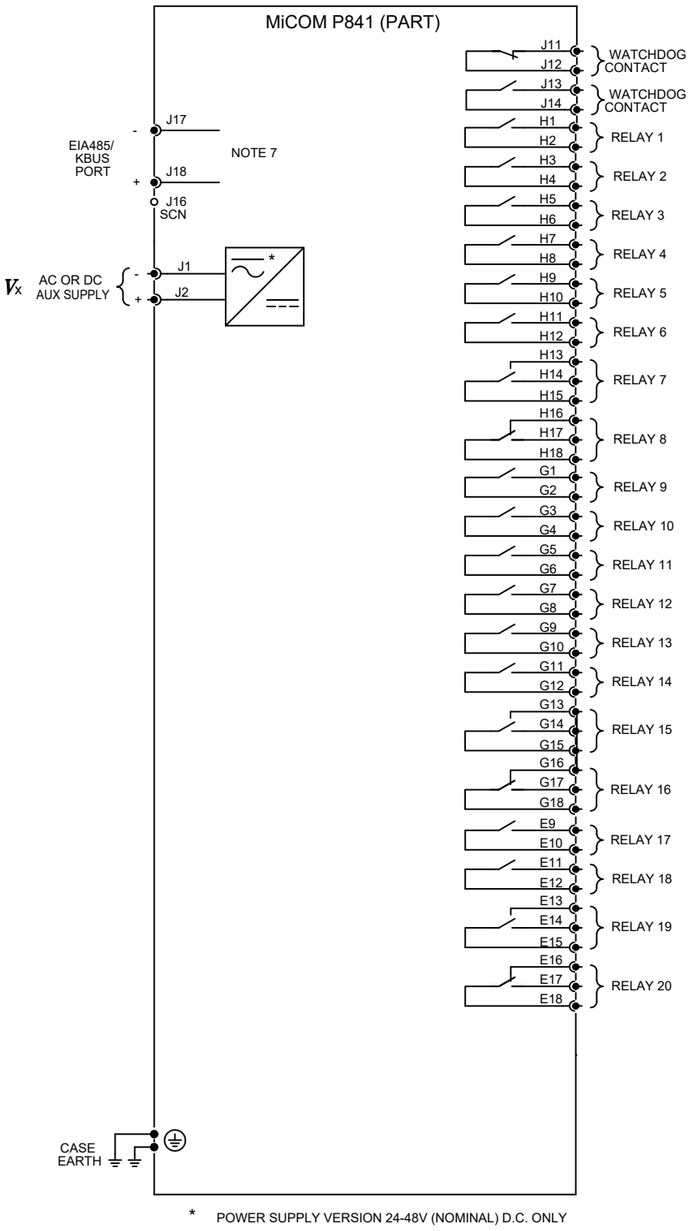
9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: A	Revision: CID007390. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 16I/24O		
Date: 19/08/2022	Name: S WOOTTON		Drg No: 10P84120	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 20I/20O	
Date: 09/02/2024	Name: S WOOTTON		Drg No: 10P84195	Sht: 1
Date:	Chkd:			Next Sht: -

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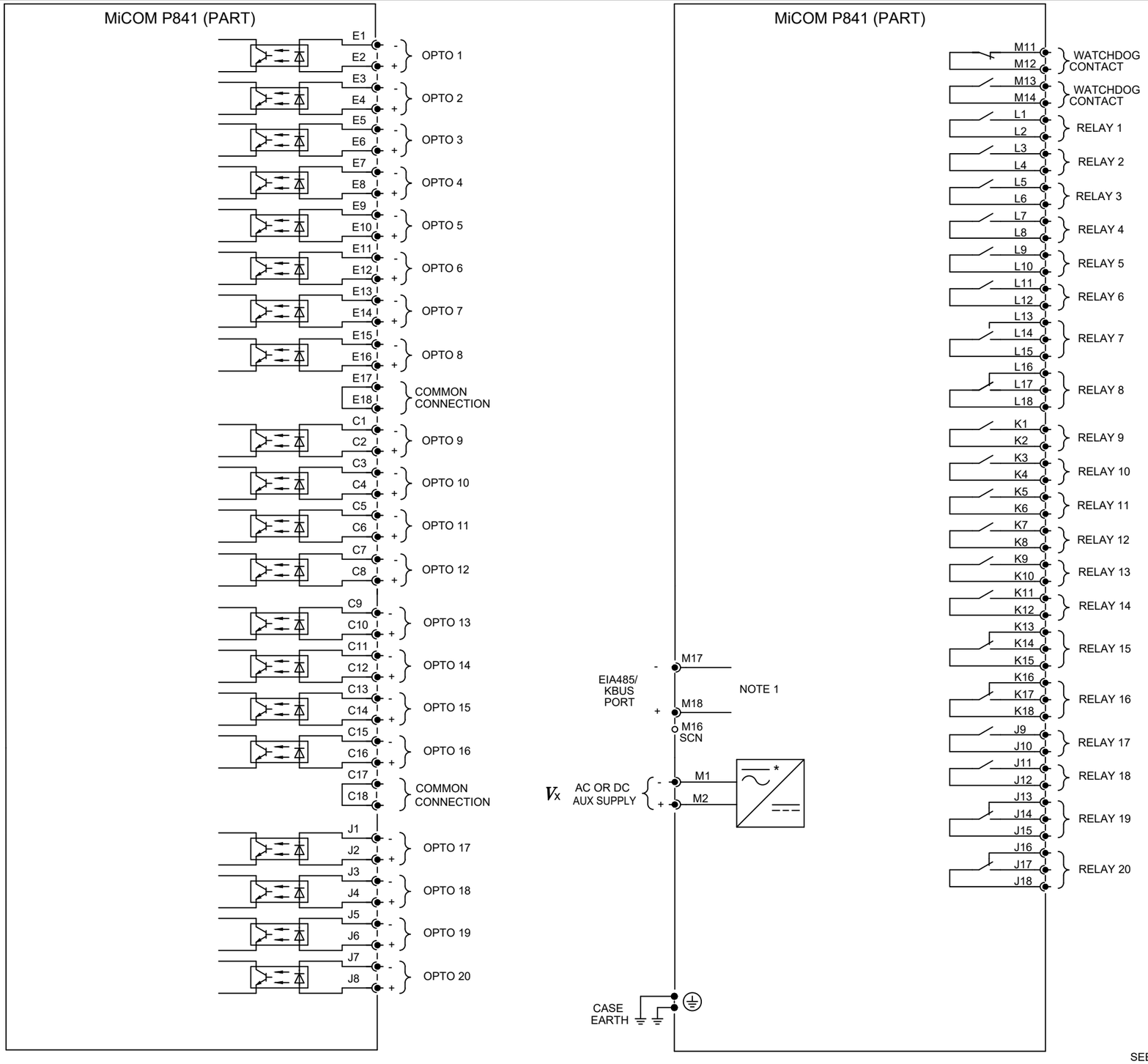
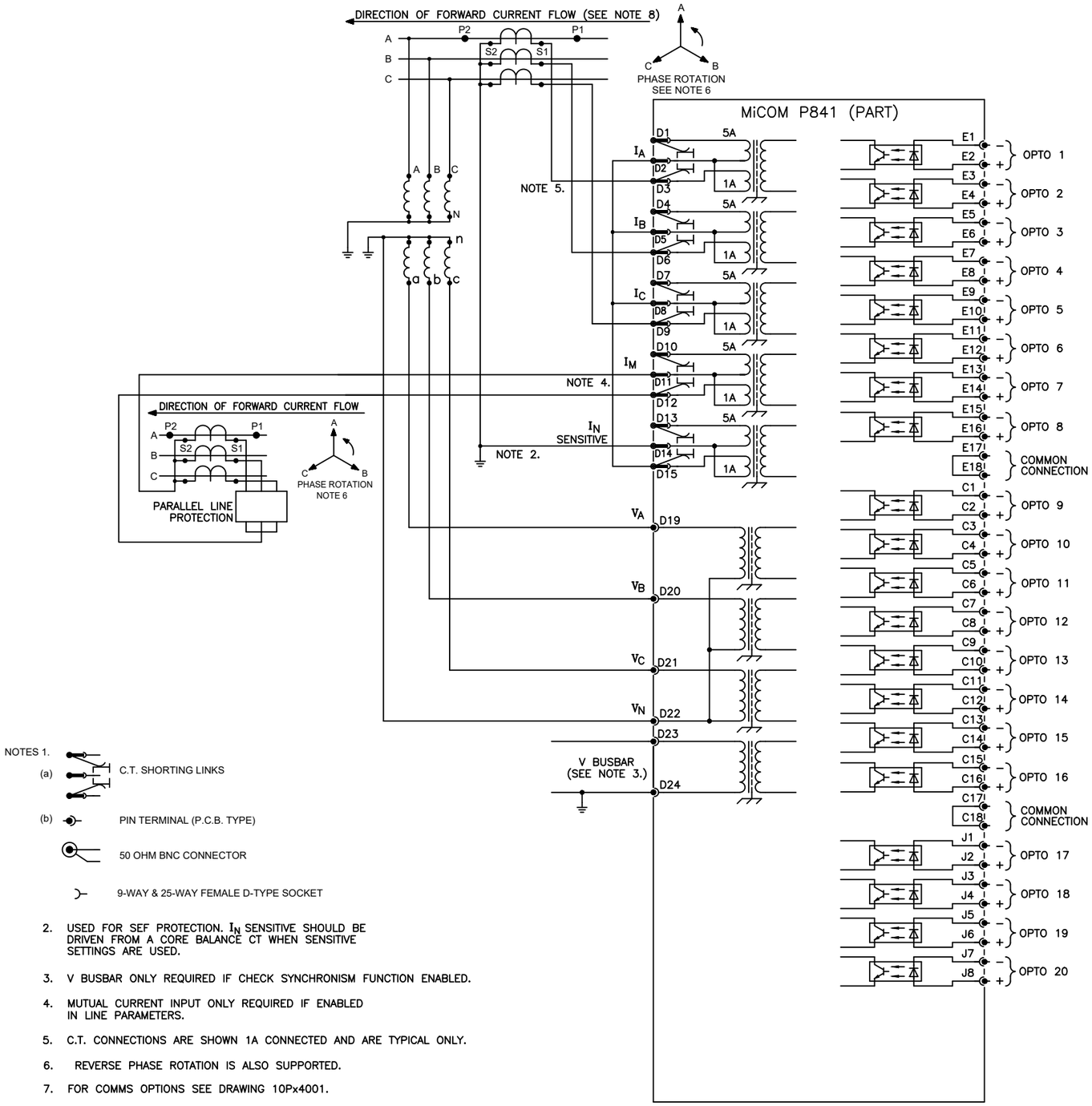
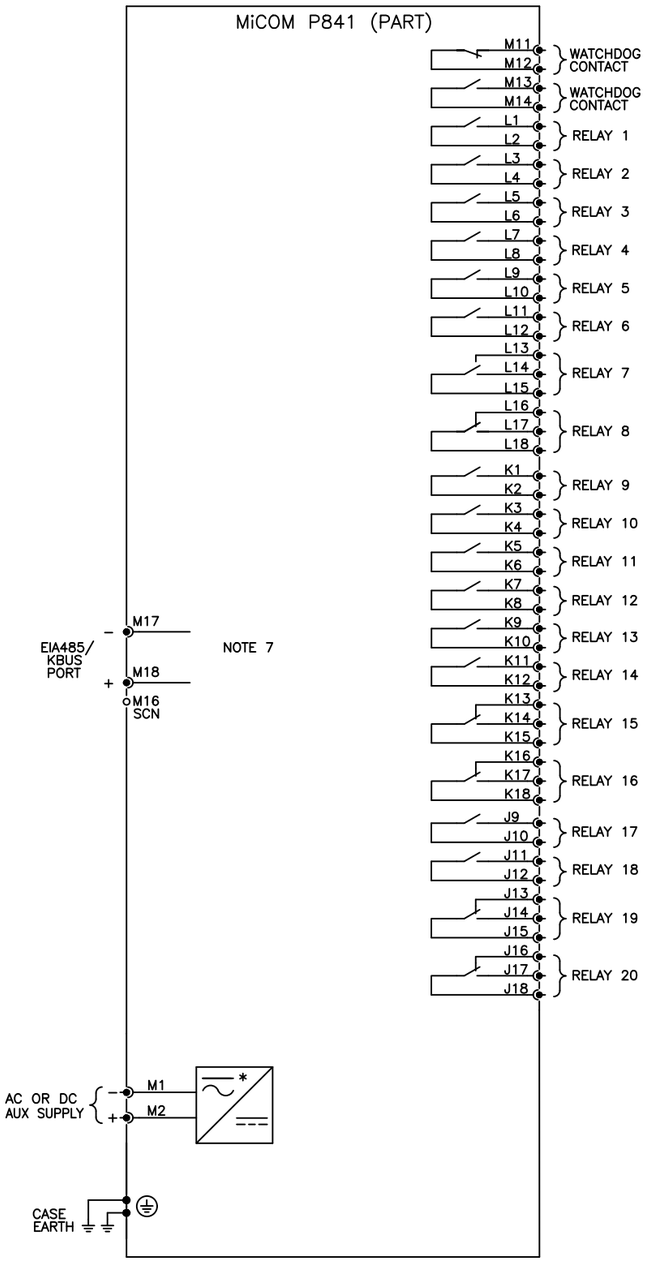
ST16 1WT, UK.



Issue: A	Revision: CID007575, INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 20I/20O		
Date: 29/01/2024	Name: S WOOTTON		Drg No: **10P84176**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 20I/20O	
Date: 05/02/2024	Name: S WOOTTON		Drg No: 10P84185	Sht: 1
Date:	Chkd:			Next Sht: -

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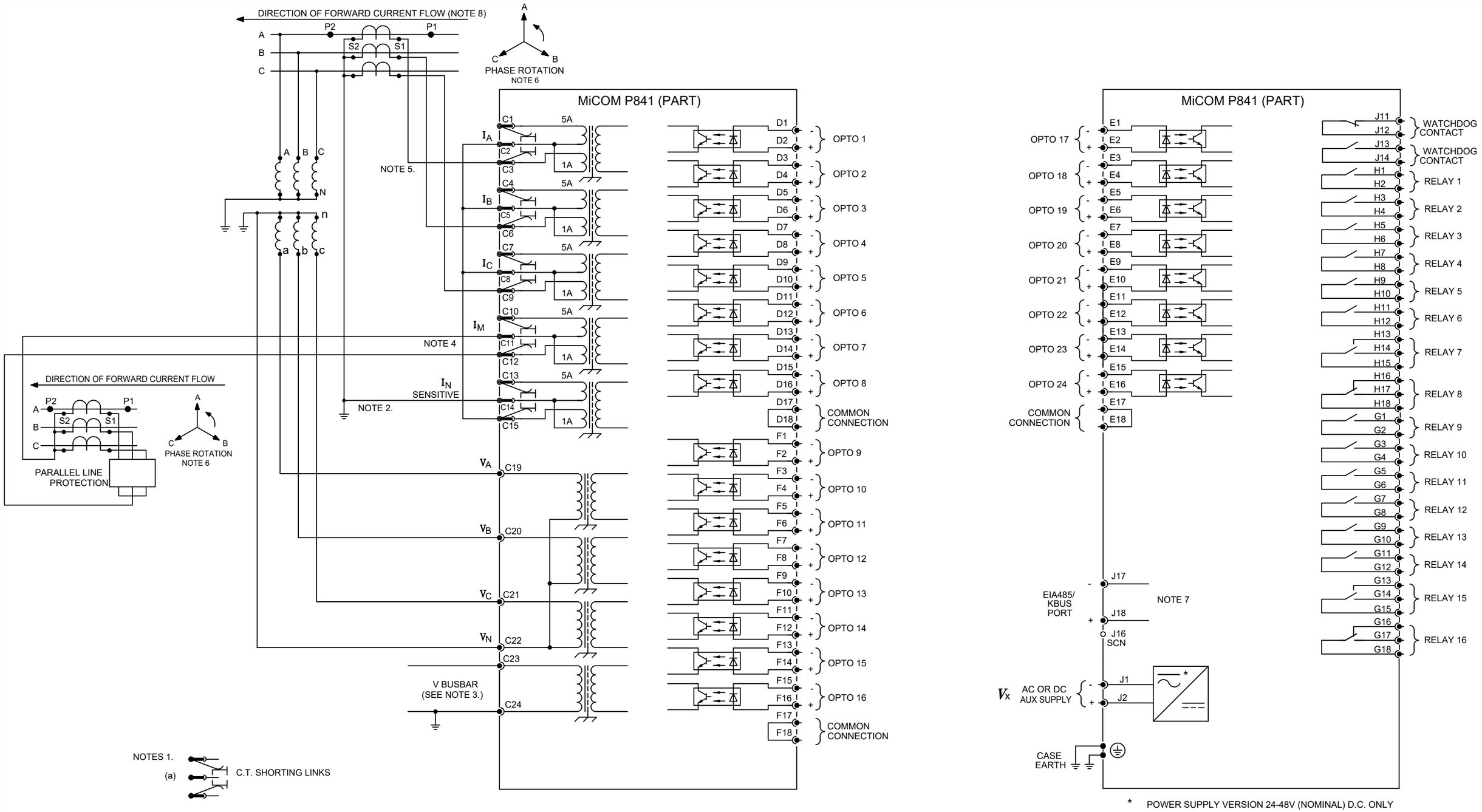

NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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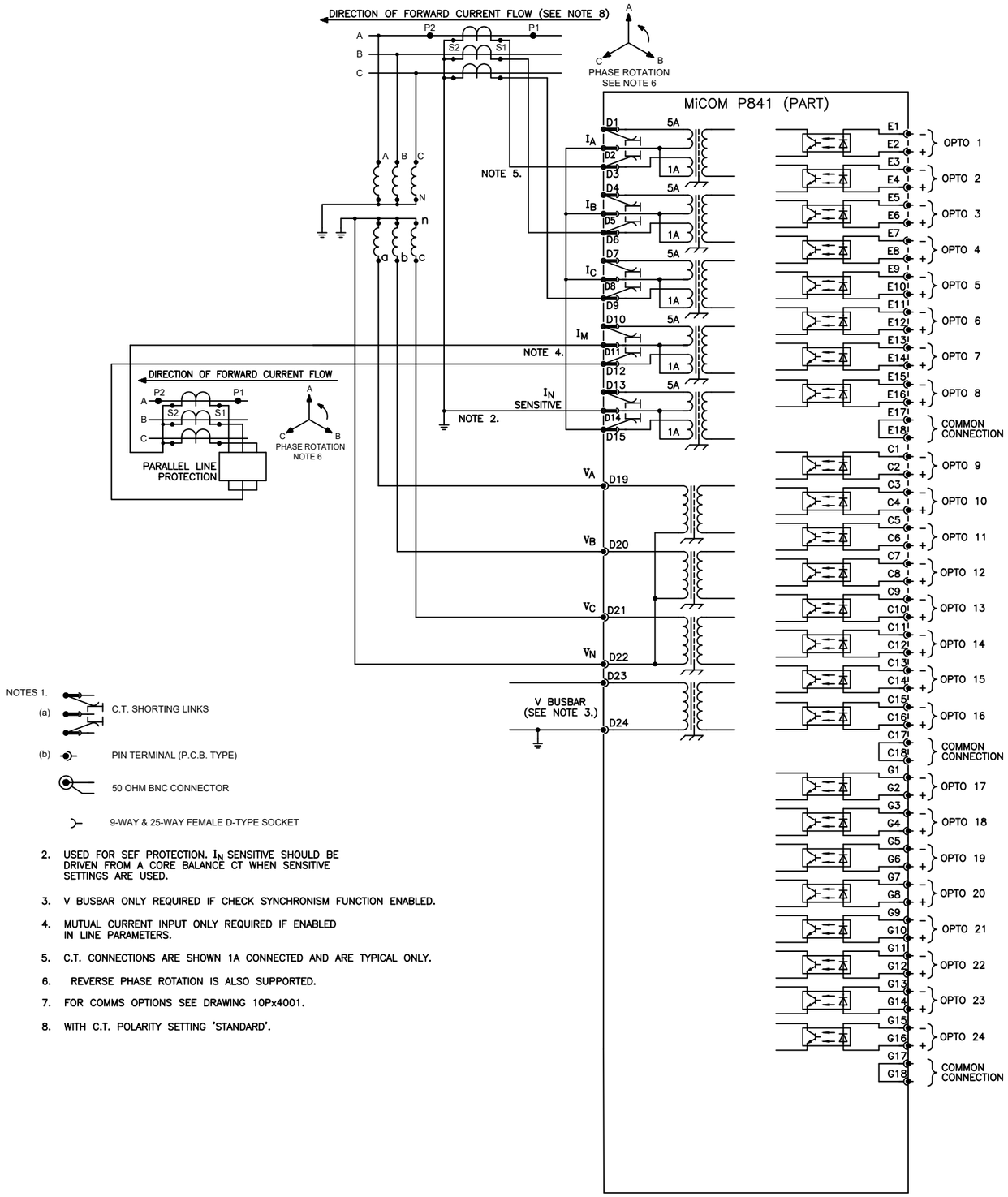
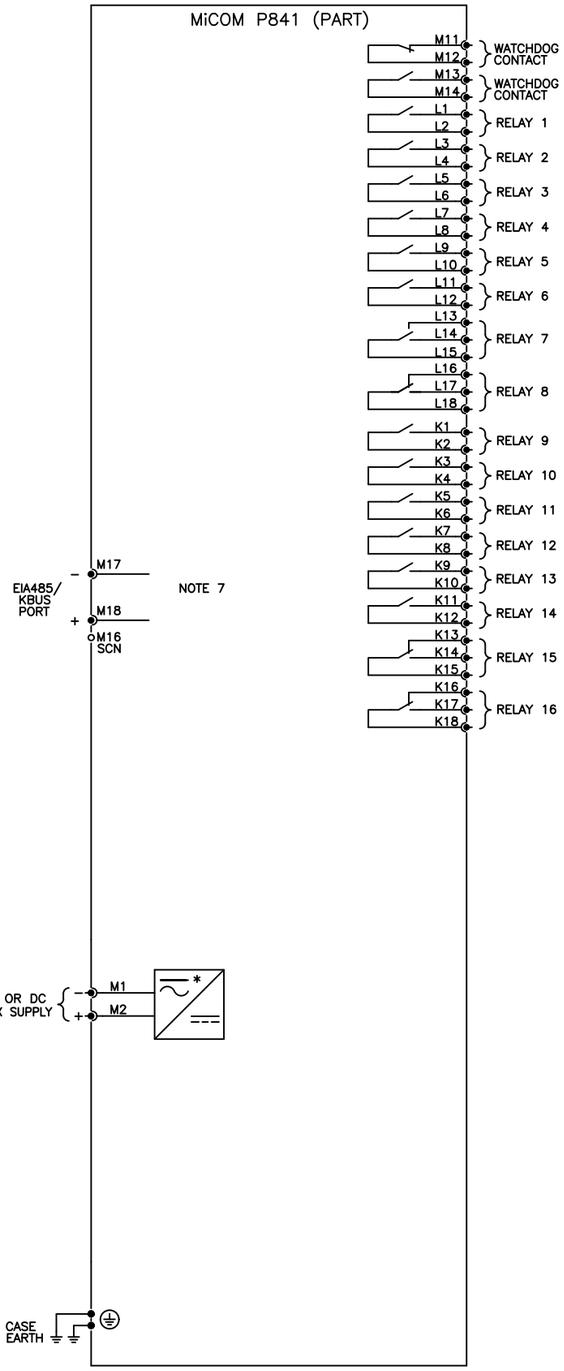
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (60TE) 24I/16O		
Date: 09/02/2024	Name: S WOOTTON		Drg No: 10P84198	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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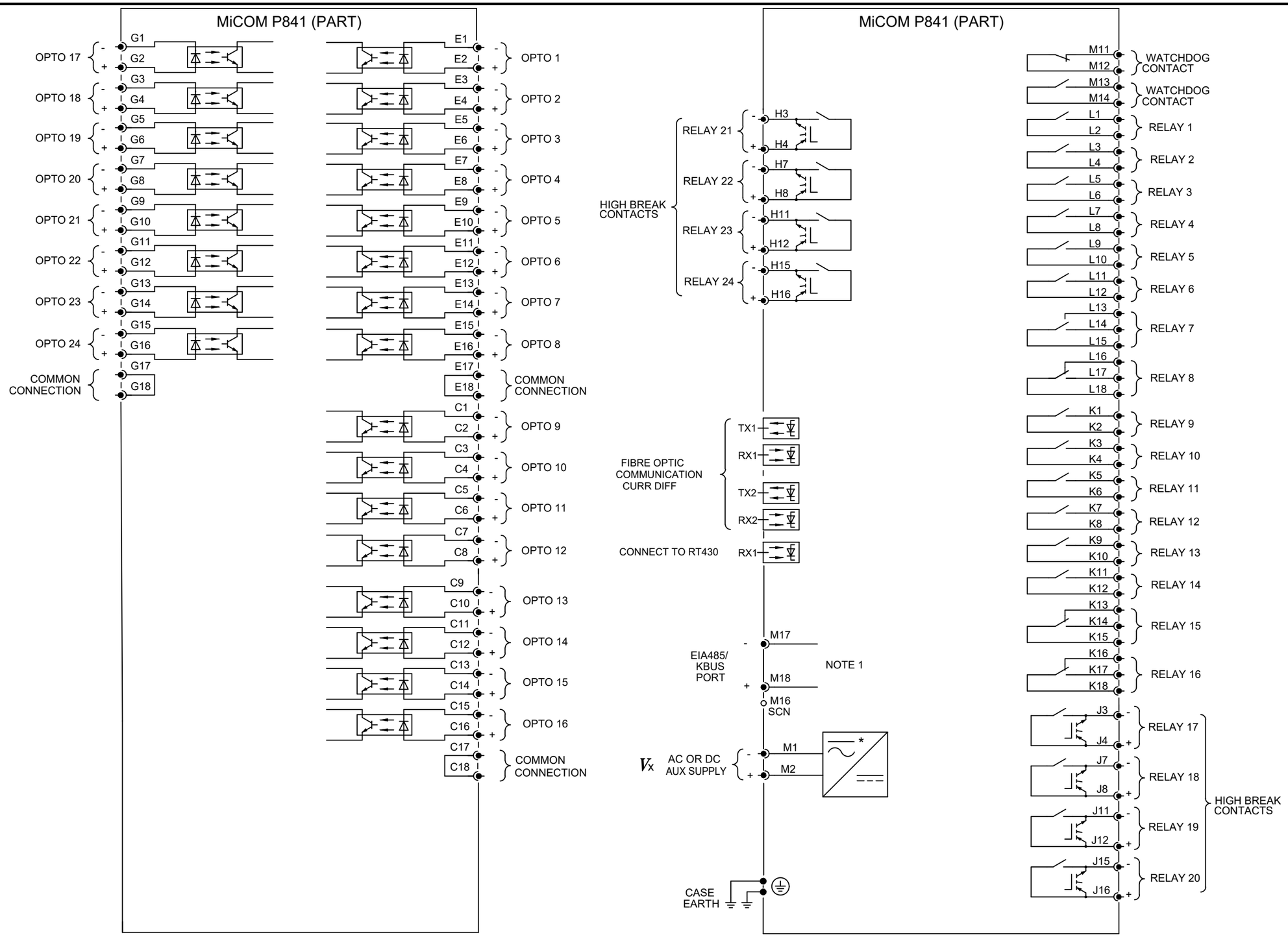
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

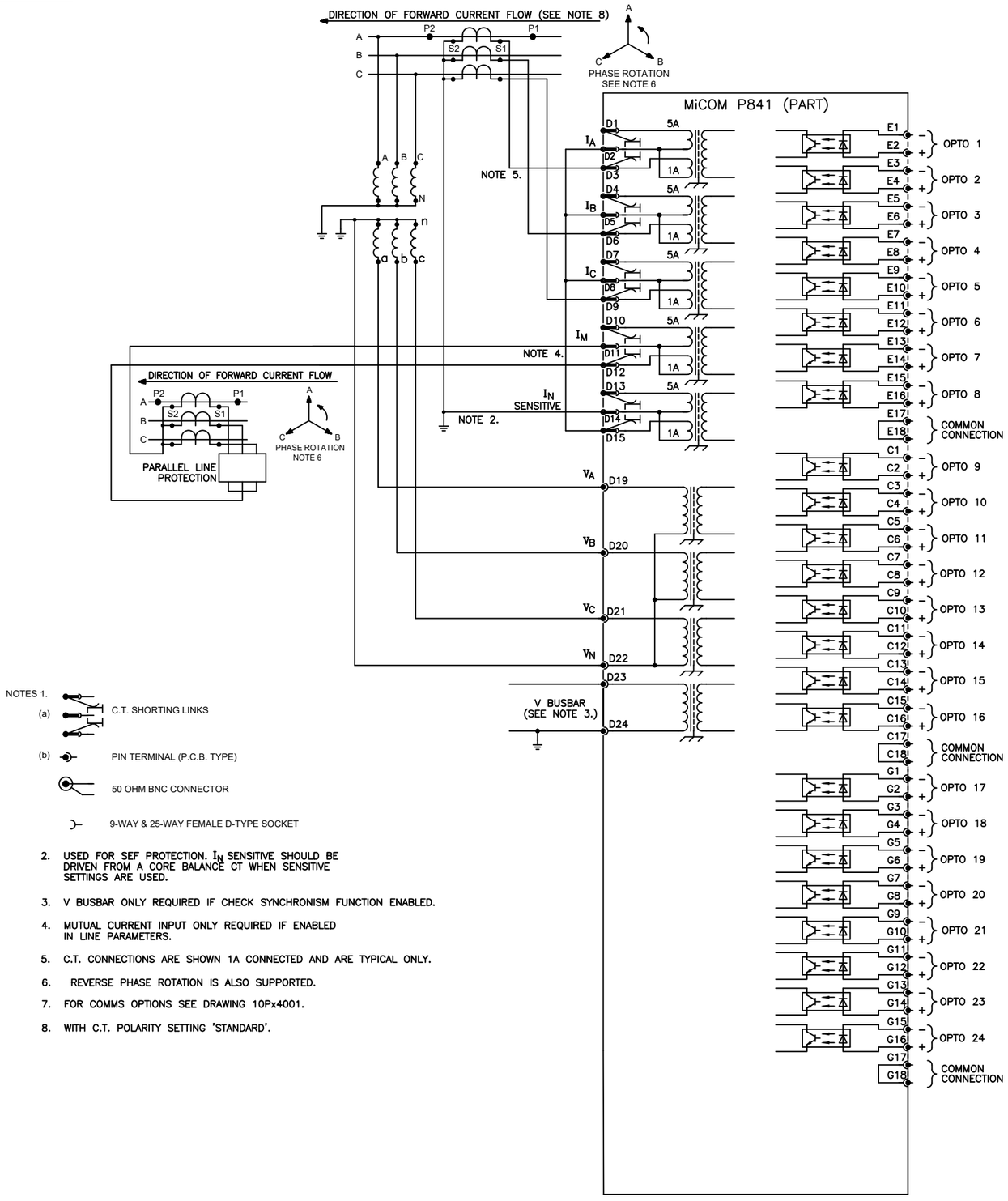
Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 24I/16O		
Date: 06/02/2024	Name: S WOOTTON		Drg No: **10P84187**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: A	Revision: CID007390. INITAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 24I/16O + 8 HIGH SPEED HIGH BREAK RELAYS		
Date: 31/08/2022	Name: S WOOTTON		Drg No: 10P84145	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
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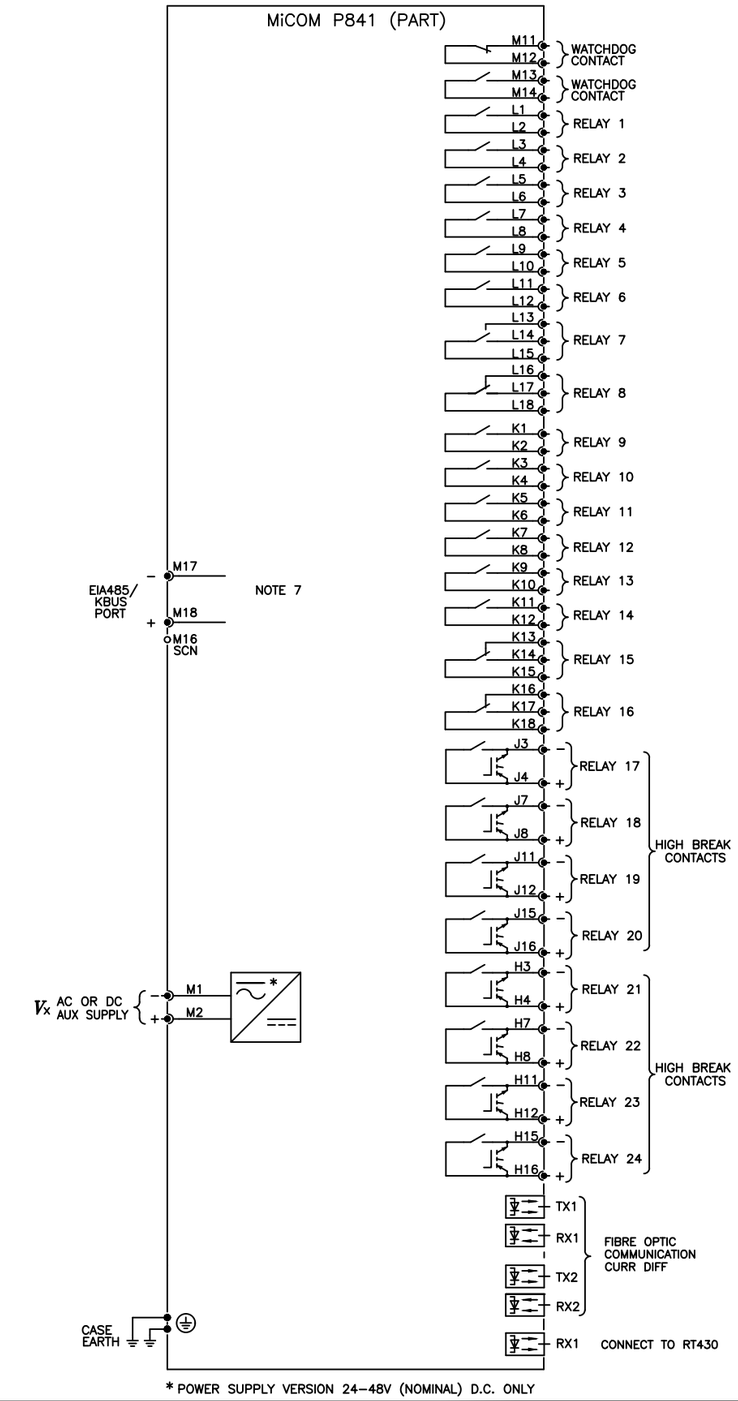
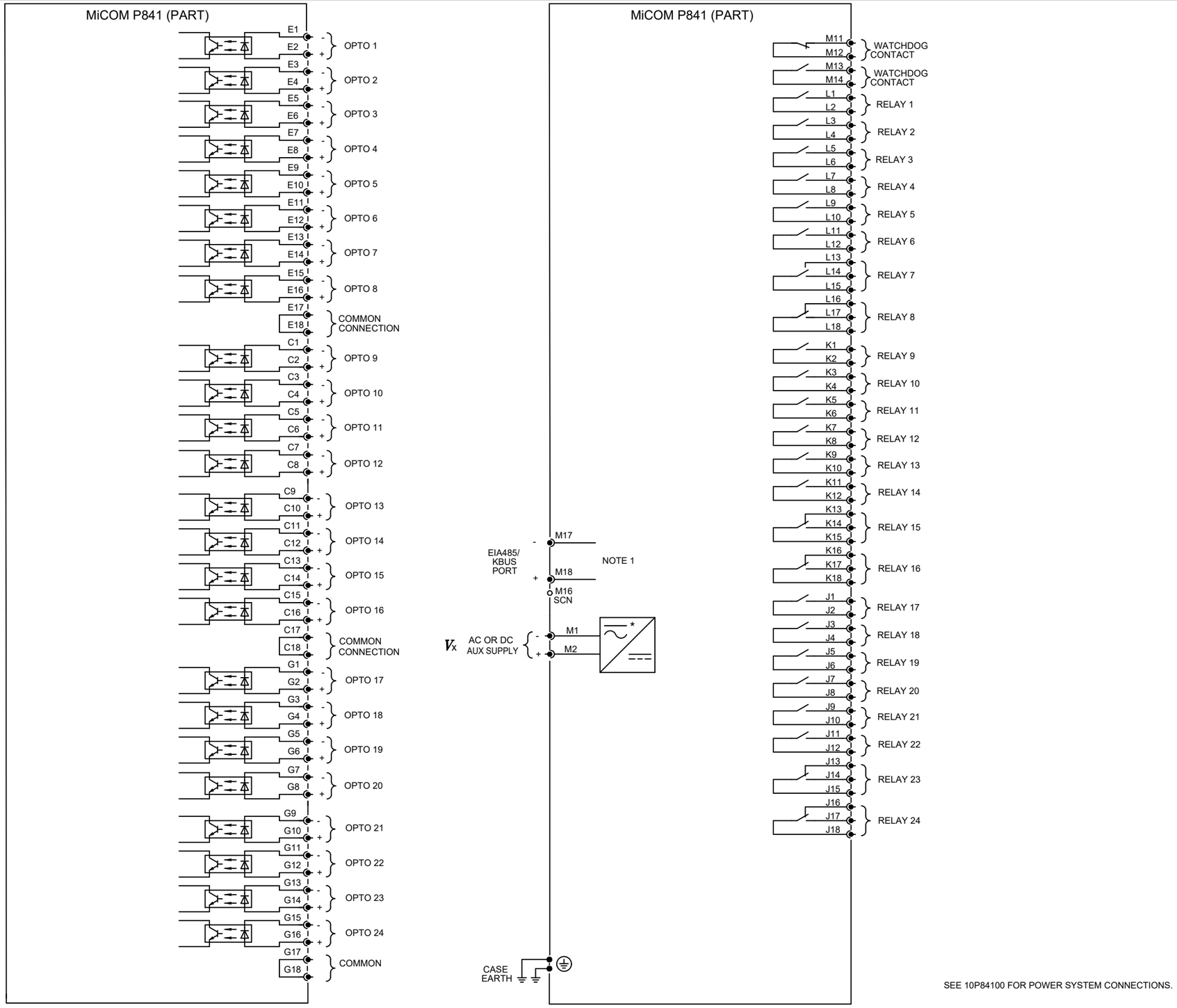
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.



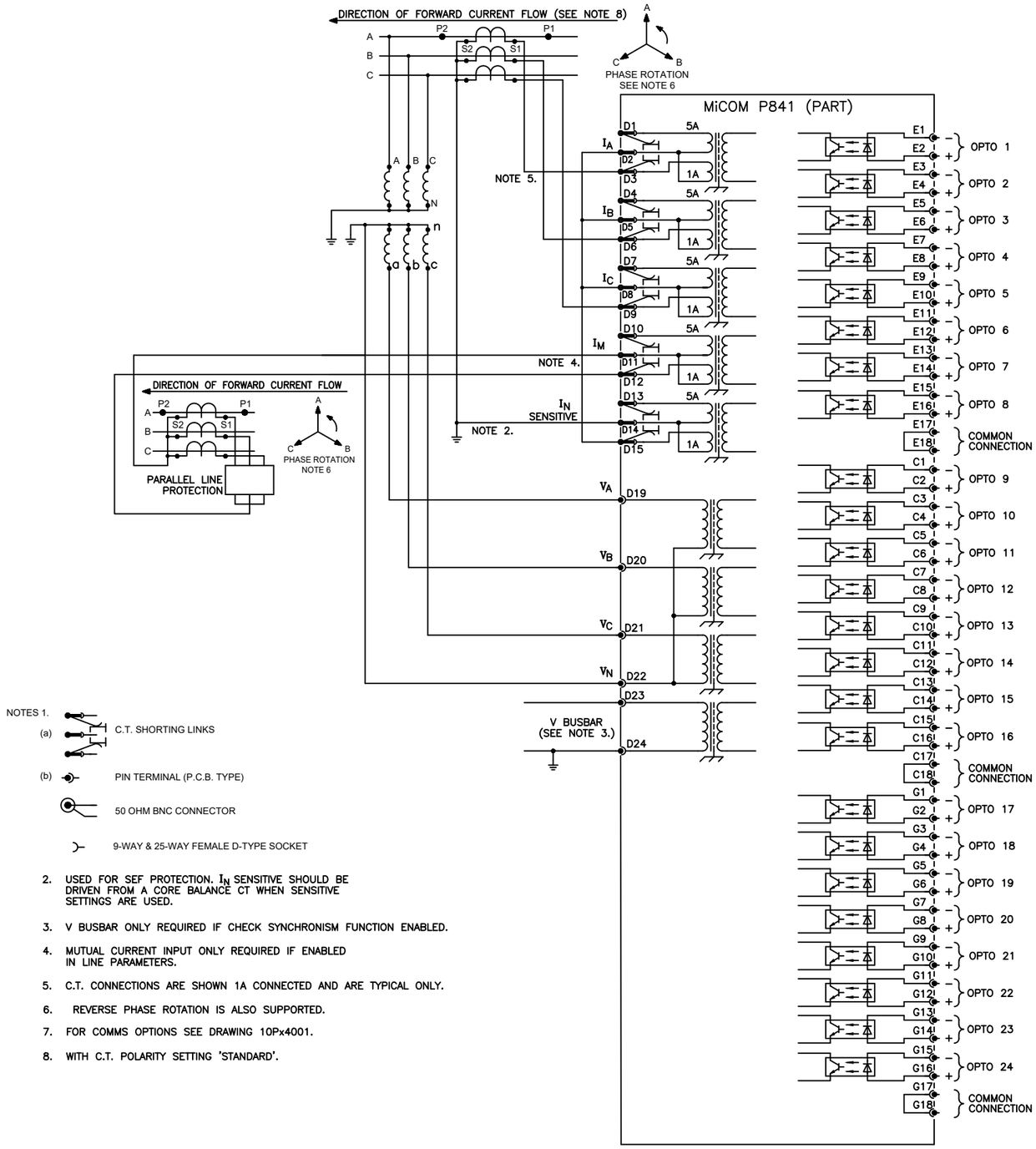
* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

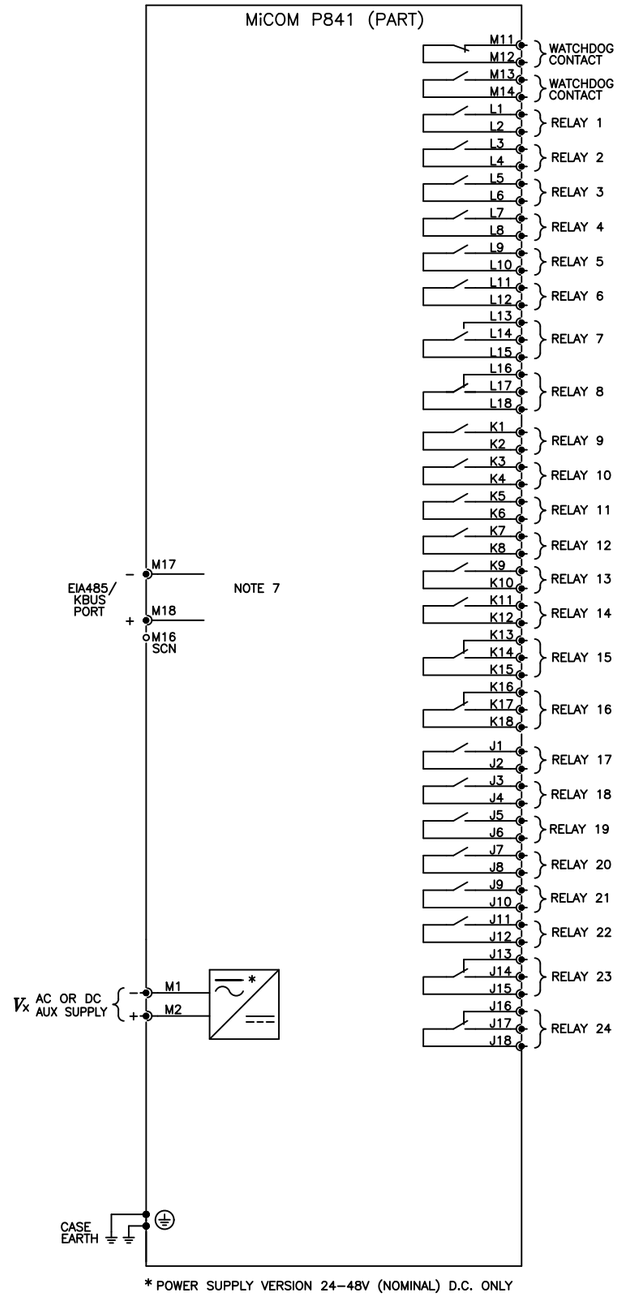
Issue: A	Revision: CID007472. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 24I/16O + 8 HIGH SPEED HIGH BREAK RELAYS		
Date: 20/10/2022	Name: S WOOTTON		Drg No: 10P84150	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 24I/24O		
Date: 30/01/2024	Name: S WOOTTON		Drg No: **10P84179**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
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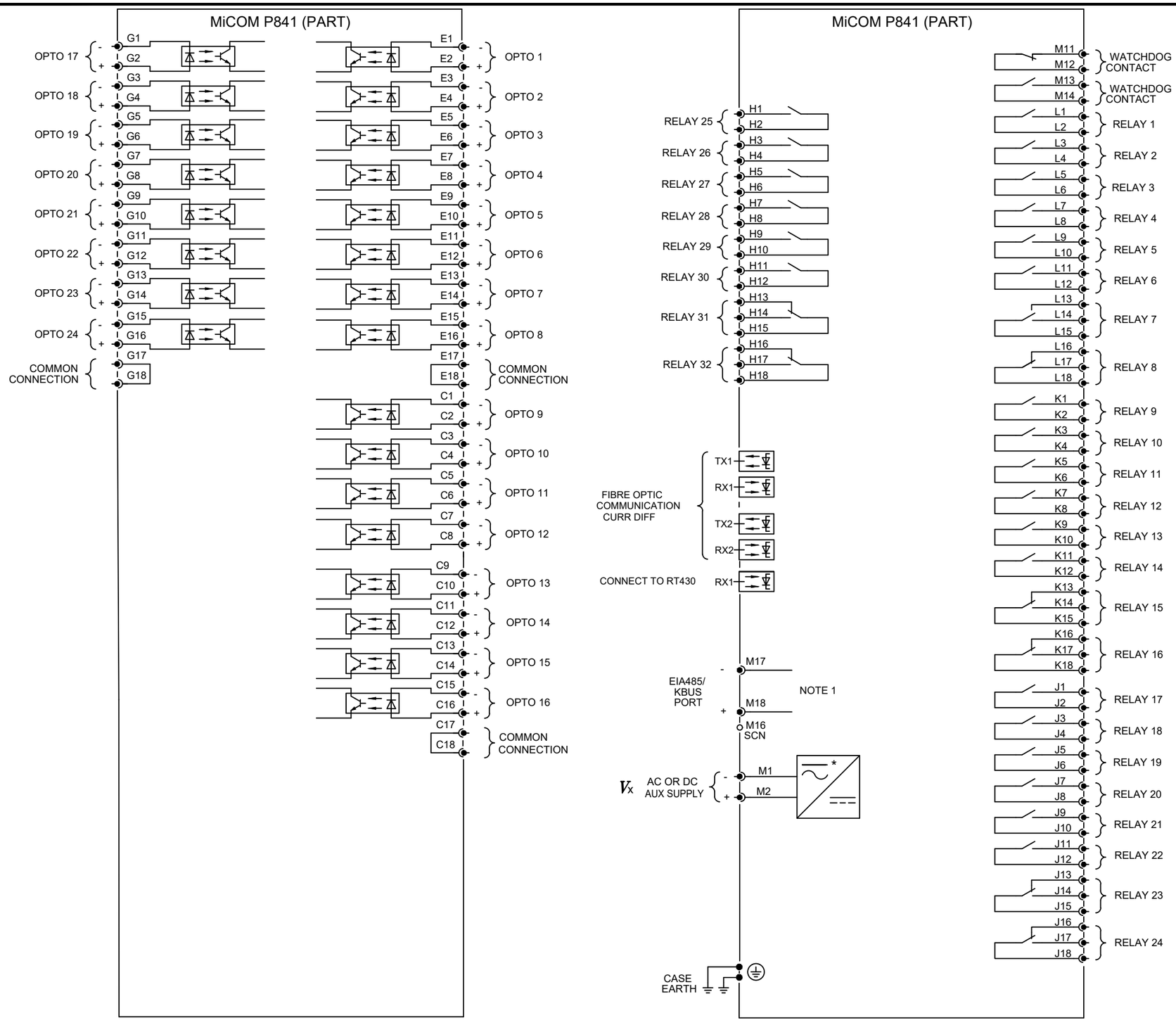
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

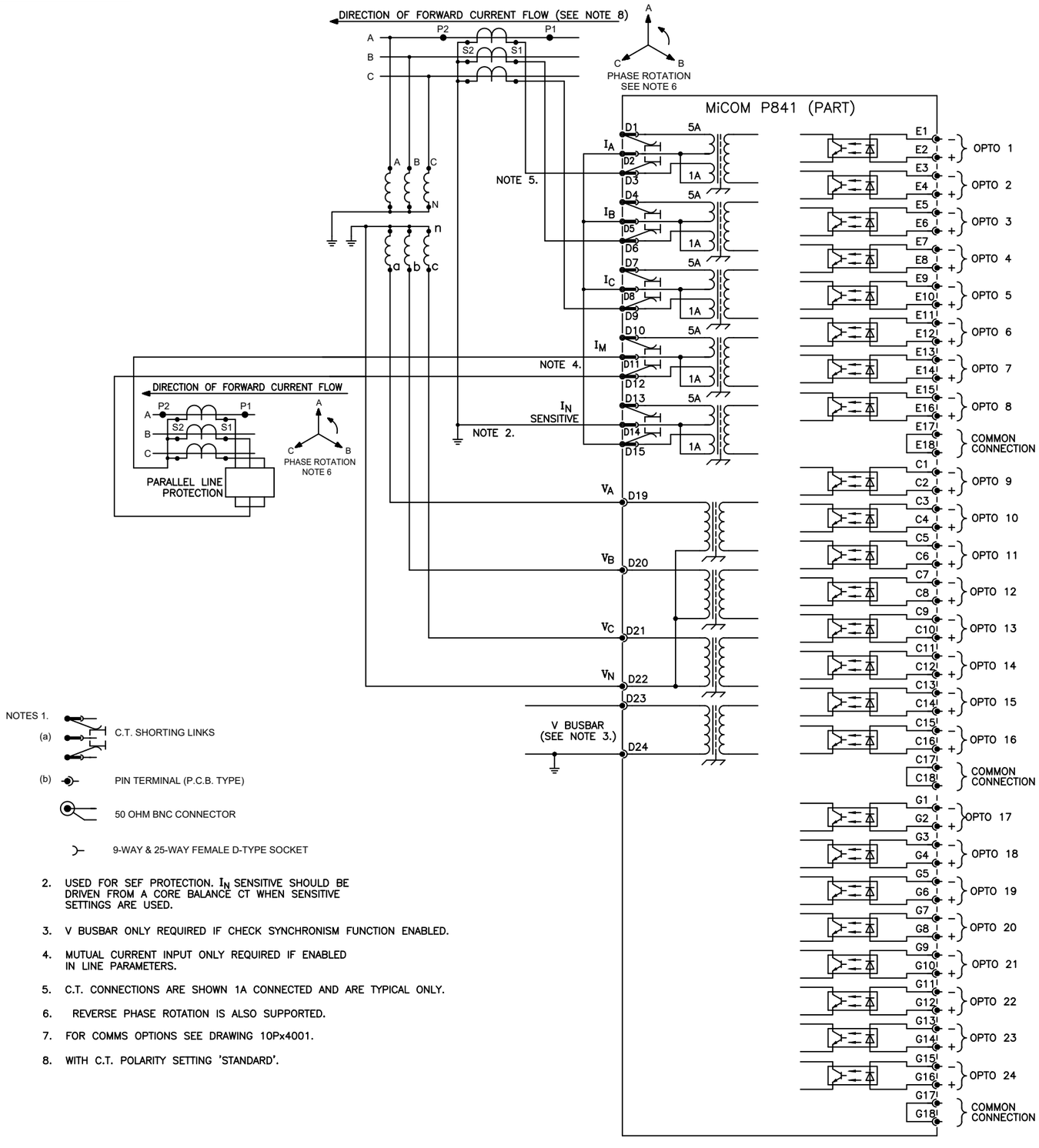
Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 24I/24O		
Date: 06/02/2024	Name: S WOOTTON		Drg No: 10P84188	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	

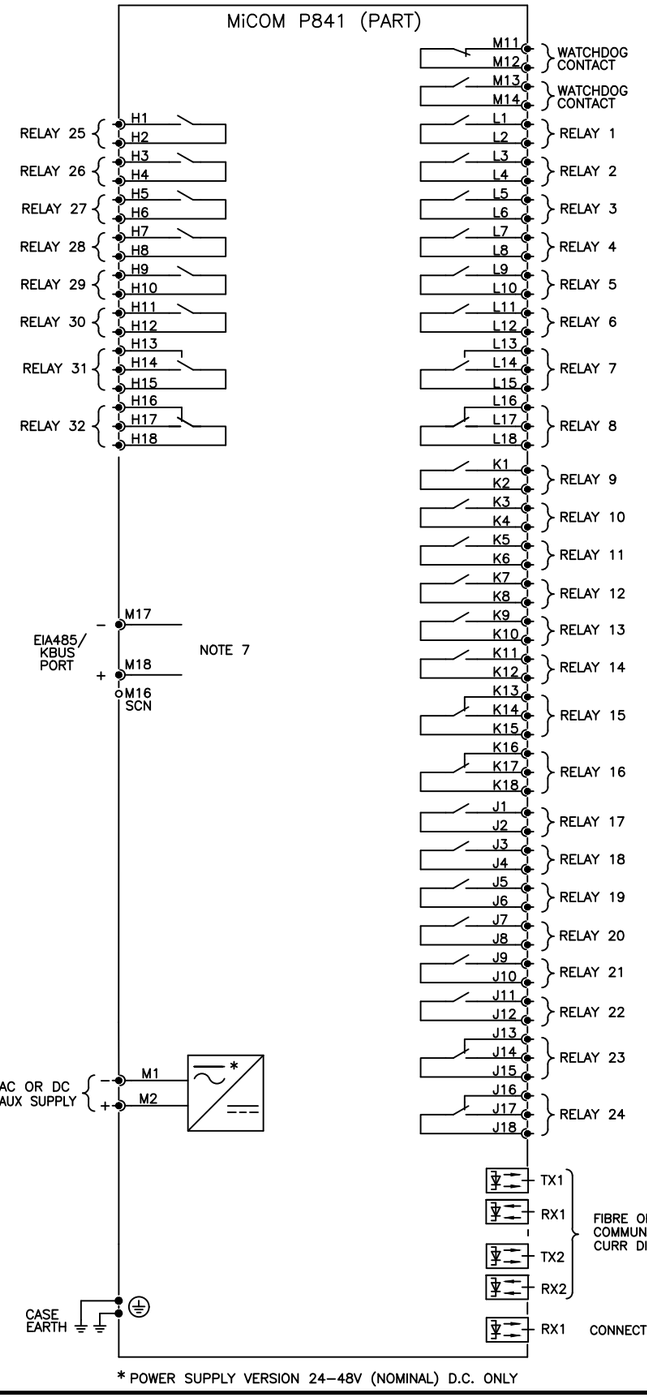


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: A	Revision: CID007390. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 24I/32O		
Date: 31/08/2022	Name: S WOOTTON		Drg No: 10P84146	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd: S SWAIN			Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
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4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

Issue: A	Revision: CID007472. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 24I/32O	
Date: 20/11/2022	Name: S WOOTTON		Drg No: 10P84151	Sht: 1
Date:	Chkd:			Next Sht: -

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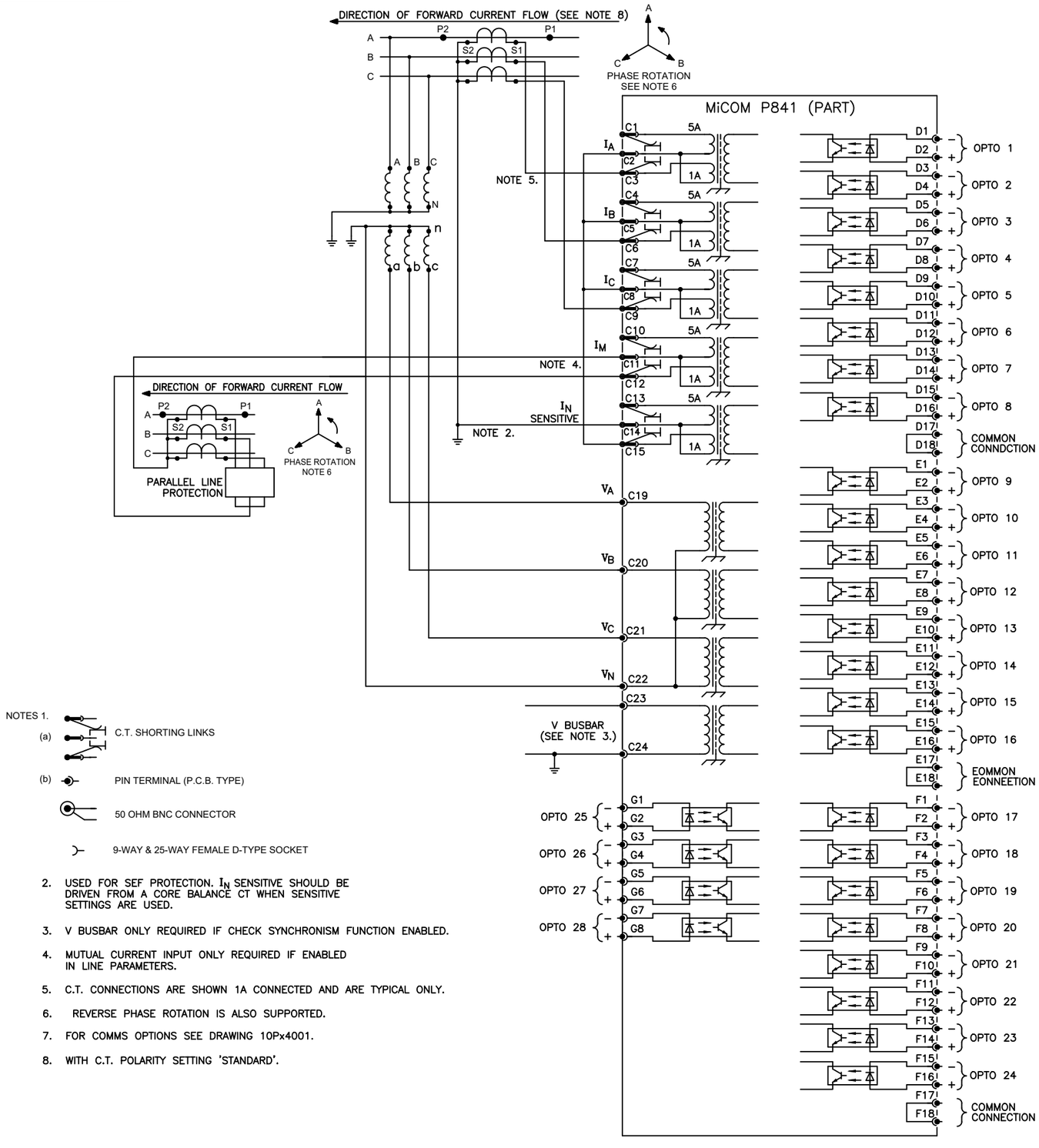
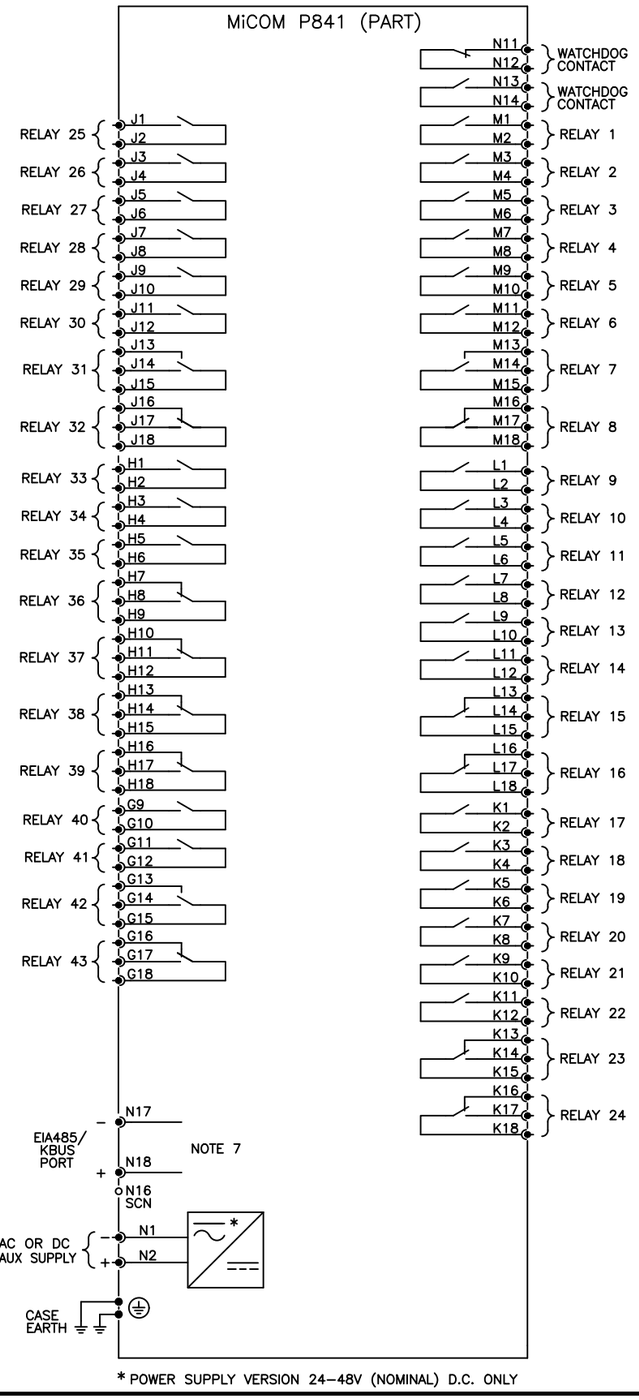
ST16 1WT, UK.





NOTES 1.

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(b) PIN TERMINAL (P.C.B. TYPE)

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7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Revision: CID008091. CURRENT DIFF CONNECTIONS REMOVED. ADDED IN ERROR.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 28I/43O	
Date: 29/11/2023	Name: S WOOTTON		Drg No: 10P84154	Sht: 1
Date:	Chkd:			Next Sht: -

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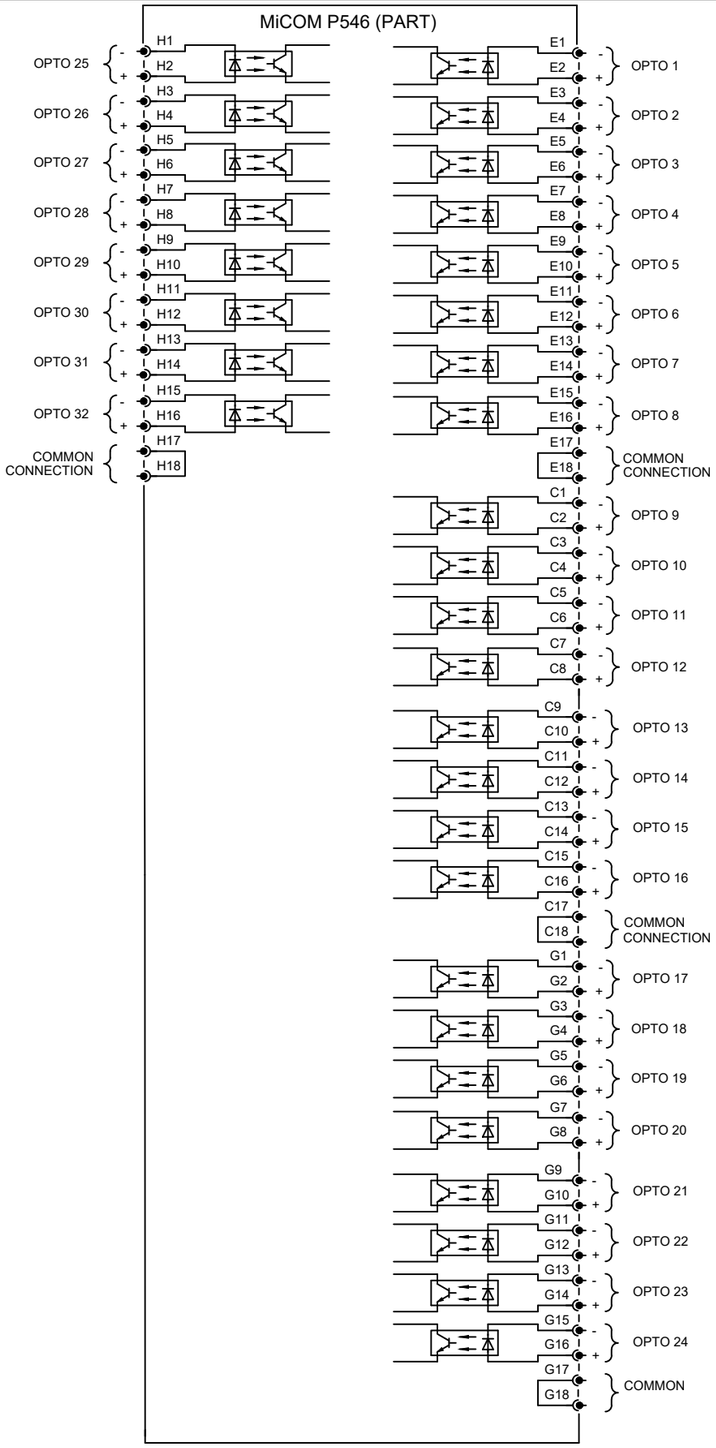
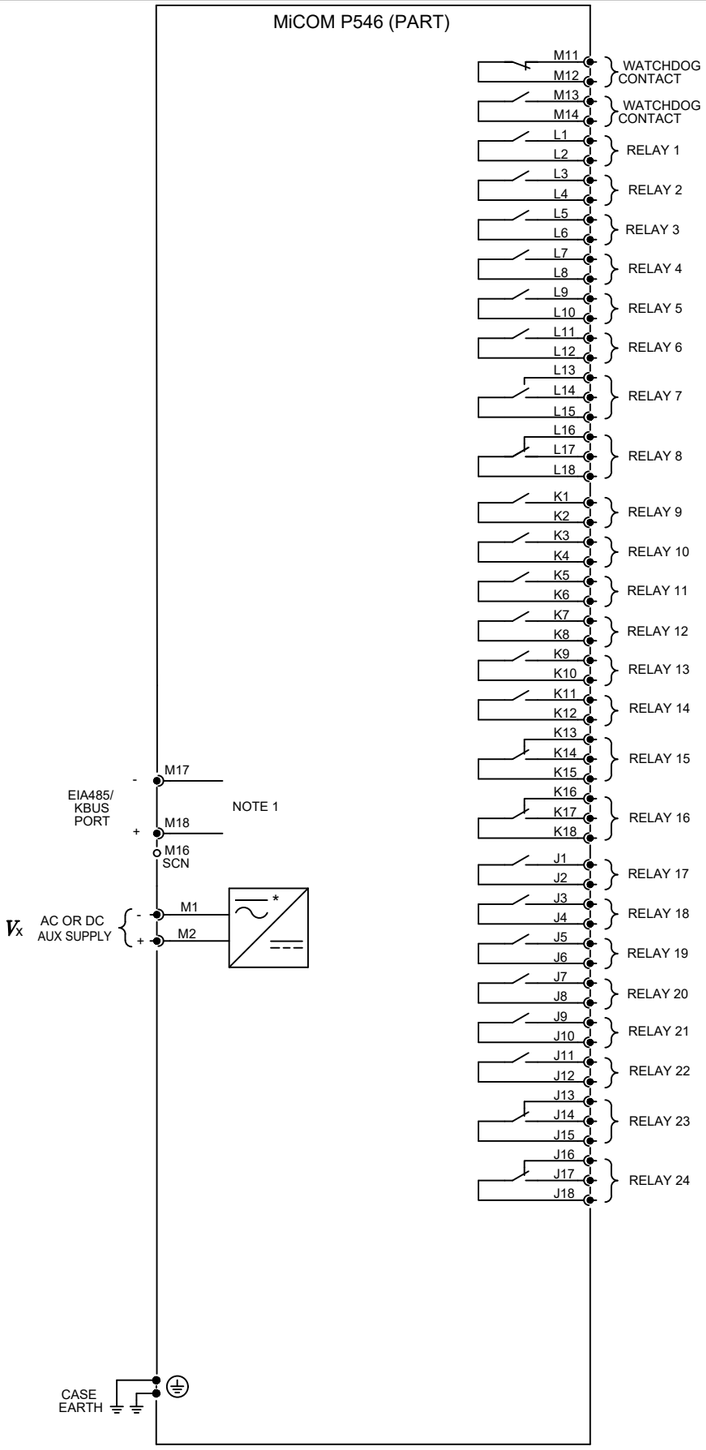


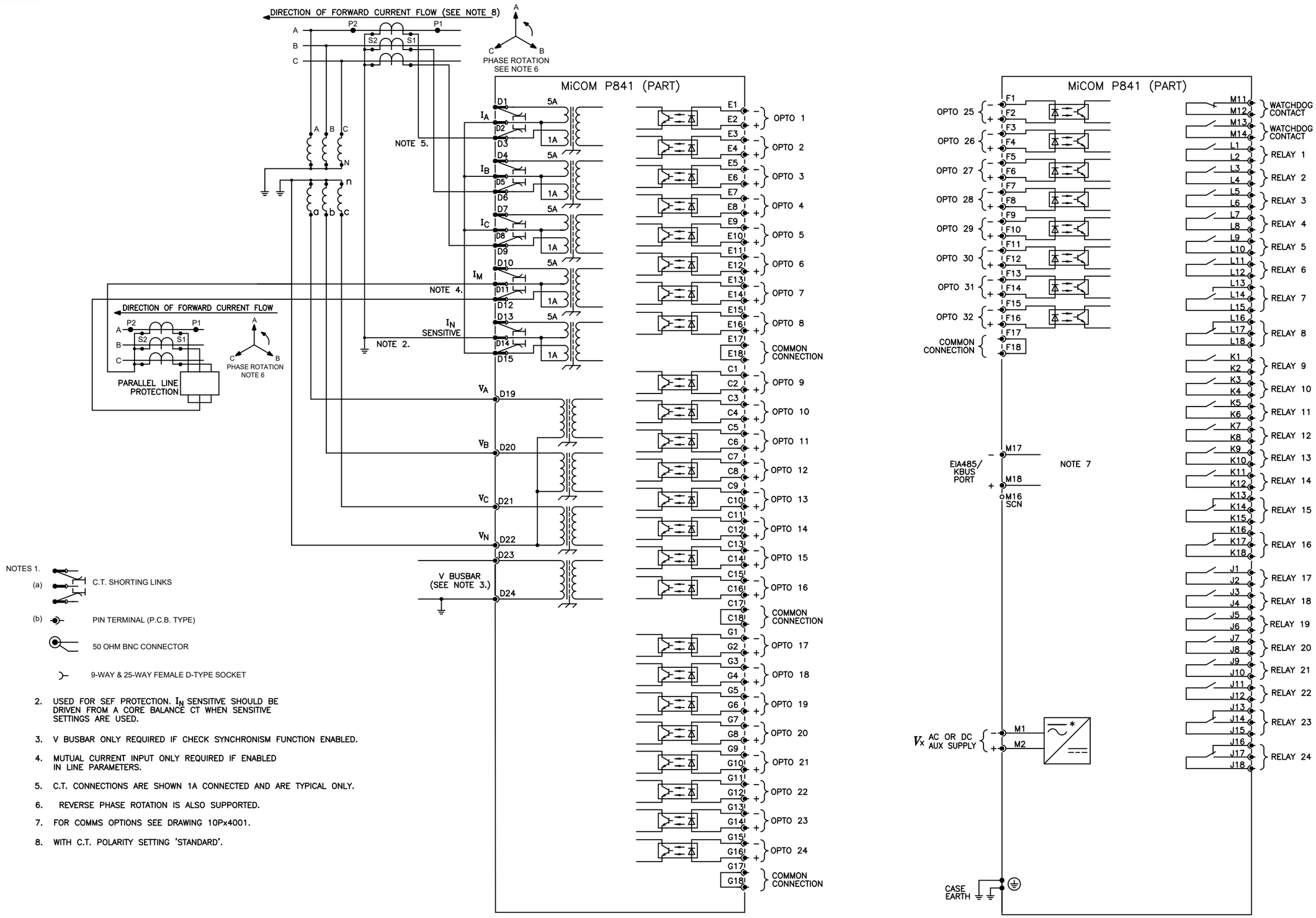


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

SEE 10P84100 FOR POWER SYSTEM CONNECTIONS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 32I/24O		
Date: 31/01/2024	Name: S WOOTTON		Drg No: 10P84181	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

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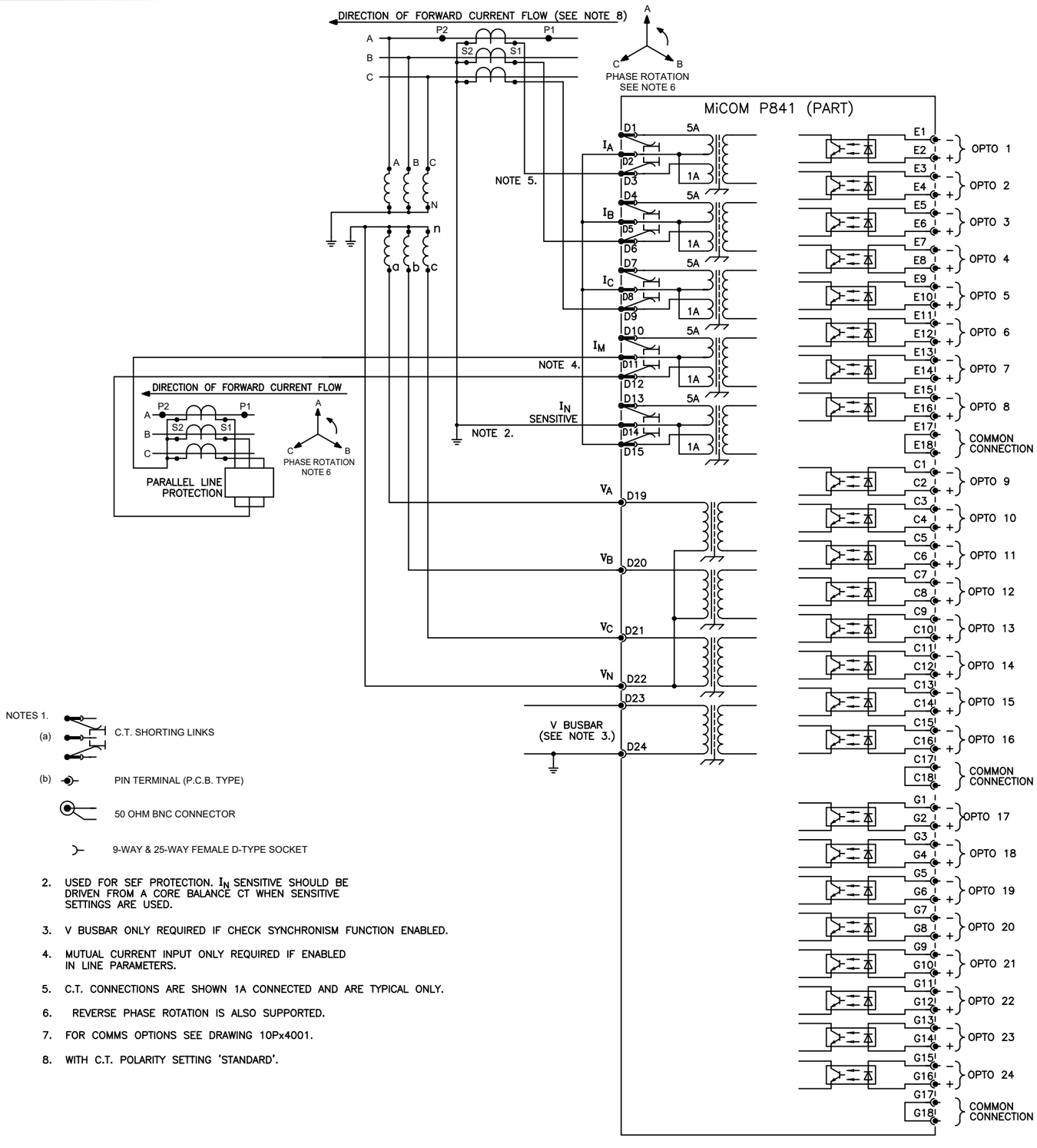
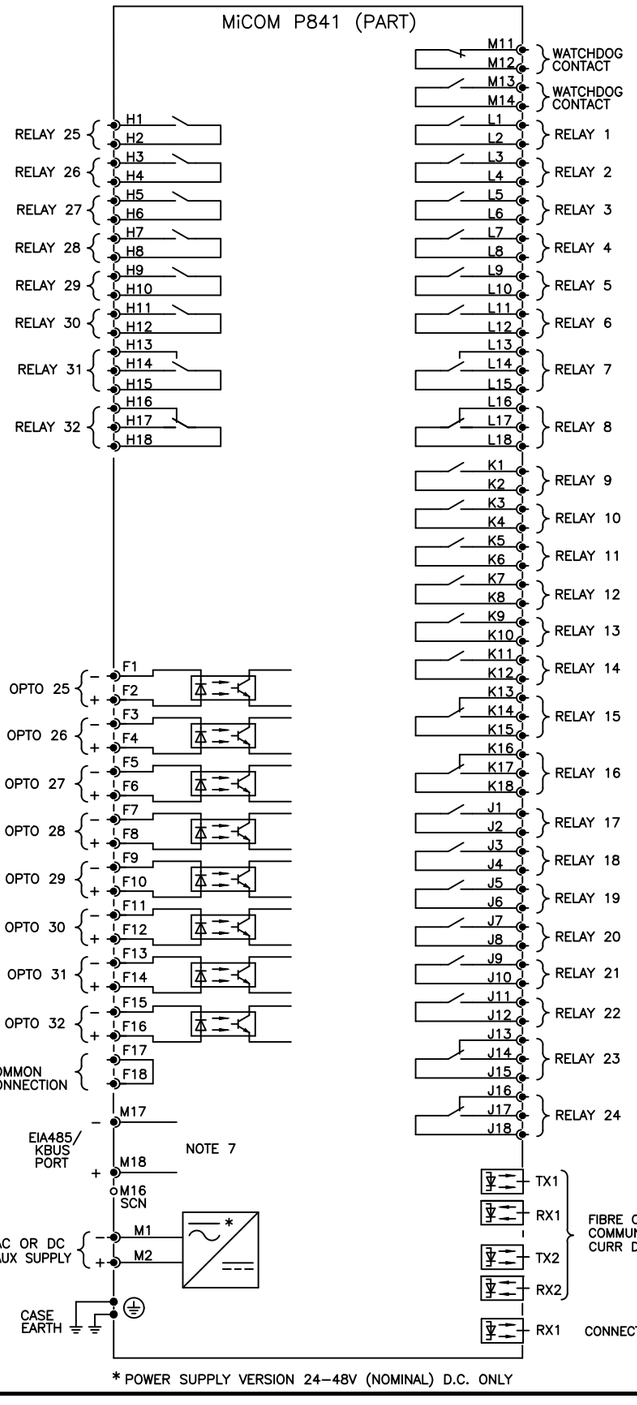
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 32I/24O		
Date: 06/02/2024	Name: S WOOTTON		Drg No: **10P84190**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

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9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: A	Revision: CID007472. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 32I/32O	
Date: 20/10/2022	Name: S WOOTTON		Drg No: 10P84152	Sht: 1
Date:	Chkd:			Next Sht: -

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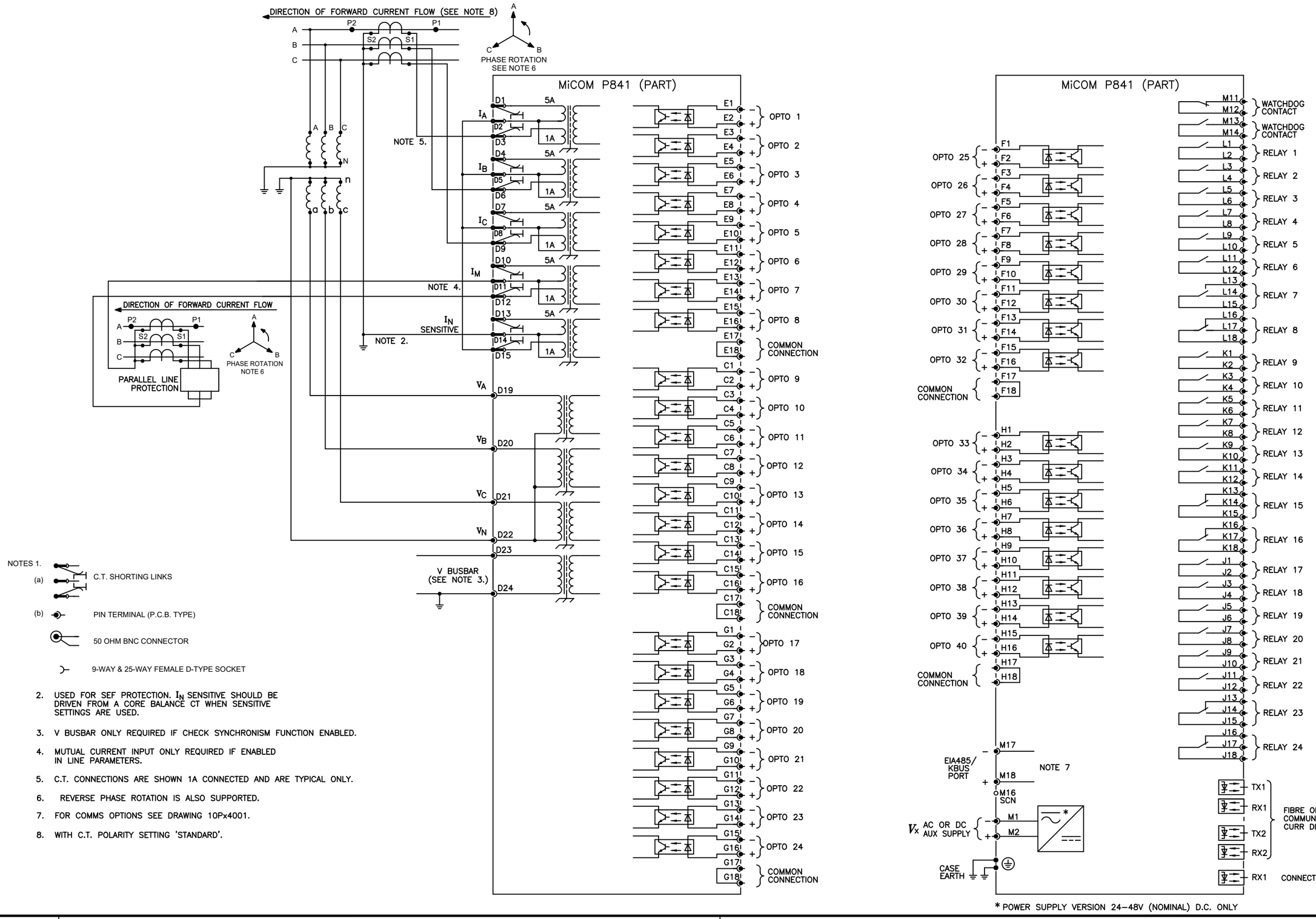
Stafford.
ST16 1WT, UK.



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: A	Revision: CID007472. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 40I/24O	
Date: 20/10/2022	Name: S WOOTTON		Drg No: 10P84153	Sht: 1
Date:	Chkd:			Next Sht: -

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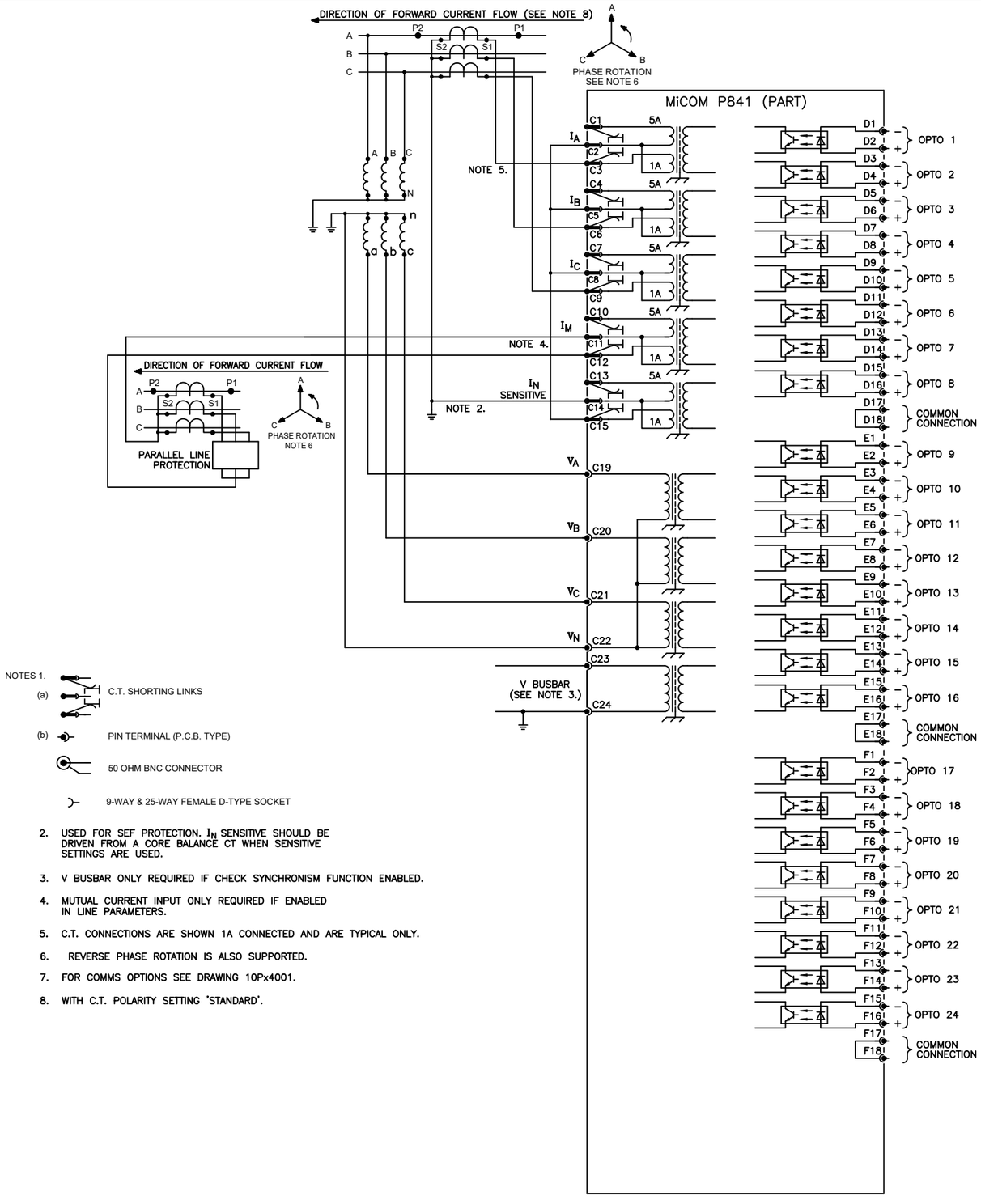

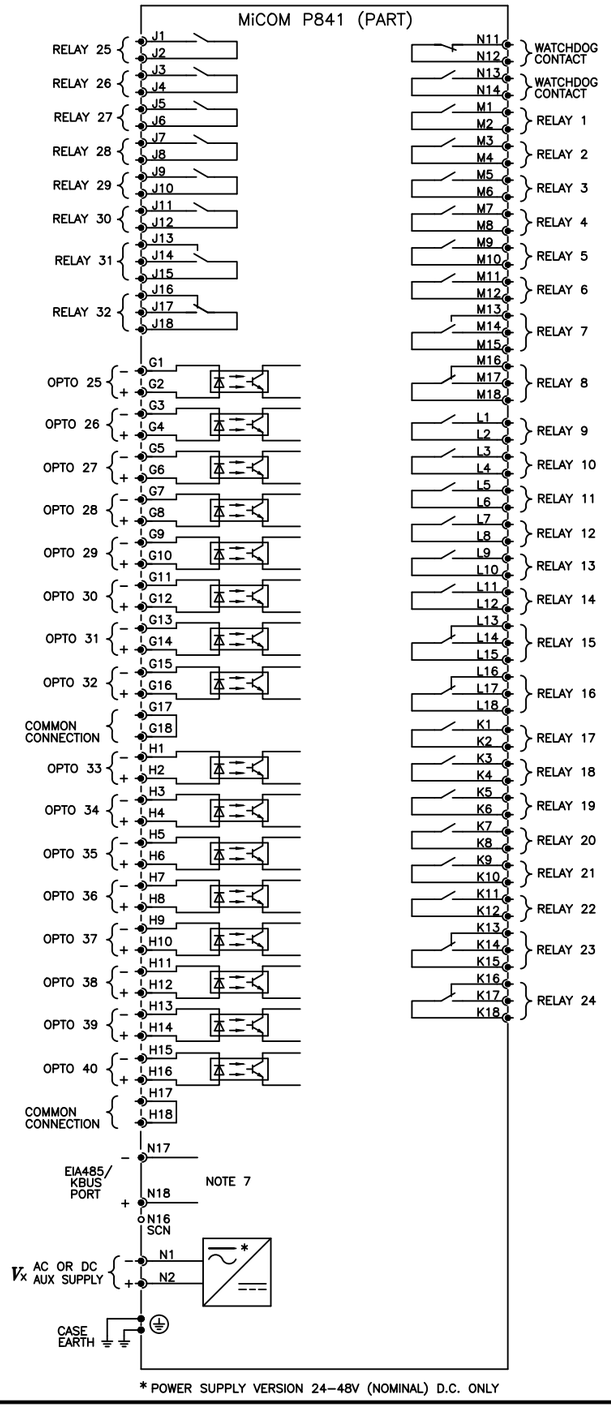

NOTES 1.

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9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM AUTORECLOSE (80TE) 40I/32O	
Date: 06/02/2024	Name: S WOOTTON		Drg No: 10P84191	Sht: 1
Date:	Chkd:			Next Sht: -

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APPENDIX D

VERSION HISTORY

1 HARDWARE AND SOFTWARE VERSION HISTORY

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
40	A	K	4 May 2006	Release of P543, P544, P545 & P546 without distance protection ▪ CTS ▪ Definitive time directional negative sequence overcurrent I2> ▪ GPS synchronization of current differential in all models ▪ P543 and P545 now facilitate in zone transformer-feeder applications ▪ All models support ABC and ACB phase rotation ▪ Standard and Inverted CT polarity setting for each set of CTs in the relay ▪ User interface with tri colored LED and function keys ▪ InterMiCOM64 ▪ Voltage protection ▪ Backwards compatibility mode	Patch for V2.12 V2.13 or later	P54x/EN M/I64
41	C	K	30 July 2006	Release of P543, P544, P545 & P546 without distance protection based on 40A ▪ IEC 61850-8-1 ▪ High break options ▪ Demodulated IRIG-B options ▪ Reduction of distance minimum reach settings to 0.05 ohm ▪ Permissive trip reinforcement ▪ Poledead modifications for Hydro Quebec ▪ CS103/auto-reclose modifications	Patch for V2.12 V2.13 or later	P54x/EN M/J74
41	D	K	16 August 2006	Release of P543, P544, P545 & P546 without distance protection based on 41C ▪ Prevents a possible reboot 15 minutes after browsing the front courier port but not making a setting change i.e. browsing using PAS&T ▪ Extended GOOSE enrolment capability ▪ Correction to ICD files, enumeration (value) and fixed data mapping	Patch for V2.12 V2.13 or later	P54x/EN M/J74
41	E	K	14 November 2006	Release of P543, P544, P545 & P546 without distance protection based on 41D ▪ Prevent a reboot in 61850 builds when NIC link is inactive and avalanche of DDB activity ▪ Correctly report a fatal error generated by the sampling call-back ▪ Correct the operation of the GOOSE messaging and a problem with the download of an IED Configuration file ▪ Correct the operation of the check sync ▪ Correct the operation of the overcurrent reset curves ▪ Removed check on the14th position of model number	Patch for V2.12 V2.13 or later	P54x/EN M/J74

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
41	E	K	14 November 2006	▪ Fixed Telegrams for public inf. 64-67	Patch for V2.12 V2.13 or later	P54x/EN M/J74
41	F	K	15 May 2007	Release of P543, P544, P545 & P546 without distance protection based on 41E ▪ Prevent a fatal error from an incorrect DNP address in not using DNP evolutions platform ▪ Default setting for 450B 'I< Current Set' reduced to 50mA ▪ French translations for DDBs 1368-1371 corrected ▪ Fun & INF values related to CS103 Command Blocking corrected ▪ Angle for negative sequence phase overcurrent setting corrected ▪ Corrected operation when using MiCOM S1 is used to activate settings group by right clicking on the group ▪ Corrected the latching of Function Key DDB signals on relay power up ▪ Corrected disturbance recorder scaling to prevent high current levels into 5A CT causing the disturbance recorder to saturate ▪ Restring defaults appears not to change the 1/5A CT selection ▪ Corrected the performance of the IM64 direct mode ▪ CB control via direct access does not work with 2CB versions of P540D ▪ Auto-reclose dead time/close cycle continues even if AR switched out of service ▪ Ch2 Statistics may not be displayed	Patch for V2.12 V2.13 or later	P54x/EN M/J74
41	G	K	May 2007	P543, P544, P545 & P546 non 61850 builds without distance protection based on 41F was approved for release but withdrawn before release ▪ Corrections to enable/disable of auto-reclose	Patch for V2.12	P54x/EN M/J74
41	H	K	4 July 2007	Release of P543, P544, P545 & P546 without distance protection based on 41G ▪ Corrections to enable/disable of auto-reclose	Patch for V2.12	P54x/EN M/J74
41	I	K	14 January 2010	Release of P543, P544, P545 & P546 non 61850 builds without distance protection based on 41H ▪ Prevented the differential protection inhibiting in three terminal schemes when GPS is enabled and loopback mode selected ▪ Improvements to the GPS code ▪ Improvements in the clock recover circuits used by the differential comms ▪ Correction to P545/P541 compatibility when used in transformer compensation mode ▪ Correction to the way latched LED/Relays are cleared ▪ Corrections to the Current Differential Inhibit when the GPS synchronization is disabled	Patch for V2.12	P54x/EN M/J74

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
41	I	K	14 January 2010	▪ Corrections to menu text ▪ Correction to auto-reclose operation for switch on to fault condition ▪ Corrected some French and German text ▪ Prevented CB Operating Time displaying 4.295Ms ▪ Fixed Inhibit CB Fail Protection in P544/6 ▪ Improved co-processor error reporting ▪ Fixed a SOTF problem	Patch for V2.12	P54x/EN M/J74
41	J	K	5 October 2010	Release of P543, P544, P545 & P546 non 61850 builds without distance protection based on 41J ▪ Fixed a problem with the co-processor stack check which could cause a re-boot	Patch for V2.12	P54x/EN M/J74
42	A	K	May 2007	Release of P543, P544, P545 & P546 without distance protection ▪ Chinese interface ▪ Replacing the existing DNP3.0 with the DNP3.0 evolutions ▪ Replacement of existing negative sequence overcurrent with multi-stage (2 IDMT + 2 DT) negative sequence overcurrent. ▪ Addition of IDG curve, commonly used in Sweden, to Earth Fault & Sensitive Earth Fault (involves moving settings) ▪ Reduction of all TMS step sizes to 0.005 ▪ Addition of Channel propagation delay statistics and alarms ▪ Changes to CTS so both techniques can be selected together ▪ Regrouping of CTS settings ▪ Addition of four stages of under frequency protection and two stages of overfrequency protection ▪ Addition of df/dt protection ▪ Changes to under and overvoltage to enable each stage to be independently set ▪ Extensions to the check sync VT position setting ▪ Changes to Permissive Inter Trip (PIT) logic to enable the user to select either local or remote current to be used ▪ Includes local time zone settings for date & time ▪ Reduced minimum setting for IN> I2pol Set ▪ Addition of propagation delay times to Fault Record ▪ Default setting for 450B 'I< Current Set' reduced to 50mA ▪ Enhancement to self-checking of output relays ▪ Change tunnelled courier address to follow the 1st Rear Port's KBUS or CS103 address	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
42	B	K	4 July 2007	Release of P543, P544, P545 & P546 without distance protection based on 42A ▪ Improvements to VTS ▪ Corrections to enable/disable of auto-reclose ▪ Resolved a problem relating to CT Ratio's not being restored when restoring default settings ▪ Resolved a problem with the Disturbance Recorder which saturates for high current levels into 5A CT	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
42	D	K	17 December 2007	Release of P543, P544, P545 & P546 without distance protection based on 42B ▪ Fixed a number of 61850/Goose problems ▪ Minor correction to fault record ▪ Corrections to over voltage stage 2 inhibit ▪ Fixed the max. prop alarm ▪ Corrected some DDB German text	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
42	E	K	14 May 2008	Release of P543, P544, P545 & P546 without distance protection based on 42D ▪ Fixed a number of 61850 problems ▪ Improved co-processor error reporting ▪ Fixed Inhibit CB Fail Protection in P544/6	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
42	F	K	-	Not released to production. Based on 42E ▪ Correction to auto-reclose operation for switch on to fault condition ▪ Prevented CB Operating Time displaying 4.295Ms ▪ Bug fixes	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
42	G	K	28 October 2008	Release of P543, P544, P545 & P546 without distance protection based on 42F ▪ Correction to the distance cross polarizing when the memory expires	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
42	H	K	21 September 2009	Release of P543, P544, P545 & P546 without distance protection based on 42G ▪ Corrected some menu translations ▪ Corrected Breaker Fail - WI Aided1 trips so they can be disabled via setting "WI Prot Reset" ▪ Timestamp in fault record adjusted for the local time setting ▪ Corrected P543 default PSL ▪ Corrections to the Current Differential Inhibit when the GPS synchronisation is disabled ▪ Corrected Thermal State measurement via DNP3.0 ▪ Correction to the way latched LED/Relays are cleared ▪ Correction to negative sequence overcurrent settings when 5A input used	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
42	H	K	21 September 2009	▪ Correction to P545/P541 compatibility when used in transformer compensation mode ▪ Improvements to the GPS code ▪ Prevented CTS generating events when CTS is disabled ▪ Prevent Z5 from setting slow swing when PSB is disabled ▪ Fixed problem which prevented residual overvoltage from initiating CB Fail ▪ Various improvements to DNP3.0, CS103 & IEC 61850 protocols ▪ Bug fixes	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
42	I	K	6 December 2010	Release of P543, P544, P545 & P546 without distance protection based on 42H ▪ Fixed a 61850 issue which blocked clients when one was disconnected ▪ Rebranded as Alstom. Minor change to software number plus changes to 61850 (New ICD files required) ▪ Bug fixes	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
42	K	K	12 September 2014	Release of P543, P544, P545 & P546 without distance protection based on 52J ▪ Current Differential communications are not stopped temporarily when navigating the default display ▪ CT Supervision can be operated in P543 42K software. ▪ CB Fail trip can be operated under faults with DC transient offsets. ▪ Bug fixes Release of P543 & P545 with distance protection based on 42J ▪ Disconnection of one of IEC 61850 Client causes other IEC 61850 Connections being Lost ▪ The disturbance record list does not show the most recent DR ▪ P145 reboots periodically when IEC 61850 comms active and SNTP active ▪ Discrepancy in the DR analogue signals magnitudes if the CT and VT ratios (primary/secondary) are not integers ▪ Incorrect behaviour of the latched LED		
44	A	K	18 March 2008	Release of P543, P544, P545 & P546 without distance protection based on 42D ▪ Positional information added to PSL ▪ DNP 3.0 Over Ethernet protocol added ▪ Extended I/O - status inputs increased from 24 to 32 ▪ Compensated overvoltage protection added ▪ IEC-103 Generic Services Measurements added ▪ Set/Reset Latch Logic Gates added to PSL ▪ Fault record to include current differential currents recorded at the time of the current differential trip in addition to the existing data from 1 cycle later ▪ Fault record increased max. number of fault records to 15	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
44	A	K	18 March 2008	▪ GPS Alarm modifications ▪ DNP enhancements for SSE ▪ Bug fixes	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
44	B	K	25 June 2008	Release of P543, P544, P545 & P546 without distance protection based on 44A ▪ Fixed a number of 61850 problems ▪ Improved co-processor error reporting ▪ Fixed Inhibit CB Fail Protection in P544/6 ▪ Corrected some French and German text ▪ Prevented CB Operating Time displaying 4.295Ms ▪ Fixed a problem which prevented extraction of DNP3.0 setting files from DNP3.0 over Ethernet variants	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
44	D	K	20 January 2009	Release of P543, P544, P545 & P546 without distance protection based on 44B ▪ Corrections to the Current Differential Inhibit when the GPS synchronisation is disabled ▪ Corrected Thermal State measurement via DNP3.0 ▪ Timestamp in fault record adjusted for the local time setting ▪ Corrected Breaker Fail - WI Aided1 trips so they can be disabled via setting "WI Prot Reset"	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
44	E	K	20 March 2009	Release of P543, P544, P545 & P546 without distance protection based on 44D ▪ Prevents the loss of IEC 61850 messages and fixed the handling of the ACD flag during GI ▪ Improved the Ethernet card boot code	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
44	F	K	21 September 2009	Release of P543, P544, P545 & P546 without distance protection based on 44E ▪ Corrected some menu translations ▪ Corrected P543 default PSL ▪ Correction to the way latched LED/Relays are cleared ▪ Correction to negative sequence overcurrent settings when 5A input used ▪ Correction to P545/P541 compatibility when used in transformer compensation mode ▪ Improvements to the GPS code ▪ Prevented CTS generating events when CTS is disabled ▪ Fixed problem which prevented residual overvoltage from initiating CB Fail ▪ Various improvements to DNP3.0, CS103 & IEC 61850 protocols ▪ Bug fixes	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
44	G	K	19 October 2010	Release of P543, P544, P545 & P546 without distance protection based on 44F ▪ Fixed a 61850 issue which blocked clients when one was disconnected ▪ Improvements to Fault record display over Courier and DNP3.0 ▪ Bug fixes	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
44	H	K	11 January 2011	Release of P543, P544, P545 & P546 without distance protection based on 44G ▪ Rebranded as Alstom. Minor change to software number plus changes to 61850 (New ICD files required)	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
45	B	K	30 March 2009	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 44E ▪ Auto-reclose, Check Sync and CB Monitoring added to P544 & P546	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
45	C	K	15 May 2009	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 45B ▪ Improvements to the Ethernet card start-up and configuration ▪ Correction to negative sequence overcurrent settings when 5A input used ▪ Correction to P545/P541 compatibility when used in transformer compensation mode ▪ Correction to the way latched LED/Relays are cleared ▪ Corrections to menu text ▪ Improvements to the GPS code ▪ Bug fixes	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
45	D	K	28 October 2009	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 45C ▪ Improvements to the GPS code ▪ Improvements in the clock recover circuits used by the Differential Comms. ▪ Bug fixes	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
45	E	K	11 January 2011	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 45D ▪ Rebranded as Alstom. Minor change to software number plus changes to 61850 (New ICD files required)	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
45	F	K	15 June 2012	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 45E ▪ Fixed dnp3 control of CB2 ▪ Improved the distance performance for cross country faults ▪ Enhanced the OST feature to make it more stable when currents are low ▪ Time stamping and status of IEC 61850 Data attribute sofPSOF1.ST.general.Op improved	Patch for V2.14 Studio FTP server	P54x/EN M/KA4

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
45	F	K	15 June 2012	▪ Improvements to Fault record display over courier and dnp3 ▪ Fixes to Autoreclose ▪ Improvements to co-processor SRAM checking ▪ Fixed PIT ▪ Several fixes to IEC 61850 problems ▪ Added Frequency trips to P445 default PSL ▪ Fixed an issue where Disturbance recorder could get out of sync	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
47	A	K	-	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 45D ▪ IEC 61850 phase 2 and 2.1 implemented ▪ Application for Inzone Transformers (2nd and 5th Harmonic Blocking/restraint) ▪ Differential Highset can be disabled when Inrush protection is enabled ▪ Restricted Earth Fault Protection (REF) ▪ Modification to Char Mod timer functionality ▪ Separate measurements for each set of CT's ▪ Interrupt Driven InterMiCOM in all models ▪ Read only mode	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB4
47	B	K	10 February 2010	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 47A ▪ Prevented the differential protection inhibiting in three terminal schemes when GPS is enabled and loopback mode selected ▪ Fault locator measurements in ohms corrected when 5A CT used or displayed in primary ▪ Frequency measurement in DNP3.0 fault record corrected	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB4
47	D	K	15 October 2010	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 47B ▪ Enhancement to GOOSE performance ▪ Fixes to 61850 ▪ Fixed protection comms. address problem in three ended scheme selected ▪ Fixed DNP3.0 control of CB2 ▪ Incorrect mapping of XCBR(n).CBOpCap.stVal data attribute corrected ▪ Improvements to fault record display over Courier and DNP3.0	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB4
47	E	K	11 January 2011	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 47D ▪ Rebranded as Alstom. Minor change to software number plus changes to 61850 (New ICD files required)	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB5

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
47	F	K	9 August 2012	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 47E ▪ Improvements to CB Fail reset times ▪ Several fixes to IEC 61850 problems ▪ Improved the co-processor SRAM checking ▪ Fixed an issue relating to Permissive Intertripping ▪ Improvement to disturbance recorder ▪ Bug fixes	Patch for V2.14 Studio FTP server	P54x/EN AD/Lb4 + P54x/EN M/La4
47	H	K	5 August 2015	Release of P543, P544, P545 & P546 without distance protection and P841-A based on 47F ▪ Correction to Error code "0x0C160013" related with the SRAM ▪ Fix an issue with P445 AutoReclose where local override by DDB was not allowed ▪ Improvement of the CB Fail operation under faults with DC transient offsets ▪ Fix a of a differential issue where the relay sometimes could reboot if working with IEE C37.94 and N=12 ▪ Other minor bug fixes	Patch for V2.14 Studio FTP server	P54x/EN AD/Lb4 + P54x/EN M/La4
50	A	K	4 May 2006	Release of P543, P544, P545 & P546 with distance protection and P443 based on Distance P443 SW 33 (Different hardware) ▪ Distance protection from P443 ▪ DEF from P443 ▪ Aided distance & DEF schemes from P443 ▪ CTS ▪ Definitive time directional negative sequence overcurrent I2> ▪ GPS synchronization of current differential in all models (N/A P443) ▪ P543 and P545 now facilitate in zone transformer-feeder applications ▪ All models support ABC and ACB phase rotation ▪ Standard and inverted CT polarity setting for each set of CTs in the relay ▪ User interface with tri-colored LED and function keys ▪ InterMiCOM^{64} ▪ Voltage protection ▪ Backwards compatibility mode	Patch for V2.12 V2.13 or later	P54x/EN M/I64
51	C	K	30 July 2006	Release of P543, P544, P545 & P546 with distance protection and P443 based on 50A ▪ IEC 61850-8-1 ▪ High break options ▪ Demodulated IRIG-B options ▪ Reduction of distance minimum reach settings to 0.05 ohm	Patch for V2.12 V2.13 or later	P54x/EN M/J74

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
51	C	K	30 July 2006	▪ Permissive trip reinforcement (N/A P443) ▪ Poledead modifications for Hydro Quebec ▪ CS103/auto-reclose modifications ▪ Out of step tripping	Patch for V2.12 V2.13 or later	P54x/EN M/J74
51	D	K	16 August 2006	Release of P543, P544, P545 & P546 with distance protection and P443 based on 51C ▪ Prevents a possible reboot 15 minutes after browsing the front courier port but not making a setting change i.e. browsing using PAS&T ▪ Extended GOOSE enrolment capability ▪ Correction to ICD files, Enumeration (value) and fixed data mapping	Patch for V2.12 V2.13 or later	P54x/EN M/J74
51	E	K	14 November 2006	Release of P543, P544, P545 & P546 with distance protection and P443 based on 51D ▪ Prevent a reboot in 61850 builds when NIC link is inactive and avalanche of DDB activity ▪ Correctly report a fatal error generated by the sampling call-back ▪ Correct the operation of the GOOSE messaging and a problem with the download of an IED configuration file ▪ Correct the operation of the check sync ▪ Correct the operation of the overcurrent reset curves ▪ Removed check on the14th position of model number ▪ Fixed Telegrams for public inf. 64-67	Patch for V2.12 V2.13 or later	P54x/EN M/J74
51	F	K	15 May 2007	Release of P543, P544, P545, P546 and P443 non 61850 builds with distance protection based on 51E ▪ Prevent a fatal error from an incorrect DNP3.0 address in not using DNP3.0 evolutions platform ▪ Default setting for 450B 'I< Current Set' reduced to 50mA ▪ French Translations for DDBs 1368-1371 corrected ▪ Dependencies for cells 3242 & 3245 corrected ▪ Fun & INF values related to CS103 Command Blocking corrected ▪ Angle for negative sequence phase overcurrent setting corrected ▪ Corrected operation when using MiCOM S1 is used to activate settings group by right clicking on the group ▪ Corrected the latching of Function Key DDB signals on relay power up ▪ Corrected disturbance recorder scaling to prevent high current levels into 5A CT causing the Disturbance Recorder to saturate ▪ Restring defaults appears not to change the 1/5A CT selection ▪ Corrected the performance of the IM^{64} direct mode ▪ CB control via direct access does not work with 2CB versions of P540D ▪ Auto-reclose dead time/close cycle continues even if AR switched out of service	Patch for V2.12 V2.13 or later	P54x/EN M/J74

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
51	F	K	15 May 2007	▪ Distance setting are not updated in simple setting mode in setting groups other than the active one ▪ Ch2 Statistics may not be displayed	Patch for V2.12 V2.13 or later	P54x/EN M/J74
51	G	K	-	Release of P543, P544, P545, P546 and P443 non 61850 builds with distance protection based on 51F was approved for release but withdrawn before release ▪ Corrections to enable/disable of auto-reclose	Patch for V2.12	P54x/EN M/J74
51	H	K	4 July 2007	Release of P543, P544, P545, P546 and P443 non 61850 builds with distance protection based on 51G ▪ Corrected power swing detection when both distance and current differential enabled ▪ Corrections to enable/disable of auto-reclose	Patch for V2.12	P54x/EN M/J74
51	I	K	14 January 2010	Release of P543, P544, P545, P546 and P443 non 61850 builds with distance protection based on 51H ▪ Prevented the differential protection inhibiting in three terminal schemes when GPS is enabled and loopback mode selected (N/A P44y) ▪ Improvements to the GPS code (N/A P44y) ▪ Improvements in the clock recover circuits used by the Differential Comms. (N/A P44y) ▪ Correction to P543/P545 compatibility when used in transformer compensation mode ▪ Correction to the way latched LED/Relays are cleared ▪ Corrections to the Current Differential Inhibit when the GPS synchronization is disabled (N/A P44y) ▪ Correction to the distance cross polarizing when the memory expires ▪ Corrections to menu text ▪ Correction to auto-reclose operation for switch on to fault condition ▪ Fix for DEF reverse operation ▪ Corrected some French and German text ▪ Prevented CB Operating Time displaying 4.295Ms ▪ Fix to Blocking scheme ▪ Fixed Inhibit CB Fail Protection in P544/6 ▪ Improved co-processor error reporting ▪ Fixed a SOTF problem	Patch for V2.12	P54x/EN M/J74

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
51	J	K	5 October 2010	Release of P543, P544, P545, P546 and P443 non 61850 builds with distance protection based on 51I ▪ Fixed a problem with the co-processor stack check which could cause a re-boot ▪ Enhanced the OST feature to make it more stable when currents are low ▪ Improved the distance performance for 2ph-g and also cross country faults	Patch for V2.12	P54x/EN M/J74
52	A	K	-	Release of P543, P544, P545 & P546 with distance protection and P443 based on SW 51E ▪ Chinese interface ▪ Replacing the existing DNP3.0 with the DNP3.0 evolutions ▪ Addition of a current but no volts trip option to Switch on to Fault and Trip on Reclose feature (SOTF/TOR) ▪ Replacement of existing negative sequence overcurrent with multi-stage (2 IDMT + 2 DT) negative sequence overcurrent ▪ Addition of IDG curve, commonly used in Sweden, to Earth Fault & Sensitive Earth Fault (involves moving settings) ▪ Reduction of all TMS step sizes to 0.005 ▪ Addition of channel propagation delay statistics and alarms (N/A P44y) ▪ Changes to CTS so both techniques can be selected together (N/A P44y) ▪ Regrouping of CTS settings ▪ Addition of four stages of under frequency protection and two stages of overfrequency protection ▪ Addition of df/dt protection ▪ Changes to under and overvoltage to enable each stage to be independently set ▪ Extensions to the Check Sync VT position setting ▪ Replacing fixed Trip on Close (TOC) Delay with a setting ▪ Improvements to slow power swing detection ▪ Changes to distance count strategy to restore the same operating time when phase differential protection is enabled ▪ Changes to Permissive Inter Trip (PIT) logic to enable the user to select either local or remote current to be used (N/A P44y) ▪ Includes local time zone settings for date & time ▪ Addition of flexible settings for distance quadrilateral top line ▪ Reduced minimum setting for IN> I2pol Set ▪ Addition of propagation delay times to Fault Record ▪ Default setting for 450B 'I< Current Set' reduced to 50mA ▪ Enhancement to self-checking of output relays ▪ Change tunnelled courier address to follow the 1st Rear Port's KBUS or CS103 address	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
52	B	K	4 July 2007	Release of P543, P544, P545 & P546 with distance protection, P547 and P443 based on 52A ▪ Phase comparison protection P547 added to range ▪ Improvements to VTS ▪ Improvements to slow power swing detection ▪ Corrected power swing detecting when both distance and current differential enabled (N/A P44y) ▪ Corrections to enable/disable of auto-reclose ▪ Resolved a problem relating to CT Ratio's not being restored when restoring default settings ▪ Resolved a problem with the Disturbance Recorder which saturates for high current levels into 5A CT	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
52	C	K	31 July 2007	Release of P543, P544, P545 & P546 with distance protection, P547 and P443 based on 52B ▪ Tilt angle of ground quadrilateral characteristic corrected ▪ Minor correction to fault record ▪ Corrections to over voltage stage 2 inhibit	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
52	D	K	17 December 2007	Release of P543, P544, P545 & P546 with distance protection, P547 and P443 based on 52C ▪ Fixed a number of 61850/Goose problems ▪ Fixed a problem in P547 related to the transient starters ▪ Fixed the max prop alarm (N/A P44y) ▪ Corrected some DDB German text ▪ Fixed a problem with weak infeed inhibit ▪ Fixed a SOTF problem when there is a short duration pre-fault ▪ Fixed a primary scaling issue relating to Zone 5 & 6	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
52	E	K	14 May 2008	Release of P543, P544, P545 & P546 with distance protection, P547 and P443 based on 52D ▪ Fixed a number of 61850 problems ▪ Improved co-processor error reporting ▪ Fix to Blocking scheme ▪ Fixed Inhibit CB Fail Protection in P544 and P546	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
52	F	K	-	Release of P543, P544, P545 & P546 with distance protection and P443 based on 52E ▪ Correction to auto-reclose operation for switch on to fault condition ▪ Prevented CB Operating Time displaying 4.295Ms ▪ Bug fixes	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
52	G	K	28 October 2008	Release of P543, P544, P545 & P546 with distance protection, P547 and P443 based on 52F ▪ Correction to the distance cross polarizing when the memory expires	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
52	H	K	21 September 2009	Release of P543, P544, P545 & P546 with distance protection, P547 and P443 based on 52G ▪ Corrected some menu translations ▪ Corrected Breaker Fail - WI Aided1 trips so they can be disabled via setting "WI Prot Reset" ▪ Timestamp in fault record adjusted for the local time setting ▪ Corrections to the Current Differential Inhibit when the GPS synchronization is disabled ▪ Corrected Thermal State measurement via DNP3.0 ▪ Correction to the way latched LED/Relays are cleared ▪ Correction to negative sequence overcurrent settings when 5A input used ▪ Correction to P545/P541 compatibility when used in transformer compensation mode ▪ Improvements to the GPS code ▪ Prevented CTS generating events when CTS is disabled ▪ Prevent Z5 from setting slow swing when PSB is disabled ▪ Resolved problem in P543/P545 which prevent correct reporting of fault record over 61850 ▪ Fixed problem which prevented residual overvoltage from initiating CB Fail ▪ Various improvements to DNP3.0, CS103 & IEC 61850 protocols ▪ Bug fixes	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
52	I	K	6 December 2010	Release of P543, P544, P545 & P546 with distance protection and P443 based on 52H ▪ Time stamping and status of IEC 61850 data attribute sofPSOF1.ST.general.Op improved ▪ Fixed a 61850 issue which blocked clients when one was disconnected ▪ Enhanced the OST feature to make it more stable when currents are low ▪ Improved the distance performance for cross country faults ▪ Rebranded as Alstom. Minor change to software number plus changes to 61850 (New ICD files required) ▪ Bug fixes	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
52	J	K	19 December 2013	Release of P543, P544, P545 & P546 with distance protection and P443 based on 52I ▪ Improvements to CB Fail reset times ▪ Several fixes to IEC 61850 problems ▪ Improved the co-processor SRAM checking ▪ Fixed an issue relating to Permissive Intertripping ▪ Improvement to disturbance recorder ▪ Corrected the OST current sensitivity ▪ Bug fixes	Patch for V2.14	P54x/EN M/J74 + Addendum P54x/EN AD/J84
52	K	K	12 September 2014	Release of P543, P544, P545 & P546 with distance protection and P443 based on 52J ▪ Current Differential communications are not stopped temporarily when navigating the default display ▪ CT Supervision can be operated in P543 52K software ▪ CB Fail trip can be operated under faults with DC transient offsets ▪ Bug fixes		
54	A	K	18 March 2008	Release of P543, P544, P545 & P546 with distance protection, P443 and P445 based on 52D ▪ Positional information added to PSL ▪ DNP3.0 Over Ethernet protocol added ▪ Extended I/O - status inputs increased from 24 to 32 ▪ Compensated overvoltage protection added ▪ IEC-103 Generic Services Measurements added ▪ Set/Reset Latch Logic Gates added to PSL ▪ Improved Sensitivity Range for DEF ▪ Fault record to include current differential currents recorded at the time of the current differential trip in addition to the existing data from 1 cycle later ▪ Fault record increased max. number of fault records to 15 ▪ GPS Alarm modifications (N/A P44y) ▪ Scheme Delta from P443 included (N/A P445) ▪ DNP3.0 enhancements for SSE ▪ Bug fixes	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
54 35 (P445)	B	K J (P445)	25 June 2008	Release of P543, P544, P545 & P546 with distance protection, P443 and P445 based on 54A ▪ Fixed a number of 61850 problems ▪ Improved co-processor error reporting	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
54 35 (P445)	B	K J (P445)	25 June 2008	▪ Fix to Blocking scheme ▪ Fix for DEF reverse operation ▪ Fixed Inhibit CB Fail Protection in P544/6 ▪ Corrected some French and German text ▪ Prevented CB Operating Time displaying 4.295Ms ▪ Fixed a problem which prevented extraction of DNP3.0 setting files from DNP3.0 over Ethernet variants ▪ Bug fixes	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
54 35 (P445)	C	K J (P445)	25 June 2008	Release of P543, P544, P545 & P546 with distance protection, P443 and P445 based on 54B ▪ Correction to auto-reclose operation for switch on to fault condition	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
54	D	K	20 January 2009	Release of P543 and P544, with distance protection and P443 based on 54C ▪ Correction to the distance cross polarizing when the memory expires ▪ Corrections to the Current Differential Inhibit when the GPS synchronization is disabled (N/A P44y) ▪ Corrected Thermal State measurement via DNP3.0 ▪ Timestamp in fault record adjusted for the local time setting ▪ Corrected Breaker Fail - WI Aided1 trips so they can be disabled via setting "WI Prot Reset"	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
54 35 (P445)	E	K J (P445)	20 March 2009	Release of P543, P544, P545 & P546 with distance protection, P443 and P445 based on 54D ▪ Prevents the loss of IEC6 1850 messages and fixed the handling of the ACD flag during GI ▪ Improved the Ethernet card boot code	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
54 35 (P445)	F	K J (P445)	21 September 2009	Release of P543, P544, P545 & P546 with distance protection, P443 and P445 based on 54E ▪ Corrected some menu translations ▪ Correction to the way latched LED/Relays are cleared ▪ Correction to negative sequence overcurrent settings when 5A input used ▪ Correction to P545/P541 compatibility when used in transformer compensation mode ▪ Improvements to the line differential GPS code (N/A P44y) ▪ Prevented CTS generating events when CTS is disabled ▪ Prevent Z5 from setting slow swing when PSB is disabled ▪ Resolved problem in P543/P545 which prevent correct reporting of fault record over 61850	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
54 35 (P445)	F	K J (P445)	21 September 2009	▪ Fixed problem which prevented residual overvoltage from initiating CB Fail ▪ Various improvements to DNP3.0, CS103 & IEC 61850 protocols ▪ Bug fixes	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
54 35 (P445)	G	K J (P445)	19 October 2010	Release of P543, P544, P545 & P546 with distance protection, P443 and P445 based on 54F ▪ Time stamping and status of IEC 61850 data attribute sofPSOF1.ST.general.Op improved ▪ Fixed a 61850 issue which blocked clients when one was disconnected ▪ Enhanced the OST feature in the models with distance protection to make it more stable when currents are low (no applicable P445) ▪ Improved the distance performance for cross country faults ▪ Improvements to fault record display over Courier and DNP3.0 ▪ Bug fixes	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
54 35 (P445)	H	K J (P445)	11 January 2011	Release of P543, P544, P545 & P546 with distance protection, P443 and P445 based on 54G ▪ Rebranded as Alstom. Minor change to software number plus changes to 61850 (New ICD files required)	Patch for V2.14 First release of Studio	P54x/EN M/J74 + Addendum P54x/EN AD/J94
55 36 (P445)	B	K J (P445)	30 March 2009	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841, based on 54D. This is a major release because in the P540D range, the P446 model was added ▪ Auto-reclose, Check Sync and CB Monitoring added to P544 & P546 ▪ Improved Ethernet card boot code ▪ Introduction of new model P446	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
55 36 (P445)	C	K J (P445)	15 May 2009	Release of P543, P544, P545 & P546 with distance protection, P547,P443,P445, P446 and P841, based on 55B ▪ Improvements to the Ethernet card start-up and configuration ▪ Correction to negative sequence overcurrent settings when 5A input used ▪ Correction to P545/P541 compatibility when used in transformer compensation mode ▪ Correction to the way latched LED/Relays are cleared ▪ Corrections to menu text ▪ Improvements to the differential GPS code ▪ Bug fixes	Patch for V2.14 Studio FTP server	P54x/EN M/KA4

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
55 36 (P445)	D	K J (P445)	28 October 2009	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on 55C ▪ Improvements to the differential GPS code (N/A P44y) ▪ Correction to slow power swing configuration for ph-ph Quads only (N/A P445) ▪ Improvements in the clock recover circuits used by the Differential Comms. ▪ Prevent Z5 from setting slow swing when PSB is disabled ▪ Bug fixes	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
55 36 (P445)	E	K J (P445)	11 January 2011	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on 55D ▪ Rebranded as Alstom. Minor change to software number plus changes to 61850 (New ICD files required)	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
55 36 (P445)	F	K J (P445)	14 June 2012	Release of P543, P544, P545 & P546 with distance protection, P443, P445, P446 and P841 based on 55E ▪ Fixed dnp3 control of CB2 (Only for models with 2 CB) ▪ Improved the distance performance for cross country faults ▪ Enhanced the OST feature to make it more stable when currents are low (N/A P445) ▪ Time stamping and status of IEC 61850 Data attribute sofPSOF1.ST.general.Op improved ▪ Improvements to Fault record display over courier and dnp3 ▪ Fixes to Autoreclose ▪ Improvements to co-processor SRAM checking ▪ Fixed PIT ▪ Several fixes to IEC 61850 problems ▪ Added Frequency trips to P445 default PSL ▪ Fixed an issue where Disturbance recorder could get out of sync	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
55	G	K	18 December 2014	Release of P545 based on 55F ▪ PX40PL-33 Error code “0x0C160013” issue ▪ Several fixes to IEC 61850 and IEC-103 problems ▪ Other Bug fixes	Patch for V2.14 Studio FTP server	P54x/EN M/KA4
57 37 (P445)	A	K J (P445)	December 2009	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on 55D ▪ IEC 61850 phase 2 and 2.1 implemented ▪ Application for in zone Transformers (2nd and 5th Harmonic Blocking/restraint) for line diff. (N/A P44y, P544 and P546)) ▪ Differential High set can be disabled when Inrush protection is enabled (N/A P44y) ▪ Restricted Earth Fault Protection (REF)	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB4

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
57 37 (P445)	A	K J (P445)	December 2009	▪ Modification to Char Mod timer functionality for line diff. (N/A P44y) ▪ Separate measurements for each set of CT's (Only for models with 2 CB's) ▪ Interrupt Driven InterMiCOM in all models ▪ Read Only Mode	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB4
57 37 (P445)	B	K J (P445)	10 February 2010	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on 57A ▪ Prevented the differential protection inhibiting in three terminal schemes when GPS is enabled and loopback mode selected (N/A P44y) ▪ Fault locator measurements in ohms corrected when 5A CT used or displayed in primary ▪ Frequency measurement in DNP3.0 fault record corrected ▪ Other bug fixes	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB4
57	C	K	5 May 2010	Release of P543 based on 57B ▪ Enhancement to GOOSE performance ▪ Fixes to 61850 ▪ Fixed protection comms. address problem in three ended schemes selected ▪ Fixed DNP3.0 control of CB2 (although models no released) ▪ Fixed a small issue with the detection of slow swings	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB4
57 37 (P445)	D	K J (P445)	15 October 2010	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on 57C (which had a very limited release for one model) ▪ Incorrect mapping of XCBR(n).CBOpCap.stVal data attribute corrected ▪ Time stamping and status of IEC 61850 Data attribute sofPSOF1.ST.general.Op improved ▪ Enhanced the OST feature to make it more stable when currents are low (N/A P445) ▪ Improved the distance performance for cross country faults ▪ Fixed the inrush restraint feature in P547 ▪ Improvements to fault record display over Courier and DNP3.0 ▪ Other bug fixes	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB4
57 37 (P445)	E	K J (P445)	11 January 2011	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on 57D ▪ Rebranded as Alstom. Minor change to software number plus changes to 61850 (New ICD files required)	Patch for V2.14 Studio FTP server	P54x/EN M/KA4 + Addendum P54x/EN AD/KB5

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
57 37 (P445)	F	K J (P445)	9 August 2012	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on 57E ▪ Improvements to CB Fail reset times ▪ Several fixes to IEC 61850 problems ▪ Improved the co-processor SRAM checking ▪ Fixed an issue relating to Permissive Intertripping (N/A P44y) ▪ Improvement to disturbance recorder ▪ Corrected the OST current sensitivity (N/A P445) ▪ Bug fixes	Studio FTP server	P54x/EN AD/Lb4 + P54x/EN M/La4
57	G	K	13 December 2012	Release of P547 with distance protection based on 57F ▪ Addition of PSL based phase selection for P547 ▪ Fixed an issue where the carrier was not muted when it should have been ▪ Bug Fixes	Studio FTP server	P54x/EN AD/Lb4 + P54x/EN M/La4
57 37 (P445)	H	K J (P445)	5 August 2015	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on 57G and 57F ▪ Correction to Error code “0x0C160013” related with the SRAM ▪ Fix an issue with P445 AutoReclose where local override by DDB was not allowed ▪ Improvement of the CB Fail operation under faults with DC transient offsets ▪ Fix a of a differential issue where the relay sometimes could reboot if working with IEE C37.94 and N=12. (N/A P44y) ▪ Other minor bug fixes	Patch for V2.14 Studio FTP server	P54x/EN AD/Lb4 + P54x/EN M/La4
57	I	K	15 July 2021	Release of P543 & P545 with distance protection and P443 based on 57H ▪ Improvement of Distance protection algorithm for Phase to Phase to ground remote faults ▪ Other minor bug fixes	Patch for V2.14 Studio FTP server	P54x/EN AD/Lb4 + P54x/EN M/La4
60	A	M	1 February 2011	Release of P546 without distance protection based on 57D ▪ Cyber Security ▪ Main processor board replaced by ZN0069 001 ▪ Final Assembly for P546 GN0364 changed to issue F ▪ New sheet 3 & 4 of Final Assembly User Interface GN0341 added	MiCOM S1 studio v3.3 or later	P54x/EN M/KA4 + P54x/EN AD/KB4
61	A	M	1 August 2011	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 47E ▪ Cyber security phase 1 ▪ Separate CT ratios for models with 2 sets of CTs ▪ Option to use 2nd Check Sync VT as a measured VT input for earth fault protection ▪ Increase the number of available protection scheme addresses from 20 to 32	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
61	A	M	1 August 2011	▪ Single End Testing operation ▪ Stub Bus logic enhancement ▪ CB Fail improvements ▪ Common auto-reclose, check sync and CB status for P540D products ▪ Check sync stage 2 enhancements ▪ Inhibit SEF feature added ▪ Enhanced disturbance recorder ▪ Increase in number of event records ▪ Increase PSL timers to 32 ▪ User Programmable Curves feature added ▪ Improvements to GOOSE performance ▪ IEC 870-5-103 fault location added to ASDU4 ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
61	B	M	9 August 2012	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 61 A ▪ Fix to the alternative basic scheme to cover changing faults ▪ Several fixes to IEC 61850 problems ▪ Fixed an issue relating to restoring user curves ▪ Improved the co-processor SRAM checking ▪ Optimized the start-up of 61850 models ▪ Fixed an issue relating to Permissive Intertripping ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M
61	C	M	12 September 2012	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 61 B ▪ Fixed several IEC 61850 problems ▪ Corrected the password required to clear alarms ▪ Fixed a DR problem ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
61	D	M	24 September 2013	Release of P543, P544, P545 & P546 with distance protection and P841-A based on SW 1 B ▪ Improved MMI response when events are being generated ▪ Fixed an evolving fault issue in the Auto-reclose Logic ▪ Fixed a number of IEC 61850 issues ▪ Fixed a number of DNP3.0 issues	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
61	D	M	24 September 2013	▪ Resolved a setting change issue which caused the co-processor to reconfigure un-necessarily ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
61	F	M	20 January 2015	Release of P543, P544, P545 & P546 without distance protection and P841-A. This software is based on 61D software which is the last full release but also incorporating the P446 71E changes ▪ P540D Goose/Bandwidth Code Optimisation ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
61	G	M	28 August 2015	Release P545 without distance protection. This release is mainly to solve a mal operation of current differential protection when CIT<->NCIT mixed mode scheme. Is based on SW 71F ▪ Fixed several bugs related to IEC 61850 issues ▪ Fixed a SNTP configuration performance ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
61	I	M	17 January 2017	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P446 and P841-B. The main reason for this release is to include the changes that were made /fixed in version G ▪ Code optimisation ▪ Changes to CB fail function to include External DDB reset inputs ▪ Fixed several bugs related to IEC 61850 issues ▪ Fixed bug related to measurements ▪ Fixed bug: CS1 and CS2 do not work independently when CB Comp enabled for CS2 ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
61	J	M	21 December 2017	Release of P546 without distance protection, based on software version P540D 61/71I. **This version was released only for one particular customer**	MiCOM S1 Agile v1.3 or later	
61	K	M	28 February 2018	Release of P546 without distance protection, based on software version P540D 61/7J. **This version was released only for one particular customer**, to include the threshold for the undercurrent of pole dead as fix threshold of 5%In	MiCOM S1 Agile v1.3	
63	A	M	4 September 2012	Release of P543 & P545 High Break versions without distance protection based on 61B or 71B ▪ Sub Cycle Differential Protection ▪ Note: This version is not compatible with any other P540	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M + P543&5/EN RN/A

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
65	A	M	14 January 2013	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 61C ▪ CB Fail enhancements ▪ 2nd Harmonic Blocking Based on SEF Input ▪ Addition of Polish, Italian and Portuguese languages ▪ Addition of Checksync Voltage Diff Measurement ▪ Improvements to GOOSE ▪ Ethernet Failover ▪ SNTP Alarm ▪ Minimum setting value of CheckSync UV [48 8B] changed to 10V ▪ Fixed several bugs related to IEC 61850 issues ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
65	B	M	21 March 2013	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 65A ▪ Improved MMI response when events are being generated ▪ Fixed reporting of power swing blocking over IEC 61850 ▪ Fixed an evolving fault issue in the Auto-reclose Logic ▪ Fixed a number of IEC 61850 issues ▪ Fixed a number of DNP3.0 issues ▪ Fixed an issue with the Delta Direction count state ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
65	C	M	5 December 2013	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 65B ▪ Resolved a setting change issue which caused the co-processor to reconfigure un-necessarily ▪ Additional English/Italian/Polish/Portuguese language option (7) ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
65	D	M	9 December 2013	Release of P546 without distance protection based on SW 65C with only IEC 61850 protocol. **This version was released only for one customer**	MiCOM S1 Agile v1.3 or later	
66	A	M	5 December 2013	Release of P543, P544, P545 & P546 without distance protection an P841-A, based on SW 65B including all bug fixes of SW 75C ▪ Addition of starters to Current Differential protection ▪ Addition of Current Differential Supervision ▪ Additional English/Italian/Polish/Portuguese language option (7) ▪ Correction of stamping issues involving 61850	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
66	A	M	5 December 2013	▪ Fixed the CB open echo feature in POR scheme for 2 CB ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
66	B	M	9 May 2014	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 66 A ▪ Code optimisation ▪ Improved CB fail algorithm to avoid incorrect operation under faults with DC transient offsets ▪ Fixed bug: Frequent changes in data causes IEC 61850 application to stop ▪ Fixed bug: Vn Measured is not measured following a power cycle of relay ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
66	C	M	22 January 2015	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 66 B ▪ Goose/Bandwidth Code Optimisation. ▪ Fixed bugs related to IEC 61850 and IEC103 protocols ▪ Fixed bug that occurs when using a Dual Redundant IEE C37.94 Differential Scheme with N=12: if one leg of the communications path was broken, the relay could reboot ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
66	D	M	12 February 2015	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 66 C ▪ Fixed an issue with IEC 61850 models: Digital Inputs, Virtual Inputs and PSL validity could be recognised at a different time	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
66	G	M	24 January 2017	Release of P546 without distance protection based on 76E ▪ Fixed a number of IEC 61850 issues ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
66	H	M	15 February 2017	Release of P546 without distance protection based on 66F ▪ Fixed bug: Current of phase A is not the sum of currents in CT1 and CT2 in the corresponding phase ▪ Fixed bug: CS1 and CS2 do not work independently when CB Comp enabled for CS2 ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
66	I	M	31 March 2017	Release of P543, P544, P545 & P546 without distance protection and P841-A. This release includes all bug fixes of SW 66G and SW 66H	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
66	J	M	12 January 2017	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 76I. This release is to include 3 new options (R, S, T) in the CORTEC related to the IRIG B as follows: ▪ R - Redundant Ethernet PRP/HSR/RSTP, 2 multi-mode fibre ports + Modulated/ Un-Modulated IRIG-B ▪ S - Redundant Ethernet PRP/HSR/RSTP, 2 coper ports RJ45 + Modulated/Un-Modulated IRIG-B ▪ T - Single Ethernet, 1 multi-mode fibre ports + Modulated/Un-Modulated IRIG-B This release is not a general release but for particular customers	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
66	K	M	21 December 2017	Release of P546 without distance and for only one model: IEC 61850 + 103 based on 66J Particular customer ▪ Fixed bug: Reboot of IEDs after Maintenance Records	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
66	L	M	29 March 2018	Release of P546 without distance protection based on 66K ▪ Threshold for the undercurrent of pole dead as fix threshold of 5%In ▪ Minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
69	A	M	25 May 2018	Release of P543, P544, P545, P546 without distance protection, and P841-A based on based on 66I ▪ Additional Comms mode added to allow 128 kBPS comms ▪ In models with current differential, additional IM64 option can be selected between 8 or 32 'IM64' bits per channel ▪ In models with distance , additional IM64 option can be selected between 8 or 24 'IM64' bits per channel ▪ Settable hysteresis for overvoltage ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&51Z-EN-TM-N P543&51NZ-EN-TM-N P544&61Z-EN-TM-N P544&61NZ-EN-TM-N
69	C	M	27 September 2018	Release of P543, P544, P545, P546 without distance protection, and P841-A based on 69B (Interim SW not released to production) ▪ Fixed bugs related to IEC 61850		

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
69	D	M	8 January 2019	Release of P543, P544, P545 & P546 without distance protection and P841-A based on SW 79C ▪ Threshold for undercurrent of pole dead changed has been fixed to 5% ▪ Fixed bugs related to IEC 61850	MiCOM S1 Agile v1.3 or later	
71 41 (P445)	A	M P (P445)	1 August 2011	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 57E ▪ Cyber security phase 1 ▪ Separate CT ratios (Only for models with 2 set of CT's) ▪ Option to use 2nd Check Sync VT as a measured VT input for earth fault protection (Only for models with 2 VT's) ▪ Neutral Differential Protection Element (N/A P44y) ▪ Phase Differential Transient Bias (N/A P44y) ▪ Increase the number of available protection scheme addresses from 20 to 32 (N/A P44y) ▪ Single End Testing operation (N/A P44y) ▪ Improvements to distance protection ▪ DEF Virtual Current Polarizing option ▪ OST/PSB improvements (N/A P445) ▪ Stub Bus line diff logic enhancement (N/A P44y) ▪ CB Fail improvements ▪ Common auto-reclose, check sync and CB status for P540D Products ▪ Check sync stage 2 enhancements ▪ Inhibit SEF feature added ▪ Enhanced disturbance recorder ▪ Increase in number of event records ▪ Increase PSL timers to 32 ▪ User Programmable Curves feature added ▪ Improvements to GOOSE performance ▪ IEC 870-5-103 fault location added to ASDU4 ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
71 41 (P445)	B	M P (P445)	9 August 2012	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 71 A ▪ Fix to the alternative basic scheme to cover changing faults ▪ Several fixes to IEC 61850 problems ▪ Fixed an issue relating to restoring user curves ▪ Improved the co-processor SRAM checking	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
71 41 (P445)	B	M P (P445)	9 August 2012	▪ Optimized the start-up of 61850 models ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
71 41 (P445)	C	M P (P445)	12 September 2012	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 71 B ▪ Corrected language translations for some distance settings ▪ Fixed several IEC 61850 problems ▪ Corrected the password required to clear alarms ▪ Fixed a DR problem ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
71 41 (P445)	D	M P (P445)	24 September 2013	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 71 C ▪ Improved MMI response when events are being generated ▪ Fixed reporting of power swing blocking over IEC 61850 ▪ Fixed an evolving fault issue in the Auto-reclose Logic ▪ Fixed a number of IEC 61850 issues ▪ Fixed a number of DNP3.0 issues ▪ Fixed an issue with the Delta Direction count strategy ▪ Resolved a setting change issue which caused the co-processor to reconfigure un-necessarily ▪ Fixed the CB open echo feature in POR scheme (Only for models with 2 CB's) ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
71	E	M	9 December 2013	Release of P446 based on SW 71 D ▪ Fixed bug related to the Vn measurement ▪ Fixed other minor bug related to df/dt function	MiCOM S1 Agile v1.3 or later	
71 41 (P445)	F	M P (P445)	20 January 2015	Release of P543, P544, P545 & P546 with distance protection, P547,P443, P445, P446 and P841. This software is based on 71D and 61D software but also incorporating the P446 71E changes ▪ Goose/Bandwidth Code Optimisation ▪ Bug fixes related to IEC 61850 ▪ Fix bug: CB Control Interlocking Fail ▪ Fixed bug: When using a Dual Redundant IEE C37.94 Differential Scheme with N=12, if one leg of the communications path is broken the relay can reboot (N/A P44y) ▪ Fix other minor bugs	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
71	G	M	28 August 2015	Release P545 with distance protection. This release is mainly to solve the mal operation of current differential protection when CIT<->NCIT mixed mode scheme. Is based on SW 71F ▪ P540 NCIT and CIT combination trips for some external fault ▪ Fixed an issue with IEC 61850 models: Digital Inputs, Virtual Inputs and PSL validity could be recognised at a different time ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
71	H	M	14 October 2015	Release of P545 with distance protection and P443 based on 71G ▪ Fix bug when reporting of complex data points (ACD/ACT) on IEC 61850 ▪ Fix other minor issues related to IEC 61850 and 103 protocols	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
71 41 (P445)	I	M P (P445)	17 January 2017	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 71F and including the changes that were made/fixed in versions 71G and 71H	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M
71	J	M	21 December 2017	Release of P546 with distance protection, based on software version P540D 61/71I. **This version was released only for one particular customer**	MiCOM S1 Agile v1.3 or later	
71	K	M	28 February 2018	Release of P546 with distance protection, based on software version P540D 61/7J. **This version was released only for one particular customer**, to include the threshold for the undercurrent of pole dead as fix threshold of 5%In	MiCOM S1 Agile v1.3	
71	L	M	22 October 2020	Release of P443 distance protection, based on software version P540D 61/71K. **This version was released only for one particular customer**	MiCOM S1 Agile v1.3	
71	M	M	16 August 2023	Release of P545 with distance protection and P443 Distance protection, based on software version P540D 61/71I. **This version was released only for one particular customer**, to improve the phase selection	MiCOM S1 Agile v1.3	
72	A	M	29 June 2012	Release of P546 with distance protection, P446 and P841-B based on SW 70A ▪ Support of 9-2 LE ▪ GOOSE performance improvement ▪ Replace of analogue CT/VT board with 9-2LE board ▪ Update the 80TE case for 9-2 relay ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P54x/EN AD/Lb4 + P54x/EN M/La4 Px4x_92LE-TM-EN-002
72	B	M	13 July 2012	Release of P546 with distance protection, P446 and P841-B based on SW 72A ▪ NCIT version of P546 sometimes reboots with error code 0xE0050004 following a setting change ▪ Use ASE2000 send 'Device Attribute' command to P546 DNP3 builds, relay reboot. ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	- P54x/EN AD/Lb4 + P54x/EN M/La4 Px4x_92LE-TM-EN-002

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
74	B	M	24 January 2013	Release of P546 with distance protection, P446 and P841-B based on 72B ▪ VT selection ▪ Addition of Checksync Voltage Diff Measurement ▪ Improvements to GOOSE ▪ Ethernet Failover ▪ SNTP Alarm ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P54x/EN AD/Lb4 + P54x/EN M/La4 Px4x_92LE-TM-EN-002
74	C	M	24 June 2014	Release of P546 with distance protection, P446 and P841-B based on 74B ▪ All protection functions are not blocked for IEC 61850-9.2LE IEDs if the secondary current exceeds 64A ▪ Current Differential communications are not stopped temporarily when navigating the default display ▪ Goose/Bandwidth Code Optimisation ▪ CB Fail trip can be operated under faults with DC transient offsets ▪ IEC 61850 Application is not stopped when frequent changes in data are caused ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P54x/EN AD/Lb4 + P54x/EN M/La4 Px4x_92LE-TM-EN-002
74	D	M	29 September 2016	Release of P546 with distance protection based on 74C ▪ Fixed a number of IEC 61850 issues ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P54x/EN AD/Lb4 + P54x/EN M/La4 Px4x_92LE-TM-EN-002
75 45 (P445)	A	M P (P445)	14 January 2013	Release of P543, P544, P545 & P546 with distance protection, P443, P445, P446 and P841 based on SW 71C ▪ CB Fail enhancements ▪ 2nd Harmonic Blocking Based on SEF Input ▪ Addition of Polish, Italian and Portuguese languages ▪ Addition of Checksync Voltage Diff Measurement ▪ Improvements to GOOSE ▪ Ethernet Failover ▪ SNTP Alarm ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-00
75 45 (P445)	B	M P (P445)	21 March 2013	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 75A ▪ Improved MMI response when events are being generated ▪ Fixed reporting of power swing blocking over IEC 61850 ▪ Fixed an evolving fault issue in the Auto-reclose Logic ▪ Fixed a number of IEC 61850 issues	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
75 45 (P445)	B	M P (P445)	21 March 2013	▪ Fixed a number of DNP3.0 issues ▪ Fixed an issue with the Delta Direction count state ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
75 45 (P445)	C	M P (P445)	5 December 2013	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 75B ▪ Resolved a setting change issue which caused the co-processor to reconfigure un-necessarily ▪ Additional English/Italian/Polish/Portuguese language option (7) ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
75	D	M	9 December 2013	Release of P546 with distance protection based on SW 65C with only IEC 61850 protocol. **This version was released only for one particular customer**	MiCOM S1 Agile v1.3 or later	
76	A	M	5 December 2013	Release of P543, P544, P545 & P546 with distance protection based on 75C ▪ Addition of starters to Current Differential protection ▪ Addition of Current Differential Supervision ▪ Additional English/Italian/Polish/Portuguese language option (7) ▪ Correction of stamping issues involving 61850 ▪ Fixed the CB open echo feature in POR scheme (Only for models with 2 CB's) ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
76 46 (P445)	B	M P (P445)	9 May 2014	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 76 A ▪ Code optimisation ▪ Improved CB fail algorithm to avoid incorrect operation under faults with DC transient offsets ▪ Fixed bug: Frequent changes in data causes IEC 61850 application to stop ▪ Fixed bug: Vn Measured is not measured following a power cycle of relay ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
76 46 (P445)	C	M P (P445)	22 January 2015	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 76 B ▪ Goose/Bandwidth Code Optimisation ▪ Fixed bugs related to and IEC103 protocols ▪ Fixed bug that occurs when using a Dual Redundant IEE C37.94 Differential Scheme with N=12 : if one leg of the communications path was broken, the relay could reboot (N/A P44y) ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
76 46 (P445)	D	M P (P445)	12 February 2015	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841 based on SW 76 B ▪ Fixed an issue with IEC 61850 models: Digital Inputs, Virtual Inputs and PSL validity could be recognised at a different time	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
76	E	M	12 October 2015	Release of P443 based on SW 76 D ▪ Fixed an issue related to P443 InterMiCOM	MiCOM S1 Agile v1.3 or later	
76	F	M	24 August 2016	Release of P546 only for model P54681KA6N0760M based on SW 76 D ▪ Fixed bug: Periodic loss of GOOSE subscription	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
76	G	M	24 January 2017	Release of P546 with distance protection based on 76E ▪ Fixed a number of IEC 61850 issues ▪ Fixed bug: For Power swing, the relay is not using angle " Alpha cell 3D.49 " of Power Swing settings but angle " Blinder angle cell 3D.2C " of Out of Step setting ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
76	H	M	15 February 2017	Release of P546 with distance protection based on 76F ▪ Fixed bug: Current of phase A is not the sum of currents in CT1 and CT2 in the corresponding phase ▪ Fixed bug: CS1 and CS2 do not work independently when CB Comp enabled for CS2 ▪ Other minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
76 46 (P445)	I	M P (P445)	31 March 2017	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841. This release includes all bug fixes of SW 76G and SW 76H	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
76 46 (P445)	J	M P (P445)	12 January 2017	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P446 and P841-B based on SW 76 I. This release is to include 3 new options (R,S,T) in the CORTEC related to the IRIG B as follows: ▪ R - Redundant Ethernet PRP/HSR/RSTP, 2 multi-mode fibre ports + Modulated/ Un-Modulated IRIG-B ▪ S - Redundant Ethernet PRP/HSR/RSTP, 2 coper ports RJ45 + Modulated/ Un-Modulated IRIG-B ▪ T - Single Ethernet, 1 multi-mode fibre ports + Modulated/Un-Modulated IRIG-B **This release is a restricted release for particular customers**	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
76	K	M	21 December 2017	Release of P546 with distance and for only one model: IEC 61850 + 103 based on 76J for a Particular customer ▪ Fixed bug: Reboot of IEDs after Maintenance Records	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
76	L	M	29 March 2018	Release of P546 with distance protection based on 76K ▪ Threshold for the undercurrent of pole dead as fix threshold of 5%In ▪ Minor bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
76	M	M	10 August 2018	Release of P544 with distance protection for all communication protocols and P546 IEC 61850 models. SW based on 76L. SW strictly limited to some users ▪ Some bug fixes related to IEC 61850 and DNP	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
			28 March 2019	Release of P543, P544, P545 & P546 with distance protection P443, P446 and P841-B based on SW 76L. Include all the protocols ▪ Some bug fixes related to IEC 61850 and DNP		
76	P	M	10 August 2018	Release of P544 with distance protection for all communication protocols and P546 IEC 61850 models. SW based on 76L Some bug fixes related to IEC 61850 and DNP	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P544&6/EN M/M + P540D-RNC1-TM-EN-001
			15 July 2021	Release of P443 for all communication protocols and P546 IEC 61850 models. SW based on 76L Some bug fixes related to IEC 61850 and DNP		
77	A	M	2 December 2015	Release of P546 with distance protection and P446 based on 76E ▪ Add new function for IRIG-B local time ▪ The IM input CT can be used as IN measured for earth fault function (residual E/F) ▪ The IM input CT can be used as IN measured for Aided DEF function ▪ Updated set range of stage2 of earth fault in case of DT ▪ Measured IN always include the IEC 61850, CS103 and DNP protocols	MiCOM S1 Agile v1.3 or later	P54x2-TM-EN-1
78	A	M	16 April 2015	Release of P443 based on 77A ▪ Added a new distance zone Q ▪ Delink of power swing and DeltaZ ▪ Modify RAW comparator for the isolated or compensated earthing system ▪ Added option of Measure the residual voltage through the check sync input channel		

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
78	A	M	16 April 2015	▪ Added new indication for all elapsed timers of distance zones ▪ Minor bug fixes		
78	B	M	22 May 2015	Release of P443 based on 78A ▪ Minor bug fixes		
79 49 (P445)	A	M P (P445)	25 May 2018	Release of P543, P544, P545 & P546 with distance protection, P547, P443,P445, P446 and P841 based on 76I ▪ Additional Comms mode added to allow 128 kBPS comms ▪ In models with current differential or the relay working with differential function enabled, additional IM64 option can be selected between 8 or 32 'IM64' bits per channel. (N/A P44y) ▪ In models with distance, or the relay NO working in differential mode, additional IM64 option can be selected between 8 or 24 'IM64' bits per channel ▪ Settable hysteresis for overvoltage ▪ Other minor bug fixes **THIS VERSION REQUIRES SPECIAL SOFTWARE TO BE INSTALLED IN THE RELAY (FPGA)**	MiCOM S1 Agile v1.3 or later	P543&51Z-EN-TM-N P543&51NZ-EN-TM-N P544&61Z-EN-TM-N P544&61NZ-EN-TM-N
79 49 (P445)	C	M P (P445)	27 September 2018	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445, P446 and P841-B based on 79B (Interim SW which was not released to production) ▪ Fixed bugs related to IEC 61850 **THIS VERSION REQUIRES SPECIAL SOFTWARE TO BE INSTALLED IN THE RELAY (FPGA)**	MiCOM S1 Agile v1.3 or later	
79 49 (P445)	D	M P (P445)	6 December 2018 for P543 and P545 8 January 2019 for P544, P546, P547, P443,P445, P446 and P841	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P446 and P841-B based on SW 79C ▪ Threshold for undercurrent of pole dead changed has been fixed to 5% ▪ Bug fixes **THIS VERSION REQUIRES SPECIAL SOFTWARE TO BE INSTALLED IN THE RELAY (FPGA)**	MiCOM S1 Agile v1.3 or later	
79 49 (P445)	E	M P (P445)	7 May 2020	Release of P543, P545,P544 & P546 with distance protection, P445 and P446 based on SW 79D ▪ Fixed bugs related to the platform ▪ Distance IM64 propagation delay measurement error fixed ▪ Improvements to Current diff starters. (N/A P44y) **THIS VERSION REQUIRES SPECIAL SOFTWARE TO BE INSTALLED IN THE RELAY (FPGA)**	MiCOM S1 Agile v1.3 or later	

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
79 49 (P445)	F	M P (P445)	21 August 2020	Release of P543, P544, P545 & P546 with distance protection, P547, P443, P445 and P446 and P841-B based on SW 79E ▪ Added setting VTS V> Under SUPERVISION. This was a fixed value (30 V) in previous versions ▪ Fixed a minor indication bug related the VTS **THIS VERSION REQUIRES SPECIAL SOFTWARE TO BE INSTALLED IN THE RELAY (FPGA)**	MiCOM S1 Agile v1.3 or later	
80	A	M	9 October 2014	Release of P546 with distance protection, P446 and P841B sample values relays based on 74B ▪ IEC 61850 Ed.2 platform integration ▪ Logical nodes extensions ▪ Minimum I/O boards with 40TE front panel for P540D post intelligent relay ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P40L-AD-ED2-EN
80	B	M	19 December 2014	Release of P546 with distance protection, P446 and P841B sample values relays based on 80A ▪ IEC 61850 Ed.2 platform integration ▪ Logical nodes extensions, Editable Logic Nodes ▪ Minimum I/O boards with 40TE front panel for P540D post intelligent relay ▪ FAST GOOSE Solution ▪ Bug fixes	MiCOM S1 Agile v1.3 or later	P40L-AD-ED2-EN
80	C	M	28 August 2015	Release of P546 with distance protection, P446 and P841B sample values relays based on 80B ▪ Fix bug: NCIT and CIT combination trips for external fault. ▪ Fix bugs when using IEC 61850 models, Digital Inputs, Virtual Inputs and PSL validity are recognised at different times ▪ Some other bugs related to IEC 61850	MiCOM S1 Agile v1.3 or later	P40L-AD-ED2-EN
82	A	M	24 September 2015	Release of P543, P544, P545 & P546 with distance protection P443, P446 and P841-B based on SW 76B ▪ IEC 61850 Ed.2 platform integration ▪ Logical nodes extensions ▪ FAST GOOSE Solution ▪ Other bug fixes	MiCOM S1 Agile v1.3 or later	P54x1Z TM EN
82	C	M	26 November 2020	Release of P546 with distance protection P443, P446 and P841-B based on SW 82A ▪ Interim release not for wide distribution. ▪ Support software for new Ethernet board ▪ Other bug fixes	MiCOM S1 Agile v1.3 or later	P54x1Z TM EN

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
82	D	M	04 March 2021	Release of P543, P544, P545 & P546 with distance protection P443, P446 and P841-B based on SW 82C ▪ The IM input CT can be used as IN measured for earth fault function (residual E/F) ▪ The IM input CT can be used as IN measured for Aided DEF function. ▪ Other bug fixes	MiCOM S1 Agile v1.3 or later	P54x1Z TM EN
83	A	M	13 March 2015	Release of P543 & P545 without distance protection based on 63A . This is the relay with Sub Cycle Differential Protection ▪ IEC 61850 Ed.2 platform integration ▪ Logical nodes extensions, Editable Logic Nodes ▪ GOOSE Bandwidth Optimisation ▪ FAST GOOSE Solution ▪ Other Bug fixes	MiCOM S1 Agile v1.3 or later	P543&5/EN M/M P543&5/EN RN/A
84	A	M	28 June 2016	Release of P546 with distance protection and only IEC 61850 plus 103 protocol based on 82A ▪ Allow control inputs to be set as enabled/disabled in the setting file ▪ New DDB's inputs to be able to reset CB failure externally ▪ Other bug fixes	MiCOM S1 Agile v1.3 or later	P544&6/EN M
84	B	M	31 August 2016	Release of P546 with distance protection and only IEC 61850 plus103 protocol based on 84A ▪ Check sync options improvement allowing possible check sync between busbars ▪ Scheme Logic Column visible in setting file when Distance & DEF disabled	MiCOM S1 Agile v1.3 or later	P544&6/EN M
85	A	M	19 January 2017	Release of P543 & P545 with distance protection and P443, based on SW 82 A ▪ Add a new distance zone Q ▪ Delink Delta I power swing and slow power swing ▪ Include option to use distance relays with phase preference logic for isolated compensated system ▪ Measure the residual voltage through the check sync input channel ▪ Add new indication for all elapsed timers of distance zones ▪ Add Transient Ground Fault (TGFD) ▪ Rebranded to GE ▪ Other bug fixes	MiCOM S1 Agile v1.3 or later	P54x1-TM-EN-1 P54x2-TM-EN-1
86	A	M	12 January 2018	Release of sample values relays P5469CNA6R0860P and P8419CNC6R0860P only based on SW 80C ▪ Auto reclose reclaim time extended logic ▪ Auto reclose new DDB's signals for dead time is complete & enable and CB in service	MiCOM S1 Agile v1.3 or later	P546SV-TM-EN-1

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
86	A	M	12 January 2018	▪ New system split function ▪ Addition of differential starters and differential supervision ▪ Self-reset alarms have been increased from 4 to 8 and manual reset alarms have been increased from 4 to 20 ▪ Main VT location control for use with check synchronism and auto recloser ▪ Other bug fixes	MiCOM S1 Agile v1.3 or later	P546SV-TM-EN-1
86	B	M	27 February 2018	Release of sample values relays P5469CNA6R0860P and P8419CNC6R0860P only based on SW 86A ▪ System split function new DDB's for CB1 & CB2 SS to enable SS from PSL besides setting	MiCOM S1 Agile v1.3 or later	P546SV-TM-EN-1
86	E	M	5 July 2018	Release of P546 with distance protection, P446 and P841B sample values relays based on 86B ▪ Support for new Ethernet board (ZN0087) ▪ Inclusion of Duplicate GOOSE feature ▪ IRIG-B Type setting ▪ Rebranded SW to GE ▪ Other bug fixes	MiCOM S1 Agile v1.4 or later	P546SV-TM-EN-1
87	A	M	7 September 2018	Release of P543 & P545 with distance protection and P443 based on SW 85A ▪ 6 Fully Directional Distance Zone (all zones 100% reverse reach) ▪ Distance Protection "Force No Memory" option via DDB ▪ 4 stages of Directional Power Protection (each stage configurable as under/over Power) ▪ Separate UnderCurrent setting for Pole Dead and CBFail ▪ Inclusion of Duplicate GOOSE feature ▪ IEC 61850 Modelling of Sensitive Earth fault ▪ Other bug fixes	MiCOM S1 Agile v1.4 or later	P54x1i-TM-EN-2
87	B	M	2 November 2020	Release of P543 & P545 with distance protection and P443 based on SW 87A ▪ Fix of TEFD Wrong Directional Decision for Low Residual transient Reactive Power ▪ Improvements in "P Swing Detector" indication ▪ Other bug fixes	MiCOM S1 Agile v1.4 or later	P54x1i-TM-EN-2
87	C	M	24 June 2021	Release of P543 & P545 with distance protection and P443 based on SW 87B ▪ Improvement of Distance protection algorithm for Phase to Phase to ground remote faults ▪ Other bug fixes	MiCOM S1 Agile v1.4 or later	P54x1i-TM-EN-2

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
91	D	M	21 January 2020	Release of P543 & P545 with distance protection and P443 based on SW 87A ▪ RBAC (Role Base Access Control) including: Device/Server RBAC, Syslog and Multi-client reporting ▪ IEC 61850 Ed1/Ed2 Switching ▪ In models with current differential or the relay working with differential function enabled, additional IM64 option can be selected between 8 or 32 'IM64' bits per channel. (N/A P44y) ▪ In models with distance, or the relay NO working in differential mode, additional IM64 option can be selected between 8 or 24 'IM64' bits per channel ▪ Distance zone phase and ground can be settable as offset ▪ Duplicate GOOSE ▪ Other bug fixes	MiCOM S1 Agile v2.0.1 or later	P54x1Z-TM-EN-2
92	A	M	15 November 2019	Release of P545 with distance protection and P443 based on SW 91D. This release is only for 50Hz applications ▪ Added two additional zones: Zone R and Zone S. They can be reverse, forward or offset ▪ Schemes POR, PUR and blocking for Aided Scheme 1 can now be selected to work with 1 channel per phase i.e., 3 channels or with only one channel ▪ Added three new aided Schemes using a dedicated independent zone "Aided Zone 1 extension" (Different to the existing zone 1 Extension) to keying the channel. They will be equivalent to PUR, POR and Blocking but working with an independent keying zone instead of Zone 2. They work with 1 channel per phase i.e., 3 channels or with only one channel ▪ Zone 1 Extension has two additional settings to extend independently the resistive reach: phase and ground ▪ Load Blinder can be now set independently for phase and ground loops. ▪ Echo delay setting added ▪ Other small bug fixes	MiCOM S1 Agile v2.0.1 or later	P54x1Z-TM-EN-3
92	B	M	12 June 2020	Release of P543 & P545 with distance protection and P443 based on SW 92A. This release is only for 50Hz applications ▪ CB open echo can now be enabled or disabled ▪ CB open Echo delay setting added ▪ New setting to block weak infeed trip if the pole has been dead for a settable time delay ▪ Other small bug fixes	MiCOM S1 Agile v2.0.1 or later	-

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
92	C	M	21 May 2021	Release of P543 & P545 with distance protection and P443 based on SW 92B. This release is only for 50Hz applications. SW strictly limited to some users ▪ The main update in this version is related to compliance to IEC 61850 ED2.1 ▪ Fixed bug related to DE schemes: The scheme was using Z2 instead of AidedZ2 and reversal guard was not being applied to the Aided Distance signal "send" for the schemes that work with 3 channels. ▪ Other small bug fixes	MiCOM S1 Agile v2.0.1 or later	-
				Release of P543 & P545 with distance protection and P443 based on SW 92B. This release is only for 50Hz applications ▪ To make it compliant to IEC 61850 ED2 for new procedures TP2.0 and correction to Germanic Translations ▪ Some other bug fixes		
92	D	M	26 January 2023	Release of P543 & P545 with distance protection and P443 based on SW 92C. This release is only for 50Hz applications ▪ Improvements in phase preference logic ▪ Improvements to TGFD logic	MiCOM S1 Agile v2.0.1 or later	-
AA	K	Q	23 February 2023	First release of MiCOM 5th Generation. Relay models: P54, P44 and P84 are released. This includes models: P443, P446, P543, P546, P841-1CB and P841_2CB with CIT and NCIT. They are based on software 91B and SW 92D. The main changes in this new hardware and software release are as follows: ▪ A 10x performance increase in processing power over the previous Generation (4th Gen) ▪ Colour graphical HMI available as standard, and with native USB support. It includes 1 configurable page, for SLD, measurements and status signals ▪ Simplified ordering options (CORTEC). For instance, distance P44 and line differential P54 can be ordered with models P443 and P543 for single CB applications, or with models P446 and P546 for dual CB applications. They can also be ordered as sub-transmission or sub cycle ▪ Any model can be ordered in the 3 size cases: 40TE (W 203.2 mm or 8"), 60TE (W 304.8 mm or 12") or 80TE (W 406.4 mm or 16"), with a variation in the number of I/O ▪ PRP, HSR and RSTP supported in the same order option ▪ All products are process bus compliant ▪ CyberSentry IEC 62351-8 ▪ 5000 Events, 100 Faults, 1050s Oscillography and 128 Digital Signals ▪ 9 Independently directional distance zones + Z1 extension ▪ Phase segregated aided schemes		P54-TM-EN-1.1 P44-TM-EN-1.1 P84-TM-EN-1.1

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
AA	K	Q	23 February 2023	Adaptive autoreclose to reduce the single pole dead time in case of transient faults, or to block the autoreclose in case of a single fault to ground permanent faults	MiCOM S1 Agile v3.0.1 or later	P54-TM-EN-1.1 P44-TM-EN-1.1 P84-TM-EN-1.1
			29 November 2023	Release of models: P443, P446, P543, P546, P841-1CB and P841_2CB with CIT and NCIT based on software AAK The main reason for this release is to fix a reboot issue and some other bug fixes		
AB	-	Q	August 2024	▪ Compliance to IEC 61850 Edition 2.1 ▪ Support for IEC 61850 Substitution - data points for status and measurement can be substituted ▪ Time Synchronization modelled in new LN LTIM/LTMS ▪ Support for Alarm Handling new LN CALH ▪ Ethernet port link status via new LN LCCH and new DDBs ▪ Top-down engineering - configuration of P40 including GOOSE from SCD file ▪ Configurable RCB name and GCB name ▪ Multi-level control, new DO MltLev - select local or remote for control. To comply to local and remote requirements ▪ Secure Event Logging aligned to IEC 62351-14 - separate audit log for security operations and Syslog updated to align with IEC 62351-14 ▪ Implementation of secure SSH (Secure Shell) communication to the relay from S1 Agile for configuration over Ethernet ▪ New Ethernet board - 1-2 Station Bus ports + Engineering port (CORTEC Hardware Option U/V/W/Y) ▪ All distance zones settable to non-directional/offset/Fwd/Rev (P44/P54 models) ▪ Fault locator improvements for evolving faults (P44/P54 models) ▪ Process bus not supported in this release	MiCOM S1 Agile v3.0.1 or later	P54-TM-EN-2 P44-TM-EN-2 P84-TM-EN-2

2 SOFTWARE VERSION COMPATIBILITY

IED S/W Version	Setting File Version	Menu Text File Version*8	PSL File Version
40	40, 50*4	40	40, 50*2
41	41, 51*4	41	41, 51*2
50	40*5, 50	50	50
51	41*5, 51	51	51
52	52, 54*3	52	52
54	54	54	54
55	55	55	55
57	57	57	57
61	61, 65*1	61	61, 65*3
65	65, 66*1	65	65, 66*3
66	66	66	66
71	71, 75*1	71	71, 75*3
75	75, 76*1	75	75, 76*3
76	76	76	76
77	77	77	77
79	79	79	79
80	80	80	80
82	82	82	82
83	83	83	83
84	84	84	84
85	85	85	85
86	86	86	86
87	87	87	87
91	91	91	91
92	92	92	92
AA	AA	AA	AA
AB	AA, AB	AA, AB	AA, AB

Notes:

*1: Compatible except for Disturbance recorder digital channel selection

*2: Additional functionality added such that setting files from earlier software versions will need additional settings to be made

*3: Compatible except for Disturbance recorder digital channel selection & settings for additional functionality will be missing

*4: Compatible except for the Disturbance recorder digital channel selection and the distance settings

*5: Compatible except for Disturbance recorder digital channel selection & the setting file contains a large number of Distance setting which will each produce an error on download

*6: Additional DDBs were added such that PSL files from earlier software versions will not be able to access them

*7: Additional DDB for the Distance protection will not be included

*8: Menu text remains compatible within each software version but is NOT compatible across different versions

Imagination at work

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