High-Impedance Differential Relaying

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CURRENT DIFFERENTIAL PROTECTION WITH OVERCURRENT RELAYS

The current-differential scheme of protection in which the differential relay current is proportional to the vector difference between the currents entering and leaving the protected circuit is widely applied in various forms for the protection of discrete power system components. Each protected component (i.e. — generator, transformer, etc.) presents unique problems to the successful implementation of the basic current-differential scheme, and unique solutions embodied in the design of the associated relay are required. Usually there are also related restrictions on the CT's used in the scheme.

On a first look basis the protection of station buses would apear to 'lend itself to the application of a current-differential scheme. Figure 1 is a differential circuit for bus protection. It is assumed that the differential relay employed is a low impedance unrestrained instantaneous overcurrent relay. If all the CT's maintain the same nominal ratio for all external faults the assumed scheme is perfectly valid since no current can flow in the relay coil. However, when the instantaneous overcurrent relay is set low enough to give useful sensitivity to internal faults the relay may in practice operate falsely on external faults due to a reduction of the nominal ratio of the fault CT resulting from fault CT core saturation. This reduction of the fault CT nominal ratio results in a "false" differential relay current that may operate the instantaneous overcurrent relay.

The mechanism by which the fault CT core becomes saturated for an external fault is attributable to two factors: (1) the dc component of an offset primary fault current and (2) residual magnetism in the core. The most onerous case occurs when the core fluxes produced by these two phenomena are additive. An improvement of this instantaneous overcurrent scheme would be to utilize an inverse-time, induction-type overcurrent relay. The induction principle makes this relay less responsive to the dc and harmonic components of the "false" differential current resulting from CT errors due to saturation. As well, the time delay can be set to over-ride the dc transient allowing the "false" differential current to subside below the relay's pickup before operation is permitted. This approach usually results in objectionably long clearing times, and from an application viewpoint the complexity of calculations required to obtain an optimum time delay is a predominant reason why this scheme is not widely used for important buses.

An obvious solution to the problem of the saturating fault CT is to design CT's that cannot saturate even for the worst external fault that can be expected. This may be done in a number of ways. One method is to increase the core area and/or reduce the length of the flux path (decrease the mean diameter of a bushing CT). This is usually not practical from the standpoint of cost and space requirements.

The elegant resolution of this problem would be to utilize the fact that the fault CT may saturate as a basis for the solution. This is exactly what has been accomplished. To gain an insight into the reasoning behind the solution it is necessary to examine in more detail the cause and effect of fault-CT saturation for an external fault.

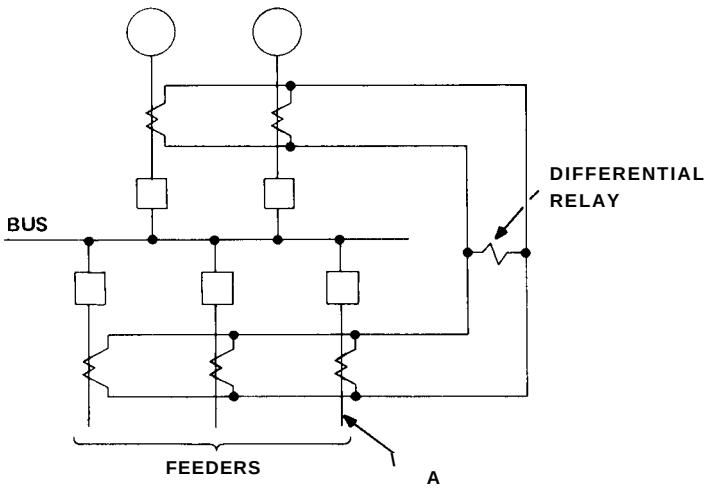


Figure 1

CT PERFORMANCE FOR AN EXTERNAL FAULT THAT SATURATES THE FAULT CT

To prevent duplication of effort in analyzing CT response the burden of the differential relay, ZB, is assumed purely resistive throughout the following considerations. When the differential relay is an overcurrent type ZB will be closer to pure inductance. However, for a qualitative description of CT response the imposition of a resistive burden is not impractical. Actually, foreknowledge that the relay utilized in the solution to this problem has a resistive burden dictates this choice. The magnetization characteristic of the transformer core will be considered to be as shown in Fig. 2. This characteristic assumes zero exciting current and is consequently unrealistic, but a qualitative picture of the CT saturation effect may be obtained. It is further assumed that the CT is wound on a toroidal core resulting in negligible leakage reactance, and the equivalent circuit of Fig. 3 is applicable. In Fig. 3:

X_m = magnetizing inductance (infinite)

R_2 = secondary winding resistance

Z_B = resistive burden that includes the CT lead resistance

$R_p' = \left(\frac{1}{N}\right)^2 R_p$ = core loss-resistance (referred to primary)

The secondary leakage reactance is negligible since a fully distributed winding is assumed, and the core-loss is assumed to be zero.

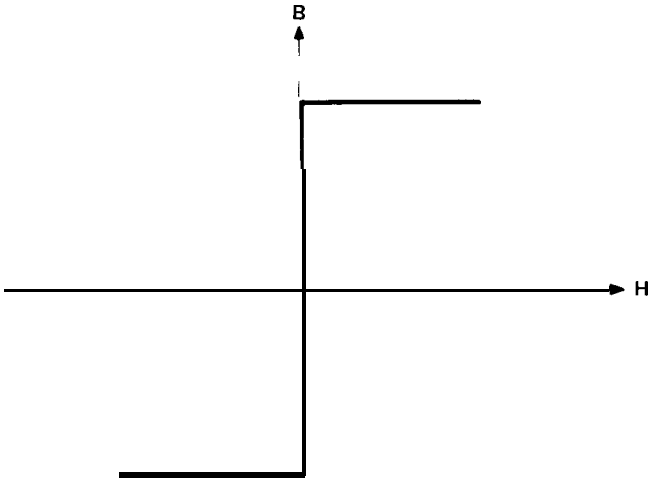


Figure 2

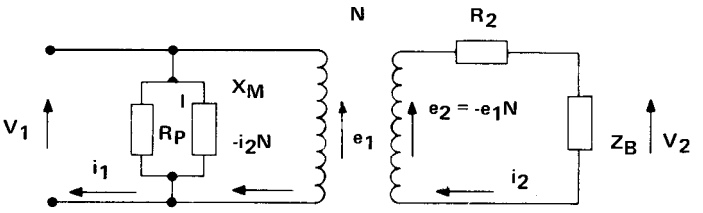


Figure 3

The foregoing assumptions imply that the secondary current of the CT is an exact image of the primary current while the core is unsaturated and that no e.m.f. can be produced while the core is in the saturated state. During unsaturated periods the secondary voltage would be:

$$e_2 = -i_1(R_2 + Z_B)/N \qquad (1)$$

With $i_1 = I_1 \sin \omega t$ the secondary voltage becomes

$$e_2 = -I_1 R_S/N \sin \omega t \qquad (2)$$

where $R_S = R_2 + Z_B$

During the saturated periods e_2 would be zero.

The core flux variation is given by

$$\Phi = -\frac{1}{N} \int e_2 \, dt \qquad (3)$$

$$\Phi = -I_1 \frac{R_S}{\omega N^2} \cos \omega t \qquad (4)$$

Equation 4 assumes no saturation. Figure 4 shows the steady state current and flux variations. It is possible although highly unlikely that saturation will occur for a steady state sinusoidal primary current. Should saturation be reached it must occur before the peak value of the flux wave of Fig. 4B. If at $\omega t = \omega t_1$ the saturation point is reached then for $\omega t > \omega t_1$ no further e.m.f. will be produced and the secondary current will collapse instantly to zero. The core remains saturated until the exciting current falls to its saturation value which in this instance is zero. The core cannot unsaturate before the primary current zero.

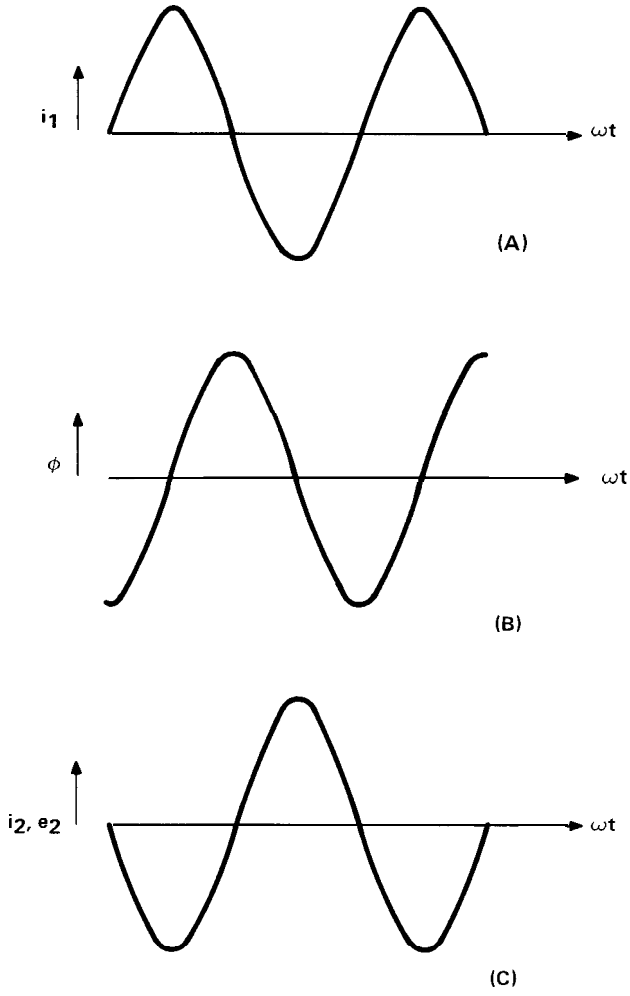


Figure 4

For this steady state saturation case the flux may be expressed as

$$\Phi \Big|_{\omega t_1}^{\pi} = \Phi_{SAT} \qquad (5)$$

$$\Phi \Big|_{\pi}^{\omega t} = \Phi_{SAT} - I_1 \frac{R_S}{\omega N^2} \cos \omega t \Big|_{\pi}^{\omega t} \qquad (6)$$

$$\Phi \Big|_{\pi}^{\omega t} = \Phi_{SAT} + I_1 \frac{R_S}{\omega N^2} (1 + \cos \omega t) \qquad (7)$$

where in the above equations $\pi \leqslant \omega t \leqslant (\pi + \omega t_1)$. Figure 5 shows the waveforms for this case. An ex-

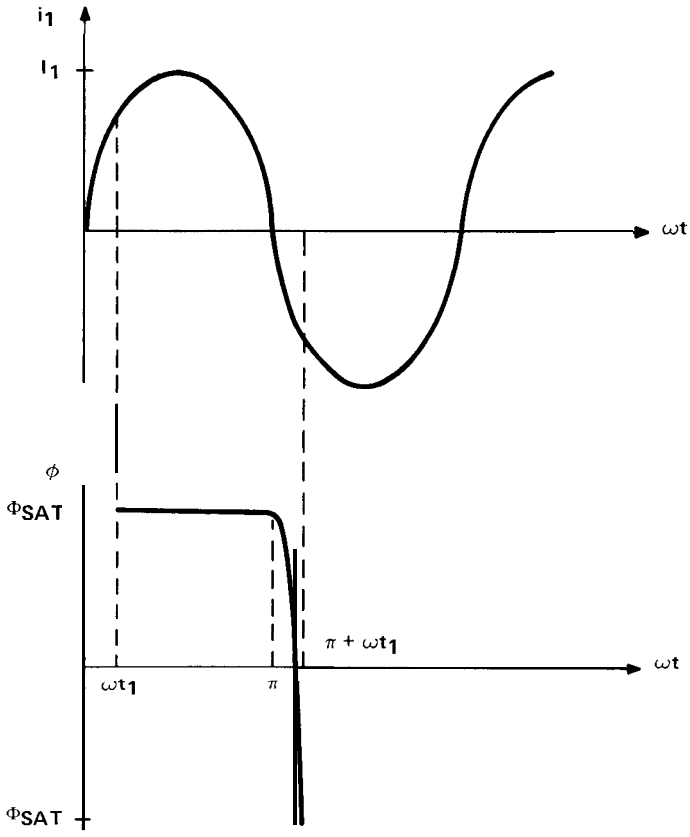


Figure 5

pression for Φ_{SAT} may be obtained by noting that at $\omega t = \pi + \omega t_1$, $\Phi = -\Phi_{SAT}$.

$$\Phi_{SAT} = \Phi_{SAT} + I_1 \frac{R_S}{\omega N^2} (1 + \cos (\pi + \omega t_1)) \qquad (8)$$

$$\Phi_{SAT} = I_1 \frac{R_S}{2\omega N^2} (\cos \omega t_1 - 1) \qquad (9)$$

A given CT will have a fixed value of Φ_{SAT} and to just avoid core saturation ωt_1 must have a value of π which results in a primary current given below.

$$I_1 = \frac{\omega N^2}{R_S} \Phi_{SAT}$$

The above equation may be rewritten as

$$\Phi_{SAT} = I_1 \frac{R_S}{\omega N^2}$$

with the realization that I_1 is the dependent variable.

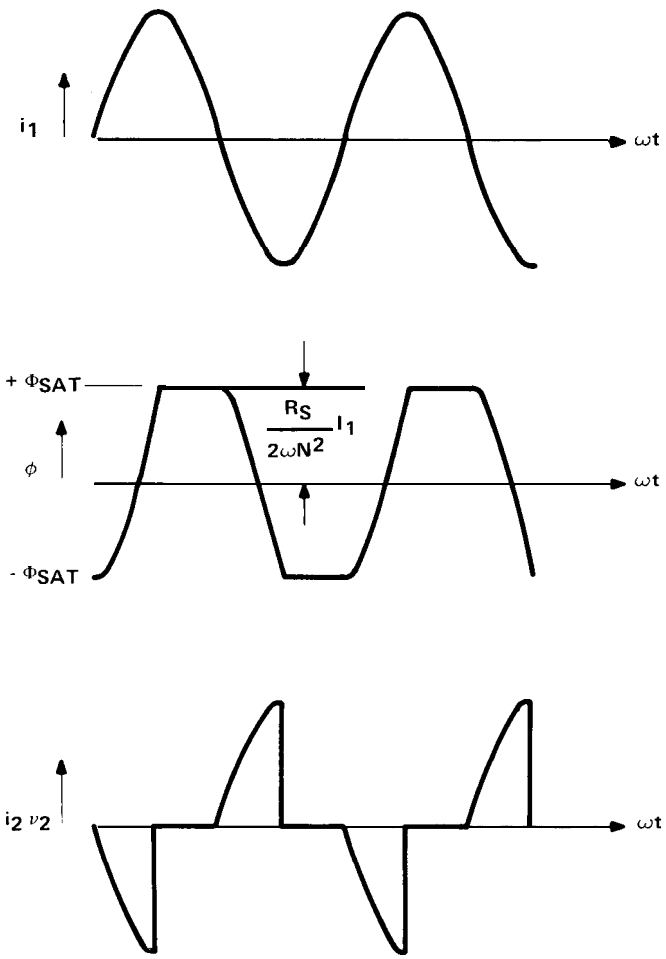


Figure 6

Assuming that

$$\Phi_{SAT} = I_1 \frac{R_s}{2\omega N^2}$$

means that $\omega t_1 = \pi/2$, and Fig. 6 shows the current and flux variations for this case. The secondary current and voltage is cutoff past the saturation time ωt_1 for each half cycle. The preceding has been a qualitative analysis concerned with steady state sinusoidal primary currents, but as mentioned previously the primary cause of fault CT saturation is dc offset in the primary current.

Figure 7a shows a fully offset primary current wave. It is assumed that

$$\Phi_{SAT} = I_1 \frac{R_s}{\omega N^2}$$

so that in the steady state (no offset) full reproduction of the primary current will take place. The primary current is given as

$$i_1 = I_1 \cos(\omega t + a - \theta) - \epsilon^{-\frac{R'}{L'} t} \cos(a - \theta) \quad (10)$$

where: a = ∢ after voltage peak at which fault occurs

θ = primary circuit phase angle

R′ = total resistance in power system

L′ = total inductance in power system

For the waveform of Fig. 7a it was assumed that $\omega L'/R' = 8$ and $(a - \theta) = 0$. This results in

$$i_1 = I_1 (\cos \omega t - \epsilon^{-\frac{\omega t}{8}}) \quad (11)$$

The flux is then:

$$\phi = -\frac{1}{N} e2\, dt = -\frac{R_s}{N2} i_1\, dt \quad (12)$$

$$\Phi = -\frac{I_1 R_s}{\omega N^2} \sin \omega t + 8(\epsilon^{-\frac{\omega t}{8}} - 1) \quad (13)$$

$$\phi = -\Phi_{SAT} \sin \omega t + 8(\epsilon^{\frac{\omega t}{8}} - 1) \quad (14)$$

Equation (14) is valid until the saturation point is reached. Once saturation is reached it is maintained until the next primary current zero at which time desaturation would begin. Upon desaturation the flux would change from the constant saturation value at the same rate it would have changed had saturation not occurred. This flux variation is shown in Fig. 7b. The resulting secondary current is depicted in Fig. 7c.

It is now possible to qualitatively explain the appearance of a "false" differential current for the case of a saturated fault CT during an external fault. A fault at A is assumed as shown in Fig. 1. Figure 8 is a simplified diagram of the actual conditions where the CT lead resistances are neglected.

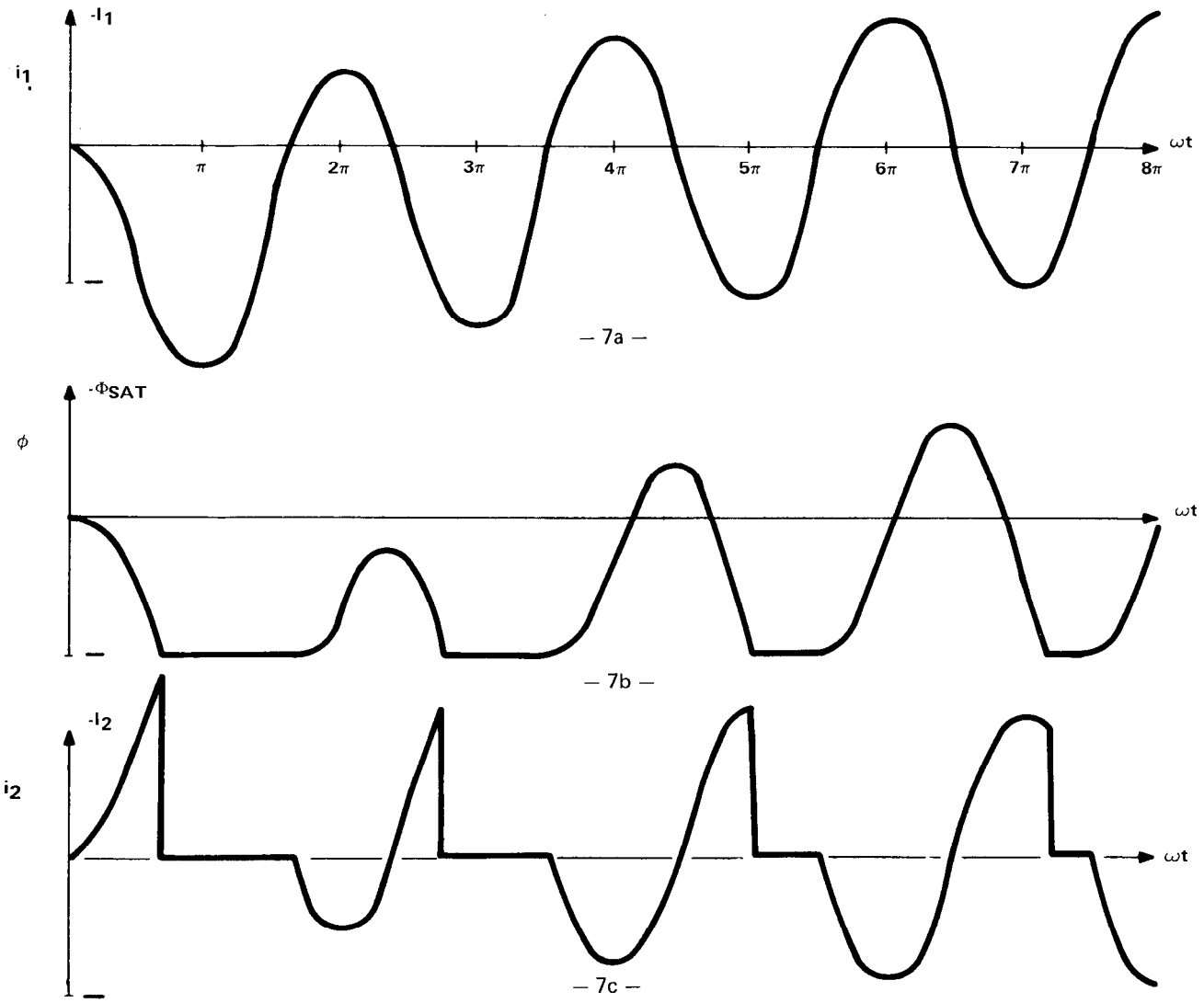


Figure 7

The sum of the two source CT secondary currents, i_T, is assumed to be the fully-offset waveform of Fig. 7a referred to the secondary. This means the source CT's do not saturate. It is further assumed that the fault CT saturates and its secondary current is as shown in Fig. 7c. During the periods that the fault CT is saturated the secondary source CT current, it, will flow through the differential relay coil provided its impedance is low compared with the fault CT resistance. During the period that the fault CT is not saturated id = 0 since the fault CT is producing the required current. The consequence is that a current waveform shown in Fig. 9b flows through the low impedance relay. This "false" differential current decreases in magnitude and pulse width as the primary current waveform approaches a sinusoidal steady state value since concurrently the fault CT saturates for less of each succeeding negative primary current half cycle. For the example assumed the "false" differential current decays to zero in approximately five cycles.

Had there been residual flux in the fault CT core prior to the occurrence of the external fault the "false" differential current in the low impedance

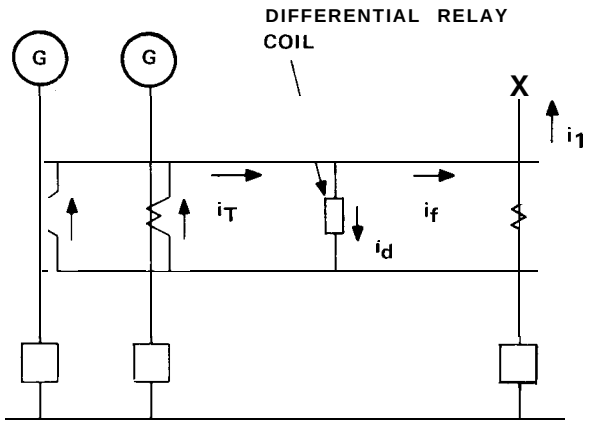
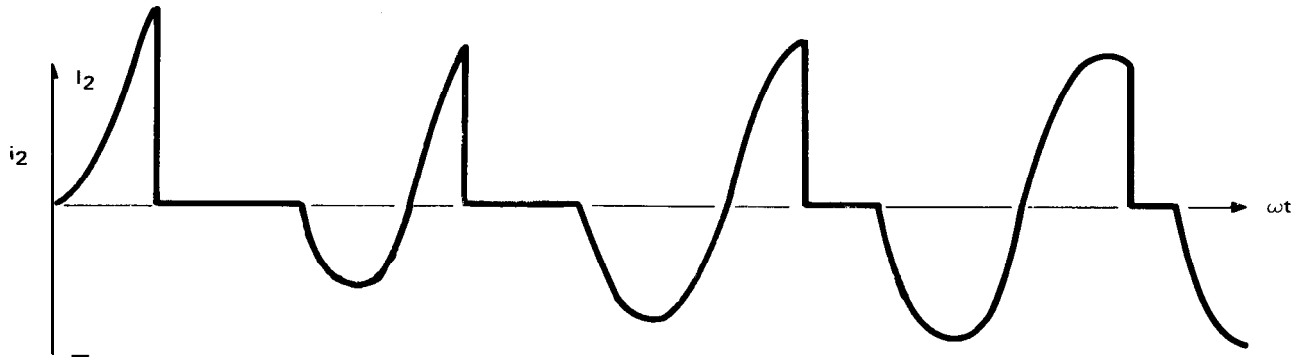


Figure 8

relay coil could have increased. Assume that a residual flux equal to the previously stated saturation level, Φ_{SAT}, was present and that its direction is such that it adds to the flux produced by the first half cycle of the fully offset primary current. The result is shown in Fig. 10. In this case the entire fully offset half cycle is reproduced as "false" differential current.

It is this "false" differential current flowing in the low impedance coil of an instantaneous overcurrent relay that can cause false operation for an external fault. Figure 11 is an actual oscillogram for a fully offset external fault current with several source CT's feeding the fault, and with a low impedance overcurrent relay as the differential relay. Trace A shows the fully offset primary current in the fault CT and trace B is the total current from all source CT's fed into the differential junction, also fully offset. Trace C shows the secondary current in the fault CT which can be assumed to be transformed current since the differential relay impedance is very low compared with the fault CT resistance. The differential current is represented by trace D and shows that the initial cycle is nearly a fully offset wave. Trace C is a good illustration of the current in the secondary of a saturated CT as shown in Figs. 7c and 10b.



– 9a –

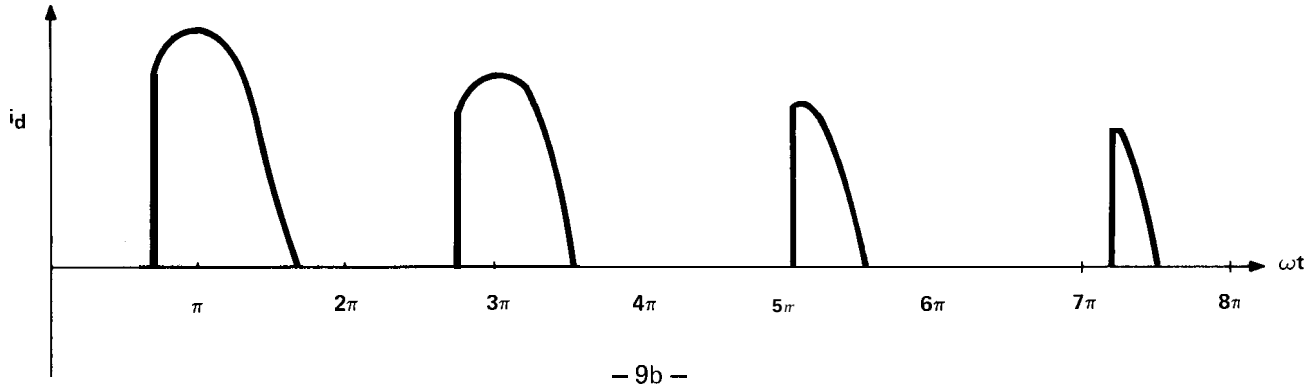


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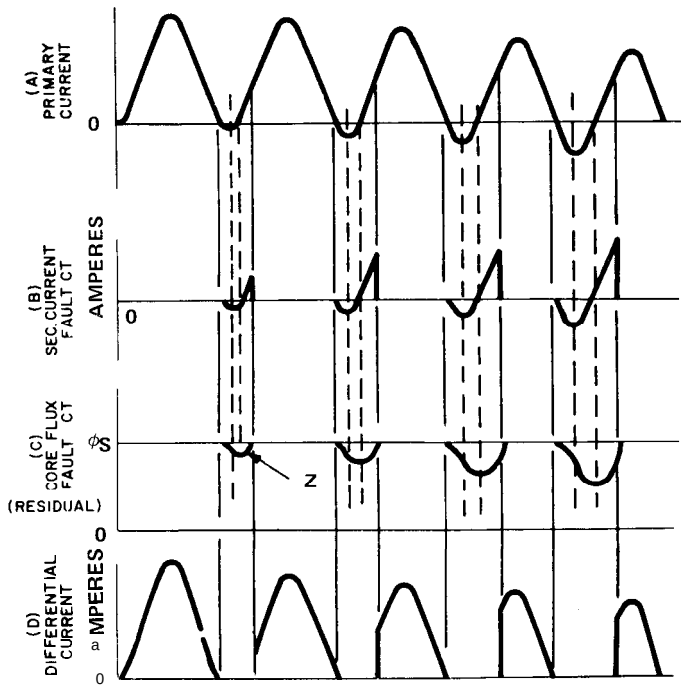
Figure 9

USE OF A HIGH IMPEDANCE RELAY IN
THE DIFFERENTIAL SCHEME



FLUX AND
CURRENT VARIATIONS IN FAULT CURRENT
TRANSFORMER

Figure 10

If the relay coil is a high impedance in relation to the fault CT secondary winding resistance the "false" differential current would then flow through the secondary of the fault CT. A corresponding "error" voltage, V_E, would appear across the saturated CT secondary and across the high impedance relay coil connected to this CT. This voltage magnitude across the high impedance relay would be

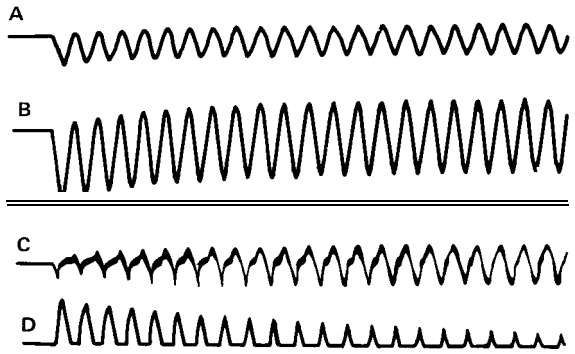
$$V_E = i_d R_c \qquad (15)$$

where R_c = secondary winding resistance of fault CT plus CT lead resistance from fault CT to relay

i_d = "false" differential current

VE would have a waveshape like that shown in Fig. 11d.

The high impedance relay would have to be set such that it would not operate for the maximum



A. PRIMARY CURRENT. B. SECONDARY CURRENT FROM SOURCE CT'S. C. SECONDARY CURRENT FAULT CT. D. DIFFERENTIAL CURRENT

Figure 11

"error" voltage expected. The maximum error would occur when the fault CT reached full saturation and the source CT's did not saturate at all. For a worst case analysis it is assumed that the fully offset primary current has no exponential decay component and that the fault CT remains completely saturated. The "false" differential current through the secondary winding of the fault CT under these unrealistic conditions would be as shown in Fig. 12. The peak voltage between the junction points is:

$$V_E\,(pk) = 2\,I_D R_c \qquad (16)$$

$$V_E\,(pk) = 2\,\frac{I_F}{N} R_c \qquad (17)$$

where IF = peak value of maximum external fault current

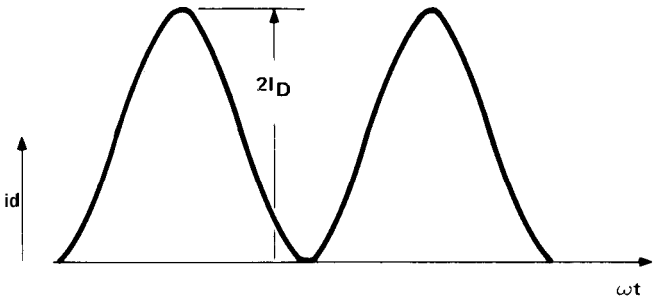


Figure 12

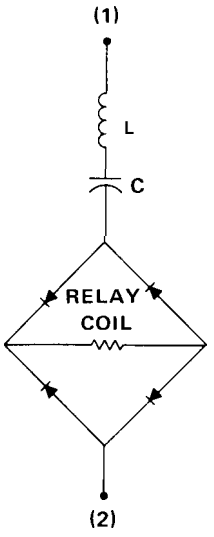


Figure 13

In the actual design of the high impedance relay, type PVD, a resonant circuit tuned to 60 hertz is placed in series with the operating coil. This is shown in Fig. 13.

The operating unit is isolated within a full wave rectifier so that changes in its inductive reactance due to adjustment changes will not disturb the tuning of the resonant circuit. This circuit design means the unit tends to respond more to the RMS 60 Hz component of whatever waveshape is applied than to the peak value. Consequently for the waveform of Fig. I2 the relay would be set for an RMS value given by equation (18)

$$V_E = \frac{I_F}{\sqrt{2}N} R_C = \frac{I_{F(RMS)}}{N} R_C \qquad (18)$$

Actually a safety factor of 2 is incorporated into the setting.

$$\text{PICKUP SETTING} = 2 \frac{I_{F(RMS)}}{N} RC \qquad (19)$$

With a voltage setting on the high impedance differential relay as determined by equation (19) the scheme is now secure against operation on external faults. If for all *internal* faults the voltage across the relay circuit exceeds the setting as determined by equation (19) then this approach will be applicable. It is necessary to investigate CT performance with a high impedance burden to ascertain what the voltage across the relay will be for an internal fault.

CT PERFORMANCE FOR AN INTERNAL FAULT WITH A HIGH IMPEDANCE BURDEN

The ultimate high impedance burden is the open secondary condition. It is common knowledge that current transformers are not to be operated with their secondary windings open-circuited because of the high-peak voltages that result. When the secondary is open-circuited the primary side ampere-turns provide excitation only, and at all reasonable current levels the core is in saturation except for short periods near the current zeroes. Since the magnetization characteristic of the assumed core material dictates that the magnetizing inductance is infinite the core-loss resistance referred to the secondary, R_p, must now be assumed to be some value less than infinity to provide for a realistic equivalent circuit for open secondary conditions. Figure 14 shows this equivalent circuit referred to the primary.

For unsaturated conditions the secondary voltage will be:

$$e2 = -Ne_1 = -(N) i_E \left(\frac{1}{N}\right)^2 R_p \qquad (20)$$

$$e2 = -\frac{1}{N} R_p I_1 \sin \omega t \qquad (21)$$

The core flux variation will be:

$$\phi = -\frac{1}{N} \int e_2 dt = \frac{1}{N^2} R_p I_1 \sin \omega t \qquad (22)$$

If at $\omega t = 0$, $\phi = -\Phi_{SAT}$ then for $\omega t > 0$ equation (23) is valid up to the point where $\phi = +\Phi_{SAT}$.

$$\phi = -\Phi_{SAT} + \frac{1}{\omega N^2} R_p I_1 (1 - \cos \omega t) \qquad (23)$$

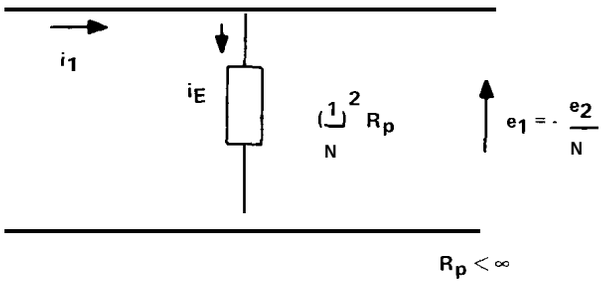


Figure 14

The flux and secondary voltage variation with primary current is as shown in Fig. 15. These waveforms are similar to those in Fig. 6 except that the core saturates sooner and consequently the secondary voltage approaches a pulse. The peak magnitude of the secondary voltage is much higher for the open circuited condition because $R_p \gg R_S$.

If at $\omega t = \omega t_2$, $\phi = +\Phi_{SAT}$, then

$$\frac{1}{\omega N^2} R_p I_1 (1 - \cos \omega t_2) = 2 \Phi_{SAT}.$$

$$\cos \omega t_2 = \sqrt{1 - \sin^2 \omega t_2} = 1 - \frac{2\Phi_{SAT} \omega N^2}{I_1 R_p}$$

$$\sin^2 \omega t_2 = 1 - \left(1 - \frac{2\Phi_{SAT} \omega N^2}{I_1 R_p}\right)^2$$

$$\sin \omega t_2 = \left(1 - \left(1 - \frac{2\Phi_{SAT} \omega N^2}{I_1 R_p}\right)^2\right)^{1/2}$$

$$\sin \omega t_2 = \left(1 - 1 + \frac{4\Phi_{SAT} \omega N^2}{I_1 R_p}\right)$$

$$\left(\frac{2\Phi_{SAT} \omega N^2}{I_1 R_p}\right)^{1/2}$$

$$\sin \omega t_2 \cong 2 \left(\frac{\Phi_{SAT} \omega N^2}{I_1 R_p}\right)^{1/2} \quad (24)$$

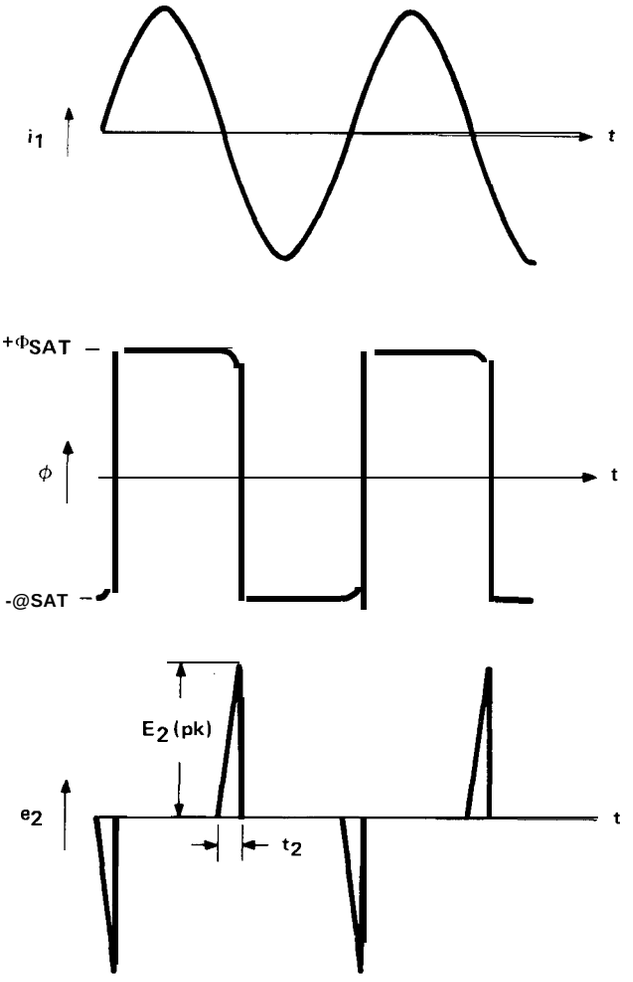


Figure 15

From equation (21) the peak secondary voltage is

$$E_2 (pk) = -\frac{1}{N} R_p I_1 2 \left(\frac{\Phi_{SAT} \omega N^2}{I_1 R_p}\right)^{1/2}$$

$$E_2 (pk) = 2 (\omega R_p I_1 \Phi_{SAT})^{1/2} \quad (25)$$

In actuality the current transformer is not open circuited but rather shunted by the high impedance of the differential relay. If $R_p \gg Z_B$ then R_p in equation (25) may be replaced with Z_B.

$$E_2 (pk) = 2 (\omega Z_B I_1 \Phi_{SAT})^{1/2} \quad (26)$$

An example follows to show the relative magnitude of peak voltage across the high impedance differential relay coil for internal versus external faults. The following values are assumed:

$R_c = 1.7\ \Omega$

$I'_F = 14{,}500$ a (RMS)

$N = 240$ (1200/5 CT)

$Z_B = 2600\ \Omega$

For an external fault the error voltage is given by equation **(18)**.

$$V_E = \frac{1}{N} I'_F R_c = 102 \text{ VRMS}$$

For an internal fault of the same magnitude the voltage across the high impedance relay is given by equation (26).

The flux saturation level, Φ_{SAT}, may be expressed as in equation (27) where I_1 is actually the dependent variable.

$$\Phi_{SAT} = \eta I_1 \frac{Z_B}{\omega N^2} \qquad (27)$$

where $0 < \eta \leq 1$

The peak voltage may now be expressed as

$$E_2(pk) = 2 \quad W Z_B I_1 . \frac{Z_B I_1}{\omega N^2} . \quad \eta^{1/2} =$$

$$2\sqrt{\eta} . \frac{Z_B I_1}{N}$$

Since it is known that the core saturates quickly a value of $\eta = 10^{-4}$ might be assumed.

$$E2\ (pk) = 2\sqrt{\eta}\frac{Z_B \sqrt{2} I'_F}{N}$$

$$E2\ (pk) = 4440 \text{ v}$$

Although there is a wide divergence between maximum "error" voltage during an external fault and peak voltage during an internal fault for faults of the same current magnitude, the actual margin of operation for the relay is less since the relay does not respond to peak voltage values. When determining the sensitivity of a high impedance differential relay for a given situation the minimum internal fault current required to operate the relay at its pickup setting (determined from equation (19)) is calculated. With a fault on the bus of Fig. 1 the equivalent circuit will be that of Fig. 16 in which the secondary winding resistances have been neglected. The minimum primary internal fault current necessary to operate the relay is given by equation (28).

$$i_F(MIN) = N\, i_{MIN} = N \sum_{n=1}^{X} i_{E_n} + i_R \qquad (28)$$

where: i_R = PICKUP SETTING/Z_B

X = number of CT's connected to relay

The excitation current, i_E, of each CT is determined from its associated secondary excitation curve by finding the exciting current corresponding to the voltage pickup setting of the relay. The idealized B-H characteristic of Fig. 2 is now replaced with a more realistic characteristic to produce secondary characteristics as shown in Fig. 17. If the calculated current from equation (28) is less than the minimum internal fault current expected the application is sound.

To insure a substantial margin of operation the high impedance relay pickup setting should not be greater than the knee voltage, E_S, of the poorest CT connected to the relay. A significant increase in voltage across the high impedance relay over the pickup value should be realized for internal fault currents that exceed 2 to 3 times that calculated from equation (28). With the pickup voltage at or above the knee point of the worst excitation characteristic an increase in internal fault current above the minimum value may not produce an appreciable increase in secondary RMS voltage. This may be verified by referring to Fig. 17.

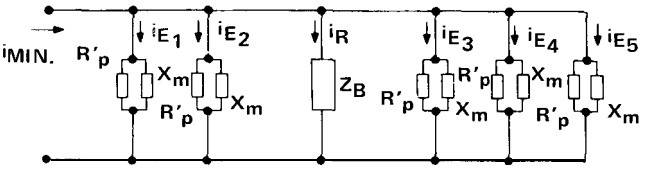


Figure 16

CT SECONDARY EXCITATION CHARACTERISTICS

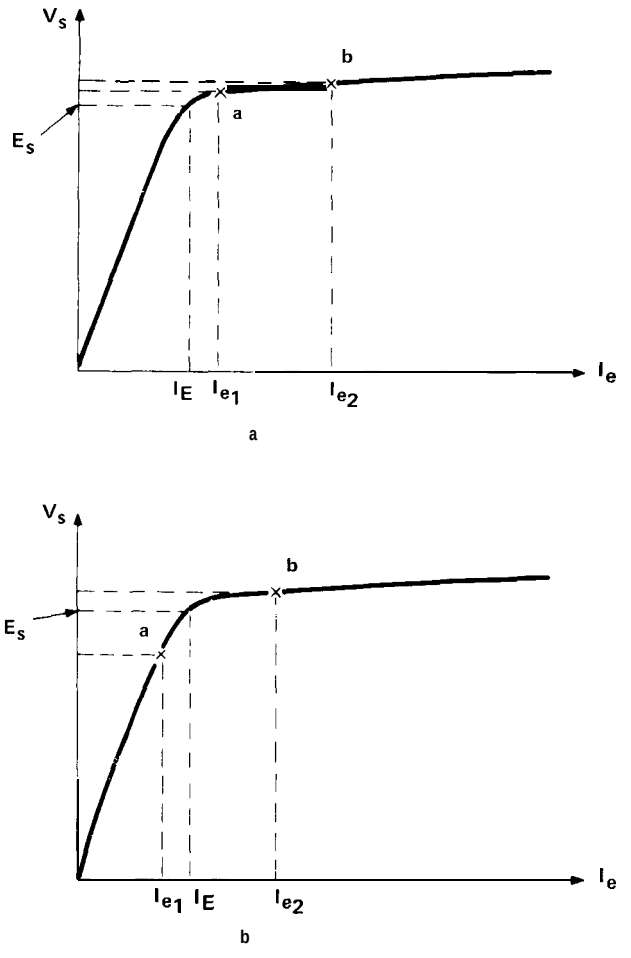


Figure 17

In Fig. 17a point a is located by plotting the pickup voltage, and I_{e1} is the corresponding excitation current. It is assumed that some multiple of minimum internal fault current will cause the excitation current to increase to I_{e2} which establishes point b. Figure 17b is similarly constructed except that point a is located below the knee of the curve. There is a greater increment in RMS secondary voltage in 17b than in 17a. For the same increase in internal fault current above the minimum value the pickup setting as shown in Fig. 17b will provide a greater margin of operation (increment in secondary voltage) than that shown in Fig. 17a.

Should equation (19) yield a pickup setting at or above the knee point voltage it would be desirable to decrease the setting to a value below the knee point. Usually it is possible to reduce the pickup setting determined by equation (19) by some amount and still maintain security on external faults. This is so because fault CT saturation does not exist throughout the entire current cycle, and the source CT's usually saturate quickly reducing the time that the relay must withstand the "error" voltage. The amount by which the setting determined from equation (19) may be reduced has been empirically determined for bushing CT's utilized in GE switchgear and is published in the instruction book for the PVD relay. If this allowable reduction results in a pickup setting below the knee point then scheme reliability is enhanced.

For the conditions depicted in Fig. 17b the minimum internal fault current does not saturate the core of the worst CT, but any significant increase over minimum will saturate the core. For most internal faults high peak voltages will appear across terminal points 1-2 of Fig. 13.

OVERVOLTAGE PROTECTION IN THE HIGH IMPEDANCE RELAY

To protect the various relay components and the associated insulation from these potentially excessive voltages a Thyrite resistor is placed across the relay. The Thyrite is a non-linear resistor with an I-V characteristic as shown in Fig. 18.

The addition of the Thyrite resistor will desensitize the relay since it limits the peak voltage which in turn decreases the RMS value. This desensitizing effect may be taken into account by modifying equation (28).

$$i_{F(MIN)} = N \sum_{n=1}^{X} i_{E_n} + i_R + i_{Thyrite} \qquad (29)$$

Equation (29) indicates that the minimum internal fault current necessary to operate the relay at its pickup setting has increased. The Thyrite current, $i_{Thyrite}$ is determined from a published I-V characteristic similar to that of Fig. 18 evaluated at the pickup setting of the relay. In general this current is quite small at the relay pickup voltage setting.

THYRITE I-V CHARACTERISTICS

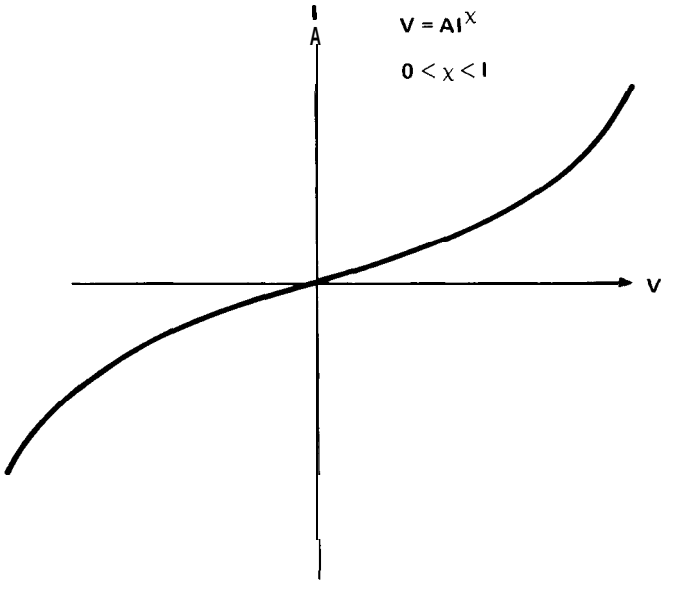


Figure 18

In the application of the PVD high impedance relay the contact of an auxiliary lockout relay short circuits the Thyrite following relay operation to protect it from overheating. The Thyrite is short-time rated in regards to heat dissipation, and the shorting action of the lockout relay reduces the duty time of the Thyrite by an amount equal to the difference between breaker operating time and auxiliary lockout operating time.

CT APPLICATION CONSIDERATIONS IN RELATION TO HIGH-IMPEDANCE DIFFERENTIAL RELAYING

Throughout all of the preceding considerations the use of CT's with fully distributed windings on a toroidal core has been assumed. The result has been that secondary leakage reactance was disregarded, and this fact is reflected in Figure 3 and equation (19). It is possible to apply the PVD relay with CT's that have significant secondary leakage reactance, but accurate data must be available concerning this secondary leakage reactance. Because there usually exists significant uncertainty regarding the true value of the secondary leakage reactance the pickup setting of the PVD as determined from a modified equation (19) (R_C replaced by R_C + secondary leakage reactance) will be uncertain. For this reason CT's with significant secondary leakage reactance, such as window-type CT's, are not generally recommended for application with the PVD relay. The recommended CT type is that which has its secondary wound on a toroidal core with the windings completely distributed around the core (bushing type). Figure 19 illustrates the difference between a completely distributed and a non-distributed secondary winding.

In applications involving two different CT ratios the turns ratio of each CT connected to the PVD relay must be identical requiring the higher ratio CT's to be used on a lower tap. An initial restriction on this mixed ratio CT application is that the lower tap on the higher ratio CT must be fully distributed. This is a necessary but not sufficient condition to insure a satisfactory scheme utilizing mixed ratio CT's.

Assuming that the requirement for a fully distributed tap is met the other consideration is the auto-transformer effect in the higher ratio CT's during an internal fault. A 1200/5 CT used on its fully distributed 600/5 tap will have a high secondary voltage appear across its full winding during an internal fault. The Thyrite units in the PVD will limit the voltage across the 600/5 portion of the winding but this voltage is amplified by a factor of 2 when it appears across the 1200/5 winding. This higher voltage may exceed the capability of the insulation in the circuit connected across the full winding. The basic problem is to limit this

voltage to safe values without doing thermal damage to the Thyrite units. The difficulty is ascertaining these two conditions is the primary reason why use of the PVD with different ratio CT's is not recommended. However, in those situations where use of different ratio CT's cannot be avoided there are certain connections that may be applicable.

An obvious approach might be to simply connect the PVD across the full winding of the lower ratio CT's and the matching fully distributed taps of the higher ratio CT's. The peak voltage appearing across the full winding of the higher ratio CT would then have to be calculated, and if it is determined that this value is within the insulation capability of the terminal blocks, leads, cables, etc. connected across the full winding of the higher ratio CT then this connection is applicable provided the ratings of the Thyrite unit are not exceeded.

An approach to determining the safe operating limit of the Thyrite unit is outlined below. The Thyrite unit in the PVD relay is a stack comprised of a number of disks placed in series. Each disk can withstand a given crest voltage depending upon the number of disks in the stack. A higher crest voltage can produce a punch-through effect which will destroy the disk. Each Thyrite disk is capable of dissipating 1800 watt-seconds of energy. Assuming a PVD operating time of 3 cycles and a lock out relay time of 1 cycle, the Thyrite stack will be subjected to the total secondary fault current for 4 cycles or 8 half cycles. Thus the maximum dissipation per Thyrite disk should not exceed 225 watt-seconds per half cycle.

The magnitude of the peak voltage that can be developed depends on the magnitude of the internal fault, and on the excitation characteristic of the associated CT as well as the I-V characteristic of the Thyrite. Consequently, it is possible to plot a family of curves of secondary peak voltage, e_p, versus E_S/per Thyrite disk with internal fault current magnitude as the parameter. Peak voltage is taken as the drop necessary to force through the Thyrite the total current that flows at the peak of the sinusoidal fault current (90^O) or at the point where the core saturates if this occurs before the fault current peak. The same type of plot is constructed for a fully-offset internal fault current. Figures 20 and 21 are representative curves for sinusoidal and fully-offset internal fault currents respectively. This data is computed analytically and a different set of curves will be obtained for each different CT core saturation level. However, a representative flux density at saturation, B_m, may be assumed.

It is now possible to obtain the peak voltage across the PVD by simply knowing the maximum internal fault current and the e_s value of the poorest CT connected to it. This is accomplished by determining the maximum value of e_p from either Figure 20 or 21 and multiplying this value by the number of disks in the stack. This voltage is then multiplied by the ratio of total turns to used turns to obtain the peak voltage developed across the full winding of the higher ratio CT. It then must be determined whether the CT and its associated leads and terminal blocks are capable of withstanding this magnitude of peak voltage.

Plots of watt-seconds/half-cycle versus Es/ Thyrite disk with internal fault current as the parametric quantity may be plotted as shown in

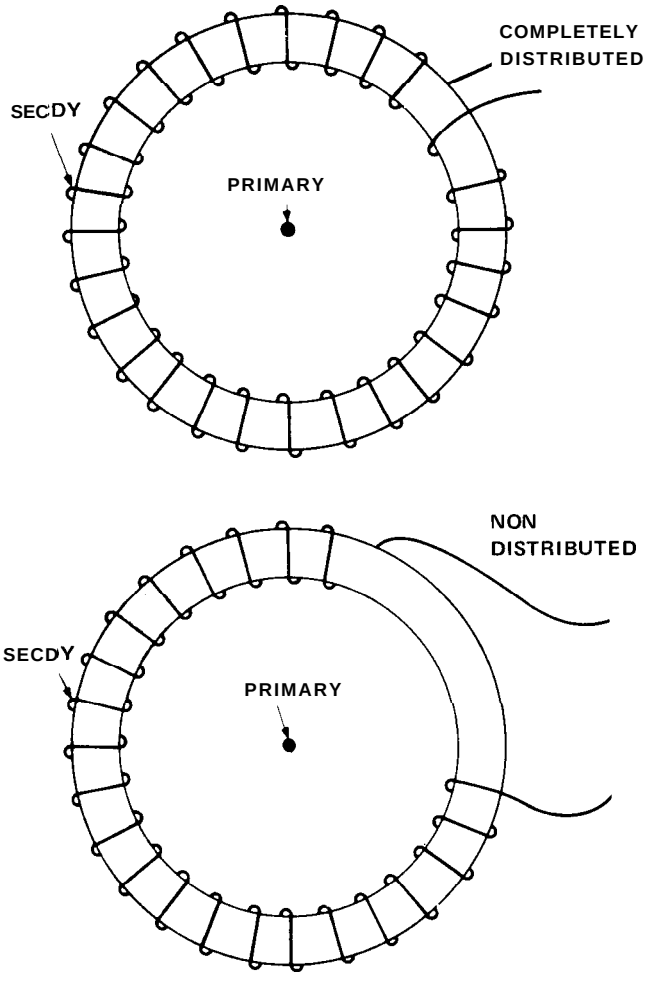


Figure 19

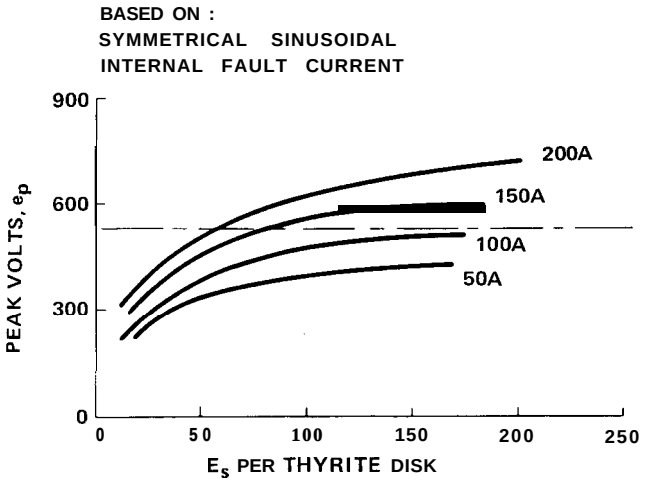


Figure 20

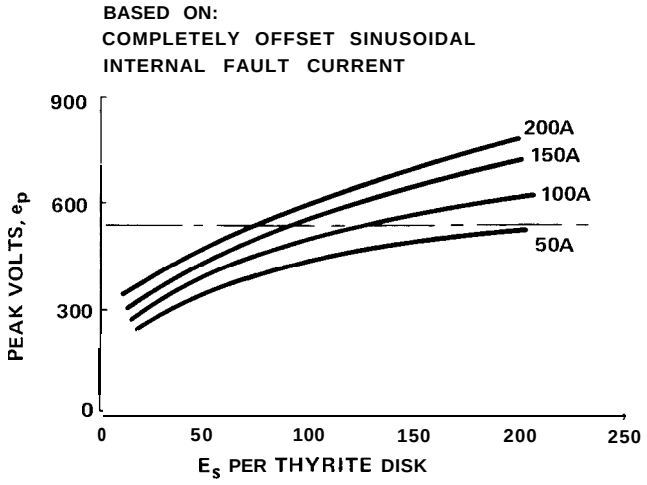


Figure 21

Figure 22. This information is obtained by means of a numerical iterative technique that calculates energy dissipated in each Thyrite disk per half cycle up to the point where the CT saturates and is based on symmetrical sine wave current. A similar curve may be plotted for a fully offset current wave, but it has been found that this case is less limiting than the symmetrical current wave.

As stated previously the watt-second rating of a Thyrite disk used in the PVD is 225 watt-seconds/ half cycle. The safe peak voltage across the stack is 2120 volts; 530 volts/disk for a 4 disk stack, 700 volts/disk for a 3 disk stack and 1060 volts/disk for a 2 disk stack. Assuming a 4 disk stack Figures 20, 21 and 22 may be combined into Figure 23. The curves of Figure 23 provides the relation between RMS symmetrical amperes and E_S of the

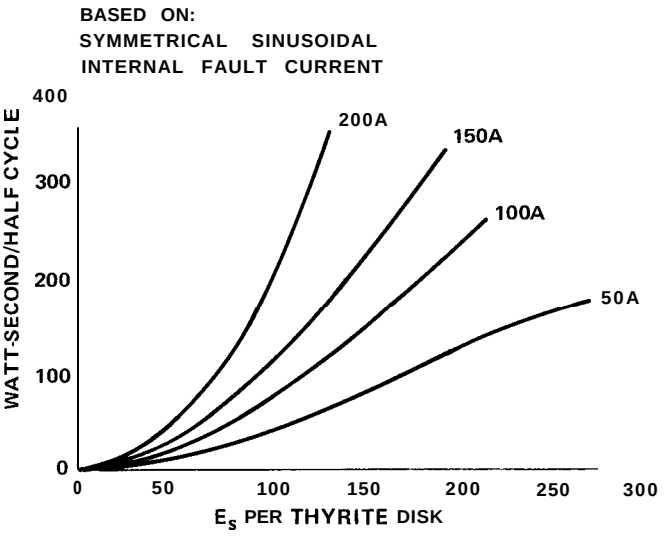


Figure 22

poorest CT that will not result in either the crest voltage rating, 530 volts/disk, or heating limit of the Thyrite unit from being exceeded. As can be seen the crest voltage is actually the limiting factor. Figure 24 would be used to determine if the Thyrite unit is within its rating and this information coupled with the previously determined peak voltage across the full winding of the higher ratio CT will determine if the previously mentioned connection for a mixed ratio CT application is feasible.

The curves in Figures 20 through 23 are not accurately plotted and should not be used to determine actual values. Accurate plots are available upon request.

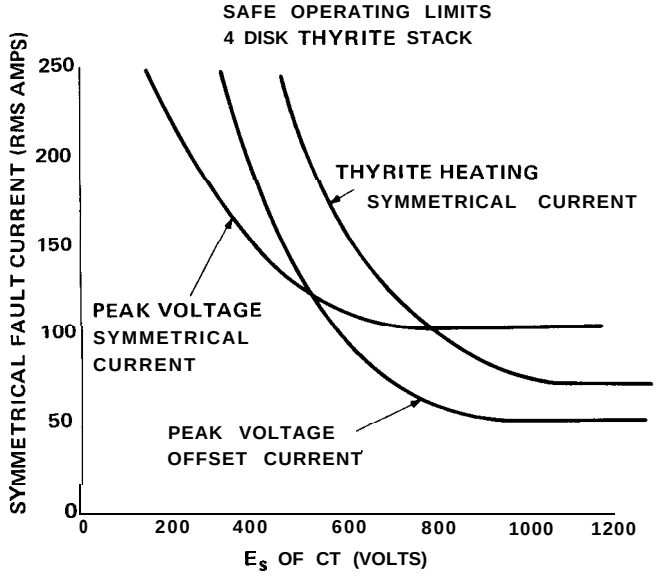


Figure 23

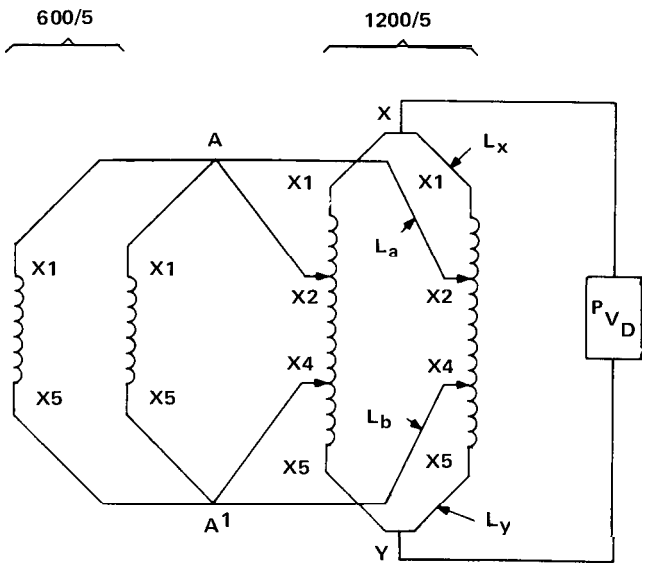


Figure 24

A better connection for a mixed ratio CT application might be to place the Thyrite unit across the full winding of the higher ratio CT. There are numerous connections that incorporate this feature, but the particular connection shown in Figure 24 has a number of desirable features. The connection shown in Figure 24 does not require any modification to the PVD nor does it require any auxiliary CT's. In fact the higher ratio CT's serve as auxiliary CT's as well as main CT's, and any CT may be removed from service without removing the differential protection.

A difficulty with this scheme is that of calculating the voltage V_{xy} for external faults. This comes about because it is difficult, if not impossible, to determine the current distribution in the CT secondary jumpers. For example, for a fault on one of the 600/5 circuits, it would be difficult to determine how much current would flow in leads L_a and L_b, and how much current would flow in leads L_x and L_y. Since this information is required to establish the V_x voltage, and hence the PVD setting, a problem exists.

Outlined below is a conservative approach for obtaining a safe PVD setting for this arrangement. Initially assume that all the lower ratio taps of all the CT's are connected in parallel, and the end windings of the higher ratio CT's are "floating". Fig. 25 shows the arrangement for this assumption. Calculate the voltage across the full winding of each higher ratio CT for single phase to ground and

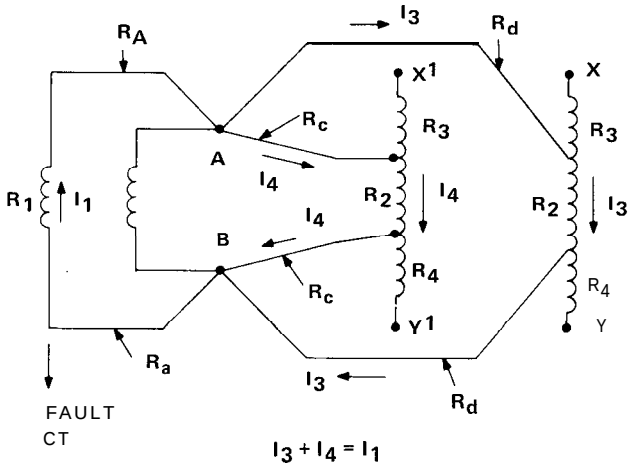


Figure 25

three phase faults just off the bus on each of the lower rated circuits in turn.

For the purpose of calculating V_{xy} or $V_{x'y'}$ it is assumed as usual that the fault CT saturates completely. The voltage drop across A-B is therefore

$$V_{AB} = I_1 (R_1 + KR_A) \qquad (30)$$

where:

I_1 = secondary current being pushed through saturated fault CT

R_A = one-way lead resistance from fault CT to junction pts. A&B.

K = 1 for three phase faults, and 2 for single phase to ground faults

The voltage across the taps of the higher ratio CT, V_T, is then V_{AB} plus the voltage drop in the connecting leads.

$$V_T (xy) = V_{AB} + I_3 (KR_D) = \qquad (31)$$

$$I_1 (R_1 + KR_A) + I_3 (KR_D)$$

The *internal* voltage, V'_i, that is amplified by the total turns/tap turns ratio is V_T plus the voltage drop in the secondary winding the xy CT. Consequently, the amplified internal voltage is:

$$V'_i = P \quad I_1 (R_1 + KR_A) + I_3 (R_2 + KR_D) \qquad (32)$$

where

P = total turns/tap turns

To obtain the *external* voltage across XY the voltage drop across the secondary winding resistance, R2, must be subtracted from V'i.

$$V_{xy} = P \quad I_1(R_1 + KR_A) + \quad (33)$$
$$I_3(R_2 + KR_D) \quad - I_3 R_2$$

$$V_{x'y'} = P \quad I_1(R_1 + KR_A) + \quad (34)$$
$$I_4(R_2 + KR_C) \quad - I_4 R_2$$

Now assume that all the lower ratio CT's do not exist, and all the higher voltage CT's are connected in parallel as shown in Figure 26. Calculate the voltage across xy for three phase and single phase to ground faults just off bus on each of the higher rated circuits in turn. This voltage is determined by equation (35)

$$V_{xy} = I_1(R_2 + R_3 + R_4 + 2R_C) \quad (35)$$

where:

I_1 = fault current being pushed through saturated fault CT.

The pickup setting of the relay will be twice the higher of the three voltages in equations (33), (34) and (35).

When calculating the minimum internal fault current required to trip the relay equation (36) should be used.

$$i_{F(min)} = N' \quad i_R + i_{Thyrite} + \sum_{n=1}^{X_1} I_{E_n} + \quad (36)$$
$$\sum_{n=1}^{X2} K' I_{E_n}$$

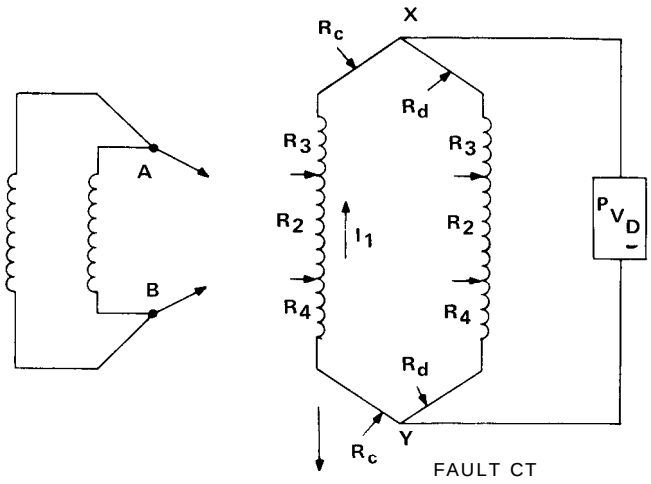


Figure 26

where:

X_2 = number of higher ratio CT's

X_1 = number of lower ratio CT's

K' = the ratio of the lower to the higher CT rating

N' = secondary turns of higher ratio CT's

In this instance the pickup setting of the PVD must not exceed the E_s value of the poorest higher ratio CT, nor 1/K' times the E_s value of the poorest lower ratio CT.

TYPICAL APPLICATIONS

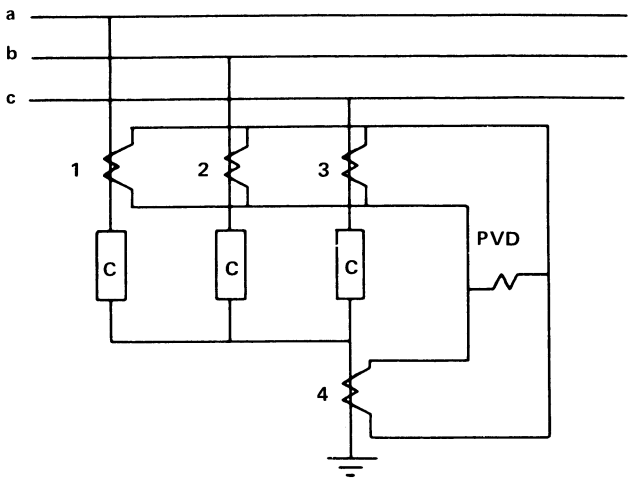


Figure 27

There are two categories for PVD applications, and these are (1) bus protection and (2) "other". Well over 90 percent of all PVD's in service will be found in bus differential schemes. For bus protection the PVD is applied per phase necessitating 3 relays for each bus section. The considerations for PVD use in a bus differential scheme have been discussed throughout the foregoing text.

Since the PVD scheme is a true current differential scheme other applications exist and a few of these will be mentioned. The applications other than bus protection may be termed unit-type protection. A diagram of a generalized unit-type scheme is shown in Figure 27.

In this case the CT labeled 4 need not be the type that has negligible leakage reactance since tripping for an external fault on line 4 is not objectionable. The pickup setting of the PVD may be based on the maximum external fault current on either line 1, 2 or 3 utilizing previously stated equations. The possibly high leakage reactance of CT #4 added to the secondary winding resistance and lead resistance may result in a voltage across the PVD during an external fault on line 4 higher than the calculated pickup setting. However, this is certainly not harmful and may be beneficial.

The Y connected windings, labeled C, may be legs of a shunt reactor bank or the Y grounded windings of a Δ - Y transformer. In the case of this unit-type application protection is afforded only for ground faults, and in the particular case of the transformer other protection must be provided for turn to turn faults.

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