GE VERNOVA

MiCOM P40 Agile

P342, P343, P344, P345, P346, P348 & P391

Technical Manual
Generator Protection Relay

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SAFETY SECTION

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1. OVERVIEW

This chapter provides information about the safe handling of the equipment. The equipment must be properly installed and handled in order to maintain it in a safe condition and to keep personnel safe at all times. You must be familiar with information contained in this chapter before unpacking, installing, commissioning, or servicing the equipment.

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2. HEALTH AND SAFETY

Personnel associated with the equipment must be familiar with the contents of this Safety Information.

When electrical equipment is in operation, dangerous voltages are present in certain parts of the equipment. Improper use of the equipment and failure to observe warning notices will endanger personnel.

Only qualified personnel may work on or operate the equipment. Qualified personnel are individuals who are:

- familiar with the installation, commissioning, and operation of the equipment and the system to which it is being connected.
- familiar with accepted safety engineering practises and are authorised to energise and de-energise equipment in the correct manner.
- trained in the care and use of safety apparatus in accordance with safety engineering practises
- trained in emergency procedures (first aid).

The documentation provides instructions for installing, commissioning and operating the equipment. It cannot, however cover all conceivable circumstances. In the event of questions or problems, do not take any action without proper authorisation. Please contact your local sales office and request the necessary information.

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3. SYMBOLS

Throughout this manual you will come across the following symbols. You will also see these symbols on parts of the equipment.



Refer to equipment documentation. Failure to do so could result in damage to the equipment



Risk of electric shock



Earth terminal. Note: This symbol may also be used for a protective conductor (earth) terminal if that terminal is part of a terminal block or sub-assembly.



Protective conductor (earth) terminal



Instructions on disposal requirements



The term 'Earth' used in this manual is the direct equivalent of the North American term 'Ground'.

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4. INSTALLING, COMMISSIONING AND SERVICING

4.1 Lifting Hazards

Many injuries are caused by:

- Lifting heavy objects
- Lifting things incorrectly
- Pushing or pulling heavy objects
- Using the same muscles repetitively

Plan carefully, identify any possible hazards and determine how best to move the product. Look at other ways of moving the load to avoid manual handling. Use the correct lifting techniques and Personal Protective Equipment (PPE) to reduce the risk of injury.

4.2 Electrical Hazards



All personnel involved in installing, commissioning, or servicing this equipment must be familiar with the correct working procedures.



Consult the equipment documentation before installing, commissioning, or servicing the equipment.



Always use the equipment as specified. Failure to do so will jeopardise the protection provided by the equipment.



Removal of equipment panels or covers may expose hazardous live parts. Do not touch until the electrical power is removed. Take care when there is unlocked access to the rear of the equipment.



Isolate the equipment before working on the terminal strips.



Use a suitable protective barrier for areas with restricted space, where there is a risk of electric shock due to exposed terminals.



Disconnect power before disassembling. Disassembly of the equipment may expose sensitive electronic circuitry. Take suitable precautions against electrostatic voltage discharge (ESD) to avoid damage to the equipment.



NEVER look into optical fibres or optical output connections. Always use optical power meters to determine operation or signal level.



Testing may leave capacitors charged to dangerous voltage levels. Discharge capacitors by reducing test voltages to zero before disconnecting test leads.



Operate the equipment within the specified electrical and environmental limits.



Before cleaning the equipment, ensure that no connections are energised. Use a lint free cloth dampened with clean water.



Contact fingers of test plugs are normally protected by petroleum jelly, which should not be removed.

4.3 UL/CSA/CUL Requirements

The information in this section is applicable only to equipment carrying UL/CSA/CUL markings.



Equipment intended for rack or panel mounting is for use on a flat surface of a Type 1 enclosure, as defined by Underwriters Laboratories (UL).



To maintain compliance with UL and CSA/CUL, install the equipment using UL/CSA-recognised parts for: cables, protective fuses, fuse holders and circuit breakers, insulation crimp terminals, and replacement internal batteries.

4.4 Fusing Requirements



Where UL/CSA listing of the equipment is required for external fuse protection, a UL or CSA Listed fuse must be used for the auxiliary supply. The listed protective fuse type is: Class J time delay fuse, with a maximum current rating of 15 A and a minimum DC rating of 250 V dc (for example type AJT15).



Where UL/CSA listing of the equipment is not required, a high rupture capacity (HRC) fuse type with a maximum current rating of 16 Amps and a minimum dc rating of 250 V dc may be used for the auxiliary supply (for example Red Spot type NIT or TIA).
For P50 models, use a 1A maximum T-type fuse.
For P60 models, use a 4A maximum T-type fuse.



Digital input circuits should be protected by a high rupture capacity NIT or TIA fuse with maximum rating of 16 A. for safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.

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CTs must NOT be fused since open circuiting them may produce lethal hazardous voltages

4.5 Equipment Connections



Terminals exposed during installation, commissioning and maintenance may present a hazardous voltage unless the equipment is electrically isolated.

Tighten M4 clamping screws of heavy duty terminal block connectors to a nominal torque of 1.3 Nm.
Tighten captive screws of terminal blocks to 0.5 Nm minimum and 0.6 Nm maximum.

Always use insulated crimp terminations for voltage and current connections.

Always use the correct crimp terminal and tool according to the wire size.

Watchdog (self-monitoring) contacts are provided to indicate the health of the device on some products. We strongly recommend that you hard wire these contacts into the substation's automation system, for alarm purposes.

4.6 Protection Class 1 Equipment Requirements

Earth the equipment with the supplied PCT (Protective Conductor Terminal).

Do not remove the PCT.

The PCT is sometimes used to terminate cable screens. Always check the PCT's integrity after adding or removing such earth connections.

Use a locknut or similar mechanism to ensure the integrity of stud-connected PCTs.



The recommended minimum PCT wire size is 2.5 mm² for countries whose mains supply is 230 V (e.g. Europe) and 3.3 mm² for countries whose mains supply is 110 V (e.g. North America). This may be superseded by local or country wiring regulations.
For P60 products, the recommended minimum PCT wire size is 6 mm². See product documentation for details.



The PCT connection must have low-inductance and be as short as possible.



All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should be earthed, or connected to a common grouped potential.

4.7 Pre-energisation Checklist



Check voltage rating/polarity (rating label/equipment documentation).



Check CT circuit rating (rating label) and integrity of connections.



Check protective fuse or miniature circuit breaker (MCB) rating.



Check integrity of the PCT connection.



Check voltage and current rating of external wiring, ensuring it is appropriate for the application.

4.8 Peripheral Circuitry



Do not open the secondary circuit of a live CT since the high voltage produced may be lethal to personnel and could damage insulation. Short the secondary of the line CT before opening any connections to it.



For most General Electric equipment with ring-terminal connections, the threaded terminal block for current transformer termination is automatically shorted if the module is removed. Therefore external shorting of the CTs may not be required. Check the equipment documentation and wiring diagrams first to see if this applies.



Where external components such as resistors or voltage dependent resistors (VDRs) are used, these may present a risk of electric shock or burns if touched.

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Take extreme care when using external test blocks and test plugs such as the MMLG, MMLB and P990, as hazardous voltages may be exposed. Ensure that CT shorting links are in place before removing test plugs, to avoid potentially lethal voltages.

4.9 Upgrading/Servicing



Do not insert or withdraw modules, PCBs or expansion boards from the equipment while energised, as this may result in damage to the equipment. Hazardous live voltages would also be exposed, endangering personnel.



Internal modules and assemblies can be heavy and may have sharp edges. Take care when inserting or removing modules into or out of the IED.

5. DECOMMISSIONING AND DISPOSAL



Before decommissioning, completely isolate the equipment power supplies (both poles of any dc supply). The auxiliary supply input may have capacitors in parallel, which may still be charged. To avoid electric shock, discharge the capacitors using the external terminals before decommissioning.



Avoid incineration or disposal to water courses. Dispose of the equipment in a safe, responsible and environmentally friendly manner, and if applicable, in accordance with country-specific regulations.

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6. REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.

CE

6.1 EMC Compliance: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

6.2 LVD Compliance: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

6.3 R&TTE Compliance: 2014/53/EU

Radio and Telecommunications Terminal Equipment (R&TTE) directive 2014/53/EU.

Conformity is demonstrated by compliance to both the EMC directive and the Low Voltage directive, to zero volts.

6.4 UL/CUL Compliance

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.

c UL us

6.5 ATEX Compliance: 2014/34/EU

Products marked with the 'explosion protection' Ex symbol (shown in the example, below) are compliant with the ATEX directive. The product specific Declaration of Conformity (DoC) lists the Notified Body, Type Examination Certificate, and relevant harmonized standard or conformity assessment used to demonstrate compliance with the ATEX directive.

The ATEX Equipment Protection level, Equipment group, and Zone definition will be marked on the

product.

For example:

Ex II (2) G

Where:

'II' Equipment Group: Industrial.

'(2)G' High protection equipment category, for control of equipment in gas atmospheres in Zone 1 and 2. This equipment (with parentheses marking around the zone number) is not itself suitable for operation within a potentially explosive atmosphere.

IT

INTRODUCTION

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 DOCUMENTATION STRUCTURE

The manual provides a functional and technical description of General Electric's P34x protection relay. It also provides a comprehensive set of instructions for the relay's use and application.

The chapter contents are summarised below:

P34x/EN IT Introduction

A guide to the range of relays and the documentation structure. General safety aspects of handling Electronic Equipment is discussed with particular reference to relay safety symbols. Also a general functional overview of the relay and brief application summary is given.

P34x/EN TD Technical Data

Technical data including setting ranges, accuracy limits, recommended operating conditions, ratings and performance data. Compliance with norms and international standards is quoted where appropriate.

P34x/EN GS Getting Started

A guide to the different user interfaces of the protection relay describing how to start using it. This chapter provides detailed information regarding the communication interfaces of the relay, including a detailed description of how to access the settings database stored within the relay.

P34x/EN ST Settings

List of all relay settings, including ranges, step sizes and defaults, together with a brief explanation of each setting.

P34x/EN OP Operation

A comprehensive and detailed functional description of all protection and non-protection functions.

P34x/EN AP Application Notes

This chapter includes a description of common power system applications of the relay, calculation of suitable settings, some typical worked examples, and how to apply the settings to the relay.

P34x/EN PL Programmable Logic

Overview of the programmable scheme logic and a description of each logical node. This chapter includes the factory default (PSL) and an explanation of typical applications.

P34x/EN MR Measurements and Recording

Detailed description of the relays recording and measurements functions including the configuration of the event and disturbance recorder and measurement functions.

P34x/EN FD Firmware Design

Overview of the operation of the relay's hardware and software. This chapter includes information on the self-checking features and diagnostics of the relay.

P34x/EN CM Commissioning

Instructions on how to commission the relay, comprising checks on the calibration and functionality of the relay.

P34x/EN MT Maintenance

A general maintenance policy for the relay is outlined.

P34x/EN TS Troubleshooting

Advice on how to recognise failure modes and the recommended course of action. Includes guidance on whom within General Electric to contact for advice.

P34x/EN SC SCADA Communications

This chapter provides an overview regarding the SCADA communication interfaces of the relay. Detailed protocol mappings, semantics, profiles and interoperability tables are not provided within this manual. Separate documents are available per protocol, available for download from our website.

P34x/EN CS Cybersecurity

This chapter includes a description of the cybersecurity features of the relay and compliance to NERC and other standards.

P34x/EN SG Symbols and Glossary

List of common technical abbreviations found within the product documentation.

P34x/EN IN Installation

Recommendations on unpacking, handling, inspection and storage of the relay. A guide to the mechanical and electrical installation of the relay is provided, incorporating earthing recommendations. All external wiring connections to the relay are indicated.

P34x/EN VH Firmware and Service Manual Version History

History of all hardware and software releases for the product.

2 INTRODUCTION TO MiCOM

MiCOM is a comprehensive solution capable of meeting all electricity supply requirements. It comprises a range of components, systems and services from General Electric.

Central to the MiCOM concept is flexibility.

MiCOM provides the ability to define an application solution and, through extensive communication capabilities, integrate it with your power supply control system.

The components within MiCOM are:

- P range protection relays;
- C range control products;
- M range measurement products for accurate metering and monitoring;
- S range versatile PC support and substation control packages.

Our products include extensive facilities for recording information on the state and behavior of the power system using disturbance and fault records. They can also provide measurements of the system at regular intervals to a control center enabling remote monitoring and control to take place.

For up-to-date information on any MiCOM product, visit our website:

https://www.gevernova.com/grid-solutions

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3 PRODUCT SCOPE

The P342/3/4/5/6/8 generator protection relays have been designed for the protection of a wide range of generators.

The P342 is suitable for protection of small to medium size generators (1-10 MVA) or can be used as back-up protection for larger generators.

The P343 is suitable for protection of medium to large size generators (>10 MVA) or more important generators, providing generator differential, 100% stator earth fault via a 3rd harmonic measuring technique, pole slipping and unintentional energisation at standstill protection in addition to the features of the P342.

The P344 is similar to the P343 but includes a second neutral voltage input for earth fault/interturn protection.

The P345 is suitable for protection of large generators (>50 MVA) providing 100% stator earth fault protection via a low frequency injection technique in addition to the features of the P344.

The P346 is suitable for the protection of medium to large size generators and is the same as the P343 but without 100% stator earth fault, pole slipping and dead machine protection.

The P348 is suitable for the protection of large variable speed DFI (Double Fed Induction) machines for pumped storage plants. For these machines low frequency currents are supplied to the rotor by means of VSC (Voltage Source Converter) power electronic converters from the AC system. During normal operation the frequency of the rotor currents is very low, during start up and breaking it varies from zero to rated grid frequency. To measure the low frequency current and voltage signals new cutting edge “Digital Substation” technology incorporating Non-Conventional Instrument Transformers (NCIT) with IEC 61850 9-2 LE process bus communications to the protection relays is used.

The P348 provides protection for the rotor from extremely low frequencies (0.1Hz) to higher power system frequencies (70Hz). The P348 also provides protection for the stator during starting from 0.1Hz to 70Hz, below the 5Hz lower limit of the standard P342-6 protection relays.

The P343/4/5/6/8 also includes 10 function keys for integral scheme or operator control functionality and tri-color (red/yellow/green) LEDs. Rotor earth fault protection is provided by the P391 low frequency square wave injection, coupling and measurement unit connected to the rotor circuit. The measurement of the rotor resistance is passed to the P342/3/4/5/6 via a current loop output (0-20 mA) on the P391 connected to one of the 4 current loop inputs on the P342/3/4/5/6. The rotor ground fault protection is only available if the relay includes the CLIO hardware option.

3.1 Functional overview

The P342/3/4/5 generator protection relays contain a wide variety of protection functions. The protection features are summarized below:

PROTECTION FUNCTIONS OVERVIEW		P34x
87	Two types of differential protections are provided in P343/4/5/6, (1) generator differential protection and (2) generator - transformer protection. 1. Phase segregated generator differential protection is provided for high speed discriminative protection for all fault types. The differential protection can be selected as biased or high impedance or interturn. 2. Phase-segregated generator-transformer biased differential protection is provided for high-speed discriminative protection for all fault types. The differential protection includes ratio and vector compensation and 2nd/5th harmonic blocking for magnetizing inrush conditions.	3/4/5/6

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PROTECTION FUNCTIONS OVERVIEW		P34x
64	Restricted earth fault is configurable as a high impedance or a biased low impedance element. This can be used to provide high speed earth fault protection and is mainly applicable to small machines where differential protection is not possible or for transformer applications. The CT input is selectable as IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 via a setting.	2/3/4/5/6
32P/Q	Four definite time stages of power/VAr protection are provided and each stage can be independently configured to operate as under/over and forward/reverse. The power protection can be used to provide simple back-up overload protection (Overpower), protection against motoring (Reverse Power), CB interlocking to prevent overspeeding during machine shutdown (Low Forward Power) and motor loss of load protection (Low Reverse Power). The reverse VAr protection can be used to provide simple under excitation protection. The P342-6 relays provide a standard 3 phase power/VAr protection element and also a single phase sensitive power/VAr protection element. The P345 sensitive power protection can be a single or wattmetric power/VAr element. The sensitive power/VAr protection can be used with dedicated metering class CTs using the sensitive current inputs (1 for single phase or 2 for wattmetric).	2/3/4/5/6
40	A two stage offset mho definite time impedance element with a supervising directional line is provided to detect failure of the machine excitation. A power factor alarm element is also available to offer more sensitive protection.	2/3/4/5/6
46T	Negative phase sequence thermal overload protection is provided to protect against unbalanced loading which can cause overheating in the rotor. Both alarm and trip stages are provided.	2/3/4/5/6
51V, 21	A voltage dependent overcurrent (controlled or restrained) or underimpedance protection is provided for back-up protection of phase faults. The voltage dependent overcurrent protection may be set as controlled or restrained with an Inverse Definite Minimum Time (IDMT) or Definite Time (DT). There are 2 stages of underimpedance protection which may be set as definite time only.	2/3/4/5/6
50/51/67	Four overcurrent protection stages are provided which can be selected to be either non-directional, directional forward or directional reverse. Stages 1 and 2 may be set Inverse Definite Minimum Time (IDMT) or Definite Time (DT); stages 3 and 4 may be set DT only. The CT input is selectable as IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 via a setting.	2/3/4/5/6
50/51S 50/51R	Four Peak sampled value (SV) overcurrent protection stages and four RMS overcurrent protection stages are provided for stator and rotor overcurrent protection. The RMS overcurrent stages 1 and 2 may be set as Inverse Definite Minimum Time (IDMT) or Definite Time (DT) or as a programmable User Curve; stages 3 and 4 may be set DT only. The Peak overcurrent stages are all Definite Time (DT). The CT input is selectable as IA-1/IB-1/IC-1 (rotor) or IA-2/IB-2/IC-2 (stator) via a setting.	8
46OC	Four definite time stages of negative phase sequence overcurrent protection are provided for remote back-up protection for both phase to earth and phase to phase faults. Each stage can be selected to be either non-directional, directional forward or directional reverse. The CT input is selectable as IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 via a setting.	2/3/4/5/6
46S	Four definite time stages of RMS negative phase sequence overcurrent protection are provided for stator protection.	8
49G	Generator thermal overload protection based on I1 and I2 is provided to protect the stator/rotor against overloading due to balanced and unbalanced currents. Both alarm and trip stages are provided.	2/3/4/5/6

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PROTECTION FUNCTIONS OVERVIEW		P34x
49T	Transformer thermal overload protection is provided based on IEEE Std C57.91-1995. The thermal trip can be based on either hot spot or top oil temperature, each with three time-delayed stages available.	2/3/4/5/6
50N/51N	Two stages of non-directional earth fault protection are provided for stator earth fault protection. Stage 1 may be set Inverse Definite Minimum Time (IDMT) or Definite Time (DT); stage 2 may be set DT only.	2/3/4/5/6
64R	Rotor earth fault protection can be provided by a low frequency injection method. There are 2 stages of definite time under resistance protection. An external injection, coupling and measurement unit (P391) is required with this function. The measurement of the rotor resistance is passed to the P34x via a current loop output (0-20 mA) on the P391 connected to one of the 4 current loop inputs on the P34x. The rotor ground fault protection is only available if the relay includes the CLIO hardware option. The injection frequency is selectable 0.25/0.5/1 Hz via a jumper link in the P391	2/3/4/5/6
67N/67W	One sensitive earth fault element is provided for discriminative earth fault protection of parallel generators. The protection can be selected to be either non-directional, directional forward or directional reverse. Either Zero sequence or negative sequence polarizing is available. The Sensitive Earth Fault element can be configured as an $I\cos\phi$, $I\sin\phi$ or $VI\cos\phi$ (Wattmetric) element for application to isolated and compensated networks.	2/3/4/5/6
59N	Residual overvoltage protection is available for stator earth fault protection where there is an isolated or high impedance earth. The residual voltage can be measured from a broken delta VT, from the secondary winding of a distribution transformer earth at the generator neutral, or can be calculated from the three phase to neutral voltage measurements. Two independent stages of protection are provided for each measured neutral voltage input and also for the calculated value, each stage can be selected as either IDMT or DT. The P342/3/4/5 have 2 measured and 2 calculated stages of residual overvoltage protection. The P344/5 has an additional neutral voltage input and so has an additional 2 stages of measured residual overvoltage protection.	2/3/4/5/6
59NR	RMS residual overvoltage protection is available for rotor earth fault protection where the rotor is high impedance earthed. The RMS residual voltage is calculated from the three phase to neutral voltage measurements. Two independent RMS stages of protection are provided. Each stage can be selected as either DT or IDMT or a programmable user curve.	8
27TN/59TN	A 3rd harmonic voltage element is provided to detect earth fault close to the generator star point. This element combined with the standard stator earth fault protection (59N/50N/51N) provides 100% stator earth fault protection. A definite time 3rd harmonic undervoltage element is provided if neutral voltage measurement is available at the neutral of the machine. This element is supervised by a 3 phase undervoltage element and optionally by 3 phase W/VA/VAr elements. A 3rd harmonic overvoltage element is provided if neutral voltage measurement is available from the terminals of the machine.	2/3/4/5
64S	100% stator earth fault protection can also be provided by a low frequency injection method. There are 2 stages of definite time under resistance protection and 1 stage of definite time overcurrent protection. An external 20 Hz generator and bandpass filter is required with this function.	5

PROTECTION FUNCTIONS OVERVIEW		P34x
24	A five stage overfluxing (V/Hz) element is provided to protect the generator, or connected transformer, against overexcitation. The first stage is a definite time alarm, the second stage can be used to provide an inverse or definite time trip characteristic and stages 3/4/5 are definite time.	2/3/4/5/6
81R	A 4-stage rate of change of frequency element (df/dt) is provided for Loss of Mains/Grid and load shedding applications.	2/3/4/5/6
50/27	A voltage supervised overcurrent scheme is provided for dead machine/generator unintentional energisation at standstill (GUESS) protection to detect if the machine circuit breaker is closed accidentally, when the machine is not running. The CT input is selectable as IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 via a setting.	2/3/4/5
27	A 3 stage undervoltage protection element, configurable as either phase to phase or phase to neutral measuring is provided to back up the automatic voltage regulator. Stage 1 may be selected as either IDMT or DT and stage 2 and 3 are DT only.	2/3/4/5/6
59	A 2 stage overvoltage protection element, configurable as either phase to phase or phase to neutral measuring is provided to back up the automatic voltage regulator. Stage 1 may be selected as either IDMT or DT and stage 2 is DT only.	2/3/4/5/6
59R	A 4 stage overvoltage protection element, with 2 Peak sampled value (SV) and 2 RMS stages, configurable as either phase to phase or phase to neutral measuring is provided for rotor overvoltage protection. The first stage of Peak/RMS protection may be selected as either DT or IDMT or a programmable user curve and the second stage of Peak/RMS protection is DT only.	8
47	A definite time negative phase sequence overvoltage protection element is provided for either a tripping or interlocking function upon detection of unbalanced supply voltages.	2/3/4/5/6
81U/O	A 4 stage definite time underfrequency and 2 stage definite time overfrequency protection is provided for load shedding and back-up protection of the speed control governor.	2/3/4/5/6
81OR	A 4 stage definite time overrfrequency protection is provided for back-up protection for excessive rotor slip.	8
81AB	Turbine abnormal frequency protection is provided to protect the turbine blade from potential damage due to prolonged under/overfrequency operation of the generator. Up to six frequency bands can be programmed, each having an integrating timer to record the time spent within the band.	2/3/4/5/6
RTD	10 RTDs (PT100) are provided to monitor the temperature accurately in the windings and bearings of the machine. Each RTD has an instantaneous alarm and definite time trip stage.	Option 2/3/4/5/6
50BF	A 2 stage circuit breaker failure function is provided with a 3 pole initiation input from external protection.	2/3/4/5/6
37P/37N	Phase, neutral and sensitive earth fault undercurrent elements are available for use with for example the circuit breaker fail function.	2/3/4/5/6
78	A lens shaped impedance characteristic is used to detect loss of synchronization (pole slipping) between the generation and the power system. Two zones are created by a reactance line which is used to distinguish whether the impedance centre of the pole slip is located in the power system or in the generator. Separate counters are used to count pole slips in the 2 zones. A setting is also provided to determine whether the protection operates in a generating mode, motoring mode or both.	2/3/4/5
BOL	Blocked overcurrent logic is available on each stage of the overcurrent, earth fault and sensitive earth fault protection. This consists of start outputs and block inputs that can be used to implement busbar blocking schemes for example.	2/3/4/5/6

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PROTECTION FUNCTIONS OVERVIEW		P34x
VTS	Voltage transformer supervision is provided (1, 2 & 3 phase fuse failure detection) to prevent mal-operation of voltage dependent protection elements on loss of a VT input signal.	2/3/4/5/6/8
CTS	Current transformer supervision is provided to prevent mal-operation of current dependent protection elements upon loss of a CT input signal.	2/3/4/5/6/8
CLIO	4 analog (or current loop) inputs are provided for transducers (vibration, tachometers etc.). Each input has a definite time trip and alarm stage and each input can be set to operate for 'Over' or 'Under' operation. Each input can be independently selected as 0-1/0-10/0-20/4-20 mA. 4 analogue (or current loop) outputs are provided for the analogue measurements in the relay. Each output can be independently selected as 0-1/0-10/0-20/4-20 mA.	Option 2/3/4/5/6/8
25	Check synchronizing (2-stage) with advanced system split features and breaker closing compensation time is provided. The P345 includes a dedicated voltage input for check synchronizing. For the P344 the VN2 input can be used for neutral voltage protection or check synchronizing. For the P342/3 the VN1 input can be used for neutral voltage protection or check synchronizing.	2/3/4/5/6
	Phase rotation - the rotation of the phases ABC or ACB for all 3 phase current and voltage channels can be selected. Also, for pumped storage applications where 2 phases are swapped the swapping of 2 phases can be emulated independently for the 3 phase voltage and 3 phase current channels.	2/3/4/5/6
	Programmable function keys	10 (P343/4/5/6/8)
	Programmable LEDs (tri-color P343/4/5/6, red P342)	18 (P343/4/5/6/8) 8 (P342)
	Digital inputs (order option)	7 to 32
	Output relays (order option)	8 to 32
	Front communication port (EIA(RS)232)	2/3/4/5/6/8
	Rear communication port (KBUS/EIA(RS)485). The following communications protocols are supported; Courier, MODBUS, IEC870-5-103 (VDEW) and DNP3.0.	2/3/4/5/6/8
	Rear communication port (Fibre Optic). The following communications protocols are supported; Courier, MODBUS, IEC870-5-103 (VDEW) and DNP3.0.	Option 2/3/4/5/6/8
	Second rear communication port (EIA(RS)232/EIA(RS)485). Courier protocol.	Option 2/3/4/5/6/8
	Rear IEC 61850/DNP3.0 Ethernet communication port.	Option 2/3/4/5/6/8
	Rear redundant IEC 61850/DNP3.0 Ethernet communication port	Option 2/3/4/5/6/8
	Time synchronization port (IRIG-B)	Option 2/3/4/5/6/8

Table 1: Functional overview

The P34x supports the following relay management functions in addition to the functions shown above.

- Measurement of all instantaneous & integrated values
- Circuit breaker control, status & condition monitoring
- Trip circuit and coil supervision
- 4 Alternative setting groups
- Programmable function keys (P343/4/5/6/8)
- Control inputs

IT

- Programmable scheme logic
- Programmable allocation of digital inputs and outputs
- Sequence of event recording
- Comprehensive disturbance recording (waveform capture)
- Fault recording
- Fully customizable menu texts
- Multi-level password protection
- Power-up diagnostics and continuous self-monitoring of relay
- Commissioning test facilities
- Real time clock/time synchronization - time synchronization possible from IRIG-B input, opto input or communications

Application overview

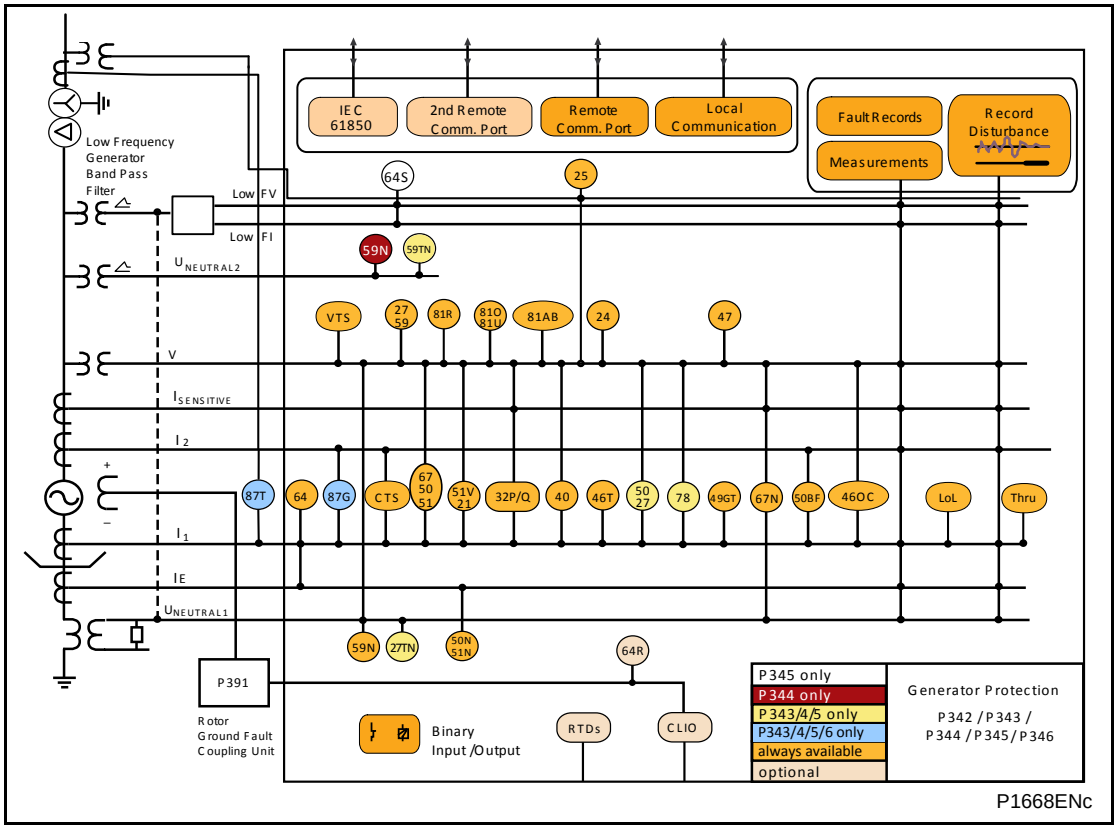


Figure 1: Functional diagram (P342 - 6 only)

IT

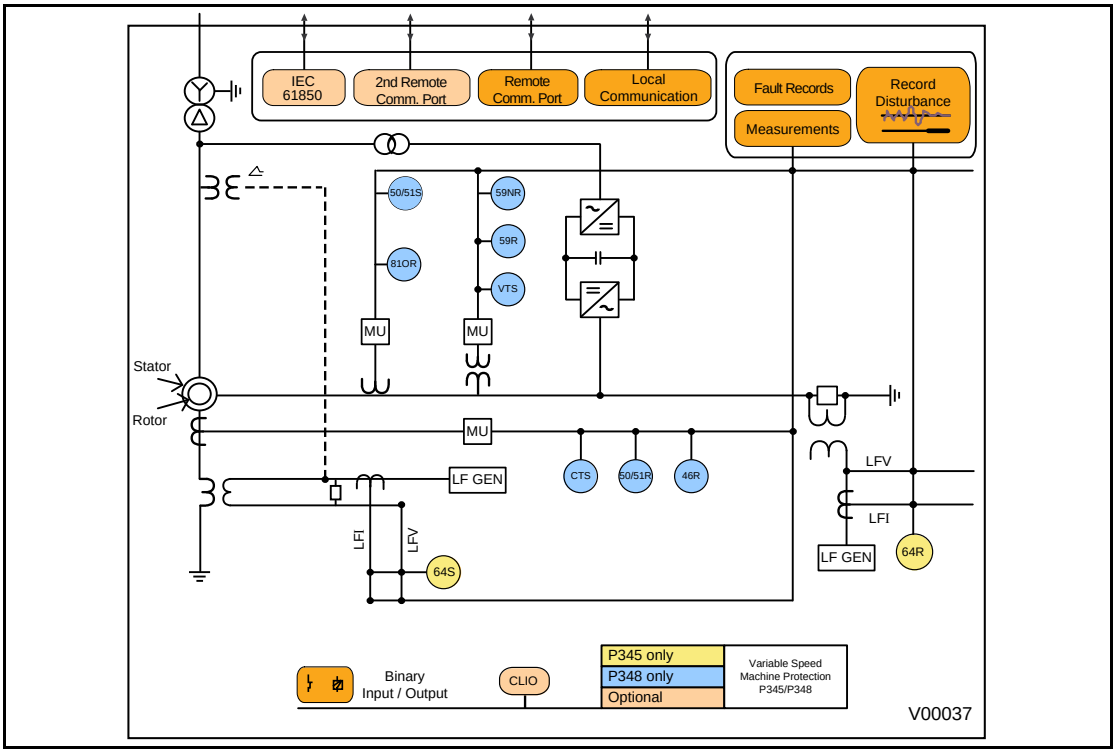


Figure 2: Functional diagram (P348 only)

3.2 Ordering options

Information required with order

Variants Order No.			P342											
Generator Protection Relay												**		
Design Suffix														
As J plus increased main processor memory (CPU3)														P
Phase 2 CPU and front panel with 2 hotkeys and dual characteristic optos														J
Improved power supply														C
Universal Optos, Low Powered Relay Outputs														B
Vx Auxiliary Rating														
24 - 54Vdc									7					
48 - 125Vdc (40 - 100Vac)									8					
110 - 250Vdc, 100 - 240Vac									9					
In/Vn Rating														
In = 1/5A, Vn = 100 - 120Vac										1				
In = 1/5A, Vn = 380 - 480Vac										2				
Hardware Options	Protocol Compatibility	Design Suffix Compatibility												
Standard - None	1, 2, 3 & 4	All								1				
IRIG-B Only (modulated)	1, 2, 3 & 4	All								2				
Fibre Optic Converter Only	3	All								3				
	1, 2 & 4	J & P												
IRIG-B (modulated) & Fibre Optic Converter	3	All								4				
	1, 2 & 4	J & P												
Ethernet (100Mbit/s)	6, 8	J & P *								6				
2nd Rear Comms	1, 2, 3 & 4	B, C or J & P								7				
IRIG-B (modulated) & 2nd Rear Comms	1, 2, 3 & 4	B, C or J & P								8				
Ethernet (100Mbit/s) plus IRIG-B (modulated)	6, 8	J & P *								A				
Ethernet (100Mbit/s) plus IRIG-B (un-modulated)	6, 8	J & P *								B				
IRIG-B (un-modulated)	1, 2, 3 & 4	J & P *								C				
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	J & P **								G				
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	J & P **								H				
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	J & P **								J				
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	J & P **								K				
Redundant Ethernet Dual Homing Star, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	J & P **								L				
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	J & P **								M				
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	J & P ***								N				
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	J & P ***								P				

* NB: Options are only available with software version 32 and later
** Options are only available with software version 35 and later
*** Options are only available with software version 36 and later

Product Specific Option														
40TE Case, 8 Opto Inputs + 7 Relay Outputs										A				
40TE Case, 8 Opto Inputs + 7 Relay Outputs + RTD										B				
40TE Case, 8 Opto Inputs + 7 Relay Outputs + CLIO										C				
40TE Case, 16 Opto Inputs + 7 Relay Outputs										D				
40TE Case, 8 Opto Inputs + 15 Relay Outputs										E				
40TE Case, 12 Opto Inputs + 11 Relay Outputs										F				
60TE Case, 16 Opto Inputs + 16 Relay Outputs										G				
60TE Case, 16 Opto Inputs + 16 Relay Outputs + RTD										H				
60TE Case, 16 Opto Inputs + 16 Relay Outputs + CLIO										J				
60TE Case, 24 Opto Inputs + 16 Relay Outputs										K				
60TE Case, 16 Opto Inputs + 24 Relay Outputs										L				
60TE Case, 16 Opto Inputs + 16 Relay Outputs + RTD + CLIO										M				
60TE Case, 24 Opto Inputs + 16 Relay Outputs + RTD										N				
60TE Case, 16 Opto Inputs + 24 Relay Outputs + RTD										P				
40TE Case, 8 Opto Inputs + 11 Relay Outputs (Including 4 High Break)										Q				
60TE Case, 16 Opto Inputs + 20 Relay Outputs (Including 4 High Break)										R				
60TE Case, 16 Opto Inputs + 12 Relay Outputs (Including 4 High Break) + RTD										S				
60TE Case, 16 Opto Inputs + 12 Relay Outputs (Including 4 High Break) + CLIO										T				
60TE Case, 16 Opto Inputs + 12 Relay Outputs (Including 4 High Break) + RTD + CLIO										U				
Protocol / Communications Options	Hardware Compatibility	Design Suffix Compatibility												
K-Bus	1 & 2	All									1			
	7 & 8	B, C, J or P												
	3, 4 & C	J & P												
Modbus	1 & 2	All									2			
	7 & 8	B, C, J or P												
	3, 4 & C	J & P												
IEC 60870-5-103 (VDEW)	1, 2, 3 & 4	All									3			
	7 & 8	B, C, J or P												
	C	J & P												
DNP3.0	1 & 2	All									4			
	7 & 8	B, C, J or P												
	3, 4 & C	J & P												
IEC61850 + Courier (via rear RS485 port)	6, A & B	J & P									6			
	G, H, J, K, L, M **	J & P												
	N, P ***	J & P												
DNP3.0 Over Ethernet with Courier rear port K-Bus/RS485 protocol	6, A, B, G, H, J, K, L, M, N, P ****	P only									8			

* Options are only available with software version 32 and later
**Options only available with software version 35 and later
***Options only available with software version 36 and later
**** Options only available with software version 37 and later

Mounting Option														
Flush Panel Mounting, with harsh environment coating												M		
Order FX0021001 if rack mounting is required														
Multilingual Language Option														
English, French, German, Spanish													0	
English, French, German, Russian													5	
Chinese, English or French via HMI, with English or French only via Communications port													C	
Software Issue														**
Customisation														
Default														0
Customer														A

IT

Variants Order No.

Generator Protection Relay with Differential — P343 **

Design Suffix

As K plus increased main processor memory (XCPU3)	M
Extended Phase 2 CPU (phase 2 CPU and front panel with 10 function keys and tri-color LEDs and dual characteristic optos)	K
Phase 2 CPU and front panel with 2 hotkeys and dual characteristic optos	J
Improved power supply	C
Universal Optos, Low Powered Relay Outputs	B

Vx Auxiliary Rating

24 - 54Vdc	7
48 - 125Vdc (40 - 100Vac)	8
110 - 250Vdc, 100 - 240Vac	9

In/Vn Rating

In = 1/5A, Vn = 100 - 120Vac	1
In = 1/5A, Vn = 380 - 480Vac	2

Hardware Options	Protocol Compatibility	Design Suffix Compatibility	
Standard - None	1, 2, 3 & 4	All	1
IRIG-B Only (modulated)	1, 2, 3 & 4	All	2
Fibre Optic Converter Only	3	All	3
	1, 2 & 4	J, K & M only	
IRIG-B (modulated) & Fibre Optic Converter	3	All	4
	1, 2 & 4	J, K & M only	
Ethernet (100Mbit/s)	6, 8	J, K & M only	6
2nd Rear Comms	1, 2, 3 & 4	B, C, J, K & M	7
IRIG-B (modulated) & 2nd Rear Comms	1, 2, 3 & 4	B, C, J & K	8
Ethernet (100Mbit/s) plus IRIG-B (modulated)	6, 8	J, K & M only *	A
Ethernet (100Mbit/s) plus IRIG-B (un-modulated)	6, 8	J, K & M only *	B
IRIG-B (un-modulated)	1, 2, 3 & 4	J, K & M only *	C
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	J, K & M only *	G
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	J, K & M only *	H
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	J, K & M only *	J
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	J, K & M only *	K
Redundant Ethernet Dual Homing Star, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	J, K & M only *	L
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	J, K & M only *	M
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	K & M only ***	N
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	K & M only ***	P

* Options are only available with software version 32 and later
** Options are only available with software version 35 and later
*** Options are only available with software version 36 and later

Product Specific Option

Size 60TE Case, No Option (16 Optos + 14 Relays)	A
Size 60TE Case, 16 Optos + 14 Relays + RTD	B
Size 60TE Case, 16 Optos + 14 Relays + CLIO	C
Size 60TE Case, 24 Optos + 14 Relays	D
Size 60TE Case, 16 Optos + 22 Relays	E
Size 80TE Case, 24 Optos + 24 Relays	F
Size 80TE Case, 24 Optos + 24 Relays + RTD	G
Size 80TE Case, 24 Optos + 24 Relays + CLIO	H
Size 80TE Case, 32 Optos + 24 Relays	J
Size 80TE Case, 24 Optos + 32 Relays	K
Size 80TE Case, 24 Optos + 24 Relays + RTD + CLIO	L
Size 80TE Case, 32 Optos + 24 Relays + RTD	M
Size 80TE Case, 24 Optos + 32 Relays + RTD	N
Size 80TE Case, 32 Optos + 16 Relays + RTD + CLIO	P
Size 80TE Case, 16 Optos + 32 Relays + RTD + CLIO	Q
Size 60TE Case, 16 Optos + 18 Relays (4 High Break)	R
Size 60TE Case, 16 Optos + 11 Relays (4 High Break)	S
Size 60TE Case, 16 Optos + 11 Relays (4 High Break) + CLIO	T
Size 80TE Case, 16 Optos + 24 Relays (8 High Break)	U
Size 80TE Case, 16 Optos + 24 Relays (8 High Break) + RTD	V
Size 80TE Case, 16 Optos + 24 Relays (8 High Break) + CLIO	W
Size 80TE Case, 16 Optos + 24 Relays (8 High Break) + RTD + CLIO	X

Protocol / Communications Options	Hardware Compatibility	Design Suffix Compatibility	
K-Bus	1 & 2	All	1
	7 & 8	B, C, J, K & M	
	3, 4 & C	J, K & M only *	
Modbus	1 & 2	All	2
	7 & 8	B, C, J, K & M	
	3, 4 & C	J, K & M only *	
IEC 60870-5-103 (VDEW)	1, 2, 3 & 4	All	3
	7 & 8	B, C, J, K & M	
	C	J, K & M only *	
DNP3.0	1 & 2	All	4
	7 & 8	B, C, J, K & M	
	3, 4 & C	J, K & M only **	
IEC61850 + Courier (via rear RS485 port)	6, A & B	J, K & M only **	6
	G, H, J, K, L, M	J, K & M only **	
	N, P	K & M only ***	
DNP3.0 Over Ethernet with Courier rear port K-Bus/RS485 protocol	6, A, B, G, H, J, K, L, M, N, P	M only ****	8

* Options are only available with software version 32 and later
**Options only available with software version 35 and later
***Options only available with software version 36 and later
***Option only available with software version 38 and later

Mounting Option

Flush Panel Mounting, with Harsh Environment Coating	M
Rack Panel Mounting, with Harsh Environment Coating (Size 80TE Case Only)	N

Multilingual Language Option

English, French, German, Spanish	0
English, French, German, Russian	5
Chinese, English or French via HMI, with English or French only via Communications port	C

Software Issue **

Customisation

Default	0
Customer	A

IT

| Variants Order No. | | | P344 | | |

IT

Variants Order No. P345 **

Generator Protection Relay

Design Suffix

As K plus increased main processor memory (XCPU3) — M

Extended Phase 2 CPU — K

Vx Auxiliary Rating

24 - 54Vdc — 7

48 - 125Vdc (40 - 100Vac) — 8

110 - 250Vdc, 100 - 240Vac — 9

In/Vn Rating

In = 1/5A, Vn = 100 - 120Vac — 1

In = 1/5A, Vn = 380 - 480Vac — 2

Hardware Options	Protocol Compatibility	Design Suffix Compatibility	
Standard - None	1, 2, 3 & 4	K/M	1
IRIG-B Only (modulated)	1, 2, 3 & 4	K/M	2
Fibre Optic Converter Only	1, 2, 3 & 4	K/M	3
IRIG-B (modulated) & Fibre Optic Converter	1, 2, 3 & 4	K/M	4
Ethernet (100Mbit/s)	6, 8	K/M	6
2nd Rear Comms	1, 2, 3 & 4	K/M	7
IRIG-B (modulated) & 2nd Rear Comms	1, 2, 3 & 4	K/M	8
Ethernet (100Mbit/s) plus IRIG-B (modulated)	6, 8	K/M	A
Ethernet (100Mbit/s) plus IRIG-B (un-modulated)	6, 8	K/M	B
IRIG-B (un-modulated)	1, 2, 3 & 4	K/M	C
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	K/M *	G
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	K/M *	H
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	K/M *	J
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	K/M *	K
Redundant Ethernet Dual Homing Star, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	K/M *	L
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	K/M *	M
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8	K/M **	N
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8	K/M **	P

* Options are only available with software version 35 and later

** Options are only available with software version 36 and later

Product Specific Option

Size 16 Case, No Option (24 Opto Inputs + 24 Relay Outputs)	A
Size 16 Case, 24 Opto Inputs + 24 Relay Outputs + RTD	B
Size 16 Case, 24 Opto Inputs + 24 Relay Outputs + CLIO	C
Size 16 Case, 32 Opto Inputs + 24 Relay Outputs	D
Size 16 Case, 24 Opto Inputs + 32 Relay Outputs	E
Size 16 Case, 24 Opto Inputs + 24 Relay Outputs + RTD + CLIO	F
Size 16 Case, 32 Opto Inputs + 24 Relay Outputs + RTD	G
Size 16 Case, 24 Opto Inputs + 32 Relay Outputs + RTD	H
Size 16 Case, 32 Opto Inputs + 16 Relay Outputs + RTD + CLIO	J
Size 16 Case, 16 Opto Inputs + 32 Relay Outputs + RTD + CLIO	K
Size 16 Case, 24 Opto Inputs + 16 Relay Outputs + 4 High Break Outputs	L
Size 16 Case, 24 Opto Inputs + 16 Relay Outputs + 4 High Break Outputs + RTD	M
Size 16 Case, 24 Opto Inputs + 16 Relay Outputs + 4 High Break Outputs + CLIO	N
Size 16 Case, 24 Opto Inputs + 16 Relay Outputs + 4 High Break Outputs + RTD + CLIO	P
Size 16 Case, 16 Opto Inputs + 16 Relay Outputs + 8 High Break Outputs	Q
Size 16 Case, 16 Opto Inputs + 16 Relay Outputs + 8 High Break Outputs + RTD	R
Size 16 Case, 16 Opto Inputs + 16 Relay Outputs + 8 High Break Outputs + CLIO	S
Size 16 Case, 16 Opto Inputs + 16 Relay Outputs + 8 High Break Outputs + RTD + CLIO	T

Protocol / Communications Options	Hardware Compatibility	Design Suffix Compatibility	
K-Bus	1, 2, 3, 4, 7, 8, C	K/M	1
Modbus	1, 2, 3, 4, 7, 8, C	K/M	2
IEC 60870-5-103 (VDEW)	1, 2, 3, 4, 7, 8, C	K/M	3
DNP3.0	1, 2, 3, 4, 7, 8, C	K/M	4
IEC61850 + Courier (via rear RS485 port)	6, A & B	K/M	6
	G, H, J, K, L, M *	K/M	
	N, P **	K/M	
DNP3.0 Over Ethernet with Courier rear port K-Bus/RS485 protocol	6, A, B, G, H, J, K, L, M, N, P ***	M only	8

* Options are only available with software version 35 and later

** Options are only available with software version 36 and later

*** Options are only available with software version 38 and later

Mounting Option

Panel Mounting, with Harsh Environment Coating — M

Rack Mounting, with Harsh Environment Coating — N

Multilingual Language Option

English, French, German, Spanish — 0

English, French, German, Russian — 5

Chinese, English or French via HMI, with English or French only via Communications port — C

Software Issue **

Customisation

Default — 0

Customer — A

SEPARATELY ORDERED Accessories - See worksheet with "Accessories" tab

20 Hz Generator	PCS Material/Ordering code	P345:20HZ-GEN-*
Bandpass Filter	PCS Material/Ordering code	P345:BP-FILTER-*
400/5A Tripping CT	PCS Material/Ordering code	P345:CT
Generator and Filter mounting	PCS Material/Ordering code	Surface-mounting S Flush-mounting F Rail-mounting R

replace "*" in PCS Material/Ordering code for Generator & Filter by "S", "F" or "R"

IT

Variants Order No.		P346									
Generator Protection Relay with Differential											
Design Suffix											
As K plus increased main processor memory (XCPU3)											M
Extended Phase 2 CPU (phase 2 CPU and front panel with 10 function keys and tri-color LEDs and dual characteristic optos)											K
Vx Auxiliary Rating											
24 - 54Vdc			7								
48 - 125Vdc (40 - 100Vac)			8								
110 - 250Vdc, 100 - 240Vac			9								
In/Vn Rating											
In = 1/5A, Vn = 100 - 120Vac				1							
In = 1/5A, Vn = 380 - 480Vac				2							
Hardware Options	Protocol Compatibility										
Standard - None	1, 2, 3 & 4			1							
IRIG-B Only (modulated)	1, 2, 3 & 4			2							
Fibre Optic Converter Only	1, 2, 3 & 4			3							
IRIG-B (modulated) & Fibre Optic Converter	1, 2, 3 & 4			4							
Ethernet (100Mbit/s)	6, 8			6							
2nd Rear Comms	1, 2, 3 & 4			7							
IRIG-B (modulated) & 2nd Rear Comms	1, 2, 3 & 4			8							
Ethernet (100Mbit/s) plus IRIG-B (modulated)	6, 8			A							
Ethernet (100Mbit/s) plus IRIG-B (un-modulated)	6, 8			B							
IRIG-B (un-modulated)	1, 2, 3 & 4			C							
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8			G							
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8			H							
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8			J							
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8			K							
Redundant Ethernet Dual Homing Star, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8			L							
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8			M							
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8			N							
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8			P							
Product Specific Option											
Size 60TE Case, No Option (16 Optos + 14 Relays)					A						
Size 60TE Case, 16 Optos + 14 Relays + RTD					B						
Size 60TE Case, 16 Optos + 14 Relays + CLIO					C						
Size 60TE Case, 24 Optos + 14 Relays					D						
Size 60TE Case, 16 Optos + 22 Relays					E						
Size 80TE Case, 24 Optos + 24 Relays					F						
Size 80TE Case, 24 Optos + 24 Relays + RTD					G						
Size 80TE Case, 24 Optos + 24 Relays + CLIO					H						
Size 80TE Case, 32 Optos + 24 Relays					J						
Size 80TE Case, 24 Optos + 32 Relays					K						
Size 80TE Case, 24 Optos + 24 Relays + RTD + CLIO					L						
Size 80TE Case, 32 Optos + 24 Relays + RTD					M						
Size 80TE Case, 24 Optos + 32 Relays + RTD					N						
Size 80TE Case, 32 Optos + 16 Relays + RTD + CLIO					P						
Size 80TE Case, 16 Optos + 32 Relays + RTD + CLIO					Q						
Size 60TE Case, 16 Optos + 18 Relays (4 High Break)					R						
Size 60TE Case, 16 Optos + 11 Relays (4 High Break)					S						
Size 60TE Case, 16 Optos + 11 Relays (4 High Break) + CLIO					T						
Size 80TE Case, 16 Optos + 24 Relays (8 High Break)					U						
Size 80TE Case, 16 Optos + 24 Relays (8 High Break) + RTD					V						
Size 80TE Case, 16 Optos + 24 Relays (8 High Break) + CLIO					W						
Size 80TE Case, 16 Optos + 24 Relays (8 High Break) + RTD + CLIO					X						
Protocol / Communications Options	Hardware Compatibility										
K-Bus	1, 2, 3, 4, 7, 8, C					1					
Modbus	1, 2, 3, 4, 7, 8, C					2					
IEC 60870-5-103 (VDEW)	1, 2, 3, 4, 7, 8, C					3					
DNP3.0	1, 2, 3, 4, 7, 8, C					4					
IEC61850 + Courier (via rear RS485 port)	6, A, B, G, H, J, K, L, M, N, P					6					
DNP3.0 Over Ethernet with Courier rear port K-Bus/RS485 protocol	6, A, B, G, H, J, K, L, M, N, P *					8					
* Option only available with software version 38 and later											
Mounting Option											
Flush Panel Mounting, with Harsh Environment Coating							M				
Rack Panel Mounting, with Harsh Environment Coating (Size 80TE Case Only)							N				
Order FX0021001 rack mounting frame if rack mounting is required for 60TE case											
Multilingual Language Option											
English, French, German, Spanish								0			
English, French, German, Russian								5			
Chinese, English or French via HMI, with English or French only via Communications port								C			
Software Issue									**		
Customisation											
Default										0	
Customer										A	

IT

Variants Order No.		P348										
P348 VARSpeed												
Vx Auxiliary Rating												
24 - 48 Vdc		7										
48 - 110 Vdc (40 - 100 Vac)		8										
110 - 250 Vdc (100 - 240 Vac)		9										
In/Vn Rating												
IEC 61850-9-2LE Sampled Analogue Values Ethernet board			C									
Hardware Options	Protocol Compatibility											
Standard - None	1, 2, 3 & 4			1								
IRIG-B Only (modulated)	1, 2, 3 & 4			2								
Fibre Optic Converter Only	1, 2, 3 & 4			3								
IRIG-B (modulated) & Fibre Optic Converter	1, 2, 3 & 4			4								
Ethernet (100Mbit/s)	6, 8			6								
2nd Rear Comms	1, 2, 3 & 4			7								
IRIG-B (modulated) & 2nd Rear Comms	1, 2, 3 & 4			8								
Ethernet (100Mbit/s) plus IRIG-B (modulated)	6, 8			A								
Ethernet (100Mbit/s) plus IRIG-B (un-modulated)	6, 8			B								
IRIG-B (un-modulated)	1, 2, 3 & 4			C								
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8			G								
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8			H								
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8			J								
Redundant Ethernet RSTP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8			K								
Redundant Ethernet Dual Homing Star, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8			L								
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8			M								
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (modulated)	6, 8			N								
Redundant Ethernet PRP, 2 multi-mode fibre ports + IRIG-B (un-modulated)	6, 8			P								
Product Specific Option												
Size 80TE Case, 16 Optos + 16 Relays					A							
Size 80TE Case, 16 Optos + 16 Relays + CLIO					B							
Size 80TE Case, 16 Optos + 16 Relays + 4 High Break Outputs					C							
Size 80TE Case, 16 Optos + 16 Relays + 4 High Break Outputs + CLIO					D							
Size 80TE Case, 32 Optos + 32 Relays					E							
Size 80TE Case, 32 Optos + 32 Relays + CLIO					F							
Protocol / Communications Options	Hardware Compatibility											
K-Bus	1, 2, 3, 4, 7, 8, C					1						
IEC61850 + Courier (via rear RS485 port)	6, A, B, G, H, J, K, L, M, N, P					6						
Mounting Option												
Flush Panel Mounting							M					
Rack Panel Mounting							N					
Flush Panel Mounting, with harsh environment coating							P					
Rack Panel Mounting, with harsh environment coating							Q					
Multilingual Language Option												
English, French, German, Spanish								0				
English, French, German, Russian								5				
Chinese, English or French via HMI, with English or French only via Communications port								C				
Software Issue									**			
Customisation												
Default										0		
Customer										A		
Design Suffix												
Extended Phase 3 CPU with extended memory												M

MiCOM P391 (GENERATOR ROTOR EARTH FAULT MODULE) NOMENCLATURE

Character Type (A=Alpha, N=Numeric, X=Alpha-numeric)	A	N	N	N	A	X	X	X	A	X	X	N	N	X	A
Character Numbering (Maximum = 15)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	P	3	9	1	9	0	1	A	0	M	0	0	0	0	A

Vx Aux Rating 60-250 Vdc, 100-230 V ac	9
In/Vn Rating N/A	0
Hardware Options None	1
Product Specific None	A
Protocol Options N/A	0
Mounting	
Panel Mounting	P
Rack Mounting	R
Wall Mounting	W
Panel Mounting with Harsh Environment Coating	Q
Rack Mounting with Harsh Environment Coating	S
Wall Mounting with Harsh Environment Coating	X
Software	36
Setting Files N/A	0
Design Suffix Original hardware	A

IT

TD

TECHNICAL DATA

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

Technical Data

Mechanical Specifications

Design

Modular Px40 platform relay, P342 in 40TE or 60TE case, P343/6 in 60TE or 80TE case, P344/5/8 in 80TE case.
Mounting is front of panel flush mounting, or 19" rack mounted (ordering options).

Enclosure Protection

Per IEC 60529: 1992:
IP 52 Protection (front panel) against dust and dripping water,
IP 50 Protection for rear and sides of the case, against dust,
IP 10 Protection Product safety protection for the rear due to live connections on the terminal block.

Weight

P342	40TE): 7.9kg
P342	(60TE): 9.2kg
P343/6	(60TE): 11.5kg
P343/4/5/6	(80TE): 14kg
P348	(80TE): 8kg

Terminals

AC Current and Voltage Measuring Inputs

Located on heavy duty (black) terminal block:
Threaded M4 terminals, for ring lug connection.
CT inputs have integral safety shorting, on removal of the terminal block.

General Input/Output Terminals

For power supply, opto inputs, output contacts and RP1 rear communications.
Located on general purpose (grey) blocks:
Threaded M4 terminals, for ring lug connection.

Case Protective Earth Connection

Two rear stud connections, threaded M4.
Must be earthed (grounded) for safety, minimum earth wire size 2.5 mm^2.

Front Port Serial PC Interface

EIA(RS)232 DCE, 9 pin D-type female connector Socket SK1.
Courier protocol for interface to S1 Studio software.
Isolation to ELV (extra low voltage) level.
Maximum cable length 15 m.

Front Download/Monitor Port

EIA(RS)232, 25 pin D-type female connector Socket SK2.
For firmware and menu text downloads.
Isolation to ELV level.

Rear Communications Port (RP1)

EIA(RS)485 signal levels, two wire connections located on general purpose block, M4 screw.
For screened twisted pair cable, multidrop, 1000 m max.
For K-Bus, IEC-60870-5-103, MODBUS or DNP3.0 protocol (ordering options).
Isolation to SELV (Safety Extra Low Voltage) level.

Optional Rear Fiber Connection for SCADA/DCS

BFOC 2.5 -(ST®)-interface for glass fiber, as per IEC 874-10.
850 nm short-haul fibers, one Tx and one Rx. For Courier, IEC-60870-5-103, MODBUS or DNP3.0 (Ordering options).

Optional Second Rear Communications Port (RP2)

EIA(RS)232, 9 pin D-type female connector, socket SK4.
Courier protocol: K-Bus, EIA(RS)232, or EIA(RS)485 connection.
Isolation to SELV level.

Optional Rear IRIG-B Interface modulated or de-modulated

BNC plug
Isolation to SELV level.
50 ohm coaxial cable.

Optional Rear Ethernet Connection for IEC 61850/DNP 3.0

10BaseT/100BaseTX Communications

Interface in accordance with IEEE802.3 and IEC 61850
Isolation: 1.5 kV
Connector type: RJ45
Cable type: Screened Twisted Pair (STP)
Max. cable length: 100 m

100 Base FX Interface

Interface in accordance with IEEE802.3 and IEC 61850
Wavelength: 1300 nm
Fiber: multi-mode 50/125 µm or 62.5/125 µm
Connector type: BFOC 2.5 -(ST®)

Optional rear redundant Ethernet connection for IEC 61850/DNP3.0

100 base FX interface

Interface in accordance with IEEE802.3 and IEC 61850
Wavelength: 1300 nm
Fiber: multi-mode 50/125 µm or 62.5/125 µm
Connector style: BFOC 2.5 -(ST®)

Transmitter optical characteristics 100 base FX interface

Parameter	Sym	Min	Typ	Max	Unit
Output Optical Power BOL 62.5/125 µm, NA = 0.275 Fiber EOL	PO	-19 -20	-16.8	-14	dBm avg.
Output Optical Power BOL 50/125 µm, NA = 0.20 Fiber EOL	PO	-22.5 -23.5	-20.3	-14	dBm avg.
Optical Extinction Ratio				10 -10	% dB
Output Optical Power at Logic "0" State	PO ("0")			-45	dBm avg.

BOL - Beginning of life

EOL - End of life

Receiver optical characteristics 100 base FX interface

Parameter	Sym	Min	Typ	Max	Unit
Input Optical Power Minimum at Window Edge	PIN Min. (W)		-33.5	-31	dBm avg.
Input Optical Power Minimum at Eye Center	PIN Min. (C)		-34.5	-31.8	Bm avg.
Input Optical Power Maximum	PIN Max.	-14	-11.8		dBm avg.

Fiber defect connector (watchdog relay) – redundant Ethernet board

Connector (3 terminals): 2 NC contacts
Rated voltage: 250 V
Continuous current: 5 A
Short-duration current: 30 A for 3 s

Breaking capacity:
DC: 50 W resistive
DC: 25 W inductive (L/R = 40 ms)
AC: 1500 VA resistive (cos ϕ = unity)
AC: 1500 VA inductive (cos ϕ = 0.5)
Subject to maxima of 5 A and 250 V

Rear Ethernet connection for IEC 61850-9-2 LE (P348)

10BaseT/100BaseTX Communications

The same as optional rear Ethernet connection for IEC 61850

100 base FX interface

The same as the optional rear redundant Ethernet connection for IEC 61850

Ratings

AC Measuring Inputs

Nominal frequency: 50 and 60 Hz (settable)
Operating range: 5 to 70 Hz

AC Current

Nominal current (In): 1 and 5 A dual rated. (1A and 5A inputs use different transformer tap connections, check correct terminals are wired).
Nominal burden
<0.04 VA at In, <40 mΩ(0-30 In)In = 1A
<0.01 VA at In, <8 mΩ(0-30 In)In = 5A
Thermal withstand:
continuous 4 In
for 10 s: 30 In
for 1 s; 100 In
Standard: linear to 16 In (non-offset AC current).
Sensitive: linear to 2 In (non-offset AC current).

AC Voltage

Nominal voltage (Vn): 100 to 120 V or 380 to 480 V phase-phase
Nominal burden per phase: < 0.02 VA at 110/√3 V or 440/√3 V
Thermal withstand:
continuous 2 Vn
for 10 s: 2.6 Vn
Linear to 200 V (100 V/120 V), 800 V (380/480 V).

Power Supply

Auxiliary Voltage (Vx)

Three ordering options:
(i) Vx: 24 to 48 Vdc
(ii) Vx: 48 to 110 Vdc, and 40 to 100 Vac (rms)
(iii) Vx: 110 to 250 Vdc, and 100 to 240 Vac (rms)

Operating Range

(i) 19 to 65 V (dc only for this variant)
(ii) 37 to 150 V (dc), 32 to 110 V (ac)
(iii) 87 to 300 V (dc), 80 to 265 V (ac).
With a tolerable ac ripple of up to 15% for a dc supply, per IEC 60255-11: 2008.

Nominal Burden

Quiescent burden: 11 W (Extra 1.25 W when fitted with second rear communications board).
Additions for energized binary inputs/outputs:
Per opto input:
0.09 W (24 to 54 V)
0.12 W (110/125 V)
0.19 W (220/250 V)
Per energized output relay: 0.13 W
Power-up Time
Time to power up < 11 s.

Power Supply Interruption

Per IEC 60255-11: 1979:
The relay will withstand a 20 ms interruption in the DC auxiliary supply, without de-energizing.
Per IEC 61000-4-11: 1994:
The relay will withstand a 20 ms interruption in an AC auxiliary supply, without de-energizing.

Battery Backup

Front panel mounted
Type ½ AA, 3.6V Lithium Thionyl Chloride Battery (SAFT advanced battery reference LS14250)
Battery life (assuming relay energized for 90% time) >10 years

Digital (“Opto”) Inputs

Universal opto inputs with programmable voltage thresholds (24/27, 30/34, 48/54, 110/125, 220/250 V). May be energized from the 48 V field voltage, or the external battery supply.
Rated nominal voltage: 24 to 250 Vdc
Operating range: 19 to 265 Vdc
Withstand: 300 Vdc, 300 Vrms.

Nominal pick-up and reset thresholds:
Nominal battery 24/27: 60 - 80% DO/PU
(logic 0) <16.2 (logic 1) >19.2
Nominal battery 24/27: 50 - 70% DO/PU
(logic 0) <12.0 (logic 1) >16.8
Nominal battery 30/34: 60 - 80% DO/PU
(logic 0) <20.4 (logic 1) >24.0
Nominal battery 30/34: 50 - 70% DO/PU
(logic 0) <15.0 (logic 1) >21.0
Nominal battery 48/54: 60 - 80% DO/PU
(logic 0) <32.4 (logic 1) >38.4
Nominal battery 48/54: 50 - 70% DO/PU
(logic 0) <24.0 (logic 1) >33.6
Nominal battery 110/125: 60 - 80% DO/PU
(logic 0) <75.0 (logic 1) >88.0
Nominal battery 110/125: 50 - 70% DO/PU
(logic 0) <55.0 (logic 1) >77.0
Nominal battery 220/250: 60 - 80% DO/PU
(logic 0) <150.0 (logic 1) >176.0
Nominal battery 220/250: 50 - 70% DO/PU
(logic 0) <110 (logic 1) >154
Recognition time:
<2 ms with ac immunity filter off
<12 ms with ac immunity filter on
Time to operate an output contact from energizing a digital input:
<11ms with ac immunity filter off
<21ms with ac immunity filter on

Compliant to ESI 48-4

Output Contacts

Standard Contacts

General purpose relay outputs for signaling, tripping and alarming:
Continuous Carry Ratings (Not Switched):

Maximum continuous current:	10A (UL: 8A)
Short duration withstand carry:	30A for 3 s 250A for 30 ms
Rated voltage:	300 V

Make & Break Capacity:
DC: 50 W resistive
DC: 62.5 W inductive (L/R = 50 ms)
AC: 2500 VA resistive (cos ϕ = unity)
AC: 2500 VA inductive (cos ϕ = 0.7)

Make, Carry:
30A for 3 secs, dc resistive, 10,000 operations (subject to the above limits of make/break capacity and rated voltage)

Make, Carry & Break:
30A for 200 ms, ac resistive, 2,000 operations (subject to the above limits of make/break capacity & rated voltage)
4A for 1.5 secs, dc resistive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage)
0.5A for 1 sec, dc inductive, 10,000

operations (subject to the above limits of make/break capacity & rated voltage)
10A for 1.5 secs, ac resistive/inductive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage)

Durability:
Loaded contact: 10 000 operations minimum,
Unloaded contact: 100 000 operations minimum.

Operate Time
Less than 5 ms
Reset Time
Less than 5 ms

High Break Contacts

Continuous Carry Ratings (Not Switched):
Maximum continuous current: 10A
Short duration withstand carry: 30A for 3 s
250A for 30ms
Rated voltage: 300 V

Make & Break Capacity:
DC: 7500 W resistive
DC: 2500 W inductive (L/R = 50 ms)

Make, Carry:
30A for 3 secs, dc resistive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage)

Make, Carry & Break:
30A for 3 secs, dc resistive, 5,000 operations (subject to the above limits of make/break capacity & rated voltage)

30A for 200 ms, dc resistive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage)
10A (*), dc inductive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage)

*Typical for repetitive shots – 2 minutes idle for thermal dissipation

Voltage	Current	L/R	No of shots in 1 sec
65 V	10A	40 ms	5
150 V	10A	40 ms	4
250 V	10A	40 ms	2
250 V	10A	20 ms	4

MOV protection: Max Voltage 330 V dc

Durability:
Loaded contact: 10 000 operations minimum,
Unloaded contact: 100 000 operations minimum.

Operate Time:
Less than 0.2 ms
Reset Time:
Less than 8 ms

Watchdog Contacts

Non-programmable contacts for relay healthy/relay fail indication:
Breaking capacity:
DC: 30 W resistive
DC: 15 W inductive (L/R = 40 ms)
AC: 375 VA inductive (cos ϕ = 0.7)

IRIG-B 12X Interface (Modulated)

External clock synchronization per IRIG standard 200-98, format B12x
Input impedance 6 kΩ at 1000 Hz
Modulation ratio: 3:1 to 6:1
Input signal, peak-peak: 200 mV to 20 V

IRIG-B 00X Interface (Un-modulated)

External clock synchronization per IRIG standard 200-98, format B00X.
Input signal TTL level
Input impedance at dc 10 kΩ

Environmental Conditions

Ambient Temperature Range

Per IEC 60255-27: 2005:
Test Method IEC 6068-2-1:2007 and IEC 60068-2-2: 2007
Operating temperature range:
-25°C to +55°C (or -13°F to +131°F)
Storage and transit:
-25°C to +70°C (or -13°F to +158°F)
Tested as per
IEC 60068-2-1: 2007
-25°C storage (96 hours)
-40°C operation (96 hours)
IEC 60068-2-2: 2007
+85°C storage (96 hours)
+85°C operation (96 hours)

Ambient Humidity Range

Per IEC 60068-2-78: 2001 and IEC 60068-2-30:2005:
56 days at 93% relative humidity and + 40 °C
Per IEC 60068-2-30: 1980
Damp heat cyclic, six (12 + 12) hour cycles, 93% RH, +25 to +55 °C

Corrosive Environments

Per IEC 60068-2-60: 1995, Part 2, Test Ke, Method (class) 3
Industrial corrosive environment/poor environmental control, mixed gas flow test.
21 days at 75% relative humidity and +30ºC
exposure to elevated concentrations of H_2S, (100ppb) NO_2, (200ppb) Cl_2 (20ppb).

Per IEC 60068-2-52: 1996
Salt mist (7 days)
Per IEC 60068-2-43: 2003
H_2S (21 days), 15 ppm
Per IEC 60068-2-42: 2003
SO_2 (21 days), 25 ppm

Type Tests

Insulation

Per IEC 60255-27: 2005
Insulation resistance > 100 MΩ at 500 Vdc
(Using only electronic/brushless insulation tester).

Creepage Distances and Clearances

IEC 60255-27: 2005
Pollution degree 3,
Overvoltage category III,
Impulse test voltage (not RJ45) 5 kV
Impulse test voltage (RJ45) 1 kV

High Voltage (Dielectric) Withstand

(i) Per IEC 60255-27: 2005, 2 kV rms AC, 1 minute:
Between all independent circuits.
Between independent circuits and protective (earth) conductor terminal.
2 kV rms AC for 1 minute, across open watchdog contacts.
1 kV rms AC for 1 minute, across open contacts of changeover output relays.
1 kV rms AC for 1 minute for all D-type EIA(RS)232/EIA(RS)485 ports between the communications port terminals and protective (earth) conductor terminal.
(ii) Per ANSI/IEEE C37.90-1989 (reaffirmed 1994):
1.5 kV rms AC for 1 minute, across open contacts of normally open output relays.
1 kV rms AC for 1 minute, across open watchdog contacts.
1 kV rms AC for 1 minute, across open contacts of changeover output relays.

Impulse Voltage Withstand Test

Per IEC 60255-27: 2005
Front time: 1.2 µs, Time to half-value: 50 µs,
Peak value: 5 kV, 0.5 J
Between all independent circuits.
Between all independent circuits and protective (earth) conductor terminal.
Between the terminals of independent circuits.
EIA(RS)232 & EIA(RS)485 ports and normally
open contacts of output relays excepted.

Electromagnetic Compatibility (EMC)

TD

1 MHz Burst High Frequency Disturbance Test

Per IEC 60255-22-1: 2008, Class III,
Common-mode test voltage: 2.5 kV,
Differential test voltage: 1.0 kV,
Test duration: 2 s, Source impedance: 200 Ω
(EIA(RS)232 ports excepted).

100 kHz Damped Oscillatory Test

Per EN61000-4-18: 2011: Level 3, 100 kHz and 1 MHz Level 4
Common mode test voltage (level 3): 2.5 kV
Common mode test voltage (level 4): 4 kV
Differential mode test voltage: 1 kV

Immunity to Electrostatic Discharge

Per IEC 60255-22-2: 1996, Class 4,
15 kV discharge in air to user interface, display, communication port and exposed metalwork.
8 kV point contact discharge to any part of the front of the product.

Electrical Fast Transient or Burst Requirements

Per IEC 60255-22-4: 2008 and EN61000-4-4:2004. Test severity Class III and IV:
Amplitude: 2 kV, burst frequency 5 kHz (Class III) and 100 kHz (Class IV)
Amplitude: 4 kV, burst frequency 2.5 kHz and 100 kHz (Class IV).
Applied directly to auxiliary supply, and applied to all other inputs. (EIA(RS)232 ports excepted).
Amplitude: 4 kV, burst frequency 5 kHz (Class IV) applied directly to auxiliary.

Surge Withstand Capability

Per IEEE/ANSI C37.90.1: 2002:
4 kV fast transient and 2.5 kV oscillatory applied directly across each output contact, optically isolated input, and power supply circuit.
4 kV fast transient and 2.5 kV oscillatory applied common mode to communications, IRIG-B.

TD

Surge Immunity Test

(EIA(RS)232 ports excepted).
Per IEC 61000-4-5: 2005 Level 4,
Time to half-value: 1.2 / 50 µs,
Amplitude: 4 kV between all groups and protective (earth) conductor terminal,
Amplitude: 2 kV between terminals of each group.

Conducted/Radiated Immunity

For RTDs used for tripping applications the conducted and radiated immunity performance is guaranteed only when using totally shielded RTD cables (twisted leads).

Immunity to Radiated Electromagnetic Energy

Per IEC 60255-22-3: 2007, Class III:
Test field strength, frequency band 80 MHz to 3 GHz:
10 V/m,
Test using AM: 1 kHz / 80%,
Spot tests at 80, 160, 380, 450, 900, 1850, 2150 MHz
Per IEEE/ANSI C37.90.2: 2004:
80 MHz to 1000 MHz, 1 kHz 80% am and am pulsed modulated.
Field strength of 35 V/m.

Radiated Immunity from Digital Communications

Per EN61000-4-3: 2006, Level 4:
Test field strength, frequency band 800 to 960 MHz, and 1.4 to 2.0 GHz:
30 V/m,
Test using AM: 1 kHz/80%.

Radiated Immunity from Digital Radio Telephones

Per IEC 61000-4-3: 2002:
10 V/m, 900 MHz and 1.89 GHz.

Immunity to Conducted Disturbances Induced by Radio Frequency Fields

Per IEC 61000-4-6: 2008, Level 3,
Frequency bands, 150 kHz to 80 MHz
Disturbing test voltage: 10 V.
Test using AM: 1 kHz / 80%
Spot tests at 27, 68 MHz

Magnetic Field Immunity

Per IEC 61000-4-8: 2009, Level 5,
100 A/m applied continuously,
1000 A/m applied for 3 s.
Per IEC 61000-4-9: 2001, Level 5,
1000 A/m applied in all planes.
Per IEC 61000-4-10: 2001, Level 5,
100 A/m applied in all planes at 100 kHz/1 MHz with a burst duration of 2 s.

Conducted Emissions

Per EN 55022: 2010 Class A:
Power Supply: 0.15 - 0.5 MHz, 79 dBµV (quasi peak), 66 dBµV (average)
Power Supply: 0.5 - 30 MHz, 73 dBµV (quasi peak), 60 dBµV (average).
RJ45: 0.15 - 0.5 MHz, 97 dBµV (quasi peak), 84 dBµV (average)
RJ45: 0.5 - 30 MHz, 87 dBµV (quasi peak), 74 dBµV (average).

Radiated Emissions

Per EN 55022: 2010 Class A:
30 - 230 MHz, 40 dBµV/m at 10 m measurement distance
230 MHz - 1 GHz, 47 dBµV/m at 10 m measurement distance.
1 - 2 GHz, 76 dBµV/m at 10 m measurement distance.

Power Frequency

Per IEC 60255-22-7: 2003
Opto inputs (compliance is achieved using the opto input filter):
300V common mode (ClassA)
150V differential mode (ClassA)

EU Directives

EMC Compliance

Per 2004/108/EC:
Compliance to the European Commission Directive on EMC is demonstrated using a Technical File. Product Specific Standards were used to establish conformity:
EN 50263: 2000

Product Safety

Per 2006/95/EC:
Compliance to the European Commission Low Voltage Directive. (LVD) is demonstrated using a Technical File.
A product specific standard was used to establish conformity.
EN 60255-27: 2005

CE

R&TTE Compliance

Radio and Telecommunications Terminal Equipment (R & TTE) directive 99/5/EC.
Compliance demonstrated by compliance to both the EMC directive and the Low voltage directive, down to zero volts.
Applicable to rear communications ports.

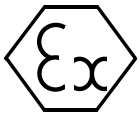
ATEX Compliance

ATEX Potentially Explosive Atmospheres directive 94/9/EC, for equipment.
The equipment is compliant with Article 1(2) of European directive 94/9/EC.
It is approved for operation outside an ATEX hazardous area. It is however approved for connection to Increased Safety, “Ex e”, motors with rated ATEX protection, Equipment Category 2, to ensure their safe operation in gas Zones 1 and 2 hazardous areas.

Certificate Number: 104 Issue 3
Assessment Date: 21-07-2010

CAUTION - Equipment with this marking is not itself suitable for operation within a potentially explosive atmosphere.

Compliance demonstrated by Notified Body certificates of compliance.



II (2) G

Mechanical Robustness

Vibration Test

Per IEC 60255-21-1: 1996:
Response Class 2
Endurance Class 2

Shock and Bump

Per IEC 60255-21-2: 1996:
Shock response Class 2
Shock withstand Class 1
Bump Class 1

Seismic Test

Per IEC 60255-21-3: 1995:
Class 2

P34x THIRD PARTY COMPLIANCES

Underwriters Laboratory (UL)



File Number: E202519
Original Issue Date: 18-07-2011
(Complies with Canadian and US requirements).

Energy Networks Association (ENA)



Technical Data P391

Mechanical Specifications

Design

80TE case.
Mounting options are, wall mounting, front of panel flush mounting, or 19" rack mounted (ordering options)

Enclosure Protection

Per IEC 60529: 1992

Rack and Panel Mounting Options

IP 20 (Safety) Protection for the case with the terminal safety cover fitted.

Wall Mounting Option

IP 20 (Safety) Protection for the P391 unit with the terminal safety cover fitted.

Weight

P391 (80TE): 5kg

Terminals

AC Voltage Measuring Inputs

Located on general purpose (grey) terminal blocks:
Threaded M4 terminals, for insulated ring crimped connectors.

Protective Conductor (Earth) Terminal

Two rear stud connections, threaded M4.
Must be earthed (grounded) for safety, using the protective (earth) conductor, of minimum wire size 2.5 mm2.

Current Loop Output

Located on general purpose (grey) terminal blocks:
Threaded M4 terminals, for insulated ring crimped connectors.

Ratings

Low Frequency Measuring Inputs

Nominal frequency: 0.25, 0.5, 1 Hz (settable with an internal jumper link)

DC Field Voltage Inputs

1200 V dc maximum

Power Supply

Auxiliary Voltage (Vx)

60-250 V dc, or 100-230 V ac (rms) 50/60 Hz

Operating Range

48-300 V dc, or 85-253 V ac (rms) 50/60 Hz
With a tolerable ac ripple of up to 15% for a dc supply, per IEC 60255-11: 2008.

Nominal Burden

Auxiliary Supply Input burden: 11 W or 24 VA.

Power Supply Interruption

Per IEC 60255-11: 1979
The relay will withstand a 20 ms interruption in the DC auxiliary supply, without de-energizing.
Per IEC 61000-4-11: 2004
The relay will withstand a 20 ms interruption in an AC auxiliary supply, without de-energizing.

Output Contacts

Watchdog Contacts

Non-programmable contacts for relay healthy/relay fail indication:
Breaking capacity:
DC: 30 W resistive
DC: 15 W inductive (L/R = 40 ms)
AC: 375 VA inductive (cos ϕ = 0.7)
Loaded contact: 10 000 operations Minimum,
Unloaded contact: 10 000 operations Minimum.

Environmental Conditions

Ambient Temperature Range

Per IEC 60068-2-1: 2007: cold;
IEC 60068-2-2: 2007: dry heat
Operating temperature range:
-25°C to +55°C (or -13°F to +131°F)
Storage and transit:
-25°C to +70°C (or -13°F to +158°F)

Ambient Humidity Range

Per IEC 60068-2-78: 2001
56 days at 93% relative humidity and +40 °C

Type Tests

Insulation

Per IEC 60255-27: 2005:
Insulation resistance > 100 MΩ at 500 Vdc (Using only electronic/brushless insulation tester).

Creepage Distances and Clearances

Per IEC 60664-1: 2007
Pollution degree 2,
Impulse 9.6 kVp between injection resistor inputs and protective (case earth) conductor terminal.
Minimum of 10.5 mm clearance and 12 mm creepage distance.

High Voltage (Dielectric) Withstand

(i) Per IEC 60255-27: 2005, 2 kV rms ac, 1 minute:
Between all independent circuits.
Between independent circuits and protective (case earth) conductor terminal.
1 kV rms ac for 1 minute, across open watchdog contacts.
(ii) Per ANSI/IEEE C37.90: 2005
1 kV rms ac for 1 minute across open watchdog contacts.
(iii) Per 60664-1: 2007
5.8 kV rms 1 minute between injection resistor inputs and protective (case earth) conductor terminal.

Impulse Voltage Withstand Test

Per IEC 60255-27 2005
Front time: 1.2 µs, Time to half-value: 50 µs,
Peak value: 5 kV, 0.5 J
Between all independent circuits.
Between all independent circuits and protective (case earth) conductor terminal.
Between the terminals of independent circuits.
Normally open contacts of output relays excepted.
IEC 60664-1: 2007

Impulse 9.6 kV between injection resistor inputs and protective (case earth) conductor terminal

Electromagnetic Compatibility (EMC)

1 MHz Burst High Frequency Disturbance Test

Per IEC 60255-22-1: 2005, Class III,
Common-mode test voltage: 2.5 kV,
Differential test voltage: 1.0 kV,
Test duration: 2 s, Source impedance: 200 Ω

100 kHz Damped Oscillatory Test

Per EN61000-4-18: 2007: Level 3
Common mode test voltage: 2.5 kV
Differential mode test voltage: 1 kV

Electrical Fast Transient or Burst Requirements

Per IEC 60255-22-4: 2002 and EN61000-4-4:2004. Test severity Class III and IV:
Amplitude: 2 kV, burst frequency 5 kHz (Class III),
Amplitude: 4 kV, burst frequency 2.5 kHz (Class IV).
Applied directly to auxiliary supply, and applied to all other inputs. (EIA(RS)232 ports excepted).
Amplitude: 4 kV, burst frequency 5 kHz (Class IV) applied directly to auxiliary.

Surge Withstand Capability

Per IEEE/ANSI C37.90.1: 2002
4 kV fast transient and 2.5 kV oscillatory applied directly across each output contact, optically isolated input, and power supply circuit.
4 kV fast transient and 2.5 kV oscillatory applied common mode to communications, IRIG-B.

Surge Immunity Test

(EIA(RS)232 ports excepted).
Per EN 61000-4-5: 2006 Level 4, EN 60255-22-5: 2002
Time to half-value: 1.2 / 50 µs,
Amplitude: 4 kV between all groups and protective (earth) conductor terminal,
Amplitude: 2 kV between terminals of each group.
Level 3: 1 kV between terminals of injection resistor inputs

Immunity to Radiated Electromagnetic Energy

Per IEC 60255-22-3: 2007, Class III:
(EN61000-4-3: 2006, Level 3)
Test field strength, frequency band 80 to 1000 MHz:
10 V/m,
Test using AM: 1 kHz / 80%,
Spot tests at 80, 160, 450, 900 MHz
Per IEEE/ANSI C37.90.2: 2004:
80 MHz to 1000 MHz, 1 kHz 80% am and am pulsed modulated.
Field strength of 35 V/m.

Radiated Immunity from Digital Communications
Per EN61000-4-3: 2002, Level 4:
Test field strength, frequency band 800 to 960 MHz, and 1.4 to 2.0 GHz:
30 V/m,
Test using AM: 1 kHz/80%.

Radiated Immunity from Digital Radio Telephones
Per IEC61000-4-3: 2002:
10 V/m, 900 MHz and 1.89 GHz.

Immunity to Conducted Disturbances Induced by Radio Frequency Fields
Per IEC 61000-4-6: 2007, Level 3,
IEC60255-22-6: 2001
Disturbing test voltage: 10 V.

Power Frequency Magnetic Field Immunity
Per IEC 61000-4-8: 1994, Level 5,
100 A/m applied continuously,
1000 A/m applied for 3 s.
Per IEC 61000-4-9: 1993, Level 5,
1000 A/m applied in all planes.
Per IEC 61000-4-10: 1993, Level 5,
100 A/m applied in all planes at
100 kHz/1MHz with a burst duration of 2 s.

Conducted Emissions
Per EN 55022: 1998 Class A:
0.15 - 0.5 MHz, 79 dBμV (quasi peak)
66 dBμV (average)
0.5 - 30 MHz, 73 dBμV (quasi peak)
60 dBμV (average).

Radiated Emissions
Per EN 55022: 1998 Class A:
30 - 230 MHz, 40 dBμV/m at 10 m measurement distance
230 - 1 GHz, 47 dBμV/m at 10 m measurement distance.

EU Directives

EMC Compliance
Per 2004/108/EC:
Compliance to the European Commission Directive on EMC is demonstrated using a Technical File route. Product Specific Standards were used to establish conformity:
EN 50263: 2000

Product Safety
Per 2006/95/EC:
Compliance with European Commission Low Voltage Directive (LVD). A Product Specific Standard was used to establish conformity:
EN 60255-27: 2005

CE

Mechanical Robustness

Vibration Test
Per IEC 60255-21-1: 1996:
Response Class 2
Endurance Class 2

Shock and Bump
Per IEC 60255-21-2: 1996:
Shock response Class 2
Shock withstand Class 1
Bump Class 1

Seismic Test
Per IEC 60255-21-3: 1995:
Class 2

Protection Functions

Generator Differential

Accuracy

Pick-up: Formula ±5%
Drop-off: 95% of setting ±5%
Operating time: <30 ms for currents applied at 4x pickup level or greater
Repeatability: <7.5%
Disengagement time: <40 ms

Transformer Differential

Accuracy

Low Set Biased Differential

Pick-up: formula ±5%
Drop-off: 95% x formula ±5%
Pick-up and drop-off repeatability: <1%
Operating time: <33 ms for currents applied at 3x pickup level or greater
DT operating time: ±2% or 33 ms whichever is greater for currents applied at 3x pickup level or greater
Operating time repeatability: < 2 ms
Disengagement time: <40 ms

High Set Operation

Operating time :< 25 ms.
Reset time: < 40 ms
Operation time repeatability: < 2 ms
Pick-up and drop-off repeatability: <2%

2nd Harmonic Blocking

Pick-up: Setting ±5%
Drop-off: 0.95 of setting ±5%
Pick-up and drop-off repeatability: <2%

5th Harmonic Blocking(P343/4/6)

Pick-up: Setting ±10%
Drop-off: 0.95 of setting ±10%
Pick-up and drop-off repeatability: <2%

5th Harmonic Blocking (P345)

Pick-up: Setting ±5%
Drop-off: 0.95 of setting ±5%
Pick-up and drop-off repeatability: <2%

Circuitry Fault Alarm

Accuracy

Pick-up: formula ±5%
Drop-off: 0.95 x formula ±5%
Pick-up and drop-off repeatability: <1%
Instantaneous operating time: <33 ms at 3x pick-up value
DT operating time: ±2% or 33 ms whichever is greater for currents applied at 3x pickup level or greater
Disengagement time: <40 ms
Operating time repeatability: <3 ms

Through Fault Monitoring

Accuracy

TF I> pick-up: setting ±5%
TF I> drop-off: 0.95 of setting ±5%
TF I^2t> pick-up: setting ±2% or $5A^2s$ whichever is greater
Pick-up repeatability: <5%
Operating time repeatability: <50 ms

Power (3 Phase)

Accuracy

Over Active Power

Pick-up:
Setting +/- 5% (Angle <=80° & Setting >=0.6W)
Drop-off:
95% of Setting +/- 5% (Angle <=80° & Setting >=0.6W)

Over Reactive Power

Pick-up:
Setting +/- 5% (Angle >= 10°)
Drop-off:
95% of Setting +/- 5% (Angle >= 10°)

Under Active Power

Pick-up:
Setting +/- 10% (60°<Angle <=80°), +/- 5% (Angle <=60°)
Drop-off:
105% of Setting +/- 10% (60°<Angle <=80°) or
105% of Setting +/- 5% (Angle <=60°)

Under Reactive Power

Pick-up:
Setting +/- 10% (10°<=Angle <=15°) or
Setting +/- 5% (Angle >=15°)
Drop-off:
105% of Setting +/- 10% (10°<Angle <=15°) or
105% of Setting +/- 5% (Angle >=15°)
Operating time: ±2% or 50 ms whichever is greater
Disengagement time: <50 ms
tRESET: ±5%
Instantaneous operating time: <50 ms

TD

TD

Sensitive Power (1/2 Phase)

Accuracy
Sensitive Power (1 Phase)

Over Active Power
Pick-up:
Setting +/- 5% (Angle <=75°)
Drop-off:
95% of Setting +/- 5% (Angle <=75°)

Over Reactive Power
Pick-up:
Setting +/- 5% (Angle >= 10°)
Drop-off:
95% of Setting +/- 5% (Angle >= 10°)

Under Active Power
Pick-up:
Setting +/- 10% (Angle <=75° & Setting <10W) or
Setting +/- 5% (Angle <=75° & Setting >=10W)
Drop-off:
105% of Setting +/- 10% (Angle <=75° & Setting <10W) or
105% of Setting +/- 5% (Angle <=75° & Setting >=10W)

Under Reactive Power
Pick-up:
Setting +/-5% (Angle >=15°)
Drop-off:
105% of Setting +/- 5% (Angle >=15°)

Sensitive Power (2 Phase Wattmetric)
Over Active Power
Pick-up:
Setting +/- 5% (Angle <=80°)
Drop-off:
95% of Setting +/- 5% (Angle <=80°)

Over Reactive Power
Pick-up:
Setting +/- 5% (Angle >= 10°)
Drop-off:
95% of Setting +/- 5% (Angle >= 10°)

Under Active Power
Pick-up:
Setting +/- 5% (Angle <=80°)
Drop-off:
105% of Setting +/- 5% (Angle <=80°)

Under Reactive Power
Pick-up:
Setting +/-5% (Angle >=10°)
Drop-off:
105% of Setting +/- 5% (Angle >=10°)
Operating time: ±2% or 50 ms whichever is greater
Disengagement time: <50 ms
tRESET: ±5%
Instantaneous operating time: <50 ms

Negative Phase Sequence Overpower

Accuracy
Pick-up: Setting ±5%
Drop-off: 0.95 of setting ±5%
Repeatability (operating threshold): <1%
Operating time: ±2% or 70 ms whichever is greater
Disengagement time: <35 ms
Repeatability (operating times): <10 ms

Field Failure

Accuracy
Mho characteristic Pick-up:
+/- 5% or 0.5Ω of mho shape (Xb1<=10 & |Xa1|/Xb1<=16) or
+/- 5% or 0.5Ω Ohm of mho shape (Xb1>10 & |Xa1|/Xb1<=8)
Mho characteristic Drop-off:
105% of pick-up +/- 5% or 0.5Ω (Xb1 <=10 & |Xa1|/Xb1<=16) or
105% of pick-up +/- 5% or 0.5Ω (Xb1 >10 & |Xa1|/Xb1<=8)
Directional Line Pick-up:
Setting angle ±1°(offset = 0Ω & VA>=20V) or
±5% of pick up shape (offset =0Ω)
Directional Line Drop-off:
Setting angle ±1°(offset = 0Ω & VA>=20V) or
±5% of drop off shape (offset =0Ω)
Alarm Linear characteristic Pick-up:
Characteristic shape ±10%
Alarm Linear characteristic Drop-off:
105% of setting ±10%
Operating time: ±2% or 50 ms whichever is greater
Disengagement time: <50 ms

Negative Phase Sequence Thermal

Accuracy
Pick-up: Formula ±5%
Drop-off: 95% of pick-up ±5%
Operating time: ±5% or 55 ms whichever is greater
Repeatability: <5%
Disengagement time: <30 ms

System Back-up

Voltage Dependent Overcurrent

Accuracy

VCO threshold Pick-up: Setting ±5%
Overcurrent Pick-up: Formula ±5%
VCO threshold Drop-off: 1.05 x Setting ±5%
Overcurrent Drop-off: 0.95 x formula ±5%
Operating time: <50 ms
Repeatability: < 2.5%
IDMT operation: ±5% or 40 ms whichever is greater
Definite time operation: ±5% or 50 ms whichever is greater
tRESET: ±5% or 50 ms whichever is greater

Under Impedance

Accuracy

Pick-up: Setting ±5%
Drop-off: 105% of setting ±5%
Operating time: ±2% or 50 ms whichever is greater
Repeatability: <5%
Disengagement time: <50 ms
tRESET: ±5%
Instantaneous operating time: <50 ms

4-Stage Directional/Non-Directional Overcurrent

Accuracy

Pick-up: Setting ±5%
Drop-off: 0.95 x Setting ±5%
Minimum trip level (IDMT): 1.05 x Setting ±5%
IDMT characteristic shape: ±5% or 40 ms whichever is greater*
IEEE reset: ±5% or 50 ms whichever is greater
DT operation: ±2% or 50 ms whichever is greater
DT Reset: ±5%
Directional accuracy (RCA ±90°): ±2° hysteresis 2°
Characteristic UK: IEC 6025-3…1998
Characteristic US: IEEE C37.112…1996
* Under reference conditions

4-Stage Negative Phase Sequence Overcurrent

Accuracy

I2>Pick-up: Setting ±5%
I2> Drop-off: 0.95 x Setting ±5%
Vpol Pick-up: Setting ±5%
Vpol Drop-off: 0.95 x Setting ±5%
DT operation: ±2% or 60 ms whichever is greater
Disengagement time: <35 ms
Directional accuracy (RCA ±90°): ±2° hysteresis <1%
Repeatability (operating times): <10 ms

TD

Thermal Overload

Gen Thermal

Accuracy

Setting accuracy: ±5%
Reset: 95% of thermal setting ±5%
Thermal alarm Pick-up: Calculated trip time ±5%
Thermal overload Pick-up: Calculated trip time ±5%
Cooling time accuracy: ±5% of theoretical
Repeatability: <2.5%

Transformer Thermal and Loss of Life

Accuracy

Transformer Thermal

Hot Spot> Pick-up: Expected pick-up time ±5% (expected pick-up time is the time required to reach the setting)
Hot Spot> DT: ±5% or 200 ms whichever is greater
Top Oil> Pick-up: Expected Pick-up Time ±5% (expected pick-up time is the time required to reach the setting)
Top Oil> DT: ±5% or 200 ms whichever is greater
Pick-up repeatability: <2.5%
Time repeatability: <20 ms

Loss of life

FAA> Pick-up: Formula: ±5%
Loss of Life> Pick-up: Expected Pick-up Current ±5%.
Repeatability: <2.5%
FAA> DT: ±5% or 200 ms whichever is greater

TD

2-Stage Non-Directional Earth Fault

Accuracy

Pick-up: Setting ±5%
Drop-off: 0.95 x Setting ±5%
IDMT trip level elements: 1.05 x Setting ±5%
IDMT characteristic shape: ±5% or 40 ms whichever is greater*
IEEE reset: ±5% or 40 ms whichever is greater
DT operation: ±2% or 60 ms whichever is greater
DT reset: ±5%
Repeatability: 2.5%

Rotor Earth Fault

Accuracy

Pick-up: Setting ±10% (1 k to 5 kΩ)
Setting ±5% (5 k to 80 kΩ)
Drop-off: 1.05 x Setting ±10% (1 k to 5 kΩ)
1.02 x Setting ±5% (5 k to 80 kΩ)
Repeatability: <1%
DT operation for Double ended connection: ±2% or 2.5/fs whichever is greater
Disengagement time: <2.5/fs
DT operation for Single ended connection:
Field voltage 0 to 600 V DC
±2% or 2.5/fs whichever is greater
Disengagement time: <2.5/fs
Field voltage 601 to 1200 V DC
±2% or 3.5/fs whichever is greater
Disengagement time: <3.5/fs
(fs – injection frequency, 0.25/0.5/1 Hz)

Sensitive Directional Earth Fault

SEF Accuracy

Pick-up: Setting ±5%
Drop-off: 0.95 x Setting ±5%
DT operation: ±2% or 50 ms whichever is greater
DT reset: ±5%
Repeatability: 5%

Wattmetric SEF Accuracy

P = 0 W Pick-up: ISEF> ±5%
P > 0 W Pick-up: P> ±5%
P = 0 W Drop-off: (0.95 x ISEF>) ±5%
P > 0 W Drop-off: 0.9 x P> ±5%
Boundary accuracy: ±5% with 1° hysteresis
Repeatability: 5%

Polarizing Quantities Accuracy

Operating boundary Pick-up: ±2° of RCA ±90°
Hysteresis: <3°
ISEF>Vnpol Pick-up: Setting ±10%
ISEF>Vnpol Drop-off: 0.9 x Setting or 0.7 V (whichever is greater) ±10%

Restricted Earth Fault

Accuracy

Low impedance biased REF

Pick-up: Setting formula ±5%
Drop-off: 0.9 x formula ±5%
Pick-up and drop-off repeatability: <5%
Operating time: <50 ms
Disengagement time: <30 ms

High impedance REF

Pick-up: Setting ±5%
Operating time: <30 ms

Transient Overreach and Overshoot

Accuracy

Additional tolerance X/R ratios: ±5% over the X/R ratio of 1…90
Overshoot of overcurrent elements: <40 ms
Disengagement time: <60 ms (65 ms SEF)

Neutral Displacement/Residual Overvoltage

Accuracy

DT/IDMT Pick-up: Setting ±5%
Drop-off: 0.95 x Setting ±5%
IDMT characteristic shape: ±5% or 55 ms whichever is greater
DT operation: ±2% or 55 ms whichever is greater Instantaneous operation <55 ms
Reset: <35 ms
Repeatability: <1%

100% Stator Earth Fault (3rd Harmonic)

Accuracy

VN3H</VN3H> Pick-up: Setting ±5%
V/P/Q/S<Inh: Setting ±0.5%
VN3H< Drop-off: 105% of Pick-up ±5%
VN3H> Drop-off: 95% of Pick-up ±5%
V/P/Q/S<Inh Drop-off: 95% of Pick-up ±0.5%
Operating time: ±0.5% or 50 ms whichever is greater

Repeatability: < 0.5%
Disengagement/reset time: <50 ms

100% Stator Earth Fault, 64S (Low Frequency Injection)

Accuracy

R<1/R<2 Pick-up: Setting ±5% (for R ≤ 300 Ω), ±7.5% (for R> 300 Ω) or 2 Ω whichever is greater
I>1/V<1/I<1 Pick-up: Setting ±5%
R<1/R<2 Drop-off: 105% of setting ±5% (for R ≤ 300 Ω), ±7.5% (for R> 300 Ω)
V<1/I<1 Drop-off: 105% of setting ±5%
I>1 Drop-off: 95% of setting ±5%
Repeatability: <1%
R<1/R<2/I>1/V<1/I<1 operating time without bandpass filter: ±2% or 220 ms whichever is greater
R<1/R<2/I>1/V<1/I<1 disengagement time: <120 ms
Repeatability: <100 ms
R<1/R<2/I>1/V<1/I<1 operating time with bandpass filter: ±2% or 1.3 s whichever is greater
R<1/R<2/I>1/V<1/I<1 disengagement time: <700 ms
Repeatability: <100 ms

Volts/Hz

Accuracy

Pick-up: Setting ±2%
Drop-off: 98% or pick-up ±2%
Repeatability (operating threshold): <1%
IDMT operating time: ±5% or 60 ms whichever is greater
Definite time: ±2% or 30 ms whichever is greater
Disengagement time: <50 ms
Repeatability (operating times): <10 ms
V/Hz measurement: ±1%

Unintentional Energization at Standstill (Dead Machine)

Accuracy

I > Pick-up: Setting ±5%
V< Pick-up: Setting ±5%
I > Drop-off: 95% of setting ±5%
V< Drop-off: 105% of setting ±5%
Operating time: ±2% or 50 ms whichever is greater
Repeatability: 2.5% or 10 ms whichever is greater

Undervoltage

Accuracy

DT Pick-up: Setting ±5%
IDMT Pick-up: Setting ±5%
Drop-off: 1.02 x Setting ±5%
IDMT characteristic shape: ±2% or 50 ms whichever is greater
DT operation: ±2% or 50 ms whichever is greater
Reset: <75 ms
Repeatability: <1%

TD

Overvoltage

Accuracy

DT Pick-up: Setting ±5%
IDMT Pick-up: Setting ±5%
Drop-off: 0.98 x Setting ±5%
IDMT characteristic shape: ±2% or 50 ms whichever is greater
DT operation: ±2% or 50 ms whichever is greater
Reset: <75 ms
Repeatability: <1%

NPS Overvoltage

Accuracy

Pick-up: Setting ±5%
Drop-off: 0.95 x Setting ±5%
Repeatability (operating threshold): <1%
DT operation: ±2% or 65 ms whichever is greater
Instantaneous operation: <60 ms
Instantaneous operation: (accelerated): <45 ms
Disengagement time: <35 ms
Repeatability (operating times): <10 ms

Underfrequency

Accuracy

Pick-up: Setting ±0.01 Hz
Drop-off: (Setting +0.025 HZ) ±0.01 Hz
DT operation: ±2% or 50 ms whichever is greater*
* The operating will also include a time for the relay to frequency track 20 Hz/ second).

Overfrequency

Accuracy

Pick-up: Setting ±0.01 Hz
Drop-off: (Setting -0.025 Hz) ±0.01 Hz
DT operation: ±2% or 50 ms whichever is greater *

* The operating will also include a time for the relay to frequency track 20 Hz/ second).

Rate of Change of Frequency 'df/dt'

Accuracy

Fixed Window (P341/2/3/4/6)

Pick-up: Setting ±0.05 Hz/s or ±3% whichever is greater
Repeatability: <5%

Fixed Window (P345)

Pick-up: Setting ±0.05 Hz/s or ±15% whichever is greater (df/dt < 1.5 Hz/s)
Repeatability: <5%

Rolling Window (P341/2/3/4/6)

Pick-up: Setting ±0.01 Hz/s or ±3% whichever is greater
Repeatability: <5%
Rolling Window (P345)
Pick-up: Setting ±0.01 Hz/s or ±10% whichever is greater (df/dt < 1.5 Hz/s)
Repeatability: <5%

Freq Low, Freq High

Pick-up: Setting ±2% or ±0.08 Hz whichever is greater

Delay Time

Fixed Window (P342/3/4/6):

Dead time: Setting ±2% or ±(40+20*X*Y) ms
Repeatability: <20mS

Rolling Window (P342/3/4/6):

Dead time: Setting ±2% or ±(60+20*X+5*Y) ms
Repeatability: <20mS

Fixed Window (P345):

Dead time: Setting ±2% or ±(100+20*X*Y) ms
Repeatability: <30mS

Rolling Window (P345):

Dead time: Setting ±2% or ±(150+20*X*Y) ms
Repeatability: <30mS
Note: X = average cycles, Y = Iterations

Generator Abnormal Frequency

Accuracy

Pick-up: Setting ±0.01 Hz
Drop-off lower threshold: (Setting -0.025 Hz) ±0.01 Hz
Drop-off upper threshold: (Setting +0.025 Hz) ±0.01 Hz
Repeatability (operating threshold): <1%
Accumulation time: ±2% or 50 ms whichever is the greater
Dead time: ±2% or 50 ms whichever is the greater
Repeatability (operating times): <10 ms

Resistive Temperature Detectors

Accuracy

Pick-up: Setting ±1°C
Drop-off: (Setting -1°C)
Operating time: ±2% or <3 s

CB Fail

Timer Accuracy
Timers: ±2% or 40 ms whichever is greater
Reset time: <30 ms

Undercurrent Accuracy

Pick-up: Setting ±10%
Drop-off: 1.05 x Setting ±10%
Pick-up and Drop-off Repeatability: <5%
Operating time: < 15 ms
Reset: < 15 ms
Time repeatability: 10 ms

Pole Slipping

Accuracy

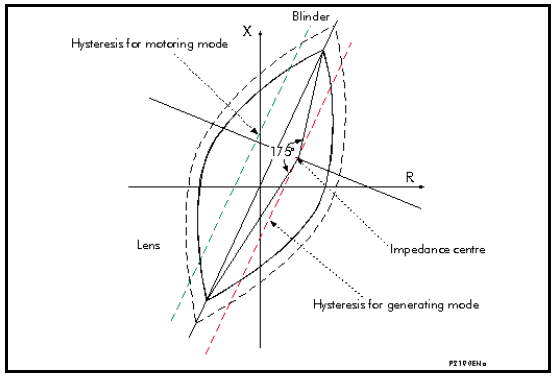
Lens Characteristic Pick-up: Setting ±5%
Blinder Pick-up: ±1°
Reactance line Pick-up: Setting ±5%
Lens DO characteristic Lens Angle: Adjusted by -5°, (ZA+ZB) + 5%
Lens DO Drop-off: Lens DO characteristic ±5%
Blinder DO characteristic:
Blinder displaced by (ZA+ZB)/2 x tan 87.5°
Blinder DO Drop-off:
Blinder DO characteristic ±1°
Repeatability: <2.5%
T1, T2 and Reset Timer: ±2% or 10 ms whichever is greater

Hysteresis:

Hysteresis is applied to the lenticular characteristic and to the blinder as soon as they pick up individually. Hysteresis is not required for the reactance line as Zone 1 or Zone 2 is determined at a single point when the locus traverses the blinder.

For the lens, the hysteresis consists of an angle of 5° subtracted from the α setting to increase the lens size and an increment of 5% applied to ZA and ZB to extend the reach. Hysteresis for the blinder is dependent on the mode of operation. For generating mode, the blinder is adjusted to the right, for motoring mode, the blinder is adjusted to the left, with a distance which is equivalent to an angle separation of 175°.

This is shown in the diagram below. This distance is equivalent to (ZA + ZB)/2*tan87.5°.
For both characteristics the hysteresis is reset when the impedance locus leaves the lens.



Hysteresis of the pole slipping characteristic

P348 Protection

Non-Directional Peak/RMS Overcurrent

Peak Overcurent

Accuracy

Pick-up: Setting ±5%
Drop-off: 0.95 x Setting ±5%
DT operation: ±2% or 50 ms whichever is greater
DT reset: ±5%

RMS Overcurent

Pick-up: Setting ±5%
Drop-off: 0.95 x Setting ±5%
Minimum trip level (IDMT): 1.05 x Setting ±5%
IDMT characteristic shape: ±5% or 40 ms or 0.6 cycles whichever is greater*
DT operation: ±2% or 50 ms or 0.4 cycles whichever is greater
DT reset: ±5% or 50 ms whichever is greater
Characteristic UK: IEC 6025-3…1998
Characteristic US: IEEE C37.112…1996
* Under reference conditions

Negative Phase Sequence Overcurrent

Accuracy

I2>Pick-up: Setting ±5%
I2> Drop-off: 0.95 x Setting ±5%
DT operation: ±2% or 60 ms or 0.4 cycles whichever is greater
Disengagement time: < 1 cycle (<30Hz) <35 ms (>30Hz)

Peak/RMS Overvoltage

TD

Peak Overvoltage

Accuracy

DT Pick-up: Setting ±5%
Drop-off: 0.98 x Setting ±5%
DT operation: ±2% or 50 ms whichever is greater
DT reset: ±5% or 50ms whichever is the greater

RMS Overvoltage

Accuracy

DT Pick-up: Setting ±5%
IDMT Pick-up: Setting ±5%
Drop-off: 0.98 x Setting ±5%
IDMT characteristic shape: ±2% or 50 ms or 0.8 cycles whichever is greater
DT operation: ±2% or 50 ms or 0.5 cycles whichever is greater
DT reset: ±5% or 35ms whichever is the greater

Neutral Displacement/Residual Overvoltage

Accuracy

DT/IDMT Pick-up: Setting ±5%
Drop-off: 0.95 x Setting ±5%
IDMT characteristic shape: ±5% or 65 ms or 1 cycle whichever is greater
DT operation: ±2% or 65 ms or 1 cycle whichever is greater Instantaneous operation <65 ms
DT reset: ±5% or 35ms whichever is the greater

Overfrequency

Accuracy

Pick-up: Setting ±0.01 Hz (<60Hz), Setting±0.075Hz (>60Hz)
Drop-off: 0.98 x Setting ±0.01 Hz (<50Hz), 0.98 x Setting ±0.05 Hz (>50Hz)

DT operation: ±2% or 70 ms or 2 cycles whichever is greater

Supervisory Functions

Voltage Transformer Supervision

Accuracy

Fast block operation: <25 ms
Fast block reset: <30 ms
Time delay: Setting ±2% or 20 ms whichever is greater

Current Transformer Supervision

Accuracy

IN > Pick-up: Setting ±5%
VN < Pick-up: Setting ±5%
IN > Drop-off: 0.9 x Setting ±5%
VN < Drop-off: (1.05 x Setting) ±5% or 1 V whichever is greater
CTS block operation: < 1 cycle
CTS reset: < 35 ms

Differential CTS

Accuracy

CTS I1 Pick-up ratio: Setting ±5%
CTS I2/I1>1 Pick-up ratio: 0.95 x setting ±5%
CTS I2/I1>2 Pick-up ratio: setting ±5%
CTS I1 Drop-off ratio: 0.95 x setting ±5%
CTS I2/I1>1 Drop-off ratio: setting ±5%
CTS I2/I1>2 Drop-off ratio: 0.95 x setting ±5%
Pick-up and drop-off repeatability: <1%
Time delay operation: ±2% or 33 ms whichever is greater
CTS terminal block operation: <33 ms
CTS differential block operation < 33 ms
Operating time repeatability: <2 ms
CTS Disengagement time <40 ms

System Checks

Voltage Monitors

Accuracy

Gen Voltage Monitor

Live Voltage:

Pick-up: setting ±3% or ±0.1 V whichever is greater
Drop-off: (0.98 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Dead Voltage:

Pick-up: Setting ±3% or ±0.1 V whichever is greater
Drop-off: (1.02 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Diff Voltage:

Pick-up: setting ±3% or ±0.1 V whichever is greater
Drop-off: (0.98 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Overvoltage:

Pick-up: Setting ±3% or ±0.1 V whichever is greater
Drop-off: (0.98 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Undervoltage:

Pick-up: Setting ±3% or ±0.1 V whichever is greater
Drop-off: (1.02 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Gen Frequency Monitor

Gen Overfrequency:

Pick-up: Setting ±0.01 Hz
Drop-off: (Setting -0.1 Hz) ±0.01 Hz
Repeatability: <1%

Gen Underfrequency:

Pick-up: Setting ±0.01 Hz
Drop-off: (Setting +0.1 Hz) ±0.01 Hz
Repeatability: <1%

Bus Voltage Monitor

Live Voltage:

Pick-up: Setting ±3% or ±0.1 V whichever is greater
Drop-off: (0.98 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Dead Voltage:

Pick-up: Setting ±3% or ±0.1 V whichever is greater
Drop-off: (1.02 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Diff Voltage:

Pick-up: Setting ±3% or ±0.1 V whichever is greater
Drop-off: (0.98 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Overvoltage:

Pick-up: Setting ±3% or ±0.1 V whichever is greater
Drop-off: (0.98 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Undervoltage:

Pick-up: Setting ±3% or ±0.1 V whichever is greater
Drop-off: (1.02 x Setting) ±3% or ±0.1 V whichever is greater
Repeatability: <1%

Check Synch

Accuracy

CS1

CS1 Phase Angle:

Pick-up: (Setting-2°) ±1°
Drop-off: (Setting-1°) ±1°
Repeatability: <1%

CS1 Slip Freq:

Pick-up: Setting ±0.01 Hz
Drop-off: (0.95 x Setting) ±0.01 Hz
Repeatability: <1%

CS1 Slip Timer:

Timers: Setting ±1% or 40 ms whichever is greater
Reset time: < 30 ms
Repeatability: <10mS

CS2

CS2 Phase Angle:

Pick-up: (Setting-2°) ±1°
Drop-off: (Setting-1°) ±1°
Repeatability: <1%

CS2 Slip Freq:

Pick-up: Setting ±0.01 Hz
Drop-off: (0.95 x Setting) ±0.01 Hz
Repeatability: <1%

CS2 Slip Timer:

Timers: Setting ±1% or 40 ms whichever is greater
Reset time: < 30 ms
Repeatability: <1%

CS2 Advanced CB Compensation Phase Angle:

Pick-up: 0°±1°
Drop-off: 2°±1°
Repeatability: <1%

CS2 Slip Timer:

Timers: CB Closing Timer
Repeatability: <10 mS

System Split

Accuracy

SS Phase Angle:

Pick-up: (Setting+2°) ±1°
Drop-off: (Setting+1°) ±1°
Repeatability: <1%

SS Undervoltage:

Pick-up: Setting ±3%
Drop-off: 1.02 x Setting
Repeatability: <1%

SS Timer:

Timers: Setting ±1% or 40 ms whichever is greater
Reset time: <30 ms
Repeatability: <10 ms

P348 Supervisory Functions

Voltage Transformer Supervision

Accuracy

V Diff Pick-up: Setting ±5%
V Diff Drop-off: 0.95 x Setting ±5%
VTS Block Operation: <1 cycle + 35ms
VTS Block reset: <35 ms
Time delay: Setting ±2% or 50 ms or 1 cycle whichever is greater

Current Transformer Supervision

Accuracy

IN > Pick-up: Setting ±5%
IN > Drop-off: 0.9 x Setting ±5%
CTS block operation: < 2 cycle + 80ms
Time delay: Setting (±2% +80ms) or (50 ms + 80ms) or (2 cycles + 80ms) whichever is greater

Plant Supervision

CB State Monitoring Control and Condition Monitoring

Accuracy

Timers: ±2% or 20 ms whichever is greater

TD

Broken current accuracy: ±5%

Programmable Scheme Logic

Accuracy

Output conditioner timer: Setting ±2% or 50 ms whichever is greater
Dwell conditioner timer: Setting ±2% or 50 ms whichever is greater
Pulse conditioner timer: Setting ±2% or 50 ms whichever is greater

TD

Measurements and Recording Facilities

Measurements

Accuracy

Current: 0.05…3 In: ±1% of reading
Voltage: 0.05…2 Vn: ±5% of reading
Power (W): 0.2…2 Vn, 0.05…3 In: ±5% of reading at unity power factor
Reactive Power (VArs): 0.2…2 Vn, 0.05…3 In: ±5% of reading at zero power factor
Apparent Power (VA): 0.2…2 Vn, 0.05…3 In: ±5% of reading
Energy (Wh): 0.2…2 Vn, 0.2…3 In: ±5% of reading at zero power factor
Energy (Varh): 0.2…2 Vn, 0.2…3 In: ±5% of reading at zero power factor
Phase accuracy: 0°…360: ±5%
Frequency: 5…70 Hz: ±0.025 Hz

IRIG-B and Real Time Clock

Performance

Year 2000: Compliant
Real time accuracy: < ±1 second / day

Features

Real time 24 hour clock settable in hours, minutes and seconds
Calendar settable from January 1994 to December 2092
Clock and calendar maintained via battery after loss of auxiliary supply
Internal clock synchronization using IRIG-B
Interface for IRIG-B signal is BNC

Current Loop Input and Outputs

Accuracy

Current loop input accuracy: ±1% of full scale
CLI drop-off threshold Under: setting ±1% of full scale
CLI drop-off threshold Over: setting ±1% of full scale
CLI sampling interval: 50 ms
CLI instantaneous operating time: < 250 ms
CLI DT operating time: ±2% setting or 200 ms whichever is the greater
CLO conversion interval: 50 ms
CLO latency: < 1.07 s or <70 ms depending on CLO output parameter's internal refresh rate - (1 s or 0.5 cycle)
Current loop output accuracy: ±0.5% of full scale
Repeatability: <5%
CLI - Current Loop Input
CLO - Current Loop Output

Other Specifications

CLI load resistance 0-1 mA: < 4 kΩ
CLI load resistance 0-1 mA/0-20 mA/4 20 mA: <300 Ω
Isolation between common input channels: zero
Isolation between input channels and case earth/other circuits: 2 kV rms for 1 minute
CLO compliance voltage 0-1 mA/0 10 mA: 10 V
CLO compliance voltage 0-20 mA/4 20 mA: 8.8 V
Isolation between common output channels: zero
Isolation between output channels and case earth/other circuits: 2 kV rms for 1 minute

Disturbance Records

Accuracy

Magnitude and relative phases: ±5% of applied quantities
Duration: ±2%
Trigger Position: ±2% (minimum 100 ms)
Record length: 50 records each 1.5 s duration (75 s total memory) with 8 analog channels and 32 digital channels (Courier, MODBUS, DNP 3.0), 8 records each 3 s (50 Hz) or 2.5 s (60 Hz) duration (IEC 60870-5-103).

Event, Fault & Maintenance Records

Maximum 512 events in a cyclic memory
Maximum 5 fault records
Maximum 10 maintenance records

Accuracy

Event time stamp resolution: 1 ms

IEC 61850/DNP 3.0 Ethernet Data

100 Base FX Interface

Transmitter Optical Characteristics
(TA = 0°C to 70°C, VCC = 4.75 V to 5.25 V)

Parameter	Sym	Min.	Typ.	Max.	Unit
Output Optical Power BOL 62.5/125 µm, NA = 0.275 Fiber EOL	PO	-19 -20	-16.8	-14	dBm avg.
Output Optical Power BOL 50/125 µm, NA = 0.20 Fiber EOL	PO	-22.5 -23.5	-20.3	-14	dBm avg.
Optical Extinction Ratio				10 -10	% dB
Output Optical Power at Logic “0” State	PO (“0”)			-45	dBm avg.

BOL - Beginning of life
EOL - End of life

Receiver Optical Characteristics
(TA = 0°C to 70°C, VCC = 4.75 V to 5.25 V)

Parameter	Sym	Min.	Typ.	Max.	Unit
Input Optical Power Minimum at Window Edge	PIN Min. (W)		-33.5	–31	dBm avg.
Input Optical Power Minimum at Eye Center	PIN Min. (C)		-34.5	-31.8	Bm avg.
Input Optical Power Maximum	PIN Max.	-14	-11.8		dBm avg.

Note: The 10BaseFL connection will no longer be supported as IEC 61850 does not specify this interface.

TD

TD

Settings, Measurements and Records List

Settings List

Global Settings (System Data)

Language:
English/French/German/Spanish/Russian
Password: ********
Sys Fn Links:
0 (Trip LED latched), 1 (Trip LED self reset)
Description: **********
Plant Reference: **********
Relay Address: 0…255
Frequency: 50/60 Hz
CB Control: No Operation Trip, Close
Access Level: 0, 1,2,3
Password Level 1: ********
Password Level 2: ********
Password Level 3: ********

Circuit Breaker Control (CB Control)

CB Control by:
- Disabled
- Local
- Remote
- Local+Remote
- Opto
- Opto+local
- Opto+Remote
- Opto+Rem+local

Close Pulse Time:	0.10…10.00 s
Trip Pulse Time:	0.10…5.00 s
Man Close Delay:	0.01…600.00 s
CB Healthy Time:	0.01…9999.00 s
Sys Check Time:	0.01…9999.00 s
Reset Lockout by:	User Interface/CB Close
Man Close RstDly:	0.10…600.00 s

CB Status Input:
- None
- 52A
- 52B
- 52A & 52B

Date and Time

IRIG-B Sync:	Disabled, Enabled
Battery Alarm:	Disabled, Enabled
LocalTime Enable:	Disabled/Fixed/Flexible
LocalTime Offset:	-720 min…720min
DST Enable:	Disabled, Enabled
DST Offset:	30min…60min
DST Start:	First/Second/Third/ Fourth/Last
DST Start Day:	Sun/Mon/Tues/Wed/ Thurs/Fri/Sat
DST Start Month:	Jan/Feb/Mar/Apr/May/ Jun/Jul/Aug/Sept/ Oct/Nov/Dec
DST Start Mins:	0min…1425min
DST End:	First/Second/Third/ Fourth/Last
DST End Day:	Sun/Mon/Tues/Wed/ Thurs/Fri/Sat
DST End Month:	Jan/Feb/Mar/Apr/May/ Jun/Jul/Aug/Sept/Oct/ Nov/Dec
DSTEnd Mins:	0min…1425min
RP1 Time Zone:	UTC/Local
RP2 Time Zone:	UTC/Local
Tunnel Time Zone:	TC/Local

Configuration

Setting Group:
- Select via Menu
- Select via Opto

Active Settings:	Group 1/2/3/4
Setting Group 1:	Disabled, Enabled
Setting Group 2:	Disabled, Enabled
Setting Group 3:	Disabled, Enabled
Setting Group 4:	Disabled, Enabled
System Config:	Invisible, Visible
Power:	Disabled, Enabled
Field Failure:	Disabled, Enabled
NPS Thermal:	Disabled, Enabled
System Back-up:	Disabled, Enabled
Overcurrent:	Disabled, Enabled
Thermal Overload:	Disabled, Enabled
Differential:	Disabled, Enabled
Earth Fault:	Disabled, Enabled
Rotor EF	Disabled, Enabled
SEF/REF/Spower:	Disabled or SEF/REF or Sensitive Power
Residual O/V NVD:	Disabled, Enabled
100% Stator EF:	Disabled, Enabled
V/Hz:	Disabled, Enabled
df/dt:	Disabled, Enabled
Dead Machine:	Disabled, Enabled
Volt Protection:	Disabled, Enabled
Freq Protection:	Disabled, Enabled
RTD Inputs:	Disabled, Enabled
CB Fail:	Disabled, Enabled
Supervision:	Disabled, Enabled
Pole Slipping:	Disabled, Enabled
Input Labels:	Invisible, Visible
Output Labels:	Invisible, Visible
RTD Labels:	Invisible, Visible
CT & VT Ratios:	Invisible, Visible
Event Recorder:	Invisible, Visible
Disturb Recorder:	Invisible, Visible
Measure't Setup:	Invisible, Visible
Comms Settings:	Invisible, Visible
Commission Tests:	Invisible, Visible
Setting Values:	Primary, Secondary
Control Inputs:	Invisible, Visible
CLIO Inputs:	Disabled, Enabled

CLIO Outputs: Disabled, Enabled
System Checks: Disabled, Enabled
Ctrl I/P Config: Invisible, Visible
Ctrl I/P Labels: Invisible, Visible
Direct Access: Disabled, Enabled
IEC GOOSE Invisible, Visible
Function Keys: Invisible, Visible
RP1 Read Only Disabled, Enabled
RP2 Read Only Disabled, Enabled
NIC Read Only Disabled, Enabled
LCD Contrast: 0…31

CT and VT Ratios

Main VT Primary: 100...1000000 V (P342-6/8)
Main VT Sec'y: 80...140 V (100/120 V) 320…560 V (380/480 V) (P342-6/8)
C/S VT Primary: 100 V...1 MV (P345)
C/S VT Secondary: 80...140 V (P345)
VN1 Primary: 100…1000000 V (P342-6)
VN1 VT Sec'y: 80…140 V (100/120 V) 320…560 V (380/480 V) (P342-6)
VN2 Primary: 100…1000000 V (P344/5)
VN2 VT Sec'y: 80…140 V (100/120 V) 320…560 V (380/480 V) (P344/5)
Ph CT Polarity/Ph CT1 Polarity:
Standard/Inverted (P342-6/8)
Phase CT Primary/Phase CT1 Primary:
1A…60 kA (P342-6/8)
Phase CT Sec'y/Phase CT1 Sec'y: 1A/5A (P342-6/8)
Ph CT2 Polarity:Standard/Inverted (P343-6/8)
Phase CT2 Primary: 1A…60 kA (P343-6/8)
Phase CT2 Sec'y: 1A/5A (P343-6/8)
E/F CT Polarity: Standard/Inverted (P342-6)
E/F CT Primary: 1A…60 KA(P342-6)
E/F CT Sec'y: 1A/5A
Isen CT Polarity: Standard, Inverted (P342-6)
ISen CT Primary: 1A…60 KA(P342-6)
ISen CT Sec'y: 1A/5A (P342-6)

Sequence of Event Recorder (Record Control)

Alarm Event: Disabled, Enabled
Relay O/P Event: Disabled, Enabled
Opto Input Event: Disabled, Enabled
General Event: Disabled, Enabled
Fault Rec Event: Disabled, Enabled
Maint Rec Event: Disabled, Enabled
Protection Event: Disabled, Enabled
DDB 31 - 0: (up to):
DDB 2047 - 2016:
Binary function link strings, selecting which DDB signals will be stored as events, and which will be filtered out.

Oscillography (Disturbance Recorder)

Duration: 0.10…10.50 s
Trigger Position: 0.0…100.0%
Trigger Mode: Single/Extended
Analog Channel 1: (up to):
Analog Channel 20:
Disturbance channels (P342-6) selected from:
Unused, VA, VB, VC, VN1, IA-1, IB-1, IC-1, IN, I Sensitive1, IA-2, IB-2, IC-2, VN2, I Sensitive2, V64S, I64S, Frequency, 64R CL Input Raw, 64R R Fault Raw, 64R R Fault, C/S voltage, 3 Phase Watts, 3 Phase VArs, 1Ph Sen Watts, 1Ph Sen VArs, 3Ph Sen Watts, 3Ph Sen VArs
P348:
Unused, VA-1, VB-1, VC-1, VN-1 Derived, VAB-1, VBC-1, VCA-1, VA-2, VB-2, VC-2, IA-1, IB-1, IC-1, IA-2, IB-2, IC-2, I2 CT2, VA-1 RMS, VB-1 RMS, VC-1 RMS, VN-1 Derived RMS, VAB-1 RMS, VBC-1 RMS, VCA-1 RMS, IA-1 RMS, IB-1 RMS, IC-1 RMS, IA-2 RMS, IB-2 RMS, IC-2 RMS, I2 CTS RMS, IN-2 Derived RMS, Frequency, Frequency 2.
Digital Input 1: (up to):
Digital Input 32:
Selected binary channel assignment from any DDB status point within the relay (opto input, output contact, alarms, starts, trips, controls, logic…).
Input 1 Trigger: No Trigger/Trigger/LH (Low to High)/Trigger H/L (High to Low)
(up to):
Input 32 Trigger: No Trigger/Trigger L/H/Trigger H/L

Measured Operating Data (Measure't Setup)

Default Display (P342-6):
User Banner
3Ph + N Current
3Ph Voltage
Power
Date and Time
Description
Plant Reference
Frequency
Access Level
Default Display (P348):
User Banner
3Ph Current
3Ph Voltage
3Ph Current 2
Date and Time

TD

TD

Description
Plant Reference
Frequency
Access Level
Frequency 2
Local Values: Primary, Secondary
Remote Values: Primary, Secondary
Measurement Ref: VA/VB/VC/IA/IB/IC
Measurement Mode: 0/1/2/3
Fix Dem Period: 1…99mins
Roll Sub Period: 1…99mins
Num Sub Periods: 1…15
Remote2 Values: Primary, Secondary

Communications

RP1 Address: (Courier or IEC870-5-103):
0…255
RP1 Address: (DNP3.0):
0…65534
RP1 Address: (MODBUS):
1…247
RP1 InactivTimer: 1…30mins
RP1 Baud Rate: (IEC870-5-103):
9600/19200 bits/s
RP1 Baud Rate: (MODBUS, Courier):
9600/19200/38400 bits/s
RP1 Baud Rate: (DNP3.0):
1200/2400/4800/9600/19200/ 38400 bits/s
RP1 Parity: Odd/Even/None
(MODBUS, DNP3.0)
RP1 Meas Period: 1…60 s
(IEC870-5-103)
RP1 PhysicalLink:
Copper (EIA(RS)485/K bus) or Fiber Optic
RP1 Time Sync: Disabled, Enabled
MODBUS IEC Timer: Standard, Reverse
RP1 CS103Blocking:
Disabled
Monitor Blocking
Command Blocking
RP1 Port Config: (Courier):
K Bus
EIA485 (RS485)

RP1 Comms Mode: (Courier):
IEC60870 FT1.2
IEC60870 10-Bit No parity

Note: If RP1 Port Config is K Bus the baud rate is fixed at 64 kbits/s

DNP 3.0 Need Time: 1…30 mins
DNP App Fragment: 100…2048 bytes
DNP App Timeout: 1…120 s
DNP SBO Timeout: 0…120 s
DNP Link Timeout: 0…120 s

Optional DNP 3.0 Over Ethernet Port

IP Address
Subnet Mask
NIC MAC Address
Gateway

DNP 3.0 Time Sync: Disabled, Enabled
Meas. Scaling:
Normalized, Primary, Secondary
NIC Tunl Timeout: 1…30 mins
NIC Link Report: Alarm, Event, None
NIC Link Timeout: 0.1…60 s
SNTP Poll Rate: 64…1024 s
DNP Need Time: 1…30 mins
DNP App Fragment: 100…2048 bytes
DNP App Timeout: 1…120 s
DNP SBO Timeout: 1…10 s

Optional IEC 61850 Ethernet Port NIC MAC Address

NIC Tunl Timeout: 1...30mins
NIC Link Report: Alarm, Event, None
NIC Link Timeout: 0.1...60 s

Optional Additional Second Rear Communication (Rear Port2 (RP2))

RP2 Port Config:
EIA(RS)232
EIA(RS)485
K-Bus
RP2 Comms Mode:
IEC60870 FT1.2
IEC60870 10-Bit No parity
RP2 Address: 0…255
RP2 InactivTimer: 1…30mins
RP2 Baud Rate:
9600/19200/38400 bits/s
Note: If RP2 Port Config is K Bus the baud rate is fixed at 64 kbits/s

IEC 61850-9-2 LE Ethernet Port

Physical Link: Copper, Fibre Optic
AntiAlias Filter: Disabled, Enabled
Synchro Alarm:
No Sync, Local 1PPS, Global 1PPS
9.2 Test Mode:
Test Bocked, Test Ignored, Test Only
Merge Unit Delay: 0.00…3.00ms
LN Count: 1…8
LN1-8 Name: ********
IA1 IB1 IC1: Unused, LN1…LN8
IA2 IB2 IC2: Unused, LN1…LN8
VA VB VC: Unused, LN1…LN8
VA2 VB2 VC2: Unused, LN1…LN8
MUs Delay Search: No, Yes
Trust Ques Data: 000000 (0=No, 1=Yes)
Loss Rate Level: 5…15%
Frame Loss Rate: Disabled, Enabled
Loss Rate Reset: No, Yes

Commission Tests

Monitor Bit 1:
(up to):
Monitor Bit 8:

Binary function link strings, selecting which DDB signals have their status visible in the Commissioning menu, for test purposes
Test Mode:
Disabled
Test Mode
Blocked Contacts
Test Pattern:
Configuration of which output contacts are to be energized when the contact test is applied

Circuit Breaker Condition Monitoring (CB Monitor Setup)

Broken I^: 1.0…2.0
I^ Maintenance: Alarm Disabled, Enabled
I^ Maintenance: 1…25000
I^ Lockout: Alarm Disabled, Enabled
I^ Lockout: 1…25000
No. CB Ops Maint: Alarm Disabled, Enabled
No. CB Ops Maint: 1…10000
No. CB Ops Lock: Alarm Disabled, Enabled
No. CB Ops Lock: 1…10000
CB Time Maint: Alarm Disabled, Enabled
CB Time Maint: 0.005…0.500 s
CB Time Lockout: Alarm Disabled, Enabled
CB Time Lockout: 0.005…0.500 s

Fault Freq Lock: Alarm Disabled, Enabled
Fault Freq Count: 1…9999
Fault Freq Time: 0…9999 s

Opto Coupled Binary Inputs (Opto Config)

Global Nominal V:
24 - 27 V
30 - 34 V
48 - 54 V
110 - 125 V
220 - 250 V
Custom
Opto Input 1:
(up to):
Opto Input #. (# = max. opto no. fitted):
Custom options allow independent thresholds to be set per opto, from the same range as above.
Opto Filter Control:
Binary function link string, selecting which optos will have an extra 1/2 cycle noise filter, and which will not.
Characteristics:
Standard 60% - 80%
50% - 70%

Control Inputs into PSL (Ctrl. I/P Config.)

Hotkey Enabled:
Binary function link string, selecting which of the control inputs will be driven from Hotkeys.

Control Input 1: Latched, Pulsed
(up to):
Control Input 32 Latched, Pulsed
Ctrl Command 1:
(up to):
Ctrl Command 32:
ON/OFF
SET/RESET
IN/OUT
DISABLED, ENABLED

Function Keys

Fn. Key Status 1:
(up to):
Fn. Key Status 10
Disable
Lock
Unlock/Enable
Fn. Key 1 Mode: Toggled, Normal
(up to):
Fn. Key 10 Mode: Toggled, Normal
Fn. Key 1 Label:
(up to):
Fn. Key 10 Label:
User defined text string to describe the function of the particular function key

IED Configurator

Switch Conf. Bank: No Action/Switch Banks
Restore MCL: No Action, Restore MCL

Security Config

User Banner: **********
Attempts Limit: 0…3
Attempts Timer: 1…3 min
Blocking Timer: 1…30 min
Front Port: Disabled, Enabled
Rear Port 1: Disabled, Enabled
Rear Port 2: Disabled, Enabled
Ethernet Port: Disabled, Enabled
Courier Tunnel: Disabled, Enabled
IEC 61850: Disabled, Enabled
DNP OE: Disabled, Enabled
Fallback Level: Level 0/1/2/3

IEC 61850 GOOSE

GoEna: Disabled, Enabled
Test Mode: Disabled/Pass Through/Forced
VOP Test Pattern: 0x00000000...
0xFFFFFFFF
Ignore Test Flag: No/Yes

TD

Control Input User Labels (Ctrl. I/P Labels)

Control Input 1:
(up to):
Control Input 32:
User defined text string to describe the function of the particular control input

Settings in Multiple Groups

Note: All settings here onwards apply for setting groups # = 1 to 4.

User Curves Data

Curve 1/2/3/4 Name: **********
UserCurve 1/2/3/4 Type:
Operate 1.0, Reset 1.1, V/Hz Operate 3.0, V/Hz 3.1, UV Operate 4.0

Protection Functions

System Config

Winding Type: Generator/Gen-Xformer
Ref Power S: 0.1…5000 M
HV Connection: D-Delta/Y-Wye/Z-Zigzag
HV Grounding: Grounded/Ungrounded
HV Nominal: 100 V to 1 MV
%Reactance: 1.00% to 100.00%
LV Vector Group: 0 to 11
LV Connection: D-Delta/Y-Wye/Z-Zigzag
LV Grounding: Grounded/Ungrounded
LV Nominal: 100 V to 1 MV
Phase Sequence: Standard ABC/Reverse ACB
VT Reversal: No Swap/A-B Swapped/B-C Swapped/C-A Swapped
CT1 Reversal: No Swap/A-B Swapped/B-C Swapped/C-A Swapped
CT2 Reversal: No Swap/A-B Swapped/B-C Swapped/C-A Swapped
C/S Input: A-N, B-N, C-N, A-B, B-C, C-A
C/S V Ratio Corr: 0.100...2.000
Main VT Vect Grp: 0...11
Main VT Location: Gen/Bus
RMS F<Block: 0.1…2.0Hz (P348)
CounterSourcePSL: 00000000000000000
Counter 1-16: 1…65535
Counter1-16 Label: **********
Timer1-16: 0…14400 ms

Generator Differential Protection

GenDiff Function:
Disabled/Percentage Bias
High Impedance
Interturn
Gen Diff Is1: 0.05…0.50 In
Gen Diff k1: 0…20%
Gen Diff Is2: 1…5.0 In
Gen Diff k2: 20…150.00%
Interturn Is_A: 0.05…2.0 In
Interturn Is_B: 0.05…2.0 In
Interturn Is_C: 0.05…2.0 In
Interturn Delay: 0.00…100.0 s

Xformer Diff protection

Xform Diff Func: Disabled, Enabled
Set Mode: Simple/Advance
Xform Is1: 0.05 to 2.50 PU
Xform K1: 0 to 150%
Xform Is2: 0.10 to 10.0 PU
Xform K2: 15 to 150%
Xform tDiff: 0 to 10.00 s
Xform Is-CTS: 0.10 to 2.50 PU
Xform HS1 Status: Disabled, Enabled
Xform Is-HS1: 2.50 to 16.0 PU
Xform HS2 Status: Disabled, Enabled
Xform Is-HS2: 2.50 to 16.0 PU
Zero seq filt HV: Disabled, Enabled
Zero seq filt LV: Disabled, Enabled
2nd harm blocked: Disabled, Enabled
Xform Ih(2)%>: 5 to 50%
Cross blocking: Disabled, Enabled
5th harm blocked: Disabled, Enabled
Xform Ih(5)%>: 0 to 100%
Circuitry Fail: Disabled, Enabled
Is-cctfail>: 0.03 to 1.00 PU
K-cctfail: 0 to 50%
tls-cctfail>: 0 to 10.0 s

Power (3 Phase)

Comp Angle: -5°…5°
Power1 Function: Disabled, Under, Over
Power1 Dirn: Forward, Reverse
Power1 Mode: Active, Reactive
Power1 3Ph Watts, Power1 3Ph VArs:
0.4…300.0 W (1A, 100 V/120 V)
1.6…1200.0 W (1A, 380 V/480 V)
2…1500.0 W (5A, 100 V/120 V)
8…6000.0 W (5A, 380 V/480 V)
Equivalent Range in %Pn 0.2%…157%
Power 1 Time Delay: 0.00…100.0 s
Power 1 DO Timer: 0.00…100.0 s
P1 Poledead Inh: Disabled, Enabled
Power 2/3/4 as Power 1

Sensitive Power (1 Phase/2 Phase)

Comp Angle: -5°…5°
P> CT Source: Single, Wattmetric
P> Phase Select: A, B, C
Sen Power1 Func: Disabled, Under, Over
Sen Power1 Dirn: Forward, Reverse
Sen Power1 Mode: Active, Reactive
Sen Power1 1Ph Watt, Sen Power1 1Ph VArs:
0.2…100.0W (1A, 100/120 V)
0.8…400.0W (1A, 380/480 V)
1…500.0W (5A, 100/120 V)
4…2000.0W (5A, 380/480 V)
Equivalent range in %Pn 0.3%…157%
Sen Power1 3Ph Watt, Sen Power1 3Ph VArs:
0.4…100.0W (1A, 100/120 V)
1.6…400.0W (1A, 380/480 V)
2…500.0W (5A, 100/120 V)
8…2000.0W (5A, 380/480 V)
Equivalent range in %Pn 0.2%…157%
Sen Power 1 Delay: 0.00…100.0 s
Power 1 DO Timer: 0.00…100.0 s
P1 Poledead Inh: Disabled, Enabled
Sen Power2/3/4 as Sen Power 1

NPS Overpower

S2> CT Source: IA-1 IB-1 IC-1/IA-2 IB-2 IC-2
S2>1 Status: Disabled, Enabled
S2>1 Setting: 0.10…30.00 In VA (100/120 V)
0.40…120.00 In VA (380/480 V)
S2> 1 Time Delay: 0.00…100.00 s

Field Failure

FFail Alm Status: Disabled, Enabled
FFail Alm Angle: 15°…75°

TD

FFail Alm Delay: 0.00…100.0 s
FFail 1 Status: Disabled, Enabled
FFail 1 Xa1:
-250.0…250.0 Ω (1A, 100/120 V)
-1250.0…1250.0 Ω (5A, 100/120 V)
-1000…1000 Ω (1A, 380/480 V)
-5000.0…5000.0 Ω (5A, 380/480 V)
FFail 1 Xb1:
0.5…500.0 Ω (1A, 100/120 V)
2.5…2500.0 Ω (5A, 100/120 V)
2…2000 Ω (1A, 380/480 V)
10…10000.0 Ω (5A, 380/480 V)
FFail 1 Time Delay: 0…100 s
FFail 1 DO Timer: 0…100 s
FFail 2 as FFail1
FFail Dirn Line: Disabled, Enabled
Line Offset
-250.0…250.0 Ω (1A, 100/120 V)
-1250.0…1250.0 Ω (5A, 100/120 V)
-1000…1000 Ω (1A, 380/480 V)
-5000.0…5000.0 Ω (5A, 380/480 V)
Line Angle: -180°...180°

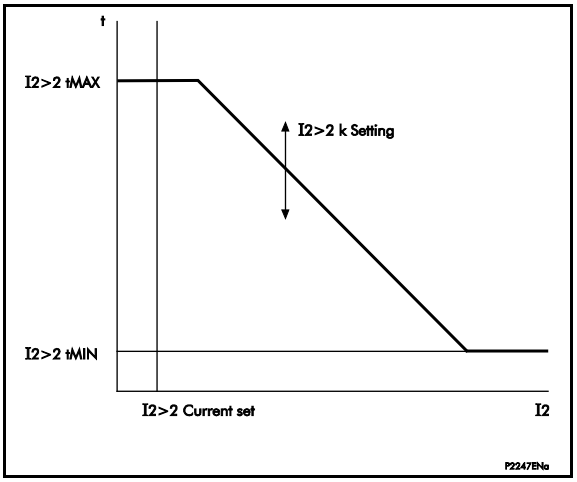
NPS Thermal

I2therm>1 Alarm: Disabled, Enabled
I2therm>1 Set: 0.03…0.5 In
I2therm>1 Delay: 0…100 s
I2therm>2 Trip: Disabled, Enabled
I2therm>2 Set: 0.05…0.5 In
I2therm>2 k Set: 2…40.0 s
I2therm>2 kRESET: 2…40.0
I2therm>2 tMAX: 500…2000.00 s
I2therm>2 tMIN: 0.25…40 s

The P34x negative phase sequence element offers a true thermal characteristic according to the following formula:

$$t = - \frac{(I2>2\ k\ Setting)}{(I2>2\ Current\ set)^2} \log_e \left(1 - \left(\frac{(I2>2\ Current\ set)}{I_2} \right)^2 \right)$$

Note: All current terms are in per-unit, based on the relay rated current, In.



Negative phase sequence thermal characteristic

System Backup

Voltage Dependent Overcurrent and Underimpedance

V Dep OC Func:
Disabled
Voltage Controlled
Voltage Restrained
Backup Function:
Disabled
Voltage Controlled
Voltage Restrained
Under Impedance
Vector Rotation: None/Delta-Star
V Dep OC Char:
DT
IEC S Inverse
IEC V Inverse
IEC E Inverse
UK LT Inverse
UK Rectifier
RI
IEEE M Inverse
IEEE V Inverse
IEEE E Inverse
US Inverse
US ST Inverse
Default Curve 1/2/3/4
V Dep OC I > Set: 0.8…4In
V Dep OC T Dial: 0.01…100
V Dep OC Reset: DT or Inverse
V Dep OC Delay: 0…100 s
V Dep OC TMS: 0.025…1.2
V Dep OC K(RI): 0.1…10
V Dep OC Usr Rst: DT, Default Curve 1/2/3/4
V Dep OC tRESET: 0…100 s
V Dep OC V<1/2 Set: 5…120 V (100/120 V)
V Dep OC V<1/2 Set: 20…480 V (380/480 V)
V Dep OC k Set: 0.1…1
Z< Function: Disabled, Enabled
Vector Rotation: None/Delta-Star
Z<1 Status: Disabled, Enabled

Z<1 Setting:
2…500.0 Ω (1A, 100/120 V)
0.4…2500.0 Ω (5A, 100/120 V)
8…2000 Ω (1A, 380/440 V)
1.60…10000.0 Ω (5A, 380/440 V)
Z<1 Time Delay: 0.00…100.0 s
Z<1 tRESET: 0…100 s
Z<2 as Z<1

Inverse time (IDMT) characteristic
IDMT characteristics are selectable from a choice of four IEC/UK and five IEEE/US curves as shown in the table below.
The IEC/UK IDMT curves conform to the following formula:

$$t = T \times \left(\frac{K}{(I/I_S)^{\alpha} - 1} + L \right)$$

The IEEE/US IDMT curves conform to the following formula:

$$t = TD \times \left(\frac{K}{(I/I_S)^{\alpha} - 1} + L \right)$$

Where:
t = Operation time
K = Constant
I = Measured current
Is = Current threshold setting
α = Constant
L = ANSI/IEEE constant (zero for IEC/UK curves)
T = Time multiplier setting for IEC/UK curves
TD = Time dial setting for IEEE/US curves

IDMT characteristics

IDMT Curve	Stand.	K	α	L
Standard inverse	IEC	0.14	0.02	0
Very inverse	IEC	13.5	1	0
Extremely inverse	IEC	80	2	0
Long time inverse	UK	120	1	0
Rectifier	UK	45900	5.6	0
Moderately inverse	IEEE	0.0515	0.02	0.114
Very inverse	IEEE	19.61	2	0.491
Extremely inverse	IEEE	28.2	2	0.1217
Inverse	US-C08	5.95	2	0.18
Short time inverse	US-C02	0.16758	0.02	0.11858

The IEC extremely inverse curve becomes definite time at currents greater than 20 x setting. The IEC standard, very and long time inverse curves become definite time at currents greater than 30 x setting.

The definite time part of the IEC inverse time characteristics at currents greater than 20x and 30x setting are only relevant for currents in the operating range of the relay.

The operating range of the P342/3/4/5 current inputs is 0 - 16 In for the standard current inputs and is 0 - 2 In for the sensitive current input.

For all IEC/UK curves, the reset characteristic is definite time only.

For all IEEE/US curves, the reset characteristic can be selected as either inverse curve or definite time.

The inverse reset characteristics are dependent upon the selected IEEE/US IDMT curve as shown in the table below.

All inverse reset curves conform to the following formula:

$$tRESET = \frac{TD \times S}{(1 - M^2)} \text{ in seconds}$$

Where:

TD = Time dial setting for IEEE curves
S = Constant
M = I/Is

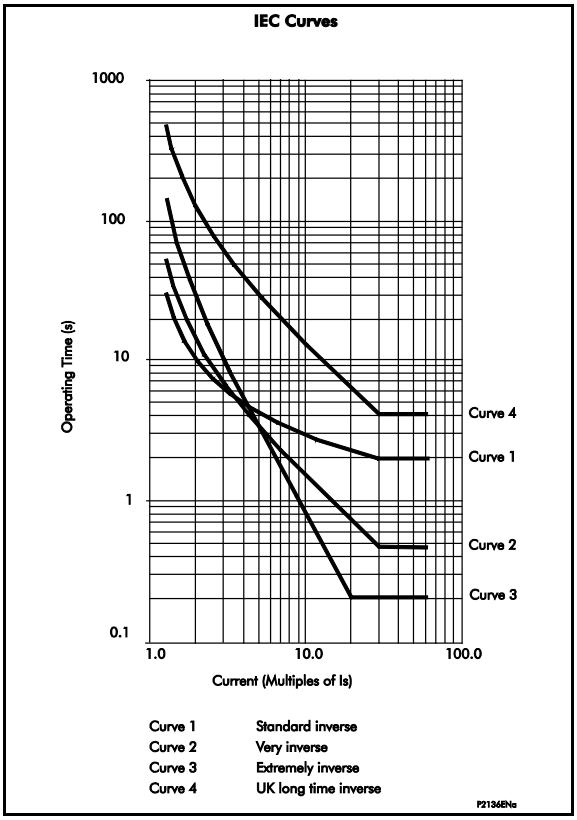
Curve Description	Standard	S
Moderately inverse	IEEE	4.85
Very inverse	IEEE	21.6
Extremely inverse	IEEE	29.1
Inverse	US	5.95
Short time inverse	US	2.261

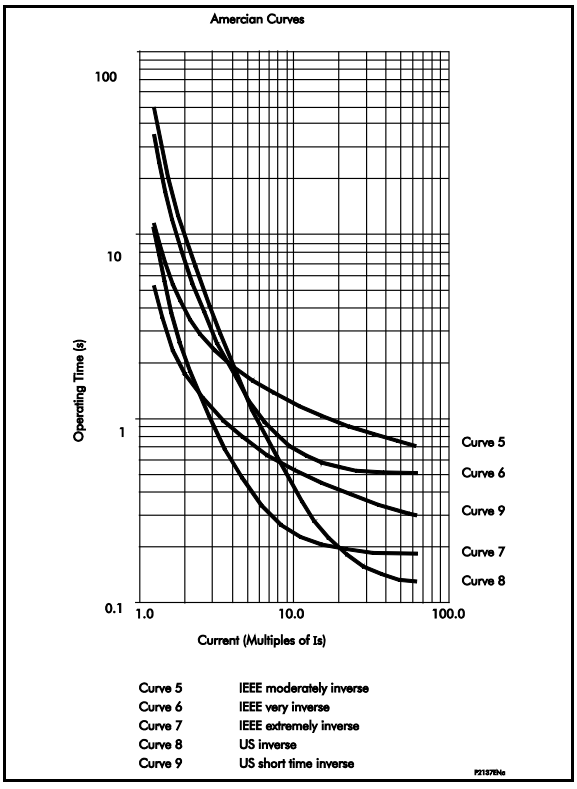
The RI curve (electromechanical) has been included in the first stage characteristic setting options for Phase Overcurrent and Earth Fault protections. The curve is represented by the following equation:

$$t = K \times \left(\frac{1}{0.339 - \left({}^{0.236}/_{M} \right)} \right) \text{ in seconds}$$

With K adjustable from 0.1 to 10 in steps of 0.05
M = I/Is

TD





Phase Overcurrent (Overcurrent)

Phase O/C: Sub Heading
I> CT Source: IA-1 IB-1 IC-1/IA-2 IB-2 IC-2
I>1 Function:
  Disabled
  DT
  IEC S Inverse
  IEC V Inverse
  IEC E Inverse
  UK LT Inverse
  UK Rectifier
  RI
  IEEE M Inverse
  IEEE V Inverse
  IEEE E Inverse
  US Inverse
  US ST Inverse
  Default Curve 1/2/3/4
I>1 Direction:
  Non-Directional
  Directional Fwd
  Directional Rev
I>1 Current Set: 0.08…4.00 In
I>1 Time Delay: 0.00…200.00 s
I>1 TMS: 0.025…1.200
I>1 Time Dial: 0.01…100.00
I>1 K (RI): 0.10…10.00
I>1 Reset Char: DT/Inverse
I>1 Usr Rst Char: DT, Default Curve 1/2/3/4
I>1 tRESET: 0.00…100.00 s
I>2 as I>1
I>3 Status: Disabled, Enabled
I>3 Direction:
  Non-Directional
  Directional Fwd
  Directional Rev
I>3 Current Set: 0.08…10.00 In
I>3 Time Delay: 0.00…200.00 s
I>4 as I>3
I> Char Angle: -95…+95°
I >Function Link:
  Bit 0 = VTS Blocks I>1
  Bit 1 = VTS Blocks I>2
  Bit 2 = VTS Blocks I>3
  Bit 3 = VTS Blocks I>4
  Bit 4, 5, 6 & 7 are not used
  Binary function link string, selecting which overcurrent elements (stages 1 to 4) will be blocked if VTS detection of fuse failure occurs.

Peak/RMS Overcurrent (P348)

Phase O/C Peak: Sub Heading
I>1 Status: Disabled, Enabled
I>1 CT Source: IA-1, IB-1, IC-1/IA-2, IB-2, IC-2
I>1 Current Set: 0.08…32.00 In
I>1 Time Delay: 0.00…200.00 s
I>1 tRESET: 0.00…100.00 s
I>1 SV Iterations: 1…10
I>2/3/4 as I>1
Phase O/C RMS: Sub Heading
I>5 Function:
  Disabled
  DT
  IEC S Inverse
  IEC V Inverse
  IEC E Inverse

UK LT Inverse
UK Rectifier
RI
IEEE M Inverse
IEEE V Inverse
IEEE E Inverse
US Inverse
US ST Inverse
Default Curve 1/2/3/4
I>5 CT Source: IA-1 IB-1 IC-1/IA-2 IB-2 IC-2
I>5 Current Set: 0.08…32.00 In
I>5 Time Delay: 0.00…200.00 s
I>1 TMS: 0.025…1.200
I>1 Time Dial: 0.01…100.00
I>1 K (RI): 0.10…10.00
I>5 tRESET: 0.00…100.00 s
I>6 as I>5
I>7 Status: Disabled, Enabled
I>7 CT Source: IA-1, IB-1, IC-1/IA-2, IB-2, IC-2
I>7 Current Set: 0.08…32.00 In
I>7 Time Delay: 0.00…200.00 s
I>8 as I>7

NPS Overcurrent

I2> CT Source: IA-1 IB-1 IC-1/IA-2 IB-2 IC-2
I2>1 Status: Disabled, Enabled
I2>1 Direction:
Non-Directional
Directional Fwd
Directional Rev
I2> Current Set: 0.08…4.00 In
I2> Time Delay: 0.00…100.00 s
I2>2/3/4 as for I2>1
I2> VTS Block:
Bit 0 = VTS Blocks I2>1
Bit 1 = VTS Blocks I2>2
Bit 2 = VTS Blocks I2>3
Bit 3 = VTS Blocks I2>4
Bits 4, 5, 6 & 7 are not used
Binary function link string, selecting which NPS overcurrent elements (stages 1 to 4) will be blocked if VTS detection of fuse failure occurs.
I2> V2pol Set: 0.5…25.0 (100 V 120 V)
2…100 V(380/480 V)
I2> Char Angle: -95°…+95°

NPS Overcurrent (P348)

I2>1 Status: Disabled, Enabled
I2>1 Current Set: 0.03…4.00 In
I2>1 Time Delay: 0.00…200.00 s
I2>2/3/4 as I>1

Thermal Overload

Gen Thermal: Sub Heading
Thermal status: Disabled, Enabled
Thermal I>: 0.50…2.50 In
Thermal Alarm: 20..100%
T-heating: 1…200 minutes
T-cooling: 1…200 minutes
M Factor: 0…10

The thermal time characteristic is given by:

$t = \tau \log_e (Ieq^2 - IP^2)/(I_{eq}^2 - (\text{Thermal } I>)^2)$
$t = \tau . \log_e (K^2-A^2/(K^2-1))$

Where:
$K = I_{eq}/\text{Thermal } I>$
$A = I_P /\text{Thermal } I>$
t = Time to trip, following application of the overload current, I
τ = Heating time constant of the protected plant
I_{eq} = Equivalent current
Thermal I> = Relay setting current
I_P = Steady state pre-load current before application of the overload
I_{eq} = $\sqrt{(I_1^2 + MI_2^2)}$
I1 = Positive sequence current
I2 = Negative sequence current
M = A user settable constant proportional to the thermal capacity of the machine

Xformer Thermal: Sub Heading
Thermal status: Disabled, Enabled
Mn't Winding: HV/LV/ Biased Current
Ambient T: RTD1-10/CLIO1-4/AVERAGE
Amb CLIO Type: 0-1 / 0-10 / 0-20 / 4-20 mA
Amb CLIO Min: -9999.0 to +9999.0
Amb CLIO Max: -9999.0 to +9999.0
Average Amb T: -25.0 to +75.0 Cel
Top Oil T: RTD1-10/CIO1-4/CALCULATED
Top Oil CLIO Typ: 0-1 / 0-10 / 0-20 / 4-20 mA
Top Oil CLIO Min: -9999.0 to +9999.0
Top Oil CLIO Max: -9999.0 to +9999.0
IB: 0.1 to 4.0 PU
Rated NoLoadLoss: 0.1 to 100.0
Hot Spot Overtop: 0.1 to 200.0 Cel
Top Oil Overamb: 0.1 to 200.0 Cel
Cooling Mode: Natural/Forced Air/ Forced Oil/ Forced Air & Oil/Select via PSL
Natural Cooling/Forced Air Cool/Forced Oil Cool/Frced AirOil Cool:
Winding exp m: 0.01 to 2.00
Oil exp n: 0.01 to 2.00
Hot spot rise co: 0.01 to 20.00 min
Top oil rise co: 1 to 1000 min
TOL Status: Disabled, Enabled
Hot Spot>1 to 3 Set: 1.0 to 300.0 Cel
tHot Spot>1 to 3 Set: 0 to 60 k min
Top Oil>1 to 3 Set: 1.0 to 300.0 Cel
tTop Oil>1 to 3 Set: 0 to 60 k min
tPre-trip Set: 0 to 60k min
LOL Status: Disabled, Enabled
Life Hours at HS: 1 to 300,000 hr
Designed HS temp: 1 to 200.0 Cel
Constant B Set: 1 to 100,000
FAA> Set: 0.10 to 30.00 min
tFAA> Set: 0 to 60 k min

LOL>1 Set: 1 to 300,000 hr
tLOL> Set: 10 to 60 k min
Reset Life Hours: 0 to 300,000 hr

2-Stage Non-Directional Earth Fault

IN>1 Function:
- Disabled
- DT
- IEC S Inverse
- IEC V Inverse
- IEC E Inverse
- UK LT Inverse
- RI
- IEEE M Inverse
- IEEE V Inverse
- IEEE E Inverse
- US Inverse
- US ST Inverse
- IDG
- Default Curve 1/2/3/4

IN>1 Current: 0.02…4 In
IN>1 IDG Is: 1…4 In
IN>1 Time Delay: 0.00…200.0 s
IN>1 TMS: 0.025…1.200
IN>1 Time Dial: 0.01…100.00
IN>1 K(RI): 0.1…10.00
IN>1 IDG Time: 1…2.00
IN>1 Reset Char: DT, Inverse
IN>1 UsrRst Char: DT, Default Curve 1/2/3/4
IN>1 tRESET: 0.00…100.00 s
IN>2 Function: Disabled, DT
IN>2 Current Set: 0.02…10.00 In
IN>2 Time Delay: 0.00…200.00 s

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stage 1 of the Earth Fault protection.

The IDG curve is represented by the following equation:

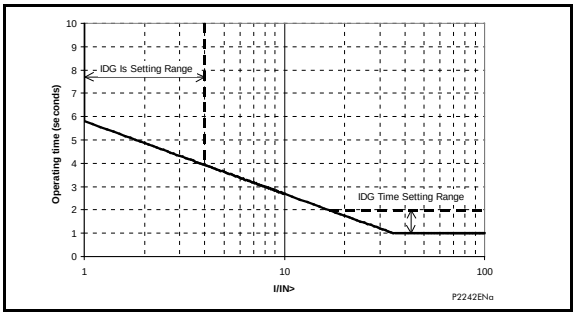
$$t = 5.8 - 1.35 \log_e \left(\frac{I}{IN > Setting} \right) \text{ in seconds}$$

Where:

I = Measured current
IN>Setting = An adjustable setting which defines the start point of the characteristic

Although the start point of the characteristic is defined by the "IN>" setting, the actual relay current threshold is a different setting called "IDG Is". The "IDG Is" setting is set as a multiple of "IN>".

An additional setting "IDG Time" is also used to set the minimum operating time at high levels of fault current.



IDG Characteristic

Rotor EF

Injection Freq: 0.25/0.5/1 Hz
CL I/P Select:
- Current Loop CL1/2/3/4

64R<1 Alarm: Disabled, Enabled
64R<1 Alm Set: 1000…80000 Ω
64R<1 Alm Dly: 0.0…600.0 s
64R<2 Trip: Disabled, Enabled
64R<2 Trip Set: 1000…80000 Ω
64R<2 Trip Dly: 0.0…600.0 s
R Compensation: -1000…1000 Ω

SEF/REF Prot'n

SEF/REF Options:
- SEF
- SEF Cos (PHI)
- SEF Sin (PHI)
- Wattmetric
- Hi Z REF
- Lo Z REF
- Lo Z REF + SEF
- Lo Z REF + Watt

ISEF>1 Function:
- Disabled
- DT

ISEF>1 Directional:
- Non-Directional
- Directional Fwd
- Directional Rev

ISEF>1 Current: 0.0050…0.1000 In A
ISEF>1 Delay: 0.00…200.00 s
ISEF>Func Link: Bit 0 - Block
ISEF>from VTS
ISEF>Char Angle: -95°…95°
ISEF>VNpol Input: Measured/Derived
ISEF>Vnpol Set: 0.5…80.0 V (100/120 V)
2…320.0 V (380/480 V)
WATTMETRIC SEF:
PN> Setting: 0.00…20.00 In W (100/120 V)
0.00…80.00 In W (380/480 V)

Restricted Earth-fault (Low Impedance)

IREF> CT Source: IA-1 IB-1 IC-1/IA-2 IB-2 IC-2
IREF > K1: 0 …20%
IREF > K2: 0 …150%

IREF > Is1: 0.05…1.00 In
IREF > Is2: 0.1…1.50 In

(High Impedance)

IREF > Is1: 0.05…1.00 In

Residual O/V NVD

VN>1 Status: Disabled, Enabled
VN>1 Input: Derived (P342-8)
VN> 1 Function:
DT
IDMT
Default Curve 1/2/3/4
VN> 1 Voltage Set:
1…80 V (100/120 V) (P342-8)
4…320 V (380/480 V) (P342-6)
VN> 1 Time Delay: 0.00…100.00 s
VN>1 TMS: 0.5…100.0
VN> 1 tRESET: 0.00…100.00
VN>2 as VN>1 (P342-8)
VN>3/4 as VN>1 except (P342-6)
VN>3/4 Input: VN1
VN>5/6 as VN>1 except
VN>5/6 Input: VN2 (P344/5)

100% Stator Earth Fault (3rd Harmonic)

100% St EF Status: Disabled, VN3H< Enabled, VN3H> Enabled
100% St EF VN3H<: 0.3…20.0V
0.1…20.0V (100/120 V)
0.4…80.0V (280/440V)
VN3H< Delay: 0.00…100.00s
V < Inhibit Set:
30…120 V (100/120 V)
120…480 V (380/440 V)
P < Inhibit: Disabled, Enabled
P < Inhibit Set:
4…200.0 In W (100/120 V)
16…800.In W (380/480 V)
Q < Inhibit: Disabled, Enabled
Q < Inhibit: Set:
4…200.0 In W (100/120 V)
16…800 In W (380/480 V)
S < Inhibit: Disabled, Enabled
S < Inhibit Set:
4…200.0 In W (100/120 V)
100% St EF VN3H>:
0.1…20.0 V (100/120 V)
0.4…80.0 V (380/480 V)
VN3H> Delay: 0.00…100.00 s

100% Stator Earth Fault (Low Frequency Injection)

64S LF Injection: Disabled, Enabled
64S R Factor: 0.01…200
64S R<1 Alarm: Disabled, Enabled
64S R<1 Alm Set: 10…700 Ω
64S R<1 Alm Delay: 0.00…100.0 s
64S R<2 Trip: Disabled, Enabled
64S R<2 Trip Set: 10…700 Ω
64S R<2 Trip Dly: 0.00…100.0 s
64S Angle Comp: -60°…60°
64S Series R: 0…700 Ω
64S Series X: 0…700 Ω
64S Parallel G: 0.00…0.1 S
64S Overcurrent: Disabled, Enabled
64S I>1 TripSet: 0.02…1.5A
64S I>1 TripDly: 0.00…100.0 s
64S Supervision: Disabled, Enabled
64S V<1 Set: 0.3…25 V
64S I<1 Set: 0.005…0.04A
64S Supern'n Dly: 0.00…100.0 s

Volts/Hz

V/Hz Alarm Status: Disabled, Enabled
V/Hz Alarm Set:
1.50…3.500 V/Hz (100/120 V)
6…14.00 V/Hz (380/480V)
V/Hz Alarm Delay: 0.00…100.0 s
V/Hz>1 Status: Disabled/Enabled
V/Hz Trip Func:
DT
IDMT
Default Curve 1/2/3/4
V/Hz> 1 Trip Set:
1.500…3.500 V/Hz (100/120 V)
6…14.00 V/Hz (380/480 V)
V/Hz> 1Trip TMS: 0.01…12.00
V/Hz> 1 Trip Delay: 0.00…600.0 s
V/Hz>1 Reset Char:
DT
Default Curve 1/2/3/4
V/Hz> 1 tReset: 0.00…600.0 s
V/Hz>2 Status: Disabled, Enabled
V/Hz>2 Trip Set:
1.500…3.500 V/Hz (100/120 V)
6…14.00 V/Hz (380/480V)
V/Hz>2 Trip Delay: .0.00…600.0 s
V/Hz>3/4 as V/Hz>2

The inverse time characteristic has the following formula:

$$t = \frac{TMS}{(M - 1)^2}$$

Where:

$$M = \frac{V/f}{(\ V/f \text{ Trip Setting}\ )}$$

V = Measured voltage
F = Measured frequency

TD

Note: The IDMT characteristic has been changed in the 31 version software. The new characteristic is compatible with the old one and allows the option of future expansion of the number of characteristics with different exponents of (M-1).

Inverse time characteristic in software version 30 and lower is as shown below:

$$t = 0.8 + \frac{0.18 * TMS}{(M - 1)^2}$$

DF/DT

Operating Mode: Fixed Window/Rolling Window
df/dt Avg Cycles: 2…12
df/dt Iterations: 1…4
df/dt>1 Status: Disabled, Enabled
df/dt>1 Setting: 0.10…10.00 Hz/S
df/dt>1 Dir'n: Negative/Positive/Both
df/dt>1 Time: 0.00…100.00 s
df/dt>1 f L/H: Disabled, Enabled
df/dt>1 f Low: 45.00…65.00 Hz
df/dt>1 f High: 45.00…65.00 Hz
df/dt>2/3/4 Status: Disabled, Enabled
df/dt>2/3/4 Setting: 0.10…10.00Hz/S
df/dt>2/3/4 Dir'n: Negative/Positive/Both
df/dt>2/3/4 Time: 0.00…100.00 s

Dead Machine

DM CT Source: IA-1 IB-1 IC-1/IA-2 IB-2 IC-2
Dead Mach Status: Disabled, Enabled
Dead Mach I>: 0.08…4.00 In A
Dead Mach V <:
  10…120 V (100/120 V)
  40…480 V (380/480 V)
Dead Mach tPU: 0.0…10.0 s
Dead Mach tDO: 0.0…10.0 s

Voltage Protection

Undervoltage

V< Measur't Mode:
  Phase-Phase
  Phase-Neutral
V< Operate Mode:
  Any Phase
  Three Phase
V< 1 Function:
  Disabled
  DT
  IDMT
  Default Curve 1/2/3/4
V<1 Voltage Set:
  10…120 V (100/120 V)
  40…480 V (380/480 V)
V<1 Time Delay: 0.00…100.00 s
V<1 TMS: 0.05…100.0
V<1 Poledead Inh: Disabled, Enabled
V<2 Function:
  Disabled
  DT
V<2 Status: Disabled, Enabled
V<2 Voltage Set:
  10…120 V (100/120 V)
  40…480 V (380/480 V)
V<2 Time Delay: 0.00…100.00 s
V<2 Poledead Inh: Disabled, Enabled
V<3 as V<2

The inverse characteristic is given by the following formula:

$$t = \frac{K}{(1 - M)}$$

Where:

K = Time multiplier setting
t = Operating time in seconds
M = Applied input voltage/relay setting voltage

Overvoltage

V> Measur't Mode:
  Phase-Phase
  Phase-Neutral
V> Operate Mode:
  Any Phase
  Three Phase
V> 1 Function:
  Disabled
  DT
  IDMT
  Default Curve 1/2/3/4
V>1 Voltage Set:
  60…185 V (100/120 V)
  240…740 V (380/480 V)
V>1 Time Delay: 0.00…100.00 s
V>1 TMS: 0.05…100.0
V>2 Status: Disabled, Enabled
V>2 Voltage Set:
  60…185 V (100/120 V)
  240…740 V (380/480 V)
V>2 Time Delay: 0.00…100.00 s

The inverse characteristic is given by the following formula:

$$t = \frac{K}{(M - 1)}$$

Where:

K = Time multiplier setting
t = Operating time in seconds
M = Applied input voltage/relay setting voltage

NPS Overvoltage

V2>1 status: Disabled, Enabled
V2>1 Voltage Set:
  1…150 V (100/120 V)
  4…600 V (380/480 V)
V2>1 Time Delay: 0.00…100.00 s

Peak/RMS Overvoltage (P348)

V> Measur't Mode:
  Phase-Phase
  Phase-Neutral
V> Operate Mode:
  Any Phase
  Three Phase
OVERVOLTAGE PEAK: Sub Heading
V>1 Status: Disabled, Enabled
V>1 Voltage Set:
  10…185 V (100/120 V)
V>1 Time Delay: 0.00…100.00 s
V>1 tReset: 0.00…100.00 s
V>1 SV Iterations: 1…10
V>2 as V>1
OVERVOLTAGE RMS: Sub Heading
V>3 Function:
  Disabled
  DT
  IDMT
  Default Curve 1/2/3/4
V>3 Voltage Set:
  10…185 V (100/120 V)
V>3 Time Delay: 0.00…100.00 s
V>3 TMS: 0.05…100.0
V>4 as V>3
The inverse characteristic is given by the following formula:

$$t = \frac{K}{(M - 1)}$$

Where:

K = Time multiplier setting
t = Operating time in seconds
M = Applied input voltage/relay setting voltage

Frequency Protection Underfrequency

F<1 Status: Disabled/Enabled
F<1 Setting: 45.00…65.00 Hz
F<1 Time Delay: 0.1…20000.0s
F<2/3/4 as F<1
F< Function Link:
  Bit 0 - Enable Block F<1 during poledead
  Bit 1 - Enable Block F<2 during poledead
  Bit 2 - Enable Block F<3 during poledead
  Bit 3 - Enable Block F<4 during poledead

Overfrequency

F>1 Status: Disabled, Enabled
F>1 Setting: 45.00…68.00 Hz

F>1 Time Delay: 0.1…100.0 s
F>2 as F>1

Overfrequency (P348)

F>1 Status: Disabled, Enabled
F>1 Setting: 0.1…70.0 Hz
F>1 Time Delay: 0.1…100.0 s
F>2/3/4 as F>1

Generator Turbine Abnormal Frequency

Turbine F Status: Disabled, Enabled
Band 1 Status: Disabled, Enabled
Band 1 Freq Low: 20.00…70.00 Hz
Band 1 Freq High: 20.00…70.00 Hz
Band 1 Duration: 0.00…3600000.00 s
Band 1 Dead Time: 0.00…200.00 s
Band 2/3/4/5/6 as Band 1

RTD Protection

Select RTD:
  Bit 0 - Select RTD 1
  Bit 1 - Select RTD 2
  Bit 2 - Select RTD 3
  Bit 3 - Select RTD 4
  Bit 4 - Select RTD 5
  Bit 5 - Select RTD 6
  Bit 6 - Select RTD 7
  Bit 7 - Select RTD 8
  Bit 8 - Select RTD 9
  Bit 9 - Select RTD 10
Binary function link string, selecting which RTDs (1 - 10) are enabled.
RTD 1 Alarm Set: 0°C…200°C
RTD 1 Alarm Dly: 0 s…100 s
RTD 1 Trip Set: 0°C…200°C
RTD 1 Trip Dly: 0 s…100 s
RTD2/3/4/5/6/7/8/9/10 as RTD1

CB Fail

CB Fail 1 Status: Disabled, Enabled
CB Fail 1 Timer: 0.00…10.00 s
CB Fail 2 Status: Disabled, Enabled
CB Fail 2 Timer: 0.00…10.00 s
CBF Non I Reset: I< Only, CB Open & I<, Prot Reset & I<
CBF Ext Reset: I< Only, CB Open & I <, Prot Reset & I<
I< Current Set: 0.02…3.200 In
IN< Current Set: 0.02…3.200 In
ISEF< Current: 0.0010…0.8000 In
Remove I> Start: Disabled, Enabled
Remove IN< Start: Disabled, Enabled
I< CT Source: IA-1, IB-1, IC-1/IA-2, IB-2, IC-2

TD

Pole Slipping

PSlip Function: Disabled, Enabled
Pole Slip Mode:
  Motoring
  Generating
  Both
PSlip Za Forward:
  0.5…350.0/InΩ (100/120 V)
  2.0…1400.0/InΩ (380/480 V)
PSlip Zb Reverse:
  0.5…350.0/InΩ (100/120 V)
  2.0…1400/InΩ (380/480 V)
Lens Angle: 90°…150°
PSlip Timer T1: 0.00…1.00 s
PSlip Timer T2: 0.00…1.00 s
Blinder Angle: 20°…90°
PSlip Zc:
  0.5…350.0/InΩ (100/120 V)
  2.0…1400.0/InΩ (380/480 V)
Zone 1 Slip Count: 1…20
Zone 2 Slip Count: 1…20
PSlip Reset Time: 0.00…100.0 s

Supervisory Functions

Voltage Transformer Supervison

VTS Status: Blocking/Indication
VTS Reset Mode: Manual/Auto
VTS Time Delay: 1.0…10.0 s
VTS I> Inhibit: 0.08 In…32.0 In
VTS I2> Inhibit: 0.05 In…0.50 In
Negative phase sequence voltage (V2):
  10 V (100/120 V)
  40 V (380/480 V)
Phase overvoltage:
  Pick-up 30 V,
  Drop-off 10 V (100/120 V)
  Pick-up 120 V,
  Drop-off 40 V (380/480 V)
Superimposed Current: 0.1 In

Voltage Transformer Supervison (P348)

VTS Status: Blocking/Indication
VTS Time Delay: 1.0…10.0 s
VTS V Diff Set:
  1…80 V (100/120 V)

Current Transformer Supervision

CTS1 Status: Disabled, Enabled
CTS1 VN Input: Measured/Derived
CTS1 VN< Inhibit:
  0.5…22 V (100/120 V)
  2…88 V (380/480 V)
CTS1 IN> Set: 0.08…4 In
CTS1 Time Delay: 0…10 s
CTS2 as CTS1

DIFF Current Transformer Supervision

DIFF CTS: Disabled, Enabled
Diff CTS Mode: Restrain/Indication
CTS Time Delay: 0.0 to 10.0 s
CTS I1: 5 to 100% in 1% steps
CTS I2/I1>1: 5 to 100%
CTS I2/I1>2: 5 to 100%

Current Transformer Supervision (P348)

CTS2 Status: Disabled, Enabled
CTS2 IN> Set: 0.08…4 In
CTS2 Time Delay: 0…10 s

Through fault

Through Fault: Disabled, Enabled
Monitored Input: HV / LV
TF I> Trigger: 0.08 to 16.00 In
TF I2t> Alarm: 0 to 500 000 A2 s

System Checks

Voltage Monitors

Live/Dead Voltage:
  1.0…132.0 V (100/110 V)
  4…528 V (380/440 V)
Gen Undervoltage:
  1.0…132.0 V (100/110 V)
  4…528 V (380/440 V)
Gen Overvoltage:
  1.0…185.0 V (100/110V)
  4…740 V (380/440 V)
CS Undervoltage:
  10.0…132.0 V (100/110 V)
  4…528 V (380/440 V)
CS Overvoltage:
  60.0…185.0 V (100/110 V)
  240…740 V (380/440 V)
CS Diff Voltage:
  1.0…132.0 V (100/110 V)
  4…528 V (380/440 V)
CS Voltage Block:
  None
  Undervoltage
  Overvoltage
  Differential
  UV & OV
  UV & DiffV
  OV & DiffV
  UV, OV & DiffV
Gen Under Freq: 45.00...65.00 Hz
Gen Over Freq: 45.00...65.00 Hz

Check Sync

CS1 Status: Disabled, Enabled
CS1 Phase Angle: 5…175.00°
CS1 Slip Control:
  None
  Timer

Frequency
Both
CS1 Slip Freq.: 0.01…1.00 Hz
CS1 Slip Timer: 0.00…99.00 s
CS2 Status: Disabled, Enabled
CS2 Phase Angle: 5…90.00°
CS2 Slip Control:
None
Timer
Frequency

Timer + Freq
Freq + CB Comp
CS2 Slip Freq.: 0.01…1.00 Hz
CS2 Slip Timer: 0.00…99.00 s

System Split

SS Status: Disabled, Enabled
SS Phase Angle: 90…175.00°
SS Under V Block: Disabled, Enabled
SS Undervoltage:
10.0…132.0 V (100/110 V)
40…528 V (380/440 V)
SS Timer: 0.00…99.00 s
CB Close Time: 0.000…0.500 s

Plant Supervision

CB State Monitoring Control and Condition Monitoring

Broken I^: 1…2.0
I^ Maintenance:
Alarm disabled
Alarm enabled
I^ Maintenance: 1In^…25000 In^
I^ Lockout:
Alarm disabled
Alarm enabled
I^ Lockout: 1…25000
No CB Ops. Maint:
Alarm disabled
Alarm enabled
No CB Ops: Maint: 1…10000
No CB Ops Lock:
Alarm disabled
Alarm enabled
No CB Ops Lock: 1…10000
CB Time Maint:
Alarm disabled
Alarm enabled
CB Time Maint: 0.005…0.500 s
CB Time Lockout:
Alarm disabled
Alarm enabled
CB Time Lockout: 0.005…0.500 s
Fault Freq Lock:
Alarm disabled
Alarm enabled
Fault Freq Count: 1…9999
Fault Freq Time: 0…9999 s

Input Labels

Opto Input 1…32: Input L1…Input L32

User defined text string to describe the function of the particular opto input.

Output Labels

Relay 1…32: Output R1…Output R32

User defined text string to describe the function of the particular relay output contact.

RTD Labels

RTD 1-10: RTD1…RTD10

User defined text string to describe the function of the particular RTD.

Current Loop Input

CLIO1 Input 1: Disabled, Enabled
CLI1 Input Type:
0 – 1 mA
0 – 10 mA
0 – 20 mA
4 – 20 mA
CLI1 Input Label: 16 characters (CLIO input 1)
CLI1 Minimum: -9999…+9999
CLI1 Maximum: -9999…+9999
CLI1 Alarm: Disabled, Enabled
CLI1 Alarm Fn: Over/Under
CLI1 Alarm Set: CLI1 min…CLI1 max
CLI1 Alarm Delay: 0.0…100.0 s
CLI1 Trip: Disabled, Enabled
CLI1 Trip Fn: Over/Under
CLI1 Trip Set: CLI1 min…CLI1 max
CLI1 Trip Delay: 0.0…100.0 s
CLI1 I< Alarm (4…20 mA input only):
Disabled/Enabled
CLI1 I< Alm Set (4…20 mA input only):
0.0…4.0mA
CLI2/3/4 as CLI1

Current Loop Output

CLO1 Output 1: Disabled, Enabled
CLO1 Output Type:
0 – 1 mA
0 – 10 mA
0 – 20 mA
4 – 20 mA
CLO1 Set Values: Primary/Secondary
CLO1 Parameter: As shown below*
CLO1 Min: Range, step size and unit corresponds to the selected parameter
CLO1 Max: Same as CLO1 Min
CLO2/3/4 as CLO1
Current Loop Output Parameters P342-6 except where specified
Current Magnitude:
IA Magnitude
IB Magnitude
IC Magnitude

TD

IN Measured Mag (P342)
IN-1 Measured Mag (P343/4/5)
IN-2 Measured Mag (P343/4/5)
0.00…16.0A…
I Sen1 Mag: 0.00… 16.0A
Phase Sequence Components:
I1 Magnitude
I2 Magnitude
I0 Magnitude:
0.00…16.0A
Phase Currents:
IA RMS*
IB RMS*
IC RMS*
0.00…16.0A
P-P Voltage Magnitude:
VAB Magnitude
VBC Magnitude
VCA Magnitude
0.0…200.0 V
P-N Voltage Magnitude:
VAN Magnitude
VBN Magnitude
VCN Magnitude
0.0…200.0 V
Neutral Voltage Magnitude:
VN1 Measured Mag
VN Derived Mag
VN2 Measured Mag (P344/5)
0.0…200.0V
VN 3rd Harmonic: 0.0…200.0 V (P343/4/5)
Phase Sequence Voltage Components:
V1 Magnitude
V2 Magnitude
V0 Magnitude
0.0…200.0 V
RMS Phase Voltages:
VAN RMS*
VBN RMS*
VCN RMS*
0.0…200.0 V
Frequency: 0.00…70.0 Hz
3 Phase Watts*: -6000 W…6000 W
3 Phase Vars*: -6000 Var…6000 Var
3 Phase VA*: 0…6000 VA
3Ph Power Factor*: -1…1
Single Phase Active Power:
A Phase Watts*:
B Phase Watts*:
C Phase Watts*:
-2000W…2000 W
Single Phase Reactive Power:
A Phase Vars*:
B Phase Vars*:
C Phase Vars*
-2000Var…2000 Var
Single Phase Apparent Power:
A Phase VA*:
B Phase VA*:
C Phase VA*
0…2000 VA
Single Phase Power Factor:
Aph Power Factor*
BPh Power Factor*
CPh Power Factor*
-1…1
3 Phase Current Demands:
IA Fixed/Roll/Peak Demand*
IB Fixed/Roll/Peak Demand*
IC Fixed/Roll/Peak Demand*
0.00…16.0A
3ph Active Power Demands:
3Ph W Fix/Roll/Peak Demand*
-6000 W…6000 W
3ph Reactive Power Demands:
3Ph Vars Fix/Roll/Peak Dem*
-6000 Var…6000 Var
NPS Thermal: 0.00…200.0%
Thermal Overload: 0.00…200.0%
RTD 1-10*: -40°C…300.0°C
CL Input 1-4: -9999…9999.0
Volts/Hz: 0…20 V/Hz
df/dt: -10.00…10.00Hz
Check Synch Voltages
C/S Voltage Mag
C/S Bus Gen-Mag
0.0…200.0 V
Slip frequency: 0…70 V/Hz
ZA Mag*: 0.0…750.0
Sen Watts*: -750…750W
Sen VArs*: -750…750W
Sen Power Factor*: -1…1
I Sen2 Mag: 0.00… 16.0A
Current Loop Output Parameters P348
Frequency: 0.00…70.0 Hz
CL Input 1-4: -9999…9999.0
Phase Currents:
Iφ-1 RMS
Iφ-1 Peak
Iφ-2 RMS
I2 CT2 RMS
IN-2 Derived RMS
Iφ-2 Peak
I2 CT2 Peak
0.00…16.0A
Phase Voltages:
Vφ-1 RMS
VN-1 Derived RMS
Vφ-1 Peak
VN-1 Derived Peak
Vφ-φ-1 RMS
Vφ-φ-1 Peak
Vφ-2 RMS
0.0…200.0 V
Frequency2: 0.00…70.0 Hz
Per phase (φ = A, B, C, φ-φ = AB, BC, CA) voltage measurements

Note 1: Measurements marked with an asterisk, the internal refresh rate is nominally 1 s, others are 0.5 power system cycles or less.

Note 2: The polarity of Watts, Var and power factor is affected by the measurements Mode setting.

Note 3: These settings are for nominal 1A and 100/120 V versions only. For other versions they need to be multiplied accordingly.

Measurements List

All measurements in P342-6 unless specified

Measurements 1

Iφ Magnitude
Iφ Phase Angle
IN Measured Mag
IN Measured Angle
IN Derived Mag
IN Derived Angle
ISen1 Mag
ISen1 Angle
I1 Magnitude
I2 Magnitude
I0 Magnitude
Iφ RMS
Iφ-1 RMS (P348)
Per phase (φ = A, B, C) RMS current measurements
IN -2 Derived
Vφ-φ Magnitude
Vφ-φ Phase Angle
Vφ Magnitude
Vφ Phase Angle
VN/VN1 Measured Mag
VN/VN1 Measured Ang
VN Derived Mag
V1 Magnitude
V2 Magnitude
V0 Magnitude
Vφ RMS
ISen2 Mag (P345)
ISen2 Angle (P345)
Frequency (P342-6/8)
Frequency2 (P348)
I1 Magnitude
I1 Angle
I2 Magnitude
I2 Angle
I0 Magnitude
I0 Angle
V1 Magnitude
V1 Angle
V2 Magnitude
V2 Angle
V0 Magnitude
V0 Angle
VN2 Measured Mag
VN2 Measured Ang
C/S Voltage Mag
C/S Voltage Ang
Gen-Bus Volt
Gen-Bus Angle
Slip Frequency
C/S Frequency
Iφ-1 RMS (P348)
Iφ-1 Peak (P348)
Iφ-2 RMS (P348)
I2 CT2 RMS (P348)
IN-2 Derived RMS (P348)
Iφ-2 Peak (P348)
I2 CT2 Peak (P348)
Vφ-1 RMS (P348)
Vφ-1 Peak (P348)
Vφ-2 RMS (P348)
VN-1 Derived RMS (P348)
Vφ-2 Peak (P348)
VN-1 Derived Peak (P348)
Vφ-φ-1 RMS (P348)
Vφ-φ-1 Peak (P348)
Vφ-2 RMS (P348)
Per phase (φ = A, B, C, φ-φ = AB, BC, CA)

Measurements 2

φ Phase Watts
φ Phase VArs
φ Phase VA
3 Phase Watts
3 Phase VArs
3 Phase VA
NPS Power S2
3Ph Power Factor
φPh Power Factor
3Ph WHours Fwd
3Ph WHours Rev
3Ph VArHours Fwd
3Ph VArHours Rev
3Ph W Fix Demand
3Ph VArs Fix Dem
Iφ Fixed Demand
3Ph W Roll Dem
3Ph VArs Roll Dem
Iφ Roll Demand
3Ph W Peak Dem
3Ph VAr Peak Dem
Iφ Peak Demand
Reset Demand: No/Yes
CT2 NPS Power S2
Per phase (φ = A, B, C)

Measurements 3

Iφ Magnitude (P343-6)
Iφ Phase Angle (P343-6)
Per phase (φ = A-2, B-2, C-2) current measurements
IA Differential (P343-6)
IB Differential (P343-6)
IC Differential (P343-6)
IA Bias (P343-6)
IB Bias (P343-6)
IC Bias (P343-6)

TD

IREF Diff
IREF Bias
VN 3rd harmonic (P343-5)
NPS Thermal
Reset NPS Thermal: No/Yes
RTD1-10
RTD Open Cct
RTD Short Cct
RTD Data Error
Reset RTD1-10: No/Yes
Sen Watts
Sen VArs
Sen Power Factor
Thermal Overload
Reset Thermal O/L: No/Yes
CLIO Input 1/2/3/4
F Band1-6 Time(s)
Reset Freq Band1-6: No/Yes
Reset Freq Bands: No/Yes
df/dt
Volts/Hz
64S Magnitude (P345)
64S I Magnitude (P345)
64S I Angle (P345)
64S R secondary (P345)
64S R primary (P345)
64R CL Input
64R R Fault
IA/IB/IC Diff PU (P343-6)
IA/IB/IC Bias PU (P343-6)
IA/IB/IC Diff 2H (P343-6)
IA/IB/IC Diff 5H (P343-6)
CT2 I1 Mag (P343-6)
CT2 I1 Angle (P343-6)
CT2 I2 Mag (P343-6)
CT2 I2 Angle (P343-6)
CT2 I0 Mag (P343-6)
CT2 I0 Angle (P343-6)
CT1 I2/I1 (P343-6)
CT2 I2/I1 (P343-6)
ZA Mag

Measurements 4

Hot Spot T
Top Oil T
Reset Thermal: No/Yes
Ambient T
TOL Pretrip left
LOL status
Reset LOL
Rate of LOL
LOL Ageing Fact
Lres at Design T
FAA,m
Lres at FAA,m
Counter 1-16

Circuit Breaker Monitoring Statistics

CB Operations
Total Iφ Broken
Cumulative breaker interruption duty on a per phase basis (φ = A, B, C).
CB Operate Time
Reset CB Data: No/Yes

GS

GETTING STARTED

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 GETTING STARTED

1.1 User interfaces and menu structure

The settings and functions of the protection relay are available from the front panel keypad and LCD, and through the front and rear communication ports.

1.2 Introduction to the relay

1.2.1 Front panel

Figure 1 shows the front panel of the relay; the hinged covers at the top and bottom of the front panel are shown open. An optional transparent front cover physically protects the front panel. With the cover in place, access to the user interface is read-only. Removing the cover allows access to the relay settings and does not compromise the protection of the product from the environment.

When editing relay settings, full access to the relay keypad is needed. To remove the front panel:

1. Open the top and bottom covers, then unclip and remove the transparent cover. If the lower cover is secured with a wire seal, remove the seal.
2. Using the side flanges of the transparent cover, pull the bottom edge away from the relay front panel until it is clear of the seal tab.
3. Move the cover vertically down to release the two fixing lugs from their recesses in the front panel.

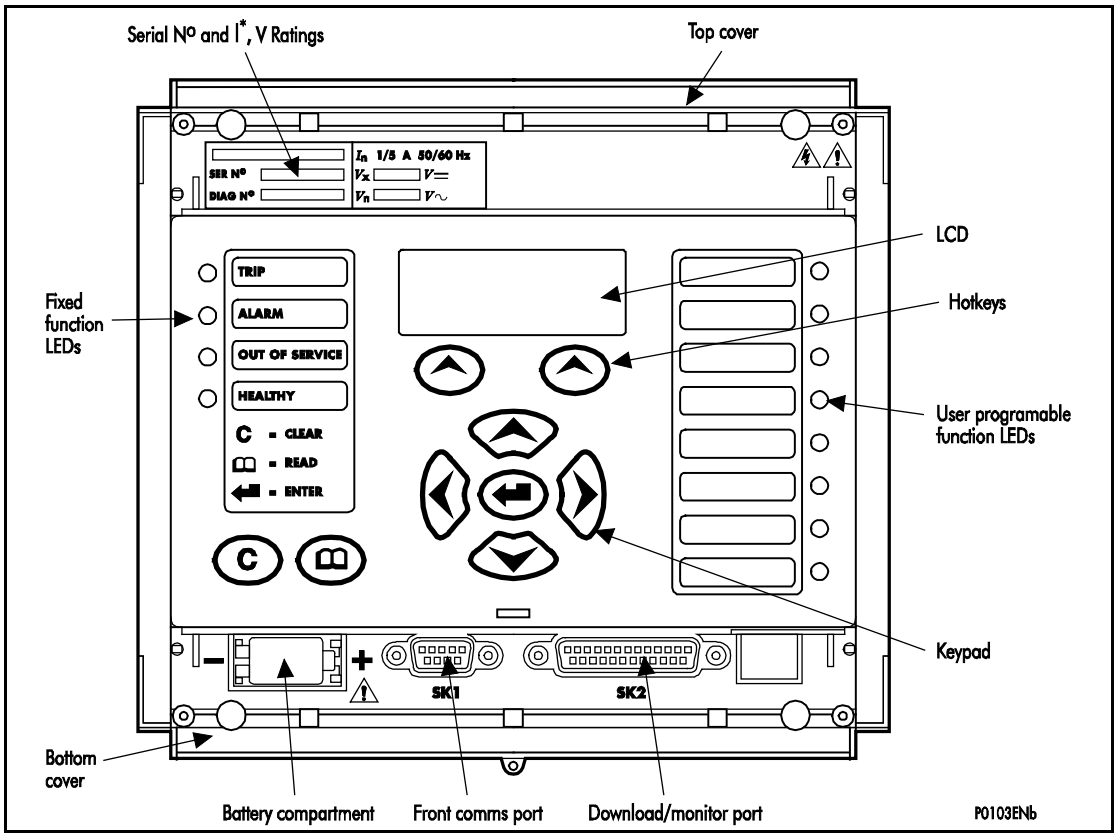


Figure 1: Relay front view (P342)

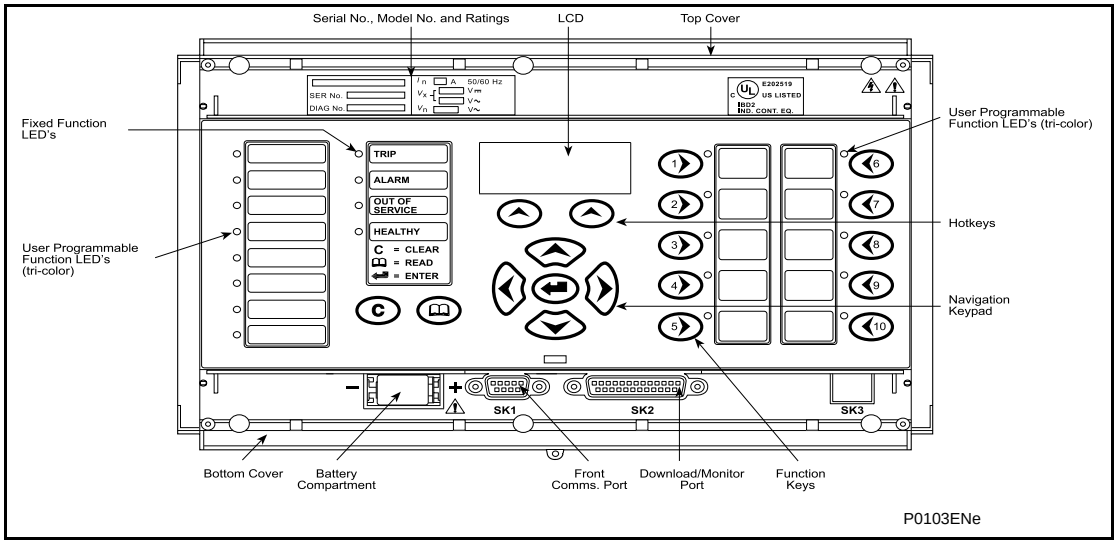


Figure 2: Relay front view (P343/4/5/6/8)

The front panel of the relay includes the following, as indicated in Figures 1 and 2:

- A 16-character by 3-line alphanumeric liquid crystal display (LCD)
- A 19-key (P343/4/5/6/8), 9 key (P342) keypad comprising 4 arrow keys (, , and), an enter key (), a clear key (), a read key (), 2 hot keys () and 10 (-) programmable function keys (P345)
- Function key functionality (P343/4/5/6/8). The relay front panel has control keys with programmable LEDs for local control. Factory default settings associate specific relay functions with these 10 direct-action keys and LEDs, such as **Enable** or **Disable the auto-recloser** function. Using programmable scheme logic, the user can change the default functions of the keys and LEDs to fit specific needs.
- Hotkey functionality:
  - **SCROLL** starts scrolling through the various default displays.
  - **STOP** stops scrolling the default display.
  - **Control** inputs and circuit breaker operation to control setting groups.
- 22 LEDs (P343/4/5/6/8), 12 LEDs (P342); 4 fixed function LEDs, 8 tri-color (P343/4/5/6/8), 8 red (P342) programmable function LEDs on the left hand side of the front panel and 10 tri-color programmable function LEDs on the right hand side associated with the function keys ((P343/4/5/6/8))
- Under the top hinged cover:
  - The relay's serial number.
  - The relay's current and voltage rating information
- Under the bottom hinged cover:
  - Compartment for a 1/2 AA size backup battery used for the real time clock and event, fault, and disturbance records.
  - A 9-pin female D-type front port for a connection of up to 15 m between a PC and the relay using an EIA(RS)232 serial data connection.
  - A 25-pin female D-type parallel port for monitoring internal signals and downloading high-speed local software and language text.

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1.2.1.1 LED indications

Fixed Function

The four fixed function LEDs on the left-hand side of the front panel indicate the following conditions:

- Trip (Red) switches ON when the relay issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the relay registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the relay's protection is unavailable.
- Healthy (Green) is ON when the relay is in correct working order, and should be ON at all times. It goes OFF if the relay's self-tests show there is an error in the relay's hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the relay.

To adjust the LCD contrast, from the **CONFIGURATION** column, select **LCD Contrast**. This is only needed in very hot or cold ambient temperatures.

Programmable LEDs

All the programmable LEDs are tri-color in the P343/4/5/6/8 and can be programmed to indicate RED, YELLOW or GREEN depending on the requirements. All the programmable LEDs are RED in the P342. The 8 programmable LEDs are suitable for programming alarm indications and the default indications and functions are indicated in the table below. The 10 programmable LEDs physically associated with the function keys (P343/4/5/6/8), are used to indicate the status of the associated pushbutton's function and the default indications are shown below:

The default settings are shown in Table 1 and Table 2.

LED number	Default indication	P342 relay
1	Red	Earth Fault Trip -IN>1/2/ISEF>1/IREF>/VN>1/2/3/4/64R R<2 Trip
2	Red	Overcurrent Trip - I>1/2/3/4/V Dep OC Trip
3	Red	Field Failure Trip - Field Fail 1/2 Trip
4	Red	I2> Trip - I2>1/2/3/4/NPS Thermal Trip
5	Red	Voltage Trip - V>2/V<2/V2>1 Trip
6	Red	Frequency Trip - F>2/F<4/Freq Band 1/2/3/4/5/6 Trip
7	Green	Power Trip - Power 1/SPower 1 Trip
8	Red	Any Start
F1	Red	Not used
F2	Yellow	Not used
F3	Yellow	Not used
F4	Red	Inhibit Turbine Abnormal Frequency Protection
F5	Red	Setting Group 2 Enabled
F6	Red	Not used
F7	Red	Reset NPS Thermal State to 0
F8	Red	Reset Thermal Overload State to 0
F9	Yellow	Reset Latched LEDs and Relay Contacts
F10	Yellow	Manual Trigger Disturbance Recorder

Table 1: P342 default mappings for programmable LEDs

LED number	Default indication	P343/4/5/6 relay
1	Red	Earth Fault Trip -IN>1/2/ISEF>1/IREF>/VN>1/2/3/4/5/6/100% ST EF 3H/64S I>1/64S R<2 Trip/64R R<2 Trip
2	Red	Overcurrent Trip - I>1/2/3/4/V Dep OC Trip
3	Red	Field Failure Trip - Field Fail 1/2 Trip
4	Red	I2> Trip - I2>1/2/3/4/NPS Thermal Trip
5	Red	Voltage Trip - V>2/V<2/V2>1 Trip
6	Red	Frequency Trip - F>2/F<4/Freq Band 1/2/3/4/5/6 Trip
7	Green	Power Trip - Power 1/SPower 1 Trip
8	Red	Any Start
F1	Red	Not used
F2	Yellow	Not used
F3	Yellow	Not used
F4	Red	Inhibit Turbine Abnormal Frequency Protection
F5	Red	Setting Group 2 Enabled
F6	Red	Not used
F7	Red	Reset NPS Thermal State to 0
F8	Red	Reset Thermal Overload State to 0
F9	Yellow	Reset Latched LEDs and Relay Contacts
F10	Yellow	Manual Trigger Disturbance Recorder

Table 2: P343/4/5/6 default mappings for programmable LEDs

LED number	Default indication	P348 relay
1	Red	Overcurrent Trip – I>1/2/3/4 Peak Trip, I>5/6/7/8 RMS Trip
2	Red	Overvoltage Trip – V>1/2/3/4 Trip
3	Red	NPS Overcurrent Trip – I2>1/2/3/4 Trip
4	Red	Neutral Voltage Trip – VN>1/2 Trip
5	Red	Overfrequency Trip – F>1/2/3/4 Trip
6	Red	Current Loop Input Trip – CL Input 1/2/3/4 Trip
7	Red	Machine Start and Inhibit F>1/2/3/4 input
8	Red	Any Start
F1	Yellow	Function Key 1
F2	Yellow	Function Key 2
F3	Yellow	Function Key 3
F4	Yellow	Function Key 4
F5	Yellow	Setting Group 2 Enabled
F6	Yellow	Function Key 6
F7	Yellow	Function Key 7
F8	Yellow	Function Key 8
F9	Yellow	Reset Latched LEDs and Relay Contacts
F10	Yellow	Manual Trigger Disturbance Recorder

Table 3: P348 default mappings for programmable LEDs

1.2.2 Relay rear panel

Figure 3 shows the rear panel of the relay. All current and voltage signals, digital logic input signals and output contacts are connected at the rear of the relay. Also connected at the rear is the twisted pair wiring for the rear EIA(RS)485 communication port, the IRIG-B time synchronizing input and the optical fiber rear communication port which are both optional.

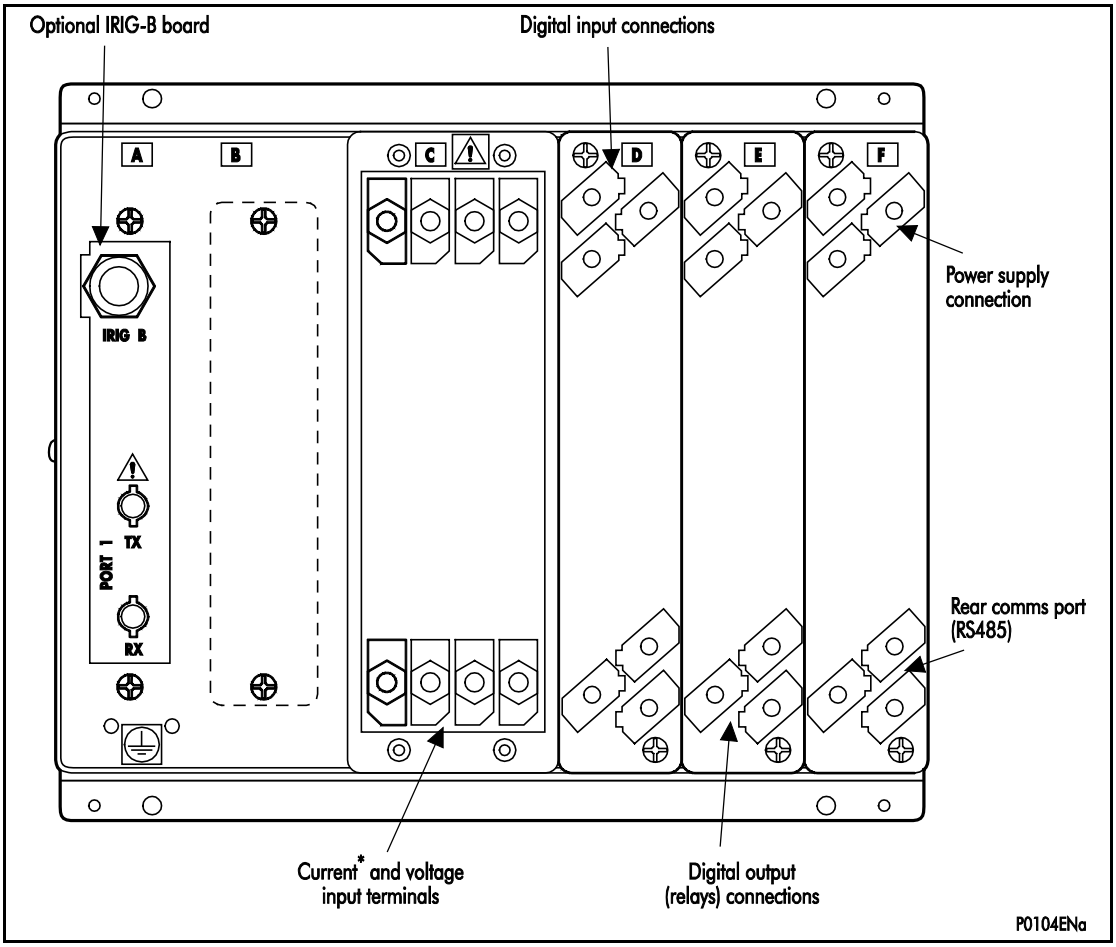


Figure 3: Relay rear view

See the wiring diagrams in the Installation chapter (*P34x/EN IN*) for complete connection details.

1.3 Relay connection and power-up

Before powering-up the relay, confirm that the relay power supply voltage and nominal ac signal magnitudes are appropriate for your application. The relay serial number, and its current, voltage and power rating are under the top hinged cover. The relay is available in the auxiliary voltage versions which are specified in Table 4.

Nominal ranges	Operative dc range	Operative ac range
24 - 48 V dc (P34x)	19 to 65 V	-
48 - 110 V dc (40 - 100 V ac rms) ** (P34x)	37 to 150 V	32 to 110 V
110 - 250 V dc (100 - 240 V ac rms) **	87 to 300 V	80 to 265 V
48 - 250 V dc, (100 - 230 V ac rms) ** (P391)	48 to 300 V	85 to 253 V

Table 4: Auxiliary voltage options

** rated for ac or dc operation

Note: The label does not specify the logic input ratings.

The P34x relay has universal opto isolated logic inputs. These can be programmed for the nominal battery voltage of the circuit where they are used. See Universal opto isolated logic inputs in the Firmware chapter *P34x/EN FD* for more information on logic input specifications.

Note: The opto inputs have a maximum input voltage rating of 300 V dc at any setting.

Once the ratings have been verified for the application, connect external power according to the power requirements specified on the label. See P34x external connection diagrams in the Installation chapter *P34x/EN IN* for complete installation details, ensuring the correct polarities are observed for the dc supply.

1.4 Introduction to the user interfaces and settings options

The relay has the following user interfaces:

- The front panel using the LCD and keypad
- The front port which supports Courier communication
- The rear port which supports one protocol of either Courier, MODBUS, IEC 60870-5-103, DNP3.0 or IEC 61850. The protocol for the rear port must be specified when the relay is ordered
- 2nd rear port (option) which supports Courier communication

	Keypad/ LCD	Courier	MODBUS	IEC 870-5-103	IEC 61850-8-1	DNP3.0
Display & modification of all settings	•	•	•			
Digital I/O signal status	•	•	•	•	•	•
Display/extraction of measurements	•	•	•	•	•	•
Display/extraction of fault records	•	•	•	•		•
Extraction of disturbance records		•	•	•	•	
Programmable scheme logic settings		•				
Reset of fault & alarm records	•	•	•	•	•	•
Clear event & fault records	•	•	•			•
Time synchronization		•	•	•	•	•
Control commands	•	•	•	•	•	•

Table 5: Measurement information and relay settings that can be accessed from the interfaces

1.5 Menu structure

The menu is arranged in a table. Each setting in the menu is known as a cell, and each cell in the menu can be accessed using a row and column address. The settings are arranged so that each column contains related settings, for example all of the disturbance recorder settings are contained within the same column. As shown in Figure 4, the top row of each column contains the heading that describes the settings in that column. You can only move between the columns of the menu at the column heading level. For a complete list of all of the menu settings, see the Settings chapter P34x/EN ST and the Relay Menu Database document P34x/EN MD.

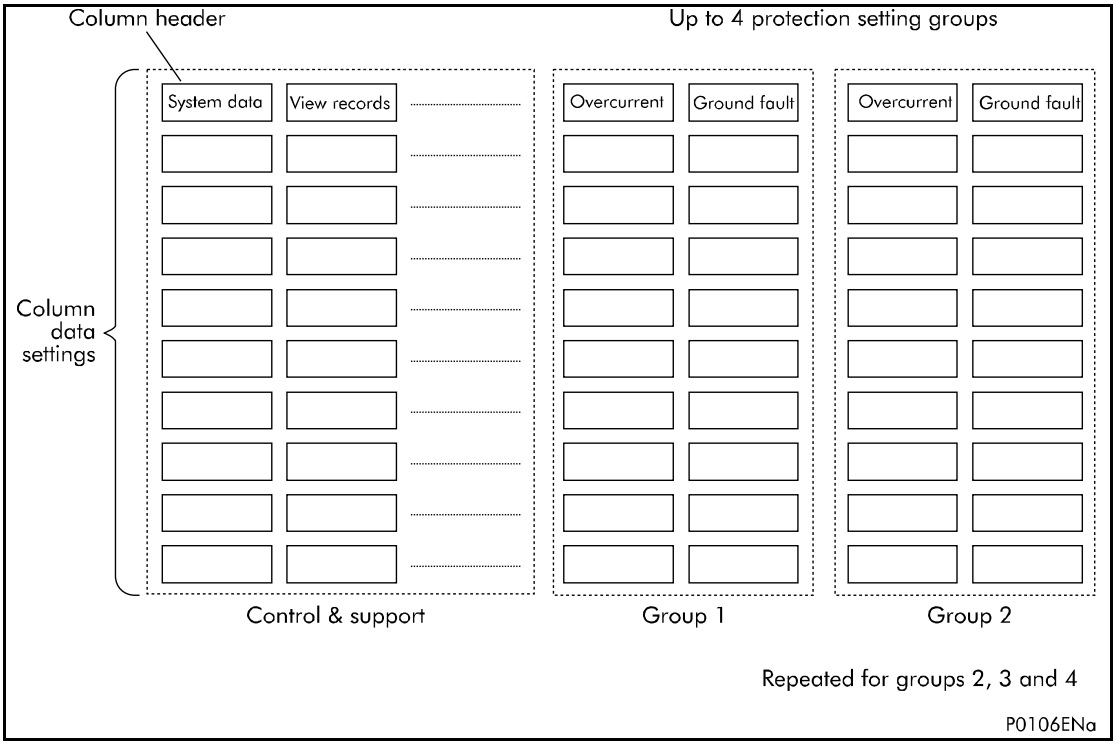


Figure 4: Menu structure

The settings in the menu are in three categories: protection settings, disturbance recorder settings, or control and support (C&S) settings.

New control and support settings are stored and used by the relay immediately after they are entered. New Protection settings or disturbance recorder settings are stored in a temporary 'scratchpad'. Once the new settings have been confirmed, the relay activates all the new settings together. This provides extra security so that several setting changes, made in a group of protection settings, all take effect at the same time.

1.5.1 Protection settings

The protection settings include the following items:

- Protection element settings
- Scheme logic settings

There are four groups of protection settings, with each group containing the same setting cells. One group of protection settings is selected as the active group, and is used by the protection elements.

1.5.2 Disturbance recorder settings

The disturbance recorder settings include the record duration and trigger position, selection of analog and digital signals to record, and the signal sources that trigger the recording.

1.5.3 Control and support settings

The control and support settings include:

- Relay configuration settings
- Open/close circuit breaker (may vary according to relay type/model)
- CT & VT ratio settings
- Reset LEDs
- Active protection setting group
- Password & language settings

- Circuit breaker control & monitoring settings (may vary according to relay type/model)
- Communications settings
- Measurement settings
- Event & fault record settings
- User interface settings
- Commissioning settings

1.6 Relay configuration

The relay is a multi-function device that supports numerous different protection, control and communication features. To simplify the setting of the relay, there is a configuration settings column which can be used to enable or disable many of the functions of the relay. The settings associated with any function that is disabled are not shown in the menu. To disable a function change the relevant cell in the **Configuration** column from **Enabled** to **Disabled**.

The configuration column controls which of the four protection settings groups is selected as active through the **Active settings** cell. A protection setting group can also be disabled in the configuration column, provided it is not the present active group. Similarly, a disabled setting group cannot be set as the active group.

1.7 Front panel user interface (keypad and LCD)

When the keypad is exposed it provides full access to the menu options of the relay, with the information displayed on the LCD.

The ⟨, ⟩, ⌔ and ⌔ keys which are used for menu navigation and setting value changes. These keys have an auto-repeat function if any of them are held continually. This can speed up both setting value changes and menu navigation: the longer the key is held pressed, the faster the rate of change or movement.

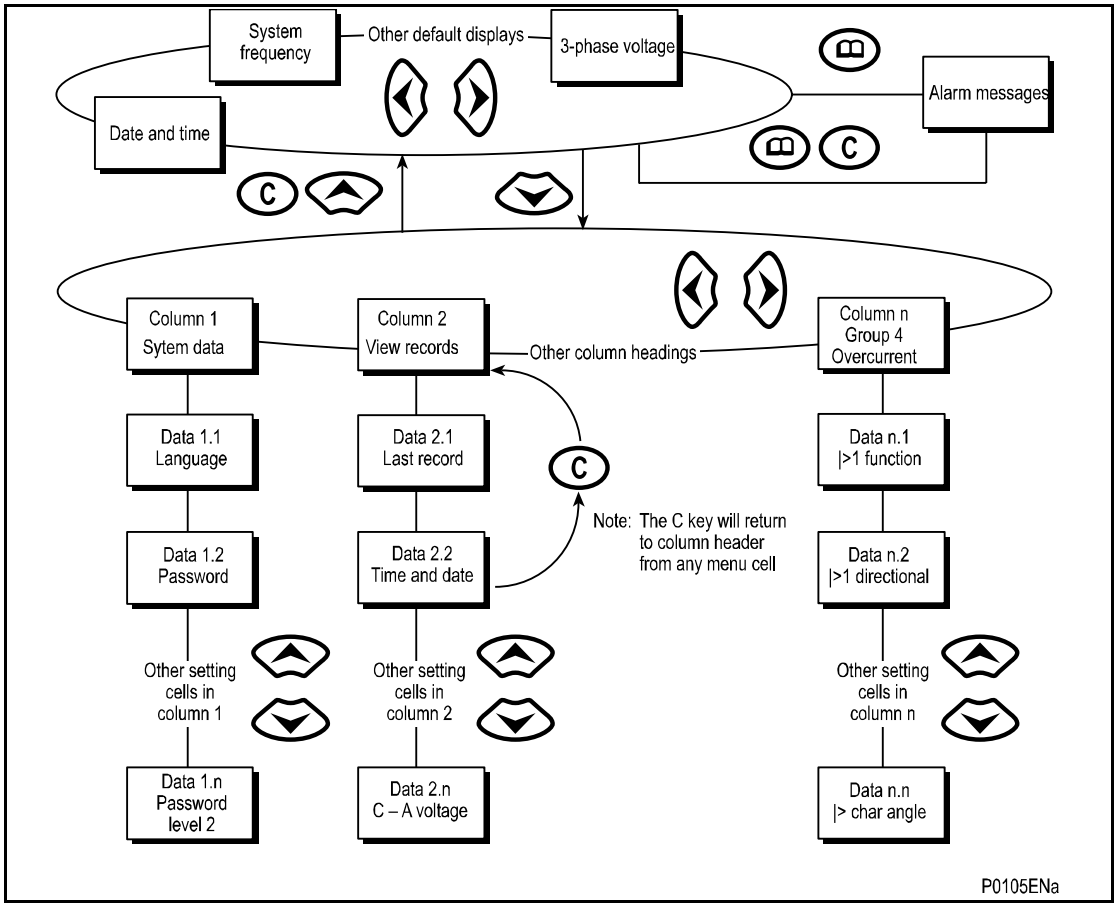


Figure 5: Front panel user interface

1.7.1 Default display and menu time-out

The front panel menu has a default display. To change it, select **Measure't. setup > default display** and the following items can be selected:

- User Banner
- Date and time
- Relay description (user defined)
- Plant reference (user defined)
- System frequency
- 3 phase voltage
- 3 phase and neutral current
- Power
- Access level

From the default display you can view the other default display options using the ◇ and ◇ keys. If there is no keypad activity for 15 minutes, the default display reverts to the previous setting and the LCD backlight switches off. Any setting changes that have not been confirmed are lost and the original setting values are maintained.

Whenever there is an uncleared alarm present in the relay (e.g. fault record, protection alarm, control alarm etc.) the default display will be replaced by:

Alarms/Faults Present

Enter the menu structure of the relay from the default display, even if the display shows the **Alarms/Faults** present message.

1.7.2 Navigating menus and browsing the settings

Use the four arrow keys to browse the menu, following the structure shown in Figure 5.

1. Starting at the default display, press the ◇ key to show the first column heading.
2. Use the ◇ and ◇ keys to select the required column heading.
3. Use the ◇ and ◇ keys to view the setting data in the column.
4. To return to the column header, either hold the ◇ key down or press the clear key Ⓒ once. It is only possible to move across columns at the column heading level.
5. To return to the default display, press the ◇ key or the clear key Ⓒ from any of the column headings. If you use the auto-repeat function of the ◇ key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
6. Press the ◇ key again to go to the default display.

1.7.3 Navigating the hotkey menu

1. To access the hotkey menu from the default display, press the key directly below the **HOTKEY** text on the LCD.
2. Once in the hotkey menu, use the ◇ and ◇ keys to scroll between the available options, then use the hotkeys to control the function currently displayed.

   If neither the ◇ or ◇ keys are pressed within 20 seconds of entering a hotkey sub menu, the relay reverts to the default display.
3. Press the clear key Ⓒ to return to the default menu from any page of the hotkey menu.

The layout of a typical page of the hotkey menu is as follows:

- The top line shows the contents of the previous and next cells for easy menu navigation
- The center line shows the function
- The bottom line shows the options assigned to the direct access keys

The functions available in the hotkey menu are listed below:

1.7.3.1 Setting group selection

To select the setting group, scroll through the available setting groups using **NXT GRP**, or press **SELECT** to select the setting group that is currently displayed.

When you press **SELECT**, the current setting group appears for 2 seconds, then the **NXT GRP** or **SELECT** options appear again.

To exit the sub menu, use the left and right arrow keys. For more information see Changing setting groups in the Operation chapter (*P34x/EN OP*).

1.7.3.2 Control inputs – user assignable functions

The control inputs are user-assignable functions or **USR ASS**.

Use the **CTRL I/P CONFIG** column to configure the number of **USR ASS** shown in the hotkey menu. To **SET/RESET** the chosen inputs, use the **HOTKEY** menu.

For more information see the Control Inputs section in the Operation chapter (*P34x/EN OP*).

1.7.3.3 CB control

The CB control functionality varies from one Px40 relay to another (CB control is included in the P342/3/4/5/6). For a detailed description of the CB control via the hotkey menu refer to the “Circuit breaker control” section of the Operation chapter (*P34x/EN OP*).

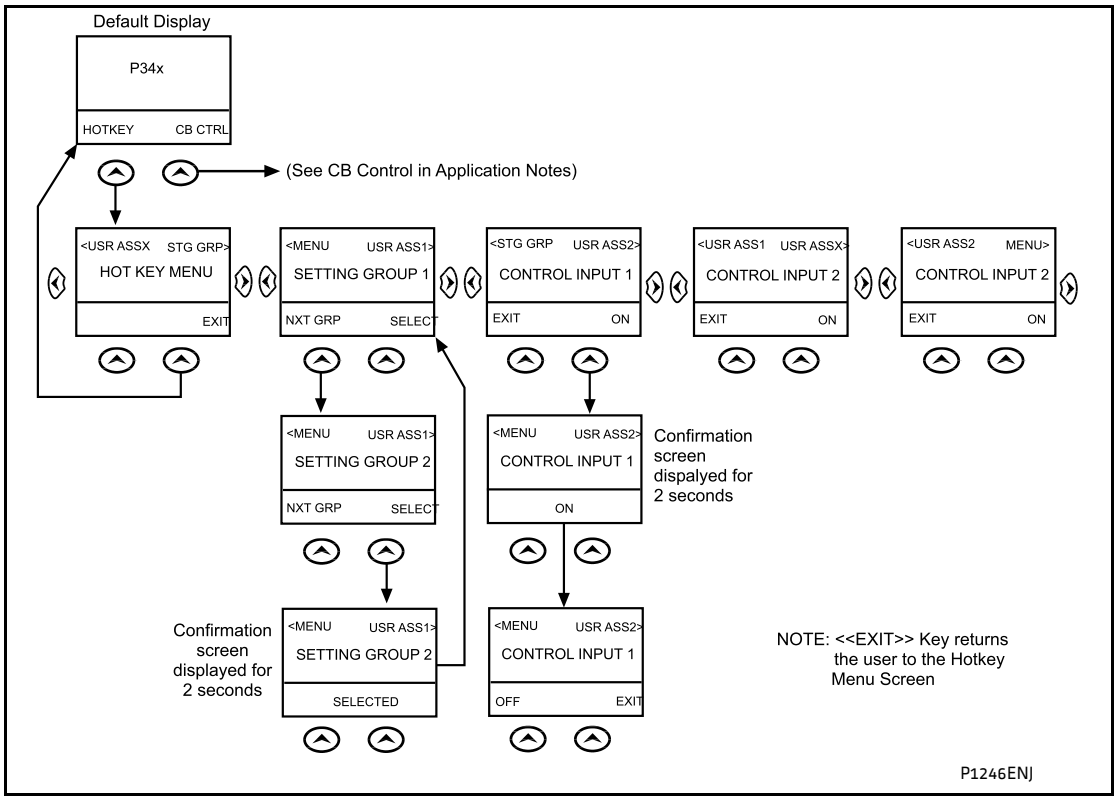
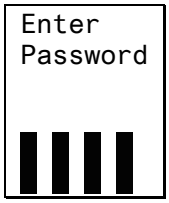


Figure 6: Hotkey menu navigation

1.7.4 Password Entry

Configuring the default display (in addition to modification of other settings) requires level 3 access. You will be prompted for a password before you can make any changes, as follows. The default level 3 password is **AAAA**.

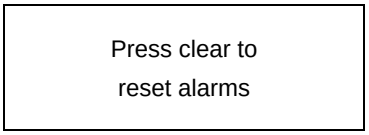


1. A flashing cursor shows which character field of the password can be changed. Press the up or down cursor keys to change each character (tip: pressing the up arrow once will return an upper case "A" as required by the default level 3 password).
2. Use the left and right cursor keys to move between the character fields of the password.
3. Press the **Enter** key to confirm the password. If you enter an incorrect password, an invalid password message is displayed then the display reverts to **Enter password**. Upon entering a valid password a message appears indicating that the password is correct and if so what level of access has been unlocked. If this level is sufficient to edit the selected setting, the display returns to the setting page to allow the edit to continue. If the correct level of password has not been entered, the password prompt page appears again.
4. To escape from this prompt press the Clear key. Alternatively, enter the password using **System data** > **Password**. If the keypad is inactive for 15 minutes, the password protection of the front panel user interface reverts to the default access level.
5. To manually reset the password protection to the default level, select **System data** > **Password**, then press the clear key instead of entering a password.

1.7.5 Reading and clearing of alarm messages and fault records

One or more alarm messages appear on the default display and the yellow alarm LED flashes. The alarm messages can either be self-resetting or latched, in which case they must be cleared manually.

1. To view the alarm messages, press the read key. When all alarms have been viewed but not cleared, the alarm LED change from flashing to constantly ON and the latest fault record appears (if there is one).
2. Scroll through the pages of the latest fault record, using the key. When all pages of the fault record have been viewed, the following prompt appears.



3. To clear all alarm messages, press C. To return to the display showing alarms or faults present, and leave the alarms uncleared, press .
4. Depending on the password configuration settings, you may need to enter a password before the alarm messages can be cleared. See section 1.7.4.
5. When all alarms are cleared, the yellow alarm LED switches OFF; also the red trip LED switches OFF if it was switched ON after a trip.
6. To speed up the procedure, enter the alarm viewer using the key, then press the C key. This goes straight to the fault record display. Press C again to move straight to the alarm reset prompt, then press C again to clear all alarms.

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1.7.6 Setting changes

1. To change the value of a setting, go to the relevant cell in the menu, then press the enter key ↵ to change the cell value. A flashing cursor on the LCD shows the value can be changed. If a password is required to edit the cell value, a password prompt appears ©.
2. To change the setting value, press the ⌄ or ⌃ keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the ‹ and › keys.
3. Press ↵ to confirm the new setting value or the clear key © to discard it. The new setting is automatically discarded if it is not confirmed in 15 seconds.
4. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used by the relay.

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To do this, when all required changes have been entered, return to the column heading level and press the ⌄ key. Before returning to the default display, the following prompt appears.

Update settings?
Enter or clear

5. Press ↵ to accept the new settings or press © to discard the new settings.

Note: If the menu time-out occurs before the setting changes have been confirmed, the setting values are also discarded.

Control and support settings are updated immediately after they are entered, without the **Update settings?** prompt.

1.8 Front communication port user interface

The front communication port is a 9-pin female D-type connector under the bottom hinged cover. It provides EIA(RS)232 serial data communication up to 15 m with a PC, see Figure 7. This port supports the Courier communication protocol only. Courier is the communication language developed by us to allow communication with its range of protection relays. The front port is intended for use with the relay settings program S1 Agile which runs on Windows™ 2000, Vista, XP or Windows 7.

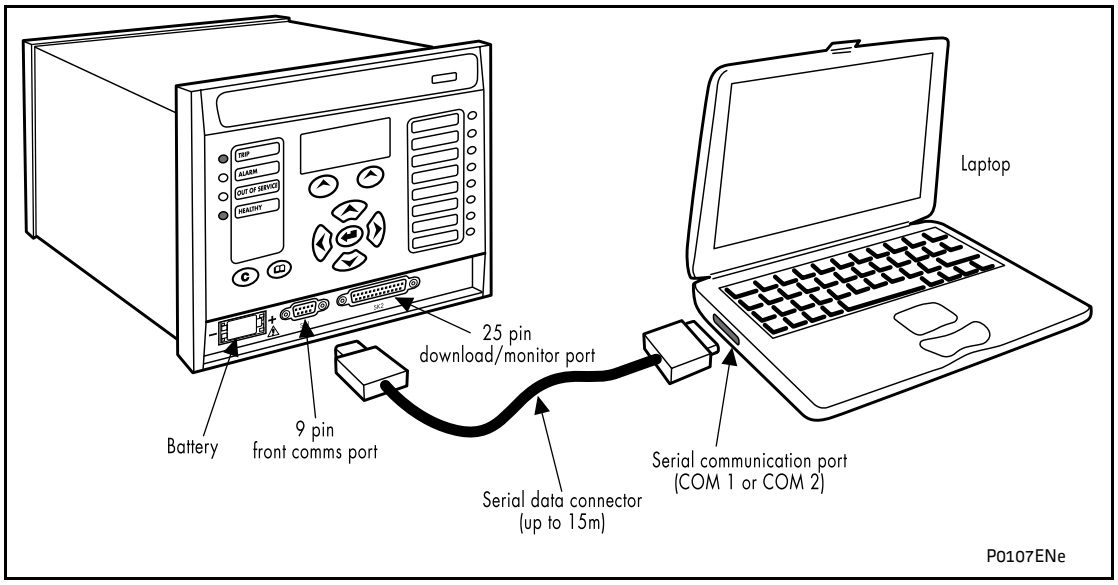


Figure 7: Front port connection

The relay is a Data Communication Equipment (DCE) device with the following pin connections on the 9-pin front port.

Pin number	Description
2	Tx Transmit data
3	Rx Receive data
5	0 V Zero volts common

Table 6: Front port pin designation

None of the other pins are connected in the relay. The relay should be connected to the COM1 or COM2 serial port of a PC. PCs are normally Data Terminal Equipment (DTE) devices which have the following serial port pin connections (if in doubt check your PC manual):

Pin number	25-way	9-way	Description
2	3	2	x Receive data
3	2	3	Tx Transmit data
5	7	5	0 V Zero volts common

Table 7: DTE devices serial port pin designation

For successful data communication, connect the Tx pin on the relay to the Rx pin on the PC, and the Rx pin on the relay to the Tx pin on the PC. Normally a straight-through serial cable is required, connecting pin 2 to pin 2, pin 3 to pin 3, and pin 5 to pin 5.

Note: A common cause of difficulty with serial data communication is connecting Tx to Tx and Rx to Rx. This could happen if a cross-over serial cable is used, connecting pin 2 to pin 3, and pin 3 to pin 2, or if the PC has the same pin configuration as the relay.

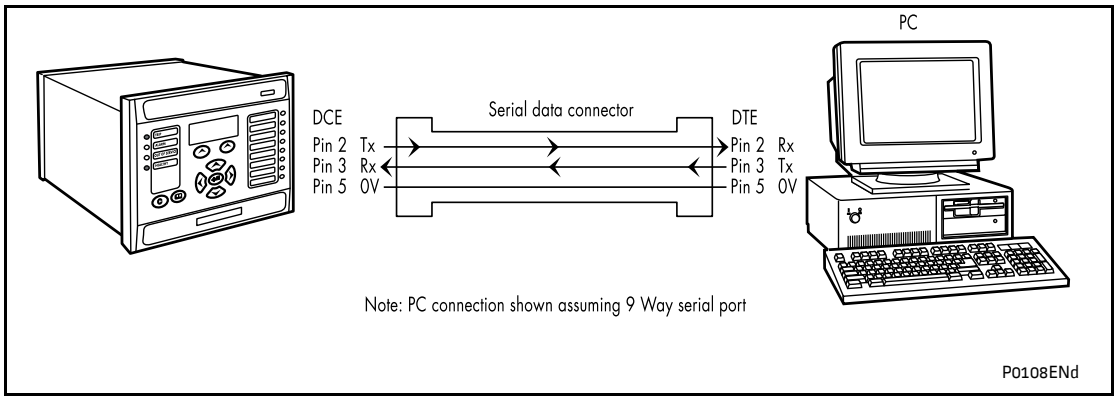


Figure 8: PC - relay signal connection

Once the physical connection from the relay to the PC is made, the PC's communication settings must be set to match those of the relay. The following table shows the relay's communication settings for the front port.

Protocol	Courier
Baud rate	19,200 bits/s
Courier address	1
Message format	11 bit - 1 start bit, 8 data bits, 1 parity bit (even parity), 1 stop bit

Table 8: Relay front port settings

If there is no communication using the front port for 15 minutes, any password access level that has been enabled is cancelled.

GS

1.8.1 Front courier port

The front EIA(RS)232[1] 9 pin port supports the Courier protocol for one-to-one communication. It is designed for use during installation and commissioning or maintenance, and is not suitable for permanent connection. Since this interface is not used to link the relay to a substation communication system, the following features of Courier are not used.

Automatic Extraction of Event Records:

- Courier Status byte does not support the Event flag
- Send Event or Accept Event commands are not implemented

Automatic Extraction of Disturbance Records:

- Courier Status byte does not support the Disturbance flag

Busy Response Layer:

- Courier Status byte does not support the Busy flag, the only response to a request will be the final data

Fixed Address:

- The address of the front courier port is always 1, the Change Device address command is not supported.

Fixed Baud Rate:

- 19200 bps

Note: Although automatic extraction of event and disturbance records is not supported, this data can be manually accessed using the front port.

1.9 S1 Agile relay communications basics

The EIA(RS)232 front communication port is intended for use with the relay settings program S1 Agile. This program runs on Windows™ 2000, XP, Vista or Windows 7 and is the universal IED Support Software used for direct access to all stored data in any IED.

S1 Agile provides full access to:

- Px40, Modulex series, K series, L series relays
- Mx20 measurements units

Connecting to the P34x relay using S1 Agile

This section is intended as a quick start guide to using S1 Agile and assumes you have a copy installed on your PC. See the *S1 Agile program online help* or 'MiCOM P40 Agile Modular and Compact Ranges, Settings Application Software User Guide', P40-M&CR-UG for more detailed information.

1. Make sure the EIA(RS)232 serial cable is properly connected between the port on the front panel of the relay and the PC. See section 1.9.
2. Start S1 Agile and click the **Quick Connect** tab and select **Create a New System**.
3. Check the **Path to System file** is correct, then enter the name of the system in the Name field. If you need to add a brief description of the system, use the **Comment** field.
4. Click **OK**.
5. Select the device type.
6. Select the communications port.
7. Once connected, select the language for the settings file, the device name, then click **Finish**. The configuration is updated.

[1] This port is actually compliant to EIA(RS)574; the 9-pin version of EIA(RS)232, see www.tiaonline.org.

8. In the **Agile Explorer** window, select **Device > Supervise Device…** to control the relay directly.

1.9.1 Off-line use of S1 Agile

S1 Agile can also be used as an off-line tool to prepare settings, without access to the relay.

1. If creating a new system, in the Agile Explorer, select **create new** system. Then right-click the new system and select **New substation**.
2. Right-click the new substation and select **New voltage level**.
3. Then right-click the new voltage level and select **New bay**.
4. Then right-click the new bay and select **New device**.
   You can add a device at any level, whether it is a system, substation, voltage or bay.
5. Select a device type from the list, then enter the relay type, such as P645. Click **Next**.
6. Enter the full model number and click **Next**.
7. Select the **Language** and **Model**, then click **Next**.
8. Enter a unique device name, then click **Finish**.
9. Right-click the **Settings** folder and select **New File**. A default file 000 is added.
10. Right-click file **000** and select click **Open**. You can then edit the settings. See the *S1 Agile program online help* for more information.

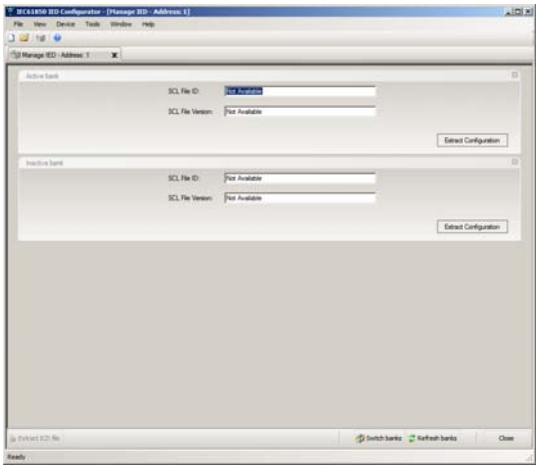
2 CONFIGURING THE ETHERNET INTERFACE

The way in which you configure the Ethernet interface depends on the particular type of interface you have. If you have a DNP3.0 interface, use the DNP setting file to configure the Ethernet interface. Otherwise you should use the IED configurator tool in MiCOM S1 Agile.

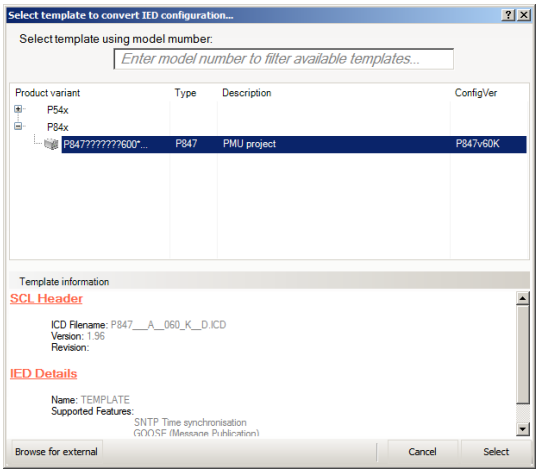
Note: Further information is available in the Communications chapter

2.1 Configuring the Ethernet Interface for IEC 61850

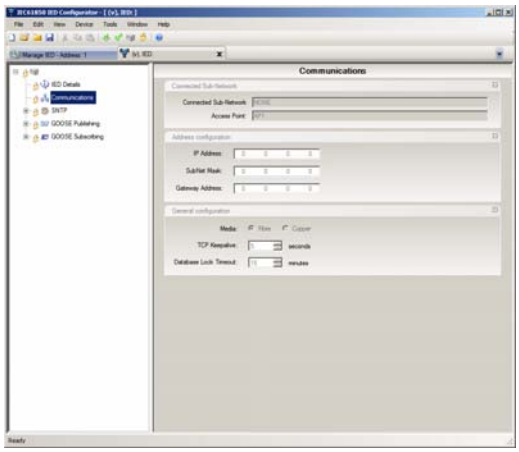
1. Open MiCOM S1 Agile:
2. Select **Tools > IEC61850 IED Configurator**
3. Select **Device > Manage IED**
4. Select **Px40**
5. Enter the address of the IED you want to manage (this will always be '1' if you are connected via the front port)
6. Click **Next.** The following screen appears



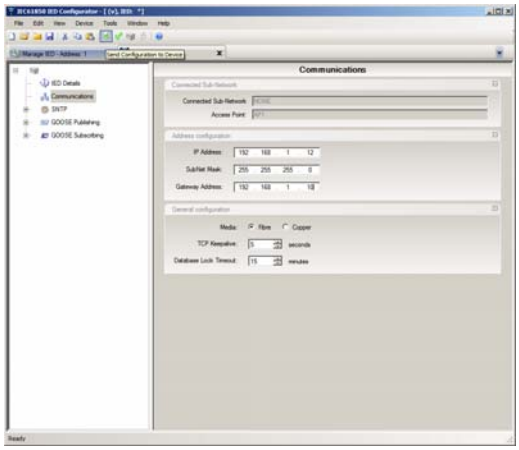
7. Select **Extract Configuration, Active Bank**

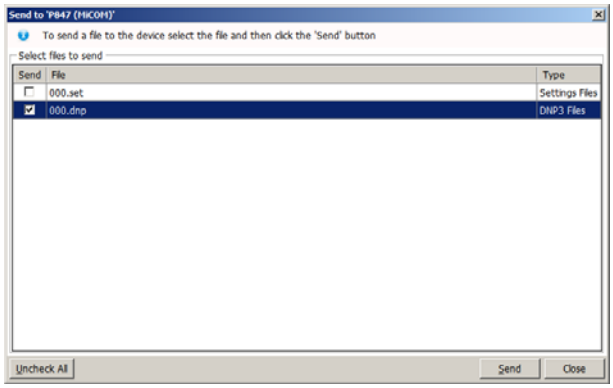


8. Select the model. The IP address data is then revealed:



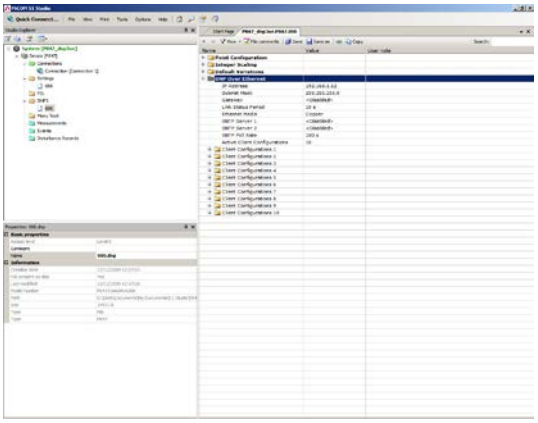
9. To change the address values, select View > Enter Manual Editing Mode
10. Enter the required IP configuration and select the green download button:



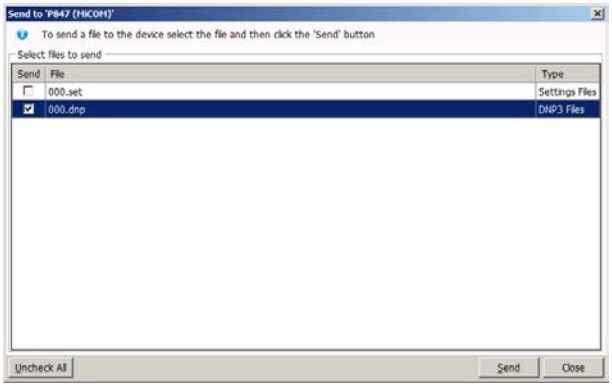


2.2 Configuring the Ethernet Interface for DNP3.0

1. Open MiCOM S1 Agile:
2. Select the device DNP3.0 file (which has been created by the DNP3.0 configurator)



3. Set the values, save them and then send the DNP3.0 file to the device



3 CONFIGURING THE REDUNDANT ETHERNET BOARD

An IP address is a logical address assigned to devices in a computer network that uses the Internet Protocol (IP) for communication between nodes. IP addresses are stored as binary numbers but they are represented using Decimal Dot Notation, whereby four sets of decimal numbers are delimited by dots as follows:

XXX.XXX.XXX.XXX

For example: 10.86.254.85

An IP address within a network is usually associated with a subnet mask that defines which network the device resides. A subnet mask takes the same form of an IP address.

For example: 255.255.255.0

A full explanation of IP addressing and subnet masking is beyond the scope of this guide. Further information is available on application.

Both the IED and the REB (Redundant Ethernet Board) each have their own IP address. Figure 9 shows the IED as IP1 and the REB as IP2.

Note: IP1 and IP2 are different but use the same subnet mask.

The switch IP address must be configured through the network.

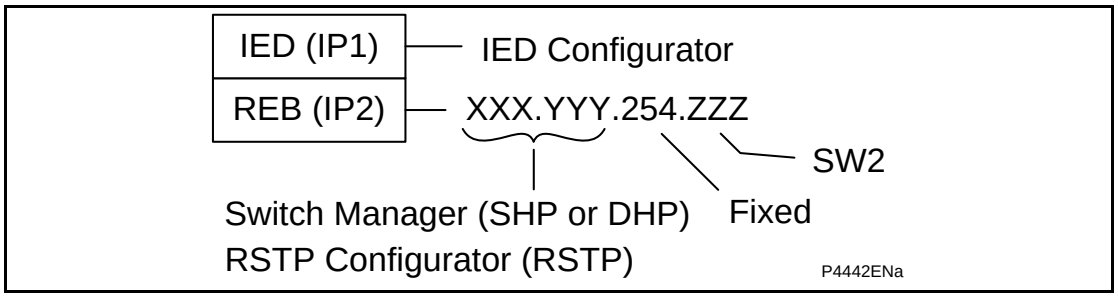


Figure 9: IED and REB IP address configuration

3.1 Configuring the IED IP address

The IP address of the IED is configured using the IED Configurator software in S1 Agile.

For IEC 61850, the IED IP address is set using the IED Configurator.

For DNP3 over Ethernet, the IED IP address is managed directly through the DNP3 file.

There are 254 addresses available, which are configurable in the last octet. These are within the range 01 to 254 decimal, which is equivalent 01 to FE hexadecimal, or 00000001 to 11111110 binary.

As with all IP networks, the first and last addresses (00 and FF) should not be used as these are reserved for the network address and broadcast address respectively.

Note: In the IED Configurator, ensure that the port type is set to "Copper" (even if redundant fibres are being used)

3.2 Configuring the Board IP Address

The IP address of the REB is configured in both software and hardware, as shown in Figure 9. Therefore this must be configured before connecting the IED to the network to avoid an IP address conflict.

Configuring the First Two Octets of the Board IP Address

If using SHP or DHP, the first two octets are configured using Switch Manager or an SNMP MIB browser. An H35 (SHP) or H36 (DHP) network device is needed in the network to configure the Px40 redundant Ethernet board IP address using SNMP.

If using Rapid Spanning Tree Protocol (RSTP), the first two octets are configured using the RSTP Configurator software tool or using an SNMP MIB browser.

Configuring the Third Octet of the Board IP Address

The third octet is fixed at 254 (FE hex, 11111110 binary, regardless of the protocol.

Configuring the Last Octet of the Board IP Address

The last octet is configured using the 8-way board address DIP switch SW2 on the REB.

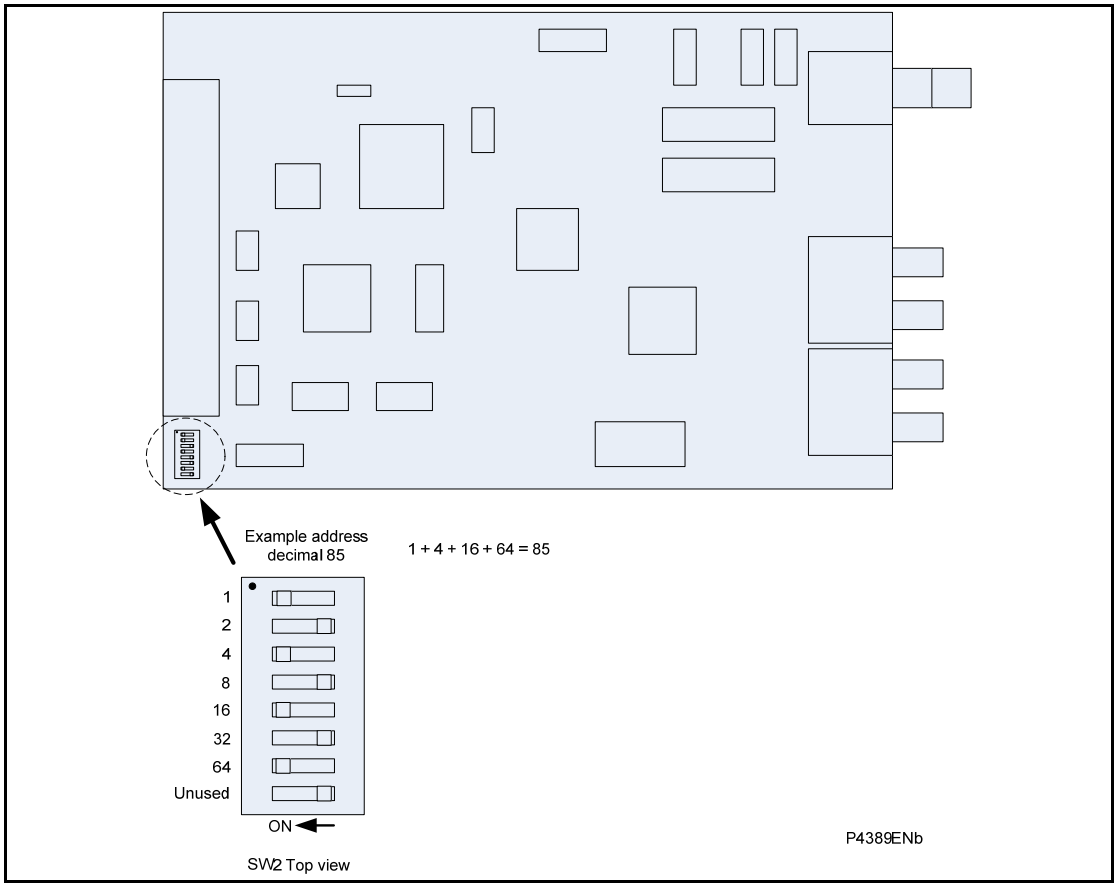


Figure 10: REB address switches (SW2)

Details of how to access the switches on the REB are provided in the Installation chapter.

Caution: This hardware configuration should ideally take place before the unit is installed. If this is not possible, this must be carried out by authorized installation engineers.

3.3 RSTP Configuration

If you are using RSTP, you will need the RSTP configurator software. This is available from General Electric on request.

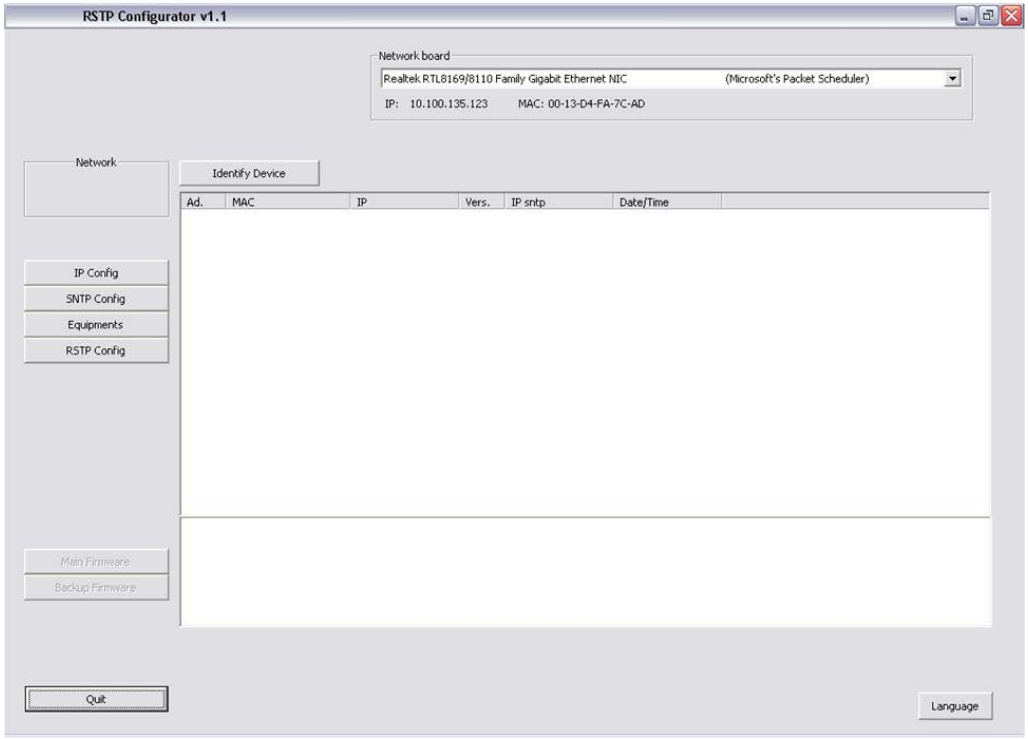
The RSTP Configurator software is used to identify a device, configure the IP address, configure the SNTP IP address and configure RSTP settings.

Installing RSTP Configurator

1. Double click **WinPcap_4_0.exe** to install WinPcap.
2. Double click **ALSTOM Grid-RSTP Configurator.msi** to install the RSTP Configurator.
3. The setup wizard appears. Click **Next** and follow the on-screen instructions to run the installation.

Starting the RSTP Configurator

1. To start the RSTP Configurator, select **Programs > RSTP Configurator > RSTP Configurator**.
2. The Login screen appears. For user mode login, enter the Login name as **User** and click **OK** with no password.
3. If the login screen does not appear, check all network connections.
4. The main window of the RSTP Configurator appears. The Network Board drop-down list shows the Network Board, IP Address and MAC Address of the PC in which the RSTP Configurator is running.



Device Identification

1. To configure the REB, go to the main window and click **Identify Device**.
2. The REB connected to the PC is identified and its details are listed as shown below:
   - Device address
   - MAC address
   - Version number of the firmware
   - SNTP IP address
   - Date & time of the real-time clock, from the board.

Note: Due to the time needed to establish the RSTP protocol, it is necessary to wait 25 seconds between connecting the PC to the IED and clicking the **Identify Device** button.

IP Address Configuration

1. To change the network address component of the IP address, go to the main window and click the **IP Config** button. The Device setup screen appears. The first three octets of the board IP address can be configured.

Note: The last octet is set using the DIP switches (SW2) next to the ribbon connector.

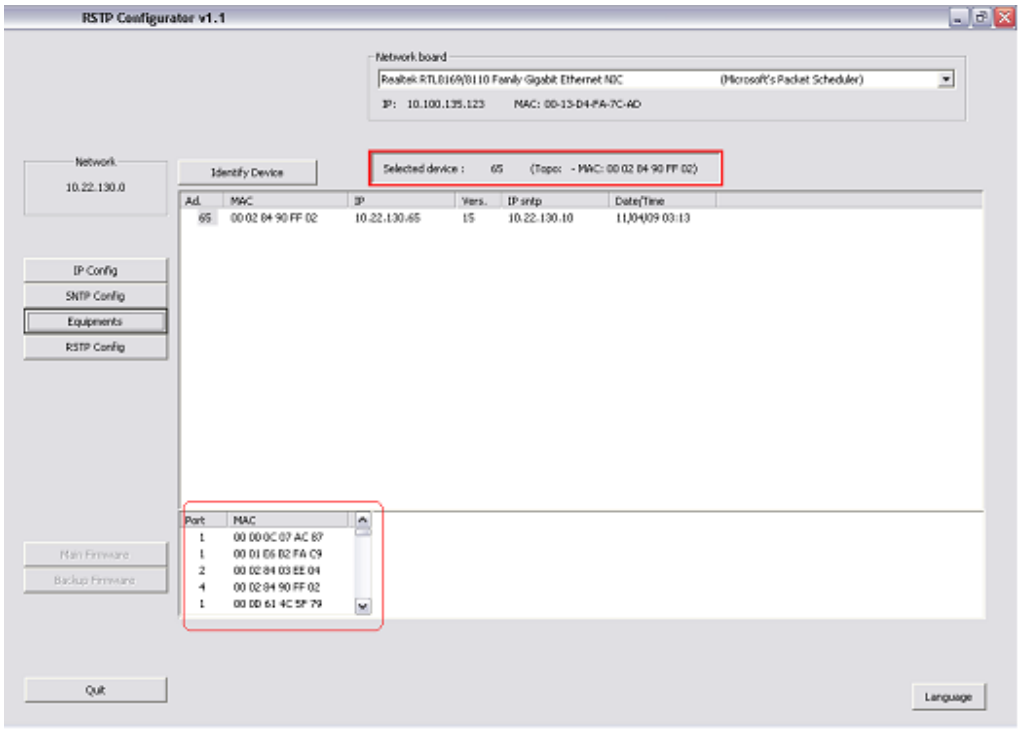
2. Enter the required board IP address and click OK. The board network address is updated and displayed in the main window.

SNTP IP Address Configuration

1. To Configure SNTP server IP address, go to the main window and click the SNTP Config button. The Device setup screen appears.
2. Enter the required SNTP MAC and server IP address, then click **OK**. The updated SNTP server IP address appears in the main screen.

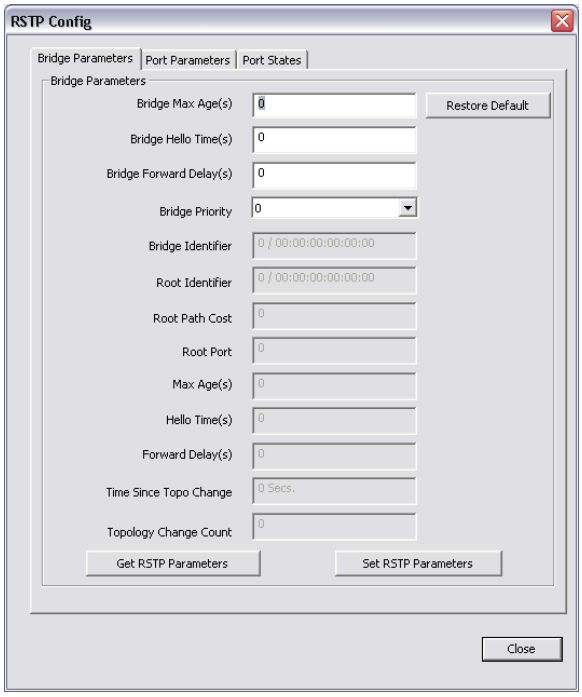
Equipment

1. To view the MAC addresses learned by the switch, go to the main window and click the Identify Device button. The selected device MAC address then appears highlighted.
2. Click the **Equipment** button. The list of MAC addresses learned by the switch and the corresponding port number are displayed.



RSTP Parameters

1. To view or configure the RSTP Bridge Parameters, go to the main window and click the device address to select the device. The selected device MAC address appears highlighted.
2. Click the **RSTP Config** button. The RSTP Config screen appears.



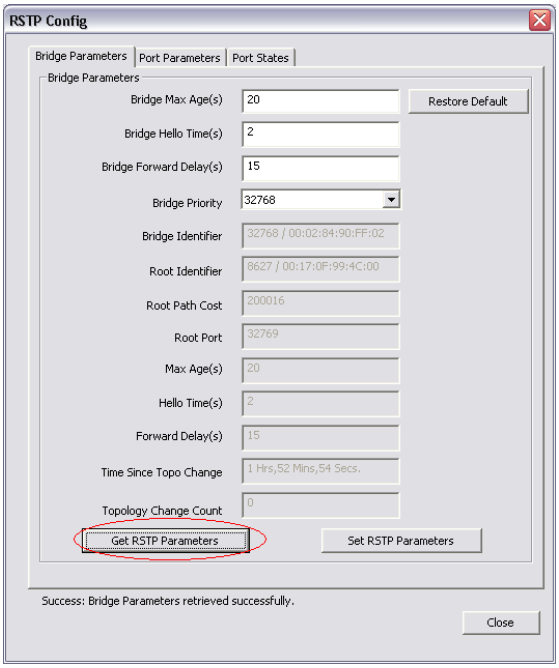
1. To view the available parameters in the board that is connected, click the **Get RSTP Parameters** button.
2. To set the configurable parameters such as **Bridge Max Age**, **Bridge Hello Time**, **Bridge Forward Delay**, and **Bridge Priority**, modify the parameter values and click **Set RSTP Parameters** as below:

S.No	Parameter	Default Value (seconds)	Minimum Value (seconds)	Maximum Value (seconds)
1	Bridge Max Age	20	6	40
2	Bridge Hello Time	2	1	10
3	Bridge Forward Delay	15	4	30
4	Bridge Priority	32768	0	61440

Bridge Parameters

1. To read the RSTP bridge parameters from the board, go to the main window and click the device address to select the device. The **RSTP Config** window appears and the default tab is **Bridge Parameters**.
2. Click the **Get RSTP Parameters** button. This displays all the RSTP bridge parameters from the Ethernet board.

GS

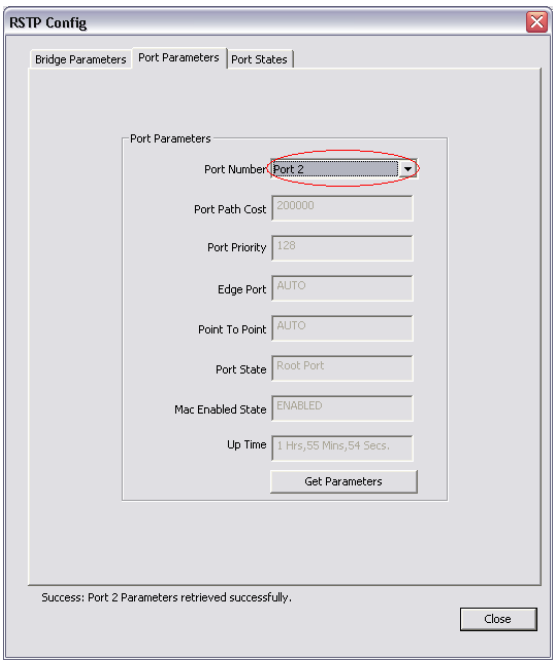


1. To modify the RSTP parameters, enter the values and click **Set RSTP Parameters**.
2. To restore the default values, click **Restore Default** and click **Set RSTP Parameters**.
3. The grayed parameters are read-only and cannot be modified.

Port Parameters

This function is useful if you need to view the parameters of each port.

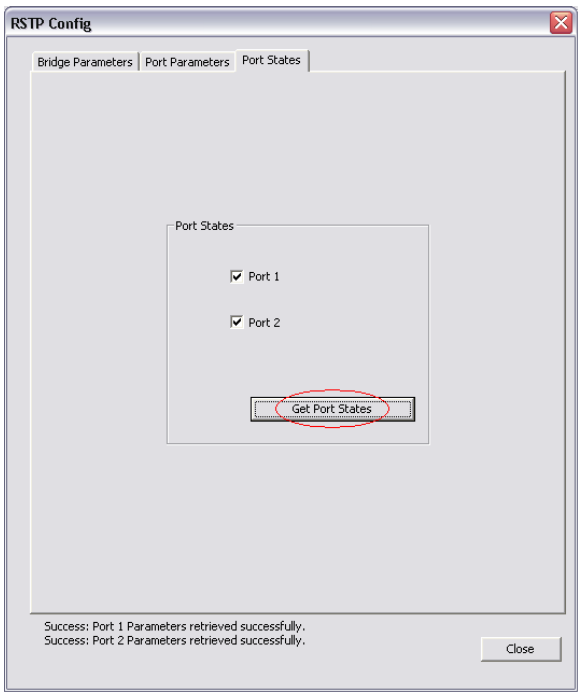
1. From the main window, click the device address to select the device and the **RSTP Config** window appears.
2. Select the **Port Parameters** tab, then click **Get Parameters** to read the port parameters.
3. Alternatively, select the port numbers to read the parameters.



Port States

This is used to see which ports of the board are enabled or disabled.

1. From the main window, click the device address to select the device. The **RSTP Config** window appears.
2. Select the **Port States** tab then click the **Get Port States** button. This lists the ports of the Ethernet board. A tick shows they are enabled.



4 CONFIGURING THE DATA PROTOCOLS

Depending on the model, various protocols can be used with the serial rear ports. However, only one protocol can be configured at any one time on any one IED. The range of available communication settings depend on which protocol has been chosen

4.1 Courier Configuration

To use the rear port with Courier, you can configure the settings using the HMI panel. Courier can be used with either a copper connection or a fibre connection.

1. Select the **CONFIGURATION** column and check that the **Comms settings** cell is set to Visible.
2. Select the **COMMUNICATIONS** column.
3. Move to the first cell down (**RP1 protocol**). This is a non settable cell, which shows the chosen communication protocol – in this case **Courier**.


```
COMMUNICATIONS
RP1 Protocol
              Courier
```

4. Move down to the next cell (**RP1 Address**). This cell controls the address of the IED. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. Courier uses an integer number between 0 and 254 for the IED address. It is important that no two IEDs have the same address.

```
COMMUNICATIONS
RP1 Address
                  255
```

5. Move down to the next cell (**RP1 InactivTimer**). This cell controls the inactivity timer. The inactivity timer controls how long the IED waits without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

```
COMMUNICATIONS
RP1 Inactivtimer
          10.00 mins.
```

6. If the optional fibre optic connectors are fitted, the **RP1 PhysicalLink** cell is visible. This cell controls the physical media used for the communication (**Copper** or **Fibre optic**).

```
COMMUNICATIONS
RP1 Physical Link
               Copper
```

7. Move down to the next cell (**RP1 Card Status**). This cell is not settable. It just displays the status of the chosen physical layer protocol for RP1.

```
COMMUNICATIONS
RP1 Card Status
             K-Bus OK
```

8. Move down to the next cell (**RP1 Port Config**). This cell controls the type of serial connection. Select between **K-Bus** or **RS485**.

```
COMMUNICATIONS
RP1 Port Config
K-Bus
```

9. If using EIA(RS)485, the next cell selects the communication mode. The choice is either **IEC 60870 FT1.2** for normal operation with 11-bit modems, or **10-bit no parity**. If using K-Bus this cell will not appear.

```
COMMUNICATIONS
RP1 Comms Mode
      IEC 60870 FT1.2
```

10. If using EIA(RS)485, the next cell down controls the baud rate. Three baud rates are supported; **9600**, **19200** and **38400**. If using K-Bus this cell will not appear as the baud rate is fixed at 64kbps.

```
COMMUNICATIONS
RP1 Baud Rate
                19200
```

Note: If you modify protection and disturbance recorder settings using an on-line editor such as PAS&T, you must confirm them. To do this, from the Configuration column select the Save changes cell. Off-line editors such as MiCOM S1 Agile do not need this action for the setting changes to take effect.

4.2 DNP3.0 configuration

To use the rear port with DNP3.0, you can configure the settings using the HMI panel. DNP3.0 can be used with either a copper connection or a fibre connection.

1. Select the **CONFIGURATION** column and check that the **Comms settings** cell is set to Visible.
2. Select the **COMMUNICATIONS** column.
3. Move to the first cell down (**RP1 protocol**). This is a non settable cell, which shows the chosen communication protocol – in this case **DNP3.0**.

```
COMMUNICATIONS
RP1 Protocol
               DNP3.0
```

4. Move down to the next cell (**RP1 Address**). This cell controls the DNP3.0 address of the IED. Up to 32 IEDs can be connected to one spur, therefore it is necessary for each IED to have a unique address so that messages from the master control station are accepted by only one IED. DNP3.0 uses a decimal number between 1 and 65519 for the IED address. It is important that no two IEDs have the same address.

```
COMMUNICATIONS
RP1 Address
                     1
```

5. Move down to the next cell (**RP1 Baud Rate**). This cell controls the baud rate to be used. Six baud rates are supported by the IED **1200bits/s**, **2400bits/s**, **4800bits/s**, **9600bits/s**, **19200bits/s** and **38400bits/s**. Make sure that the baud rate selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Baud rate
          9600 bits/s
```

6. Move down to the next cell (**RP1 Parity**). This cell controls the parity format used in the data frames. The parity can be set to be one of **None**, **Odd** or **Even**. Make sure that the parity format selected on the IED is the same as that set on the master station.


```
COMMUNICATIONS
RP1 Parity
                  None
```

7. If the optional fibre optic connectors are fitted, the **RP1 PhysicalLink** cell is visible. This cell controls the physical media used for the communication (**Copper** or **Fibre optic**).

```
COMMUNICATIONS
RP1 Physical Link
                Copper
```

8. Move down to the next cell (**RP1 Time Sync**). This cell sets the time synchronization request from the master by the IED. It can be set to **Enabled** or **Disabled**. If enabled it allows the DNP3.0 master to synchronize the time.

```
COMMUNICATIONS
RP1 Time sync
               Enabled
```

4.3 IEC 60870-5-103 Configuration

To use the rear port with IEC 60870-5-103, you can configure the settings using the HMI panel. IEC 60870-5-103 can be used with either a copper connection or a fibre connection.

The device operates as a slave in the system, responding to commands from a master station.

1. Select the **CONFIGURATION** column and check that the **Comms settings** cell is set to Visible.
2. Select the **COMMUNICATIONS** column.
3. Move to the first cell down (**RP1 protocol**). This is a non settable cell, which shows the chosen communication protocol – in this case **IEC 60870-5-103**.

```
COMMUNICATIONS
RP1 Protocol
      IEC 60870-5-103
```

4. Move down to the next cell (**RP1 Address**). This cell controls the IEC 60870-5-103 address of the IED. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. IEC 60870-5-103 uses an integer number between 0 and 254 for the IED address. It is important that no two IEDs have the same IEC 60870 5 103 address. The IEC 60870-5-103 address is then used by the master station to communicate with the IED.

```
COMMUNICATIONS
RP1 address
                  162
```

5. Move down to the next cell (**RP1 Baud Rate**). This cell controls the baud rate to be used. Two baud rates are supported by the IED, '**9600 bits/s**' and '**19200 bits/s**'. Make sure that the baud rate selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Baud rate
          9600 bits/s
```

6. Move down to the next cell (**RP1 Meas. period**). The next cell down controls the period between IEC 60870-5-103 measurements. The IEC 60870-5-103 protocol allows the IED to supply measurements at regular intervals. The interval between measurements is controlled by this cell, and can be set between 1 and 60 seconds.

```
COMMUNICATIONS
RP1 Meas. Period
              30.00 s
```

7. If the optional fibre optic connectors are fitted, the **RP1 PhysicalLink** cell is visible. This cell controls the physical media used for the communication (**Copper** or **Fibre optic**).

```
COMMUNICATIONS
RP1 Physical Link
               Copper
```

8. The next cell down can be used for monitor or command blocking.

```
COMMUNICATIONS
RP1 CS103Blcking
             Disabled
```

9. There are three settings associated with this cell; these are:

Setting:	Description:
Disabled	No blocking selected.
Monitor Blocking	When the monitor blocking DDB Signal is active high, either by energizing an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the device returns a “Termination of general interrogation” message to the master station.
Command Blocking	When the command blocking DDB signal is active high, either by energizing an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the device returns a “negative acknowledgement of command” message to the master station.

4.4 IEC 61850 Configuration

The only IEC 61850 configuration changes you can make with the HMI panel is to turn GOOSE on or off.

4.5 DNP3.0 Configuration Using MiCOM S1 Agile

A PC support package for DNP3.0 is available as part of MiCOM S1 Agile to allow configuration of the device's DNP3.0 response. The configuration data is uploaded from the device to the PC in a block of compressed format data and downloaded in a similar manner after modification. The new DNP3.0 configuration takes effect after the download is complete. To restore the default configuration at any time, from the **CONFIGURATION** column, select the **Restore Defaults** cell then select '**All Settings**'.

In MiCOM S1 Agile, the DNP3.0 data is shown in three main folders, one folder each for the point configuration, integer scaling and default variation (data format). The point configuration also includes screens for binary inputs, binary outputs, counters and analogue input configuration.

4.6 IEC 61850 Configuration

You cannot configure the device for IEC 61850 using the HMI panel on the product. For this you must use the IED Configurator.

IEC 61850 allows IEDs to be directly configured from a configuration file. The IED’s system configuration capabilities are determined from an **IED Capability Description** file (ICD), supplied with the product. By using ICD files from the products to be installed, you can design, configure and even test (using simulation tools), a substation’s entire protection scheme before the products are even installed into the substation.

To help with this process, MiCOM S1 Agile provides an IED Configurator tool, which allows the pre-configured IEC 61850 configuration file to be imported and transferred to the IED. As well as this, you can manually create configuration files for MiCOM IEDs, based on their original IED capability description (ICD file).

Other features include:

- The extraction of configuration data for viewing and editing.
- A sophisticated error checking sequence to validate the configuration data before sending to the IED.

Note: To help the user, some configuration data is available in the **IED CONFIGURATOR** column, allowing read-only access to basic configuration data.

4.6.1 IEC 61850 Configuration Banks

To help version management and minimize down-time during system upgrades and maintenance, the MiCOM IEDs have incorporated a mechanism consisting of multiple configuration banks. These configuration banks fall into two categories:

- Active Configuration Bank

- Inactive Configuration Bank

Any new configuration sent to the IED is automatically stored in the inactive configuration bank, therefore not immediately affecting the current configuration.

When the upgrade or maintenance stage is complete, the IED Configurator tool can be used to transmit a command, which authorizes activation of the new configuration contained in the inactive configuration bank. This is done by switching the active and inactive configuration banks. The capability of switching the configuration banks is also available using the **IED CONFIGURATOR** column of the HMI.

The SCL Name and Revision attributes of both configuration banks are also available in the **IED CONFIGURATOR** column of the HMI.

4.6.2 IEC 61850 Network Connectivity

Configuration of the IP parameters and SNTP time synchronization parameters is performed by the IED Configurator tool. If these parameters are not available using an SCL file, they must be configured manually.

As the IP addressing will be completely detached and independent from any public network, it is up to the company's system administrator to establish the IP addressing strategy. Every IP address on the network must be unique. This applies to all devices on the network. Duplicate IP addresses will result in conflict and must be avoided. The IED will check for a conflict on every IP configuration change and at power up. An alarm will be raised if an IP conflict is detected.

The IED can be configured to accept data from other networks using the **Gateway** setting. If multiple networks are used, the IP addresses must be unique across networks.

ST

SETTINGS

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

ST

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1 SETTINGS

The P342/3/4/5/6/8 must be configured to the system and application using appropriate settings. In this chapter settings are described in sequence: protection settings, control and configuration settings and the disturbance recorder settings. The relay is supplied with a factory-set configuration of default settings.

1.1 Relay settings configuration

The relay is a multi-function device that supports numerous different protection, control and communication features. To simplify the setting of the relay, there is a configuration settings column which can be used to enable or disable many of the functions of the relay. The settings associated with any disabled function are not shown in the menu. To disable a function change the relevant cell in the **Configuration** column from **Enabled** to **Disabled**.

The configuration column controls which of the four protection settings groups is selected as active through the **Active settings** cell. A protection setting group can also be disabled in the configuration column, provided it is not the present active group. Similarly, a disabled setting group cannot be set as the active group.

The configuration column also allows all of the setting values in one group of protection settings to be copied to another group.

To do this first set the **Copy from** cell to the protection setting group to be copied, then set the **Copy to** cell to the protection group where the copy is to be placed. The copied settings are initially placed in a temporary scratchpad and will only be used by the relay following confirmation.

To restore the default values to the settings in any protection settings group, set the **Restore Defaults** cell to the relevant group number. Alternatively, set the **Restore Defaults** cell to **All Settings** to restore all of the relay's settings to default values, not just the protection groups' settings. The default settings are initially placed in the scratchpad and are only used by the relay after they have been confirmed.

Note: That restoring defaults to all settings includes the rear communication port settings may result in communication via the rear port being disrupted if the new (default) settings do not match those of the master station.

Menu text	Default setting	Available settings
Restore Defaults	No Operation	No Operation All Settings Setting Group 1 Setting Group 2 Setting Group 3 Setting Group 4
Setting to restore a setting group to factory default settings.		
Setting Group	Select via Menu	Select via Menu Select via PSL
Allows setting group changes to be initiated via 2 DDB signals in the programmable scheme logic or via the Menu settings.		
Active Settings	Group 1	Group 1, Group 2, Group 3 Group 4
Selects the active setting group.		
Save Changes	No Operation	No Operation, Save, Abort
Saves all relay settings.		
Copy from	Group 1	Group 1, 2, 3 or 4
Allows displayed settings to be copied from a selected setting group.		
Copy to	No Operation	No Operation Group 1, 2, 3 or 4
Allows displayed settings to be copied to a selected setting group. (ready to paste).		

Menu text	Default setting	Available settings
Setting Group 1	Enabled	Disabled, Enabled
To enable or disable Group 1 settings. If the setting group is disabled from the configuration, then all associated settings and signals are hidden, with the exception of this setting. (paste).		
Setting Group 2 (as above)	Disabled	Disabled, Enabled
Setting Group 3 (as above)	Disabled	Disabled, Enabled
Setting Group 4 (as above)	Disabled	Disabled, Enabled
System Config	Visible	Invisible, Visible
Sets the System Config menu visible further on in the relay settings menu.		
Power	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the 3 phase Power Protection function, reverse power / low forward power / overpower. ANSI 32R/32LFP/32O. P342-6		
Field Failure	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Field Failure Protection function. ANSI 40. P342-6		
NPS Thermal	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Negative Phase Sequence Thermal Protection function. ANSI 46T. P342-6		
System Backup	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the System Backup Protection function, voltage controlled / voltage restrained / underimpedance protection. ANSI 51V/21. P342-6		
Overcurrent	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Phase Overcurrent and NPS Overcurrent Protection function. ANSI 50/51/67P, 46OC. P342-6 and P348		
Thermal Overload	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Thermal Overload (Generator and Transformer Thermal Overload) Protection function. ANSI 49. P342-6		
Differential	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Differential (Generator and Transformer Differential) Protection function. ANSI 87G/87T. P343-6		
Earth Fault	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Earth Fault Protection function. ANSI 50N/51N. P342-6		
Rotor EF	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Rotor Earth Fault Protection function. ANSI 64R. P342-6		
SEF/REF/SPower	SEF/REF	Disabled or SEF/REF or Sensitive Power
Enables (activates) or disables (turns off) the Sensitive Earth Fault or Restricted Earth Fault or Sensitive Power (1 Phase) Protection (reverse power / low forward power / overpower) function. ANSI 50/51/67N, 64, 32R/32LFP/32O. P342-6		
Residual O/V NVD	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Residual Overvoltage (Neutral Voltage Displacement) Protection function. ANSI 59N. P342-6 and P348		

Menu text	Default setting	Available settings
100% Stator EF	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the 100% Stator Earth Fault Protection function (3rd harmonic in P343, 4, 5 and low frequency injection in P345). ANSI 27TN/59TN (3rd harmonic), 64S (low frequency injection). P343-5		
V/Hz	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Overfluxing Protection function. ANSI 24. P342-6		
df/dt	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Rate of Change of Frequency Protection function. ANSI 81R. P342-6		
Dead Machine	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Dead Protection function. ANSI 50/27. P342-6		
Volt Protection	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Voltage Protection (Under/Overvoltage and NPS Overvoltage) function. ANSI 27/59/47. P342-6 and P348		
Freq Protection	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Frequency Protection (Under/Overfrequency) function. ANSI 81O/U. P342-6 and P348		
RTD Inputs	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the RTD (Resistance Temperature Device) Inputs. P342-6		
CB Fail	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Circuit Breaker Fail Protection function. ANSI 50BF. P342-6		
Supervision	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Supervision (VTS&CTS) functions. ANSI VTS/CTS. P342-6 and P348		
Pole Slipping	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the Pole Slipping Protection function. ANSI 78. P343-5		
Input Labels	Visible	Invisible, Visible
Sets the Input Labels menu visible in the relay settings menu.		
Output Labels	Visible	Invisible, Visible
Sets the Output Labels menu visible in the relay settings menu.		
RTD Labels	Visible	Invisible, Visible
Sets the RTD Labels menu visible in the relay settings menu. P342-6		
CT & VT Ratios	Visible	Invisible, Visible
Sets the Current & Voltage Transformer Ratios menu visible in the relay settings menu.		
Record Control	Invisible	Invisible, Visible
Sets the Record Control menu visible in the relay settings menu.		
Disturb Recorder	Invisible	Invisible, Visible
Sets the Disturbance Recorder menu visible in the relay settings menu.		
Measure't Set-up	Invisible	Invisible, Visible
Sets the Measurement Setup menu visible in the relay settings menu.		
Comms Settings	Visible	Invisible, Visible
Sets the Communications Settings menu visible in the relay settings menu. These are the settings associated with the 1st and 2nd rear communications ports.		

Menu text	Default setting	Available settings
Commission Tests	Visible	Invisible, Visible
Sets the Commissioning Tests menu visible in the relay settings menu.		
Setting Values	Primary	Primary, Secondary
This affects all protection settings that are dependent upon CT and VT ratio's.		
Control Inputs	Visible	Invisible, Visible
Sets the Control Inputs menu visible in the relay setting menu.		
CLIO Inputs	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the CLIO (Current Loop Input Output) Inputs function.		
CLIO Outputs	Enabled	Disabled, Enabled
Enables (activates) or disables (turns off) the CLIO (Current Loop Input Output) Outputs function.		
System Checks	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the System Checks (Check Sync. and Voltage Monitor) function. ANSI 25. P342-6		
Ctrl I/P Config.	Visible	Invisible, Visible
Sets the Control Input Configuration menu visible in the relay setting menu.		
Ctrl I/P Labels	Visible	Invisible, Visible
Sets the Control Input Labels menu visible in the relay setting menu.		
Direct Access	Enabled	Disabled/Enabled/Hotkey Only /CB Cntrl Only.
Defines what controls are available via the direct access keys - Enabled (Hotkey and CB Control functions) / Hotkey Only (Control Inputs and Setting group selection) / CB Cntrl Only (CB open/close).		
IEC GOOSE	Visible	Invisible, Visible
Sets the IEC61850 GOOSE menu visible in the relay setting menu.		
Function Key	Visible	Invisible, Visible
Sets the Function Key menu visible in the relay setting menu. P343-6 and P348		
RP1 Read Only	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the rear communications port 1 (RP1) Read Only function.		
RP2 Read Only	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the rear communications port 2 (RP2) Read Only function.		
NIC Read Only	Disabled	Disabled, Enabled
Enables (activates) or disables (turns off) the rear Ethernet communications port (NIC) Read Only function.		
LCD Contrast	11	0…31
Sets the LCD contrast. To confirm acceptance of the contrast setting the relay prompts the user to press the right and left arrow keys together instead of the enter key as an added precaution to someone accidentally selecting a contrast which leaves the display black or blank. **Note:** The LCD contrast can be set via the front port communications port with the S1 setting software if the contrast is set incorrectly such that the display is black or blank.		

Table 1: General configuration settings

1.2 Protection settings

The P342-8 protection settings include all the following items that become active once enabled in the configuration column of the relay menu database:

- Protection element settings.
- Scheme logic settings.

There are four groups of protection settings, with each group containing the same setting cells. One group of protection settings is selected as the active group, and is used by the protection elements. The settings for group 1 only are shown below. The settings are discussed in the same order in which they are displayed in the menu.

1.2.1 System config

The P34x maintains correct operation of all the protection functions even when the generator is running in a reverse phase sequence and for generator-transformer applications. This is achieved through user configurable settings available for the four setting groups.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: SYSTEM CONFIG				
Winding Config	Generator	Generator, Xformer		
The winding type may be configured as Generator or Xformer (Generator-transformer). This setting makes the Generator Diff or Xformer Diff settings visible in the DIFFERENTIAL menu P343-6.				
Ref Power S	100 MVA	0.1 MVA	5000 MVA	0.1 MVA
Reference power. Used by the differential function to calculate the ratio correction factors. Used by the transformer thermal function to calculate the rated load current P343-6.				
HV Connection	Y-Wye	Y-Wye, D-Delta, Z-Zigzag		
The HV winding connections can be configured as Wye, Delta, or Zigzag P343-6.				
HV Grounding	Grounded	Grounded, Ungrounded		
In **DIFFERENTIAL** menu, the **Set Mode** setting can be set as **Simple** or **Advanced**. In simple mode when set as grounded, the P34x applies zero sequence filtering to the HV side current. When set as ungrounded, no zero sequence filtering is applied to the HV side current. In advanced mode, the HV Grounding setting is only for information and the zero sequence filtering depends on the Zero seq filt HV setting. While **Zero seq filt HV** is set as **Enabled**, **the HV Grounding** setting will be set as **Grounded** automatically P343-6.				
HV Nominal	220 kV	100 V	1 MV	1 V
Nominal voltage of the HV winding. Typically set to the mid-tap voltage of the on-load tap changer, or no-load tap changer tap voltage P343-6.				
%Reactance	10%	1%	100%	0.1%
Transformer leakage reactance P343-6.				
LV Vector Group	0	0	11	1
This is used to provide vector correction for the phase shift between HV and LV windings P343-6.				
LV Connection	Y-Wye	Y-Wye, D-Delta, Z-Zigzag		
The LV winding connections can be configured as Wye, Delta, or Zigzag P343-6.				
LV Grounding	Grounded	Grounded, Ungrounded		
In **DIFFERENTIAL** menu, the **Set Mode** setting can be set as **Simple** or **Advanced**. In simple mode when set as grounded, the P34x applies zero sequence filtering to the LV side current. When set as ungrounded, no zero sequence filtering is applied to the LV side current. In advanced mode, the LV Grounding setting is only for information, and the zero sequence filtering depends on the Zero seq filt LV setting. While **Zero seq filt HV** is set as **Enabled**, **the HV Grounding** setting will be set as **Grounded** automatically P343-6.				
LV Nominal	220 kV	100 V	1 MV	1 V
Nominal voltage of the LV winding. Typically set to the mid-tap voltage of the on-load tap changer, or no-load tap changer tap voltage P343-6.				
Match Factor HV	This is only calculated by the relay.			
HV ratio correction factor used by the differential function P343-6.				
Match Factor LV	This is only calculated by the relay.			
LV ratio correction factor used by the differential function P343-6.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: SYSTEM CONFIG				
Phase Sequence	Standard ABC	Standard ABC, Reverse ACB		N/A
The Phase Sequence setting applies to a power system that has a permanent phase sequence of either ABC or ACB. It is also applicable for temporary phase reversal which affects all the 3 phase VTs and CTs P342-8.				
VT Reversal	No Swap	No Swap, A-B Swapped, B-C Swapped, C-A Swapped		N/A
The VT Reversal, CT1 Reversal and CT2 Reversal settings apply to applications where some or all of the 3 phase voltage or current inputs are temporarily reversed, as in pump storage applications. The settings affect the order of the analogue channels in the relay and are set to emulate the order of the channels on the power system P342-6.				
CT1 Reversal	No Swap	No Swap, A-B Swapped, B-C Swapped, C-A Swapped		N/A
As described above P342-6.				
CT2 Reversal	No Swap	No Swap, A-B Swapped, B-C Swapped, C-A Swapped		N/A)
As described above. P343, 4, 5, 6.				
C/S Input	A-N	A-N, B-N, C-N, A-B, B-C, C-A		
Selects the check synchronizing input voltage measurement P342-6.				
C/S V Ratio Corr	1	0.1	2	0.001
Check synchronizing voltage ratio correction. This is used by the System Check function to provide the magnitude correction for the difference between main VT and C/S VT. The Main VT is the reference, and the C/S VT is corrected to Main VT. The formula is: $V_{C/S\ VT\ Corrected} = V_{C/S\ VT}$ * C/S Ratio Corr P342-6.				
C/S VT Vect Grp	0	0	11	1
This is used to provide vector correction for the phase shift between main VT and C/S VT. The Main VT is the reference, and the C/S VT is corrected to Main VT. Two examples are shown below: Case1 (Main VT Location = Gen): For C/S VT Vect Grp = 0~5 The formula is: $\Theta_{c/s\ VT\ Corrected} = \theta_{C/S\ VT}$ - (C/S VT Vect Grp)*30°; And for C/S VT Vect Grp = 6~11 $\theta_{c/s\ VT\ Corrected} = \theta_{C/S\ VT}$ + (12-C/S VT Vect Grp)*30°. Case 2 (Main VT Location = Bus): For C/S VT Vect Grp = 0~5 The formula is: $\Theta_{c/s\ VT\ Corrected} = \theta_{C/S\ VT}$ + (C/S VT Vect Grp)*30°; And for C/S VT Vect Grp = 6~11 $\theta_{c/s\ VT\ Corrected} = \theta_{C/S\ VT}$ - (12-C/S VT Vect Grp)*30°.				
Main VT Location	Gen	Gen, Bus		
Selects the main voltage transformer location, Generator or Busbar P342-6.				
RMS F< Block	1Hz	0.1Hz	2Hz	0.1Hz
Blocks RMS based protection when the frequency is lower than this threshold. (P348)				
CounterSourcePSL	0000000000000000			
This menu cell sets the status of the 16 PSL counters as a binary string. A '1' allows the Counter to be set in the PSL and '0' allows the Counter to be set via the 'Counter 1-16' menu settings. The right hand bit represents Counter 1 and the left hand bit represent Counter 16.				
Counter 1	65535	1	65535	1
Counter 1 setting				
Counter 2-16	65535	1	65535	1
Counter 2-16 setting				
Counter 1 Label	Counter 1	16 Character Text		
Text label to describe each counter. This text will be displayed in the programmable scheme logic and event record description of the counter.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: SYSTEM CONFIG				
Counter 2-16 Label	Counter 2-16	16 Character Text		
Text label to describe each counter. This text will be displayed in the programmable scheme logic and event record description of the counter.				
Timer 1	0 ms	0 ms	14400 ms	1 ms
PSL Timer 1 setting. If the timer is selected as 'Menu Set' in PSL timer element then the timer value can be set in the menu settings using this cell.				
Timer 2-16	0 ms	0 ms	14400 ms	1 ms
PSL Timer 2-16 setting. If the timer is selected as 'Menu Set' in PSL timer element then the timer value can be set in the menu settings using this cell.				

Table 2: System configuration settings

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1.2.2 Power protection (32P/Q)

The 3 phase power protection included in the P342/3/4/5/6 relay provides four stages of power protection. Each stage can be independently selected to operate as either under or over or disabled. The direction of operation of the power protection, forward or reverse, can also be defined with the direction setting. Each stage can be independently selected to operate as either active or reactive power. There is also a single stage NPS overpower protection function.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: POWER				
Comp Angle	0	-5°	5°	
Setting for the compensation angle.				
Power1 Function	Over	Disabled, Under, Over		
First stage power function operating mode, under or over.				
Power1 Dirn	Forward	Forward, Reverse		
First stage power function direction, forward or reverse.				
Power1 Mode	Active	Active, Reactive		
First stage power function power mode, active or reactive power.				
Power1 3Ph Watts	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the first stage 3 phase active power protection element.				
Power1 3Ph VArs	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the first stage 3 phase reactive power protection element.				
Power1 Time Delay	5 s	0 s	100 s	0.1 s
Operating time-delay setting of the first stage power protection.				
Power1 DO Timer	0 s	0 s	10 s	0.1 s
Drop-off time delay setting of the first stage power protection function. Setting of the drop-off timer to a value other than zero, delays the resetting of the protection element timers for this period. By using the drop-off timer the relay will integrate the fault power pulses, thereby reducing fault clearance times.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: POWER				
P1 Poledead Inh	Enabled	Disabled, Enabled		
If the setting is enabled, the relevant stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the power protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
Power2 Function	Over	Disabled, Under, Over		
Second stage power function operating mode, under or over.				
Power2 Dirn	Forward	Forward, Reverse		
Second stage power function direction, forward or reverse.				
Power2 Mode	Active	Active, Reactive		
Second stage power function power mode, active or reactive power.				
Power2 3Ph Watts	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the second stage 3 phase active power protection element.				
Power2 3Ph VArs	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the second stage 3 phase reactive power protection element.				
Power2 Time Delay	5 s	0 s	100 s	0.1 s
Operating time-delay setting of the second stage power protection.				
Power2 DO Timer	0 s	0 s	10 s	0.1 s
Drop-off time delay setting of the second stage power protection function. Setting of the drop-off timer to a value other than zero, delays the resetting of the protection element timers for this period. By using the drop-off timer the relay will integrate the fault power pulses, thereby reducing fault clearance times.				
P2 Poledead Inh	Enabled	Disabled, Enabled		
If the setting is enabled, the relevant stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the power protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
Power3 Function	Disabled	Disabled, Under, Over		
Third stage power function operating mode, under or over.				
Power3 Dirn	Forward	Forward, Reverse		
Third stage power function direction, forward or reverse.				
Power3 Mode	Active	Active, Reactive		
Third stage power function power mode, active or reactive power.				
Power3 3Ph Watts	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the third stage 3 phase active power protection element.				
Power3 3Ph VArs	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the third stage 3 phase reactive power protection element				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: POWER				
Power3 Time Delay	5 s	0 s	100 s	0.1 s
Operating time-delay setting of the third stage power protection.				
Power3 DO Timer	0 s	0 s	10 s	0.1 s
Drop-off time delay setting of the third stage power protection function. Setting of the drop-off timer to a value other than zero, delays the resetting of the protection element timers for this period. By using the drop-off timer the relay will integrate the fault power pulses, thereby reducing fault clearance times.				
P3 Poledead Inh	Enabled	Disabled, Enabled		
If the setting is enabled, the relevant stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the power protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
Power4 Function	Disabled	Disabled, Under, Over		
Fourth stage power function operating mode, under or over.				
Power4 Dirn	Forward	Forward, Reverse		
Fourth stage power function direction, forward or reverse.				
Power4 Mode	Active	Active, Reactive		
Fourth stage power function power mode, active or reactive power.				
Power4 3Ph Watts	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the fourth stage 3 phase active power protection element.				
Power4 3Ph VArs	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the fourth stage 3 phase reactive power protection element.				
Power4 Time Delay	5 s	0 s	100 s	0.1 s
Operating time-delay setting of the fourth stage power protection.				
Power4 DO Timer	0 s	0 s	10 s	0.1 s
Drop-off time delay setting of the fourth stage power protection function. Setting of the drop-off timer to a value other than zero, delays the resetting of the protection element timers for this period. By using the drop-off timer the relay will integrate the fault power pulses, thereby reducing fault clearance times.				
P4 Poledead Inh	Enabled	Disabled, Enabled		
If the setting is enabled, the relevant stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the power protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
NPS OVERPOWER				
S2> CT Source	IA-1 IB-1 IC-1	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		
This setting is used to select the 3 phase current inputs used by the NPS OVERPOWER protection elements in the P343/4/5/6 - IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 CT inputs.				
S2>1 Status	Disabled	Disabled, Enabled		
Enables or disables the Negative Phase Sequence Overpower function.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: POWER				
S2>1 Setting	0.5 In VA (Vn=100/120 V) 2 In VA (Vn=380/480 V)	0.1 In VA (Vn=100/120 V) 0.4 In VA (Vn=380/480 V)	30 In VA (Vn=100/120 V) 120 In VA (Vn=380/480 V)	0.01 In VA (Vn=100/120 V) 0.04 In VA (Vn=380/480 V)
Pick-up setting for the NPS overpower protection element, S2 = V2xI2.				
S2>1 Time Delay	0.1 s	0	100 s	0.01 s
Operating time-delay setting of the NPS overpower protection.				

Table 3: Power protection settings

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1.2.3 Field failure protection (40)

The field failure protection included in the P342/3/4/5/6 relay provides two impedance based stages of protection and a directional line and a leading power factor alarm element. The directional line can be used to supervise the field failure impedance characteristics by blocking them in PSL.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: FIELD FAILURE				
FFail Alm Status	Disabled	Disabled, Enabled		
Enables or disables the Field Failure Alarm function.				
FFail Alm Angle	15°	15°	75°	1°
Pick-up setting for field failure alarm angle (leading power factor angle).				
FFail Alm Delays	5 s	0 s	100 s	0.1 s
Operating time-delay setting of the field failure alarm.				
FFail1 Status	Enabled	Disabled, Enabled		
Enables or disables the first stage field failure protection function.				
FFail1 Xa1	20/In Ω□□□□ (Vn=100/120 V) 80/In Ω (Vn=380/480 V)	-250/In Ω (Vn=100/120 V) -1000/In Ω (Vn=380/480 V)	250/In Ω (Vn=100/120 V) 1000/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)
Positive/negative reactance offset setting of first stage field failure impedance protection.				
FFail1 Xb1	220/In Ω (Vn=100/120 V) 880/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)	500/In Ω (Vn=100/120 V) 2000/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)
Diameter setting of circular impedance characteristic of first stage field failure protection.				
FFail1 TimeDelay	5 s	0 s	100 s	0.01 s
Operating time-delay setting of the field failure first stage protection.				
FFail1 DO Timer	0 s	0 s	10 s	0.01 s
Drop-off time delay setting of the first stage field failure protection function. Setting of the drop-off timer to a value other than zero, delays the resetting of the protection element timers for this period. By using the drop-off timer the relay will integrate the fault impedance pulses, for example during pole slipping, thereby reducing fault clearance times.				
FFail2 Status	Enabled	Disabled, Enabled		
Enables or disables the second stage field failure protection function.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: FIELD FAILURE				
FFail2 Xa2	20/In Ω (Vn=100/120 V) 80/In Ω (Vn=380/480 V)	-250/In Ω (Vn=100/120 V) -1000/In Ω (Vn=380/480 V)	250/In Ω (Vn=100/120 V) 1000/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)
Positive/negative reactance offset setting of second stage field failure impedance protection.				
FFail2 Xb2	220/In Ω (Vn=100/120 V) 880/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)	500/In Ω (Vn=100/120 V) 2000/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)
Diameter setting of circular impedance characteristic of second stage field failure protection.				
FFail2 TimeDelay	5 s	0 s	100 s	0.01 s
Operating time-delay setting of the field failure second stage protection.				
FFail2 DO Timer	0 s	0 s	10 s	0.01 s
Drop-off time delay setting of the second stage field failure protection function. Setting of the drop-off timer to a value other than zero, delays the resetting of the protection element timers for this period. By using the drop-off timer the relay will integrate the fault impedance pulses, for example during pole slipping, thereby reducing fault clearance times.				
FFail Dirn Line	Disabled	Disabled, Enabled		
Enables or disables the directional line.				
Line Offset	0/In Ω (Vn=100/120 V) 0/In Ω (Vn=380/480 V)	-250/In Ω (Vn=100/120 V) -1000/In Ω (Vn=380/480 V)	250/In Ω (Vn=100/120 V) 1000/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)
Directional line impedance offset.				
Line Angle	0°	-180°	180°	0.1°
Directional line angle.				

Table 4: Field failure protection settings

1.2.4 NPS thermal (46T)

The negative phase sequence (NPS) thermal protection included in the P342/3/4/5/6 relay provides a definite time alarm stage and a thermal trip stage.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: NPS Thermal				
I2therm>1 Alarm	Enabled	Disabled, Enabled		
Enables or disables the negative phase sequence (NPS) Thermal Alarm function.				
I2therm>1 Set	0.05 In A	0.03 In A	0.5 In A	0.01 In A
Pick-up setting for NPS thermal alarm.				
I2therm>1 Delay	20 s	0 s	100 s	0.01 s
Operating time-delay of the NPS thermal alarm.				
I2therm>2 Trip	Enabled	Disabled, Enabled		
Enables or disables the NPS Thermal Trip function.				
I2therm>2 set	0.1 In	0.05 In	0.5 In	0.01 In
Pick-up setting for NPS thermal trip.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: NPS Thermal				
I2therm>2 kSet	15 s	2 s	40 s	0.1 s
Thermal capacity constant setting of the NPS thermal characteristic.				
I2therm>2 kRESET	15 s	2 s	40 s	0.1 s
Reset (cooling) thermal capacity constant setting of the NPS thermal characteristic.				
I2therm>2 tMAX	1000 s	500 s	2000 s	10 s
Maximum operating time setting of the NPS thermal characteristic.				
I2therm>2 tMIN	0.25 s	0 s	100 s	0.01 s
Minimum operating time setting of the NPS thermal characteristic				

Table 5: NPS thermal protection settings

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1.2.5 System backup protection (51V/21)

The system backup protection included in the P342/3/4/5/6 relay provides a single stage of voltage restrained or voltage controlled overcurrent protection or a two stage underimpedance protection.

The voltage dependent overcurrent protection have time-delayed characteristics which are selectable between inverse definite minimum time (IDMT), or definite time (DT) or a user curve (Default Curve 1/2/3/4). The underimpedance protection is definite time only.

The voltage controlled overcurrent pick-up setting (V Dep OC I> Set) is modified by a multiplying factor (V Dep OC k Set) when the voltage is below a specific voltage (V Dep OC V<1Set).

The voltage restrained overcurrent pick-up setting varies on a linear scale between the two voltage thresholds, V Dep OC V<1 Set and V Dep OC V<2 Set. The pick-up setting is V Dep OC I> Set when the voltage is greater than V Dep OC V<1 Set and is V Dep OC I> Set x V Dep OC k Set when the voltage is less than V Dep OC V<2 Set.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: System Back-up				
V Dep OC Func	Voltage Controlled	Disabled, Voltage Controlled, Voltage Restrained		
Voltage dependant overcurrent protection operating mode.				
Vector Rotation	None	None, Delta-Star		N/A
Selection of Delta-Star voltage vector correction, enabled where there is a delta-star step-up transformer to improve sensitivity for HV phase faults.				
V Dep OC Char	IEC S Inverse	DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, UK Rectifier, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, Default Curve 1/2/3/4		
Selection of the tripping characteristic for the voltage dependent overcurrent protection.				
V Dep OC I> Set	1 x In A	0.8 x In A	4 x In A	0.01 x In A
Pick-up setting for voltage controlled and restrained overcurrent trip.				
V Dep OC T Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
V Dep OC Reset	DT	DT or Inverse		N/A
Type of reset/release characteristic of the IEEE/US curves and user programmable curves.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: System Back-up				
V Dep OC Delay	1 s	0 s	100 s	0.01 s
Operating time-delay setting for the definite time setting if selected for the voltage controlled or restrained overcurrent protection.				
V Dep OC TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
V Dep OC K(RI)	1	0.1	10	0.05
Time multiplier setting to adjust the operating time for the RI curve.				
V Dep OC Usr Rst	DT	DT, Default Curve 1/2/3/4		
Type of reset/release characteristic of the user curves				
V Dep OC tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
V Dep OC V<1Set	80V (Vn=100/120 V) 320 V (Vn=380/480 V)	5 V (Vn=100/120 V) 20 V (Vn=380/480 V)	120 V (Vn=100/120 V) 480 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)
Undervoltage setting for voltage controlled and restrained overcurrent characteristic.				
V Dep OC V<2Set	60 V (Vn=100/120 V) 240 V (Vn=380/480 V)	5 V (Vn=100/120 V) 20 V (Vn=380/480 V)	120 V (Vn=100/120 V) 480 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)
Undervoltage setting for voltage restrained overcurrent characteristic.				
V Dep OC k Set	0.25	0.1	1	0.05 s
Multiplying factor for voltage controlled and restrained overcurrent protection, pick-up setting is 'V Dep OC I> Set x V Dep OC k Set' dependent on the voltage level.				
Z< Function	Enabled	Disabled, Enabled		
Enables or disables the under impedance function.				
Vector Rotation	None	None, Delta-Star		
Selection of Delta-Star voltage vector correction, enabled where there is a delta-star step-up transformer to improve sensitivity for HV phase faults.				
Z<1 Status	Enabled	Disabled, Enabled		
Enables or disables the first stage under-impedance function.				
Z<1 Setting	70/InΩ (Vn=100/120 V) 120/InΩ (Vn=380/480 V)	2/InΩ (Vn=100/120 V) 8/InΩ (Vn=380/480 V)	500/InΩ (Vn=100/120V) 2000/InΩ (Vn=380/480V)	0.5/InΩ (Vn=100/120 V) 2/InΩ (Vn=380/480 V)
Pick-up impedance setting for first stage underimpedance protection.				
Z<1 Time Delay	5 s	0 s	100 s	0.01 s
Operating time-delay setting of the first stage underimpedance protection.				
Z<1 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for the first stage underimpedance protection.				
Z<2 Status	Disabled	Disabled, Enabled		
Enables or disables the second stage underimpedance function.				
Z<2 Setting	70/InΩ (Vn=100/120 V) 120/InΩ (Vn=380/480 V)	2/InΩ (Vn=100/120 V) 8/InΩ (Vn=380/480 V)	500/InΩ (Vn=100/120 V) 2000/InΩ (Vn=380/480 V)	0.5/InΩ (Vn=100/120 V) 2/InΩ (Vn=380/480 V)
Pick-up impedance setting for second stage underimpedance protection.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: System Back-up				
Z<2 Time Delay	5 s	0 s	100 s	0.01 s
Operating time-delay setting of the second stage underimpedance protection				
Z<2 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for the second stage underimpedance protection.				

Table 6: System backup protection settings

1.2.6 Phase overcurrrent protection (50/51/46OC)

The overcurrent protection included in the P342/3/4/5/6 relay provides four stage non-directional / directional three-phase overcurrent protection with independent time delay characteristics. All overcurrent and directional settings apply to all three phases but are independent for each of the four stages.

The first two stages of overcurrent protection have time-delayed characteristics which are selectable between inverse definite minimum time (IDMT), or definite time (DT) or a user curve (Default Curve 1/2/3/4). The third and fourth stages have definite time characteristics only.

The overcurrent protection menu also includes settings for four stages of non-directional / directional negative phase sequence (NPS) overcurrent protection with independent definite time delay characteristics.

The overcurrent protection included in the P348 relay provides four stages of non-directional three-phase RMS and four stages of non-directional three-phase peak (Sampled Values) overcurrent protection with independent definite time delay characteristics. Each peak overcurrent stage has an **SV iterations** setting for the number of samples required above setting to start. Each Peak and RMS overcurrent stage has an **I>x CT Source** setting used to select the 3 phase current inputs used by the peak overcurrent protection - **IA-1/IB-1/IC-1** (the rotor) or **IA-2/IB-2/IC-2** (the stator) CT inputs.

The first two stages of the RMS overcurrent protection have time-delayed characteristics which are selectable between inverse definite minimum time (IDMT), or definite time (DT) or a user curve. The third and fourth RMS overcurrent stages have definite time characteristics only. The four peak overcurrent stages have definite time characteristics only.

The P348 overcurrent protection menu also includes settings for four stages of non-directional RMS negative phase sequence (NPS) overcurrent protection with independent definite time delay characteristics.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: OVERCURRENT				
PHASE O/C				
I> CT Source	IA-1 IB-1 IC-1	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		
This setting is used to select the 3 phase current inputs used by the Phase Overcurrent elements in the P343/4/5/6 - IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 CT inputs.				
I>1 Function	IEC S Inverse	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, UK Rectifier, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, Default Curve 1/2/3/4		
Tripping characteristic for the first stage overcurrent protection.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
I>1 Direction	Non-directional	Non-directional Directional Fwd Directional Rev		
Direction of the first stage overcurrent protection.				
I>1 Current Set	1 In	0.08 In	4.0 In	0.01 In
Pick-up setting for first stage overcurrent protection.				
I>1 Time Delay	1 s	0 s	200 s	0.01 s
Operating time-delay setting for the definite time setting if selected for first stage element curves and user programmable curves.				
I>1 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I>1 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I>1 K (RI)	1	0.1	10	0.05
Time multiplier setting to adjust the operating time for the RI curve.				
I>1 Reset Char	DT	DT, Inverse		N/A
Type of reset/release characteristic of the IEEE/US curves.				
I>1 Usr Rst Char	DT	DT, Default Curve 1/2/3/4		N/A
Type of reset/release characteristic of the user curves.				
I>1 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
I>2 Cells as for I>1 above				
Setting the same as for the first stage overcurrent protection.				
I>3 Status	Disabled	Disabled, Enabled		N/A
Enable or disables the third stage overcurrent protection.				
I>3 Direction	Non-directional	Non-directional Directional Fwd Directional Rev		N/A
Direction of the third stage overcurrent protection.				
I>3 Current Set	10 In	0.08 In	10 In	0.01 In
Pick-up setting for third stage overcurrent protection.				
I>3 Time Delay	0 s	0 s	200 s	0.01 s
Operating time-delay setting for third stage overcurrent protection.				
I>4 Cells as for I>3 Above				
Settings the same as the third stage overcurrrent protection.				
I> Char. Angle	45°	–95°	+95°	1°
Relay characteristic angle setting used for the directional decision.				
I> Function Link	00001111	Bit 0 = VTS Blocks I>1, Bit 1 = VTS Blocks I>2, Bit 2 = VTS Blocks I>3, Bit 3 = VTS Blocks I>4, Bits 4 - 7 are not used.		
Logic Settings that determine whether blocking signals from VT supervision affect certain overcurrent stages. VTS Block – only affects directional overcurrent protection. With the relevant bit set to 1, operation of the Voltage Transformer Supervision (VTS), will block the stage. When set to 0, the stage will revert to Non-directional upon operation of the VTS.				

ST

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
NPS OVERCURRENT				
I2> CT Source	IA-1 IB-1 IC-1	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		
This setting is used to select the 3 phase current inputs used by the Negative Sequence Overcurrent elements in the P343/4/5/6 - IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 CT inputs.				
I2>1 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the first stage negative phase sequence overcurrent protection.				
I2>1Direction	Non-directional	Non-directional Directional Fwd Directional Rev		N/A
Direction of the negative phase sequence overcurrent element.				
I2>1 Current Set	0.2 In	0.08 In	4 In	0.01 In
Pick-up setting for the first stage negative phase sequence overcurrent protection.				
I2>1 Time Delay	10 s	0 s	100 s	0.01 s
Operating time-delay setting for the first stage negative phase sequence overcurrent protection.				
I2>2/3/4 Cells as for I2>1 Above				
I2> VTS Block	1111	Bit 0 = VTS blocks I2>1 Bit 1 = VTS blocks I2>2 Bit 2 = VTS blocks I2>3 Bit 3 = VTS blocks I2>4		
Logic settings that determine whether VT supervision blocks selected negative phase sequence overcurrent stages. With the relevant bit set to 1, operation of the Voltage Transformer Supervision (VTS), will block the stage. When set to 0, the stage will revert to Non-directional upon operation of the VTS.				
I2> V2pol Set	5 V (Vn=100/120 V) 20 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)	25 V (Vn=100/120 V) 100 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Minimum negative phase sequence voltage polarizing quantity for directional decision.				
I2> Char Angle	–60°	–95°	+95°	1°
Relay characteristic angle setting used for the directional decision.				

Table 7: Phase overcurrent protection settings (P342-6)

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: OVERCURRENT				
PHASE O/C PEAK				
I>1 Status	Enabled	Disabled, Enabled		
Enable or disables the first stage peak overcurrent protection.				
I>1 CT Source	IA-1 IB-1 IC-1	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		
This setting is used to select the 3 phase current inputs used by the first stage peak overcurrent protection - IA-1/IB-1/IC-1 (the rotor) or IA-2/IB-2/IC-2 (the stator) CT inputs.				
I>1 Current Set	1 In	0.08 In	32 In	0.01 In
Pick-up setting for first stage peak overcurrent protection.				
I>1 Time Delay	1 s	0 s	200 s	0.01 s
Operating time-delay setting for the definite time setting if selected for first stage element.				
I>1 tRESET	1 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
I>1 SVIterations	3	1	10	1
Sets the number of iterations of the sampled values used by the first stage Peak Overcurrent protection element to obtain a start signal.				
I>2 Status	Enabled	Disabled, Enabled		
Enable or disables the second stage peak overcurrent protection.				
I>2 CT Source	IA-2 IB-2 IC-2	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		
This setting is used to select the 3 phase current inputs used by the second stage peak overcurrent protection - IA-1/IB-1/IC-1 (the rotor) or IA-2/IB-2/IC-2 (the stator) CT inputs.				
I>2 Current Set	1 In	0.08 In	32 In	0.01 In
Pick-up setting for first stage peak overcurrent protection.				
I>2 Time Delay	1 s	0 s	200 s	0.01 s
Operating time-delay setting for the definite time setting if selected for first stage element.				
I>2 tRESET	1 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
I>2 SVIterations	3	1	10	1
Sets the number of iterations of the sampled values used by the second stage Peak Overcurrent protection element to obtain a start signal.				
I>3 Status	Enabled	Disabled, Enabled		
Enable or disables the third stage peak overcurrent protection.				
I>3 CT Source	IA-1 IB-1 IC-1	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		
This setting is used to select the 3 phase current inputs used by the third stage peak overcurrent protection - IA-1/IB-1/IC-1 (the rotor) or IA-2/IB-2/IC-2 (the stator) CT inputs.				
I>3 Current Set	10 In	0.08 In	32 In	0.01 In
Pick-up setting for third stage peak overcurrent protection.				
I>3 Time Delay	0 s	0 s	200 s	0.01 s
Operating time-delay setting for the definite time setting if selected for third stage element.				
I>3 tRESET	1 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
I>4 Status	Enabled	Disabled, Enabled		
Enable or disables the fourth stage peak overcurrent protection.				
I>4 CT Source	IA-2 IB-2 IC-2	IA-1 vB-1 IC-1, IA-2 IB-2 IC-2		
This setting is used to select the 3 phase current inputs used by the fourth stage peak overcurrent protection - IA-1/IB-1/IC-1 (the rotor) or IA-2/IB-2/IC-2 (the stator) CT inputs.				
I>4 Current Set	10 In	0.08 In	32 In	0.01 In
Pick-up setting for fourth stage peak overcurrent protection.				
I>4 Time Delay	0 s	0 s	200 s	0.01 s
Operating time-delay setting for the definite time setting if selected for fourth stage element.				
I>4 tRESET	1 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
PHASE O/C RMS				
I>5 Function	DT	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, UK Rectifier, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, Default Curve 1/2/3/4		N/A
Tripping characteristic for the fifth stage RMS overcurrent protection.				

ST

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
I>5 CT Source	IA-1 IB-1 IC-1	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		N/A
This setting is used to select the 3 phase current inputs used by the fifth stage RMS overcurrent protection - IA-1/IB-1/IC-1 (the rotor) or IA-2/IB-2/IC-2 (the stator) CT inputs.				
I>5 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for fifth stage RMS overcurrent protection.				
I>5 Time Delay	1 s	0 s	200 s	0.01 s
Operating time-delay setting for fifth stage RMS overcurrent protection.				
I>5 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I>5 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I>5 K (RI)	1	0.1	10	0.05
Time multiplier setting to adjust the operating time for the RI curve.				
I>5 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
I>6 Function	DT	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, UK Rectifier, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, Default Curve 1/2/3/4		N/A
Tripping characteristic for the sixth stage RMS overcurrent protection.				
I>6 CT Source	IA-2 IB-2 IC-2	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		N/A
This setting is used to select the 3 phase current inputs used by the sixth stage RMS overcurrent protection - IA-1/IB-1/IC-1 (the rotor) or IA-2/IB-2/IC-2 (normally the stator) CT inputs.				
I>6 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for fifth stage RMS overcurrent protection.				
I>6 Time Delay	1 s	0 s	200 s	0.01 s
Operating time-delay setting for fifth stage RMS overcurrent protection.				
I>6 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I>6 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves and user programmable curves.				
I>6 K (RI)	1	0.1	10	0.05
Time multiplier setting to adjust the operating time for the RI curve.				
I>6 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
I>7 Status	Enabled	Disabled, Enabled		N/A
Enable or disables the seventh stage RMS overcurrent protection.				
I>7 CT Source	IA-1 IB-1 IC-1	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		N/A
This setting is used to select the 3 phase current inputs used by the seventh stage RMS overcurrent protection - IA-1/IB-1/IC-1 (the rotor) or IA-2/IB-2/IC-2 (the stator) CT inputs.				
I>7 Current Set	10 In	0.08 In	32 In	0.01 In
Pick-up setting for seventh stage RMS overcurrent protection.				
I>7 Time Delay	0 s	0 s	200 s	0.01 s

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Operating time-delay setting for the definite time setting if selected for seventh stage element.				
I>8 Status	Enabled	Disabled, Enabled		N/A
Enable or disables the eighth stage RMS overcurrent protection.				
I>8 CT Source	IA-2 IB-2 IC-2	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		N/A
This setting is used to select the 3 phase current inputs used by the eighth stage RMS overcurrent protection - IA-1/IB-1/IC-1 (the rotor) or IA-2/IB-2/IC-2 (the stator) CT inputs.				
I>8 Current Set	10 In	0.08 In	32 In	0.01 In
Pick-up setting for seventh stage RMS overcurrent protection.				
I>8 Time Delay	0 s	0 s	200 s	0.01 s
Operating time-delay setting for the definite time setting if selected for seventh stage element.				
NPS OVERCURRENT				
I2>1 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the first stage stator negative phase sequence RMS overcurrent protection.				
I2>1 Current Set	0.2 In	0.03 In	4 In	0.01 In
Pick-up setting for the first stage stator negative phase sequence RMS overcurrent protection.				
I2>1 Time Delay	10 s	0 s	200 s	0.01 s
Operating time-delay setting for the first stage stator negative phase sequence RMS overcurrent protection.				
I2>2/3/4 Cells as for I2>1 Above				

Table 8: Phase overcurrent protection settings (P348)

1.2.7 Thermal overload (49)

The thermal overload function within the P342/3/4/5/6 relay is a single time constant thermal trip characteristic, dependent on the type of plant to be protected. It also includes a definite time alarm stage.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: THERMAL OVERLOAD				
GEN THERMAL				
Thermal	Enabled	Disabled, Enabled		
Enables or disables the Generator Thermal Overload trip function.				
Thermal I>	1.2 In	0.5 In	2.5 In	0.01 In
Pick-up setting for thermal overload trip.				
Thermal Alarm	90%	20%	100%	1%
Thermal state pick-up setting corresponding to a percentage of the trip threshold at which an alarm will be generated.				
T-heating	60 mins	1 min	200 mins	1 min
Heating thermal time constant setting for the thermal overload characteristic.				
T-cooling	60 mins	1 min	200 mins	1 min
Cooling thermal time constant setting for the thermal overload characteristic.				
M Factor	0	0	10	1
The M factor setting is a constant that relates negative phase sequence current heating to positive sequence current heating.				
XFORMER THERMAL				
Thermal	Enabled	Disabled, Enabled		

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Enables or disables the transformer Thermal Overload trip function.				
Mn't Winding	HV Current	HV Current, LV Current, Biased Current		
Monitored winding – HV current or LV current or Bias current. Bias current = (HV current + LV current)/2. The through load current of the transformer is monitored when the monitor winding is set to Biased Current.				
Ambient T	AVERAGE	RTD 1 to 10, CLIO1 to 4, AVERAGE		
The ambient temperature may be a setting (Average) or it may be measured using RTD or CLIO inputs.				
Amb CLI Type	4-20 mA	0-1 mA, 0-10 mA, 0-20 mA, 4-20 mA		
Ambient temperature current loop input type. This setting is available when Ambient T is set to CLIOx.				
Amb CLI Min	0	-9999	9999	0.1
Ambient temperature current loop input minimum setting. Defines the lower range of the ambient temperature measured by the transducer. This setting is available when Ambient T is set to CLIOx.				
Amb CLI Max	100	-9999	9999	0.1
Ambient temperature current loop input maximum setting. Defines the upper range of the ambient temperature measured by the transducer. This setting is available when Ambient T is set to CLIOx.				
Average Amb T	25°C	-25°C	75°C	0.1°C
Average ambient temperature. This setting is available when Ambient T is set to Average.				
Top Oil T	CALCULATED	RTD 1 to 10, CLIO1 to 4, CALCULATED		
The top oil temperature may be calculated by the relay, or it may be measured using RTD or CLIO inputs.				
Top Oil CLI Typ	4-20 mA	0	3	1
Top oil current loop input type. This setting is available when Top Oil T is set to CLIOx.				
Top Oil CLI Min	0	-9999	9999	0.1
Top oil temperature current loop input minimum setting. Defines the lower range of the top oil temperature measured by the transducer. This setting is available when Top Oil T is set to CLIOx.				
Top Oil CLI Max	100	-9999	9999	0.1
Top oil temperature current loop input maximum setting. Defines the upper range of the top oil temperature measured by the transducer. This setting is available when Top Oil T is set to CLIOx.				
IB	1 pu	0.1 pu	4 pu	0.01 pu
IB is the load in pu. It is recommended to set it to the rated load, of 1.0 pu. The relay uses this setting to calculate the ratio of ultimate load to rated load.				
Rated NoLoadLoss	3	0.1	100	0.1
Ratio of load loss at rated load to no-load loss (iron loss). The transformer manufacturer should provide this parameter.				
Hot Spot Overtop	25°C	0.1°C	200°C	0.1°C
Hottest spot temperature over top oil temperature setting. The transformer manufacturer should provide this parameter.				
Top Oil Overamb	55°C	0.1°C	200°C	0.1°C
Top oil temperature over ambient temperature setting. The transformer manufacturer should provide this parameter.				
Cooling Mode	Natural	Natural, Forced Air, Forced Oil, Forced Air & Oil, Select via PSL		
This setting specifies which kind of cooling mode is used to cool the transformer. If Select Via PSL then DDB inputs (650 Frcd Air Cool and 651 Frcd Oil Cool) can be used to select the cooling mode Winding exp m and oil exp n settings, as below. If DDB 650 = 1 then cooling mode is Forced Air Cooling, if DDB 651 = 1 then cooling mode is Forced Oil Cooling, if DDB 650 and 651 = 1 then cooling mode is Forced Air & Oil Cooling, if DDB 650 and 651 = 0 then cooling mode is Natural Cooling.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Cooling Status				
Cooling Status indication; it is visible only when Cooling Mode is set as 'Select via PSL'. If DDB 650 = 1 then cooling status is Forced Air Cooling, if DDB 651 = 1 then cooling status is Forced Oil Cooling, if DDB 650 and 651 = 1 then cooling status is Forced Air & Oil Cooling, if DDB 650 and 651 = 0 then cooling status is Natural Cooling.				
NATURAL COOL				
Winding exp m	0.8	0.01	2	0.01
Winding exponent constant used to calculate the ultimate hot spot rise temperature over top oil temperature. Recommended values are provided in IEEE Std. C57.91-1995 (see the Application Notes chapter for recommended values), or can be provided by the transformer manufacturer.				
Oil exp n	0.8	0.01	2	0.01
Oil exponent constant used to calculate the ultimate top oil rise temperature over ambient temperature. Recommended values are provided in IEEE Std. C57.91-1995 (see the Application Notes chapter for recommended values), or can be provided by the transformer manufacturer.				
FORCED AIR COOL				
Winding exp m	0.8	0.01	2	0.01
As described for Natural cooling.				
Oil exp n	0.8	0.01	2	0.01
As described for Natural cooling.				
FORCED OIL COOL				
Winding exp m	0.8	0.01	2	0.01
As described for Natural cooling.				
Oil exp n	0.8	0.01	2	0.01
As described for Natural cooling.				
FORCED AIR & OIL				
Winding exp m	0.8	0.01	2	0.01
As described for Natural cooling.				
Oil exp n	0.8	0.01	2	0.01
As described for Natural cooling.				
Hot spot rise co	1 min	0.01 min	20 min	0.01 min
Winding time constant setting. The transformer manufacturer should provide this parameter.				
Top oil rise co	120 min	1 min	1000 min	1 min
Oil time constant setting. The transformer manufacturer should provide this parameter.				
TOL Status	Enabled	Disabled, Enabled		
This setting enables or disables the three hot spot and the three top oil thermal stages.				
Hot Spot>1 Set	110°C	1°C	300°C	0.1°C
Hot spot first stage setting. Recommended temperature limits are given in IEEE Std. C57.91-1995. See the Application Notes chapter for recommended values.				
tHot Spot>1 Set	10 min	0 min	60000 min	0.1 min
Hot spot first stage time delay setting.				
Hot Spot>2 Set	130°C	1°C	300°C	0.1°C
Hot spot second stage setting. Recommended temperature limits are given in IEEE Std. C57.91-1995. See the Application Notes chapter for recommended values.				
tHot Spot>2 Set	10 min	0 min	60000 min	1 min
Hot spot second stage time delay setting.				
Hot Spot>3 Set	150°C	1°C	300°C	0.1°C
Hot spot third stage setting. Recommended temperature limits are given in IEEE Std. C57.91-1995. See the Application Notes chapter for recommended values.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
tHot Spot>3 Set	10 min	0 min	60000 min	1 min
Hot spot third stage time delay setting.				
Top Oil>1 Set	70°C	1°C	300°C	0.1°C
Top oil first stage setting. Recommended temperature limits are given in IEEE Std. C57.91-1995. See the Application Notes chapter for recommended values.				
tTop Oil>1 Set	10 min	0 min	60000 min	1 min
Top oil first stage time delay setting.				
Top Oil>2 Set	80°C	1°C	300°C	0.1°C
Top oil second stage setting. Recommended temperature limits are given in IEEE Std. C57.91-1995. See the Application Notes chapter for recommended values.				
tTop Oil>2 Set	10 min	0 min	60000 min	1 min
Top oil second stage time delay setting.				
Top Oil>3 Set	90°C	1°C	300°C	0.1°C
Top oil third stage setting. Recommended temperature limits are given in IEEE Std. C57.91-1995. See the Application Notes chapter for recommended values.				
tTop Oil>3 Set	10 min	0 min	60000 min	1 min
Top oil third stage time delay setting.				
tPre-trip Set	5 min	0 min	60000 min	1 min
A pre-trip alarm is given a set time before the top oil and hot spot trips using this setting, assuming that the load remains unchanged.				
LOL Status	Enabled	Disabled, Enabled		
Enables or disables the loss of life function				
Life Hours at HS	180000 hr	1 hr	300000 hr	1 hr
Life hours at the reference hottest spot temperature. Advice from the transformer manufacturer may be required.				
Designed HS temp	110°C	1°C	200°C	0.1°C
The designed hottest spot temperature is 110°C for a transformer rated 65°C average winding rise, and 95°C for a transformer rated 55°C average winding rise.				
Constant B Set	15000	1	100000	1
Constant B is associated to the life expectancy curve. It is based on modern experimental data, and it may be set to 15000 as recommended by IEEE Std. C57.91-1995.				
FAA> Set	2	0.1	30	0.01
Aging acceleration factor setting. If the aging acceleration factor calculated by the relay is above this setting and tFAA has expired, an FAA alarm would be asserted. FAA calculation depends on constant B and the hottest temperature calculated by the thermal element.				
tFAA> Set	10 min	0 min	60000 min	1 min
Aging acceleration factor timer.				
LOL>1 Set	160000 hr	1 hr	300000 hr	1 hr
Transformer loss of life setting. If the life already lost by the transformer is above this threshold, a LOL alarm would be asserted after tLOL has expired. LOL calculation depends on the life hours at design hot spot temperature and the calculated residual life.				
tLOL> Set	10 min	0 min	60000 min	1 min
Loss of life timer.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Reset Life Hours	0 hr	0 hr	300000 hr	1 hr
Resets the LOL status value to the set value when the loss of life reset command is executed. For new transformers Reset Life Hours is zero, so that when the commissioning of the thermal element is over, the loss of life statistics calculations are reset to zero. For old transformers this setting should indicate how much life the transformer has already lost; therefore, it should be set to the transformer loss of life.				

Table 9: Thermal overload protection settings

1.2.8 Generator and transformer-differential protection (87G/87GT)

The generator differential protection in the P343/4/5/6 relay may be configured to operate as either a high impedance or biased differential element. The same current inputs as used by the high impedance protection can also be used for interturn protection.

The P343/4/5/6 also includes a biased differential generator-transformer protection with two high set elements.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: DIFFERENTIAL				
Gen Diff				
Generator Diff settings are visible if SYSTEM CONFIG - Winding Type = Generator Diff				
GenDiff Func	Percentage Bias	Disabled, Percentage Bias, High Impedance, Interturn		N/A
Setting to select the function of the differential protection element.				
Gen Diff Is1	0.1 In	0.05 In	0.5 In	0.01 In
Minimum differential operating current of the low impedance biased characteristic. Also, the pick-up setting of the high impedance differential protection.				
Gen Diff k1	0%	0	20%	5%
Slope angle setting for the first slope of the low impedance biased characteristic.				
Gen Diff Is2	1.2 In A	1.0 In A	5.0 In A	0.1 In A
The bias current operating threshold for the second slope low impedance characteristic.				
Gen Diff k2	150%	20%	150%	10%
Slope angle setting for the second slope of the low impedance biased characteristic				
Interturn Is_A	0.1 In	0.05 In	2 In	0.01 In
Pick-up setting for the A phase interturn overcurrent element.				
Interturn Is_B	0.1 In	0.05 In	2 In	0.01 In
Pick-up setting for the B phase interturn overcurrent element.				
Interturn Is_C	0.1 In	0.05 In	2 In	0.01 In
Pick-up setting for the C phase interturn overcurrent element.				
Interturn ITimeDelay	0.1 s	0 s	100 s	0.01 s
Operating time-delay setting of the interturn protection.				
XFORMER DIFF				
XFORMER DIFF settings are visible if SYSTEM CONFIG - Winding Type = Xformer Diff				
Xform Diff Func	Enabled	Disabled, Enabled		
Enables or disables the transformer differential function.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: DIFFERENTIAL				
Set Mode	Simple	Simple, Advance		
If the relay is in Simple mode, zero sequence filtering (**Zero seq filt HV/LV**) is enabled automatically when the cell **HV/LV Grounding** under the **SYSTEM CONFIG** menu heading is set to grounded. If the relay is in advanced mode, the zero sequence filtering is enabled or disabled manually in the cell **Zero seq filt HV/LV** under the **DIFFERENTIAL** menu heading. Also, in the simple mode the relay calculates automatically **Xform Is-HS1** as 1/Xt, where Xt is the transformer reactance, Xt = **%Reactance** setting in the **SYSTEM CONFIG** menu. In Simple mode under the **DIFF PROTECTION** menu heading the cells **Zero seq filt HV/LV**, **Xform Is-HS1** and **Xform Is-Hs2** are Read Only.				
Xform Is1	0.2 pu	0.1 pu	2.5 pu	0.01 pu
Minimum differential threshold of the low set differential characteristic.				
Xform K1	30%	0%	150%	1%
Slope angle setting for the first slope of the low impedance biased characteristic.				
Xform Is2	1 pu	0.1 pu	10 pu	0.1 pu
Bias current threshold for the second slope of the low set differential characteristic.				
Xform K2	80%	15%	150%	1%
Slope angle setting for the second slope of the low impedance biased characteristic.				
Xform tDIFF	0 s	0 s	10 s	10 ms
Bias differential time delay				
Xform Is-CTS	1.5 pu	0.1 pu	2.5 pu	0.01 pu
In restrain mode, the differential protection Is1 setting is increased to Is-CTS setting after a CT failure is detected. The Is-CTS setting increases the restrain region of the differential characteristic.				
Xform HS1 Status	Enabled	Disabled, Enabled		
This enables or disables generator-transformer high set 1 protection.				
Xform Is-HS1	1/Xt pu	2.5 pu	16 pu	0.1 pu
High set element one. In the simple mode the relay uses the %**Reactance** in the **SYSTEM CONFIG** menu to calculate **Xform Is-HS1** as 1/Xt. Where Xt is the transformer reactance. This setting is Read Only in simple mode. In advance mode **Xform Is-HS1** is visible and settable. The high set 1 algorithm uses a peak detection method to achieve fast operating times. Above the adjustable differential current threshold **Xform Is-HS1**, the P34x will trip without taking into account either the second or fifth harmonic blocking but the bias current is considered.				
Xform Is-HS2	16 pu	2.5 pu	16 pu	0.1 pu
High set element two. This element is settable and visible in advance mode. In simple mode, it is Read Only and set to 16 pu. The Is-HS2 element uses the fundamental component of the differential current. This element is not restrained by the bias characteristic, so the P34x will trip regardless of the restraining current. Above the adjustable differential current threshold **Xform Is-HS2**, the P34x will trip without taking into account either the second or fifth harmonic blocking or the bias current.				
Zero seq filt HV	Disabled	Disabled, Enabled		
Enables or disables zero sequence filtering on the HV winding. This setting is only visible and settable in advance mode.				
Zero seq filt LV	Disabled	Disabled, Enabled		
Enables or disables zero sequence filtering on the LV winding. This setting is only visible and settable in advance mode.				
2nd harm blocked	Enabled	Disabled, Enabled		
Enables or disables 2nd harmonic blocking.				
Xform Ih(2)%>	20%	5%	50%	1%
Second harmonic blocking threshold.				

ST

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: DIFFERENTIAL				
Cross blocking	Disabled	Disabled, Enabled		
Enables or disables cross blocking. Second harmonic blocking is enabled across all three phases if cross blocking is selected and the second harmonic blocking threshold is exceeded in any phase.				
5th harm blocked	Disabled	Disabled, Enabled		
Enables or disables 5th harmonic blocking.				
Xform Ih(5)%>	35%	0%	100%	1%
Fifth harmonic blocking threshold. Fifth harmonic blocking is per phase, no cross blocking is available.				
Circuitry Fail	Enabled	Disabled, Enabled		
Enables or disables the circuitry fail alarm.				
Is-cctfail	0.1 pu	0.03 pu	1 pu	0.01 pu
Minimum differential threshold of the circuitry fail alarm.				
K-cctfail	10%	0 s	50%	1%
Slope angle setting for the circuitry fail alarm function.				
cctFail Delay	5 s	0 s	10 s	0.1 s
Circuitry fail alarm time delay.				

Table 10: Generator protection and generator-transformer differential settings

1.2.9 Earth fault (50N/51N)

The earth fault protection included in the P342/3/4/5/6 relay provides two stage non-directional earth fault protection. The first stage of earth fault protection has time-delayed characteristics which are selectable between inverse definite minimum time (IDMT), or definite time (DT) or a user curve (Default Curve 1/2/3/4). The second stage has a definite time characteristic only.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: EARTH FAULT				
IN1>1 Function	IEC S Inverse	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, IDG, Default Curve 1/2/3/4		
Tripping characteristic for the first stage earth fault protection.				
IN1>1 Current Set	0.1 In	0.02 In	4.0 In	0.01 In
Pick-up setting for the first stage earth fault protection.				
IN1>1 IDG Is	1.5	1	4	0.1
Multiple of "IN>" setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts.				
IN1>1 Time Delay	1 s	0 s	200 s	0.01 s
Operating time-delay setting for the first stage definite time element.				
IN1>1 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
IN1>1 Time Dial	1	0.01	100	0.1
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves and user programmable curves.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
IN1>1 K (RI)	1	0.1	10	0.05
Time multiplier to adjust the operating time for the RI curve.				
IN1>1 IDG Time	1.2	1	2	0.01
Minimum operating time at high levels of fault current for IDG curve.				
IN1>1 Reset Char	DT	DT or Inverse		N/A
Type of reset/release characteristic of the IEEE/US curves.				
IN>1 UsrRst Char	DT	DT, Default Curve 1/2/3/4		N/A
Type of reset/release characteristic of the user curves.				
IN1>1 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
IN1>2 Function	Disabled	Disabled, Enabled		N/A
Enables or disables the second stage definite time earth fault protection.				
IN1>2 Current	0.45 In	0.02 In	10 In	0.01 In
Pick-up setting for second stage earth fault protection.				
IN1>2 Time Delay	0 s	0 s	200 s	0.01 s
Operating time delay setting for the second stage earth fault protection.				

Table 11: Earth fault protection settings

1.2.10 Rotor earth fault (64R)

Rotor earth fault protection is provided by the P391 low frequency square wave injection, coupling and measurement unit connected to the rotor circuit. The measurement of the rotor resistance is passed to the P342/3/4/5/6 via a current loop output (0-20 mA) on the P391 connected to one of the 4 current loop inputs on the P342/3/4/5/6. The rotor ground fault protection is only available if the relay includes the CLIO hardware option.

The rotor earth fault protection in the P342/3/4/5/6 includes 2 stages of under resistance protection. The under resistance protection is designed as a two stage protection system, one alarm stage (64R R<1) and one trip stage (64R R<2), with each stage having a definite time delay setting. The injection frequency is selectable 0.25/0.5/1 Hz via a jumper link in the P391.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: ROTOR EF				
Injection Freq	1 Hz	0.25 Hz, 0.5 Hz, 1 Hz		N/A
Injection frequency. Must be equal to injection frequency set on P391.				
CL I/P Select	CL1	CL1, CL2, CL3, CL4		N/A
Current Loop Input used for the rotor earth fault protection.				
64R R<1 Alarm	Enabled	Disabled, Enabled		N/A
Enables or disables the first stage under resistance element.				
64R R<1 Alm Set	40,000 Ω	1000 Ω	80000 Ω	1 Ω
Pick-up setting for the first stage under resistance element.				
64R R<1 Alm Dly	10 s	0 s	600 s	0. 1 s
Operating time-delay setting of the first stage under resistance element.				
64R R<2 Trip	Enabled	Disabled, Enabled		N/A
Enables or disables the second stage under resistance trip element.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: ROTOR EF				
64R R<2 Trip Set	5000 Ω	1000 Ω	80000 Ω	1 Ω
Pick-up setting for the second stage under resistance element.				
64S R<2 Trip Dly	1 s	0 s	600 s	0. 1 s
Operating time-delay setting of the second stage under resistance trip element.				
R Compensation	0 Ω	-1000 Ω	1000 Ω	1 Ω
Resistance compensation setting.				

Table 12: Rotor earth fault protection settings

1.2.11 Sensitive earth fault/restricted earth fault (50N/51N/67N/67W/64)

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If a system is earthed through a high impedance, or is subject to high ground fault resistance, the earth fault level will be severely limited. Consequently, the applied earth fault protection requires both an appropriate characteristic and a suitably sensitive setting range in order to be effective. A separate single stage sensitive earth fault element is provided within the P342/3/4/5/6 relay for this purpose, which has a dedicated input. This input may be configured to be used as a REF input. The REF protection in the P342/3/4/5/6 relay may be configured to operate as either a high impedance or biased element.

Note: The high impedance REF element of the relay shares the same sensitive current input as the SEF protection and sensitive power protection. Hence, only one of these elements may be selected. However, the low impedance REF element does not use the SEF input and so may be selected at the same time.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: SEF/REF PROT'N				
SEF/REF Options	SEF	SEF, SEF cos (PHI), SEF sin (PHI), Wattmetric, Hi Z REF, Lo Z REF, Lo Z REF + SEF, Lo Z REF + Wattmet		
Setting to select the type of sensitive earth fault protection function and the type of high-impedance function to be used. If the function is not selected, then all associated settings and signals are hidden, with the exception of this setting.				
ISEF>1 Function	DT	Disabled, DT		
Tripping characteristic for the first stage sensitive earth fault protection.				
ISEF>1 Direction	Non-directional	Non-directional Direction Fwd Direction Rev		N/A
Direction of the first stage sensitive earth fault protection.				
ISEF>1 Current	0.05 In	0.005 In	0.1 In	0.00025 In
Pick-up setting for the first stage sensitive earth fault protection.				
ISEF>1 Delay	1 s	0 s	200 s	0.01 s
Operating time delay setting for the first stage sensitive earth fault protection.				
ISEF> Func. Link	00000001	Bit 0 = VTS Blocks ISEF>1, Bits 1 - 7 are not used.		
Setting that determines whether VT supervision logic signals blocks the sensitive earth fault stage. With the relevant bit set to 1, operation of the Voltage Transformer Supervision (VTS), will block the stage. When set to 0, the stage will revert to Non-directional upon operation of the VTS.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
ISEF DIRECTIONAL	Sub-heading in menu			
ISEF> Char. Angle	90°	–95°	+95°	1°
Relay characteristic angle setting used for the directional decision.				
ISEF> VNpol Input	Measured	Measured, Derived		
Residual/neutral voltage (Zero sequence) polarization source.				
ISEF>VNpol Set	5 V (Vn=100/120 V) 20 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)	80 V (Vn=100/120 V) 320 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Minimum zero sequence voltage polarizing quantity required for directional decision.				
WATTMETRIC SEF	Sub-heading in menu			
PN> Setting	9 In W (Vn=100/120 V) 36 In W (Vn=380/480 V)	0 W	20 In W (Vn=100/120 V) 80 In W (Vn=380/480 V)	0.05 In W (Vn=100/120 V) 0.2 In W (Vn=380/480 V)
Setting of the threshold for the wattmetric component of zero sequence power. The power calculation is as follows: The PN> setting corresponds to: Vres x Ires x Cos (ϕ – ϕc) = 9 x Vo x Io x Cos (ϕ– ϕc) Where; ϕ = Angle between the Polarizing Voltage (-Vres) and the Residual Current ϕc = Relay Characteristic Angle (RCA) Setting (ISEF> Char Angle) Vres = Residual Voltage Ires = Residual Current Vo = Zero Sequence Voltage Io = Zero Sequence Current				
RESTRICTED E/F	Sub-heading in menu			
IREF> CT Source	IA-1 IB-1 IC-1	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		
This setting is used to select the 3 phase current inputs used by the **Restricted Earth Fault** protection in the P343/4/5/6 - IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 CT inputs.				
IREF>k1	0%	0%	20%	1%
Slope angle setting for the first slope of the low impedance biased characteristic.				
IREF>k2	150%	0%	150%	1%
Slope angle setting for the second slope of the low impedance biased characteristic.				
IREF>Is1	0.2 In	0.05 In	1 In	0.01 In
Minimum differential operating current for the low impedance characteristic.				
IREF>Is2	1 In	0.1 In	1.5 In	0.01 In
Bias current operating threshold for the second slope low impedance characteristics.				

Table 13: Sensitive earth fault protection settings

For the Hi Z REF option, the following settings are available:

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
RESTRICTED E/F	Sub-heading in menu			
IREF> Is	0.2 In	0.05 In	1.0 In	0.01 In
Pick-up setting for the high impedance REF protection.				

Table 14: Restricted earth fault protection settings

1.2.12 Residual overvoltage (neutral voltage displacement) (59N)

The derived neutral voltage displacement (NVD) elements (VN>1/2) (P342/3/4/5/6/8) and the measured NVD elements from the VN1 input (VN>3/4) (P342/3/4/5/6) and the VN2 input (VN>5/6) (P344/6) are of two-stage design, each stage having separate voltage and time delay settings. All Stages may be set to operate on either an IDMT or DT or a user curve characteristic. In the P342-6 the neutral voltage is derived or measured from the stator VTs and is used to provide stator earth fault protection. In the P348 the neutral voltage is derived from the rotor VTs and is used to provide rotor earth fault protection.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
RESIDUAL O/V NVD: GROUP 1				
VN>1 Status	Enabled	Disabled, Enabled		
Enables or disables the VN>1 trip stage (P342/3/4/5/6/8).				
VN>1 Input	Derived	N/A		N/A
VN>1 uses derived neutral voltage from the 3 phase stator voltage input (VN = VA+VB+VC) (P342-6). VN>1 uses derived neutral RMS voltage from the 3 phase rotor voltage input (VN = VA RMS + VB RMS + VC RMS) (P348).				
VN>1 Function	DT	DT, IDMT, Default Curve 1/2/3/4		N/A
Tripping characteristic setting of the first stage residual overvoltage element.				
VN>1 Voltage Set	5 V (P342-8) (Vn=100/120 V) 20 V (P342-6) (Vn=380/480 V)	1 V (P342-8) (Vn=100/120 V) 4 V (P342-6) (Vn=380/480 V)	80 V (P342-8) (Vn=100/120 V) 320 V (P342-6) (Vn=380/480 V)	1 V (P342-8) (Vn=100/120 V) 4 V (P342-6) (Vn=380/480 V)
Pick-up setting for the first stage residual overvoltage characteristic.				
VN>1 Time Delay	5 s	0 s	100 s	0.01 s
Operating time delay setting for the first stage definite time residual overvoltage element.				
VN>1 TMS	1	0.5	100	0.5
Setting for the time multiplier setting to adjust the operating time of the IDMT characteristic. The characteristic is defined as follows: t = K / (M – 1) where: K = Time multiplier setting t = Operating time in seconds M = Derived residual voltage/relay setting voltage (VN> Voltage Set)				
VN>1 tReset	0 s	0 s	100 s	0.01 s
Reset/release definite time setting for the first stage characteristic.				
VN>2 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the second stage residual overvoltage element (P342/3/4/5/6/8).				
VN>2 Input	Derived	N/A		N/A
VN>2 uses derived neutral voltage from the 3 phase stator voltage input (VN = VA+VB+VC) (P342-6). VN>2 uses derived neutral RMS voltage from the 3 phase rotor voltage input (VN = VA RMS + VB RMS + VC RMS) (P348).				
VN>2 Function	DT	DT, IDMT, Default Curve 1/2/3/4		N/A
Tripping characteristic setting of the first stage residual overvoltage element.				
VN>2 Voltage Set	10 V (P342-8) (Vn=100/120 V) 40 V (P342-6) (Vn=380/480 V)	1 V (P342-8) (Vn=100/120 V) 4 V (P342-6) (Vn=380/480 V)	80 V (P342-8) (Vn=100/120 V) 320 V (P342-6) (Vn=380/480 V)	1V (P342-8) (Vn=100/120 V) 4 V (P342-6) (Vn=380/480 V)
Pick-up setting for the first stage residual overvoltage characteristic.				
VN>2 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay setting for the first stage definite time residual overvoltage element.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VN>2 TMS	1	0.5	100	0.5
Time multiplier setting to adjust the operating time of the IDMT characteristic. The characteristic is defined as above				
VN>2 tReset	0 s	0 s	100 s	0.01 s
Reset/release definite time setting for the first stage characteristic.				
VN>3 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the third stage residual overvoltage element (P342/3/4/5/6).				
VN>3 Input	VN1	N/A		N/A
VN>3 uses measured neutral voltage from the Vneutral/VN1 input.				
VN>3 cells as for VN>1 above				
VN>4 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the fourth stage residual overvoltage element (P342/3/4/5/6).				
VN>4 Input	VN1	N/A		N/A
VN>4 uses measured neutral voltage from the Vneutral/VN1 input.				
VN>4 cells as for VN>2 above				
VN>5 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the fifth stage residual overvoltage element. (P344, 5 only).				
VN>5 Input	VN2	N/A		N/A
VN>5 uses measured neutral voltage from the VN2 input.				
VN>5 cells as for VN>1 above				
VN>6 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the sixth stage residual overvoltage element. (P344, 5 only).				
VN>6 Input	VN1	N/A		N/A
VN>6 uses measured neutral voltage from the VN2 input.				
VN>6 cells as for VN>2 above				

Table 15: Residual overvoltage protection settings

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1.2.13 100% stator earth fault (27TN/59TN/64S)

100% stator earth fault protection via third harmonic voltage measurement is available in the P343/4/5. A 3rd harmonic undervoltage protection element is included. This element is supervised by a 3 phase undervoltage element to prevent maloperation when running up/down the generator. Additional three phase active, reactive and apparent power supervision elements can also be enabled for this element. A third harmonic neutral over voltage protection is also provided. Each element has a definite time delay setting.

The 100% stator earth fault protection via low frequency injection is only available in the P345. It includes 2 stages of under resistance protection and an overcurrent protection stage. The under resistance protection is designed as a two stage protection system, one alarm stage (64S R<1 Alarm) and one trip stage (64S R<2 Trip), with each stage having a definite time delay setting. The overcurrent stage (64S I> Trip) is a single protection stage with a definite time delay setting. The protection includes a supervision element to evaluate a failure of the low frequency generator or the low frequency connection. The operation of an undervoltage and an undercurrent element after a time delay are used to indicate a failure. In case of a failure the protection is blocked and an alarm given.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: 100% STATOR EF				
VN 3rd Harmonic	VN3H< Enabled	Disabled, VN3H< Enabled, VN3H> Enabled		N/A
Operating mode of the 3rd harmonic 100% stator earth fault protection defining – disabled or 3rd harmonic undervoltage or 3rd harmonic overvoltage. (P343, 4, 5 only).				
100% St. EF VN3H<	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)	0.1 V (Vn=100/120 V) 0.4 V (Vn=380/480 V)	20 V (Vn=100/120 V) 80 V (Vn=380/480 V)	0.1 V (Vn=100/120 V) 0.4 V (Vn=380/480 V)
Pick-up setting for the 3rd harmonic undervoltage protection element.				
VN3H< Delay	5 s	0 s	100 s	0.01 s
Operating time-delay setting of the 3rd harmonic undervoltage protection.				
V<Inhibit Set	80 V (Vn=100/120 V) 320 V (Vn=380/480 V)	30 V (Vn=100/120 V) 120 V (Vn=380/480 V)	120 V (Vn=100/120 V) 480 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)
Pick-up setting for undervoltage inhibit of the 3rd harmonic 100% stator earth fault protection.				
P<Inhibit	Disabled	Disabled, Enabled		N/A
Enables or disables the power (W) inhibit of the 3rd harmonic 100% stator earth fault protection.				
P<Inhibit Set	4 x In W (Vn=100/120 V) 16 x In W (Vn=380/480 V)	4 x In W (Vn=100/120 V) 16 x In W (Vn=380/480 V)	200 x In W (Vn=100/120 V) 800 x In W (Vn=380/480 V)	0.5 x In W (Vn=100/120 V) 2 x In W (Vn=380/480 V)
Pick-up setting for the power (W) inhibit of the 3rd harmonic 100% stator earth fault protection.				
Q<Inhibit	Disabled	Disabled, Enabled		N/A
Enables or disables the reactive power (VAr) inhibit of the 3rd harmonic 100% stator earth fault protection.				
Q<Inhibit Set	4 x In W (Vn=100/120 V) 16 x In W (Vn=380/480 V)	4 x In W (Vn=100/120 V) 16 x In W (Vn=380/480 V)	200 x In W (Vn=100/120 V) 800 x In W (Vn=380/480 V)	0.5 x In W (Vn=100/120 V) 2 x In W (Vn=380/480 V)
Pick-up setting for the reactive power (VAr) inhibit of the 3rd harmonic 100% stator earth fault protection.				
S<Inhibit	Disabled	Disabled, Enabled		N/A
Enables or disables the apparent power (VA) inhibit of the 3rd harmonic 100% stator earth fault protection.				
S<Inhibit Set	4 x In W (Vn=100/120 V) 16 x In W (Vn=380/480 V)	4 x In W (Vn=100/120 V) 16 x In W (Vn=380/480 V)	200 x In W (Vn=100/120 V) 800 x In W (Vn=380/480 V)	0.5 x In W (Vn=100/120 V) 2 x In W (Vn=380/480 V)
Pick-up setting for the apparent power (VA) inhibit of the 3rd harmonic 100% stator earth fault protection.				
100% St. EF VN3H>	20 V (Vn=100/120 V) 4 V (Vn=380/480V)	0.1 V (Vn=100/120 V) 0.4 V (Vn=380/480 V)	20 V (Vn=100/120 V) 80 V (Vn=380/480 V)	0.1 V (Vn=100/120 V) 0.4 V (Vn=380/480 V)
Pick-up setting for the 3rd harmonic overvoltage protection element.				
VN3H> Delay	5 s	0 s	100 s	0.01 s
Operating time-delay setting of the 3rd harmonic overvoltage protection.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: 100% STATOR EF				
64S LF Injection	Disabled	Disabled, Enabled		N/A
Enables or disables the low frequency injection 100% stator earth fault protection (64S). (P345 only)				
64S R Factor	10	0.01	200	0.1
R factor setting, defines the primary to secondary ratio factor for the resistance, reactance and conductance, R Primary = R Secondary x R Factor.				
64S R<1 Alarm	Enabled	Disabled, Enabled		N/A
Enables or disables the 64S first stage under resistance alarm element.				
64S R<1 Alm Set	100 Ω	10 Ω	700 Ω	0.1 Ω
Pick-up setting for the 64S first stage under resistance element with 64S R Factor = 1.				
64S R<1 Alm Dly	1 s	0 s	100 s	0.01 s
Operating time-delay setting of the 64S first stage under resistance alarm element.				
64S R<2 Trip	Enabled	Disabled, Enabled		N/A
Enables or disables the 64S second stage under resistance trip element with 64S R Factor = 1.				
64S R<2 Trip Set	20 Ω	10 Ω	700 Ω	0.1 Ω
Pick-up setting for the 64S second stage under resistance trip element.				
64S R<1 Trip Dly	1 s	0 s	100 s	0.01 s
Operating time-delay setting of the 64S second stage under resistance trip element.				
64S Angle Comp	0°	-60°	60°	0.1°
64S Angle compensation setting.				
64S Series R	0	0Ω	700Ω	0.1Ω
64S series resistance setting with 64S R Factor = 1.				
64S Parallel G	0	0S	0.1S	0.0000001S
64S parallel conductance setting with 64S R Factor = 1.				
64S Overcurrent	Enabled	Disabled, Enabled		N/A
Enables or disables the 64S overcurrent trip element.				
64S I>1 Trip Set	0.5A	0.02A	1.5A	0.01A
Pick-up setting for the 64S overcurrent trip element.				
64S I>1 Trip Dly	1s	0 s	100 s	0.01 s
Operating time-delay setting of the 64S overcurrent trip element.				
64S Supervision	Enabled	Disabled, Enabled		N/A
Enables or disables the 64S supervision element.				
64S V<1 Set	1V	0.3 V	25 V	0.1 V
Pick-up setting for the 64S supervision undervoltage element.				
64S I<1 Set	10 mA	5 mA	40 mA	1 mA
Pick-up setting for the 64S supervision undercurrent element.				
64S Superv'n Dly	1 s	0 s	100 s	0.01 s
Operating time-delay setting of the 64S supervision element.				

Table 16: 100% stator earth protection settings

1.2.14 Overfluxing, V/Hz (24)

The P342/3/4/5/6 relays provide a five stage overfluxing element. The element measures the ratio of voltage, (VAB), to frequency (V/Hz) and will operate when this ratio exceeds the setting. One stage can be set to operate with a definite time or inverse time delay (IDMT), or a user curve, this stage can be used to provide the protection trip output. There are also 3 other definite time stages which can be combined with the inverse time characteristic to create a combined multi-stage V/Hz trip operating characteristic using PSL. An inhibit signal is provided for the V/Hz>1 stage 1 only, which has the inverse time characteristic option. This allows a definite time stage to override a section of the inverse time characteristic if required. The inhibit has the effect of resetting the timer, the start signal and the trip signal.

There is also one definite time alarm stage.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: VOLTS/HZ				
V/Hz Alarm Status	Enabled	Disabled, Enabled		N/A
Enable or disables the V/Hz alarm element.				
V/Hz Alarm Set	2.31 V/Hz (Vn=100/120 V) 9.24 V/Hz (Vn=380/480 V)	1.5 V/Hz (Vn=100/120 V) 6 V/Hz (Vn=380/480 V)	3.5 V/Hz (Vn=100/120 V) 14 V/Hz (Vn=380/480 V)	0.01 V/Hz (Vn=100/120 V) 0.04 V/Hz (Vn=380/480 V)
Pick-up setting for the V/Hz alarm element.				
V/Hz Alarm Delay	0 s	0 s	100 s	0.01 s
Operating time-delay setting of the V/Hz alarm element.				
V/Hz>1 Status	Enabled	Disabled, Enabled		
Enables or disables the V/Hz first stage trip element.				
V/Hz>1 Trip Func.	DT	DT, IDMT, Default Curve 1/2/3/4		
Tripping characteristic setting of the V/Hz first stage trip element.				
V/Hz>1 Trip Set	2.42 V/Hz (Vn=100/120 V) 9.24 V/Hz (Vn=380/480 V)	1.5 V/Hz (Vn=100/120 V) 6 V/Hz (Vn=380/480 V)	3.5 V/Hz (Vn=100/120 V) 14 V/Hz (Vn=380/480 V)	0.01 V/Hz (Vn=100/120 V) 0.04 V/Hz (Vn=380/480 V)
Pick-up setting for the V/Hz first stage trip element.				
V/Hz>1 Trip TMS	1	0.01	12	0.01
Setting for the time multiplier setting to adjust the operating time of the IDMT characteristic. The characteristic is defined as follows: $t = \frac{TMS}{(M - 1)^2}$ Where: $M = \frac{V/f}{(V/f\ Trip\ Setting)}$ V = Measured voltage F = Measured frequency				
V/Hz>1 Delay	60 s	0 s	600 s	0.01 s
Operating time-delay setting of the V/Hz first stage trip element.				
V/Hz>1 Reset Char	DT	DT, Default Curve 1/2/3/4		
Type of reset/release characteristic of the user curves.				
V/Hz>1 tReset	0 s	0 s	600 s	0.01 s
Reset/release time setting for definite time reset characteristic.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
V/Hz>2 Trip Status	Enabled	Disabled, Enabled		N/A
Enables or disables the V/Hz second stage trip element.				
V/Hz>2 Trip Set	2.64 V/Hz (Vn=100/120 V) 10.56 V/Hz (Vn=380/480 V)	1.5 V/Hz (Vn=100/120 V) 6 V/Hz (Vn=380/480 V)	3.5 V/Hz (Vn=100/120 V) 14 V/Hz (Vn=380/480 V)	V/Hz (Vn=100/120 V) 0.04 V/Hz (Vn=380/480 V)
Pick-up setting for the V/Hz second stage trip element.				
V/Hz>1 Trip Delay	60 s	0 s	600 s	0.01 s
Operating time-delay setting of the V/Hz second stage trip element.				
V/Hz>3 Trip Status	Enabled	Disabled, Enabled		N/A
Enables or disables the V/Hz third stage trip element.				
V/Hz>3 Trip Set	2.86 V/Hz (Vn=100/120 V) 11.44 V/Hz (Vn=380/480 V)	1.5 V/Hz (Vn=100/120 V) 6 V/Hz (Vn=380/480 V)	3.5 V/Hz (Vn=100/120 V) 14 V/Hz (Vn=380/480 V)	0.01 V/Hz (Vn=100/120V) 0.04 V/Hz (Vn=380/480 V)
Pick-up setting for the V/Hz fourth stage trip element.				
V/Hz>3 Trip Delay	2 s	0 s	600 s	0.01 s
Operating time-delay setting of the V/Hz third stage trip element.				
V/Hz>4 Trip Status	Enabled	Disabled, Enabled		N/A
Enables or disables the V/Hz fourth stage trip element.				
V/Hz>4 Trip Set	3.08 V/Hz (Vn=100/120 V) 12.32 V/Hz (Vn=380/480 V)	1.5 V/Hz (Vn=100/120 V) 6 V/Hz (Vn=380/480 V)	3.5 V/Hz (Vn=100/120 V) 14 V/Hz (Vn=380/480 V)	V/Hz (Vn=100/120 V) 0.04 V/Hz (Vn=380/480 V)
Pick-up setting for the V/Hz fourth stage trip element.				
V/Hz>4 Trip Delay	1 s	0 s	600 s	0.01 s
Operating time-delay setting of the V/Hz fourth stage trip element.				

Table 17: Overfluxing protection settings

1.2.15 Rate of change of frequency protection (81R)

The P342/3/4/5/6 provides four independent stages of rate of change of frequency protection (df/dt+t). Depending on whether the rate of change of frequency setting is set positive or negative, the element will react to rising or falling frequency conditions respectively, with an incorrect setting being indicated if the threshold is set to zero.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: DF/DT				
Operating Mode	Rolling Window	Fixed Window/ Rolling Window		
Selects the algorithm method, Fixed or Rolling Window, used for df/dt calculation.				
df/dt Avg. Cycles	3	2	12	1
Sets the number of power system cycles that are used to average the rate of change of frequency measurement.				
df/dt Iterations	2	1	4	1
Sets the number of iterations of the df/dt protection element to obtain a start signal. For example if **Operating Mode** is **Fixed Window** and **df/dt Avg Cycles** = 3 and **df/dt Iterations** =2 then df/dt start will be after 2 consecutive 3 cycle windows above setting.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
df/dt>1 Status	Enabled	Disabled, Enabled		
Setting to enable or disable the first stage df/dt element.				
df/dt>1 Setting	0.2 Hz/s	100.0 mHz/s	10 Hz/s	10 mHz/s
Pick-up setting for the first stage df/dt element.				
df/dt>1 Dir'n.	Both	Negative/Positive/Both		N/A
This setting determines whether the element will react to rising or falling frequency conditions respectively, with an incorrect setting being indicated if the threshold is set to zero.				
df/dt>1 Time	0.5 s	0 s	100 s	0.01 s
Operating time-delay setting for the first stage df/dt element.				
df/dt>1 f L/H	Enabled	Disabled, Enabled		
Enables or disables the low and high frequency block function for the first stage of df/dt protection. The df/dt>1 stage is blocked if the frequency is in the deadband defined by the df/dt>1 F Low and df/dt>1 F High setting. This is typically required for loss of grid applications.				
df/dt>1 f Low	49.5 Hz	45 Hz	65 Hz	0.01 Hz
Setting for the df/dt>1 low frequency blocking.				
df/dt>1 f High	50.5 Hz	45 Hz	65 Hz	0.01 Hz
Setting for the df/dt>1 high frequency blocking.				
df/dt>2 Status	Enabled	Disabled, Enabled		
Setting to enable or disable the first stage df/dt element.				
df/dt>2 Setting	0.2 Hz/s	100.0 mHz/s	10 Hz/s	10 mHz/s
Pick-up setting for the first stage df/dt element.				
df/dt>2 Dir'n.	Positive	Negative, Positive, Both		N/A
This setting determines whether the element will react to rising or falling frequency conditions respectively.				
df/dt>2 Time	0.5 s	0 s	100 s	0.01 s
Operating time-delay setting for the second stage df/dt element.				
df/dt>3/4 Cells as for df/dt>2 Above				

Table 18: df/dt protection settings

1.2.16 Dead machine/unintentional energization at standstill (50/27)

The P342/3/4/5 relays provides dead machine protection. The dead machine protection consists on an undervoltage element which ensures the protection is enabled when the machine is not running or dead and an overcurrent element to detect when the generator CB has been unintentionally closed. The protection has a definite time delay to prevent operation during system faults and a delay on drop off timer to ensure that the protection remains operated following accidental closure of the CB when the undervoltage element could reset.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: DEAD MACHINE				
DM CT Source	IA-1 IB-1 IC-1	IA-1 IB-1 IC-1, IA-2 IB-2 IC-2		
This setting is used to select the 3 phase current inputs used by the **Dead Machine** protection in the P343/4/5 - IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 CT inputs.				
Dead Mach. Status	Enabled	Disabled, Enabled		N/A
Enables or disables the dead machine element.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Dead Mach. I>	0.1 In A	0.08 In A	4 In A	0.01 In A
Pick-up setting for the dead machine overcurrent element.				
Dead Mach. V<	80 V (Vn=100/120 V) 320 V (Vn=380/480 V)	10 V (Vn=100/120 V) 40 V (Vn=380/480 V)	120 V (Vn=100/120 V) 480 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)
Pick-up setting for the dead machine undervoltage element.				
Dead Mach. tPU	5 s	0 s	10 s	0.1 s
Operating time delay setting for the dead machine element.				
Dead Mach. tDO	0 s	0 s	10 s	0.1 s
Drop-off time-delay setting for the dead machine element.				

Table 19: Dead machine protection settings

1.2.17 Voltage protection (27/59/47)

The undervoltage and overvoltage protection included within the P342/3/4/5/6 relay consists of two independent stages of overvoltage and three stages of undervoltage. The stages are included to provide both alarm and trip stages, where required. These are configurable as either phase to phase or phase to neutral measuring. The undervoltage stages may be optionally blocked by a pole dead (CB Open) condition.

The first stage of under/overvoltage protection has a time-delayed characteristics which is selectable between inverse definite minimum time (IDMT), or definite time (DT) or a user curve (Default Curve 1/2/3/4). The second stage overvoltage and second and third stage undervoltage are definite time only.

Negative phase sequence overvoltage protection is also included with a definite time delay.

The overvoltage protection included within the P348 relay consists of two independent stages of RMS and two independent stages of peak (sampled values) overvoltage protection. Each peak overvoltage stage has a setting for the number of samples required above setting to start.

Two RMS and peak stages are included to provide both alarm and trip stages, where required. These are configurable as either phase to phase or phase to neutral measuring.

The first stage RMS and peak overvoltage protection has a time-delayed characteristic which is selectable between inverse definite minimum time (IDMT), or definite time (DT) or a user curve. The second stage RMS and peak overvoltage is definite time only.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: VOLT PROTECTION				
UNDERVOLTAGE	Sub-heading			
V< Measur't. Mode	Phase-Phase	Phase to Phase Phase to Neutral		N/A
Sets the measured input voltage, phase-phase or phase-neutral that will be used for the undervoltage elements.				
V< Operate Mode	Any Phase	Any Phase Three Phase		N/A
Setting that determines whether any phase or all three phases has to satisfy the undervoltage criteria before a decision is made.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
V<1 Function	DT	Disabled DT IDMT Default Curve 1/2/3/4		N/A
Tripping characteristic for the first stage undervoltage function. The IDMT characteristic available on the first stage is defined by the following formula: t = K / (1 - M) Where: K = Time multiplier setting t = Operating time in seconds M = Measured voltage/relay setting voltage (V< Voltage Set)				
V<1 Voltage Set	50 V (Vn=100/120 V) 200 V (Vn=380/480 V)	10 V (Vn=100/120 V) 40 V (Vn=380/480 V)	120 V (Vn=100/120 V) 480 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)
Pick-up setting for first stage undervoltage element.				
V<1 Time Delay	10 s	0 s	100 s	0.01 s
Operating time-delay setting for the first stage definite time undervoltage element.				
V<1 TMS	1	0.5	100	0.5
Time multiplier setting to adjust the operating time of the IDMT characteristic.				
V<1 Poledead Inh	Enabled	Disabled, Enabled		N/A
If the setting is enabled, the relevant stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the undervoltage protection to reset when the circuit breaker opens to cater for line or bus side VT applications				
V<2 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the second stage undervoltage element.				
V<2 Voltage Set	38 V (Vn=100/120 V) 152 V (Vn=380/480 V)	10 V (Vn=100/120 V) 40 V (Vn=380/480 V)	120 V (Vn=100/120 V) 480 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)
Pick-up setting for second stage undervoltage element.				
V<2 Time Delay	5 s	0 s	100 s	0.01 s
Operating time-delay setting for the second stage definite time undervoltage element.				
V<2 Poledead Inh	Enabled	Enabled Disabled		N/A
If the setting is enabled, the relevant stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the undervoltage protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
V<3 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the third stage undervoltage element.				
V<3 Voltage Set	38 V (Vn=100/120 V) 152 V (Vn=380/480 V)	10 V (Vn=100/120 V) 40 V (Vn=380/480 V)	120 V (Vn=100/120 V) 480 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)
Pick-up setting for third stage undervoltage element.				
V<3 Time Delay	5 s	0 s	100 s	0.01 s
Operating time-delay setting for the third stage definite time undervoltage element.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
V<3 Poledead Inh	Enabled	Enabled Disabled		N/A
If the setting is enabled, the relevant stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the undervoltage protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
OVERVOLTAGE	Sub-heading			
V> Measur't. Mode	Phase-Phase	Phase to Phase Phase to Neutral		N/A
Sets the measured input voltage, phase-phase or phase-neutral that will be used for the overvoltage elements.				
V> Operate Mode	Any Phase	Any Phase Three Phase		N/A
Setting that determines whether any phase or all three phases has to satisfy the overvoltage criteria before a decision is made.				
V>1 Function	DT	Disabled DT IDMT Default Curve 1/2/3/4		N/A
Tripping characteristic setting for the first stage overvoltage element. The IDMT characteristic available on the first stage is defined by the following formula: t = K / (M - 1) Where: K = Time multiplier setting t = Operating time in seconds M = Measured voltage/relay setting voltage (V<>Voltage Set)				
V>1 Voltage Set	130 V (Vn=100/120 V) 520 V (Vn=380/480 V)	60 V (Vn=100/120 V) 240 V (Vn=380/480 V)	185 V (Vn=100/120 V) 740 V (Vn=380/480 V)	1V (Vn=100/120 V) 4 V (Vn=380/480 V)
Pick-up setting for first stage overvoltage element.				
V>1 Time Delay	10 s	0 s	100 s	0.01 s
Operating time-delay setting for the first stage definite time overvoltage element.				
V>1 TMS	1	0.5	100	0.5
Time multiplier setting to adjust the operating time of the IDMT characteristic.				
V>2 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the second stage overvoltage element.				
V>2 Voltage Set	150 V (Vn=100/120 V) 600 V (Vn=380/480 V)	60 V (Vn=100/120 V) 240 V (Vn=380/480 V)	185 V (Vn=100/120 V) 740 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)
Pick-up setting for the second stage overvoltage element.				
V>2 Time Delay	0.5 s	0 s	100 s	0.01 s
Operating time-delay setting for the second stage definite time overvoltage element.				
NPS OVERVOLTAGE	Sub-heading			
V2>1 status	Enabled	Disabled, Enabled		N/A
Enables or disables the definite time negative sequence overvoltage element.				
V2>1 Voltage Set	15 V (Vn=100/120 V) 60 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)	150 V (Vn=100/120 V) 600 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Pick-up setting for the negative sequence overvoltage element.				
V2>1 Time Delay	1 s	0 s	100 s	0.01 s
Operating time delay setting for the definite time negative sequence overvoltage element.				
OVERVOLTAGE	Sub-heading (P348 settings are shown below)			
V> Measur't. Mode	Phase-Phase	Phase to Phase Phase to Neutral		N/A
Sets the measured input voltage, phase-phase or phase-neutral that will be used for the overvoltage elements.				
V> Operate Mode	Any Phase	Any Phase Three Phase		N/A
Setting that determines whether any phase or all three phases has to satisfy the overvoltage criteria before a decision is made.				
OVERVOLTAGE PEAK	Sub-heading			
V>1 Status	Enabled	Disabled, Enabled		N/A
Enables or disables the first stage peak overvoltage element.				
V>1 Voltage Set	110 V (Vn=100/120 V)	10 V (Vn=100/120 V)	185 V (Vn=100/120 V)	1V (Vn=100/120 V)
Pick-up setting for first stage peak overvoltage element.				
V>1 Time Delay	1 s	0 s	100 s	0.01 s
Operating time-delay setting for the first stage definite time peak overvoltage element.				
V>1 tReset	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
V>1 SV Iterations	3	1	10	1
Sets the number of iterations of the sampled values used by the Peak Overvoltage protection element to obtain a start signal.				
V>2 Cells as for V>1 above except default setting for V>2 Status is Disabled				
OVERVOLTAGE RMS	Sub-heading			
V>3 Function	DT	Disabled DT IDMT Default Curve 1/2/3/4		N/A
Tripping characteristic setting for the first stage RMS overvoltage element. The IDMT characteristic available on the first stage is defined by the following formula: t = K / (M - 1) Where: K = Time multiplier setting t = Operating time in seconds M = Measured voltage/relay setting voltage (V<>Voltage Set)				
V>3 Voltage Set	110 V (Vn=100/120 V)	10 V (Vn=100/120 V)	185 V (Vn=100/120 V)	1V (Vn=100/120 V)
Pick-up setting for first stage RMS overvoltage element.				
V>3 Time Delay	1 s	0 s	100 s	0.01 s
Operating time-delay setting for the first stage RMS definite time overvoltage element.				
V>3 TMS	1	0.5	100	0.5
Time multiplier setting to adjust the operating time of the IDMT characteristic.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
V>4 Cells as for V>3 above except default setting for V>3 Function is Disabled				

Table 20: Under/Overvoltage protection settings

1.2.18 Frequency protection (81U/81O/81AB)

The P342/3/4/5/6 relays include 4 stages of underfrequency and 2 stages of overfrequency protection to facilitate load shedding and subsequent restoration. The underfrequency stages may be optionally blocked by a pole dead (CB Open) condition.

The P348 relay includes 4 stages of overfrequency protection to provide excessive rotor slip frequency protection for variable speed double fed induction machines.

The P342/3/4/5/6 relays also include six bands of generator turbine abnormal frequency protection. Each band has its own frequency limit settings and an individual accumulative time measurement. Operation within each of these bands is monitored and the time added to a cumulative timer. An individual dead band time delay setting is provided for each band. Within this dead band time delay, the frequency is allowed to stay inside the band without initiating the accumulative time measurement. This delay allows the blade's resonance during under frequency conditions to be established first, thus avoiding unnecessary accumulation of time. The delay therefore does not contribute to the accumulated time.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: FREQ. PROTECTION				
UNDERFREQUENCY				
F<1 Status	Enabled	Disabled, Enabled		N/A
Enables or disables the first stage underfrequency element.				
F<1 Setting	49.5 Hz	45 Hz	65 Hz	0.01 Hz
Pick-up setting for the first stage underfrequency element.				
F<1 Time Delay	4 s	0 s	20000 s	0.01 s
Operating time-delay setting for the definite time first stage underfrequency element.				
F<2 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the second stage underfrequency element.				
F<2 Setting	49 Hz	45 Hz	65 Hz	0.01 Hz
Pick-up setting for the second stage underfrequency element.				
F<2 Time Delay	3 s	0 s	20000 s	0.01 s
Operating time-delay setting for the definite time second stage underfrequency element.				
F<3 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the third stage underfrequency element.				
F<3 Setting	48.5 Hz	45 Hz	65 Hz	0.01 Hz
Pick-up setting for the third stage underfrequency element.				
F<3 Time Delay	2 s	0 s	20000 s	0.01 s
Operating time-delay setting for the definite time third stage underfrequency element.				
F<4 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the fourth stage underfrequency element.				
F<4 Setting	48 Hz	45 Hz	65 Hz	0.01 Hz
Pick-up setting for the fourth stage underfrequency element.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
F<4 Time Delay	1 s	0 s	20000 s	0.01 s
Operating time-delay setting for the definite time fourth stage underfrequency element.				
F< Function Link	0000	Bit 0 = F<1 Poledead Blk. Bit 1 = F<2 Poledead Blk. Bit 2 = F<3 Poledead Blk. Bit 3 = F<4 Poledead Blk.		N/A
Settings that determine whether pole dead logic signals blocks the underfrequency elements. With the relevant bit set to 1, the relevant underfrequency stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the underfrequency protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
OVERFREQUENCY	(P342/3/4/5/6)			
F>1 Status	Enabled	Disabled, Enabled		N/A
Enables or disables the first stage overfrequency element.				
F>1 Setting	50.5 Hz	45 Hz	68 Hz	0.01 Hz
Pick-up setting for the first stage overfrequency element.				
F>1 Time Delay	2 s	0 s	100 s	0.01 s
Operating time-delay setting for the first stage overfrequency element.				
F>2 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the second stage overfrequency element.				
F>2 Setting	51 Hz	45 Hz	68 Hz	0.01 Hz
Pick-up setting for the second stage overfrequency element.				
F>2 Time Delay	1 s	0 s	100 s	0.01 s
Operating time-delay setting for the second stage overfrequency element.				
OVERFREQUENCY	(P348)			
F>1 Status	Enabled	Disabled, Enabled		N/A
Enables or disables the first stage rotor overfrequency element.				
F>1 Setting	5 Hz	0.1 Hz	70 Hz	0.1 Hz
Pick-up setting for the first stage rotor overfrequency element.				
F>1 Time Delay	2 s	0 s	100 s	0.01 s
Operating time-delay setting for the first stage rotor overfrequency element.				
F>2 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the second stage rotor overfrequency element.				
F>2 Setting	5 Hz	0.1 Hz	70 Hz	0.1 Hz
Pick-up setting for the second stage rotor overfrequency element.				
F>2 Time Delay	1 s	0 s	100 s	0.01 s
Operating time-delay setting for the second stage rotor overfrequency element.				
F>3/4 Cells as for F>2 above				
TURBINE F PROT				
Turbine F Status	Disabled	Disabled, Enabled		N/A
Enables or disables the turbine abnormal frequency element.				
Band 1 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the turbine abnormal frequency Band 1 element.				
Band 1 Freq. Low	46.50 Hz	20 Hz	70 Hz	0.01 Hz
Lower limit frequency setting for the Band 1 element.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Band 1 Freq. High	47.00 Hz	20 Hz	70 Hz	0.01 Hz
Upper limit frequency setting for the Band 1 element.				
Band 1 Duration	1.0 s	0 s	3600000 s	0.01 s
Accumulation time-delay setting for frequency in the Band 1 element.				
Band 1 Dead Time	0.2 s	0 s	200 s	0.01 s
Time-delay setting before time accumulation starts for the Band 1 element.				
Band 2 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the turbine abnormal frequency Band 2 element.				
Band 2 Freq. Low	47.00 Hz	20 Hz	70 Hz	0.01 Hz
Lower limit frequency setting for the Band 2 element.				
Band 2 Freq. High	47.50 Hz	20 Hz	70 Hz	0.01 Hz
Upper limit frequency setting for the Band 2 element.				
Band 2 Duration	2.5 s	0 s	3600000 s	0.01 s
Accumulation time-delay setting for frequency in the Band 2 element.				
Band 2 Dead Time	0.2 s	0 s	200 s	0.01 s
Time-delay setting before time accumulation starts for the Band 2 element.				
Band 3 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the turbine abnormal frequency Band 3 element.				
Band 3 Freq. Low	47.50 Hz	20 Hz	70 Hz	0.01 Hz
Lower limit frequency setting for the Band 3 element.				
Band 3 Freq. High	48.00 Hz	20 Hz	70 Hz	0.01 Hz
Upper limit frequency setting for the Band 2 element.				
Band 3 Duration	14 s	0 s	3600000 s	0.01 s
Accumulation time-delay setting for frequency in the Band 3 element.				
Band 3 Dead Time	0.2 s	0 s	200 s	0.01 s
Time-delay setting before time accumulation starts for the Band 3 element.				
Band 4 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the turbine abnormal frequency Band 4 element.				
Band 4 Freq. Low	48.00 Hz	20 Hz	70 Hz	0.01 Hz
Lower limit frequency setting for the Band 4 element.				
Band 4 Freq. High	48.50 Hz	20 Hz	70 Hz	0.01 Hz
Upper limit frequency setting for the Band 4 element.				
Band 4 Duration	100 s	0 s	3600000 s	0.01 s
Accumulation time-delay setting for frequency in the Band 4 element.				
Band 4 Dead Time	0.2 s	0 s	200 s	0.01 s
Time-delay setting before time accumulation starts for the Band 4 element.				
Band 5 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the turbine abnormal frequency Band 5 element.				
Band 5 Freq. Low	48.50 Hz	20 Hz	70 Hz	0.01 Hz
Lower limit frequency setting for the Band 5 element.				
Band 5 Freq. High	49.00 Hz	20 Hz	70 Hz	0.01 Hz
Upper limit frequency setting for the Band 5 element.				
Band 5 Duration	540 s	0 s	3600000 s	0.01 s
Accumulation time-delay setting for frequency in the Band 5 element.				
Band 5 Dead Time	0.2 s	0 s	200 s	0.01 s
Time-delay setting before time accumulation starts for the Band 5 element.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Band 6 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the turbine abnormal frequency Band 6 element.				
Band 6 Freq. Low	49.00 Hz	20 Hz	70 Hz	0.01 Hz
Lower limit frequency setting for the Band 6 element.				
Band 6 Freq. High	49.50 Hz	20 Hz	70 Hz	0.01 Hz
Upper limit frequency setting for the Band 6 element.				
Band 6 Duration	3000 s	0 s	3600000 s	0.01 s
Accumulation time-delay setting for frequency in the Band 6 element.				
Band 6 Dead Time	0.2 s	0 s	200 s	0.01 s
Time-delay setting before time accumulation starts for the Band 6 element.				

Table 21: Frequency protection settings

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1.2.19 Resistor temperature device (RTD)

The P342/3/4/5 relays provide temperature protection from 10 PT100 resistor temperature devices (RTD). Each RTD has a definite time trip and alarm stage.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: RTD PROTECTION				
Select RTD	0000000000	Bit 0 - Select RTD 1 Bit 1 - Select RTD 2 Bit 2 - Select RTD 3 Bit 3 - Select RTD 4 Bit 4 - Select RTD 5 Bit 5 - Select RTD 6 Bit 6 - Select RTD 7 Bit 7 - Select RTD 8 Bit 8 - Select RTD 9 Bit 9 - Select RTD 10		N/A
10 bit setting to enable or disable the 10 RTDs. For each bit 1 = Enabled, 0 = Disabled.				
RTD 1 Alarm Set	80°C	0°C	200°C	1°C
Temperature setting for the RTD 1 alarm element.				
RTD 1 Alarm Dly	10 s	0 s	100 s	1 s
Operating time delay setting for the RTD 1 alarm element.				
RTD 1 Trip Set	85°C	0°C	200°C	1°C
Temperature setting for the RTD 1 trip element.				
RTD 1 Trip Dly	1 s	0	100 s	1 s
Operating time delay setting for the RTD 1 alarm element.				
RTD 2-10 Alarm and Trip Settings are the same as RTD1.				

Table 22: RTD protection settings

1.2.20 Circuit breaker fail and undercurrent function (50BF)

This function in the P342/3/4/5/6 consists of a two-stage circuit breaker fail function that can be initiated by:

- Current based protection elements
- Non current based protection elements
- External protection elements

For current-based protection, the reset condition is based on undercurrent operation to determine that the CB has opened. For the non-current based protection, the reset criteria may be selected by means of a setting for determining a CB Failure condition.

It is common practice to use low set undercurrent elements in protection relays to indicate that circuit breaker poles have interrupted the fault or load current, as required. The current source of the undercurrent elements in the P343/4/5/6 can also be selected – terminal or neutral side CTs.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: CB FAIL & I<				
BREAKER FAIL	Sub-heading			
CB Fail 1 Status	Enabled	Disabled, Enabled		
Enables or disables the first stage of the circuit breaker function.				
CB Fail 1 Timer	0.2 s	0 s	10 s	0.01 s
Circuit breaker fail timer setting for stage 1 for which the initiating condition must be valid.				
CB Fail 2 Status	Disabled	Disabled, Enabled		
Enables or disables the second stage of the circuit breaker function.				
CB Fail 2 Timer	0.4 s	0 s	10 s	0.01 s
Circuit breaker fail timer setting for stage 2 for which the initiating condition must be valid.				
CBF Non I Reset	CB Open & I<	I< Only, CB Open & I<, Prot. Reset & I<		
Setting which determines the elements that will reset the circuit breaker fail time for non current based protection functions (e.g. voltage, frequency) initiating circuit breaker fail conditions.				
CBF Ext Reset	CB Open & I<	I< Only, CB Open & I<, Prot. Reset & I<		
Setting which determines the elements that will reset the circuit breaker fail time for external protection functions initiating circuit breaker fail conditions.				
UNDERCURRENT	Sub-heading			
I< Current Set	0.1 In	0.02 In	3.2 In	0.01 In
Circuit breaker fail phase fault undercurrent setting. This undercurrent element is used to reset the CB failure function initiated from the internal or external protection (Any Trip and Ext Trip 3Ph signals).				
IN< Current Set	0.1 In	0.02 In	3.2 In	0.01 In
Circuit breaker fail earth fault undercurrent setting. This undercurrent element is used to reset the CB failure function initiated from the internal or external protection (Any Trip and Ext Trip 3Ph signals).				
ISEF< Current	0.02 In	0.001 In	0.8 In	0.0005 In
Circuit breaker fail sensitive earth fault undercurrent setting. This undercurrent element is used to reset the CB failure function initiated from the sensitive earth fault protection.				
BLOCKED O/C	Sub-heading			
I< CT Source	IA-1, IB-1, IC-1	IA-1, IB-1, IC-1/IA-2, IB-2, IC-2		
This setting is used to select the 3 phase current inputs used by the CB failure undercurrent elements in the P343/4/5/6 - neutral or terminal side CT inputs.				

Table 23: CB Fail protection settings

1.2.21 Supervision (VTS, CTS and Through Fault Monitoring)

The VTS feature in the P342/3/4/5/6 relay operates when it detects a negative phase sequence (NPS) voltage when there is no negative phase sequence current. This gives operation, for the loss of one or two-phase voltages. Stability of the VTS function is assured during system fault conditions, by the presence of NPS current. The use of negative sequence quantities ensures correct operation even where three-limb or 'V' connected VTs are used.

If all three-phase voltages to the relay are lost, there are no negative phase sequence quantities to operate the VTS function, and the three-phase voltages collapse. If this is detected without a corresponding change in any of the phase current signals (which would be indicative of a fault), a VTS condition will be raised. In practice, the relay detects superimposed current signals, which are changes in the current applied to the relay.

If a VT is inadvertently left isolated before line energization, voltage dependent elements may operate incorrectly. The previous VTS element detected 3-phase VT failure due to the absence of all 3-phase voltages with no corresponding change in current. However, on line energization there is a change in current, for example, due to load or line charging current. An alternative method of detecting 3-phase VT failure is therefore required on line energization.

The absence of measured voltage on all three-phases on line energization can be as a result of two conditions. The first is a 3-phase VT failure and the second is a close up 3-phase fault. The first condition would require blocking of the voltage dependent function and the second would require tripping. To differentiate between these two conditions an overcurrent level detector (VTS I> Inhibit) is used to prevent a VTS block from being issued if it operates. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close up 3-phase fault. If the line is closed where a 3-phase VT failure is present the overcurrent detector will not operate and a VTS block will be applied. Closing onto a 3-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

This logic will only be enabled during a live line condition (as indicated by the relays pole dead logic) to prevent operation under dead system conditions i.e. where no voltage will be present and the VTS I> Inhibit overcurrent element will not be picked up.

The CT supervision feature operates on detection of derived zero sequence current, in the absence of corresponding derived zero sequence voltage that would normally accompany it.

The CT supervision can be set to operate from the residual voltage measured at the VNEUTRAL input (VN1 input for P342/3/4/5/6) or the residual voltage derived from the three phase-neutral voltage inputs as selected by the 'CTS Vn Input' setting.

There are two stages of CT supervision CTS-1 and CTS-2. CTS-1 supervises the CT inputs to IA, IB, IC which are used by the biased differential protection and all the power, impedance and overcurrent based protection functions. CTS-2 supervises the CT inputs to IA-2, IB-2, IC-2 which are used by the biased or high impedance differential or interturn protection in the P343/4/5/6. The CTS-2 independent enabled/disabled setting is to prevent CTS-2 from giving unnecessary alarms when the Generator Differential is disabled. For interturn faults, some utilities may isolate the faulted winding section and return the generator to service, therefore producing unbalanced phase currents. Under these circumstances the CTS-2 may also need to be disabled or de-sensitized to prevent a false alarm and a false block.

The Through Fault monitoring is implemented in the P342/3/4/5/6. Through faults are a major cause of transformer damage and failure. Both the insulation and the mechanical effects of fault currents are considered. The through fault current monitoring function in the P34x gives the fault current level, the duration of the faulty condition, the date and time for each through fault. An I^2t calculation based on the recorded time duration and maximum current is performed for each phase. Cumulative stored calculations for each phase are monitored so that the user may schedule the transformer maintenance based on this data. This may also justify possible system enhancement to reduce through fault level.

The P348 provides stator CT supervision to detect CT failure and block the stator negative phase sequence overcurrent protection. The P348 CT supervision operates in the same way as the P342-6 CT supervision by detecting derived residual current in the absence of corresponding derived or measured residual voltage that would normally accompany it during an unbalanced fault. However, it is not possible to measure stator residual voltage in the P348 as the P348 does not measure the stator voltages. The residual voltage, therefore, needs to come from an external source, for example the stator P34x protection relay.

The P348 provides rotor VT supervision to detect VT failure and block the NVD protection in such cases. The rotor VT supervision is based on voltage balance scheme, where two sets of three phase voltages are provided and the difference between the sample values of the two voltages are calculated. The VTS includes a time delay and voltage difference setting.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
SUPERVISION GROUP 1				
VT SUPERVISION	Sub-heading (P342/3/4/5/6)			
VTS Status	Blocking	Blocking, Indication		
This setting determines whether the following operations will occur upon detection of VTS. - VTS set to provide alarm indication only. - Optional blocking of voltage dependent protection elements. - Optional conversion of directional overcurrent elements to non-directional protection (available when set to blocking mode only). These settings are found in the function links cell of the relevant protection element columns in the menu.				
VTS Reset Mode	Manual	Manual, Auto		
The VTS block will be latched after a user settable time delay 'VTS Time Delay'. Once the signal has latched then two methods of resetting are available. The first is manually via the front panel interface (or remote communications) and secondly, when in 'Auto' mode, provided the VTS condition has been removed and the 3 phase voltages have been restored above the phase level detector settings for more than 240 ms.				
VTS Time Delay	5 s	1 s	10 s	0.1 s
Operating time-delay setting of the VTS element upon detection of a voltage supervision condition.				
VTS I> Inhibit	10 In	0.08 In	32 In	0.01 In
This overcurrent setting is used to inhibit the voltage transformer supervision in the event of a loss of all 3 phase voltages caused by a close up 3 phase fault occurring on the system following closure of the CB to energize the line.				
VTS I2> Inhibit	0.05 In	0.05 In	0.5 In	0.01 In
This NPS overcurrent setting is used to inhibit the voltage transformer supervision in the event of a fault occurring on the system with negative sequence current above this setting.				
CT SUPERVISION	Sub-heading			
CTS1 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the current transformer supervision 1 element. (P342-6)				
CTS1 VN Input	Derived	Derived, Measured		N/A
Residual/neutral voltage source for CTS1.				
CTS VN< Inhibit	5 V (Vn=100/120 V) 20 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)	22 V (Vn=100/120 V) 88 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Residual/neutral voltage setting to inhibit the CTS1 element.				
CTS1 IN> Set	0.2 In	0.08 In	4 In	0.01 In
Residual/neutral current setting for a valid current transformer supervision condition for CTS1.				
CTS1 Time Delay	5 s	0 s	10 s	1 s
Operating time-delay setting of CTS1.				
CTS2 Status	Disabled	Disabled, Enabled		N/A
Enables or disables the current transformer supervision 2 element (P343/4/5/6/8).				
CTS2 VN Input	Derived	Derived, Measured		N/A
Residual/neutral voltage source for CTS2. (P343-6)				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CTS VN< Inhibit	5 V (Vn=100/120 V) 20 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)	22 V (Vn=100/120 V) 88 V (Vn=380/480 V)	CTS VN< Inhibit
Residual/neutral voltage setting to inhibit the CTS2 element. (P343-6)				
CTS2 IN> Set	0.2 In	0.08 In	4 In	0.01 In
Residual/neutral current setting for a valid current transformer supervision condition for CTS1 (P343/4/5/6/8).				
CTS2 Time Delay	5 s	0 s	10 s	1 s
Operating time-delay setting of CTS2 (P343/4/5/6/8).				
DIFF CTS Status	Enabled	Disabled, Enabled		
Enables or disables the differential current transformer supervision function. (P343-6)				
Diff CTS Mode	Restrain	Indication, Restrain		
In **Indication** mode, the CTS alarm is issued without delay when a CT failure is detected. Also the differential protection is set to the **Is-CTS setting in Restrain** mode. The differential protection is sensitized to the **Is-CTS** setting and the CTS alarm is issued after the time delay defined in **CTS time delay**				
CTS Time delay	2 s	0 s	10 s	0.1 s
Differential CTS alarm time delay on detection of a current transformer supervision condition. This setting does not affect the CTS blocking operation.				
CTS I1	10%	5%	100%	1%
Set release threshold.				
CTS I2/I1>1	5%	5%	100%	1%
Low set ratio of negative to positive sequence current.				
CTS I2/I1>2	30%	5%	100%	1%
High set ratio of negative to positive sequence current.				
		Disabled, Enabled		N/A
		0.08 In	4 In	0.01 In
		0 s	10 s	1 s
THROUGH FAULT				
Through Fault	Enabled	Disabled, Enabled		
Enables or disables monitoring of through faults.				
Monitored Input	HV	HV, LV		
Selects the input winding to be monitored.				
TF I> Trigger	1 In	0.08 In	16 In	0.01 In
A through fault event is recorded if any of the phase currents is larger than this setting.				
TF I2t> Alarm	800 A2s	0	50000 A^2s	1 A^2s
An alarm is asserted if the maximum cumulative I2t in the three phases exceeds this setting.				
VT SUPERVISION	Sub-heading (P348)			
VTS Status	Blocking	Blocking, Indication, Disabled		
This setting determines whether the following operations will occur upon detection of VTS. - VTS set to provide alarm indication only. - Optional blocking of voltage dependent protection elements (NVD) - VTS is disabled				
VTS Time Delay	2 s	0 s	10 s	1 s
Operating time-delay setting of the VTS.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VTS V Diff Set	5 V (Vn=100/120 V)	1 V (Vn=100/120 V)	80 V (Vn=100/120 V)	0.5 V (Vn=100/120 V)
VTS differential voltage setting				

Table 24: VTS, CTS and through fault monitoring protection settings

1.2.22 Sensitive power protection (32P/Q)

The single phase power protection included in the P342/3/4/5/6 relay provides four stages of power protection. Each stage can be independently selected to operate as either under or over or disabled. The direction of operation of the power protection, forward or reverse, can also be defined with the direction setting. Each stage can be independently selected to operate as either active or reactive power.

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The P345 has an additional option to select wattmetric power instead of single phase power.

Note: The high impedance REF element of the relay shares the same sensitive current input as the SEF protection and sensitive power protection. Hence, only one of these elements may be selected.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: SENSITIVE POWER				
Comp Angle	0	-5°	5°	0.1
Setting for the compensation angle.				
P> CT Source	Single	Single (P342/3/4/6) Single, Wattmetric (P345)		
Sensitive power CT source. A single sensitive current input for single phase power is the only option for P342/3/4/6. The P345 has the option of using the single sensitive current input for single phase power or 2 sensitive current inputs for wattmetric power.				
P> Phase Select	A	A, B, C		
Phase to be used for single phase power calculation, A or B or C.				
Sen Power1 Func	Over	Disabled, Under, Over		
First stage sensitive power function operating mode, under or over.				
Sen Power1 Dirn	Forward	Forward, Reverse		
First stage sensitive power function direction, forward or reverse.				
Sen Power1 Mode	Active	Active, Reactive		
First stage sensitive power function power mode, active or reactive power.				
Sen Power1 1Ph Watt	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.2 In W (Vn=100/120 V) 0.8 In W (Vn=380/480 V)	100 In W (Vn=100/120 V) 400 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the first stage single phase sensitive active power protection element.				
Sen Power1 1Ph VArs	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.2 In W (Vn=100/120 V) 0.8 In W (Vn=380/480 V)	100 In W (Vn=100/120 V) 400 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the first stage single phase sensitive reactive power protection element.				
Sen Power1 3Ph Watt	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the first stage wattmetric sensitive active power protection element.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: SENSITIVE POWER				
Sen Power1 3Ph VArs	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the first stage wattmetric sensitive reactive power protection element.				
Sen Power1 Delay	5 s	0 s	100 s	0.01 s
Operating time-delay setting of the first stage sensitive power protection.				
Power1 DO Timer	0 s	0 s	100 s	0.01 s
Drop-off time delay setting of the first stage sensitive power protection function. Setting of the drop-off timer to a value other than zero, delays the resetting of the protection element timers for this period. By using the drop-off timer the relay will integrate the fault power pulses, thereby reducing fault clearance times.				
P1 Poledead Inh	Enabled	Disabled, Enabled		
If the setting is enabled, the relevant stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the power protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
Sen Power2 Func	Over	Disabled, Under, Over		
Second stage sensitive power function operating mode, under or over.				
Sen Power2 Dirn	Forward	Forward, Reverse		
Second stage sensitive power function direction, forward or reverse.				
Sen Power2 Mode	Active	Active, Reactive		
Second stage sensitive power function power mode, active or reactive power.				
Sen Power2 1Ph Watt	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.2 In W (Vn=100/120 V) 0.8 In W (Vn=380/480 V)	100 In W (Vn=100/120 V) 400 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the second stage single phase sensitive active power protection element.				
Sen Power2 1Ph VArs	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.2 In W (Vn=100/120 V) 0.8 In W (Vn=380/480 V)	100 In W (Vn=100/120 V) 400 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the second stage single phase sensitive reactive power protection element.				
Sen Power2 3Ph Watt	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the second stage wattmetric sensitive active power protection element.				
Sen Power2 3Ph VArs	0.5 In W (Vn=100/120 V) 2 In W (Vn=380/480 V)	0.4 In W (Vn=100/120 V) 1.6 In W (Vn=380/480 V)	300 In W (Vn=100/120 V) 1200 In W (Vn=380/480 V)	0.1 In W (Vn=100/120 V) 0.4 In W (Vn=380/480 V)
Pick-up setting for the second stage wattmetric sensitive reactive power protection element.				
Sen Power2 Delay	5 s	0 s	100 s	0.01 s
Operating time-delay setting of the second stage sensitive power protection.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: SENSITIVE POWER				
Power2 DO Timer	0 s	0 s	100 s	0.01 s
Drop-off time delay setting of the second stage sensitive power protection function. Setting of the drop-off timer to a value other than zero, delays the resetting of the protection element timers for this period. By using the drop-off timer the relay will integrate the fault power pulses, thereby reducing fault clearance times.				
P2 Poledead Inh	Enabled	Disabled, Enabled		
If the setting is enabled, the relevant stage will become inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the power protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
Sen Power 3 and Sen Power 4 settings are the same as Sen Power 1 and Sen Power 2 settings.				

Table 25: Sensitive power protection settings

1.2.23 Pole slipping (78)

The P343/4/5 pole slipping characteristic consists of three parts. The first part is the lenticular (lens) characteristic. The second is a straight line referred to as the blinder that bisects the lens and divides the impedance plane into the left and right halves. The third is a reactance line which is perpendicular to the blinder.

The inclination of the lens and the blinder, (Blinder Angle) is determined by the angle of the total system impedance. The equivalent impedance of the system and the step-up transformer determines the forward reach of the lens, (PSlip Za Forward), whereas the generator's transient reactance determines the reverse reach (PSlip Zb Reverse). The width of the lens is varied by the setting of the lens angle (Lens Angle). A reactance line (PSlip Zc), perpendicular to the axis of the lens, is used to distinguish whether the impedance centre of the swing is located in the power system or in the generator. The reactance line splits the lens into Zone 1 (lens below the line) and Zone 2 (all of the lens). During a pole slip the impedance crosses the lens spending at least time PSlip T1 and PSlip T2 in each half. Counters are available for both zone 1 and zone 2 to count the number of pole slip cycles before a trip. There is a reset timer (PSlip Reset Time) which is required to reset the counters for pole slips that are cleared by external protection.

When a generator is out of step with the system, the impedance locus is expected to traverse from right to left across the lens and the blinder. However, if the generator is running as a motor, as in the pumping mode of a pump storage generator, the impedance locus is expected to swing from the left to the right. A pole slip mode setting is provided to determine whether the protection operates in a 'Generating' mode or in a 'Motoring' mode or 'Both'. For a pump storage generator, its operation can switch from generating mode to motoring mode and vice versa.

Menu text	Default setting	Setting range		Step size
		Min	Max	
Group 1: POLE SLIPPING				
Pslip Function	Enabled	Disabled, Enabled		N/A
Enables or disables the pole slipping protection.				
Pole Slip Mode	Generating	Motoring, Generating, Both		N/A
Selection of the pole slip operating mode.				
Pslip Za Forward	100/In Ω	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)	350/In Ω (Vn=100/120 V) 1400/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)

Menu text	Default setting	Setting range		Step size
		Min	Max	
Group 1: POLE SLIPPING				
Forward impedance reach setting of the pole slipping lens characteristic.				
Pslip Zb Reverse	150/In Ω	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)	350/In Ω (Vn=100/120 V) 1400/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)
Reverse impedance reach setting of the pole slipping lens characteristic.				
Lens Angle	120°	90°	150°	1°
Lens angle setting. The lens width is proportional to the lens angle, a 90° lens angle is a circle.				
PSlip Timer T1	0.015 s	0 s	1 s	0.005 s
Minimum time-delay setting that impedance must remain in half of the lens characteristic. The lens is split in half by the blinder defining left and right hand halves. Timer T1 starts when the impedance is in the right hand half of the lens when the operating mode is Generating and the left hand half of the lens when the operating mode is Motoring. If the operating mode is set to Both then T1 starts timing in whichever half the impedance first appears.				
PSlip Timer T2	0.015 s	0 s	1 s	0.005 s
Minimum time-delay setting that impedance must remain in half of the lens characteristic. The lens is split in half by the blinder defining left and right hand halves. Timer T2 starts when the impedance is in the opposite half of the lens characteristic to T1 operating.				
Blinder Angle	75°	20°	90°	1°
Blinder angle setting. This defines the inclination of the lens characteristic which should be consistent with the system impedance angle.				
PSlip Zc	50/In Ω	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)	350/In Ω (Vn=100/120 V) 1400/In Ω (Vn=380/480 V)	0.5/In Ω (Vn=100/120 V) 2/In Ω (Vn=380/480 V)
Forward impedance reach setting of the reactance line. The reactance line splits the lens into 2 zones. Zone 1 is the lens characteristic below the reactance line and Zone 2 is all of the lens characteristic. The reactance line provides a means of discriminating pole slipping within the generator or within the power system. Typically the reactance line is set to encompass the generator and part of the generator-transformer.				
Zone1 Slip Count	1	1	20	1
Number of allowed pole slips in zone 1.				
Zone2 Slip Count	2	1	20	1
Number of allowed pole slips in zone 2.				
PSlip Reset Time	30 s	0 s	100 s	0.01 s
Reset time setting for pole slip protection. Resets the counters for pole slips cleared by external protection.				

Table 26: Pole slipping protection settings

1.2.24 Input labels

The GROUP 1 INPUT LABELS column is used to individually label each opto-input. The text is restricted to 16 characters and is available if ‘Input Labels’ are set to 'visible' in the CONFIGURATION column.

Menu text	Default setting	Setting range	Step size
GROUP 1: INPUT LABELS			
Opto Input 1	Input L1	16 Character Text	
Text label to describe each individual opto input. This text will be displayed in the programmable scheme logic and event record description of the opto input.			

Menu text	Default setting	Setting range	Step size
Opto Input 2 to 32	Input L2 to L32	16 Character Text	
Text label to describe each individual opto input. This text will be displayed in the programmable scheme logic and event record description of the opto input.			

Table 27: Input labels settings

1.2.25 Output labels

The GROUP 1 OUTPUT LABELS column is used to individually label each output relay. The text is restricted to 16 characters and is available if 'Input Labels' are set to 'visible' in the CONFIGURATION column.

Menu text	Default setting	Setting range	Step size
GROUP 1: OUTPUT LABELS			
Relay 1	Output R1	16 Character Text	
Text label to describe each individual relay output contact. This text will be displayed in the programmable scheme logic and event record description of the relay output contact.			
Relay 2 to 32	Output R2 to R32	16 Character Text	
Text label to describe each individual relay output contact. This text will be displayed in the programmable scheme logic and event record description of the relay output contact.			

Table 28: Output labels settings

1.2.26 RTD labels

10 RTD are provided in the P342/3/4/5/6 for temperature measurement. The GROUP 1 RTD LABELS column is used to individually label each RTD. The text is restricted to 16 characters and is available if 'RTD Labels' are set to 'visible' in the CONFIGURATION column.

Menu text	Default setting	Setting range	Step size
GROUP 1: RTD LABELS			
RTD 1	RTD 1	16 Character Text	
Text label to describe each individual RTD. This text will be displayed in the Measurements 3 menu and fault records for the description of the RTDs.			
Relay 2 to 32	Output R2 to R32	16 Character Text	
Text label to describe each individual RTD. This text will be displayed in the Measurements 3 menu and fault records for the description of the RTDs.			

Table 29: RTD labels settings

1.2.27 Current loop inputs and outputs (CLIO)

Four analog or current loop inputs are provided in the P342/3/4/5/6/8 for transducers with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA. The analog inputs can be used for various transducers such as vibration monitors, tachometers and pressure transducers. Associated with each input there are two protection stages, one for alarm and one for trip. Each stage can be individually enabled or disabled and each stage has a Definite Time delay setting. The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold 'Under' or when the input current is above the input value 'Over'. The
4-20 mA input has an undercurrent alarm element which can be used to indicate a fault with the transducer or wiring.

There are four analog current outputs with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA which can reduce the need for separate transducers. These outputs can be fed to standard moving coil ammeters for analog measurements or to a SCADA system using an existing analog RTU.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: CLIO PROTECTION				
CLIO Input 1	Disabled	Disabled, Enabled		N/A
Enables or disables the current loop (transducer) input 1 element.				
CLI1 Input Type	4 - 20 mA	0 - 1 mA, 0 - 10 mA, 0 - 20 mA, 4 - 20 mA		N/A
Current loop 1 input type.				
CLI1 Input Label	CLIO Input 1	16 characters		
Current loop 1 input description. The minimum and maximum settings define the range but they have no units. The user can use the label to enter the transducer function and unit of measurement, e.g. Power MW, which is used in the Measurements 3 menu to describe the CLI1 measurement.				
CLI1 Minimum	0	-9999	9999	0.1
Current loop input 1 minimum setting. Defines the lower range of the physical or electrical quantity measured by the transducer.				
CLI1 Maximum	100	-9999	9999	0.1
Current loop input 1 maximum setting. Defines the upper range of the physical or electrical quantity measured by the transducer.				
CLI1 Alarm	Disabled	Disabled, Enabled		N/A
Enables or disables the current loop input 1 alarm element.				
CLI1 Alarm Fn	Over	Over, Under		N/A
Operating mode of the current loop input 1 alarm element.				
CLI1 Alarm Set	50	Min. (CLI1 Min., Max.)	Max. (CLI1 Min., Max.)	0.1
Pick-up setting for the current loop input 1 alarm element.				
CLI1 Alarm Delay	1	0	100 s	0.1 s
Operating time-delay setting of current loop input 1 alarm element.				
CLI1 Trip	Disabled	Disabled, Enabled		N/A
Pick-up setting for the current loop input 1 trip element.				
CLI1 Trip Fn	Over	Over, Under		N/A
Operating mode of the current loop input 1 alarm element.				
CLI1 Trip Set	50	Min. (CLI1 Min., Max.)	Max. (CLI1 Min., Max.)	0.1
Pick-up setting for the current loop input 1 trip element.				
CLI1 Trip Delay	1	0	100 s	0.1 s
Operating mode of the current loop input 1 trip element.				
CLI1 I< Alarm	Disabled	Disabled, Enabled		N/A
Enables or disables the current loop input 1 undercurrent element used to supervise the 4-20mA input only.				
CLI1 I< Alm Set	3.5 mA	0	4 mA	0.1 mA
Pick-up setting for the current loop input 1 undercurrent element. (4 - 20 mA input only).				
CLI2/3/4 settings are the same as CLI1				
CLIO Output 1	Disabled	Disabled, Enabled		N/A
Enable or disables the current loop (transducer) output 1 element.				
CLO1 Output Type	4 - 20 mA	0 - 1 mA, 0 - 10 mA, 0 - 20 mA, 4- 20 mA		
Current loop 1 output type				
CLO1 Set Values	Primary	Primary, Secondary		N/A
This setting controls if the measured values via current loop output 1 are Primary or Secondary values.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CLO1 Parameter	IA Magnitude (P342-6) IA-1 RMS (P348)	A list of parameters are shown in the table below		N/A
This setting defines the measured quantity assigned to current loop output 1.				
CLO1 Minimum	0	Range, step size and unit corresponds to the selected parameter in the table below		N/A
Current loop output 1 minimum setting. Defines the lower range of the measurement.				
CLO1 Maximum	1.2 In	Range, step size and unit corresponds to the selected parameter in the table below		N/A
Current loop output 1 maximum setting. Defines the upper range of the measurement.				
CLO2/3/4 settings are the same as CLO1, except default setting for CLO2 Parameter is IB Magnitude (P342-6), IB-1 RMS (P348), CLO3 Parameter is IC Magnitude (P342-6), IC-1 RMS (P348), CLO4 Parameter is IN Measured Mag (P342-6) VA-1 RMS (P348).				

Table 30: Current loop inputs and outputs settings

The CLIO output conversion task runs every 50 ms and the refresh interval for the output measurements is nominally 50 ms. The exceptions are marked with an asterisk in the table of current loop output parameters below. Those exceptional measurements are updated once every second.

Current loop output parameters are shown in Table 31.

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
Current Magnitude	IA Magnitude (P342-6) IB Magnitude (P342-6) IC Magnitude (P342-6) IN Measured Mag. (P342) IN-1 Measured Mag. (P343/4/5/6) IN-2 Measured Mag. (P343/4/5/6) IA Diff 2H (P343/4/5/6) IB Diff 2H (P343/4/5/6) IC Diff 2H (P343/4/5/6) IA Diff 5H (P343/4/5/6) IB Diff 5H (P343/4/5/6) IC Diff 5H (P343/4/5/6)	A	0 to 16A	0.01A	0A	1.2A
Sensitive Current Input Magnitude	I Sen1 Magnitude (P342-6)	A	0 to 16A	0.01A	0A	1.2A
Phase Sequence Current Components	I1 Magnitude I2 Magnitude I0 Magnitude (P342-6)	A	0 to 16A	0.01A	0A	1.2A
RMS Phase Currents	IA RMS* IB RMS* IC RMS* (P342-6/8)	A	0 to 16A	0.01A	0A	1.2A

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
P-P Voltage Magnitude	VAB Magnitude VBC Magnitude VCA Magnitude (P342-6)	V	0 to 200 V	0.1 V	0 V	140 V
P-N voltage Magnitude	VAN Magnitude VBN Magnitude VCN Magnitude (P342-6)	V	0 to 200 V	0.1 V	0 V	80 V
Neutral Voltage Magnitude	VN1 Measured Mag. (P342-6) VN Derived Mag. (P342-6) VN2 Measured Mag. (P344/5)	V	0 to 200 V	0.1 V	0 V	80 V
3rd Harmonic Neutral Voltage	VN 3rd Harmonic (P343-5)	V	0 to 200 V	0.1 V	0 V	80 V
Phase Sequence Voltage Components	V1 Magnitude* V2 Magnitude V0 Magnitude (P342-6)	V	0 to 200 V	0.1 V	0 V	80 V
RMS Phase Voltages	VAN RMS* VBN RMS* VCN RMS* (P342-6/8)	V	0 to 200 V	0.1 V	0 V	80 V
Frequency (Stator Frequency P342-6 and Rotor Frequency P348)	Frequency (P342-6/8)	Hz	0 to 70 Hz	0.01 Hz	45 Hz (P342-6) 0.1 Hz (P348)	65 Hz (P342-6) 10 Hz (P348)
3 Ph Active Power	Three-Phase Watts* (P342-6)	W	-6000 W to 6000 W	1 W	0 W	300 W
3 Ph Reactive Power	Three-Phase Vars* (P342-6)	VAr	-6000 VAr to 6000 VAr	1 VAr	0 VAr	300 VAr
3 Ph Apparent Power	Three-Phase VA* (P342-6)	VA	0 to 6000 VA	1 VA	0 VA	300 VA
3 Ph Power Factor	3Ph Power Factor* (P342-6)	-	-1 to 1	0.01	0	1
Single-Phase Active Power	A Phase Watts* B Phase Watts* C Phase Watts* (P342-6)	W	-2000 W to 2000 W	1 W	0 W	100 W
Single-Phase Reactive Power	A Phase Vars* B Phase Vars* C Phase Vars* (P342-6)	VAr	-2000 VAr to 2000 VAr	1 VAr	0 VAr	100 VAr

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
Single-Phase Apparent Power	A Phase VA* B Phase VA* C Phase VA* (P342-6)	VA	0 to 2000 VA	1 VA	0 VA	100 VA
Single-Phase Power Factor	APh Power Factor* BPh Power Factor* CPh Power Factor* (P342-6)		-1 to 1	0.01	0	1
Three-Phase Current Demands	IA Fixed Demand* IB Fixed Demand* IC Fixed Demand* IA Roll Demand* IB Roll Demand* IC Roll Demand* IA Peak Demand* IB Peak Demand* IC Peak Demand* (P342-6)	A	0 to 16A	0.01A	0A	1.2A
3Ph Active Power Demands	3Ph W Fix Demand* 3Ph W Roll Dem* 3Ph W Peak Dem* (P342-6)	W	-6000 W to 6000 W	1 W	0 W	300 W
3Ph Reactive Power Demands	3Ph Vars Fix Dem* 3Ph Var Roll Dem* 3Ph Var Peak Dem* (P342-6)	VAr	-6000 VAr to 6000 VAr	1 VAr	0 VAr	300 VAr
Rotor Thermal State	NPS Thermal (P342-6)	%	0 to 200	0.01	0	120
Stator Thermal State	Thermal Overload (P342-6)	%	0 to 200	0.01	0	120
RTD Temperatures	RTD 1* RTD 2* RTD 3* RTD 4* RTD 5* RTD 6* RTD 7* RTD 8* RTD 9* RTD 10* (P342-6)	°C	-40°C to 300°C	0.1°C	0°C	200°C
Current Loop Inputs	CL Input 1 CL Input 2 CL Input 3 CL input 4 All (P342-6, 8)	-	-9999 to 9999	0.1	0	9999

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
Flux, V/Hz	Volts/Hz (P342-6)	V/Hz	0-20	0.01	0	4
df/dt	df/dt (P342-6)	Hz/s	-10 to 10 Hz/s	0.01 Hz/s	-1 Hz/s	1 Hz/s
Check Synch Voltages	C/S Voltage Mag C/S Bus Gen-Mag (P342-6)	V	0 to 200 V	0.1 V	0 V	80 V
Slip Frequency	Slip frequency (P342-6)	Hz	0 to 70 Hz	0.01 Hz	-0.5 Hz	0.5 Hz
Rotor RMS Phase Currents	IA-1 RMS* IB-1 RMS* IC-1 RMS* (P348)	A	0 to 16A	0.01A	0A	1.2A
Rotor Peak Phase Currents	IA-1 Peak* IB-1 Peak * IC-1 Peak * (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator RMS Phase Currents	IA-2 RMS* IB-2 RMS* IC-2 RMS* (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator RMS Negative Phase Sequence Current	I2 CT2 RMS* (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator Derived RMS Neutral Current	IN-2 Derived RMS* (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator Peak Phase Currents	IA-2 Peak* IB-2 Peak* IC-2 Peak* (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator Peak Negative Phase Sequence Current	I2 CT2 Peak* (P348)	A	0 to 16A	0.01A	0A	1.2A
Rotor RMS Phase Voltages	VA-1 RMS* VB-1 RMS* VC-1 RMS* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Rotor RMS Derived Neutral Voltage	VN-1 Derived RMS* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Rotor Peak Phase Voltages	VA-1 Peak* VB-1 Peak* VC-1 Peak* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Rotor Peak Derived Neutral Voltage	VN-1 Derived Peak* (P348)	V	0 to 200 V	0.1 V	0 V	80 V

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
Rotor RMS Phase-Phase Voltages	VAB-1 RMS* VBC-1 RMS* VCA-1 RMS* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Rotor Peak Phase-Phase Voltages	VAB-1 Peak* VBC-1 Peak* VCA-1 Peak* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Stator Peak Phase Voltages	VA-2 Peak* VB-2 Peak* VC-2Peak* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Stator Frequency	Frequency 2* (P348)	Hz	0 to 70 Hz	0.01 Hz	45 Hz	65 Hz
A Phase Impedance Magnitude	ZA Mag	Ω	0 to 750 Ω	0.5 Ω	0 Ω	1.2 Ω
Sensitive Single-Phase Active Power	Sen Watts	VAr	-750 W to 750 W	1 W	0 W	37.5 W
Sensitive Single-Phase Reactive Power	Sen VArs	VAr	-750 W to 750 W	1 W	0 W	37.5 W
Sensitive Single-Phase Power Factor	Sen Power Factor	W	-1 to 1	0.01	0	1
Sensitive Current Input 2 Magnitude	I Sen2 Mag (P345)	A	0 to 16A	0.01A	0A	1.2A

Table 31: Current loop outputs units and setting range

Note 1: For measurements marked with an asterisk, the internal refresh rate is nominally 1 s, others are 0.5 power system cycle or less.

Note 2: The polarity of Watts, Vars and power factor is affected by the Measurements Mode setting.

Note 3: These settings are for nominal 1A and 100/120 V versions only. For other nominal versions they need to be multiplied accordingly.

Note 4: For the P343/4/5/6, the IA/IB/IC Current magnitudes are IA-1 Magnitude, IB-1 Magnitude, IC-1 Magnitude.

1.2.28 System checks (check sync. function)

The P342/3/4/5/6 has a two stage Check Synchronization function that can be set independently.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
SYSTEM CHECKS GROUP 1				
VOLTAGE MONITORS	Sub-heading			
Live Voltage	32 V	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)	132 V (Vn=100/120 V) 528V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Minimum voltage setting above which a generator or busbar is recognized as being 'Live'.				
Dead Voltage	13 V	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)	132 V (Vn=100/120 V) 528 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Maximum voltage setting below which a generator or busbar is recognized as being 'Dead'.				
Gen Undervoltage	54 V	1 V (Vn=100/120V) 22 V (Vn=380/480 V)	132 V (Vn=100/120V) 528 V (Vn=380/480V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Undervoltage setting above which the generator voltage must be satisfied for the Check Sync. condition if V< is selected in the **CS Voltage Block** cell.				
Gen Overvoltage	130	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)	185 V (Vn=100/120 V) 740 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Overvoltage setting which the generator voltage must be satisfied for the Check Sync. condition if **V>** is selected in the **CS Voltage Block** cell.				
Bus Undervoltage	54 V (Vn=100/120 V) 216 V (Vn=380/480 V)	10 V (Vn=100/120 V) 40 V (Vn=380/480 V)	132 V (Vn=100/120 V) 528 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Undervoltage setting above which the busbar voltage must be satisfied for the Check Sync. condition if **V<** is selected in the **CS Voltage Block** cell..				
Bus Overvoltage	130 V (Vn=100/120 V) 520 V (Vn=380/480 V)	60V (Vn=100/120 V) 240V (Vn=380/480 V)	185V (Vn=100/120 V) 740V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Overvoltage setting below which the busbar voltage must be satisfied for the Check Sync. condition if **V>** is selected in the **CS Voltage Block** cell.				
CS Diff Voltage	6.5 V (Vn=100/120 V) 26 V (Vn=380/480 V)	1 V (Vn=100/120 V) 4 V (Vn=380/480 V)	132 V (Vn=100/120 V) 528 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Voltage magnitude difference setting between the generator and busbar volts below which the generator and bus voltage difference must be satisfied for the Check Sync. condition if selected in the **CS Voltage Block** cell.				
CS Voltage Block	V<	None, V<, V>, Vdiff>, V< and V>, V< and Vdiff>, V> and Vdiff>, V< V> Vdiff>		
Selects the undervoltage(V<), overvoltage (V>) and voltage difference (Vdiff>) voltage blocking options for the generator and bus voltages that must be satisfied in order for the Check Sync. conditions to be satisfied.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Gen Under Freq	49.5 Hz	45 Hz	65 Hz	0.01 Hz
Underfrequency setting for the generator. This setting only affects DDB 1347 Freq Low which indicates the generator frequency is lower than the **Gen Under Freq** setting.				
Gen Over Freq	50.5 Hz	45 Hz	65 Hz	0.01 Hz
Overfrequency setting for the generator. This setting only affects DDB 1348 Freq High which indicates the generator frequency is higher than the **Gen Over Freq** setting				
CHECK SYNC.	Sub-heading			
CS1 Status	Enabled	Disabled, Enabled		
Enables or disables the first stage check sync. element.				
CS1 Phase Angle	20.00°	5°	175°	0.01°
Maximum phase angle difference setting between the line and bus voltage for the first stage check sync. element phase angle criteria to be satisfied.				
CS1 Slip Control	Frequency	None, Timer Only, Frequency Only, Frequency + Timer		
Slip control method - slip frequency only, frequency + timer or timer only criteria to satisfy the first stage check sync. conditions. If slip control by timer or frequency + timer is selected, the combination of phase angle and timer settings determines an effective maximum slip frequency, calculated as: $\frac{2 \times A}{T \times 360}$ Hz. for Check Sync. 1, or where A = Phase angle setting (°) T = Slip timer setting (seconds) For example, with Check Sync. 1 Phase Angle setting 30° and Timer setting 3.3 sec, the "**slipping**" vector has to remain within ±30° of the reference vector for at least 3.3 seconds. Therefore a synch check output will not be given if the slip is greater than 2 x 30° in 3.3 seconds. Using the formula: 2 x 30 ÷ (3.3 x 360) = 0.0505 Hz (50.5 mHz). If Slip Control by Frequency + Timer is selected, for an output to be given, the slip frequency must be less than BOTH the set Slip Freq. value and the value determined by the Phase Angle and Timer settings. If Slip Control by Frequency, for an output to be given, the slip frequency must be less than the set Slip Freq. value setting only.				
CS1 Slip Freq.	50 mHz	10 mHz	1 Hz	10 mHz
Maximum frequency difference setting between the generator and bus voltage for the first stage check sync. element slip frequency to be satisfied.				
CS1 Slip Timer	1 s	0 s	99 s	0.01 s
Minimum operating time-delay setting for the first stage check sync. element.				
CS2 Status	Enabled	Disabled, Enabled		
Enable or disables the second stage check sync. element.				
CS2 Phase Angle	20.00°	5°	90°	0.01°
Maximum phase angle difference setting between the line and bus voltage for the second stage check sync. element phase angle criteria to be satisfied.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CS2 Slip Control	Frequency	None, Timer Only, Frequency Only, Frequency + Timer, Frequency + CB		
Slip control method - slip frequency only, frequency + timer or timer only criteria to satisfy the CS1 conditions. If Slip Control by Timer or Frequency + Timer is selected, the combination of Phase Angle and Timer settings determines an effective maximum slip frequency, calculated as: $\frac{A}{T \times 360}$ Hz. for Check Sync. 2, or where A = Phase angle setting (°) T = Slip timer setting (seconds) For Check Sync 2, with Phase Angle setting 10° and Timer setting 0.1 sec, the slipping vector has to remain within 10° of the reference vector, with the angle decreasing, for 0.1 sec. When the angle passes through zero and starts to increase, the synch check output is blocked. Therefore an output will not be given if slip is greater than 10° in 0.1 second. Using the formula: 10 ÷ (0.1 x 360) = 0.278 Hz (278 mHz). If Slip Control by Frequency + Timer is selected, for an output to be given, the slip frequency must be less than BOTH the set Slip Freq. value and the value determined by the Phase Angle and Timer settings. If Slip Control by Frequency, for an output to be given, the slip frequency must be less than the set Slip Freq. value setting only. The **Frequency + CB** (Frequency + CB Time Compensation) setting modifies the Check Sync. 2 function to take account of the circuit breaker closing time. By measuring the slip frequency, and using the **CB Close Time** setting as a reference, the relay will issue the close command so that the circuit breaker closes at the instant the slip angle is equal to the **CS2 phase angle** setting. Unlike Check Sync 1, Check Sync 2 only permits closure for decreasing angles of slip, therefore the circuit breaker should always close within the limits defined by Check Sync. 2.				
CS2 Slip Freq.	50 mHz	10 mHz	1 Hz	10 mHz
Slip frequency setting for the second stage check sync. element.				
CS2 Slip Timer	1 s	0 s	99 s	0.01 s
Second stage Check Sync. slip timer setting.				
SYSTEM SPLIT	Sub-heading			
SS Status	Enabled	Enabled, Disabled		
Enables or disables the system split function.				
SS Phase Angle	120°	90°	175°	0.01°
Maximum phase angle difference setting between the generator and bus voltage, which must be exceeded, for the System Split condition to be satisfied.				
SS Under V Block	Enabled	Enabled, Disabled		
Activates the system split undervoltage block criteria				
SS Undervoltage	54 V (Vn=100/120 V) 216 V (Vn=380/480 V)	10 V (Vn=100/120 V) 40 V (Vn=380/480 V)	132 V (Vn=100/120 V) 528 V (Vn=380/480 V)	0.5 V (Vn=100/120 V) 2 V (Vn=380/480 V)
Undervoltage setting above which the generator and bus voltage must be satisfied for the System Split condition.				
SS Timer	1 s	0 s	99 s	0.01 s
The System Split output remains set for as long as the System Split criteria are true, or for a minimum period equal to the System Split Timer setting, whichever is longer.				
CB Close Time	50 ms	0 s	0.5 s	1 ms
Circuit breaker closing time setting used in the second stage Check Sync criteria to compensate for the breaker closing time if selected.				

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Table 32: System checks settings

1.3 Control and support settings

The control and support settings are part of the main menu and are used to configure the relays global configuration. It includes the following submenu settings.

- Relay function configuration settings
- Open/close circuit breaker
- CT & VT ratio settings
- Reset LEDs
- Active protection setting group
- Password & language settings
- Circuit breaker control & monitoring settings
- Communications settings
- Measurement settings
- Event & fault record settings
- User interface settings
- Commissioning settings

1.3.1 System data

This menu provides information for the device and general status of the relay (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
SYSTEM DATA				
Language	English	English, Francais, Deutsch, Espanol or English, Francais, Deutsch, Русский (Russian) or English, Francais, 中文(Chinese)		N/A
The default language used by the device. Selectable as: English, French, German, Spanish (language order option 0) or English, French, German, Russian (Русский) (language order option 5) or English, French, Chinese (中文) (language order option C)				
Password	****			
Device password for level 1 or 2. If password level 1 is input then the access level is set as 1 and if password level 2 is input then the access level is set as 2.				
Sys. Fn. Links	0			1
Setting to allow the fixed function trip LED to be self resetting, 1= self reset, 0 = latched.				
Description	P343			
16 character relay description. Can be edited.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Plant Reference	MiCOM			
Plant description. Can be edited.				
Model Number	P343?11???0380M			
Relay model number.				
Serial Number	149188B			
Relay serial number.				
Frequency	50 Hz	50 Hz	60 Hz	10Hz
Relay set frequency. Settable as 50 or 60 Hz.				
Comms. Level				
Displays the conformance of the relay to the Courier Level 2 comms.				
Relay Address				
Sets the first rear port relay address.				
Plant Status	0000000000000000			
Displays the circuit breaker plant status for up to 8 circuit breakers. The P34x relay supports only a single circuit breaker configuration.				
Control Status	0000000000000000			
Not used.				
Active Group	1			
Displays the active settings group.				
CB Trip/Close	No Operation, Trip, Close			
Used to control trip or close a CB.				
Software Ref. 1	P343____1__380_A			
Software Ref. 2				
Displays the relay software version including protocol and relay model. Software Ref. 2 is displayed for relays with UCA2.0 protocol only and this will display the software version of the Ethernet card. UCA2.0 is not one of the protocols supported by P34x relays so Software Ref. 2 is blank.				
Opto I/P Status	0000000000000000			
This menu cell displays the status of the relay's opto-isolated inputs as a binary string, a '1' indicating an energized opto-isolated input and a '0' a de-energized one.				
Relay O/P Status	0000001000000000			
This menu cell displays the status of the relay's output contacts as a binary string, a '1' indicating an operated state and '0' a non-operated state.				
Alarm Status 1	00000000000000000000000000000000			
This menu cell displays the status of the first 32 alarms as a binary string, a '1' indicating an ON state and '0' an OFF state. Includes fixed and user settable alarms. See Data Type G96 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Opto I/P Status	0000000000000000			
Duplicate. Displays the status of opto inputs.				
Relay O/P Status	0000001000000000			
Duplicate. Displays the status of output contacts.				
Alarm Status 1	00000000000000000000000000000000			
Duplicate of Alarm Status 1 above.				
Alarm Status 2	00000000000000000000000000000000			
This menu cell displays the status of the second 32 alarms as a binary string, a '1' indicating an ON state and '0' an OFF state. See Data Type G128 in the Relay Menu Database document, *P34x/EN/MD* for details.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Alarm Status 3	00000000000000000000000000000000			
This menu cell displays the status of the third 32 alarms as a binary string, a '1' indicating an ON state and '0' an OFF state. Assigned specifically for platform alarms. See Data Type G228 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Access Level	0	0 = Read Some, 1 = Read All, 2 = Read All + Write Some, 3 = Read All + Write All		1
Displays the current access level. Level 0 - No password required - Read access to Security features, Model Number, Serial Number, S/W version, Description, Plant reference, Security code (UI Only), Encryption key (UI Only), User Banner and security related cells (BF12 - BF14). Level 1 - Password 1, 2 or 3 required - Read access to all data and settings. Write access to Primary/Secondary selector, Level 1 password setting, Password reset cell and log extraction cells (record selector) Level 2 - Password 2 or 3 required - Read access to all data and settings. Write access to Reset demands and counters and Level 2 password setting. Level 3 - Password 3 required - Read access to all data and settings. Write access to All settings including Level 3 password setting, PSL, IED Config, Security settings (port disabling etc.)				
Password Level 1	Blank	ASCII 33 to 122		
Allows user to change password level 1. (8 characters)				
Password Level 2	AAAA	ASCII 33 to 122		
Allows user to change password level 2. (8 characters)				
Password Level 3	AAAA	ASCII 33 to 122		
Allows user to change password level 3. (8 characters)				
Security Feature	1	1		
Displays the level of cyber security implemented, 1 = phase 1.				
Password	0	ASCII 33 to 122		
Encrypted password entry cell. Not visible via UI				
Password Level 1	0	ASCII 33 to 122		
Allows user to change Encrypted password level 1. (8 characters) Not visible via UI				
Password Level 2	0	ASCII 33 to 122		
Allows user to change Encrypted password level 2. (8 characters) Not visible via UI				
Password Level 3	0	ASCII 33 to 122		
Allows user to change Encrypted password level 3. (8 characters) Not visible via UI				

Table 33: System data

1.3.2 View records

This menu provides information on fault and maintenance records. The relay will record the last 5 fault records and the last 10 maintenance records (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VIEW RECORDS				
Select Event	0	0	511	
Setting range from 0 to 511. This selects the required event record from the possible 512 that may be stored. A value of 0 corresponds to the latest event and so on.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Menu Cell Ref	(From record)	Latched alarm active, Latched alarm inactive, Self reset alarm active, Self reset alarm inactive, Relay contact event, Opto-isolated input event, Protection event, General event, Fault record event, Maintenance record event		
Indicates the type of event.				
Time and Date	Data			
Time & Date Stamp for the event given by the internal Real Time Clock.				
Event text	Data.			
Up to 32 Character description of the Event. See event sheet in the Relay Menu Database document, *P34x/EN/MD* or the Measurements and Recording chapter, *P34x/EN MR* for details.				
Event Value	Data.			
32 bit binary string indicating ON or OFF (1 or 0) status of relay contact or opto input or alarm or protection event depending on event type. Unsigned integer is used for maintenance records. See event sheet in the Relay Menu Database document, *P34x/EN/MD* or the Measurements and Recording chapter, *P34x/EN MR* for details.				
Select Fault	0	0	19	1
Setting range from 0 to 19. This selects the required fault record from the possible 20 that may be stored. A value of 0 corresponds to the latest fault and so on.				
Faulted Phase	00000000			
Displays the faulted phase as a binary string, bits 0 – 8 = Start A/B/C/N Trip A/B/C/N.				
Start elements 1	00000000000000000000000000000000			
32 bit binary string gives status of first 32 start signals. See Data Type G84 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Start elements 2	00000000000000000000000000000000			
32 bit binary string gives status of second 32 start signals. See Data Type G107 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Start elements 3	00000000000000000000000000000000			
32 bit binary string gives status of third 32 start signals. See Data Type G129 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Start elements 4	00000000000000000000000000000000			
32 bit binary string gives status of fourth 32 start signals. See Data Type G131 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Trip elements 1	00000000000000000000000000000000			
32 bit binary string gives status of first 32 trip signals. See Data Type G85 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Trip elements 2	00000000000000000000000000000000			
32 bit binary string gives status of second 32 trip signals. See Data Type G86 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Trip elements 3	00000000000000000000000000000000			
32 bit binary string gives status of third 32 trip signals. See Data Type G130 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Trip elements 4	00000000000000000000000000000000			
32 bit binary string gives status of fourth 32 trip signals. See Data Type G132 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Fault Alarms	0000001000000000			
32 bit binary string gives status of fault alarm signals. See Data Type G87 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Fault Alarms2	0000001000000000			
32 bit binary string gives status of second 32 fault alarm signals. See Data Type G89 in the Relay Menu Database document, *P34x/EN/MD* for details.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Fault Time	Data.			
Fault time and date.				
Active Group	Data.			
Active setting group 1-4.				
System Frequency	Data			
System frequency.				
SystemFrequency2	Data			
System frequency 2. (P348 only). In the P348 System Frequency 2 is measured from IA-2/IB-2/IC-2 current inputs (normally connected to the stator) and the System frequency is measured from IA-1/IB-1/IC-1 (normally connected to the rotor). In other P34x models the System Frequency is measured from VA/VB/VC or IA-1/IB-1/IC-1 (normally connected to the stator).				
Fault Duration				
Fault duration. Time from the start or trip until the undercurrent elements indicate the CB is open.				
CB Operate Time	Data.			
CB operating time. Time from protection trip to undercurrent elements indicating the CB is open.				
Relay Trip Time	Data.			
Relay trip time. Time from protection start to protection trip.				
The following cells provide measurement information of the fault: (P341-6): System Frequency, IA/IA-1, IB/IB-1, IC/IC-1, VAB, VBC, VCA, VAN, VBN, VCN, IA-2, IB-2, IC-2, IA Differential, IB Differential, IC Differential, IA Diff PU, IB Diff PU, IC Diff PU, IA Diff 2H, IB Diff 2H, IC Diff 2H, IA Diff 5H, IB Diff 5H, IC Diff 5H, VN/VN1 Measured, VN2 Measured, VN Derived, IN Measured, I Sensitive1, I Sensitive2, IREF Diff, IREF Bias, I2, V2, 3 Phase Watts, 3 Phase VARs, 3Ph Power Factor, Sen Watts, Sen VArs, Sen Power Factor, RTD 1-10, CLIO Input 1-4, df/dt, 64S V Magnitude, 64S I Magnitude, 64S Rprimary, 64R CL Input, 64R R Fault, IA Peak Mag, IB Peak Mag, IC Peak Mag, I^2t Phase A, I^2t Phase B, I^2t Phase C. P348 only: System frequency, System Frequency 2, IA-1 RMS, IB-1 RMS, IC-1 RMS, VA-1 RMS, VB-1 RMS, VC-1 RMS, IA-2 RMS, IB-2 RMS, IC-2 RMS, VA-1 Peak, VB-1 Peak, VC-1 Peak, VN-1 Derived Peak, VA-2 RMS, VB-2 RMS, VC-2 RMS, VN-1 Derived RMS, I2 CT2 Peak, I2 CT2 RMS, CLIO Input 1-4, IA-1 Peak, IB-1 Peak, IC-1 Peak, IA-2 Peak, IB-2 Peak, IC-2 Peak.				
Select Maint	0	0	9	1
Setting range from 0 to 9. This selects the required maintenance report from the possible 10 that may be stored. A value of 0 corresponds to the latest report and so on.				
Maint Text	Data.			
Up to 32 Character description of the occurrence. See the Measurements and Recording chapter, *P34x/EN MR* for details.				
Maint Type	Data.			
Maintenance record fault type. This will be a number defining the fault type.				
Maint Data	0	0	4	1
Error code associated with the failure found by the self monitoring. The Maint Type and Data cells are numbers representative of the occurrence. They form a specific error code which should be quoted in any related correspondence to Report Data.				
Evt Iface Source	Data.			
Interface on which the event was logged.				
Evt Access Level	Data.			
Any security event that indicates that it came from an interface action, such as disabling a port, will also record the access level of the interface that initiated the event. This will be recorded in the 'Event State' field of the event.				

ST

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Evt Extra Info	Data.			
Each event will have a unique event id. The event id is a 32 bit unsigned integer that is incremented for each new event record and is stored in the record in battery-backed memory (BBRAM). The current event id must be non-volatile so as to preserve it during power cycles, thus it too will be stored in BBRAM. The event id will wrap back to zero when it reaches its maximum (4,294,967,295). The event id will be used by PC based utilities when organising extracted logs from IED's.				
Reset Indication	No	No, Yes		N/A
Resets latched leds and latched relay contacts provided the relevant protection element has reset.				

Table 34: View records settings

1.3.3 Measurements 1

This menu provides measurement information (P342-6/8). P348 Peak measurements are the maximum Peak values over the previous 1s.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 1				
IA / IA-1 Magnitude	Data. IA. P342/ IA-1. P343-6			
IA / IA-1 Phase Angle	Data. IA. P342/ IA-1. P343-6			
IB / IB-1 Magnitude	Data. IA. P342/ IA-1. P343-6			
IC / IB-1 Phase Angle	Data. IA. P342/ IA-1. P343-6			
IC / IC-1 Magnitude	Data. IA. P342/ IA-1. P343-6			
IC / IC-1 Phase Angle	Data. IA. P342/ IA-1. P343-6			
IN Measured Mag	Data. P342-6			
IN Measured Angle	Data. P342-6			
IN / IN-1 Derived Mag	Data. IN = IA+IB+IC. P342/ IN-1 = IA-1+IB-1+IC-1. P343-6			
IN Derived Angle	Data. P342-6			
I Sen1 Magnitude	Data. P342-6			
I Sen1 Angle	Data. P342-6			
I1 Magnitude	Data. Positive sequence current. P342-6			
I2 magnitude	Data. Negative sequence current. P342-6			
I0 Magnitude	Data. Zero sequence current. P342-6			
IA RMS	Data. P342-6			
IB RMS	Data. P342-6			
IC RMS	Data. P342-6			
IA-1 RMS	Data. P348			
IB-1 RMS	Data. P348			
IC-1 RMS	Data. P348			
IN-2 Derived Mag	Data. IN-2 = IA-2+IB-2+IC-2. P343-6			
VAB Magnitude	Data. P342-6			
VAB Phase Angle	Data. P342-6			
VBC Magnitude	Data. P342-6			
VBC Phase Angle	Data. P342-6			
VCA Magnitude	Data. P342-6			
VCA Phase Angle	Data. P342-6			
VAN Magnitude	Data. P342-6			
VAN Phase Angle	Data. P342-6			
VBN Magnitude	Data. P342-6			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VBN Phase Angle	Data. P342-6			
VCN Magnitude	Data. P342-6			
VCN Phase Angle	Data. P342-6			
VN / VN1 Measured Mag	Data. VN.P342/ VNI. P342-6			
VN / VN1 Measured Ang	Data. VN.P342/ VNI. P342-6			
VN Derived Mag	Data. VN = VA+VB+VC. P342-6			
V1 Magnitude	Data. Positive sequence voltage. P342-6			
V2 Magnitude	Data. Negative sequence voltage. P342-6			
V0 Magnitude	Data. Zero sequence voltage. P342-6			
VAN RMS	Data. P342-6			
VBN RMS	Data. P342-6			
VCN RMS	Data. P342-6			
I Sen2 Magnitude	Data. P345			
I Sen2 Angle	Data. P345			
Frequency	Data. Stator frequency P342-6, rotor frequency P348			
Frequency2	Data. Stator frequency P348			
I1 Magnitude	Data. Positive sequence current. P342-6			
I1 Phase Angle	P342-6			
I2 Magnitude	Data. Negative sequence current. P342-6			
I2 Phase Angle	Data. P342-6			
I0 Magnitude	Data. Zero sequence current. P342-6			
I0 Phase Angle	Data. P342-6			
V1 Magnitude	Data. Positive sequence voltage. P342-6			
V1 Phase Angle	Data. P342-6			
V2 Magnitude	Data. Negative sequence voltage. P342-6			
V2 Phase Angle	Data. P342-6			
V0 Magnitude	Data. Zero sequence voltage. P342-6			
V0 Phase Angle	Data. P342-6			
VN2 Measured Mag	Data. P344/5. P342-6			
VN2 Measured Ang	Data. P344/5. P342-6			
C/S Voltage Mag	Data. P342-6			
C/S Voltage Ang	Data. P342-6			
CS Gen-Bus Mag	Data. P342-6			
CS Gen-Bus Angle	Data. P342-6			
Slip Frequency	Data. P342-6			
CS Frequency	Data. P342-6			
IA-2 RMS	Data. P348			
IB-2 RMS	Data. P348			
IC-2 RMS	Data. P348			
I2 CT2 RMS	Data. P348			
IA-1 Peak	Data. P348			
IB-1 Peak	Data. P348			
IC-1 Peak	Data. P348			
IA-2 Peak	Data. P348			
IB-2 Peak	Data. P348			
IC-2 Peak	Data. P348			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
I2 CT2 Peak	Data. P348			
VA-1 RMS	Data. P348			
VB-1 RMS	Data. P348			
VC-1 RMS	Data. P348			
VN-1 Derived RMS	Data. P348			
VA-1 Peak	Data. P348			
VB-1 Peak	Data. P348			
VC-1 Peak	Data. P348			
VN-1 DerivedPeak	Data. P348			
VAB-1 RMS	Data. P348			
VBC-1 RMS	Data. P348			
VCA-1 RMS	Data. P348			
VAB-1 Peak	Data. P348			
VBC-1 Peak	Data. P348			
VCA-1 Peak	Data. P348			
VA-2 RMS	Data. P348			
VB-2 RMS	Data. P348			
VC-2 RMS	Data. P348			
IN-2 Derived RMS	Data. P348			

Table 35: Measurement 1 menu

1.3.4 Measurements 2

This menu provides measurement information (P342-6).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 2				
A Phase Watts	Data			
B Phase Watts	Data			
C Phase Watts	Data			
A Phase VARs	Data			
B Phase VARs	Data			
C Phase VARs	Data			
A Phase VA	Data			
B Phase VA	Data			
C Phase VA	Data			
3 Phase Watts	Data			
3 Phase VARs	Data			
3 Phase VA	Data			
NPS Power S2	Data. Negative sequence power, S2 =V2xI2			
3Ph Power Factor	Data			
APh Power Factor	Data			
BPh Power Factor	Data			
CPh Power Factor	Data			
3Ph WHours Fwd	Data			
3Ph WHours Rev	Data			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
3Ph VArHours Fwd	Data			
3Ph VArHours Rev	Data			
3Ph W Fix Demand	Data			
3Ph VAr Fix Demand	Data			
IA Fixed Demand	Data			
IB Fixed Demand	Data			
IC Fixed Demand	Data			
3Ph W Roll Demand	Data			
3Ph VAr Roll Demand	Data			
IA Roll Demand	Data			
IB Roll Demand	Data			
IC Roll Demand	Data			
3Ph W Peak Demand	Data			
3Ph VAr Peak Demand	Data			
IA Peak Demand	Data			
IB Peak Demand	Data			
IC Peak Demand	Data			
Reset Demand	No	No, Yes		N/A
Reset demand measurements command. Can be used to reset the fixed, rolling and peak demand value measurements to 0.				
NPS Power S2CTS2	Negative sequence power, S2 =V2xI2.			

Table 36: Measurement 2 menu

1.3.5 Measurements 3

This menu provides measurement information (P342-6).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 3				
IA-2 Magnitude	Data. P343, 4, 5, 6			
IA-2 Phase Angle	Data. P343, 4, 5, 6			
IB-2 Magnitude	Data. P343, 4, 5, 6			
IB-1 Phase Angle	Data. P343, 4, 5, 6			
IC-2 Magnitude	Data. P343, 4, 5, 6			
IC-2 Phase Angle	Data. P343, 4, 5, 6			
IA Differential	Data. P343, 4, 5, 6. Generator Diff phase A differential current			
IB Differential	Data. P343, 4, 5, 6. Generator Diff phase B differential current			
IC Differential	Data. P343, 4, 5, 6. Generator Diff phase C differential current			
IA Bias	Data. P343, 4, 5, 6. Generator Diff phase A bias current			
IB Bias	Data. P343, 4, 5, 6. Generator Diff phase A bias current			
IC Bias	Data. P343,4,5,6. Generator Diff phase A bias current			
IREF Diff	Data. Restricted earth fault differential current			
IREF Bias	Data. Restricted earth fault bias current			
VN 3rd harmonic	Data. 3rd harmonic neutral voltage used by 100% stator earth fault. P343, 4, 5			
NPS Thermal	Data. Negative phase sequence thermal state			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Reset NPS Thermal	No	No, Yes		N/A
Reset negative phase sequence thermal state command. Resets NPS Thermal state to 0.				
RTD 1	Data			
RTD 2-10	Data			
RTD Open Cct	00000000			
This menu cell displays the status of the eight RTDs as a binary string, 0 = No Open Circuit, 1 = Open Circuit. The Open Cct alarms are latched.				
RTD Short Cct	00000000			
This menu cell displays the status of the eight RTDs as a binary string, 0 = No Short Circuit, 1 = Short Circuit. The Short Cct alarms are latched.				
RTD Data Error	00000000			
This menu cell displays the status of the eight RTDs as a binary string, 0 = No Data Error, 1 = Data Error. The Data Error alarms are latched.				
Reset RTD Flags	No	No, Yes		N/A
Reset RTD alarms command. Resets latched RTD Open Cct, Short Cct, Data Error alarms.				
Sen Watts	Data			
Sen VArs	Data			
Sen Power Factor	Data			
Thermal Overload	Data. Thermal state			
Reset Thermal O/L	No	No, Yes		N/A
Reset thermal overload command. Resets thermal state to 0.				
CLIO Input 1	Data. Current loop (transducer) input 1			
CLIO Input 2	Data. Current loop (transducer) input 2			
CLIO Input 3	Data. Current loop (transducer) input 3			
CLIO Input 4	Data. Current loop (transducer) input 4			
F Band1 Time(s)	Data. Turbine abnormal frequency accumulated time in frequency band 1			
Reset Freq Band1	No	No, Yes		N/A
Reset frequency band 1 command. Resets accumulated time of frequency band 1 to 0 s.				
F Band2-6 Time(s)	Data. Turbine abnormal frequency, accumulated time in frequency band 2-6			
Reset Freq Band2-6	No	No, Yes		N/A
Reset frequency band 2-6 command. Resets accumulated time of frequency band 2-6 to 0 s.				
Reset Freq Bands	No	No, Yes		N/A
Reset frequency bands command. Resets accumulated time of all frequency bands (1-6) to 0 s.				
df/dt	Data. Rate of change of frequency			
Volts/Hz	Data			
64S V Magnitude	Data. 100% stator earth fault 20 Hz voltage. P345			
64S I Magnitude	Data. 100% stator earth fault 20 Hz current. P345			
64S I Angle	Data. 100% stator earth fault 20 Hz current angle with respect to the voltage. P345			
64S R secondary	Data. 100% stator earth fault secondary resistance. P345			
64S R primary	Data. 100% stator earth fault primary resistance. P345			
64R CL Input	Data. Rotor earth fault current loop input current (0-20 mA)			
64R R Fault	Data. Rotor earth fault primary resistance from current loop input connected to P391			
IA Diff PU	Data. Transformer Diff phase A per unit differential current			
IB Diff PU	Data. Transformer Diff phase B per unit differential current			
IC Diff PU	Data. Transformer Diff phase C per unit differential current			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
IA Bias PU	Data. Transformer Diff phase A per unit bias current			
IB Bias PU	Data. Transformer Diff phase A per unit bias current			
IC Bias PU	Data. Transformer Diff phase A per unit bias current			
IA Diff 2H	Data. Transformer Diff phase A 2nd harmonic current			
IB Diff 2H	Data. Transformer Diff phase B 2nd harmonic current			
IC Diff 2H	Data. Transformer Diff phase C 2nd harmonic current			
IA Diff 5H	Data. Transformer Diff phase A 5th harmonic current			
IB Diff 5H	Data. Transformer Diff phase B 5th harmonic current			
IC Diff 5H	Data. Transformer Diff phase C 5th harmonic current			
CT2 I1 Mag	Data. P343, 4, 5, 6			
CT2 I1 Angle	Data. P343, 4, 5, 6			
CT2 I2 Mag	Data. P343, 4, 5, 6			
CT2 I2 Angle	Data. P343, 4, 5, 6			
CT2 I0 Mag	Data. P343, 4, 5, 6			
CT2 I0 Angle	Data. P343, 4, 5, 6			
CT1 I2/I1	Data. P343, 4, 5, 6			
CT2 I2/I1	Data. P343, 4, 5, 6			
ZA Mag	Data. A Phase impedance			

Table 37: Measurement 3 menu

1.3.6 Measurements 4

This menu provides measurement information (P342-6).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 4				
Hot Spot T	Data. Hot spot temperature			
Top Oil T	Data. Top oil temperature			
Reset Thermal	No	No, Yes		N/A
Reset thermal overload command. Resets thermal state to 0.				
Ambient T	Data. Ambient temperature			
TOL Pretrip left	Data. Top oil (TOL) time left to trip			
LOL status	Data. Accumulated loss of life (LOL) measurement in hours			
Reset LOL	No	No, Yes		N/A
Reset loss of life LOL command. Resets LOL to the value set in the setting of ‘Reset Life Hours’.				
Rate of LOL	Data. Rate of loss of life (LOL) in %.			
LOL Ageing Fact	Data. Ageing acceleration factor (FAA)			
Lres at Design T	Data. Residual life at reference hottest spot temperature			
FAA,m	Data. Mean ageing acceleration factor (FAA,m)			
Lres at FAA,m	Data. Residual life in hours at FAA,m (Lres(FAA,m))			
Counter 1	Data. Counter 1 value			
Counter 2-16	Data. Counter 2-16 value			
Reset Counter1	No	No, Yes		N/A
Reset Counter2-16	No	No, Yes		N/A

Table 38: Measurement 4 menu

1.3.7 Circuit breaker condition

The relays include measurements to monitor the CB condition (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CB CONDITION				
CB Operations	Data. Number of CB trip operations.			
Total IA Broken	Data. Accumulated broken current for A phase protection trip.			
Total IB Broken	Data. Accumulated broken current for B phase protection trip.			
Total IC Broken	Data. Accumulated broken current for C phase protection trip.			
CB Operate Time	Data. CB operating time = time from protection trip to undercurrent elements indicating the CB is open.			
CB Close Time	Data. Circuit breaker close time = time from protection close to undercurrent elements indicating the CB is closed.			
Reset CB Data	No	No, Yes		N/A
Reset CB Data command. Resets CB Operations and Total IA/IB/IC broken current counters to 0.				

Table 39: Circuit breaker condition menu

1.3.8 Circuit breaker control

The relays include settings to reset CB condition monitoring lockout alarms and set the type of CB auxiliary contacts that will be used to indicate the CB position (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CB CONTROL				
CB Control by	Disabled	Disabled,Local, Remote, Local+Remote, Opto, Opto+local, Opto+Remote, Opto+Rem+local		
This Setting selects the type of circuit breaker control that be used in the logic				
Close Pulse Time	0.5 s	0.1 s	5 s	0.01 s
Defines the duration of the close pulse.				
Trip Pulse Time	0.5 s	0.1 s	5 s	0.01
Defines the duration of the trip pulse.				
Man Close Delay	10 s	0.01 s	600 s	0.01 s
This defines the delay time before the close pulse is executed.				
CB Healthy Time	5 s	0.01 s	9999 s	0.01 s
A settable time delay included for manual closure with this circuit breaker check. If the circuit breaker does not indicate a healthy condition in this time period following a close command then the relay will lockout and alarm.				
Sys Check Time	5 s	0.01 s	9999 s	0.01 s
A user settable time delay is included for manual closure with check synchronizing. If the check sync. criteria are not satisfied in this time period following a close command the relay will lockout and alarm.				
Lockout Reset	No	No, Yes		N/A
Reset Lockout command. Can be used to reset the CB condition monitoring lockout alarms.				
Reset Lockout By	CB Close	User Interface, CB Close		N/A
Setting to determines if a lockout condition will be reset by a manual circuit breaker close command or via the user interface.				
Man Close RstDly	5 s	0.01 s	600 s	0.01 s
The manual close reset time. A lockout is automatically reset following a manual close after this time delay.				

ST

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CB Status Input	None	None, 52A, 52B, Both 52A and 52B		N/A
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic.				

Table 40: Circuit breaker condition menu

1.3.9 Date and time

The date and time displays the date and time as well as the battery condition (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DATE AND TIME				
Date/Time	Data			
Displays the relay's current date and time.				
IRIG-B Sync.	Disabled	Disabled, Enabled		N/A
Enables or disables the IRIG-B time synchronization.				
IRIG-B Status	Data	Card not fitted/Card failed/ Signal healthy/No signal		N/A
Displays the status of IRIG-B.				
Battery Status	Dead or Healthy			
Displays whether the battery is healthy or not.				
Battery Alarm	Enabled	Disabled, Enabled		N/A
Enables or disables battery alarm. The battery alarm needs to be disabled when a battery is removed or not used.				
SNTP Status	Data	Disabled/Trying Server1/ Trying Server 2/Server 1 OK/Server 2 OK/No response/No Valid Clock		N/A
Displays information about the SNTP time synchronization status				
LocalTime Enable	Disabled	Disabled, Fixed, Flexible		N/A
Setting to turn on/off local time adjustments. Disabled - No local time zone will be maintained. Time synchronization from any interface will be used to directly set the master clock and all displayed (or read) times on all interfaces will be based on the master clock with no adjustment. Fixed - A local time zone adjustment can be defined using the LocalTime offset setting and all interfaces will use local time except SNTP time synchronization and IEC 61850 timestamps. Flexible - A local time zone adjustment can be defined using the LocalTime offset setting and each interface can be assigned to the UTC zone or local time zone with the exception of the local interfaces which will always be in the local time zone and IEC 61850/SNTP which will always be in the UTC zone.				
LocalTime Offset	0 min	-720 min	720 min	1 min
Setting to specify an offset of -12 to +12 hrs in 15 minute intervals for local time zone. This adjustment is applied to the time based on the master clock which is UTC/GMT				
DST Enable	Disabled	Disabled, Enabled		N/A
Setting to turn on/off daylight saving time adjustment to local time.				
DST Offset	60 min	30 min	60 min	30 min
Setting to specify daylight saving offset which will be used for the time adjustment to local time.				
DST Start	Last	First, Second, Third, Fourth, Last		N/A
Setting to specify the week of the month in which daylight saving time adjustment starts				
DST Start Day	Sunday	Sunday, Monday, Tuesday, Wednesday, Thursday, Friday, Saturday		N/A
Setting to specify the day of the week in which daylight saving time adjustment starts				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DST Start Month	March	January, February, March, April, May, June, July, August, September, November, December		N/A
Setting to specify the month in which daylight saving time adjustment starts				
DST Start Mins	60 min	0 min	1425 min	15 min
Setting to specify the time of day in which daylight saving time adjustment starts. This is set relative to 00:00 hrs on the selected day when time adjustment is to start.				
DST End	Last	First, Second, Third, Fourth, Last		N/A
Setting to specify the week of the month in which daylight saving time adjustment ends.				
DST End Day	Sunday	Sunday, Monday, Tuesday, Wednesday, Thursday, Friday, Saturday		N/A
Setting to specify the day of the week in which daylight saving time adjustment ends				
DST End Month	October	January, February, March, April, May, June, July, August, September, November, December		N/A
Setting to specify the month in which daylight saving time adjustment ends				
DST End Mins	60 min	0 min	1425 min	15 min
Setting to specify the time of day in which daylight saving time adjustment ends. This is set relative to 00:00 hrs on the selected day when time adjustment is to end.				
RP1 Time Zone	Local	UTC/Local		N/A
Setting for the rear port 1 interface to specify if time synchronization received will be local or universal time coordinated.				
RP2 Time Zone	Local	UTC/Local		N/A
Setting for the rear port 2 interface to specify if time synchronization received will be local or universal time coordinated.				
Tunnel Time Zone	Local	UTC/Local		N/A
Setting to specify if time synchronization received will be local or universal time coordinate when 'tunneling' courier protocol over Ethernet.				

Table 41: Date and time menu

1.3.10 CT and VT ratios

The CT AND VT RATIOS column contains the settings for defining the main system current and voltage transformers, such as the primary and secondary voltage and current ratings (P342-6/8).

The P348 has an IEC 61850-9-2 LE Ethernet port to connect to Non Conventional Instrument Transformers (NCITs) via a merging unit. The IEC 61850-9-2 LE input provides primary values of current and voltage to the relay. However, the settings in the P34x relay are in secondary values and are multiplied by the CT/VT ratios to show primary setting values. Therefore, the Primary/Secondary CT/VT settings in the P348 should be selected in a similar way as for conventional CTs and VTs and selected so that the protection settings required are within the setting range of the protection functions used.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CT AND VT RATIOS				
Main VT Primary	110.0 V	100 V	1000 kV	1 V
Main voltage transformer input, primary voltage setting. (P342-6/8)				
Main VT Sec'y	110.0 V	80 V	140 V	1 V
Main transformer input, secondary voltage setting. (P342-6/8)				
C/S VT Primary	110.0 V	100 V	1000 kV	1 V
Check sync. voltage transformer input primary voltage setting. (P345)				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
C/S VT Sec'y	110.0 V	80 V	140 V	1 V
Check sync. voltage transformer input secondary voltage setting. (P345)				
VN1 Primary	110.0 V	100 V	1000 kV	1 V
VN1 input, primary voltage setting. VN1 is the neutral voltage input. (P342-6)				
VN1 Secondary	110.0 V	80 V	140 V	1 V
VN1 input, secondary voltage setting.				
VN2 Primary	110.0 V	100 V	1000 kV	1 V
VN2 input, primary voltage setting. VN2 is the 2nd neutral voltage input. (P344/5)				
VN2 Secondary	110.0 V	80 V	140 V	1 V
VN2 input, secondary voltage setting. (P344/5)				
Ph CT Polarity / Ph CT1 Polarity	Standard	Standard/Inverted		
Phase CT (P342) or Phase CT1 (P343-6/8) polarity selection. This setting can be used to easily reverse the CT polarity for wiring errors.				
Phase CT Primary / Phase CT1 Primary	300 A	1 A	60 kA	1 A
Phase CT (P342) or Phase CT1 (P343-6/8) input, primary current rating setting.				
Phase CT Sec'y / Phase CT1 Sec'y	1.000 A	1 A	5 A	4 A
Phase CT (P342) or Phase CT1 (P343-6/8) input, secondary current rating setting.				
Ph CT2 Polarity	Standard	Standard/Inverted		
Phase CT2 polarity selection. This setting can be used to easily reverse the CT polarity for wiring errors. (P343-6/8)				
Phase CT2 Primary	300 A	1 A	60 kA	1 A
Phase CT2 input, primary current rating setting. (P343-6/8)				
Phase CT2 Sec'y	1.000 A	1 A	5 A	4 A
Phase CT2 input, secondary current rating setting. (P343-6/8)				
E/F CT Polarity	Standard	Standard, Inverted		
Earth fault current transformer polarity selection. This setting can be used to easily reverse the CT polarity for wiring errors. (P342-6)				
E/F CT Primary	1.000 A	1 A	60 kA	1 A
Earth fault current transformer input, primary current rating setting. (P342-6)				
E/F CT Secondary	1.000 A	1 A	5 A	4 A
Earth fault current transformer input, secondary current rating setting. (P342-6)				
Isen CT Polarity	Standard	Standard, Inverted		
Sensitive Current transformer polarity selection. This setting can be used to easily reverse the CT polarity for wiring errors. (P342-6)				
Isen CT Primary	1.000 A	1 A	60 kA	1 A
Sensitive current transformer input, primary current rating setting. (P342-6)				
Isen CT Secondary	1.000 A	1 A	5 A	4 A
Sensitive current transformer input, secondary current rating setting. (P342-6)				

Table 42: CT and VT ratio settings

1.3.11 Record control

It is possible to disable the reporting of events from all interfaces that support setting changes. The settings that control the reporting of various types of events are in the Record Control column (P342-6/8). The effect of setting each to disabled is as follows:

Menu text	Default setting	Available settings
RECORD CONTROL		
Clear Events	No	No or Yes
Selecting **Yes** will cause the existing event log to be cleared and an event will be generated indicating that the events have been erased.		
Clear Faults	No	No or Yes
Selecting **Yes** will cause the existing fault records to be erased from the relay.		
Clear Maint.	No	No or Yes
Selecting **Yes** will cause the existing maintenance records to be erased from the relay.		
Alarm Event	Enabled	Disabled, Enabled
Disabling this setting means that no event will be generated for all alarms.		
Relay O/P Event	Enabled	Disabled, Enabled
Disabling this setting means that no event will be generated for any change in relay output contact state.		
Opto Input Event	Enabled	Disabled, Enabled
Disabling this setting means that no event will be generated for any change in logic input state.		
General Event	Enabled	Disabled, Enabled
Disabling this setting means that no General Events will be generated. See event record sheet in the Relay Menu Database document, *P34x/EN MD* for list of general events.		
Fault Rec Event	Enabled	Disabled, Enabled
Disabling this setting means that no event will be generated for any fault that produces a fault record.		
Maint. Rec Event	Enabled	Disabled, Enabled
Disabling this setting means that no event will be generated for any maintenance records.		
Clear Dist Recs	No	No, Yes
Command to clear disturbance record memory.		
Protection Event	Enabled	Disabled, Enabled
Disabling this setting means that no event will be generated for any operation of the protection elements.		
DDB 31 - 0	11111111111111111111111111111111	
32 bit setting to enable or disable the event recording for DDBs 0-31. For each bit 1 = event recording Enabled, 0 = event recording Disabled.		
DDB 2047 - 2016	11111111111111111111111111111111	
32 bit setting to enable or disable the event recording for DDBs 2047 - 2016. For each bit 1 = event recording Enabled, 0 = event recording Disabled. There are similar cells showing 32 bit binary strings for all DDBs from 0 - 2047. The first and last 32 bit binary strings only are shown here.		

Table 43: Record control menu

1.3.12 Disturbance recorder settings

The disturbance recorder settings include the record duration and trigger position, selection of analog and digital signals to record, and the signal sources that trigger the recording (P342-6/8). Each disturbance record consists of a maximum of 9/12/13/15/15 analog data channels for P342/3/4/5/8 and thirty-two digital data channels.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DISTURB RECORDER				
Duration	1.5 s	0.1 s	10.5 s	0.01 s
Overall recording time setting.				
Trigger Position	33.3%	0%	100%	0.1%
Trigger point setting as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Trigger Mode	Single	Single, Extended		
If set to single mode, if a further trigger occurs whilst a recording is taking place, the recorder will ignore the trigger. However, if this has been set to **Extended**, the post trigger timer will be reset to zero, thereby extending the recording time.				
Analog. Channel 1	VA (P342-6), VA-1 (P348)	P341-6: Unused, VA, VB, VC, VN1, IA-1, IB-1, IC-1, IN, I Sensitive1, IA-2, IB-2, IC-2, VN2, I Sensitive2, V64S, I64S, Frequency, 64R CL Input Raw (unfiltered), 64R R Fault Raw (unfiltered), 64R R Fault (filtered), C/S voltage, 3 Phase Watts, 3 Phase VArs, 1Ph Sen Watts, 1Ph Sen VArs, 3Ph Sen Watts, 3Ph Sen VArs. P348 only: Unused, VA-1, VB-1, VC-1, VN-1 Derived, VAB-1, VBC-1, VCA-1, VA-2, VB-2, VC-2, IA-1, IB-1, IC-1, IA-2, IB-2, IC-2, I2 CT2, VA-1 RMS, VB-1 RMS, VC-1 RMS, VN-1 Derived RMS, VAB-1 RMS, VBC-1 RMS, VCA-1 RMS, IA-1 RMS, IB-1 RMS, IC-1 RMS, IA-2 RMS, IB-2 RMS, IC-2 RMS, I2 CTS RMS, IN-2 Derived RMS, Frequency, Frequency 2.		
Selects any available analog input to be assigned to this channel.				
Analog. Channel 2	VB (P342-6), VB-1 (P348)	As above.		
Analog. Channel 3	VC (P342-6), VC-1 (P348)	As above.		
Analog. Channel 4	VN1 (P342-6), VN-1 Derived (P348)	As above.		
Analog. Channel 5	IA-1 (P342-8)	As above.		
Analog. Channel 6	IB-1 (P342-8)	As above.		
Analog. Channel 7	IC-1 (P342-8)	As above.		
Analog. Channel 8	I Sensitive (P342-6), IA-2 (P348)	As above.		
Analog. Channel 9	IN (P342-6), IB-2 (P348)	As above.		
Analog. Channel 10	IA-2 (P343-6), IC-2 (P348)	As above.		
Analog. Channel 11	IB-2 (P343-6), Frequency (P348)	As above.		
Analog. Channel 12	IC-2 (P343-6), Frequency 2 (P348)	As above.		
Analog. Channel 13	VN2 (P344/5), Unused (P348)	As above.		
Analog. Channel 14	V64S (P345), Unused (P348)	As above.		
Analog. Channel 15	I64S (P345), Unused (P348)	As above.		
Analog. Channel 16	Unused	As above.		
Analog. Channel 17	Unused	As above.		
Analog. Channel 18	Unused	As above.		
Analog. Channel 19	Unused	As above.		
Analog. Channel 20	Unused	As above.		

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Digital Inputs 1 to 32	Relays 1 to 12 and Opto's 1 to 12	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals		
The digital channels may be mapped to any of the opto isolated inputs or output contacts, in addition to a number of internal relay digital signals, such as protection starts, LEDs etc.				
Inputs 1 to 32 Trigger	No Trigger except Dedicated Trip Relay O/P's which are set to Trigger L/H	No Trigger, Trigger L/H, Trigger H/L		
Any of the digital channels may be selected to trigger the disturbance recorder on either a low to high (L/H) or a high to low (H/L) transition.				

Table 44: Disturbance record settings

1.3.13 Measurement setup

ST

The MEASURE'T SETUP column sets up the way quantities are measured and displayed. For example, whether they are displayed as primary or secondary quantities, how monitoring periods are defined and how distance units are selected (P342-6/8).

Menu text	Default settings	Available settings
MEASURE'T SETUP		
Default Display	Description	User Banner, 3Ph + N Current, 3Ph Neutral Voltage, Power, Date and Time, Description, Plant Reference, Frequency, Access Level (P342-6) User Banner, 3Ph Current, 3Ph Neutral Voltage, 3Ph Current 2, Date and Time, Description, Plant Reference, Frequency, Access Level, Frequency 2 (P348)
This setting can be used to select the default display from a range of options, note that it is also possible to view the other default displays whilst at the default level using the ⟨ and ⟩ keys. However once the 15 minute timeout elapses the default display will revert to that selected by this setting.		
Local Values	Primary	Primary, Secondary
This setting controls whether measured values via the front panel user interface and the front courier port are displayed as primary or secondary quantities.		
Remote Values	Primary	Primary, Secondary
This setting controls whether measured values via the rear communication port are displayed as primary or secondary quantities.		
Measurement Ref.	VA	VA/VB/VC/IA/IB/IC
Using this setting the phase reference for all angular measurements by the relay can be selected.		
Measurement Mode	0	0 to 3 step 1
This setting is used to control the signing of the real and reactive power quantities; the signing convention used is defined in the Measurements and Recording chapter (*P34x/EN MR*)		
Fix Dem Period	30 minutes	1 to 99 minutes step 1 minute
This setting defines the length of the fixed demand window.		
Roll Sub Period	30 minutes	1 to 99 minutes step 1 minute
The rolling demand uses a sliding/rolling window. The rolling demand window consists of a number of smaller sub periods (Num Sub Periods). The resolution of the rolling window is the sub period length (Roll Sub Period) with the displayed values being updated at the end of each sub period.		
Num Sub Periods	1	1 to 15 step 1
This setting is used to set the number of rolling demand sub periods.		

Menu text	Default settings	Available settings
MEASURE'T SETUP		
Remote 2 Values	Primary	Primary, Secondary
This setting controls whether measured values via the 2nd rear communication port are displayed as primary or secondary quantities.		

Table 45: Measurement setup settings

1.3.14 Communications

The communications settings apply to the rear communications ports only and will depend on the particular protocol being used (P342-6/8). For further details see the SCADA Communications chapter (*P34x/EN SC*).

1.3.14.1 Communication settings for courier protocol

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	Courier			
Indicates the communications protocol that will be used on the rear communications port.				
RP1 Address	255	0	255	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				
RP1 Inactiv Timer	15 mins	1 min	30 mins	1 min
This cell controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
RP1 Physical Link	Copper	Copper, Fiber Optic or KBus		
This cell defines whether an electrical EIA(RS)485, fiber optic or KBus connection is being used for communication between the master station and relay. If Fiber Optic is selected, the optional fiber optic communications board will be required.				
RP1 Card Status	K-Bus OK, RS485 OK, Fiber Optic OK			
Rear Port 1 Courier Protocol Status.				
RP1 Port Config.	KBus	KBus, EIA(RS)485		
This cell defines whether an electrical KBus or EIA(RS)485 is being used for communication between the master station and relay.				
RP1 Comms Mode	IEC 60870 FT1.2 Frame	IEC 60870 FT1.2 Frame or 10-Bit No Parity		
The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.				
RP1 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				

Table 46: Communication settings for courier protocol

1.3.14.2 Communication settings for MODBUS protocol

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	MODBUS			
Indicates the communications protocol that will be used on the rear communications port.				
RP1 Address	1	1	247	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
RP1 Inactiv Timer	15 mins	1 mins	30 mins	1 min
This cell controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
RP1 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				
RP1 Parity	None	Odd, Even or None		
This cell controls the parity format used in the data frames. It is important that both relay and master station are set with the same parity setting.				
RP1 Physical Link	Copper	Copper, Fiber Optic		
This cell defines whether an electrical EIA(RS) 485 or fiber optic connection is being used for communication between the master station and relay. If 'Fiber Optic' is selected, the optional fiber optic communications board will be required.				
MODBUS IEC Time	Standard IEC	Standard IEC or Reverse		
When 'Standard IEC' is selected the time format complies with IEC 60870-5-4 requirements such that byte 1 of the information is transmitted first, followed by bytes 2 through to 7. If 'Reverse' is selected the transmission of information is reversed.				

Table 47: Communication settings for MODBUS protocol

1.3.14.3 Communication settings for IEC 60870-5-103 protocol

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	IEC 60870-5-103			
Indicates the communications protocol that will be used on the rear communications port.				
RP1 Address	1	0	247	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				
RP1 Inactiv Timer	15 mins	1 min	30 mins	1 min
This cell controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
RP1 Baud Rate	19200 bits/s	9600 bits/s or 19200 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				
RP1 Measure't Period	15 s	1 s	60 s	1 s
This cell controls the time interval that the relay will use between sending measurement data to the master station.				
RP1 Physical Link	Copper	Copper, Fiber Optic		
This cell defines whether an electrical EIA(RS) 485 or fiber optic connection is being used for communication between the master station and relay. If 'Fiber Optic' is selected, the optional fiber optic communications board will be required.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
RP1 CS103 Blocking	Disabled	Disabled, Monitor Blocking or Command Blocking		
There are three settings associated with this cell:				
Disabled	-	No blocking selected.		
Monitor Blocking	-	When the monitor blocking DDB Signal is active high, either by energizing an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the relay returns a "termination of general interrogation" message to the master station.		
Command Blocking	-	When the command blocking DDB signal is active high, either by energizing an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the relay returns a "negative acknowledgement of command" message to the master station.		

Table 48: Communication settings for IEC-103 protocol

1.3.14.4 Communication settings for DNP3.0 protocol

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	DNP 3.0			
Indicates the communications protocol that will be used on the rear communications port.				
RP1 Address	3	0	65519	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				
RP1 Baud Rate	19200 bits/s	1200 bits/s, 2400 bits/s, 4800 bits/s, 9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				
RP1 Parity	None	Odd, Even or None		
This cell controls the parity format used in the data frames. It is important that both relay and master station are set with the same parity setting.				
RP1 Physical Link	Copper	Copper, Fiber Optic		
This cell defines whether an electrical EIA(RS) 485 or fiber optic connection is being used for communication between the master station and relay. If 'Fiber Optic' is selected, the optional fiber optic communications board will be required.				
RP1 Time Sync.	Disabled	Disabled, Enabled		
If set to 'Enabled' the DNP3.0 master station can be used to synchronize the time on the relay. If set to 'Disabled' either the internal free running clock, or IRIG-B input are used.				
DNP Need Time	10 mins	1 min	30 mins	1 min
The duration of time waited, before requesting another time sync from the master.				
DNP App Fragment	2048 bytes	100 bytes	2048 bytes	1 byte
The maximum message length (application fragment size) transmitted by the relay.				
DNP App Timeout	2 s	1 s	120 s	1 s
Duration of time waited, after sending a message fragment and awaiting a confirmation from the master.				
DNP SBO Timeout	10 s	1 s	10 s	1 s
Duration of time waited, after receiving a select command and awaiting an operate confirmation from the master.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DNP Link Timeout	0 s	0 s	120 s	1 s
Duration of time that the relay will wait for a Data Link Confirm from the master. A value of 0 means data link support disabled and 1 to 120 seconds is the timeout setting.				

Table 49: Communication settings for DNP3.0 protocol

1.3.14.5 Communication settings for Ethernet port - IEC 61850

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
NIC Protocol	IEC 61850			
Indicates that IEC 61850 will be used on the rear Ethernet port.				
NIC MAC Address	Ethernet MAC Address			
Indicates the MAC address of the rear Ethernet port.				
NIC Tunl Timeout	5 mins	1 min	30 mins	1 min
Duration of time waited before an inactive tunnel to S1 Studio is reset.				
NIC Link Report	Alarm	Alarm, Event, None		
Configures how a failed/unfitted network link (copper or fiber) is reported: Alarm - an alarm is raised for a failed link Event - an event is logged for a failed link None - nothing reported for a failed link				
NIC Link Timeout	60 s	0.1 s	60 s	0.1 s
Duration of time waited, after failed network link is detected, before communication by the alternative communications interface (fiber optic/copper interface) is attempted. See also the IED CONFIGURATOR column for IEC 61850 data.				

Table 50: Ethernet port communication settings - IEC 61850

1.3.14.6 Communication settings for Ethernet port - DNP 3.0

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
NIC Protocol	DNP 3.0			
Indicates that IEC 61850 will be used on the rear Ethernet port.				
IP Address	0.0.0.0			
Indicates the IP address of the relay.				
Subnet Mask	0.0.0.0			
Indicates the Subnet address.				
NIC MAC Address	Ethernet MAC Address			
Indicates the MAC address of the rear Ethernet port.				
Gateway				
Indicates the Gateway address.				
DNP 3.0 Time Sync	Disabled	Disabled, Enabled		
If set to 'Enabled' the DNP3.0 master station can be used to synchronize the time on the relay. If set to 'Disabled' either the internal free running clock, or IRIG-B input are used.				
Meas. Scaling	Primary	Normalized, Primary, Secondary		
Setting to report analog values in terms of primary, secondary or normalized (with respect to the CT/VT ratio setting) values.				
NIC Tunl Timeout	5 mins	1 min	30 mins	1 min
Duration of time waited before an inactive tunnel to S1 Studio is reset.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
NIC Link Report	Alarm	Alarm, Event, None		
Configures how a failed/unfitted network link (copper or fiber) is reported: Alarm - an alarm is raised for a failed link Event - an event is logged for a failed link None - nothing reported for a failed link				
NIC Link Timeout	60 s	0.1 s	60 s	0.1 s
Duration of time waited, after failed network link is detected, before communication by the alternative communications interface (fiber optic/copper interface) is attempted. See also the IED CONFIGURATOR column for IEC 61850 data.				
SNTP PARAMETERS	Sub-heading			
SNTP Server 1	SNTP Server 1 address			
Indicates the SNTP Server 1 address.				
SNTP Server 2	SNTP Server 2 address			
Indicates the SNTP Server 2 address.				
SNTP Poll Rate	64 s	64 s	1024 s	1 s
Duration of SNTP poll rate in seconds.				
DNP Need Time	10 mins	1 min	30 mins	1 min
The duration of time waited, before requesting another time sync from the master.				
DNP App Fragment	2048 bytes	100 bytes	2048 bytes	1 byte
The maximum message length (application fragment size) transmitted by the relay.				
DNP App Timeout	2 s	1 s	120 s	1 s
Duration of time waited, after sending a message fragment and awaiting a confirmation from the master.				
DNP SBO Timeout	10 s	1 s	10 s	1 s
Duration of time waited, after receiving a select command and awaiting an operate confirmation from the master.				

Table 51: Ethernet port communication settings - DNP 3.0

1.3.14.7 Rear port 2 connection settings

The settings shown are those configurable for the second rear port which is only available with the courier protocol (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP2 Protocol	Courier			
Indicates the communications protocol that will be used on the 2nd rear communications port.				
RP2 Card Status	K-Bus OK, RS485 OK, Fiber Optic OK			
Rear Port 2 Courier Protocol Status.				
RP2 Port Config.	RS232	EIA(RS)232, EIA(RS)485 or KBus		
This cell defines whether an electrical EIA(RS)232, EIA(RS)485 or KBus is being used for communication.				
RP2 Comms. Mode	IEC 60870 FT1.2 Frame	IEC 60870 FT1.2 Frame or 10-Bit No Parity		
The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.				
RP2 Address	255	0	255	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
RP2 Inactiv Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
RP2 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				

Table 52: Rear port connection settings

1.3.15 Commissioning tests

There are menu cells which allow the status of the opto-isolated inputs, output relay contacts, internal digital data bus (DDB) signals and user-programmable LEDs to be monitored. Also there are cells to test the operation of the output contacts and user-programmable LEDs (P342-6/8).

ST

Menu text	Default setting	Available settings
COMMISSION TESTS		
Opto I/P Status	0000000000000000	
This menu cell displays the status of the relay's opto-isolated inputs as a binary string, a **1** indicating an energized opto-isolated input and a '0' a de-energized one.		
Relay O/P Status	0000000000000000	
This menu cell displays the status of the relay's output contacts as a binary string, a **1** indicating an operated state and '0' a non-operated state. When the **Test Mode** cell is set to **Enabled** the **Relay O/P Status** cell does not show the current status of the output relays and hence can not be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.		
Test Port Status	00000000	
This menu cell displays the status of the eight digital data bus (DDB) signals that have been allocated in the **Monitor Bit** cells.		
Monitor Bit 1	64 (LED 1)	0 to 2047 See PSL chapter for details of digital data bus signals
The eight **Monitor Bit** cells allow the user to select the status of which digital data bus signals can be observed in the **Test Port Status** cell or via the monitor/download port.		
Monitor Bit 8	71 (LED 8)	0 to 2047
The eight **Monitor Bit** cells allow the user to select the status of which digital data bus signals can be observed in the **Test Port Status** cell or via the monitor/download port.		
Test Mode	Disabled	Disabled, Test Mode, Contacts Blocked
The Test Mode menu cell is used to allow secondary injection testing to be performed on the relay without operation of the trip contacts. It also enables a facility to directly test the output contacts by applying menu controlled test signals. To select test mode the Test Mode menu cell should be set to **Test Mode**, which takes the relay out of service and blocks the maintenance, counters. It also causes an alarm condition to be recorded and the yellow **Out of Service** LED to illuminate and an alarm message **Prot'n. Disabled** is given. This also freezes any information stored in the CB Condition column and in IEC 60870-5-103 builds changes the Cause of Transmission, COT, to Test Mode. To enable testing of output contacts the **Test Mode** cell should be set to **Contacts Blocked**. This blocks the protection from operating the contacts and enables the test pattern and contact test functions which can be used to manually operate the output contacts. Once testing is complete the cell must be set back to **Disabled** to restore the relay back to service.		
Test Pattern	00000000000000000000000000000000	0 = Not Operated 1 = Operated
This cell is used to select the output relay contacts that will be tested when the **Contact Test** cell is set to **Apply Tes**t.		

Menu text	Default setting	Available settings
Contact Test	No Operation	No Operation, Apply Test, Remove Test
When the 'Apply Test' command in this cell is issued the contacts set for operation (set to **1**) in the 'Test Pattern' cell change state. After the test has been applied the command text on the LCD will change to 'No Operation' and the contacts will remain in the Test State until reset issuing the 'Remove Test' command. The command text on the LCD will again revert to 'No Operation' after the 'Remove Test' command has been issued. Note: When the **Test Mode** cell is set to **Enabled** the **Relay O/P Status** cell does not show the current status of the output relays and hence can not be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.		
Test LEDs	No Operation	No Operation Apply Test
When the 'Apply Test' command in this cell is issued the 8 (P342/3/4) or 18 (P345) user-programmable LEDs will illuminate for approximately 2 seconds before they extinguish and the command text on the LCD reverts to **No Operation**.		
Red LED Status	000000000000000000	
This cell is an 18 bit binary string that indicates which of the user-programmable LEDs on the relay are illuminated with the Red LED input active when accessing the relay from a remote location, a **1** indicating a particular LED is lit and a '0' not lit. If both the Green and Red LED status bits for an LED are on then this indicates the LED is yellow. This is only applicable to the P345 which has programmable tri-color LEDs – red/yellow/green.		
Green LED Status	000000000000000000	
This cell is an 18 bit binary string that indicates which of the user-programmable LEDs on the relay are illuminated with the Green LED input active when accessing the relay from a remote location, a '1' indicating a particular LED is lit and a '0' not lit. If both the Green and Red LED status bits for an LED are on then this indicates the LED is yellow. This is only applicable to the P345 which has programmable tri-color LEDs – red/yellow/green.		
DDB 31 - 0	00000000000000000000001000000000	
Displays the status of DDB signals 0-31.		
DDB 2047 - 2016	00000000000000000000000000000000	
Displays the status of DDB signals 2047- 2016. There are similar cells showing 32 bit binary strings for all DDBs from 0 – 2047. The first and last 32 bit words only are shown here.		

Table 53: Commissioning tests menu cells

1.3.16 Circuit breaker condition monitor setup

The Circuit Breaker condition monitoring includes features to monitor the CB condition such as the current broken, number of CB operations, number of CB operations in a set time and CB operating time. Alarms or a circuit breaker lockout can be raised for different threshold values (P342-6).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CB MONITOR SETUP				
Broken I^	2	1	2	0.1
This sets the factor to be used for the cumulative I^ counter calculation that monitors the cumulative severity of the duty placed on the interrupter. This factor is set according to the type of Circuit Breaker used.				
I^ Maintenance	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Enables or disables the cumulative I^ maintenance alarm element.				
I^ Maintenance	1000 In^	1 In^	25000 In^	1 In^
Threshold setting for the cumulative I^ maintenance counter. This alarm indicates when preventative maintenance is due.				
I^ Lockout	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Enables or disables the cumulative I^lockout element.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
I^ Lockout	2000 In^	1 In^	25000 In^	1 In^
Threshold setting for the cumulative I^ lockout counter. The relay can be used to lockout the CB reclosing if maintenance is not carried out on reaching this lockout threshold.				
No CB Ops Maint.	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Number of circuit breaker operations setting for the maintenance alarm.				
No CB Ops Maint.	10	1	10000	1
Threshold setting for number of circuit breaker operations for the maintenance alarm. This alarm indicates when preventative maintenance is due.				
No CB Ops Lock	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Enables or disables the number of circuit breaker operations lockout alarm.				
No CB Ops Lock	20	1	10000	1
Threshold setting for number of circuit breaker operations for maintenance lockout. This lockout alarm can be used to block or lockout the CB reclosing if maintenance is not carried out on reaching this lockout threshold.				
CB Time Maint	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Enables or disables the circuit breaker operating time maintenance alarm.				
CB Time Maint	0.1 s	0.005 s	0.5 s	0.001 s
Circuit breaker operating time threshold setting. This alarm is set in relation to the specified interrupting time of the circuit breaker.				
CB Time Lockout	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Enables or disables the circuit breaker operating time lockout alarm.				
CB Time Lockout	0.2 s	0.005 s	0.5 s	0.001 s
Circuit breaker operating time threshold setting. This lockout alarm is set in relation to the specified interrupting time of the circuit breaker.				
Fault Freq Lock	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Enables or disables the fault frequency counter alarm.				
Fault Freq Count	10	1	9999	1
Circuit breaker frequent operations counter setting. This element monitors the number of operations over a set time period.				
Fault Freq. Time	3600 s	0 s	9999 s	1 s
Time period setting over which the circuit breaker frequent operations are to be monitored.				

Table 54: Circuit breaker condition monitoring menu

1.3.17 Opto configuration

The OPTO CONFIG settings define the opto-input configuration settings, including setting the nominal voltage values for each opto-input, setting filters to remove ac induced voltage as well as pick-up and drop-off characteristics for the opto-inputs (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
OPTO CONFIG.				
Global Nominal V	24 - 27	24 - 27, 30 - 34, 48 - 54, 110 - 125, 220 - 250, Custom		
Sets the nominal battery voltage for all opto inputs by selecting one of the five standard ratings in the Global Nominal V settings. If Custom is selected then each opto input can individually be set to a nominal voltage value.				
Opto Input 1	24 - 27	24 - 27, 30 - 34, 48 - 54, 110 - 125, 220 - 250		
Each opto input can individually be set to a nominal voltage value if custom is selected for the global setting.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Opto Input 2 - 32	24 - 27	24 - 27, 30 - 34, 48 - 54, 110 - 125, 220 - 250		
Each opto input can individually be set to a nominal voltage value if custom is selected for the global setting.				
Opto Filter Cntl.	1111111111111111	0 = Disable Filtering 1 = Enable filtering		
A binary string is used to represent the opto inputs available. A '1' or '0' is used to enable or disable for each input a pre-set filter of ½ cycle that renders the input immune to induced ac noise on the wiring.				
Characteristics	Standard 60% - 80%	Standard 60% - 80%, 50% - 70%		
Selects the pick-up and drop-off characteristics of the optos. Selecting the standard setting means they nominally provide a Logic 1 or On value for Voltages ≥80% of the set lower nominal voltage and a Logic 0 or Off value for the voltages ≤60% of the set higher nominal voltage.				

Table 55: Opto inputs configuration settings

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1.3.18 Control Inputs

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function that they are connected to as part of the PSL (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CONTROL INPUTS				
Ctrl I/P Status	00000000000000000000000000000000	0 = Reset (Not Operated/OFF) 1 = Set (Operated/ON)		
This menu cell displays the status of the relay's control inputs as a binary string, a '1' indicating a Set control input and a '0' a Reset one.				
Control Input 1 to 32	No Operation	No Operation, Set, Reset		
When the 'Set' command in this cell is issued the Control Input 1 is set ON and when the 'Reset' command in this cell is issued the Control Input 1 is set OFF.				

Table 56: Control inputs settings

1.3.19 Control input configuration

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function that they are connected to as part of the PSL (P342-6/8).

Menu text	Default setting	Setting range	Step size
CTRL I/P CONFIG.			
Hotkey Enabled	11111111111111111111111111111111		
Setting to allow the control inputs to be individually assigned to the "Hotkey" menu by setting '1' in the appropriate bit in the "Hotkey Enabled" cell. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the "CONTROL INPUTS" column.			
Control Input 1	Latched	Latched, Pulsed	
Configures the control inputs as either 'latched' or 'pulsed'. A latched control input will remain in the set state until a reset command is given, either by the menu or the serial communications. A pulsed control input, however, will remain energized for 10 ms after the set command is given and will then reset automatically (i.e. no reset command required).			
Ctrl Command 1	Set/Reset	Set/Reset, In/Out, Enabled/Disabled, On/Off	
Allows the SET/RESET text, displayed in the hotkey menu, to be changed to something more suitable for the application of an individual control input, such as "ON/OFF", "IN/OUT" etc.			
Control Input 2 to 32	Latched	Latched, Pulsed	
Configures the control inputs as either 'latched' or 'pulsed'.			

Menu text	Default setting	Setting range	Step size
Ctrl Command 2 to 32	Set/Reset	Set/Reset, In/Out, Enabled/Disabled, On/Off	
Allows the SET/RESET text, displayed in the hotkey menu, to be changed to something more suitable for the application of an individual control input, such as “ON/OFF”, “IN/OUT” etc.			

Table 57: Control inputs configuration settings

1.3.20 Function keys

The function keys produce logical inputs that are fed into the unit's PSL. These inputs can be used to trigger any function to which they are connected as part of the PSL. The settings in the FUNCTION KEYS column allow you to enable or disable each function key, to set internal labels, and to set the operating mode to Normal or Toggled (P343-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
FUNCTION KEYS				
Fn. Key Status	0000000000			
Displays the status of each function key.				
Fn. Key 1 Status	Unlocked	Disable, Unlocked, Locked		
Setting to activate the function key. The ‘Lock’ setting allows a function key output that is set to toggle mode to be locked in its current active state.				
Fn. Key 1 Mode	Toggled	Toggled, Normal		
Sets the function key in toggle or normal mode. In ‘Toggle’ mode, the first keypress will latch the function key DDB output signal ON and the next keypress will reset the function key DDB output to OFF. This feature can be used to enable/disable relay functions. In the ‘Normal’ mode the function key DDB signal output will remain ON/ ‘high’ as long as the key is pressed.				
Fn. Key 1 Label	Function Key 1			
Allows the text of the function key to be changed to something more suitable for the application.				
Fn. Key 2 to 10 Status	Unlocked	Disable, Unlocked, Locked		
Setting to activate the function key. The ‘Lock’ setting allows a function key output that is set to toggle mode to be locked in its current active position.				
Fn. Key 2 to 10 Mode	Toggled (4/5/6) Normal (2/3/7/8/9/10)	Toggled, Normal		
Sets the function key in toggle or normal mode. In ‘Toggle’ mode, the first keypress will latch the function key DDB output signal ON and the next keypress will reset the function key DDB output to OFF. This feature can be used to enable/disable relay functions. In the ‘Normal’ mode the function key DDB signal output will remain ON/ ‘high’ as long as the key is pressed.				
Fn. Key 2 to 10 Label	Function Key 2 to 10			
Allows the text of the function key to be changed to something more suitable for the application.				

Table 58: Function keys settings

1.3.21 IEC 61850-9-2 LE

IEDs which have the IEC 61850-9-2LE interface must be configured to the system and application (P348).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
IEC 61850-9-2 LE				
Physical Link	Fibre Optic	Copper, Fibre Optic		
This setting specifies the physical connection between the IED and the Process Bus network. The RJ45 copper port is for service use only and should not be used as a permanent connection.				
Anti-Alias Filter	Enabled	Disabled, Enabled		
This setting activates or deactivates the anti-aliasing filter, which conditions the Sampled Values from the Process Bus network.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Synchro Alarm	Local 1PPS	No SYNC CLK, Local 1PPS, Global 1PPS		
This setting specifies the type of Sampled Value synchronisation expected by the IED, depending on the application. Global 1PPS: the Sampled Values are synchronised with a global area clock (GPS like clock). The IED issues an alarm ('9-2 Sample Alarm') when it receives Sampled Value frames without Global 1PPS. Local 1PPS: the Sampled Values are synchronised with a local area clock signal at the substation. Sampled Value frames received with Global or Local synchronisation are acceptable with this setting. The IED issues the alarm '9-2 Sample Alarm' if the Sampled Value frames received have no synchronisation. No SYNC CLK: the Sampled Values do not need to be synchronized. With this setting the IED ignores the synchronisation flag in the Sampled Value frames.				
9.2 Test Mode	Test Blocked	Test Blocked, Test Ignored, Test Only		
This setting is used for processing Sampled Value frames with an IEC 61850 Test mode flag. This setting is common to all Logical Nodes configured in the IED. Test Blocked: all channel data frames received with an IEC 61850 Test flag are treated as invalid. The IED blocks relevant protection functions and issues a '9-2 Sample Alarm'. Test Ignored: all channel data frames received with an IEC 61850 Test flag are treated as good so all protection functions remain active. Test Only: all channel data received with an IEC 61850 Test flag are treated as good. Any channel data received without the Test flag are treated as invalid. The IED blocks relevant protection functions and issues a '9-2 Sample Alarm'.				
Merge Unit Delay	1 ms	0 ms	3ms	0.25ms
When Sampled Values are received at the IED from different Merging Units, they may not arrive simultaneously due to differences in Merging Unit performance or different network path delays. This setting specifies the maximum time delay expected, starting at the reception of the Sampled Value frame from the first Merging Unit to the reception of the Sampled Value frame from the last Merging Unit for each sample count. Signal processing starts at the end of the Merging Unit delay and if a frame is not received in that specified time, an alarm appears. (9-2 Sample Alarm). The IED has a search command to measure and display the maximum Sampled Value frame delay. The Merging Unit Delay can be set based on the result of the search, which is displayed on the IED.				
LN Count	4	1	8	1
This setting specifies the number of Logical Nodes in use for receiving the Sampled Values required by the IED. The default value varies with the product. Modify the LN Count to match the number of Merging Units relevant for the IED in each specific application. The default LN Count is model dependent.				
LN1 Name to LN8 Name	MiCOM Logical Node 1 to 8			
Each Logical Node must be identified by a unique name that allows it to receive Sampled Values from a specific Merging Unit. The default name for LN1 is 'MiCOM Logical Node 1', which may be edited by the user to any ASCII text string between 10 and 34 characters to match the Merging Unit name. The same applies for LN2 to 8. The Logical Node name is the system-wide unique identification 'MsvID' defined in the Merging Unit control block MSVCB according to IEC 61850-9-2 Ed 1. The number of Logical Nodes available is variable, as set in LN Count. For example, with an LN Count of 3, LN1 Name, LN2 Name and LN3 Name should be set to match those of the corresponding Merging Units. Rename the Logical Nodes used for the application. Use between 10 and 34 characters to match each MU Logical Node name. Each Logical Node name must be exactly the same as the one set in the Merging Unit that broadcasts it.				
IA1 IB1 IC1	LN1	Unused, LN1, LN2, LN3,…,LN 8		
Three-phase rotor current inputs to the IED.				
IA2 IB2 IC2	LN2	Unused, LN1, LN2, LN3,…,LN 8		
Three-phase stator current inputs to the IED.				
VA VB VC	LN3	Unused, LN1, LN2, LN3,…,LN 8		
Three-phase rotor voltage inputs to the IED.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VA2 VB2 VC2	LN4	Unused, LN1, LN2, LN3,…,LN 8		
Three-phase rotor voltage inputs to the IED from 2nd rotor VT.				
MUs Delay Search	No	No, Yes		
The IED has a search command to measure and display the maximum Sampled Value frame delay. The Merging Unit Delay can be set based on the result of the search, which is displayed on the IED.				
MUs Delay Max	Data			
When sampled values are received at the IED from different Merging Units, they may not arrive simultaneously due to differences in Merging Unit performance or different network path delays. This cell provides the maximum time-delay measured by the relay, starting at the reception of the sampled value frame from the "first" Merging Unit to the reception of the sampled value frame from the last Merging Unit for each sample count.				
Trust Ques Data	000000	0 or 1 for each flag		
This setting specifies how the Sampled Values are processed by the IED when the associated Quality tag is 'Questionable'. There are six binary flags (0 = No, 1 = Yes) which can be set by the user, corresponding to the data quality attributes 'Out of Range', 'Bad Reference', 'Oscillatory', 'Old Data', 'Inconsistent' and 'Inaccurate'. Questionable data is treated as invalid if the flag is '0'. To process the data as good samples, the flag is changed to '1'. The setting is common to all Logical Nodes in service.				
Loss Rate Level	10%	5%	15%	1%
This setting is related to Process Bus network performance, in particular, the possibility of loss of samples. The set threshold is an upper limit for the loss of Sampled Values from any of the Logical Nodes configured in the IED, calculated every cycle. If the loss rate level exceeds the set value, the IED generates the '9-2 Sample Alarm' and the related protection functions are inhibited. 1.25% corresponds to the loss of 1 out of the 80 samples expected every cycle, averaged over one second. The loss rate calculation and threshold check is performed independently for each Logical Node configured.				
SAV Absence	00000000	0 or 1 for each flag		
This is a data cell with 8 binary flags. It indicates the presence or absence of Sampled Values from each of the Merging Units the IED is communicating with. There is a maximum of 8 Logical Nodes. The cell data for each Logical Node is continuously refreshed. 0: Sampled Values being received from the Merging Unit. 1: No Sampled Values being received from the Merging Unit.				
SAV No SmpSynch	00000000	0 or 1 for each flag		
This is a data cell with 8 binary flags. It indicates the healthiness of the Sampled Values being received from each of the Merging Units configured: 0: Sampled Values received are synchronised and any loss of samples is within acceptable limits. 1: Sampled Values received are not synchronised (Setting : Synchro Alarm) or the Sampled Value delay exceeds the acceptable value (Merging Unit Delay setting). The IED raises a 'SAV No SmpSynch' when any one of the binary flags is '1'.				
SAV Test	00000000 00000000 00000000	0 or 1 for each flag		
This is a data cell with 24 binary flags. It indicates the status of the IEC 61850 Test mode flag for each analogue channel processed by the IED (eg: VA, the A-phase voltage). The channel assignment depends on the IED.				
SAV Questionable	00000000 00000000 00000000	0 or 1 for each flag		
This is a data cell with 24 binary flags. It indicates the status of the IEC 61850 Quality attribute 'Questionable' in the Sampled Value frames for each of the analogue channels. The channel assignment depends on the IED.				
SAV Invalid	00000000 00000000 00000000	0 or 1 for each flag		
This is a data cell with 24 binary flags. It indicates the status of the IEC 61850 Quality attribute 'Invalid' in the Sampled Value frames for each of the analogue channels. The channel assignment depends on the IED.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Frame Loss Data	Sub-heading			
This column contains all the configure/setting measurement parameters relative to frame loss data.				
Frame Loss Rate	Enabled	Disabled, Enabled		
Enables the frame loss rate counter.				
LN1 - LN8 LossRate Sec	Data			
Percentage of SV frames missing during the past second, for LN1 - LN8.				
LossRate Reset	No	No, Yes		
Resets the frame loss rate counter.				
Reset Time	Data			
Reset time.				
LN1 - LN8 FrmLoss Cuml	Data			
Number of frames lost since last reset for LN1 - LN8; the most recent reset time available in the IED menu.				
LN1 to 8 Error Second	Data			
Frame Error Seconds is a cumulative value since the last reset. If the Frame Loss Rate exceeds 1.25% (one sample per cycle on average for one second) the IED records this as an Error Second for LN1 - LN8.				

Table 59: IEC 61850-9-2 LE settings

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1.3.22 Control input labels

Each control input may have a 16 character label associated with it. The CTRL I/P LABELS column contains settings that allow you to specify these labels (P342-6/8).

Menu text	Default setting	Setting range	Step size
CTRL I/P LABELS			
Control Input 1	Control Input 1	16 Character Text	
Text label to describe each individual control input. This text will be displayed when a control input is accessed by the hotkey menu and it is displayed in the programmable scheme logic description of the control input.			
Control Input 2 to 32	Control Input 2 to 32	16 Character Text	
Text label to describe each individual control input. This text will be displayed when a control input is accessed by the hotkey menu and it is displayed in the programmable scheme logic description of the control input.			

Table 60: Control input label settings

1.3.23 IED configurator (for IEC 61850 configuration)

The contents of the IED CONFIGURATOR column are mostly data cells, displayed for information but not editable. In order to edit the configuration, it is necessary to use the IED Configurator tool within S1 Studio Agile (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
IED CONFIGURATOR				
Switch Conf.Bank	No Action	No Action, Switch Banks		
Setting which allows the user to switch between the current configuration, held in the Active Memory Bank (and partly displayed below), to the configuration sent to and held in the Inactive Memory Bank.				
Restore MCL	No Action	No Action, Restore		
Setting which allows the user to reset any changes and restores the MCL stored in the relay.				
Active Conf.Name	Data			
The name of the configuration in the Active Memory Bank, usually taken from the SCL file.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Active Conf.Rev	Data			
Configuration Revision number of the configuration in the Active Memory Bank, usually taken from the SCL file.				
Inact.Conf.Name	Data			
The name of the configuration in the Inactive Memory Bank, usually taken from the SCL file.				
Inact.Conf.Rev	Data			
Configuration Revision number of the configuration in the Inactive Memory Bank, usually taken from the SCL file.				
IP PARAMETERS				
IP Address	Data			
Displays the unique network IP address that identifies the relay.				
Subnet Mask	Data			
Displays the sub-network that the relay is connected to.				
Gateway	Data			
Displays the IP address of the gateway (proxy) that the relay is connected to, if any.				
SNTP PARAMETERS				
SNTP Server 1	Data			
Displays the IP address of the primary SNTP server.				
SNTP Server 2	Data			
Displays the IP address of the secondary SNTP server.				
IEC 61850 SCL				
IED Name	Data			
8 character IED name, which is the unique name on the IEC 61850 network for the IED, usually taken from the SCL file.				
IEC 61850 GOOSE				
GoEna	00000000	0 = Disabled, 1 = Enabled		
Setting to enable GOOSE settings, GOOSE configuration blocks (GCB) 1 to 8.				
Test Mode	00000000			
The Test Mode bit sets the test flag in the outgoing (published) Goose message. Each bit corresponds to one of the eight GOCBs in the same way that the GOEna bits enable or disable the corresponding Goose message. Clearing the test mode bit clears the test flag of the published Goose message. The data in the Goose message is unaffected.				
VOP Test Pattern	0x00000000	0x00000000	0xFFFFFFFF	1
The 32-bit test pattern applied in 'Forced' test mode.				
Ignore Test Flag	No	No, Yes		
When set to 'Yes', the test flag in the subscribed GOOSE message is ignored, and the data treated as normal.				

Table 61: IEC-61850 IED configurator

1.3.24 Cyber security configuration

The SECURITY CONFIG column contains all settings related to the NERC-compliant cyber security features. These include settings to do with password control as well as settings to allow the possibility of disabling physical ports (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
SECURITY CONFIG				
User Banner	ACCESS ONLY FOR AUTHORISED USERS	ASCII 32 to 234		
NERC compliant user IED description.				
Attempts Limit	2	0	3	1
Defines the maximum number of failed password attempts.				
Attempts Timer	2 min	1 min	3 min	1 min
Defines the time duration used for detection of maximum failed password attempts.				
Blocking Timer	5 mins	1 min	30 min	1 min
Defines the time duration for which the user is blocked after exceeding the maximum attempts limit.				
Front Port	Enabled	Disabled, Enabled		
Enable/disable of Physical Front Port.				
Rear Port 1	Enabled	Disabled, Enabled		
Enable/disable of Physical Rear Port 1.				
Rear Port 2	Enabled	Disabled, Enabled		
Enable/disable of Physical Rear Port 2.				
Ethernet Port	Enabled	Disabled, Enabled		
Enable/disable of Physical Ethernet Port.				
Courier Tunnel	Enabled	Disabled, Enabled		
Enable/disable of Logical Tunnelled courier Port.				
IEC 61850	Enabled	Disabled, Enabled		
Enable/disable of Logical IEC 61850 Port.				
DNP OE	Enabled	Disabled, Enabled		
Enable/disable of Logical DNP 3.0 over Ethernet Port.				
Attempts Remaining	Data			
Number of password attempts remaining.				
Blk Time Remain	Data			
Blocking time remaining.				
Fallback Level	Level 0	Level 0 Level 1 Level 2 Level 3		
The password level adopted by the IED after an inactivity timeout, or after the user logs out. This will be either the level of the highest level password that is blank, or level 0 if no passwords are blank.				
Security Code	Data			
This cell displays the 16-character security code required when requesting a recovery password.				

Table 62: SECURITY CONFIG column

1.3.25 PSL data

The PSL DATA column contains cells that display information relating to the PSL scheme used in each of the settings groups. The items that can be displayed are the PSL reference, ID, and the Date and Time that the scheme was downloaded to the device or the default was restored (P342-6/8).

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
PSL DATA				
Grp 1 PSL Ref.	ASCII Text (32 Chars)			
User settable PSL reference during PSL file download.				
Date/Time	IEC 870 Date & Time			
Date and Time of when PSL file was downloaded or when firmware was downloaded/default settings restored.				
Grp 1 PSL ID	Data			
CRC of Group 1 PSL file.				
Grp 2 PSL Ref	ASCII Text (32 Chars)			
User settable PSL reference during PSL file download.				
Date/Time	IEC 870 Date & Time			
Date and Time of when PSL file was downloaded or when firmware was downloaded/default settings restored.				
Grp 2 PSL ID	Data			
CRC of Group 2 PSL file.				
Grp 3 PSL Ref	ASCII Text (32 Chars)			
User settable PSL reference during PSL file download.				
Date/Time	IEC 870 Date & Time			
Date and Time of when PSL file was downloaded or when firmware was downloaded/default settings restored.				
Grp 3 PSL ID	Data			
CRC of Group 3 PSL file.				
Grp 4 PSL Ref	ASCII Text (32 Chars)			
User settable PSL reference during PSL file download.				
Date/Time	IEC 870 Date & Time			
Date and Time of when PSL file was downloaded or when firmware was downloaded/default settings restored.				
Grp 4 PSL ID	Data			
CRC of Group 4 PSL file.				

Table 63: PSL Data column

1.3.26 User curves data

The USER CURVES DATA column contains cells that display information relating to the user curves. The items that can be displayed are the curve name and version and the date and time it was created. The only settable items are the curve versions (1.0 for Operate and 1.1 for Reset) and a command for restoring the default curve (P342-6/8).

Note: The factory curves loaded into Default Curve 1/2/3/4 in the relay are 1. IEEE Moderately Inverse operate curve 2. IEEE Very Inverse operate curve 3. IEEE Moderately Inverse reset curve 2. IEEE Very Inverse reset curve.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
USER CURVES DATA				
Curve 1 Name	Default Curve 1	ASCII 32 to 234		
Name entered when curve downloaded.				
Date/Time	IEC 870 Date & Time			
Date and Time of when curve was downloaded or when firmware was downloaded/default settings restored.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Curve 1 ID	Data			
CRC of curve 1.				
UserCurve 1 Type	Operate 1.0	Operate 1.0, Reset 1.1, V/Hz Operate 3.0, V/Hz Reset 3.1, UV Operate 4.0		
Defines the user curve template, either operate or reset.				
Curve 2 Name	Default Curve 2	ASCII 32 to 234		
Name entered when curve downloaded.				
Date/Time	IEC 870 Date & Time			
Date and Time of when curve was downloaded or when firmware was downloaded/default settings restored.				
Curve 2 ID	Data			
CRC of curve 2.				
UserCurve 2 Type	Operate 1.0	Operate 1.0, Reset 1.1, V/Hz Operate 3.0, V/Hz Reset 3.1, UV Operate 4.0		
Defines the user curve template, either operate or reset.				
Curve 3 Name	Default Curve 3	ASCII 32 to 234		
Name entered when curve downloaded.				
Date/Time	IEC 870 Date & Time			
Date and Time of when curve was downloaded or when firmware was downloaded/default settings restored.				
Curve 3 ID	Data			
CRC of curve 3.				
UserCurve 3 Type	Reset 1.1	Operate 1.0, Reset 1.1, V/Hz Operate 3.0, V/Hz Reset 3.1, UV Operate 4.0		
Defines the user curve template, either operate or reset.				
Curve 4 Name	Default Curve 4	ASCII 32 to 234		
Name entered when curve downloaded.				
Date/Time	IEC 870 Date & Time			
Date and Time of when curve was downloaded or when firmware was downloaded/default settings restored.				
Curve 4 ID	Data			
CRC of curve 4.				
UserCurve 4 Type	Reset 1.1	Operate 1.0, Reset 1.1, V/Hz Operate 3.0, V/Hz Reset 3.1, UV Operate 4.0		
Defines the user curve template, either operate or reset.				

Table 64: User Curve column

OP

OPERATION

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 OPERATION OF INDIVIDUAL PROTECTION FUNCTIONS

The following sections detail the individual protection functions.

1.1 Phase rotation

A facility is provided in the P340 to maintain correct operation of all the protection functions even when the generator is running in a reverse phase sequence. This is achieved through user configurable settings available for the four setting groups.

The **Phase Sequence – Standard ABC/Reverse ACB** setting applies to a power system that has a permanent phase sequence of either ABC or ACB. It is also applicable for temporary phase reversal which affects all the VTs and CTs. As distinct from the other phase reversal settings, this setting does not perform any internal phase swapping of the analogue channels.

The Phase Sequence setting affects the sequence component calculations as follows:

Standard ABC	The calculations of positive (I1, V1) and negative (I2, V2) phase sequence voltage and current remain unchanged as follows: $\overline{X_1} = \frac{1}{3}\left(\overline{X_a} + \alpha\overline{X_b} + \alpha^2\overline{X_c}\right)$ $\overline{X_2} = \frac{1}{3}\left(\overline{X_a} + \alpha^2\overline{X_b} + \alpha\overline{X_c}\right)$
Reverse ACB	The calculations of positive (I1, V1) and negative (I2, V2) phase sequence voltage and current are given by the equations: $\overline{X_1} = \frac{1}{3}\left(\overline{X_a} + \alpha^2\overline{X_b} + \alpha\overline{X_c}\right)$ $\overline{X_2} = \frac{1}{3}\left(\overline{X_a} + \alpha\overline{X_b} + \alpha^2\overline{X_c}\right)$

Where $\alpha = 1\angle 120^o$.

The Phase Sequence setting also affects the directional overcurrent protection as follows:

Phase rotation	67 (Directional Overcurrent)
Standard ABC	Phase A use Ia, Vbc Phase B use Ib, Vca Phase C use Ic, Vab
Reverse ACB	Phase A use Ia, -Vbc Phase B use Ib, -Vca Phase C use Ic, -Vab

Table 1: Table properties

The **VT Reversal**, **CT1 Reversal** and **CT2 Reversal – No Swap/ A-B Swapped/ B-C Swapped/ C-A Swapped** settings apply to applications where some or all of the voltage or current inputs are temporarily reversed, as in pump storage applications. The settings affect the order of the analogue channels in the relay and are set to emulate the order of the channels on the power system. So, assuming the settings emulate the change in phase configuration on the power system all the protection functions will naturally operate as per a standard phase rotation system. The phase sequence calculations and the protection functions all remain unchanged.

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1.2 Generator differential protection (87G)

Circulating current differential protection operates on the principle that current entering and leaving a zone of protection will be equal. Any difference between these currents is indicative of a fault being present in the zone. If CTs are connected as shown in Figure 1 it can be seen that current flowing through the zone of protection will cause current to circulate around the secondary wiring. If the CTs are of the same ratio and have identical magnetizing characteristics they will produce identical secondary currents and so zero current will flow through the relay.

If a fault exists within the zone of protection there will be a difference between the output from each CT; this difference flowing through the relay causing it to operate.

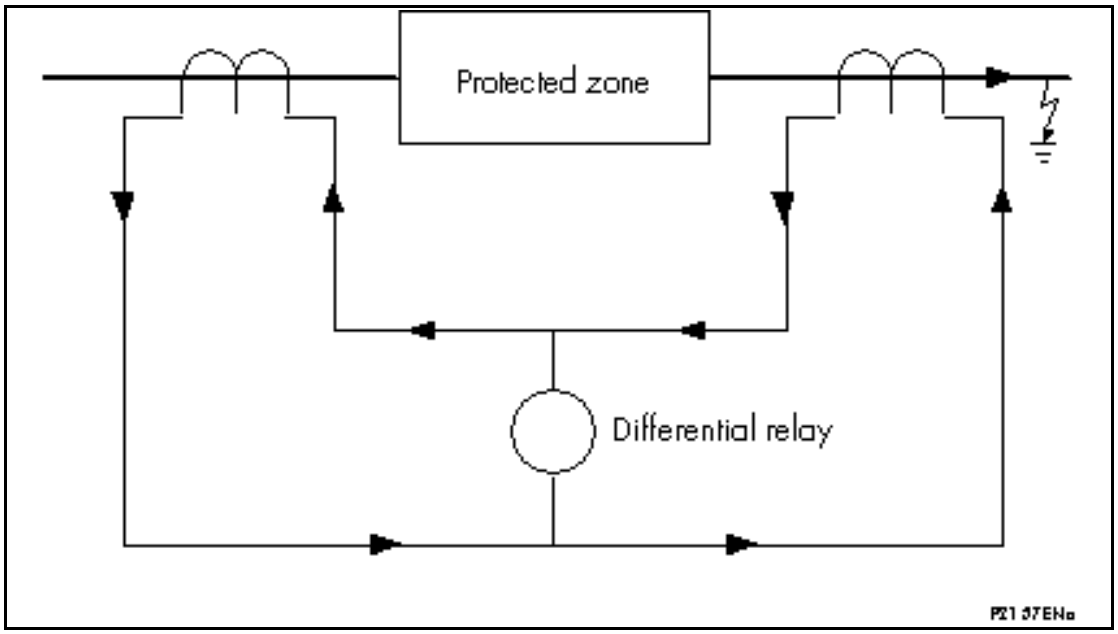


Figure 1: Principle of circulating current differential protection

Heavy through current, arising from an external fault condition, can cause one CT to saturate more than the other, resulting in a difference between the secondary current produced by each CT. It is essential to stabilize the protection for these conditions. Two methods are commonly used. A biasing technique, where the relay setting is raised as through current increases. Alternatively, a high impedance technique, where the relay impedance is such that under maximum through fault conditions, the current in the differential element is insufficient for the relay to operate.

The generator differential protection function available in the P343/4/5/6 relay can be used in either biased differential or high impedance differential mode. Both modes of operation are equally valid; users may have a preference for one over the other. The operating principle of each is described in the following sections.

The generator differential protection may also be used for interturn protection that is described in the following sections.

The generator differential protection can be blocked by energizing the relevant DDB signal via the PSL (Gen Diff Block: DDB 512). If blocking of the generator differential protection or interturn protection is required from the CT supervision this must be done in PSL by connecting DDB 1263: CTS-1 Block OR DDB 1264: CTS-2 Block OR DDB 1265: CTS Block to DDB 512: Gen Diff Block.

A DDB (Digital Data Bus) signal is available to indicate the tripping of each phase of differential protection (DDB 737, DDB 738, DDB 739), in addition a three-phase trip DDB signal is provided (DDB 736). These signals are used to operate the output relays and trigger the disturbance recorder as programmed into the Programmable Scheme Logic (PSL). The state of the DDB signals can also be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The generator differential protection operation is shown in Figure 2.

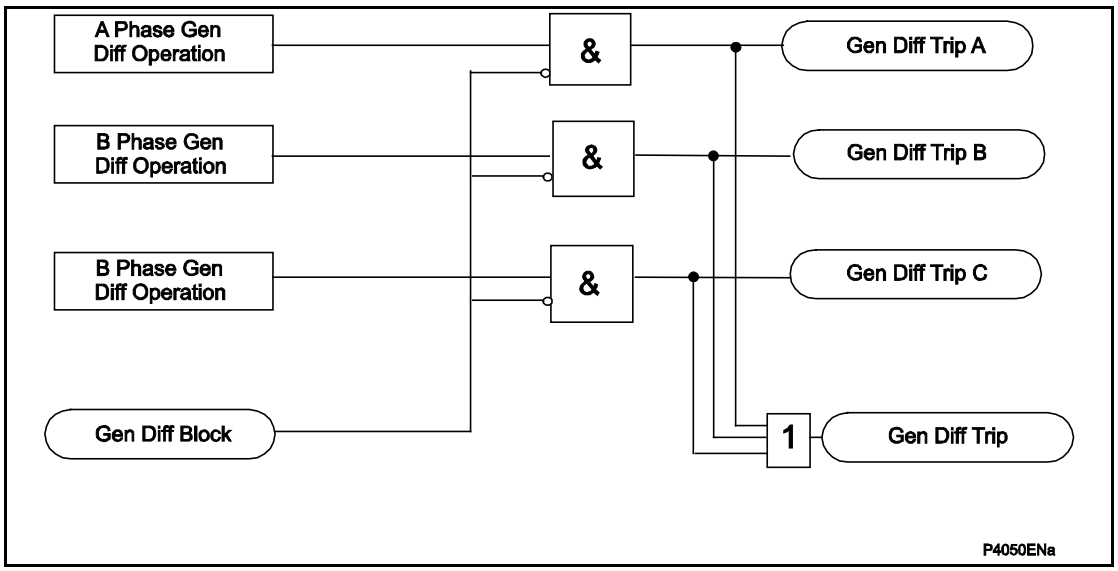


Figure 2: Generator differential logic diagram

1.2.1 Biased differential protection

In a biased differential relay, the through current is used to increase the setting of the differential element. For heavy through faults, it is unlikely that the CT outputs at each zone end will be identical, due to the effects of CT saturation. In this case a differential current can be produced. However, the biasing will increase the relay setting, such that the differential spill current is insufficient to operate the relay.

A dual slope percentage bias characteristic is implemented in the P34x. The lower slope provides sensitivity for internal faults, whereas the higher slope provides stability under through fault conditions, during which there may be transient differential currents due to saturation effect of the generator CT's.

The through current is calculated as the average of the scalar sum of the current entering and leaving the zone of protection. This calculated through current is then used to apply a percentage bias to increase the differential setting. The percentage bias can be varied to give the operating characteristic as shown in Figure 3.

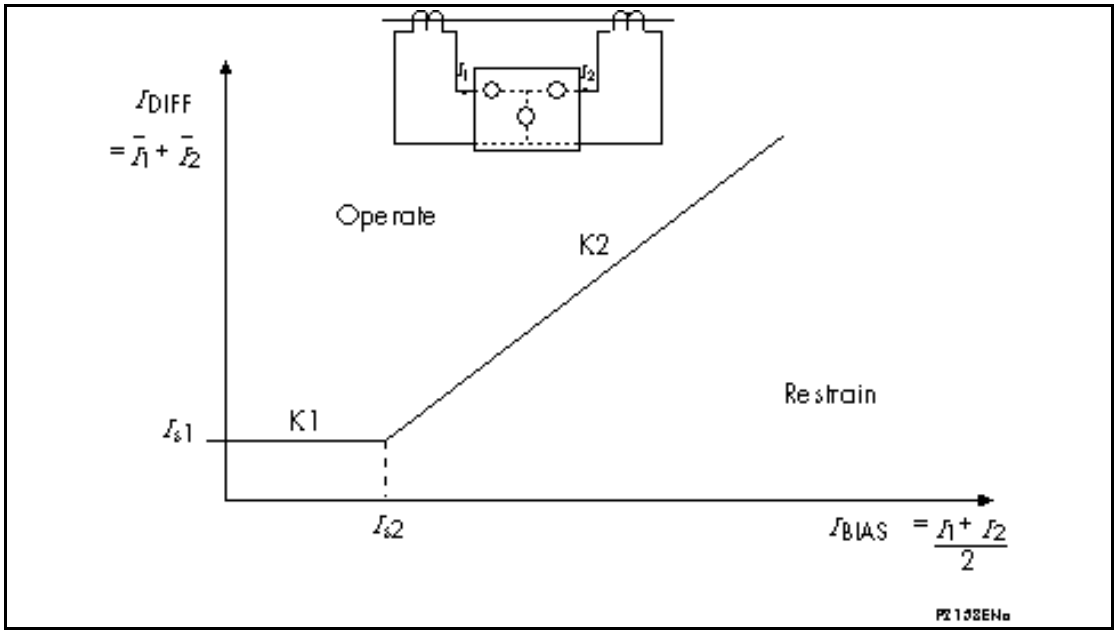


Figure 3: Biased differential protection operating characteristic

Two bias settings are provided in the P343/4/5/6 relay. The initial bias slope, **Gen Diff k1**, is applied for through currents up to **Gen Diff Is2**. The second bias slope, **Gen Diff k2**, is applied for through currents above the **Gen Diff Is2** setting.

The Biased differential protection function uses the two sets of three-phase current measurement inputs (IA, IB, IC, IA2, IB2, IC2), connected to measure the phase current at the neutral end and terminals of the machine, as shown in Figure 4. The bias and differential currents are calculated by the relay software, providing a phase segregated differential protection function, and may be viewed in the **MEASUREMENTS** columns in the relay menu.

1.2.1.1 Differential and bias current calculation

The calculation is performed on a per phase basis. The differential current is the vector sum of the phase currents measured at either end of the generator. The mean bias current (Ibias) is the scalar mean of the magnitude of these currents, i.e.

$$I_a - diff = \left| \overline{I_a - 1} + \overline{I_a - 2} \right|$$

$$I_b - diff = \left| \overline{I_b - 1} + \overline{I_b - 2} \right|$$

$$I_c - diff = \left| \overline{I_c - 1} + \overline{I_c - 2} \right|$$

$$I_a - bias = \frac{|I_a - 1| + |I_a - 2|}{2}$$

$$I_b - bias = \frac{|I_b - 1| + |I_b - 2|}{2}$$

$$I_c - bias = \frac{|I_c - 1| + |I_c - 2|}{2}$$

To provide further stability for external faults, a number of additional measures are taken on the bias calculations:

1.2.1.1.1 Delayed bias

The bias quantity used is the maximum of the bias quantities calculated within the last cycle. This is to maintain the bias level, thus providing stability, during the time when an external fault is cleared. This feature is implemented on a per phase basis. The algorithm is expressed as follows; the function is executed 4 times per cycle:

Ia-bias(n) = Maximum [Ia-bias(n), Ia-bias(n-1), ..., Ia-bias(n - 3)]

Ib-bias(n) = Maximum [Ib-bias(n), Ib-bias(n-1),....., Ib-bias(n - 3)]

Ic-bias(n) = Maximum [Ic-bias(n), Ic-bias(n-1), ..., Ic-bias(n - 3)]

1.2.1.1.2 Transient bias

An additional bias quantity is introduced into the bias calculation, on a per phase basis, if there is a sudden increase in the mean-bias measurement. This quantity decays exponentially afterwards. The transient bias is reset to zero once the relay has tripped or if the mean-bias quantity is below the Is1 setting. The transient bias is used to make the protection stable for external faults and allows for the time delay in CT saturation caused by small external fault currents and high X/R ratios. For single-end or double-end fed faults the differential current will be dominant and the transient bias will have no effect.

The transient bias is removed after the relay has tripped to avoid the possibility of chattering. It is also removed when Ibias is less than Is1 to avoid the possibility of residual values due to the numerical effects.

1.2.1.1.3 Maximum bias

The bias quantity used per phase for the percentage bias characteristic is the maximum bias current calculated from all three phases, i.e.,

I-bias-max = Maximum [Ia-bias, Ib-bias, Ic-bias]

1.2.1.1.4 Tripping criteria

The tripping criteria per phase are formulated as follows. The differential threshold changes according to the value of I-bias-max, as in the percentage bias characteristic. Note that the transient bias is on a per phase basis and is not be affected by the K1 or K2 setting.

For I-bias-max <= Is2

Idiff > K1*I-bias-max + Transient_bias + Is1

For I-bias-max > Is2

Idiff > K2*I-bias-max + Transient Bias - Is2*(K2-K1) + Is1

A count strategy is used so that the protection will operate slower near the boundary of operation. This approach is used to stabilize the relay under some marginal transient conditions.

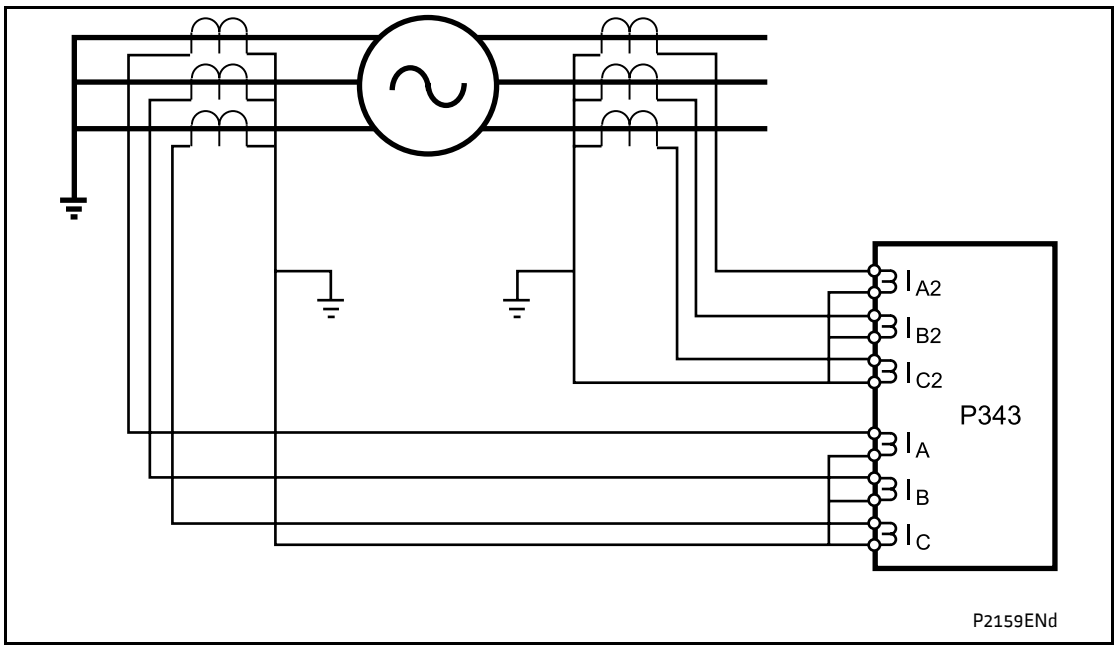


Figure 4: Relay connections for biased differential protection

1.2.2 High impedance differential protection

The high impedance principle is best explained by considering a differential scheme where one CT is saturated for an external fault, as shown in Figure 5.

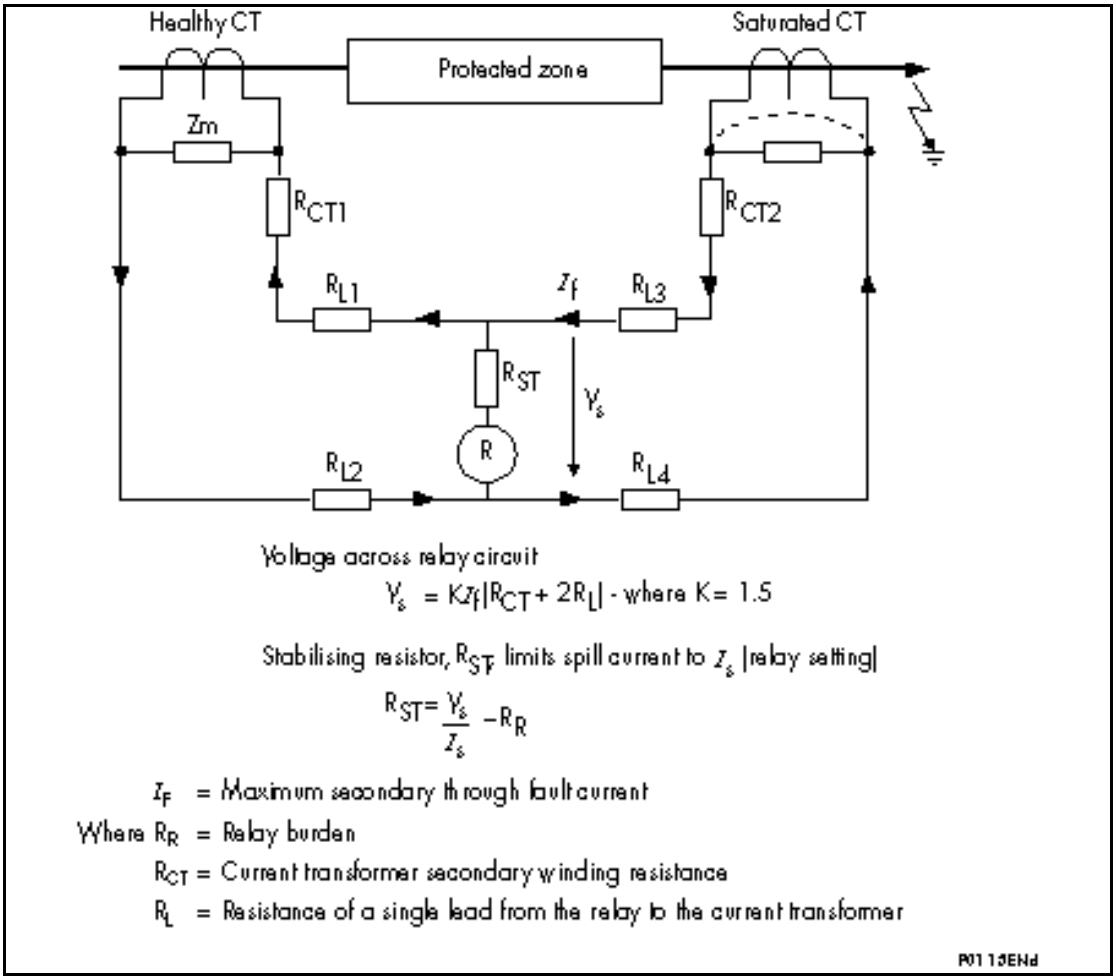


Figure 5: Principle of high impedance differential protection

If the relay circuit is considered to be a very high impedance, the secondary current produced by the healthy CT will flow through the saturated CT. If the magnetizing impedance of the saturated CT is considered to be negligible, the maximum voltage across the relay circuit will be equal to the secondary fault current multiplied by the connected impedance, ($R_L3 + R_{L4} + R_{CT2}$).

The relay can be made stable for this maximum applied voltage by increasing the overall impedance of the relay circuit, such that the resulting current through the relay is less than its current setting. As the impedance of the relay input alone is relatively low, a series connected external resistor is required. The value of this resistor, RST, is calculated by the formula shown in Figure 5. An additional non-linear resistor, Metrosil, may be required to limit the peak secondary circuit voltage during internal fault conditions.

To ensure the protection will operate quickly during an internal fault the CTs used to operate the protection must have a kneepoint voltage of at least 2 Vs.

The high impedance differential protection function uses the IA2, IB2, IC2 current inputs connected to measure the differential current in each phase, as shown in Figure 6.

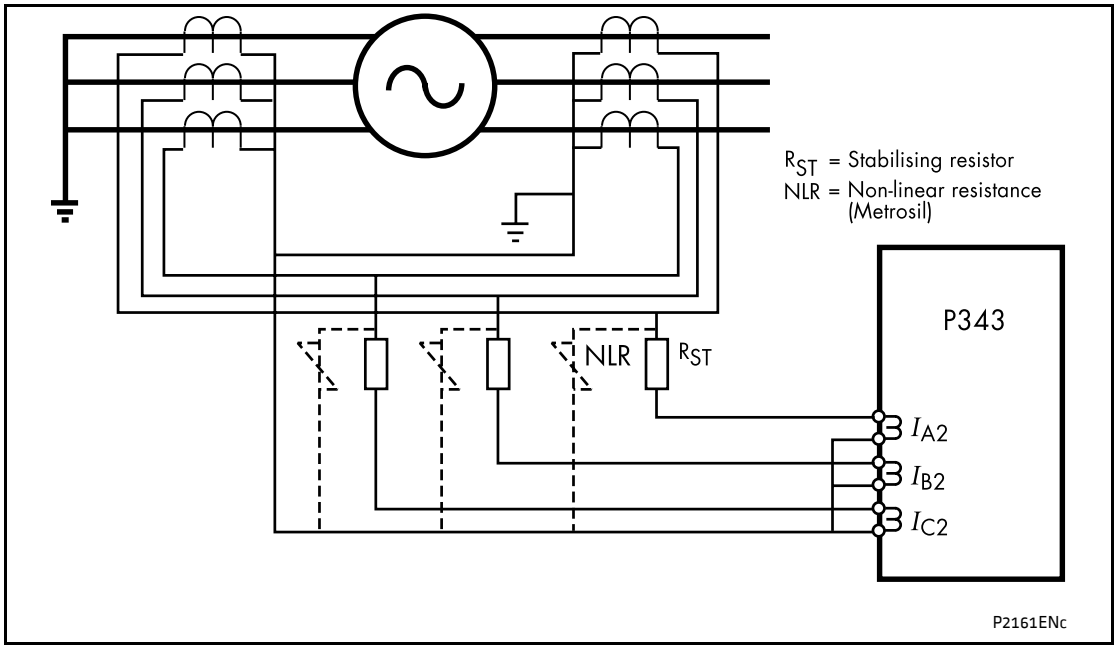


Figure 6: Relay connections for high impedance differential protection

1.2.3 Interturn (split phase) protection

For generators with multi-turn stator windings, there is the possibility of a winding inter-turn fault occurring. Unless such a fault evolves to become a stator earth fault, it will not otherwise be detected with conventional protection arrangements. Hydro generators usually involve multi-stator windings with parallel windings.

The P343/4/5/6 IA2/IB2/IC2 current inputs can be used for differential interturn protection and has independent settings per phase (**Interturn Is_A, Interturn Is_B, Interturn Is_C**). Therefore, the current setting can be increased on the faulted phase only without affecting the sensitivity of the protection on the other unfaulted phases. A time delay is used to prevent operation on CT transient error currents that may occur during external faults. The problem of CT transient error currents can be eliminated by using core balance (window) type CTs.

The interturn (split phase) protection operation is shown in the following diagrams:

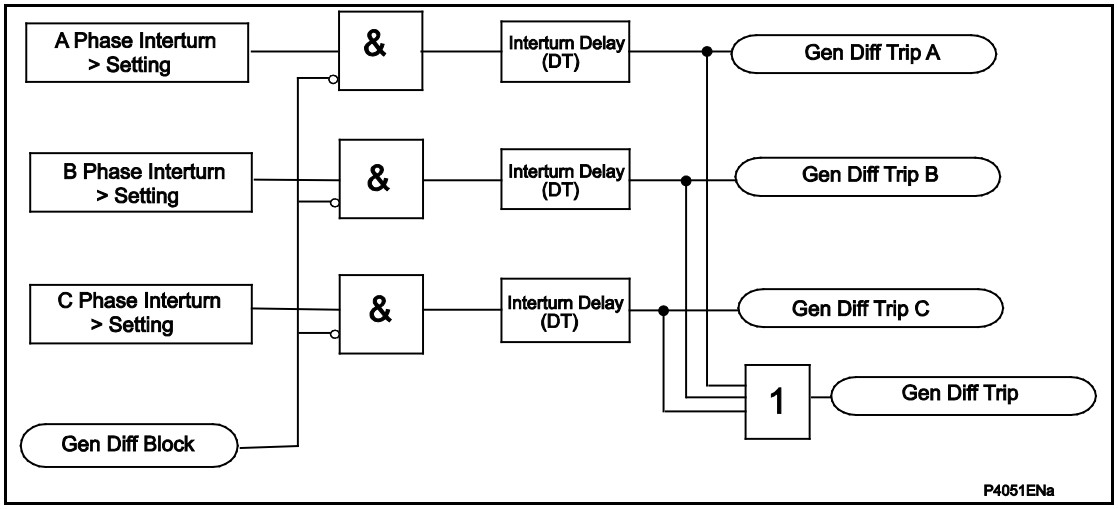


Figure 7: Interturn logic diagram

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1.3 Generator-Transformer differential protection (87GT)

The P343/4/5/6 differential protection is designed for the protection of a generator and 2 winding transformer.

For application of the device as generator-transformer differential protection, ratio correction is required. This is achieved simply by setting of the reference power generally the nominal power of the transformer and of the primary nominal voltages for all windings of the transformer. To minimize unbalance due to tap changer operation, current inputs to the differential element should be matched for the mid-tap position and not the nominal voltage.

Vector group matching is achieved by input of the relevant vector group identification number. Zero-sequence current filtering is also available. For conditions where it is possible to temporarily load the transformer with a voltage in excess of the nominal voltage, the overfluxing blocking prevents unwanted tripping. The 5th harmonic blocking feature does not require a voltage signal. A 5th harmonic signal is derived from the differential current waveform on each phase and blocking is on a per phase basis. The overfluxing protection should be used in such applications to protect the transformer accordingly.

1.3.1 Enabling or disabling differential protection

Differential protection can be disabled or enabled from the local control panel. Moreover, enabling can be done separately for each setting group. To enable the differential protection, set the cell [0912: **Differential**] to enabled under the **CONFIGURATION** menu heading, and set the cell [3001: **Winding Config**] to **Xformer** under the **SYSTEM CONFIG** menu heading. Also the generator-transformer differential function must be enabled in the required setting group, for example, set the cell [3731: Xformer Diff] to enabled under **GROUP 1 Xformer Diff** menu heading. This enables setting group1 differential protection.

1.3.2 Ratio correction

The P34x relay automatically calculates the ratio correction factor for each winding. The reference power for the protected object, identical for all windings, needs to be defined. For two-winding arrangements, the nominal power will usually be the reference power. For three transformers, the nominal power of the highest-power winding should be set as the reference power. The reference power is set in the cell [3002: **Ref Power S**] under the **GROUP 1 SYSTEM CONFIG** menu heading.

The P34x calculates the ratio correction factors on the basis of the reference power, winding nominal voltage, and primary nominal currents of the current transformers.

$$I_{ref,n} = \frac{S_{ref}}{\sqrt{3}V_{nom,n}} \qquad K_{amp,n} = \frac{I_{nom,n}}{\frac{S_{ref}}{\sqrt{3}V_{nom,n}}}$$

Sref: common reference power for all ends

n: is CT1 and CT2 for each of the CT inputs

Iref, n: reference current for the respective CT input

Kamp, n: amplitude-matching factor for the respective CT input

Inom, n: primary nominal currents for the respective CT input

Vnom, n: primary nominal voltage for the respective CT input

The P34x checks that the matching factors are within their permissible ranges. The matching factors must satisfy the following condition:

- The matching factors must always be $0.05 \leq Kamp,n \leq 20$

If the P34x calculates a matching factor that does not satisfy the above conditions, a warning, CT Mismatch Alm [DDB 396], is issued and the P34x will be blocked automatically.

Figure 8 shows the CT parameter mismatch logic diagram.

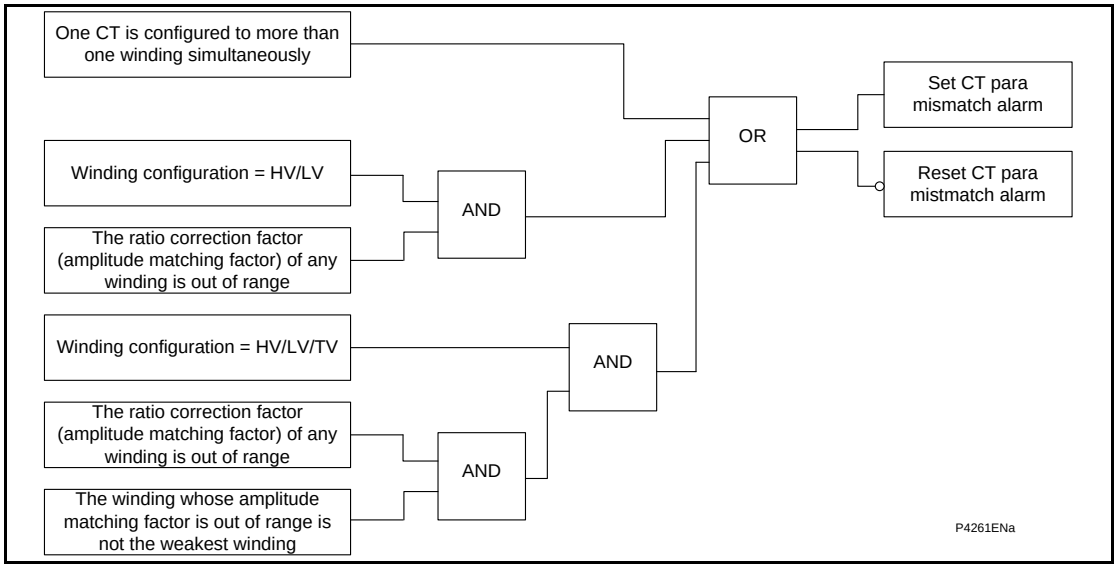


Figure 8: CT parameter mismatch logic diagram

The measured values of the phase currents of the windings of the protected object are multiplied by the relevant matching factors and are then available for further processing. Consequently, all threshold values and measured values always refer back to the relevant reference currents rather than to the transformer nominal currents or the nominal currents of the device.

1.3.3 Vector group matching

The transformer HV windings are indicated by capital letters and the LV winding by lower case letters. The numbers refer to positions on a clock face and indicate the phase displacement of balanced 3-phase LV line currents with respect to balanced 3-phase HV line currents. The HV side is taken as reference and it is the 12 o'clock position. Therefore, each hour represents a 30° shift; i.e. 1 represents a 30° lag and 11 represents a 30° lead (LV with respect to HV). An additional N, YNd1, (lower case for LV, d) indicates a neutral to earth connection on the high voltage winding of the power transformer.

By studying the relative phase shifts that can be obtained, it can be seen that star-star windings allow even vector group configurations and star-delta/delta-star windings allow odd group configurations.

Examples

A YNd1 connection indicates a two winding transformer with an earthed, Star-connected, high voltage winding and a Delta-connected low voltage winding. The low voltage balanced line currents lag the high voltage balanced line currents by 30° (−30° phase shift).

A Dyn1yn11 connection indicates a three winding transformer with a Delta-connected high voltage winding and two earthed Star-connected low voltage windings. The phase displacement of the first LV winding with respect to the HV winding is 30° lag (−30° phase shift), the phase displacement of the second LV winding with respect to the HV winding is 30° lead (+30° phase shift).

Vector group matching is performed on the amplitude-matched phase currents of the low-voltage and tertiary voltage side in accordance with the characteristic vector group number.

When the P34x is configured to protect a Yd1 transformer, the software interposing CTs used by the relay to achieve vector correction are as shown in Figure 9. No vector correction is performed on the HV amplitude matched phase currents. If the relay is in simple mode, the zero sequence filtering depends on the cell [**HV Grounding**]. The zero sequence filtering is applied when the cell [**HV Grounding**] under the **GROUP 1 SYSTEM CONFIG** menu heading is set to **Grounded**. Also, the cell [**Zero seq filt HV**] is changed to **Enabled** automatically. Otherwise, if the cell [**HV Grounding**] is set to **Ungrounded**, the cell [**Zero seq filt HV**] is changed to **Disabled** automatically.

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If the relay is in advanced mode, the zero sequence filtering depends on the cell [**Zero seq filt HV**]. The zero sequence filtering is applied when the cell [**Zero seq filt HV**] under the **GROUP 1 DIFF PROTECTION** menu heading is set to **Enabled**. Also, the cell [**HV Grounding**] is changed to **Grounded** automatically. Otherwise, if the cell [**Zero seq filt HV**] is set to **Disabled**, the cell [**Zero seq filt HV**] is changed to **Ungrouded** automatically.

Therefore on the Y high voltage side of the transformer the software interposing CT is either Yy0 (no zero sequence filtering is required) or Ydy0 (zero sequence filtering is required). The currents on the low voltage side lag by 30° the currents on the high voltage side due to the vector group (1). The relay brings the low voltage current in phase with the high voltage current by using a Yd11 software interposing CT on the low voltage side.

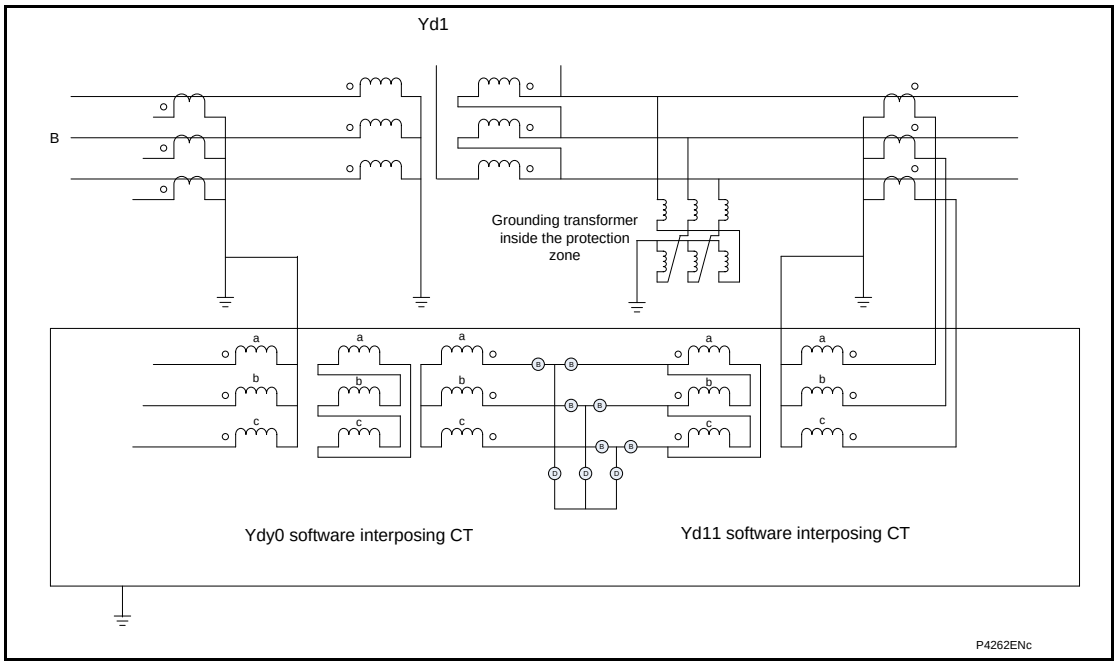


Figure 9: Software interposing CTs for a Yd1 transformer

Consider the Y grounded winding of the Yd1 transformer during external ground faults on the high voltage side. Also consider that a source is connected to the delta side. The zero sequence component of the fault current flows through the grounded neutral that lies inside the transformer differential protection zone. The zero sequence component of the fault current is only seen by the CTs in the HV side. Therefore zero sequence filtering for a Y grounded winding must be enabled to avoid undesirable tripping when an external ground fault occurs.

The Ydy0 software interposing CT is the equivalent of subtracting the zero sequence component from the phase currents on the high voltage side. The zero-sequence current is determined as follows from the amplitude-matched phase currents:

$$I_{amp,zero,n} = \frac{1}{3}\left(I_{amp,A,n} + I_{amp,B,n} + I_{amp,C,n}\right)$$

$$I_{amp,A,n,filtered} = I_{amp,A,n} - I_{amp,zero,n}$$

n: CT1, CT2 for each of the CT inputs

Iamp, zero, n: zero sequence amplitude matched current for the respective CT input

Iamp, A, n: phase A amplitude matched current of the respective CT input

The grounding transformer connected to the LV side of the power transformer provides a path for LV ground faults. To avoid misoperation during external ground faults the zero sequence component needs to be filtered. In addition, the LV currents need to be in phase with the HV currents. The P34x achieves zero sequence filtering and vector correction by using a Yd11 software interposing CT.

As previously discussed, star-star windings allow even vector group configurations and star-delta/delta-star windings allow odd group configurations. The following tables show that for all odd-numbered vector group characteristics the zero-sequence current on the low-voltage side is basically always filtered out, whereas for even-numbered vector group characteristics the zero-sequence current on the low-voltage side is never filtered out automatically. The latter is also true for the high-voltage side since in that case, as explained above, no vector correction is performed.

Vector group matching and zero-sequence current filtering must always be viewed in combination. Tables 1, 2 and 3 list the mathematical phasor operations executed by the P34x during vector correction.

The indices in the formulae have the following meaning:

am: amplitude-matched
s: amplitude- and vector group-matched
x: phase A, B or C
y: differential measuring system that corresponds to phases A, B or C.
n: CT1, CT2 for each of the CT inputs
x+1: cyclically lagging phase
x-1: cyclically leading phase

No vector correction is done on the HV side of the transformer. Only zero sequence filtering is carried on if in the simple mode the winding is set as grounded or if in the advanced mode the high voltage zero sequence filter is enabled. As a result, the relay may perform the following mathematical operations on the HV side:

	With I_{zero} filtering	Without I_{zero} filtering
0	$I_{vec,y,n} = I_{amp,x,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x,n}$

Table 2: Mathematical phasor operations on the HV side

The following figure shows the various even-numbered vector group configurations:

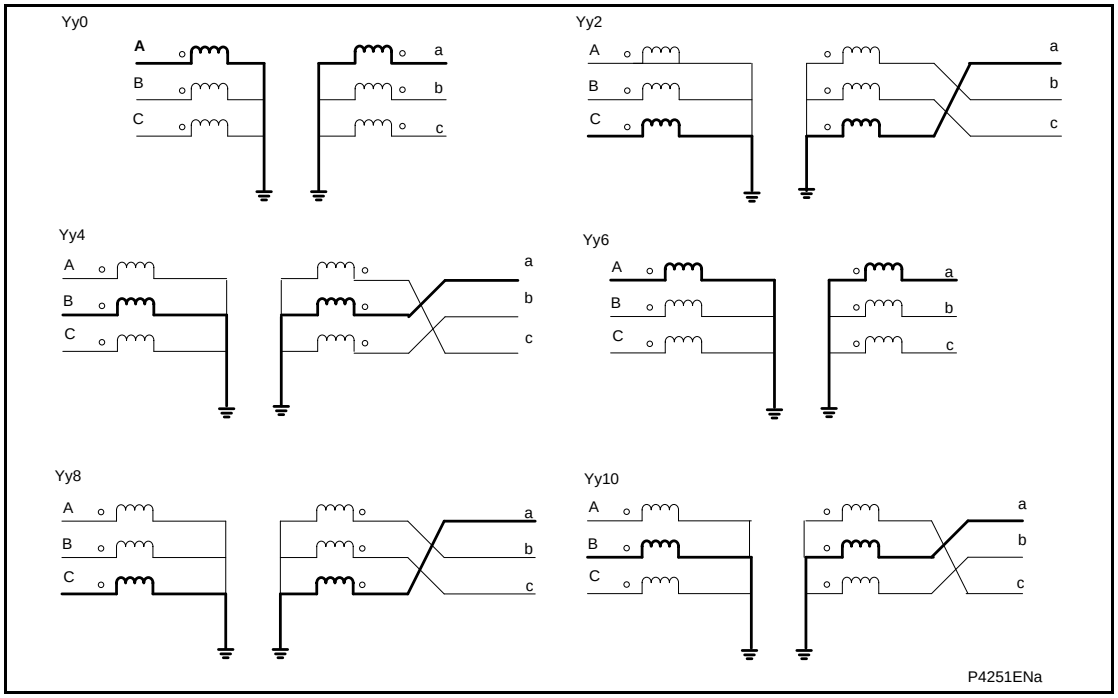


Figure 10: Yy transformer connections

Consider the configurations as shown in Figure 10.

- In a Yy0 power transformer configuration, the LV currents are already in phase with the HV currents. Therefore the relay only filters the zero sequence current as required.
- In a Yy2 power transformer configuration, the LV currents lag the HV currents by 60°. To bring the LV currents in phase with the HV currents, the P34x uses a Yy10 software interposing CT.
- In a Yy4 power transformer configuration, the LV currents lag the HV currents by 120°. To bring the LV currents in phase with the HV currents, the P34x uses a Yy8 software interposing CT.
- In a Yy6 power transformer configuration, the LV currents lag the HV currents by 180°. To bring the LV currents in phase with the HV currents, the P34x uses a Yy6 software interposing CT.
- In a Yy8 power transformer configuration, the LV currents lead the HV currents by 120°. To bring the LV currents in phase with the HV currents, the P34x uses a Yy4 software interposing CT.
- In a Yy10 power transformer configuration, the LV currents lead the HV currents by 60°. To bring the LV currents in phase with the HV currents, the P34x uses a Yy2 software interposing CT.

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Table 3 shows the mathematical operations, equivalent to the corresponding software interposing CT, on the low-voltage side for an even-numbered vector group characteristic.

VG	With I_{zero} filtering	Without I_{zero} filtering
0	$I_{vec,y,n} = I_{amp,x,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x,n}$
2	$I_{vec,y,n} = -\left(I_{amp,x+1,n} - I_{amp,zero,n}\right)$	$I_{vec,y,n} = -I_{amp,x+1,n}$
4	$I_{vec,y,n} = I_{amp,x-1,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x-1,n}$
6	$I_{vec,y,n} = -\left(I_{amp,x,n} - I_{amp,zero,n}\right)$	$I_{vec,y,n} = -I_{amp,x,n}$
8	$I_{vec,y,n} = I_{amp,x+1,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x+1,n}$
10	$I_{vec,y,n} = -\left(I_{amp,x-1,n} - I_{amp,zero,n}\right)$	$I_{vec,y,n} = -I_{amp,x-1,n}$

Table 3: Mathematical phasor operations on the LV side of Yy power transformers

Figure 11 shows the software interposing CTs used by the P34x when a Yy0 power transformer is being protected. Notice that zero sequence filter is enabled on the HV and LV sides since Ydy0 interposing CTs are being used.

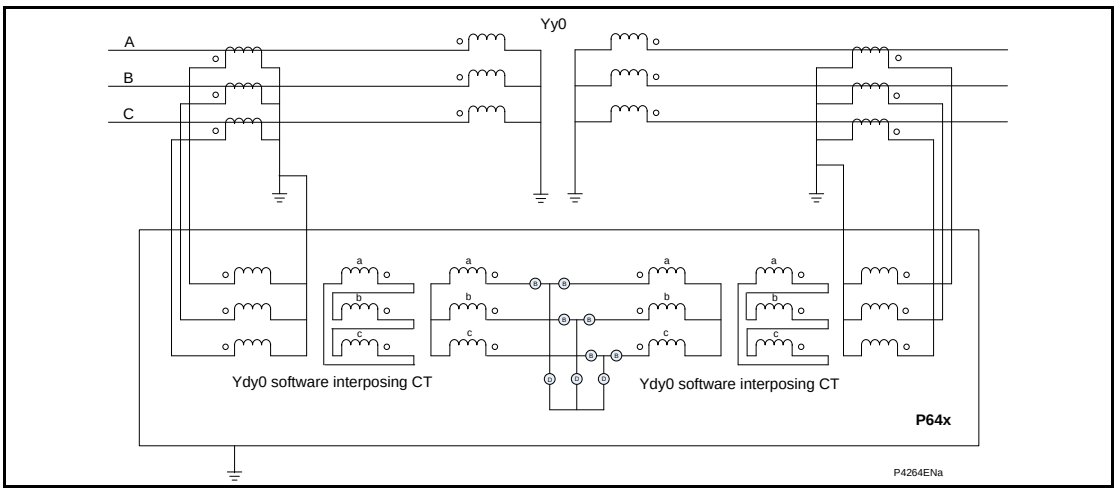


Figure 11: Software interposing CTs for a Yy0 transformer

The following figure shows the various odd-numbered vector group configurations:

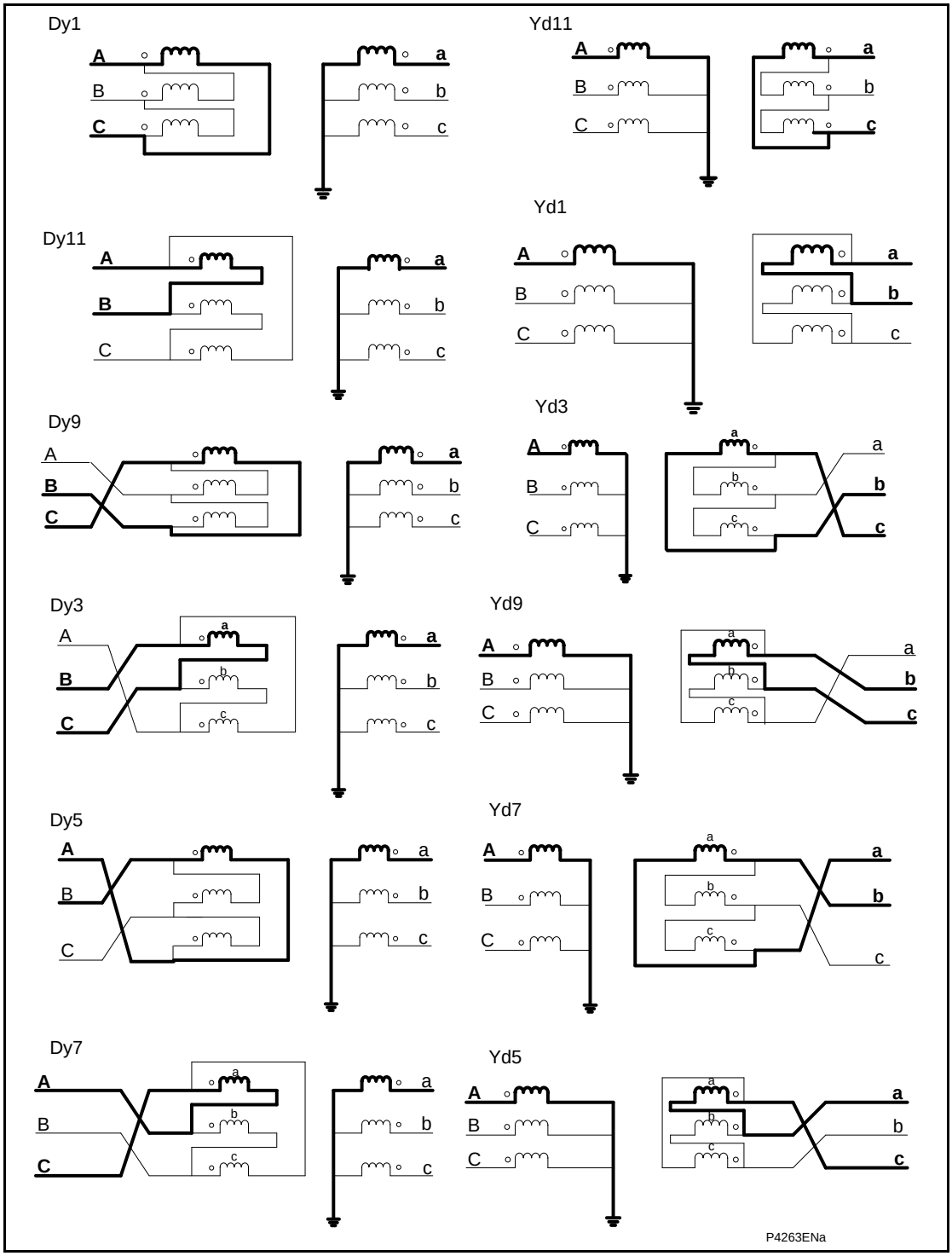


Figure 12: Yd or Dy transformer connections

Consider the configurations shown in Figure 12.

- In a Dy1 or Yd1 power transformer configuration, the LV currents lag the HV currents by 30°. The P34x uses a Yd11 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy3 or Yd3 power transformer configuration, the LV currents lag the HV currents by 90°. The P34x uses a Yd9 software interposing CT to bring the LV currents in phase with the HV currents.

- In a Dy5 or Yd5 power transformer configuration, the LV currents lag the HV currents by 150°. The P34x uses a Yd7 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy7 or Yd7 power transformer configuration, the LV currents lead the HV currents by 150°. The P34x uses a Yd5 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy9 or Yd9 power transformer configuration, the LV currents lead the HV currents by 90°. The P34x uses a Yd3 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy11 or Yd11 power transformer configuration, the LV currents lead the HV currents by 30°. The P34x uses a Yd1 software interposing CT to bring the LV currents in phase with the HV currents.

Table 4 shows the mathematical operations, equivalent to the corresponding software interposing CT, on the low-voltage side for an odd-numbered vector group characteristic:

VG	With or without I_{zero} filtering
1	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x,n} - I_{amp,x+1,n} \right)$
3	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x-1,n} - I_{amp,x+1,n} \right)$
5	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x-1,n} - I_{amp,x,n} \right)$
7	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x+1,n} - I_{amp,x,n} \right)$
9	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x+1,n} - I_{amp,x-1,n} \right)$
11	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x,n} - I_{amp,x-1,n} \right)$

Table 4: Mathematical phasor operations on the LV side of Yd or Dy power transformers

Vector group matching is by input of the vector group identification number provided that the phase currents of the high and low voltage side(s) are connected in standard configuration. For other configurations, special considerations may apply. A reverse phase rotation (phase sequence A-C-B) needs to be taken into account by making the appropriate setting at the P34x. The P34x will then automatically form the complementary value of the set vector group ID to the number 12 (vector group ID = 12 - set ID).

1.3.4 Tripping characteristics

The differential and bias currents for each phase are calculated from the current variables after amplitude and vector group matching.

Calculation of differential and biased currents is as follows:

$$I_{diff} = \left| \underline{I}_1 + \underline{I}_2 \right|$$

$$I_{bias} = \frac{\left| \underline{I}_1 \right| + \left| \underline{I}_2 \right|}{2}$$

y is the measuring system that corresponds to phases A, B or C.
s is the current after the amplitude and vector group are matched.

To provide further stability for external faults, additional measures are considered on the calculation of the bias current:

1.3.4.1 Delayed bias

The bias quantity is the maximum of the bias quantities calculated within the last cycle. This is to maintain the bias level, therefore stability is provided when an external fault is cleared. This feature is implemented on a per-phase basis. The algorithm is expressed as follows; the function is executed 4 times per cycle:

$I_{bias},y(n)$ = Maximum [$I_{bias},y(n)$, I_{bias},y (n-1), ..., I_{bias},y (n – 3)]

1.3.4.2 Transient bias

If there is a sudden increase in the mean-bias measurement, an additional bias quantity is introduced in the bias calculation, on a per-phase basis. This quantity, named transient bias, decays exponentially. The transient bias resets to zero once the relay trips, or if the mean-bias quantity is below the Is1 setting. The transient bias is used to make the protection stable for external faults and allows for the time delay in CT saturation caused by small external fault currents and high X/R ratios. For single-end or double-end fed faults the differential current is dominant and the transient bias has no effect.

The transient bias is removed after the relay has tripped to avoid the possibility of chattering. It is also removed when Ibias is less than Is1 to avoid the possibility of residual values due to the numerical effects.

No transient bias is produced under load switching conditions. Also, no transient bias is generated when the CT comes out of saturation.

1.3.4.3 Maximum bias

The bias quantity used per phase for the percentage bias characteristic is the maximum "delayed" bias current calculated from all three phases:

$I_{bias},_{max}$ = Maximum [I_{bias},A, I_{bias},B, I_{bias},C]

The bias currents are available as measurements displays and in the fault records. These currents are the mean bias from all the windings before any additional bias is added.

The tripping characteristic of the differential protection device P34x has two knees. The first knee is dependent on the settings of **I_{s1}** and **K1**. The second knee of the tripping characteristic is defined by the setting **I_{s2}**. The lower slope provides sensitivity for internal faults. The higher slope provides stability under through fault conditions, since transient differential currents may be present due to current transformer saturation.

The characteristic equations for the three different ranges are given below. Figure 13 shows the tripping characteristic.

Characteristic equation for the range: $0 \le I_{bias} \le \frac{I_{s1}}{K_1}$:

$$I_{diff} = I_{s1}$$

Characteristic equation for the range: $\frac{I_{s1}}{K_1} \le I_{bias} \le I_{s2}$:

$$I_{diff} = K_1 \cdot I_{bias}$$

Characteristic equation for the range: $I_{bias} \ge I_{s2}$:

$$I_{diff} = K_1 \cdot I_{s2} + K_2\left(I_{bias} - I_{s2}\right)$$

K_1: gradient of characteristic in range $\frac{I_{s1}}{K_1} \leq I_{bias} \leq I_{s2}$

K_2: gradient of characteristic in range $I_{bias} \geq I_{s2}$

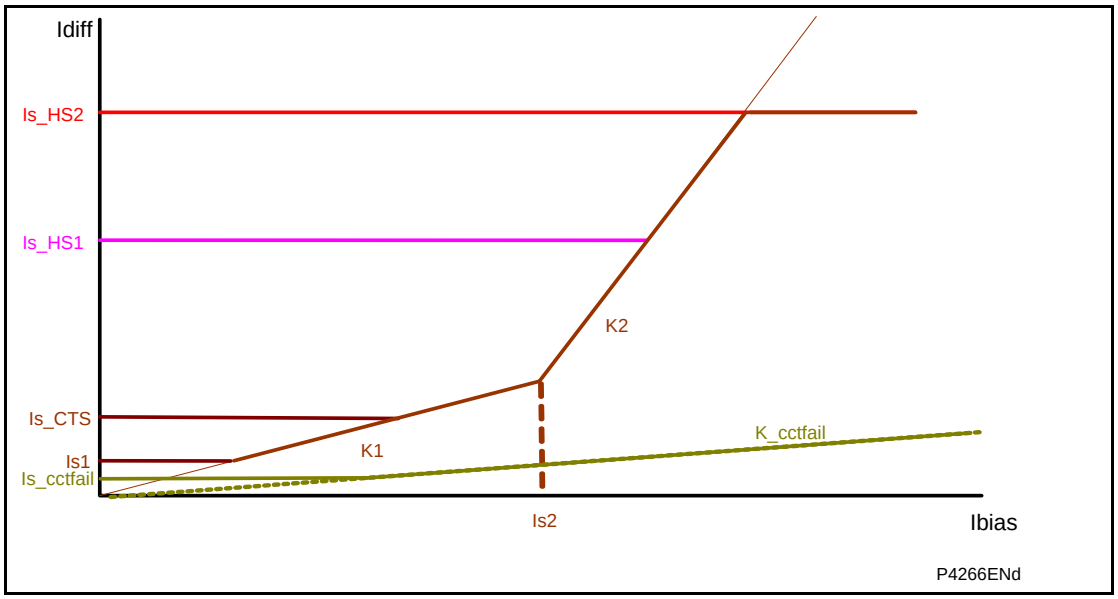


Figure 13: Tripping characteristic of differential protection

1.3.5 High-set differential protection function

The high set 1 algorithm uses a peak detection method to achieve fast operating times. The peak value is the largest absolute value in the latest 24 samples (latest cycle). Since the high set 1 algorithm uses a peak detection method, **Is-HS1** is set above the expected highest magnetizing inrush peak to maintain immunity to magnetizing inrush conditions. To declare high set 1 trip, two conditions must be fulfilled:

- The peak value of the differential current is greater than **Is-HS1** setting.
- The bias characteristic is in the operating region.

Above the adjustable threshold **Is-HS1** of the differential current, the P34x will trip without taking into account either the second harmonic blocking or the overfluxing blocking, but the bias current is considered. The high set 1 resets when the differential and bias currents are in the restraint area.

The high set 2 algorithm uses Fourier quantities. If the differential current exceeds the adjustable threshold **Is-HS2**, the bias current, the second harmonic and overfluxing restraints are no longer taken into account. As a result, the P34x issues a high set 2 trip regardless of the harmonic blocking or biased current. The high set 2 element resets when the differential current drops below 0.95*Is-HS2.

1.3.6 Low-set differential protection function

Transient bias is added for through fault stability. The transient bias is on a per-phase basis and is not affected by K1 or K2 settings.

Once the differential and bias currents are calculated, the following comparisons are made and an operate/restrained signal is obtained:

Flat slope: $I_{bias,\max} \leq \frac{I_{s1}}{K_1}$

$I_{diff} \geq I_{s1}$

K1 slope: $\frac{I_{s1}}{K_1} \le I_{bias,\max} \le I_{s2}$

$$I_{diff} \ge K_1 \cdot I_{bias.\max} + Transient \quad Bias$$

K2 slope: $I_{s2} \le I_{bias,\max}$

$$I_{diff} \ge K_1 \cdot I_{s2} + K_2 \cdot \left(I_{bias.\max} - I_{s2}\right) + Transient \quad Bias$$

A count strategy is used so that the protection operates slower near the boundary of operation. This approach is used to stabilize the relay under some marginal transient conditions. The protection trips on a count of 2, which is approximately 5 ms after fault detection. The count is increased to 4 if the differential current is within 0.5*Is1 of the threshold.

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1.3.7 Magnetizing inrush current blocking

The phenomenon of magnetizing inrush is a transient condition which occurs primarily when a transformer is energized. It is not a fault condition, and therefore does not require the operation of the protection, which, on the contrary must remain stable during the inrush transient.

Magnetizing inrush can occur under three conditions: initial, recover and sympathetic.

Initial Magnetization Inrush:

The initial magnetizing inrush may occur when energizing the transformer after a prior period of de-energization. This has the potential of producing the maximum magnetizing inrush.

The following figure portrays a transformer magnetizing characteristic. To minimize material costs, weight and size, transformers are generally operated near to the knee point of the magnetizing characteristic. Consequently, only a small increase in core flux above normal operating levels will result in a high magnetizing current.

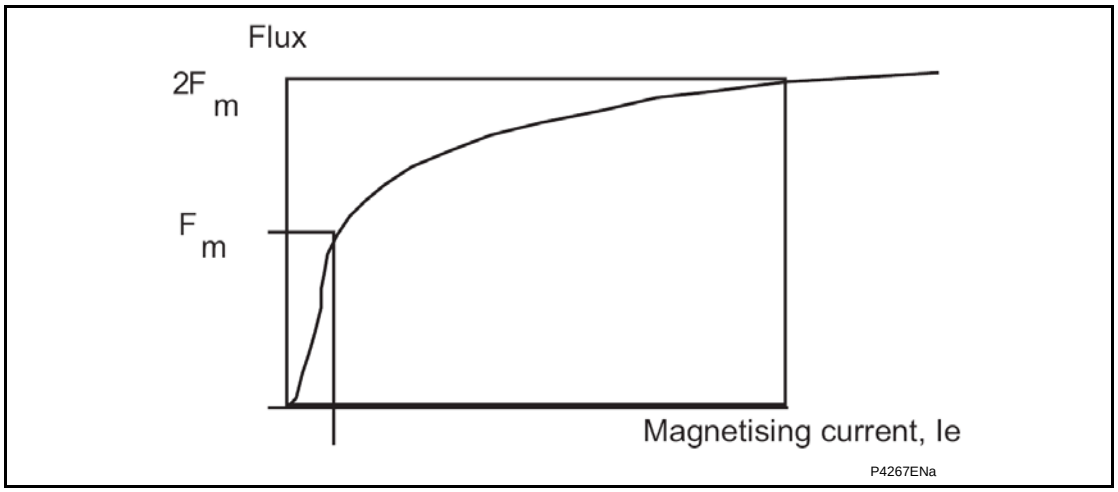


Figure 14: Transformer magnetizing characteristic

Under normal steady state conditions, the magnetizing current associated with the operating flux level is relatively small (2-5% of full load current). However, if a transformer winding is energized at a voltage zero, with no remnant flux, the flux level during the first voltage cycle (2 x normal max flux) will result in core saturation and in a high, non-sinusoidal magnetizing current waveform. This current is commonly referred to as magnetizing inrush current and may persist for several cycles. The maximum initial-magnetizing current may be as high as 8-30 times the full-load current. Resistance in the supply circuit and transformer and the stray losses in the transformer reduce the peaks of the inrush current such that it decays to the normal exciting current value. The time constant varies from 10 cycles to as long as 1

minute in very high inductive circuits. The following figure shows the magnetizing inrush phenomenon.

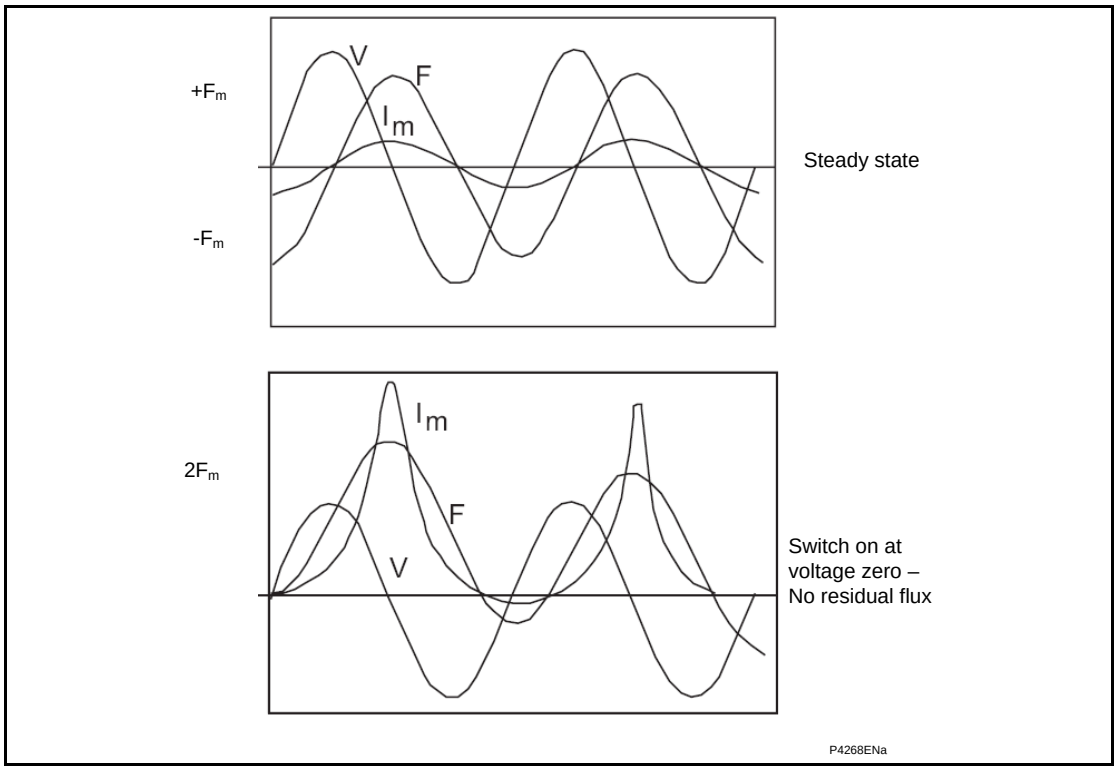


Figure 15: Magnetizing inrush phenomenon

The magnitude and duration of magnetizing inrush current waveforms are dependant on a number of factors such as transformer design, size, system fault level, point on wave of switching, number of banked transformers etc.

Some inrush will always occur in one or two phases and generally all three phases in a three phase circuit. The next figure indicates typical magnetizing inrush wave forms as seen by the differential protection.

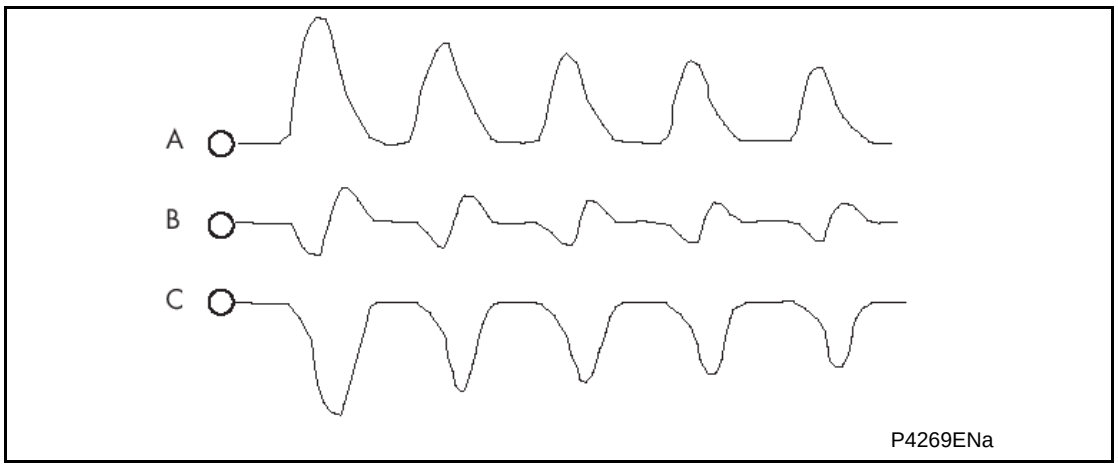


Figure 16: Magnetizing inrush current waveforms

Recovery magnetizing inrush:

As stated in IEEE Std. C37.91-2000, magnetizing inrush can be caused by any abrupt change of magnetizing voltage. These include the occurrence of a fault, the removal of the fault, change of character of a fault (a single phase fault evolving to two phase fault). The recovery inrush is when the voltage returns back to normal. The worst case of recovery

inrush occurs after a solid three phase external fault near a transformer bank is removed and the voltage gets back to normal.

Sympathetic magnetizing inrush:

According to IEEE Std. C37.91-2000, a severe magnetizing inrush may occur when energizing a transformer at a station at which at least one other transformer is already energized. This inrush will involve transformers that are already energized as well as transformers being energized. This inrush transient may be particularly long in duration. The inrush into the transformer being energized occurs during the opposite half-cycle to that of the already energized transformer. Therefore the net inrush into all transformers may approximate a sine wave of fundamental frequency, and therefore not operate the second harmonic blocking unit of the differential relay if it is protecting both parallel transformers.

As described above, when an unloaded transformer is energized, the inrush current at unfavourable points on wave such as for voltage zero may have values that exceed the transformer nominal current several times over. Since the high inrush current flows on the connected side only, the tripping characteristic of differential protection may give rise to a trip unless stabilizing action is taken. The fact that the inrush current has a high proportion of second harmonics offers a possibility of stabilization against tripping by the inrush current.

The P34x filters the differential current. The fundamental $I_{diff}(fn)$ and second harmonic components $I_{diff}(2*fn)$ of the differential current are determined. Second harmonic blocking is phase segregated. If the ratio $I_{diff}(2*fn)/I_{diff}(fn)$ exceeds a specific adjustable value in at least one phase in two consecutive calculations, and if the differential current is larger than 0.1 pu (minimum setting of Is1), tripping is blocked optionally in one of the following modes:

- Across all three phases
- Selectively for one phase

There will be no blocking if the differential current exceeds the set thresholds **Is-HS1** or **Is-HS2**.

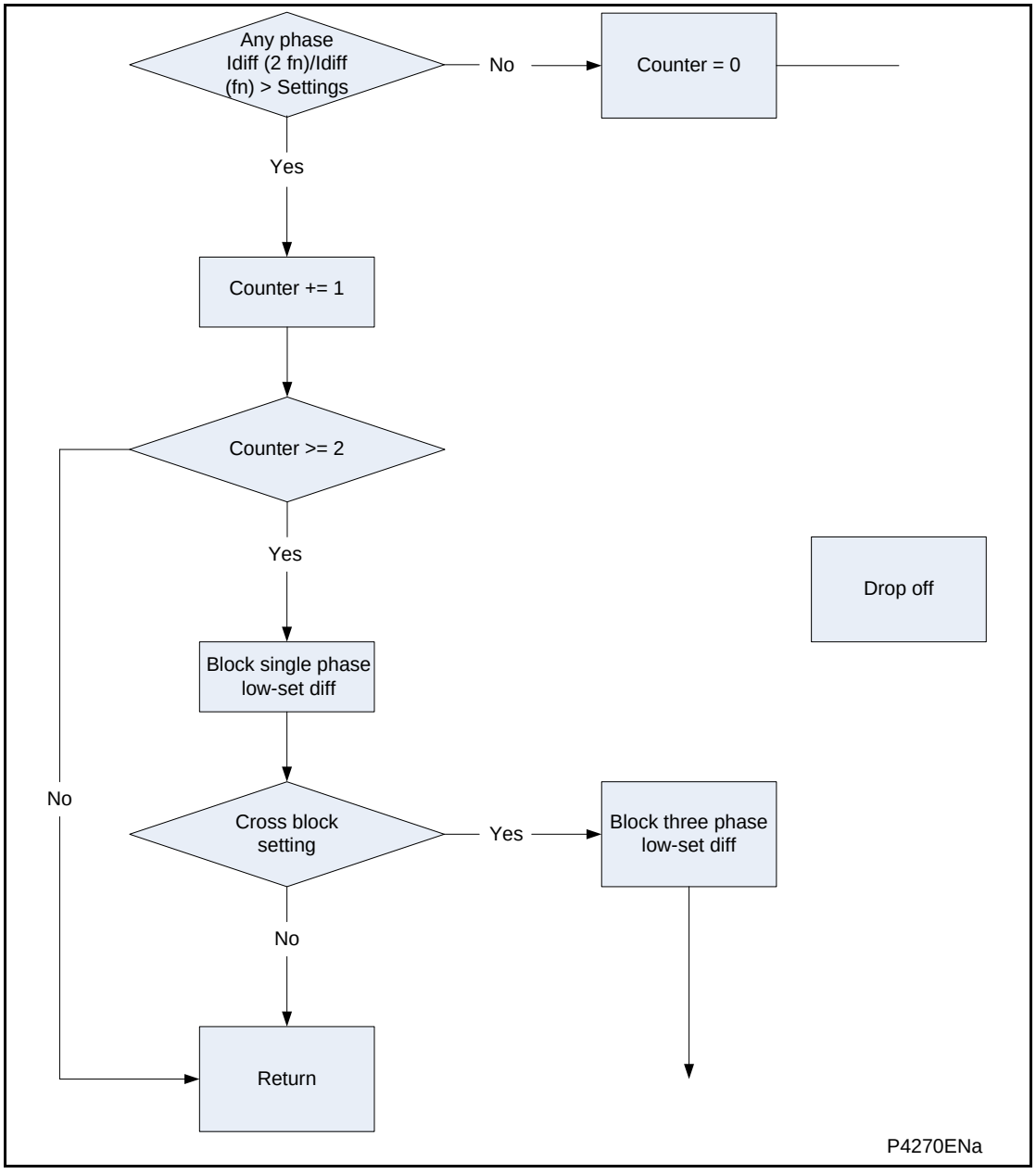


Figure 17: Inrush stabilization (second harmonic blocking)

1.3.8 Overfluxing restraint

If the transformer is loaded with a voltage in excess of the nominal voltage, saturation effects occur. Without stabilization, these could lead to differential protection tripping. The fact that the current of the protected object under saturation conditions has a high proportion of fifth harmonic serves as the basis of stabilization.

The P34x filters the differential current and determines the fundamental component $I_{diff}(fn)$ and the fifth harmonic component $I_{diff}(5 \cdot fn)$. If the ratio $I_{diff}(5 \cdot fn)/I_{diff}(fn)$ exceeds the set value Ih(5)%> in at least one phase in two consecutive calculations, and if the differential current is larger than 0.1 pu (minimum setting of Is1), tripping is blocked selectively for one phase.

To add some security, the 5th harmonic/fundamental ratio is 'AND' gated with the condition that the bias current in that phase is below the bias characteristic knee point setting Is2 (effectively confirming a load condition)

There will be no blocking if the differential current exceeds the set thresholds **Is-HS1** or **Is-HS2**.

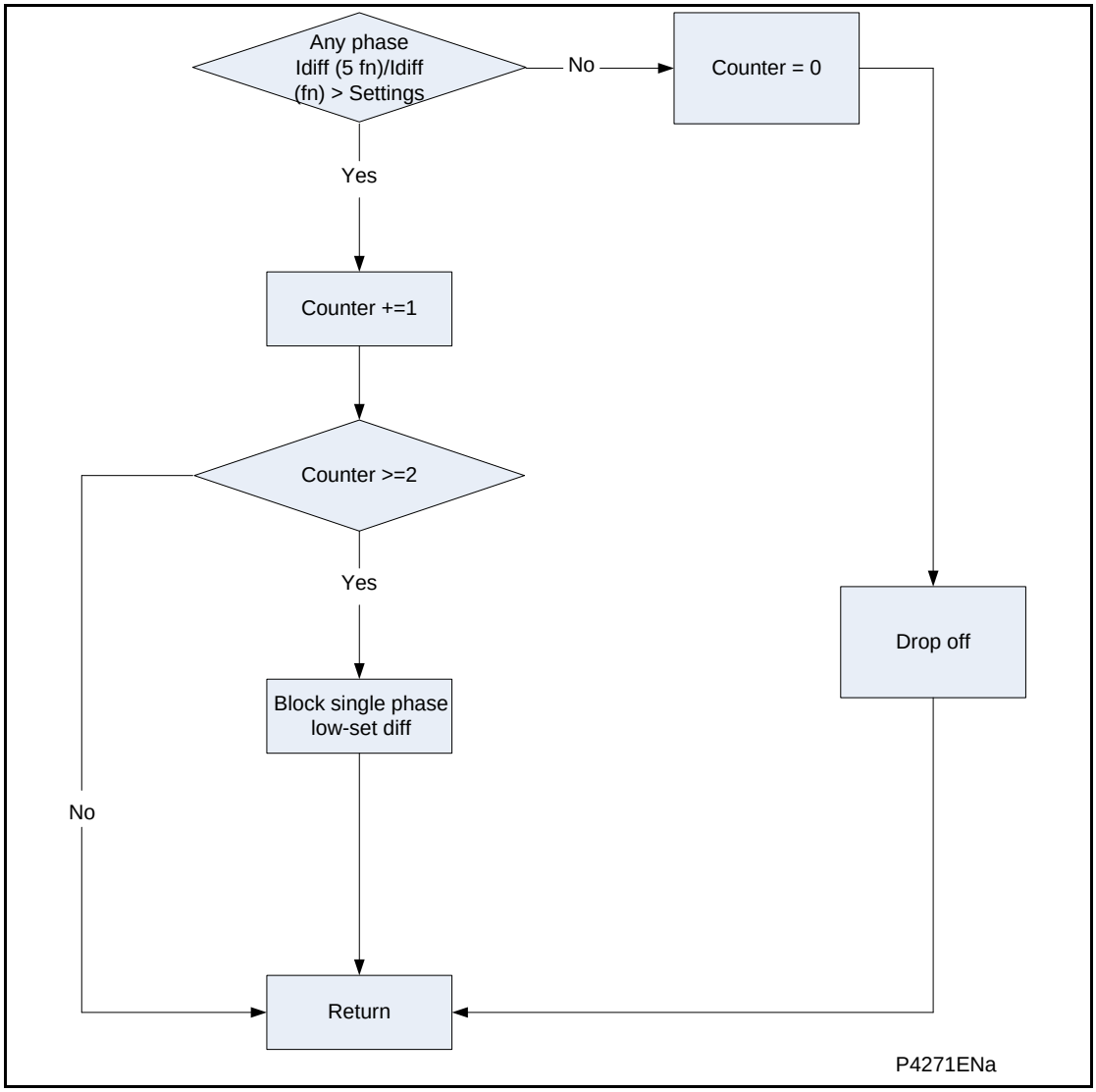


Figure 18: Overfluxing restraint

The following logic diagram shows the inhibiting of the differential algorithm by magnetizing inrush or overfluxing conditions:

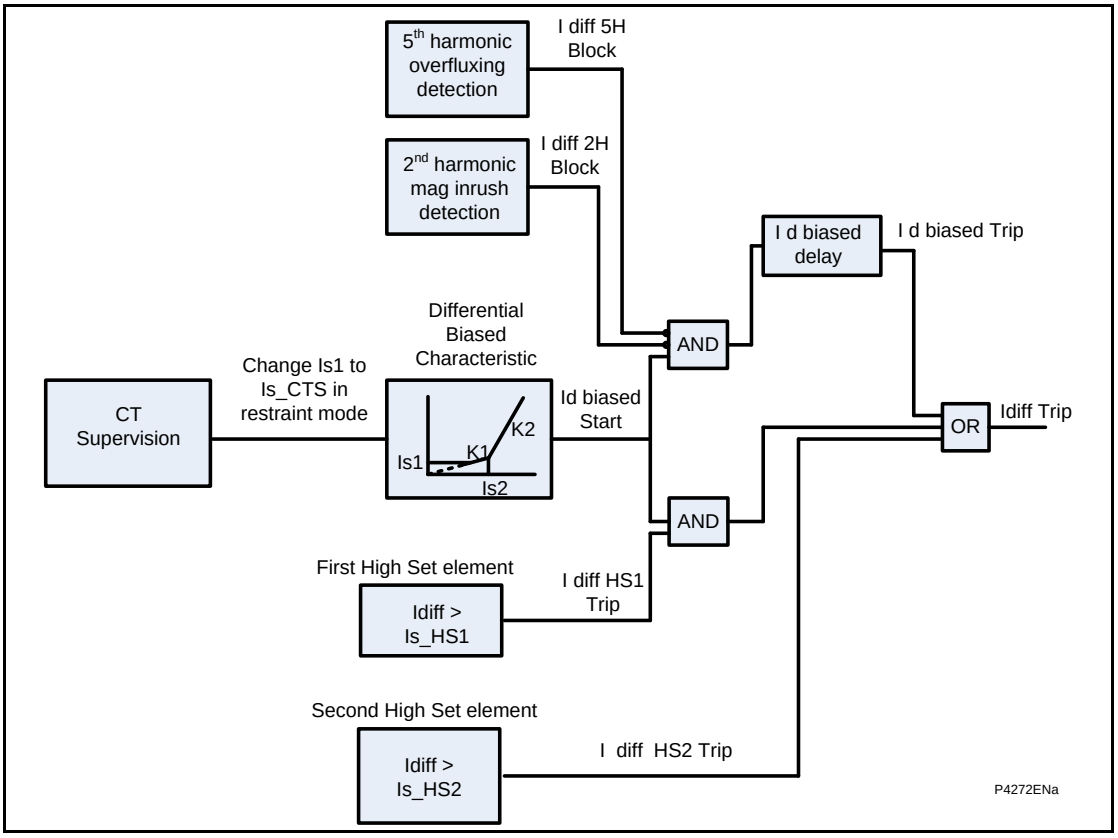


Figure 19: Differential protection

1.4 NPS overpower (32 NP)

For the interturn interlocking logic a single stage negative phase sequence apparent overpower element S2>1 is provided. The element has a start output and a time-delayed trip output.

The NPS apparent power is calculated as follows:

S2 = V2 x I2 (magnitude calculation only)

DDB signals are available to indicate the start and trip of the NPS apparent power protection, (Start: DDB 1139, Trip: DDB 881). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The negative sequence overpower protection start is mapped internally to the ANY START DDB signal – DDB 992.

The NPS overpower operation is shown in Figure 20.

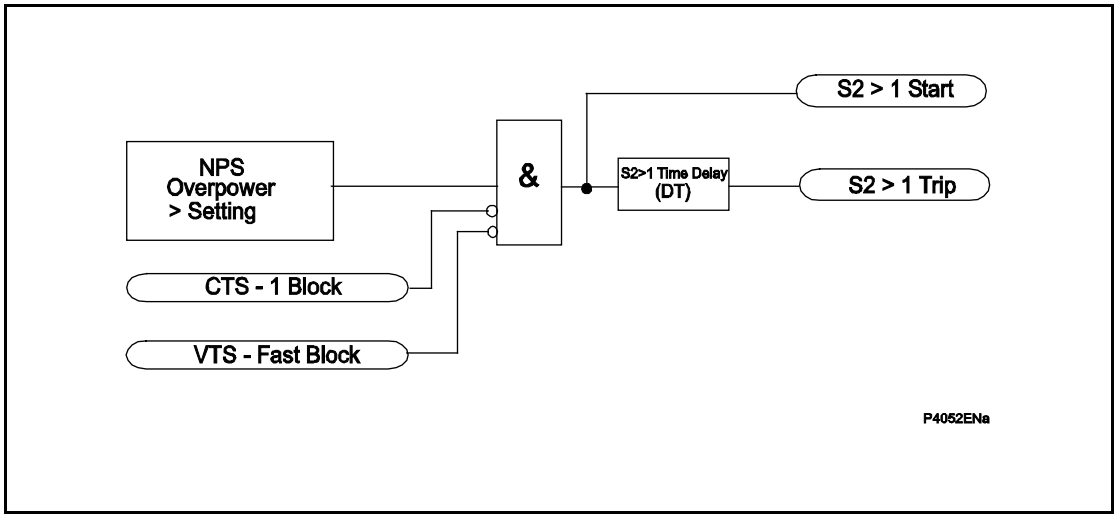


Figure 20: NPS overpower logic diagram

1.5 Overcurrent protection (50/51)

The overcurrent protection included in the P342-6 relays provides four-stage non-directional/ directional three-phase overcurrent protection with independent time delay characteristics. All overcurrent and directional settings apply to all three phases but are independent for each of the four stages. The 3 phase current source can be selected using the **I> CT Source – IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2** setting.

The first two stages of overcurrent protection have time-delayed characteristics which are selectable between inverse definite minimum time (**IDMT**), or definite time (**DT**) or a user curve (Default Curve 1/2/3/4). The third and fourth stages have definite time characteristics only.

Various methods are available to achieve correct relay co-ordination on a system; by means of time alone, current alone or a combination of both time and current. Grading by means of current is only possible where there is an appreciable difference in fault level between the two relay locations. Grading by time is used by some utilities but can often lead to excessive fault clearance times at or near source substations where the fault level is highest. For these reasons the most commonly applied characteristic in coordinating overcurrent relays is the IDMT type.

The inverse time delayed characteristics indicated above, comply with the following formula:

IEC curves

$$t = T \times \left(\frac{\beta}{(M^{\alpha} - 1)} + L \right)$$

or IEEE curves

$$t = TD \times \left(\frac{\beta}{(M^{\alpha} - 1)} + L \right)$$

where:

t = Operation time

β = Constant

M = I/Is

K = Constant

I = Measured current

Is = Current threshold setting

α = Constant

L = ANSI/IEEE constant (zero for IEC curves)

T = Time multiplier setting for IEC curves

TD = Time dial setting for IEEE curves

Curve description	Standard	β constant	α constant	L constant
Standard Inverse	IEC	0.14	0.02	0
Very Inverse	IEC	13.5	1	0
Extremely Inverse	IEC	80	2	0
Long Time Inverse	UK	120	1	0
Rectifier	UK	45900	5.6	0
Moderately Inverse	IEEE	0.0515	0.02	0.114
Very Inverse	IEEE	19.61	2	0.491
Extremely Inverse	IEEE	28.2	2	0.1217
Inverse	US	5.95	2	0.18
Short Time Inverse	US	0.16758	0.02	0.11858

Table 5: Inverse time curves

Note 1: The IEEE and US curves are set differently to the IEC/UK curves with regard to the time setting. A time multiplier setting (TMS) is used to adjust the operating time of the IEC curves and user programmable curves, whereas a time dial setting is employed for the IEEE/US curves. The menu is arranged such that if an IEC/UK/user programmable curve is selected, the **I> Time Dial** cell is not visible and vice versa for the TMS setting.

Note 2: The IEC/UK inverse characteristics can be used with a definite time reset characteristic, however, the IEEE/US curves may have an inverse or definite time reset characteristic. The following equation can used to calculate the inverse reset time for IEEE/US curves:

$$tRESET = \frac{TD \times S}{(1 - M^2)} \text{ in seconds}$$

where:

TD = Time dial setting for IEEE curves

S = Constant

M = I/Is

Curve description	Standard	S constant
Moderately Inverse	IEEE	4.85
Very Inverse	IEEE	21.6
Extremely Inverse	IEEE	29.1
Inverse	US	5.95
Short Time Inverse	US	2.261

Table 6: Reset curves

1.5.1 RI curve

The RI curve (electromechanical) has been included in the first and second stage characteristic setting options for phase overcurrent and both earth fault 1 and earth fault 2 protections. The curve is represented by the following equation.

$$t = K \times \left(\frac{1}{0.339 - \left({}^{0.236}/_{M} \right)} \right) \text{ in seconds}$$

With K adjustable from 0.1 to 10 in steps of 0.05

1.5.2 User programmable curves

As well as the standard curves as defined by various countries and standardising bodies, it is possible to program up to four custom curves Default Curve 1/2/3/4 using General Electric's User Programmable Curve Tool, described in the MiCOM S1 Agile Setting Application Software User Guide. This is a user-friendly tool by which users can create curves either by formula or by entering data points. Programmable curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves.

1.5.3 Timer hold facility

The first two stages of overcurrent protection in the P342-6 relays are provided with a timer hold facility, which may either be set to zero or to a definite time value. Setting of the timer to zero means that the overcurrent timer for that stage will reset instantaneously once the current falls below 95% of the current setting. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period. When the reset time of the overcurrent relay is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the relay will integrate the fault current pulses, thereby reducing fault clearance time.

The timer hold facility can be found for the first and second overcurrent stages as settings **I>1 tRESET** and **I>2 tRESET,** respectively. If an IEC inverse or DT operating characteristic is chosen, this time delay is set via the **I>1/2 tRESET** setting. If an IEEE/US operate curve is selected, the reset characteristic may be set to either definite time or inverse time as selected in cell **I>1/2 Reset Char**. If definite time (**DT**) is selected the **I>1/2 tRESET** cell may be used to set the time delay. If inverse time reset ('Inverse') is selected the reset time will follow the inverse time operating characteristic, modified by the time dial setting, selected for **I>1/2 Function.** If a user curve operate curve is selected, the reset characteristic may be set to either definite time or a user curve as selected in cell **I>1/2 Usr Rst Char**.

The functional logic diagram for non-directional overcurrent is shown in Figure 21.

A timer block input is available for each stage which will reset the overcurrent timers of all three phases if energized, taking account of the reset time delay if selected for the **I>1** and **I>2** stages (DDB 576-579). DDB signals are also available to indicate the start and trip of each phase of each stage of protection, (Starts: DDB 1040-1055, Trips: DDB 800-815). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Overcurrent protection starts 1/2/3/4 are mapped internally to the ANY START DDB signal – DDB 992.

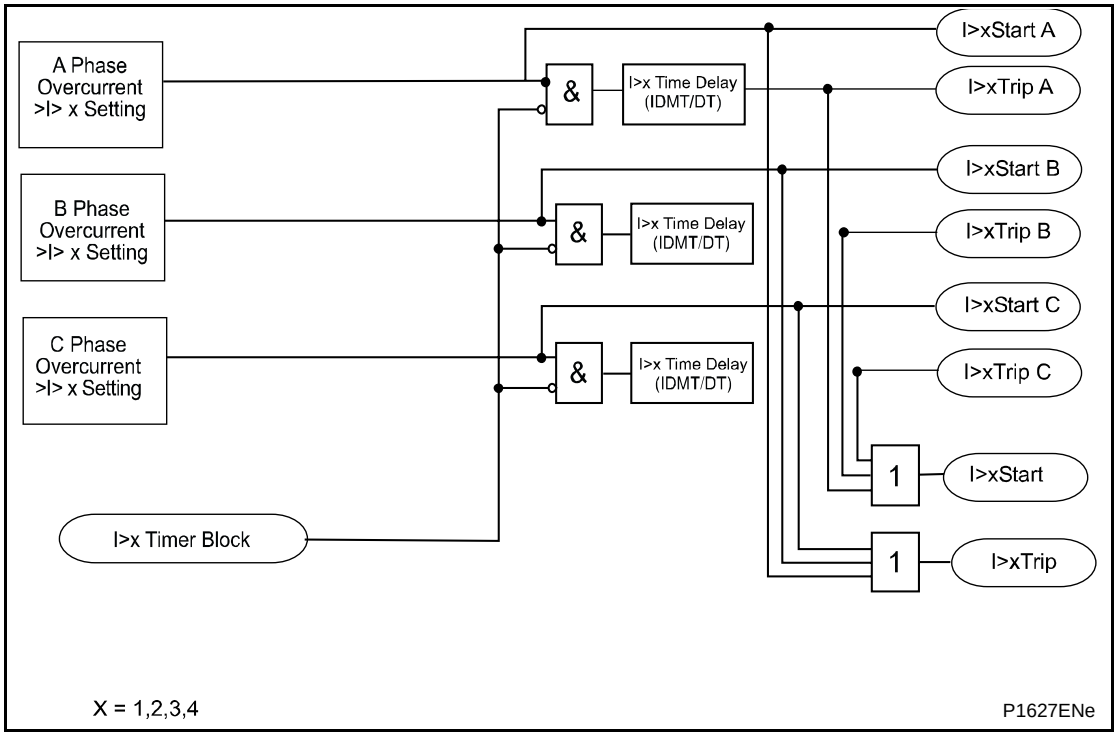


Figure 21: Non-directional overcurrent logic diagram

1.6 Directional overcurrent protection (67)

The phase fault elements of the P34x relays are internally polarized by the quadrature phase-phase voltages, as shown in the table below:

Phase of protection	Operate current	Polarizing voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

Table 7: Directional overcurrent, operate and polarizing signals

Under system fault conditions, the fault current vector will lag its nominal phase voltage by an angle dependent upon the system X/R ratio. It is therefore a requirement that the relay operates with maximum sensitivity for currents lying in this region. This is achieved by means of the relay characteristic angle (RCA) setting; this defines the angle by which the current applied to the relay must be displaced from the voltage applied to the relay to obtain maximum relay sensitivity. This is set in cell **I>Char Angle** in the overcurrent menu. On the P34x relays, it is possible to set characteristic angles anywhere in the range –95° to +95°.

The functional logic block diagram for directional overcurrent is shown in Figure 22.

The overcurrent level detector detects that the current magnitude is above the threshold and together with the respective polarizing voltage, a directional check is performed based on the following criteria:

Directional forward

-90° < (angle(I) - angle(V) - RCA) < 90°

Directional reverse

-90° > (angle(I) - angle(V) - RCA) > 90°

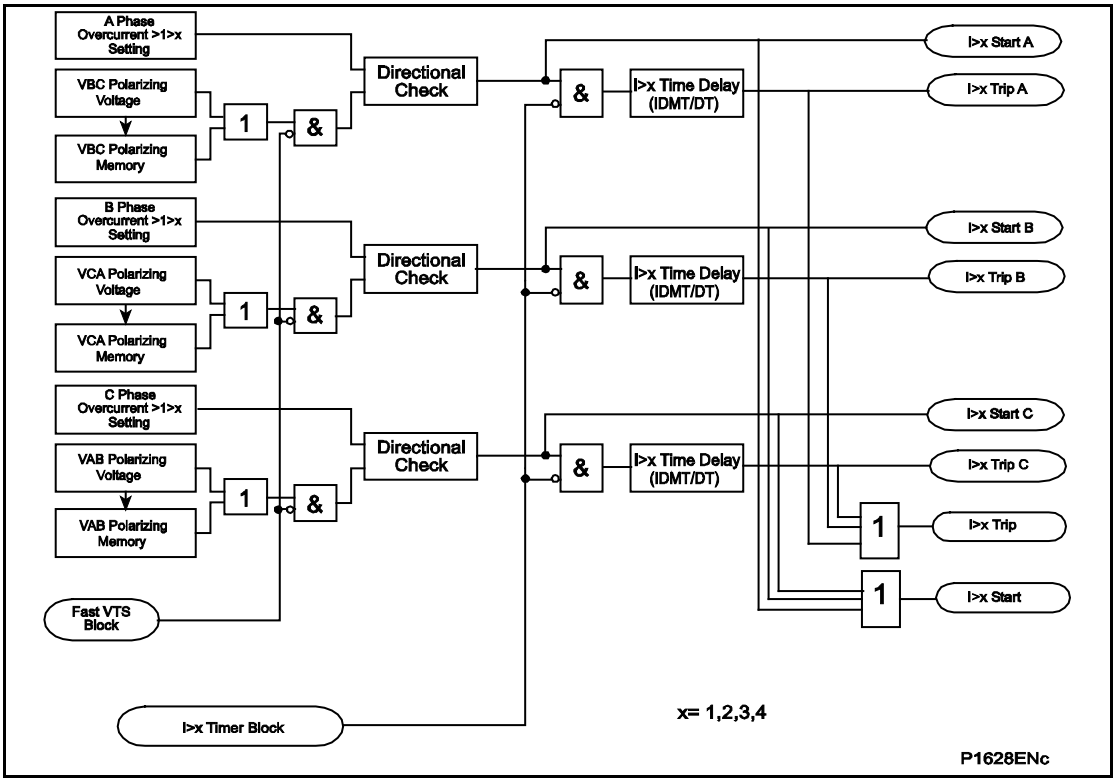


Figure 22: Directional overcurrent logic

Any of the four overcurrent stages may be configured to be directional noting that IDMT characteristics are only selectable on the first two stages. When the element is selected as directional, a VTS Block option is available. When the relevant bit is set to 1, operation of the Voltage Transformer Supervision (VTS), will block the stage if directionalized. When set to 0, the stage will revert to non-directional upon operation of the VTS.

1.6.1 Synchronous polarization

For a close up three-phase fault, all three voltages will collapse to zero and no healthy phase voltages will be present. For this reason, the P34x relays include a synchronous polarization feature that stores the pre-fault voltage information and continues to apply it to the directional overcurrent elements for a time period of 3.2 seconds. This ensures that either instantaneous or time delayed directional overcurrent elements will be allowed to operate, even with a three-phase voltage collapse.

1.7 Negative sequence overcurrent protection (NPS) (46 OC)

The P342-6 relays provide four independent stages of negative phase sequence overcurrent protection. Each stage has a current pick up setting **I2>n Current Set**, and is time delayed in operation by the adjustable timer **I2>n Time Delay**. The user may choose to directionalize operation of the elements, for either forward or reverse fault protection for which a suitable relay characteristic angle may be set. Alternatively, the elements may be set as non-directional. For the negative phase sequence directional elements to operate, the relay must detect a polarizing voltage above a minimum threshold, **I2> V2pol Set**. The 3 phase current source can be selected using the **I2> CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting.

When the element is selected as directional, a VTS Block option is available. When the relevant bit set to 1, operation of the Voltage Transformer Supervision (VTS), will block the stage if directionalized. When set to 0, the stage will revert to non-directional upon operation of the VTS.

The negative phase sequence overcurrent element has a current pick up setting **I2>x Current Set**, and is time delayed in operation by an adjustable timer **I2>x Time Delay**. The user may choose to directionalize operation of the element, for either forward or reverse fault protection for which a suitable relay characteristic angle may be set. Alternatively, the element may be set as non-directional.

A timer block input is available for each stage which will reset the NPS overcurrent timers of the relevant stage if energized, (DDB 583-586). All 4 stages can be blocked by energizing the inhibit DDB signal via the PSL (I2> Inhibit: DDB 582). DDB signals are also available to indicate the start and trip of each stage of protection, (Starts: DDB 1064-1067, Trips: DDB 824-827). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Negative sequence overcurrent protection starts 1/2/3/4 are mapped internally to the ANY START DDB signal – DDB 992.

The non-directional and directional operations are shown in Figure 23 and Figure 24.

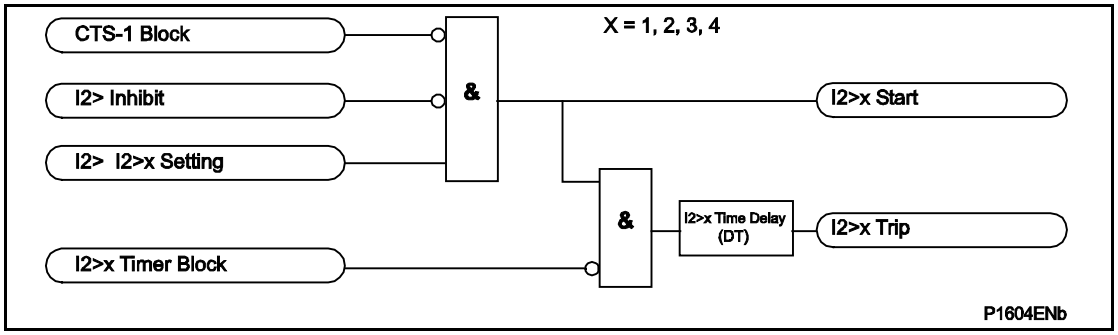


Figure 23: Negative sequence overcurrent non-directional operation

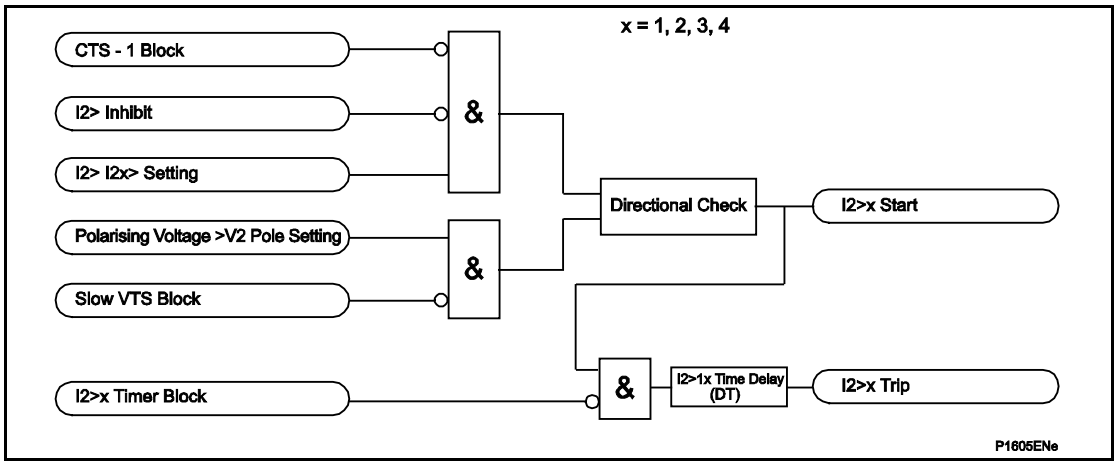


Figure 24: Directionalizing the negative phase sequence overcurrent element

Directionality is achieved by comparison of the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (I2> Char Angle) is chosen to provide optimum performance.

This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the center of the directional characteristic.

For the negative phase sequence directional elements to operate, the relay must detect a polarizing voltage above a minimum threshold, **I2> V2pol Set**. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the relay.

1.8 System back-up protection (51V/21)

Both voltage dependant overcurrent and under impedance are provided in the P34x relay for system back-up protection. The operation of the elements are described in the following sections.

The functions operate from the phase currents measured by the IA, IB and IC measurement inputs in the relay.

A timer block input is available for the voltage dependent overcurrent and underimpedance System Backup protection elements which will reset the timers of the relevant elements if energized, (VDepOC Timer Block, DDB 608 and UnderZ Timer Block, DDB 609). DDB signals are also available to indicate a three-phase and per phase start and trip, (Voltage dependent overcurrent Starts: DDB 1127-1130, Voltage dependent overcurrent Trips: DDB 868-871, Underimpedance Starts: DDB 1131-1138, Underimpedance Trips: DDB 872-879). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The protection starts for each element are mapped internally to the ANY START DDB signal – DDB 992.

1.8.1 Voltage dependant overcurrent protection

The generator terminal voltage will drop during fault conditions and so a voltage measuring element can be used to control the current setting of this element. On detection of a fault the current setting is reduced by a factor K. This ensures faults are cleared in spite of the presence of the generator decrement characteristic. Line voltages are used to control each phase overcurrent element as shown below.

Phase current	Control voltage
Ia	Vab
Ib	Vbc
Ic	Vca

Table 8: Voltages used for Phase Overcurrent elements

A single stage, non-directional overcurrent element is provided. The element has a time delayed characteristic that can be set as either Inverse Definite Minimum Time (IDMT) or Definite Time (DT) or a user curve (Default Curve 1/2/3/4). The element can be blocked via a relay input so that the element can be integrated into a blocked overcurrent protection scheme.

The element can be fed from CTs at the terminal or neutral end of the generator.

The voltage dependent overcurrent element can be disabled or set in one of two modes, voltage controlled overcurrent or voltage restrained overcurrent.

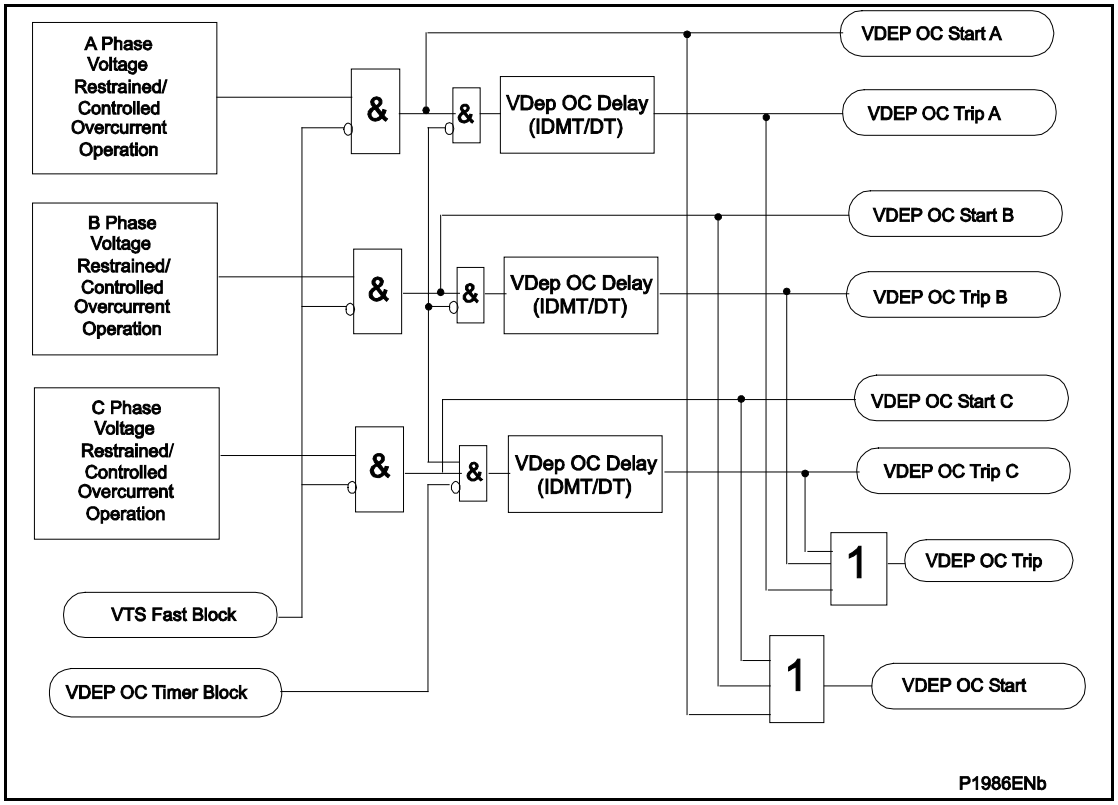


Figure 25: Voltage restrained/controlled overcurrent logic diagram

1.8.1.1 Voltage controlled overcurrent protection

In this mode of operation, the under voltage detector is used to produce a step change in the relay current setting (from **V Dep OC I> Set** to **V Dep OC k Set** x **V Dep OC I> Set**), when voltage falls below the voltage setting, **V Dep OC V<1 Set**. Under load conditions the relay can have a high current setting greater than full load current. Under fault conditions the relay is switched to a more sensitive setting leading to fast fault clearance. The operating characteristic of the current setting when voltage controlled mode is selected is shown in Figure 26.

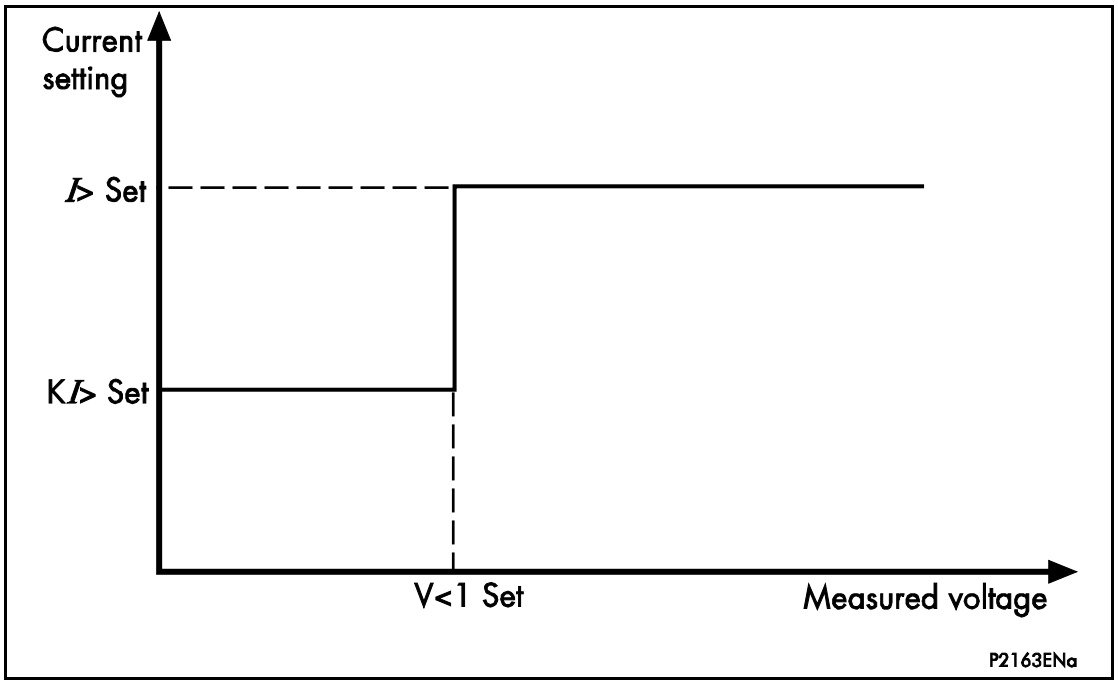


Figure 26: Modification of current pickup level for voltage controlled overcurrent protection

Where the generator is directly connected to a busbar, voltage controlled overcurrent protection may be preferred.

The voltage controlled overcurrent protection is provided with a timer hold facility. Setting the hold timer to a value other than zero delays the resetting of the protection element timers for this period.

If an IEC inverse or DT operating characteristic is chosen, this hold time delay is set via the **V Dep OC tRESET** setting.

If an IEEE/US operate curve is selected, the reset characteristic may be set to either definite time or inverse time as selected in cell **V Dep OC Reset Char**. If definite time (**DT**) is selected the **V Dep OC tRESET** cell may be used to set the time delay, as above. If inverse time reset (**Inverse**) is selected the reset time will follow the inverse time operating characteristic, modified by the time dial setting, selected for **V Dep OC Function**. If a user curve operate curve is selected, the reset characteristic may be set to either definite time or a user curve as selected in cell **V Dep OC Usr Rst**.

1.8.1.2 Voltage restrained overcurrent protection

In voltage restrained mode the effective operating current of the protection element is continuously variable as the applied voltage varies between two voltage thresholds, **V Dep OC V<1 Set** and **V Dep OC V<2 Set**, as shown in Figure 27. In this mode, it is quite difficult to determine the behavior of the protection function during a fault. This protection mode is, however, considered to be better suited to applications where the generator is connected to the system via a generator transformer.

With indirect connection of the generator, a solid phase-phase fault on the local busbar will result in only a partial phase-phase voltage collapse at the generator terminals.

The P34x voltage-restrained current setting is related to measured voltage as follows:

For V > Vs1: Current setting (I_s) = I>

For Vs2 < V < Vs1: Current setting (I_s) = $K.I> + (I > - K. I>) \left(\frac{V - Vs2}{Vs1 - Vs2} \right)$

For V < Vs2: Current setting (I_s) = K.I>

Where:

I> = **V Dep OC I> Set**

I_s = Current setting at voltage V

V = Voltage applied to relay element

Vs1 = **V Dep OC V<1 Set**

Vs2 = **V Dep OC V<2 Set**

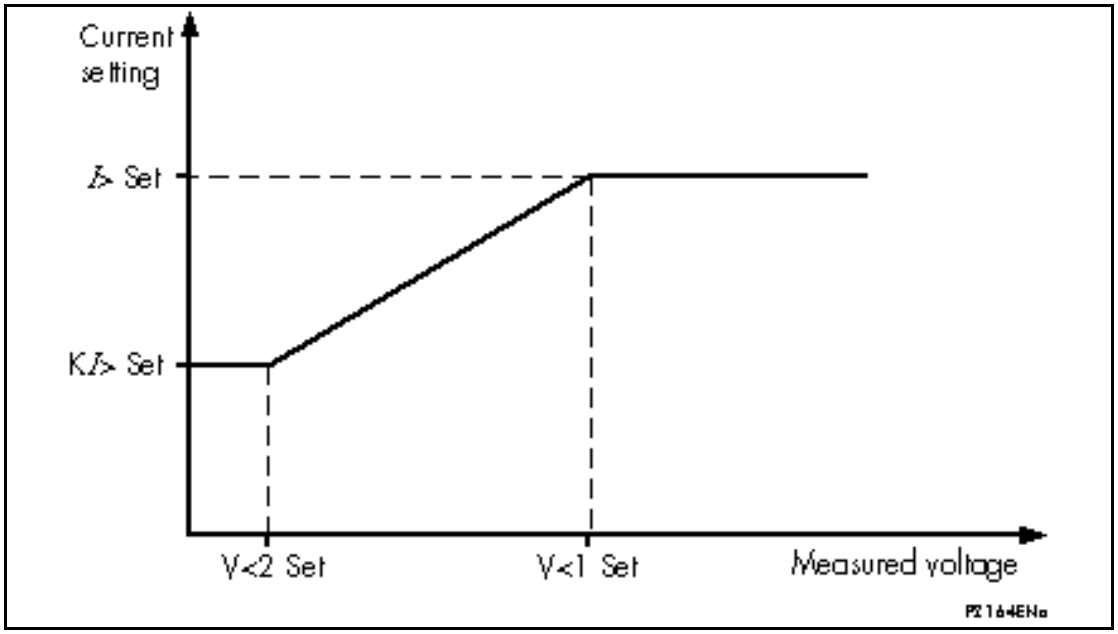


Figure 27: Modification of current pickup level for voltage restrained overcurrent protection

The voltage restrained overcurrent protection is provided with a timer hold facility. Setting the hold timer to a value other than zero, delays the resetting of the protection element timers for this period.

If an IEC inverse or DT operating characteristic is chosen, this hold time delay is set via the **V Dep OC tRESET** setting.

If an IEEE/US operate curve is selected, the reset characteristic may be set to either definite time or inverse time as selected in cell **V Dep OC Reset Char**. If definite time (DT) is selected the **V Dep OC tRESET** cell may be used to set the time delay, as above. If inverse time reset (**Inverse**) is selected the reset time will follow the inverse time operating characteristic, modified by the time dial setting, selected for **V Dep OC Function.** If a user curve operate curve is selected, the reset characteristic may be set to either definite time or a user curve as selected in cell **V Dep OC Usr Rst**.

1.8.1.3 Under impedance protection

The P342-6 relays provide two independent stages of underimpedance protection. The under impedance elements operate with a time delayed three-phase non-directional impedance characteristic, shown in Figure 28.

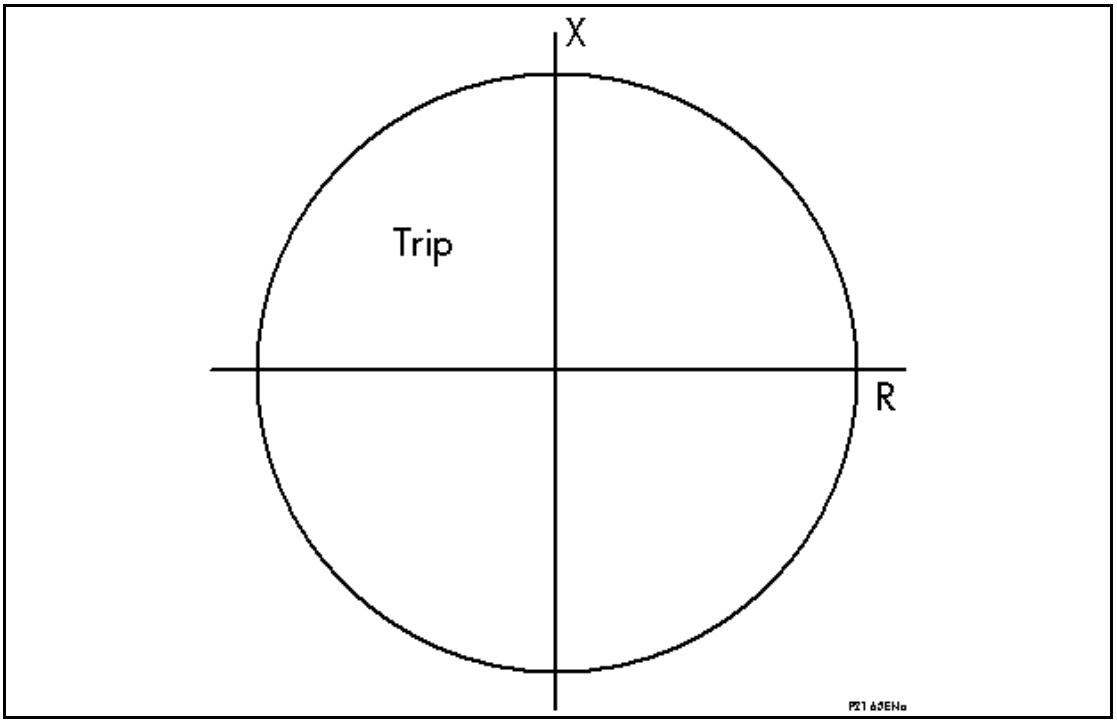


Figure 28: Under impedance element tripping characteristic

Impedance for each phase is calculated as shown:

$$Za = \frac{Vab}{Ia} \qquad Zb = \frac{Vbc}{Ib} \qquad Zc \frac{Vca}{Ic}$$

With rated voltage applied, the elements operates as a definite time overcurrent relay. It operates at a lower current as the voltage reduces, hence the elements are similar to a voltage restrained overcurrent element, operating with a definite time characteristic.

The under impedance protection is provided with a timer hold facility. Setting the hold timer, **Z<1/2 tRESET**, to a value other than zero, delays the resetting of the protection element timer for this period.

The minimum phase current and the line voltage required for the P342-6 under impedance protection to work is 20 mA and 2 V (In = 1 A, Vn = 100/120 V) and 100 mA and 8 V (In = 5 A, Vn = 380/480 V).

Note: Under impedance consists of separate three-phase elements and the checking is done on a per phase basis that is the inhibition of one phase will not affect the other phases.

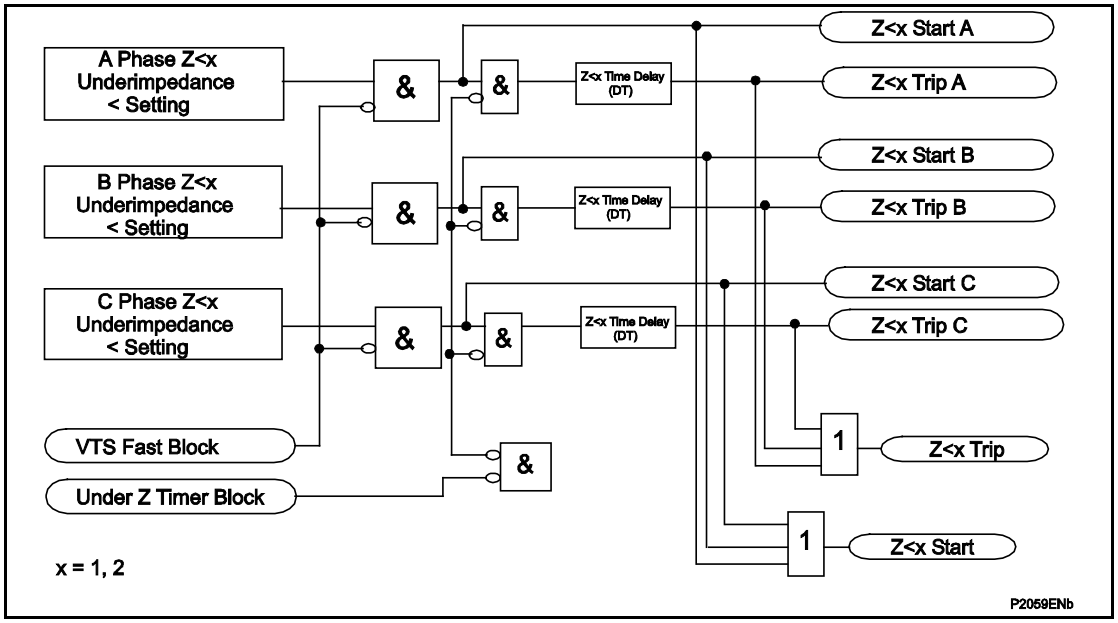


Figure 29: Under impedance logic diagram

1.9 Undervoltage protection (27)

Both the under and overvoltage protection functions can be found in the relay menu **Volt Protection**. The undervoltage protection included within the P34x relays consists of three independent stages. These are configurable as either phase to phase or phase to neutral measuring within the **V<Measur't mode** cell.

Note: If the undervoltage protection is set for phase-phase operation then the DDB signals V<1/2/3 Start/Trip A/AB, V<1/2/3 Start/Trip B/BC, V<1/2/3 Start/ Trip C/CA refer to V<1/2/3 Start/Trip AB and V<1/2/3 Start/Trip BC and V<1/2/3 Start/Trip CA. If set for phase-neutral then the DDB signals V<1/2/3 Start/Trip A/AB, V<1/2/3 Start/Trip B/BC, V<1/2/3 Start/Trip C/CA refer to V<1/2/3 Start/Trip A and V<1/2/3 Start/Trip B and V<1/2/3 Start/Trip C.

Stage 1 may be selected as IDMT, DT, Default Curve 1/2/3/4 or Disabled, within the **V<1 Function** cell. Stage 2 and 3 are is DT only and are enabled/disabled in the **V<2/3 status** cells.

The IDMT characteristic available on the first stage is defined by the following formula:

t = K / (M - 1)

Where:

K = Time multiplier setting

t = Operating time in seconds

M = Measured voltage/relay setting voltage (V< Voltage Set)

As well as the standard IDMT curve, it is possible to program up to four custom curves **Default Curve 1/2/3/4** using General Electric's User Programmable Curve Tool, described in the MiCOM S1 Agile Setting Application Software User Guide. This is a user-friendly tool by which users can create curves either by formula or by entering data points. Programmable curves can help to match more closely the withstand characteristics of the electrical equipment than standard curves. User curves can be useful to match the fault ride through characteristic.

Three stages are included to provide both alarm and trip stages, where required. Alternatively, different time settings may be required depending upon the severity of the voltage dip, i.e. motor loads will be able to withstand a small voltage depression for a longer time than if a major voltage excursion were to occur.

Outputs are available for single or three-phase conditions via the **V<Operate Mode** cell.

Each stage of undervoltage protection can be blocked by energizing the relevant DDB signal via the PSL, (DDB 601, DDB 602, DDB 591). DDB signals are also available to indicate a three-phase and per phase start and trip, (Starts: DDB 1103-1118, Trips: DDB 847-854, 908-911).

The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Undervoltage protection starts are mapped internally to the ANY START DDB signal – DDB 992.

The logic diagram of the undervoltage function is shown in Figure 30.

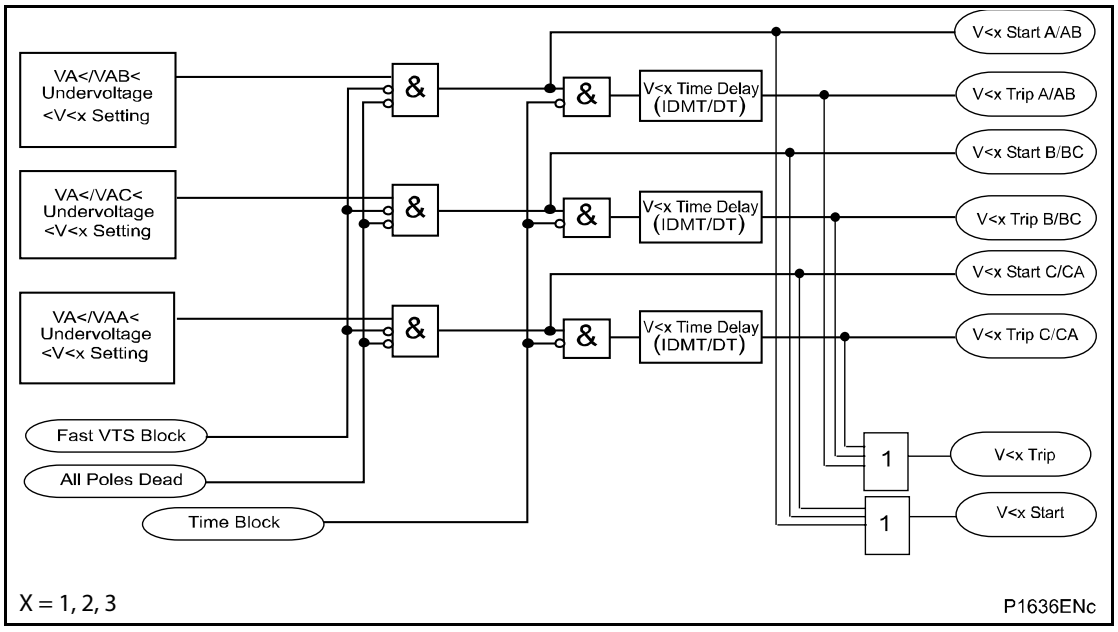


Figure 30: Undervoltage - single and three phase tripping mode (single stage)

When the protected feeder is de-energized, or the circuit breaker is opened, an undervoltage condition would be detected. Therefore, the **V<Poledead Inh** cell is included for each of the two stages to block the undervoltage protection from operating for this condition. If the cell is enabled, the relevant stage will become inhibited by the in-built pole dead logic within the relay. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase.

1.10 Overvoltage protection (59)

Both the under and overvoltage protection functions can be found in the relay menu **Volt Protection**. The overvoltage protection included within the P34x relays consists of two independent stages. These are configurable as either phase to phase or phase to neutral measuring within the **V>Measur't mode** cell.

Note: If the overvoltage protection is set for phase-phase operation then the DDB signals V>1/2 Start/Trip A/AB, V>1/2 Start/Trip B/BC, V>1/2 Start/Trip C/CA refer to V>1/2 Start/Trip AB and V>1/2 Start/Trip BC and V>1/2 Start/Trip CA. If set for phase-neutral then the DDB signals V>1/2 Start/Trip A/AB, V>1/2 Start/Trip B/BC, V>1/2 Start/Trip C/CA refer to V>1/2 Start/Trip A and V>1/2 Start/Trip B and V>1/2 Start/Trip C.

Stage 1 may be selected as IDMT, DT, Default Curve 1/2/3/4 or Disabled, within the **V>1 Function** cell. Stage 2 is DT only and is enabled/disabled in the **V>2 status** cell.

The IDMT characteristic available on the first stage is defined by the following formula:

t = K / (M – 1)

Where:

K = Time multiplier setting

t = Operating time in seconds

M = Measured voltage / relay setting voltage (V> Voltage Set)

As well as the standard IDMT curve, it is possible to program up to four custom curves **Default Curve 1/2/3/4** using General Electric's User Programmable Curve Tool, described in the MiCOM S1 Agile Setting Application Software User Guide. This is a user-friendly tool by which users can create curves either by formula or by entering data points. Programmable curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves.

A timer block input is available for each stage which will reset the undervoltage timers of the relevant stage if energized, (DDB 598, DDB 599). DDB signals are also available to indicate a three-phase and per phase start and trip, (Starts: DDB 1094-1101, Trips: DDB 838-845). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Overvoltage protection starts are mapped internally to the ANY START DDB signal – DDB 992.

The logic diagram of the overvoltage function is shown in Figure 31.

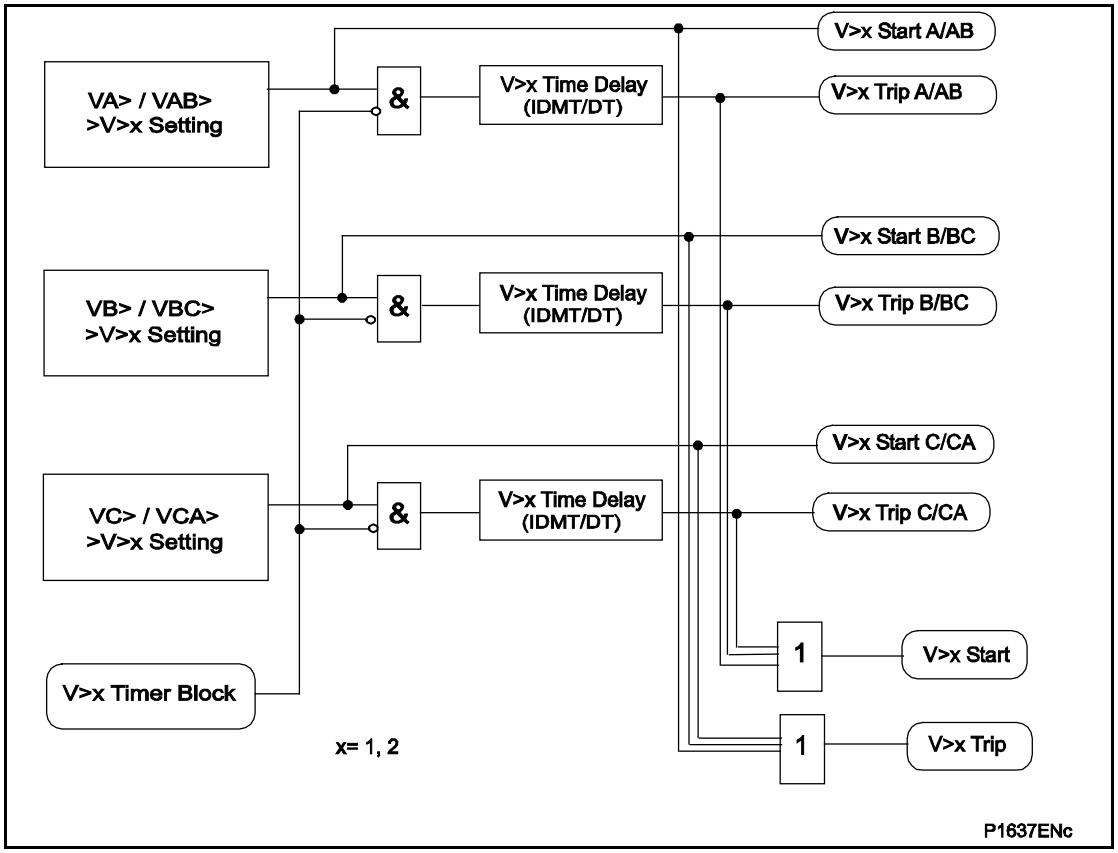


Figure 31: Overvoltage - single and three phase tripping mode (single stage)

1.11 Negative sequence overvoltage protection (47)

The P34x relay includes a negative phase sequence overvoltage element. This element monitors the input voltage rotation and magnitude (normally from a bus connected voltage transformer) and may be interlocked with the generator circuit breaker to prevent the machine from being energized whilst incorrect phase rotation exists.

This single stage is selectable as definite time only and is enabled within the **V2>status** cell.

The logic diagram for the negative sequence overvoltage protection is shown in Figure 32.

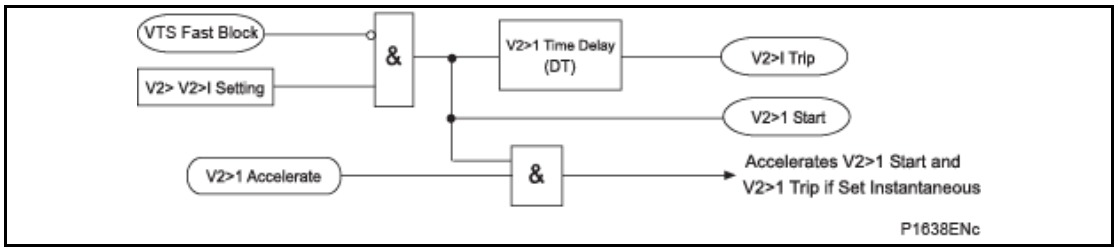


Figure 32: Negative sequence overvoltage element logic

DDB signals are available to indicate a start and a trip, (Start: DDB 1102, Trip: DDB 846). There is also a signal to accelerate the NPS overvoltage protection start (V2>1 Accelerate: DDB 600) which accelerates the operating time of the function from typically 80 ms to 40 ms when set to instantaneous.

The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The NPS overvoltage protection start is mapped internally to the ANY START DDB signal – DDB 992.

1.12 Frequency protection (81U/81O)

The P34x relays include 4 stages of underfrequency and 2 stages of overfrequency protection to facilitate load shedding and subsequent restoration. The underfrequency stages may be optionally blocked by a pole dead (CB Open) condition. All the stages may be enabled/disabled in the **F<n Status** or **F>n Status** cell depending on which element is selected.

The logic diagram for the underfrequency logic is as shown in Figure 33. Only a single stage is shown. The other 3 stages are identical in functionality.

If the frequency is below the setting and not blocked the DT timer is started. Blocking may come from the All_Poledead signal (selectively enabled for each stage) or the underfrequency timer block.

If the frequency cannot be determined (Frequency Not Found, DDB 1295), the function is also blocked.

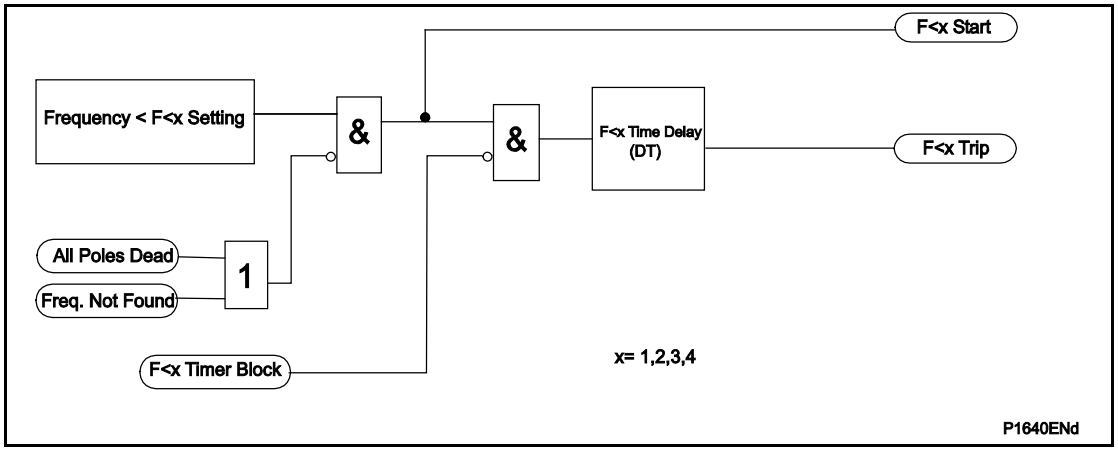


Figure 33: Underfrequency logic (single stage)

OP

The functional logic diagram is for the overfrequency function as shown in Figure 34. Only a single stage is shown as the other stages are identical in functionality. If the frequency is above the setting and not blocked the DT timer is started and after this has timed out the trip is produced. Blocking may come from the All_Poledead signal (selectively enabled for each stage) or the overfrequency timer block.

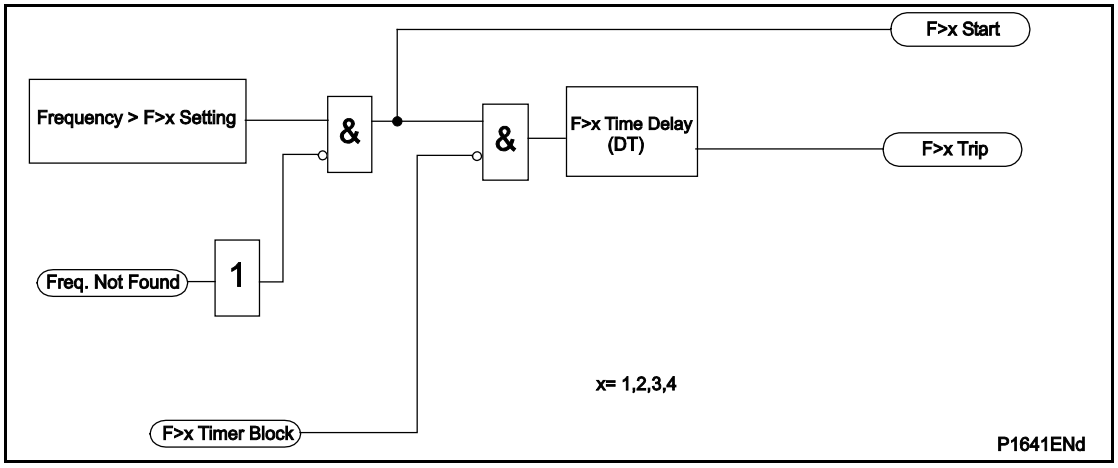


Figure 34: Overfrequency logic (single stage)

A timer block input is available for each stage which will reset the under and overfrequency timers of the relevant stage if energized, (DDB 626-629, DDB 630-631). DDB signals are also available to indicate start and trip of each stage, (Starts: DDB 1172-1175, DDB 1176-1177, Trips: DDB 916-919, DDB 920-921).

The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The under and overfrequency protection starts are mapped internally to the ANY START DDB signal – DDB 992.

1.13 Generator turbine abnormal frequency protection (81 AB)

Six bands of generator abnormal protection are provided within the P34x relays. Each band has its own frequency limit settings and an individual accumulative time measurement. Operation within each of these bands is monitored and the time added to a cumulative timer, stored within the battery backed RAM. This ensures that on loss of auxiliary supply to the relay, the information is not lost. An individual dead band time delay setting is provided for each band. Within this dead band time delay, the frequency is allowed to stay inside the band without initiating the accumulative time measurement. This delay allows the blade's resonance during under frequency conditions to be established first, avoiding unnecessary accumulation of time. The delay therefore does not contribute to the accumulated time.

Note: The dead band delay has no effect on the initiation of the start signals. Time accumulation will stop and all the start signals will be reset if the Frequency Not Found DDB 1068 is set.

The amount of time spent in each band can be viewed in the **MEASUREMENTS 3** column in the relay. The maximum allowable time in each band is 1000 hours (3600000s), beyond which no more accumulation will be made. An individual reset cell is available in the **MEASUREMENTS 3** column in the relay for each accumulative time measurement to be independently reset to zero.

It is recommended the turbine abnormal frequency protection system be in-service whenever the unit is synchronized to the system, or while separated from the system but supplying auxiliary load. An inhibit signal is available to inhibit the time accumulation when the generator is off-line, that is the circuit breaker is open.

The trip output is latched and can only be reset if any of the following conditions occur:

1. The accumulative time is reset, or
2. The corresponding band is disabled, or
3. The entire abnormal frequency protection is disabled, or
4. The Inhibit DDB 'Turbine F Inh' is energized.

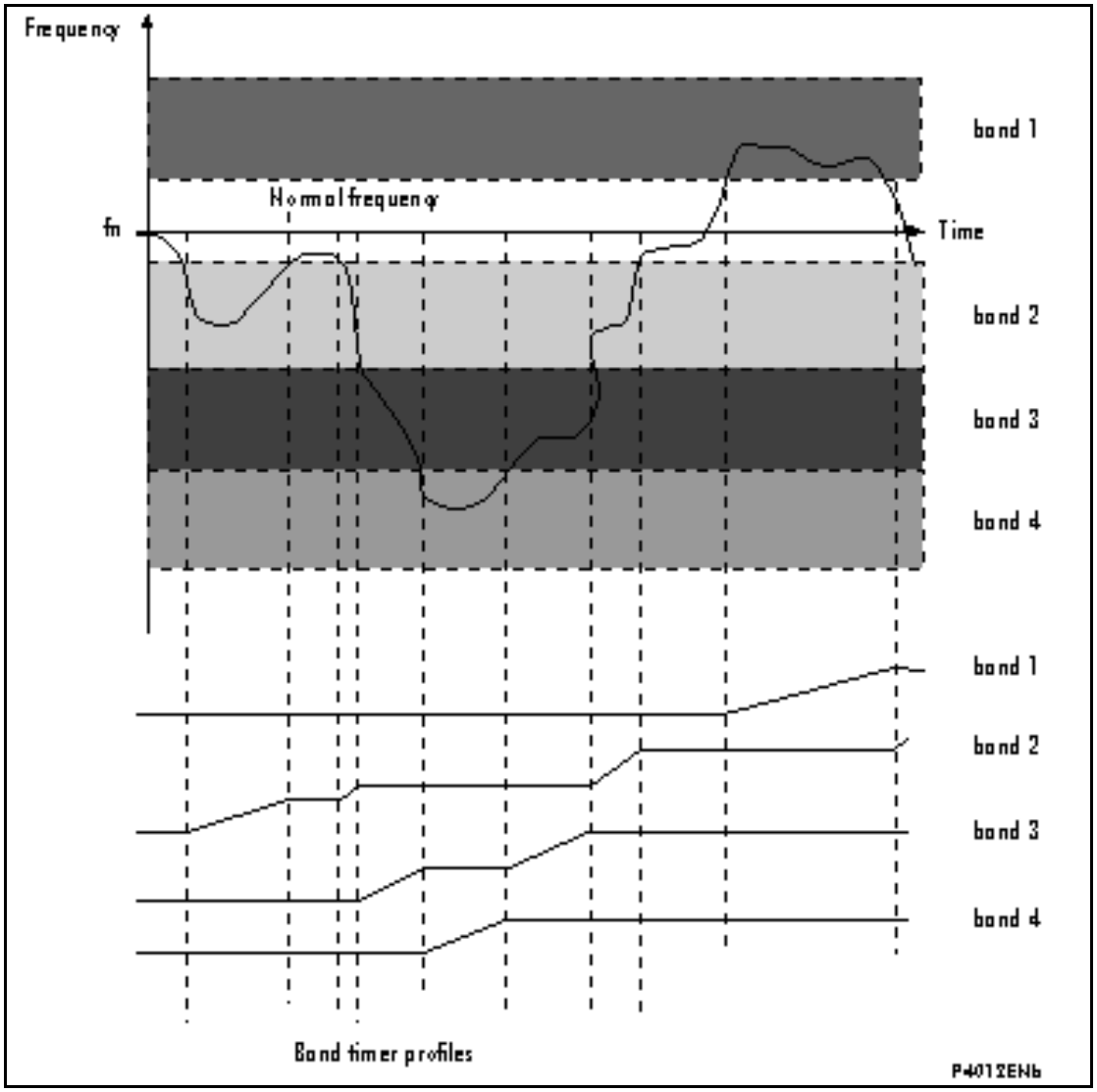


Figure 35: Generator abnormal frequency protection

Figure 35 shows the integrating timer behavior for abnormal frequency conditions over a long period of time. The timer for a particular band is incremented as long as the frequency is within the band lower and upper frequency settings. If two bands have overlapping frequency settings and the system frequency happens to be within both bands then the timers for both bands are incremented.

All frequency band stages can be inhibited by energizing a single DDB signal via the PSL (Turbine F Inh: DDB 632). DDB signals are also available to indicate the start and trip of each frequency band stage, (Starts: DDB 1178-1183, Trips: DDB 922-927).

Note: The start signals are instantaneous (i.e., without influence from the dead band delay timer) once the frequency is within the band.

The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The frequency band starts are mapped internally to the ANY START DDB signal – DDB 992.

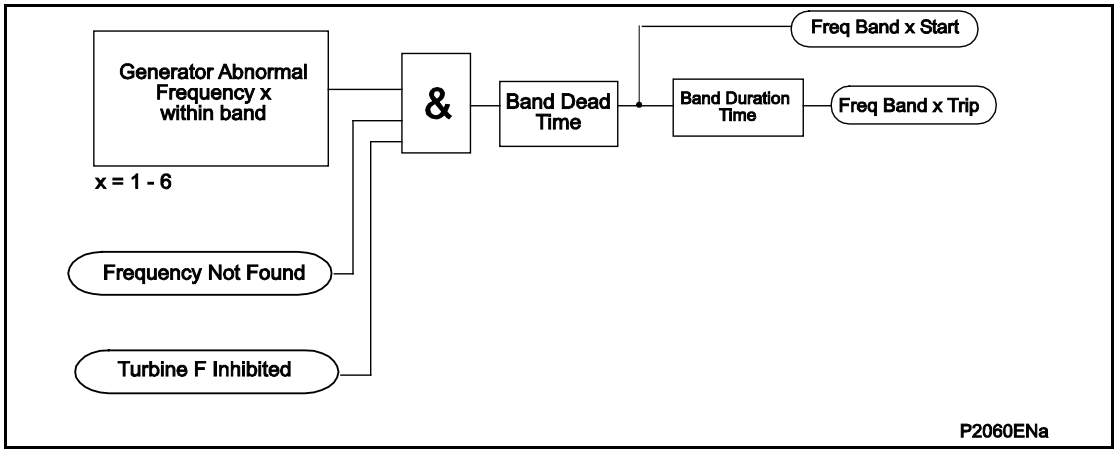


Figure 36: Generator turbine abnormal frequency logic diagram

1.14 Field failure protection function (40)

The field failure protection of the P34x consists of four elements, two time delayed impedance elements, a directional line and a power factor alarm element, shown in Figure 40.

The two impedance stages of field failure protection in the P34x relay are provided with a timer hold (drop off timer) facility, which may either be set to zero or to a definite time value. Setting of the timer to zero means that the field failure timer for that stage will reset instantaneously once the impedance falls outside 105% of the impedance characteristic. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period. For an intermittent fault when the reset time (drop-off time) of the field failure protection is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the relay will integrate the fault impedance pulses, for example during pole slipping, thereby reducing fault clearance times.

The timer hold (drop off timer) facility can be found for the two field failure impedance stages as settings **FFail 1 DO Timer** and **FFail 2 DO Timer** respectively.

The field failure protection also includes a directional line. The directional line is an impedance line with a reactance offset, Line Offset and Line Angle setting which operates as an independent element. The directional line can be used to block the field failure impedance elements in PSL using the DDB 1119, FFail Line Start, connected to DDB 653/4, FFail1 Inh and FFail2 Inh as shown below.

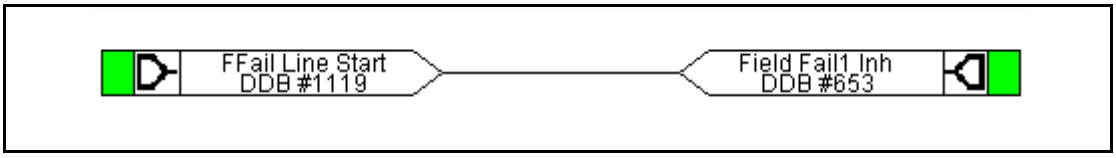


Figure 37: Inhibit logic

The directional line start signal (DDB 1119, FFail Line Start) will be ON in the blocking zone as shown in the figures below. The blocking zone is between (Line Angle, Line Angle + 180°) and operating zone is between (Line Angle, Line Angle - 180°), and the Line Angle can be set between -180° and +180°.

The directional line pick-up and drop-off characteristics are shown below. The solid line is the operating characteristic and the dotted line is the drop-off characteristic.

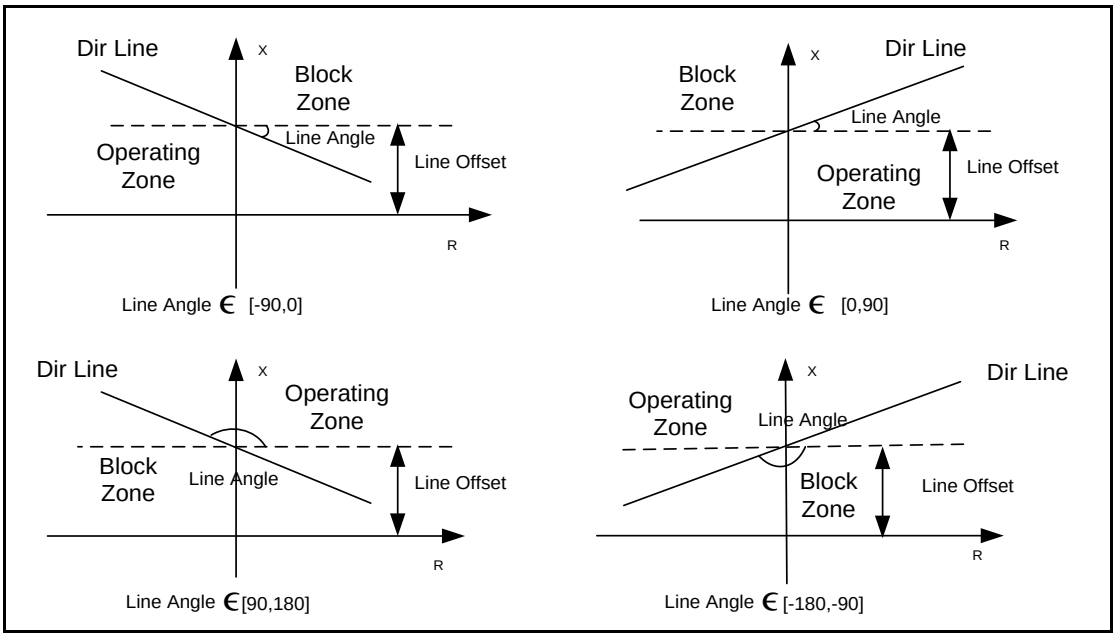


Figure 38: Pick-up characteristic of the directional line

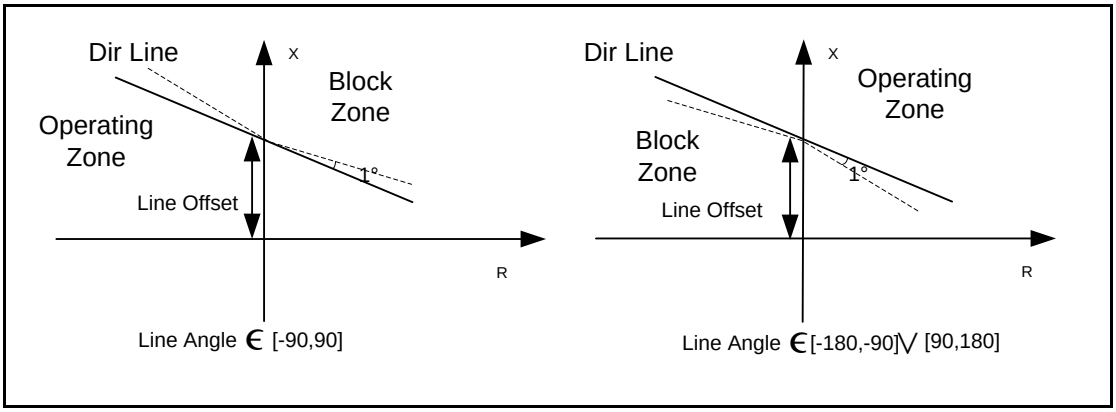


Figure 39: Drop-off characteristic of the directional line

The field failure impedance elements and directional line operate from A phase current and A phase voltage signals measured by the IA and VA inputs on the relay. The minimum phase current and voltage required for P342-6 field failure protection to work is 20 mA and 1 V (In = 1 A, Vn = 100/120 V) and 100 mA and 4 V (In = 5 A, Vn = 380/480 V).

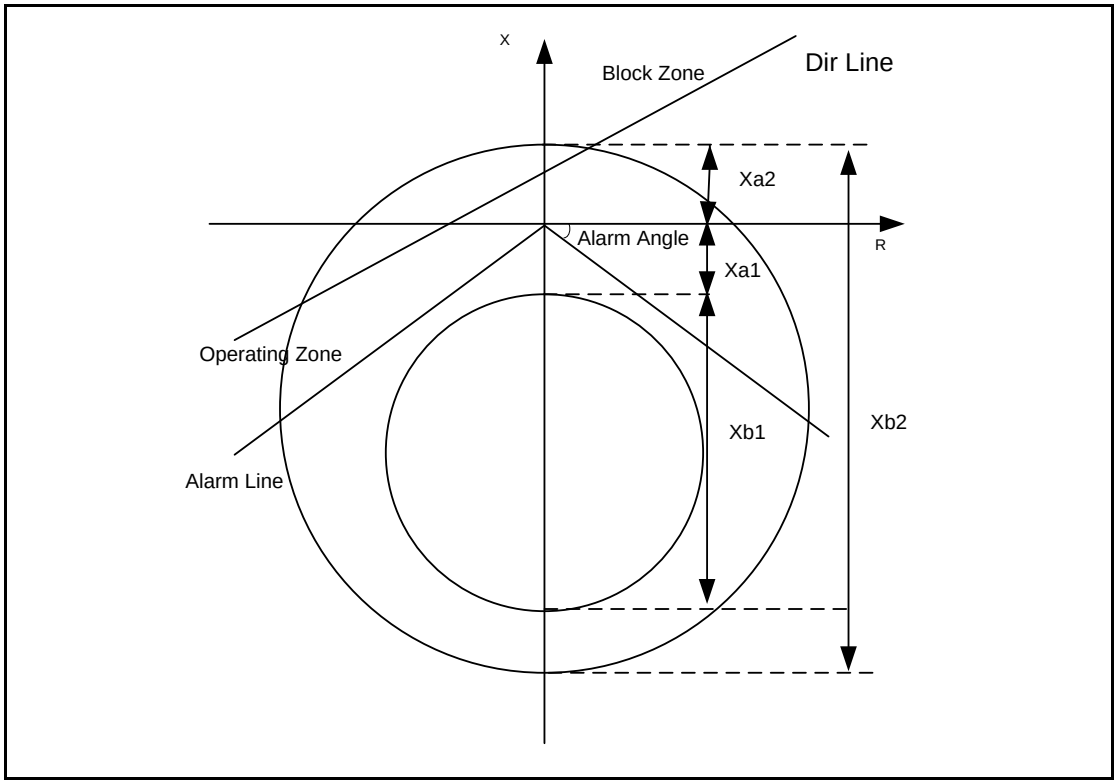


Figure 40: Field failure protection characteristics

The Field Fail1/2 and Field Fail Alarm elements can be independently inhibited by energizing the relevant DDB signal via the PSL (Field Fail1 Inh, Field Fail2 Inh, FFail Alarm Inh: DDB 653/654/655). DDB signals are also available to indicate the start and tripping of each stage (Starts: DDB 1120, DDB 1121, Trips: DDB 864, DDB 865). A DDB 'Field Fail Alarm' signal is generated from the field failure alarm stage (DDB 373). A DDB 'FFail Line Start' signal is generated from the directional line start (DDB1119).

The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The field failure protection starts are mapped internally to the ANY START DDB signal – DDB 992.

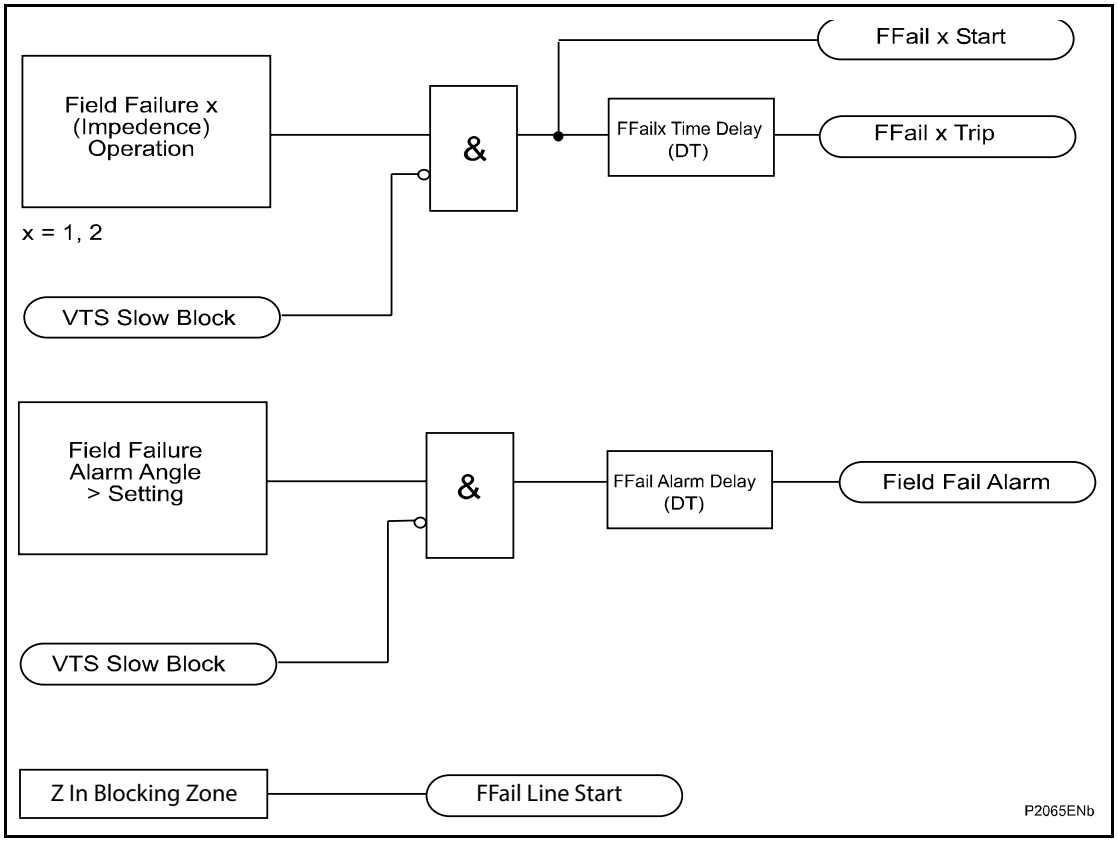


Figure 41: Field failure logic diagram

1.15 Negative phase sequence thermal protection (46T)

The Negative Phase Sequence (NPS) protection provided by the P34x is a true thermal replica with a definite-time alarm stage. The relay derives the negative phase sequence operating quantity from the following equation:

$$I_2 = \frac{I_a + a^2 I_b + aI_c}{3} \text{ where } a = 1.0 \angle 120°$$

Unbalanced loading results in the flow of positive and negative sequence current components.

Many traditional forms of generator NPS thermal protection relays have been designed with an extremely inverse (I_2^2t) operating time characteristic. Where the operating time of the characteristic is dependent solely on the instantaneous magnitude of negative phase sequence current present. This characteristic would be set to match the claimed generator thermal capacity. This is satisfactory when considering the effects of high values of negative phase sequence current.

For intermediate levels of NPS current, the rate of heating is slower. As a result, heat dissipation should be considered.

The basic expression of $t = K/I_{2cmr}$ does not cater for the effects of heat dissipation or for low standing levels of negative phase sequence current. The latter resulting in an increase in rotor temperature which remains within the machines design limits. An existing, tolerable, level of negative phase sequence current ($I_2<I_{2cmr}$), has the effect of reducing the time to reach the critical temperature level, if the negative phase sequence current level should increase beyond I_{2cmr}. The P34x NPS thermal replica is designed to overcome these problems by modeling the effects of low standing levels of negative phase sequence currents.

The temperature rise in critical rotor components is related to the negative phase sequence current (I_2 per unit) and to time (t seconds) as follows. This assumes no preceding negative phase sequence current:

$$\theta°C \propto I_2^2 (1 - e^{-t/\tau})$$

Where:

τ = The thermal time constant, $\tau = K_g/I2_{CMR}^2$

K_g is the generator's per-unit thermal capacity constant in seconds.

I_{2CMR} is the generator's per-unit continuous maximum I_2 rating.

The limiting continuous maximum temperature (θ_{CMR}) would be reached according to the following current-time relationship:

$$\theta°C = \theta_{CMR} \Rightarrow I_2^2 (1 - e^{-t/\tau}) = I_{2CMR}^2$$

OP

From the above, the time for which a level of negative phase sequence current in excess of I_{2CMR} can be maintained is expressed as follows:

$$t = - (K_g/ I_{2CMR}^2) \log_e (1- (I_{2CMR}/I_2))$$

The P34x negative phase sequence element offers a true thermal characteristic according to the following formula:

$$t = \frac{(\mathrm{I2} > 2\ k\ Setting)}{(\mathrm{I2} > 2\ Current\ set)^2}\ Log_e \left(\frac{\left(\frac{\mathrm{I2}}{\mathrm{I2}>2\ Current\ set} \right)^2 - \mathrm{I}p}{\left(\frac{\mathrm{I2}}{\mathrm{I2}>2\ Current\ set} \right)^2 - 1} \right)$$

$$\mathrm{I}p = \% \frac{Thermal\ state}{100}$$

Note: All current terms are in per-unit, based on the relay rated current, In.

So, for an applied current of I_2 = 5A = 1 In

I2>2 Current set = 0.25A = 0.05 In = 0.05 pu

I2>2 K Setting = 8.2 s

t = - I2>2 K Setting/ (I2>2 Current Set)^2 loge (1- (I2>2 Current Set/I_2)^2)

t = -8.2/0.05^2 loge (1 - (0.05/1)^2) = 8.21 s

for I2 = 4A = 0.8 In = 0.8 pu

t = -8.2/0.05^2 loge (1 - (0.05/0.8)^2) = 12.84 s

The reset time is:

$$treset = \frac{\left(I2 > 2\ k\ Setting\right)}{I2 > 2\ Current\ Set} 2\ Log_e \left(1 - \frac{\left(-0.05\right)}{\left(\left(I_2 / I_2 > 2\ Current\ Set\right)^2 - 1\right)} \right)$$

From the trip time of 8.21s the time to reset assuming I_2 =0 after tripping is:
treset = -8.2/0.05^2 loge (1 - (-0.05/-1) = 168.16 s

When the protected generator sees a reduction in negative phase sequence current, metallic rotor components will decrease in temperature. The relay is provided with a separate thermal capacity setting (**I2>2 KRESET**), used when there is a reduction in I_2.

The negative sequence protection element will respond to system phase to earth and phase to phase faults. Therefore, the element must be set to grade with downstream earth and phase fault protections. To aid grading with downstream devices a definite minimum operating time for the operating characteristic can be set.

For levels of negative phase sequence current that are only slightly in excess of the thermal element pick-up setting, there will be a noticeable deviation between the P34x negative phase sequence thermal protection current-time characteristic and that of the simple I_2^2t characteristic. For this reason, a maximum negative phase sequence protection trip time setting is provided. This maximum time setting also limits the tripping time of the negative phase sequence protection for levels of unbalance where there may be uncertainty about the machine's thermal withstand.

A time delayed negative sequence overcurrent alarm stage is provided to give the operator early warning of an unbalanced condition that may lead to generator tripping. This can allow corrective action to be taken to reduce the unbalance in the load.

The Negative Sequence element uses the current measured at the Ia, Ib, Ic inputs on the relay.

Thermal state of the machine can be viewed in the **NPS Thermal** cell in the **MEASUREMENTS 3** column. The thermal state can be reset by selecting **Yes** in the **Reset NPS Thermal** cell in **Measurements 3**. Alternatively the thermal state can be reset by energizing DDB 640 **Reset I2 Thermal** via the relay PSL.

A DDB signal is also available to indicate tripping of the element (DDB 944). A further DDB 'NPS Alarm' signal is generated from the NPS thermal alarm stage (DDB 370). The state of the DDB signal can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

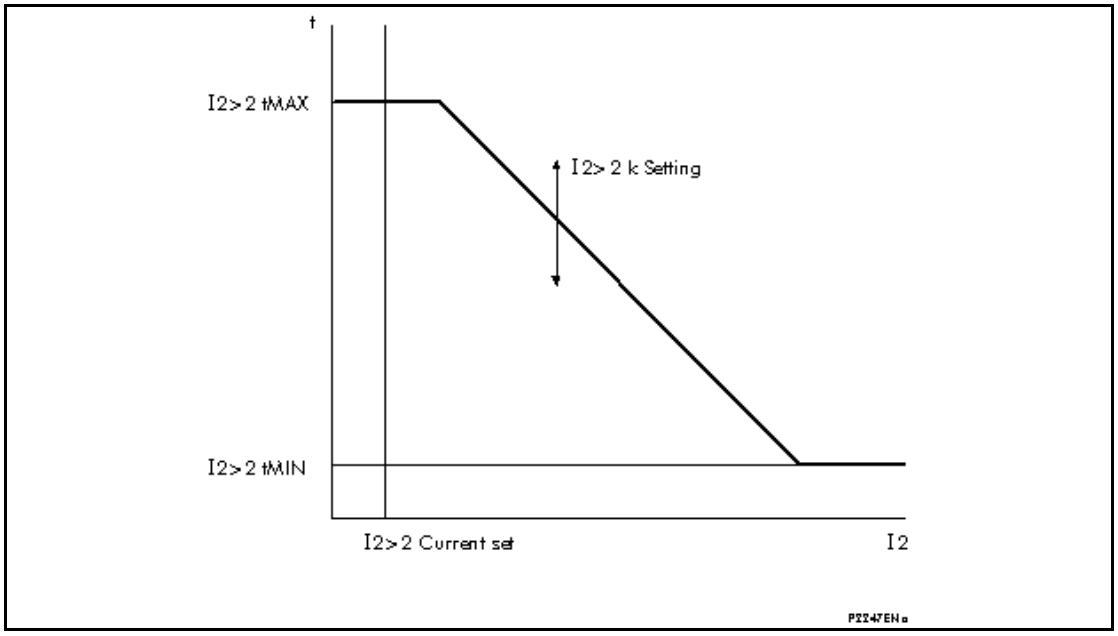


Figure 42: Negative phase sequence thermal characteristic

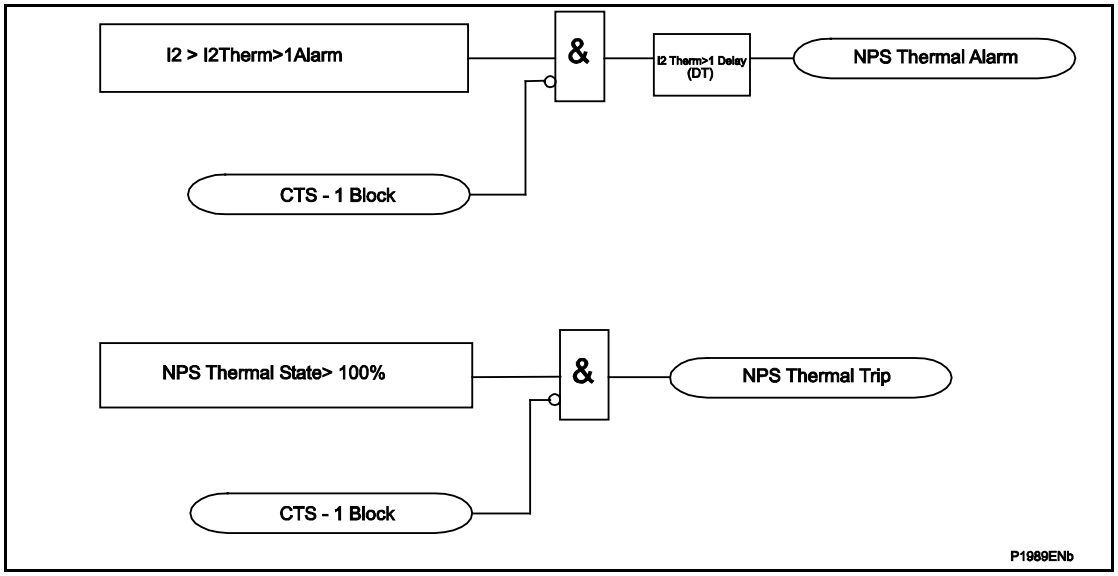


Figure 43: NPS thermal logic diagram

1.16 Power protection (32P/Q)

The standard power protection elements of the P34x relay calculate the three-phase active (P) and reactive (Q) power based on the following formula, using the current measured from the Ia, Ib, Ic inputs on the relay.

$P = Vala \cos(\phi a - \theta C) + Vb\ lb \cos(\phi b - \theta C) + Vc\ lc \cos(\phi c - \theta C)$

$Q = Vala \sin(\phi a - \theta C) + Vb\ lb \sin(\phi b - \theta C) + Vc\ lc \sin(\phi c - \theta C)$

Where $\phi a/b/c$ is the angle of IA/B/C with respect to VA/B/C and θC is the compensation angle setting. The compensation angle setting Comp Angle (θC) is provided to compensate for the angle error introduced by the system CT and VT.

The active/reactive power protection has a fixed 0.5° operating boundary. The boundary function stabilizes the protection operation for small CT/VT angle errors when the power angle approaches 90° for active power and 0° for reactive power. The operating characteristic for active and reactive power is shown.

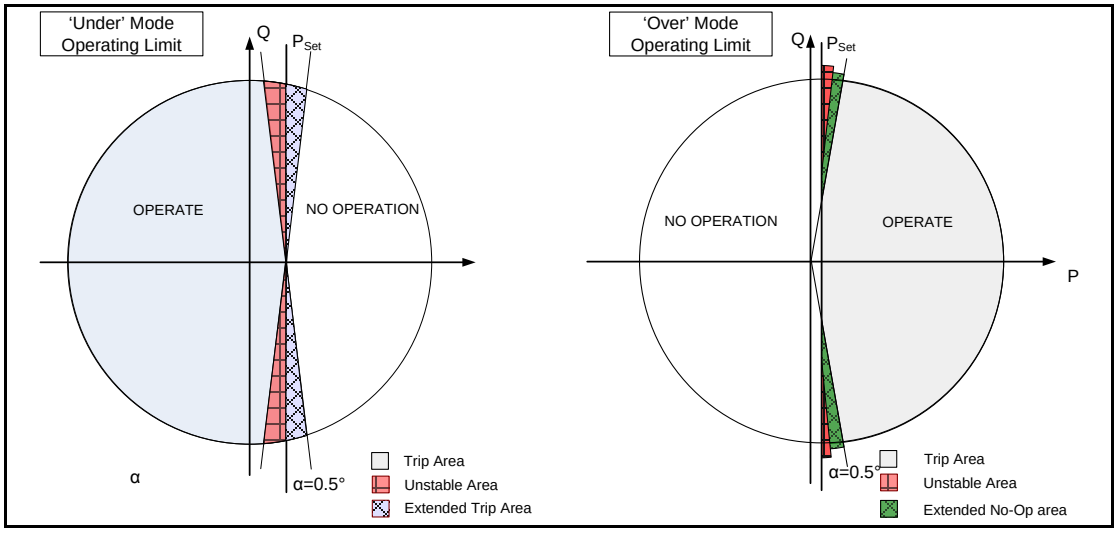


Figure 44: Operating boundary for active power

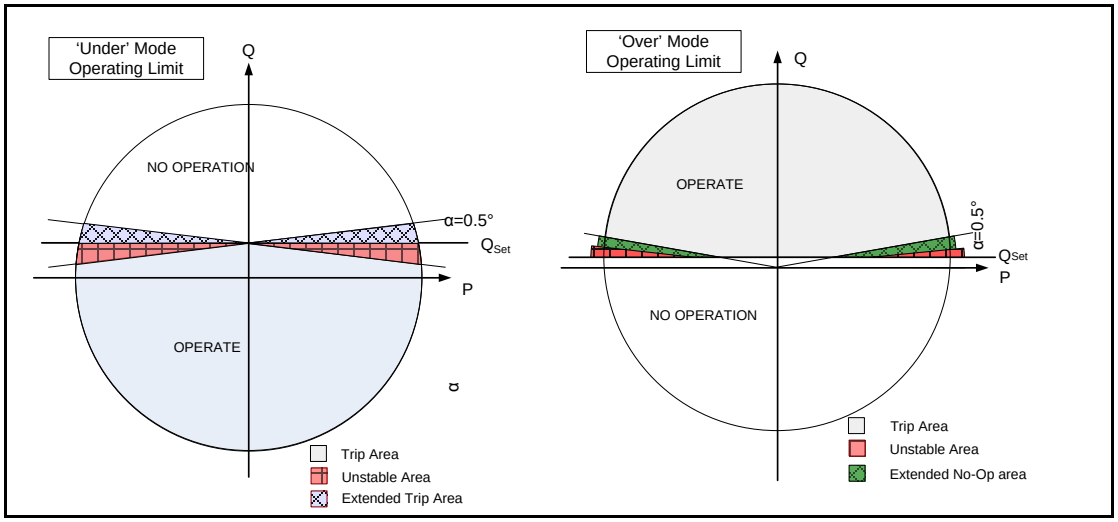


Figure 45: Operating boundary for reactive power

Four stages of power protection are provided, these can be independently selected as either under or over power, or disabled and the direction can be selected as forward or reverse. The operating mode can be selected as active or reactive. Operation in each mode and direction is described in the following sections. The power elements may be selectively disabled, via fixed pole dead logic, so that they can be inhibited when the protected machines CB is open, this will prevent mal-operation and nuisance flagging of any stage selected to operate as low forward power.

The P34x relay is connected with the convention that the forward current is the current flowing from the generator to the busbar. This corresponds to positive values of the active/reactive power flowing in the forward direction. When a generator is operating in the motoring mode, the machine is consuming active power from the power system. The motoring active power therefore flows in the reverse direction.

The **Power1/2/3/4 Dirn** setting for the power protection allows the user to set the power direction to either **Forward** or **Reverse.** The direction setting can be useful in applications involving pumped storage generators. The **Power1/2/3/4 Function** setting for the power protection allows the user to set the power operation as either **Under** or **Over**. Thus the direction and function settings can be used to select how the power protection operates e.g. as a reverse power function (Reverse/Over) or as a low forward power function (Forward/Under) or as an overpower function (Forward/Over). The **Power1/2/3/4 Mode** setting allows the user to select the power operating mode as **Active** or **Reactive** power.

The four stages of power protection in the P34x relay are provided with a timer hold (drop off timer) facility, which may either be set to zero or to a definite time value. Setting of the timer to zero means that the power timer for that stage will reset instantaneously once the current falls below 95% of the power setting. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period. For an intermittent fault when the reset time (drop-off time) of the power protection is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the relay will integrate the fault power pulses, thereby reducing fault clearance times. The timer hold (drop off timer) facility can be found for the four power stages as settings **Power 1/2/3/4 DO Timer**.

Measurement displays of active power, reactive power and power factor - **3Ph Watts**, **3Ph Vars and 3Ph Power Factor** are provided in the **MEASUREMENTS 2** menu to aid testing and commissioning. The disturbance recorder also provides channels to record the 3 phase active and reactive power - **3 Phase Watts**, and **3 Phase VArs** to aid testing and fault finding.

The power elements can be independently inhibited by energizing the relevant DDB signal via the PSL (Power1/2/3/4 Inhibit: DDB 667-670). DDB signals are also available to indicate starting and tripping of each stage (Starts: DDB 1140, DDB 1141, 1144, 1145 Trips: DDB 882, 883, 886, 887). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The power starts are mapped internally to the ANY START DDB signal - DDB 992.

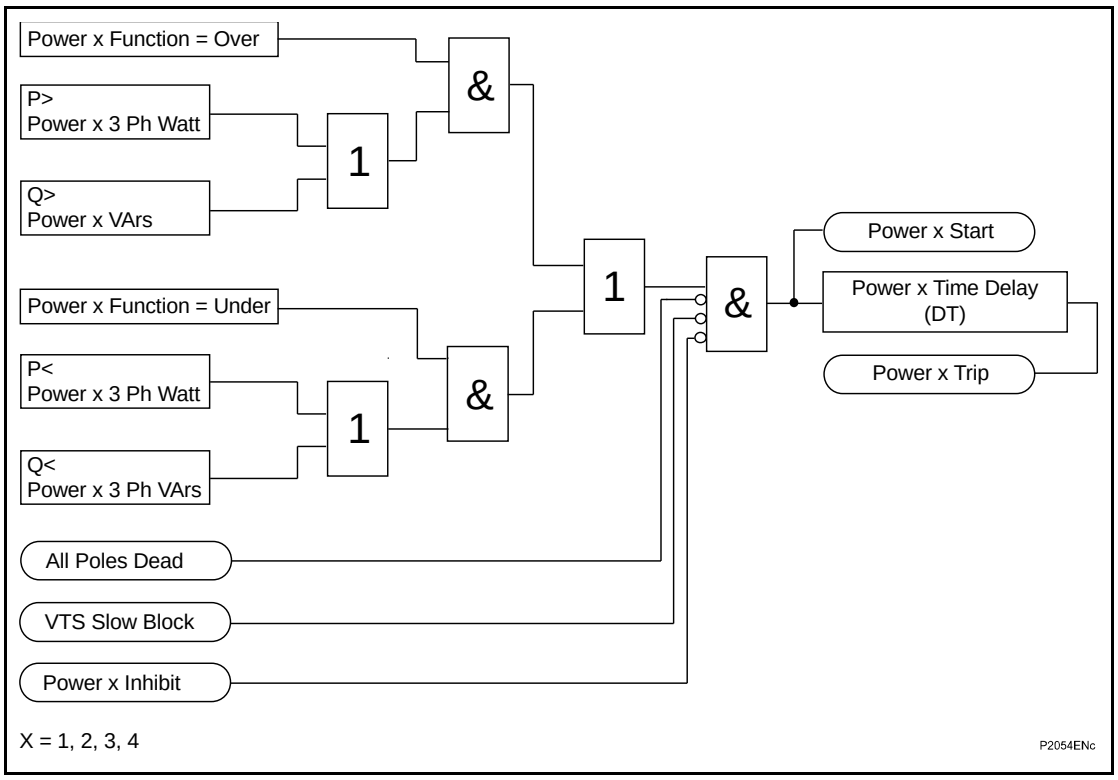


Figure 46: Power logic diagram

1.16.1 Sensitive power protection function

For steam turbine generators and some hydro generators a reverse power setting as low as 0.5%Pn is required. A sensitive setting for low forward power protection may also be required, especially for steam turbine generators that which have relatively low over speed design limits.

To improve the power protection accuracy, one or two sensitive current inputs can be used, connected to dedicated metering class CTs for sensitive power protection.

The CT inputs, IN1 Sensitive (P342-6) or IN1 Sensitive and IN2 Sensitive (P345) are the same as that of the sensitive earth fault and restricted earth fault protection elements, so the user can only select either sensitive power or SEF/REF in the **Configuration** menu, but not both. The **P> CT Source** setting, **Single/Wattmetric**, allows the user to select 1 sensitive current input for single phase power (P342-6) or 2 sensitive current inputs for wattmetric power (P345 only). The **P> Phase Select** setting allows the user to select the phase used, **A** or **B** or **C**.

Having separate CT inputs means that a correctly loaded metering class CT can be used which can provide the required angular accuracy for the sensitive power protection function. A compensation angle setting Comp Angle (θC) is also be provided to compensate for the angle error introduced by the system CT and VT. The active/reactive sensitive power protection has a fixed 0.5° operating boundary. The boundary function stabilizes the protection operation for small CT/VT angle errors when the power angle approaches 90° for active power and 0° for reactive power.

The single phase active (P) and reactive (Q) power is calculated based on the following formula:

$Px = Ix\ Vx \cos(\phi - \theta C)$

$Qx = Ix\ Vx \sin(\phi - \theta C)$

Where x = A or B or C

Where ϕ is the angle of Ix with respect to Vx and θC is the compensation angle setting.

The wattmetric active (P) and reactive (Q) power is calculated based on the following formula:

The 3-phase apparent power 'S', is calculated as:

$S = V_A I_A + V_B I_B + V_C I_C$

$S = V_A I_A + V_B I_B + V_C (-I_B - I_A)$ (Where $I_C = -I_B - I_A$)

$S = (V_A - V_C) I_A + (V_B - V_C) I_B$

$S = V_{AC} I_A + V_{BC} I_B$

The 3-phase active power, 'P', is calculated as:

$P = S \cos (\Phi - \theta C)$

$P = V_{AC} I_A \cos (\Phi - \theta C) + V_{BC} I_B \cos (\Phi - \theta C)$

The 3-phase reactive power, 'Q', is calculated as:

$Q = S \sin (\Phi - \theta C)$

$Q = V_{AC} I_A \sin (\Phi - \theta C) + V_{BC} I_B \sin (\Phi - \theta C)$

Where ϕ is the angle of I_A with respect to V_{AC} or the angle of I_B with respect to V_{BC} and θC is the compensation angle setting.

Four stages of sensitive power protection are provided, these can be independently selected as either under or over power, or disabled and the direction can be selected as forward or reverse. The operating mode can be selected as active or reactive. Operation in each mode and direction is described in the following sections. The sensitive power elements may be selectively disabled, via fixed pole dead logic, so that they can be inhibited when the protected machines CB is open, this will prevent mal-operation and nuisance flagging of any stage selected to operate as low forward power.

The P34x relay is connected with the convention that the forward current is the current flowing from the generator to the busbar. This corresponds to positive values of the active/reactive power flowing in the forward direction. When a generator is operating in the motoring mode, the machine is consuming active power from the power system. The motoring active power therefore flows in the reverse direction.

The **Sen Power1/2/3/4** Dirn setting for the sensitive power protection allows the user to set the power direction to either **Forward** or **Reverse.** The direction setting can be useful in applications involving pumped storage generators. The **Sen Power1/2/3/4 Func** setting for the sensitive power protection allows the user to set the power operation as either **Under** or **Over**. Thus the direction and function settings can be used to select how the power protection operates e.g. as a reverse power function (Reverse/Over) or as a low forward power function (Forward/Under) or as an overpower function (Forward/Over). The **Sen Power1/2/3/4 Mode** setting allows the user to select the sensitive power operating mode as **Active** or **Reactive** power.

The four stages of sensitive power protection in the P34x relay are provided with a timer hold (drop off timer) facility, which may either be set to zero or to a definite time value. Setting of the timer to zero means that the power timer for that stage will reset instantaneously once the current falls below 95% of the power setting. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period. For an intermittent fault when the reset time (drop-off time) of the power protection is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the relay will integrate the fault power pulses, thereby reducing fault clearance times. The timer hold (drop off timer) facility can be found for the four power stages as settings **Power 1/2/3/4 DO Timer**.

Measurement displays of sensitive active power, reactive power and power factor angle **Sen Watts, Sen Vars and Sen Power Angle** are provided in the **MEASUREMENTS 3** menu to aid testing and commissioning. The disturbance recorder also provides channels to record the single and wattmetric sensitive active and reactive power - **1Ph Sen Watts, 1Ph Sen VArs, 3Ph Sen Watts, 3Ph Sen VArs** to aid testing and fault finding.

The sensitive power elements can be independently inhibited by energizing the relevant DDB signal via the PSL (SPower1/2/3/4 Inhibit: DDB 660-663). DDB signals are also available to indicate starting and tripping of each stage (Starts: DDB 1142, DDB 1143, 1146, 1147 Trips: DDB 884, 885, 888, 889). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The sensitive power starts are mapped internally to the ANY START DDB signal – DDB 992.

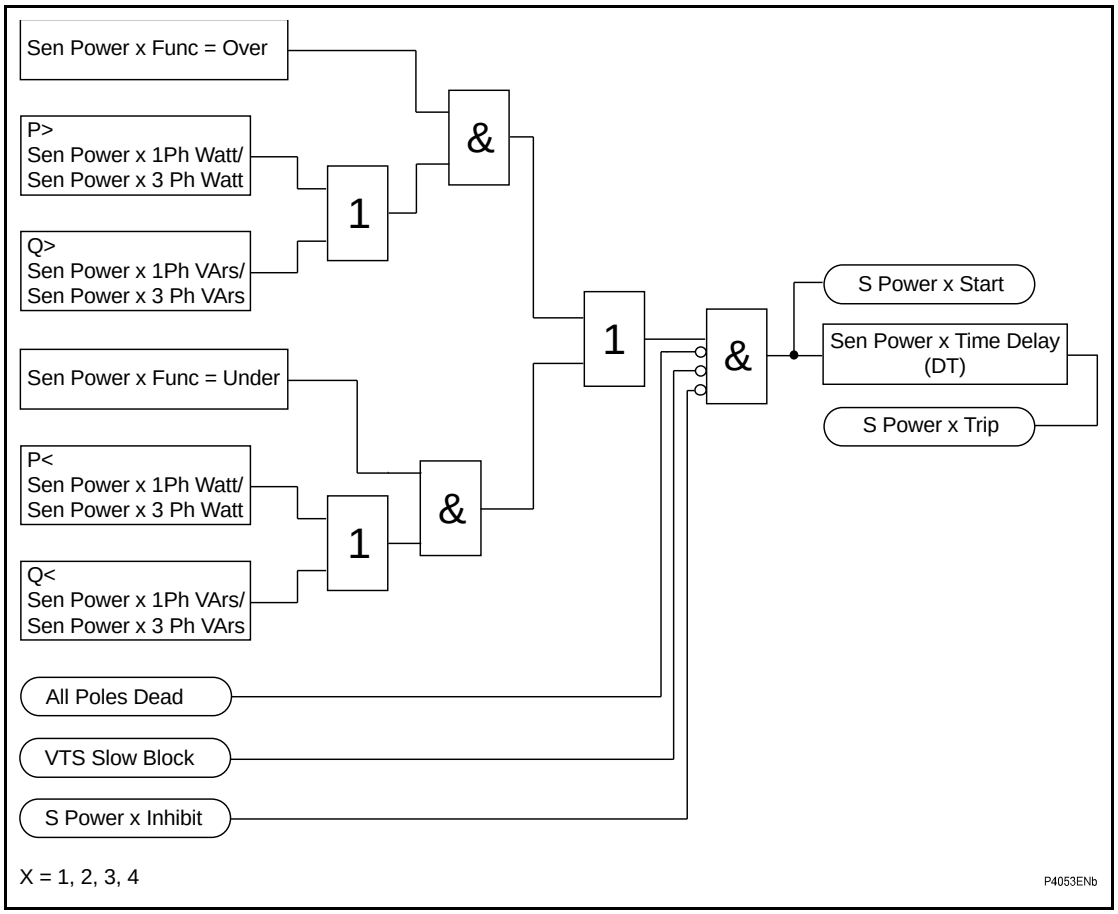


Figure 47: Sensitive power logic diagram

1.17 Stator earth fault protection function (50N/51N)

A two stage non-directional earth fault element is provided. The first stage has an inverse time curve or a user programmable curve or definite time delay characteristic and can incorporate a reset time delay to improve detection of intermittent faults. The second stage has a definite time characteristic that can be set to 0 s to provide instantaneous operation. For further details regarding the inverse time characteristics refer to the Overcurrent Protection, section 1.5

The logic diagram for non-directional stator earth fault overcurrent is shown in Figure 48.

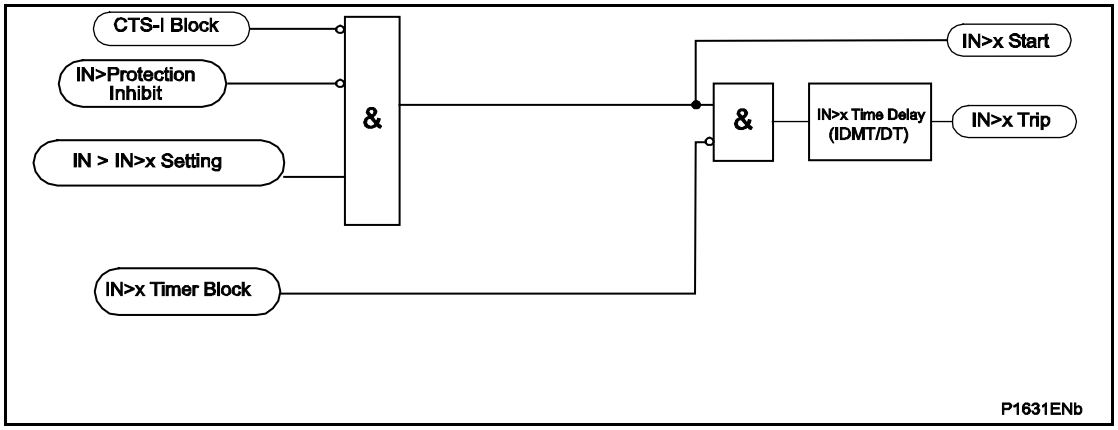


Figure 48: Non-directional EF logic (single stage)

A timer block input is available for each stage which will reset the earth fault timers of the relevant stage if energized, taking account of the reset time delay if selected for the **IN>1** stage (DDB 544, DDB 545). DDB signals are also available to indicate the start and trip of each stage of protection, (Starts: DDB 1008, DDB 1009, Trips: DDB 768, DDB 769). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The stator earth fault protection starts are mapped internally to the ANY START DDB signal – DDB 992.

The Stator Earth Fault element is powered from the In CT input on the relay.

1.17.1 IDG curve

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stages 1 and 2 of Earth Fault protection.

The IDG curve is represented by the following equation:

$$t = 5.8 - 1.35 \log_e \left(\frac{I}{IN > Setting} \right) \text{ in seconds}$$

Where:

I = Measured current

IN>Setting = An adjustable setting which defines the start point of the characteristic

Although the start point of the characteristic is defined by the **IN>** setting, the actual relay current threshold is a different setting called **IDG Is**. The **IDG Is** setting is set as a multiple of **IN>**.

An additional setting **IDG Time** is also used to set the minimum operating time at high levels of fault current.

Figure 49 shows how the IDG characteristic is implemented.

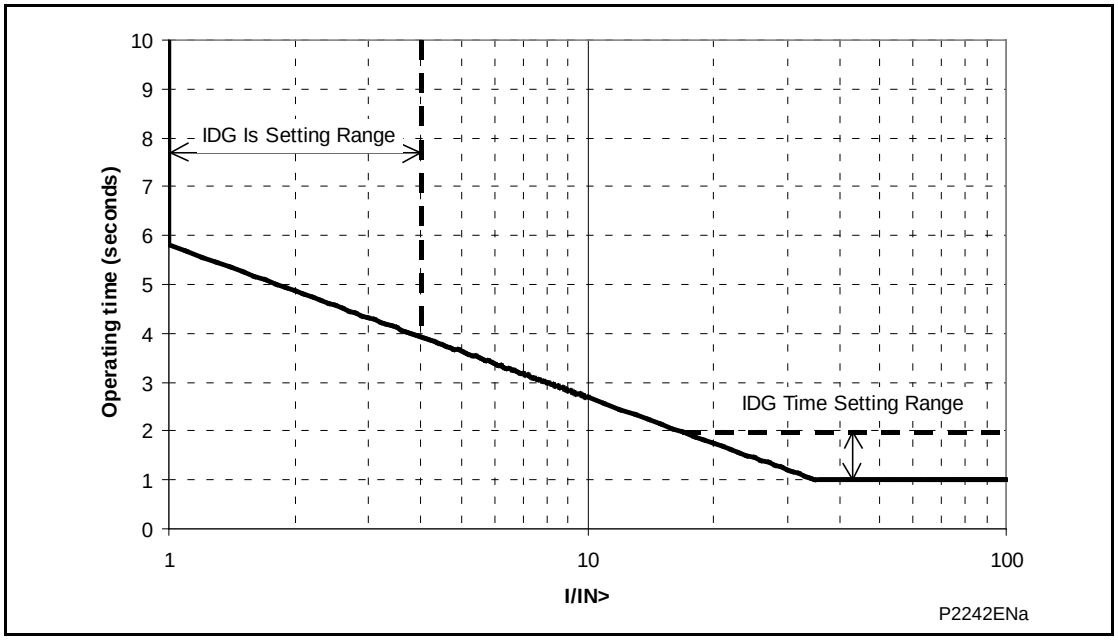


Figure 49: IDG characteristic

1.18 Residual overvoltage/neutral voltage displacement protection function (59N)

The neutral voltage displacement protection function of the P342/3/6 relays consist of two stages of derived (VN>1, VN>2) and two stages of measured (VN>3, VN>4) neutral overvoltage protection with adjustable time delays. All stages may be set to operate on either an IDMT or DT or a user curve characteristic.

The P344/5 has an additional two stages of measured (VN>5, VN>6) neutral overvoltage protection as it has a dedicated second neutral voltage input, VN(2).

The relay derives the neutral/residual voltage operating quantity from the following equation:

Vneutral = Va + Vb + Vc

A dedicated voltage input (one VN1 input is available in the P342/3/6 and two VN1/2 inputs are available in the P344/5) is provided for this protection function. This may be used to measure the residual voltage supplied from either an open delta connected VT or the voltage measured on the secondary side of a distribution transformer earth connection, as shown in Figure 50. Alternatively, the residual voltage may be derived internally from the three-phase to neutral voltage measurements. Where derived measurement is used the three-phase to neutral voltage must be supplied from either a 5-limb or three single-phase VTs. These types of VT design allow the passage of residual flux and consequently permit the relay to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. A three limb VT has no path for residual flux and is therefore unsuitable to supply the relay when residual voltage is required to be derived from the phase to neutral voltage measurement.

The residual voltage signal can be used to provide interturn protection as well as earth fault protection. The residual voltage signal also provides a polarizing voltage signal for the sensitive directional earth fault protection function.

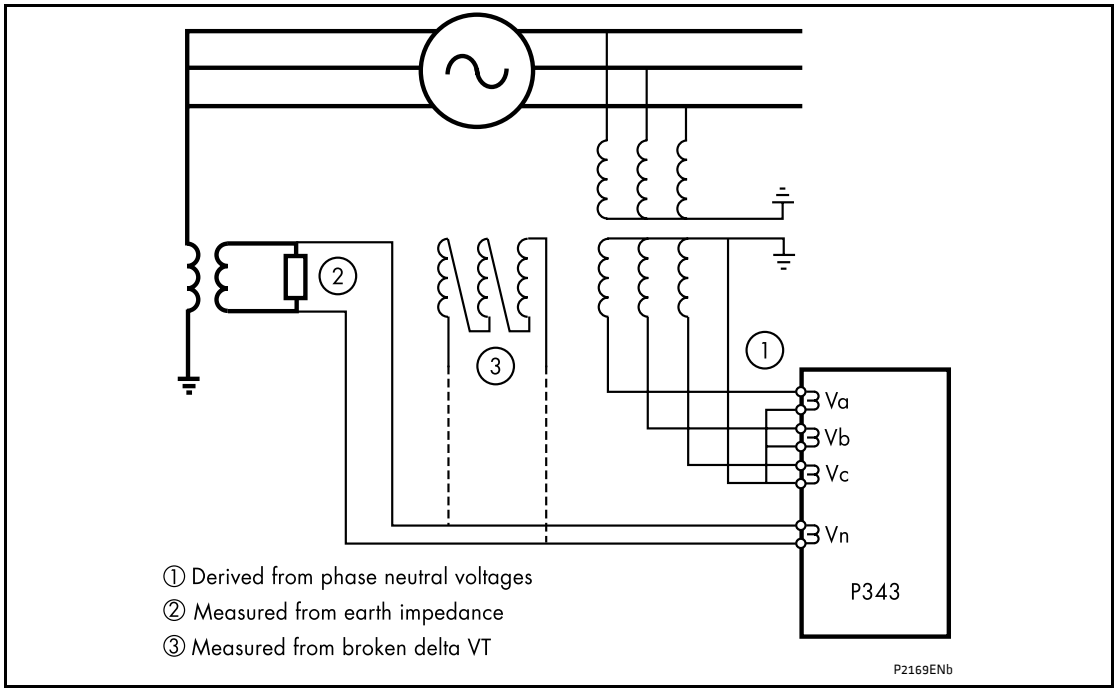


Figure 50: Alternative relay connections for residual overvoltage/NVD protection

The functional block diagram of the first stage residual overvoltage is shown in Figure 51.

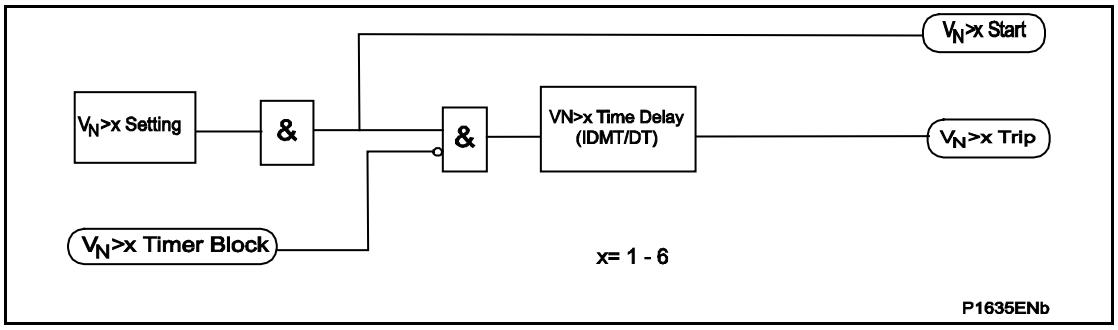


Figure 51: Residual overvoltage logic (single stage)

VTS blocking when asserted, effectively blocks the start outputs. Only the derived neutral voltage protection stages (VN>1, VN>2) are blocked by the VT Supervision.

A timer block input is available for each stage which will reset the residual overvoltage timers of the relevant stage if energized, (DDB 592-597). DDB signals are also available to indicate the start and trip of each stage of protection, (Starts: DDB 1088-1093 Trips: 832-837). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The residual overvoltage fault protection starts are mapped internally to the ANY START DDB signal – DDB 992.

The IDMT characteristic available on the first stage is defined by the following formula:

t = K / (M – 1)

Where:

K = Time Multiplier Setting (**VN>1 TMS**)

t = Operating Time in Seconds

M = Measured Residual Voltage/Relay Setting Voltage (**VN>1 Voltage Set**)

1.19 Sensitive earth fault protection function (50N/51N/67N/67W)

A single stage definite time sensitive earth fault protection element is provided in the P34x relay, this element can be set to operate with a directional characteristic when required. A separate sensitive earth fault element is provided within the P34x relay for the operating current, this has a dedicated CT input allowing very low current setting thresholds to be used. When directional earth fault protection is required the operating current should be derived from either a core balanced CT or the residual connection of three-phase CTs at the terminals of the machine. Direction of the earth fault current for this element is determined with reference to the polarizing signal, the residual voltage. The polarizing signal is taken from the residual overvoltage/NVD protection input (VN1 input for P342/3/4/5/6) or derived from the three-phase neutral voltage inputs on the relay.

A polarizing voltage threshold is also provided. The element cannot operate unless voltage exceeds this threshold. This helps to restrain the element during phase/phase faults when transient CT saturation produces spill current in the residual connection of the phase CTs. No residual voltage will be present during such non-earth fault conditions hence the DEF element cannot operate. The element will therefore be enabled only during genuine earth fault conditions when significant residual voltage will be present. To prevent the element from mal-operating due to VT fuse failure the element can be blocked from the VT supervision logic by setting the ISEF Func. Link - Block ISEF from VTS to 1. If the ISEF Func. Link is set to 0 the SEF element will revert to non-directional upon operation of the VTS.

Where Petersen Coil earthing is used, users may wish to use Wattmetric Directional Earth Fault protection or an $I\cos\phi$ characteristic. Settings to enable the element to operate as a wattmetric element are also provided. For insulated earth applications, it is common to use the $I\sin\phi$ characteristic.

The Sensitive Earth Fault protection can be blocked by energizing the relevant DDB signal via the PSL (DDB 548). This allows the protection to be integrated into busbar protection schemes as shown in section 1.32, or can be used to improve grading with downstream devices. DDB signals are also available to indicate the start and trip of the protection, (Start: DDB 1012, Trips: DDB 773). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Note: ISEF> Func Link – bit 0 When this bit is set to 1, operation of the Voltage Transformer Supervision (VTS), will block the stage if directionalized. When set to 0, the stage will revert to non-directional upon operation of the VTS.

The logic diagram for sensitive directional earth fault overcurrent with neutral voltage polarization is shown in Figure 52.

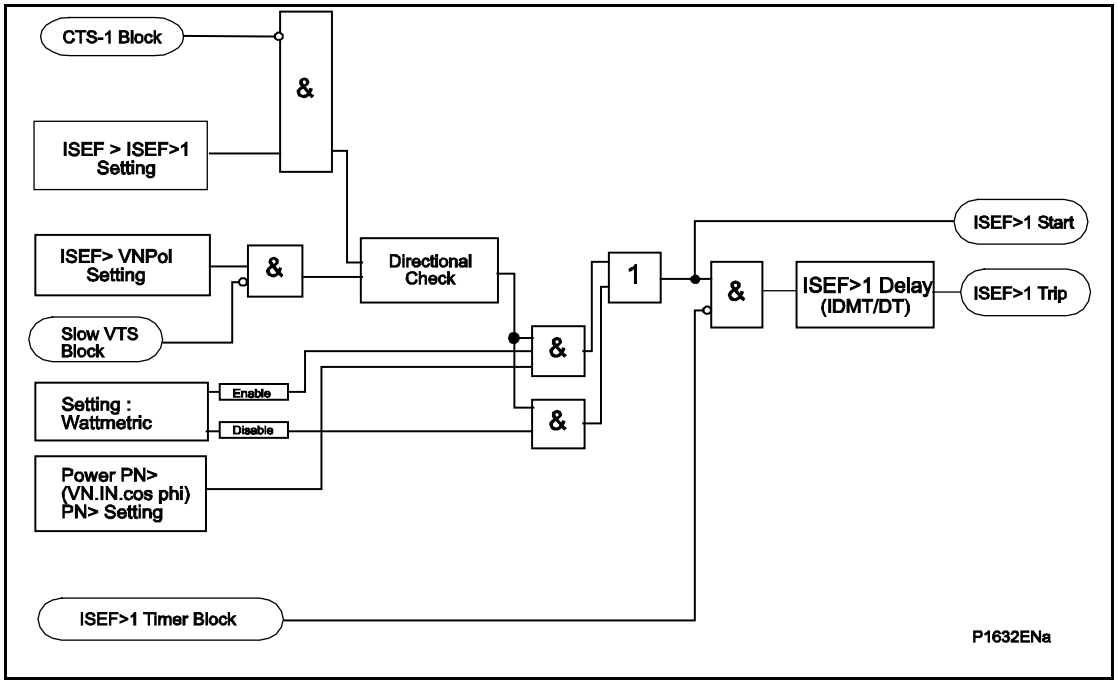


Figure 52: Directional SEF with VN polarization

The directional check criteria are given below for the standard directional sensitive earth fault element:

Directional forward

-90° < (angle(IN) - angle(VN + 180°) - RCA) < 90°

Directional reverse

-90° > (angle(IN) - angle(VN + 180°) - RCA) > 90°

1.20 Restricted earth fault protection (64)

The REF protection in the P34x relays may be configured to operate as either a high impedance differential or a low impedance biased differential element. The following sections describe the application of the relay in each mode.

Note: The high impedance REF element of the relay shares the same CT input as the SEF protection. Hence, only one of these elements may be selected.

A DDB signal is available to indicate the tripping of the REF protection, (DDB 772). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

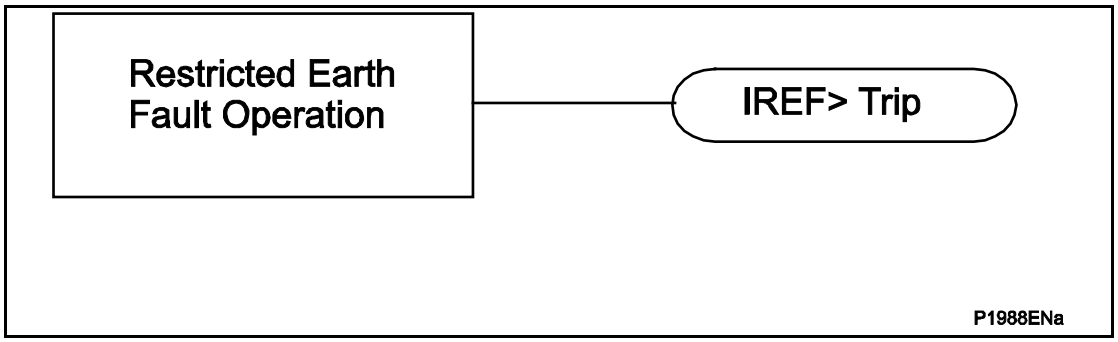


Figure 53: Restricted earth fault logic diagram

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1.20.1 Low impedance biased differential REF protection

In a biased differential relay, the through current is measured and used to increase the setting of the differential element. For heavy through faults, one CT in the scheme can be expected to become more saturated than the other and hence differential current can be produced. However, biasing will increase the relay setting such that the resulting differential current is insufficient to cause operation of the relay.

Figure 54 and Figure 55 show the appropriate relay connections and operating characteristic for the P34x relay applied for biased REF protection, respectively:

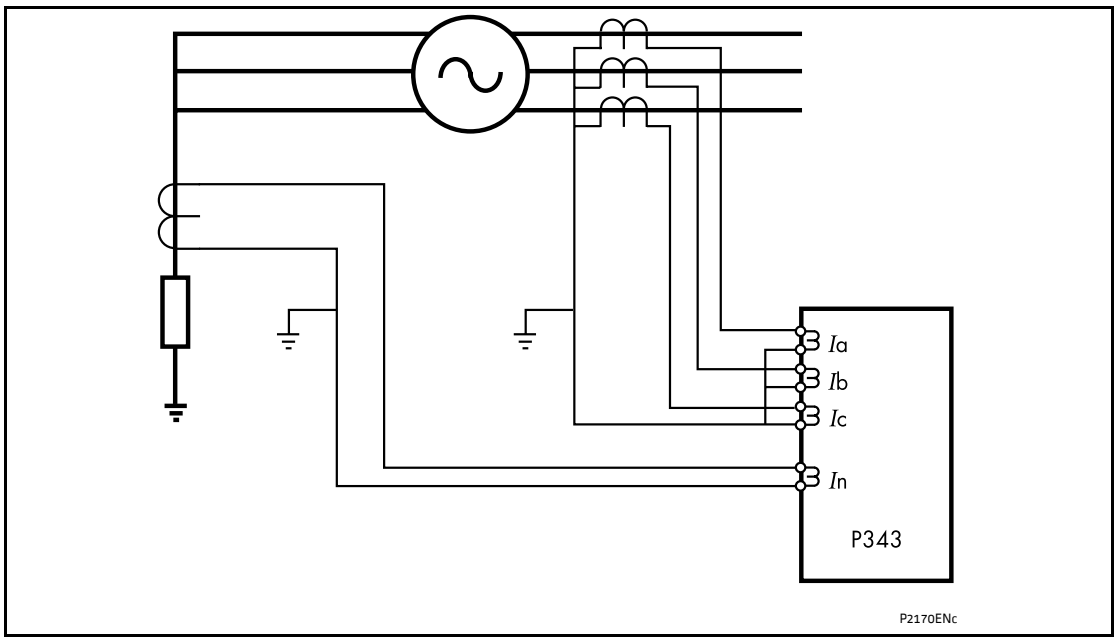


Figure 54: Relay connections for biased REF protection

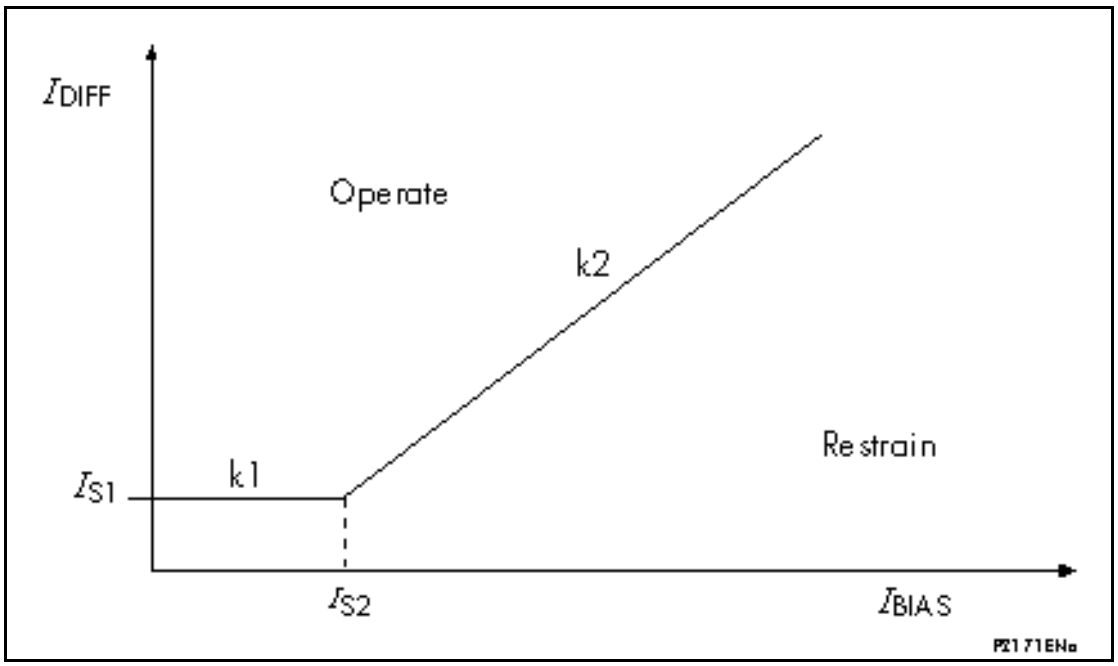


Figure 55: Biased REF protection operating characteristic

Figure 56 shows the three line CTs are connected to the three-phase CTs in the normal manner. The 3 phase current source for the line CTs can be selected using the **IREF> CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting. The neutral CT is then connected to the stator earth fault CT input. These currents are then used internally to derive both a bias and a differential current quantity for use by the low impedance biased differential REF protection.

The advantage of this method of connection is that the line and neutral CTs are not differentially connected and so the neutral CT can also be used to drive the stator earth fault protection. Also, no external equipment such as stabilizing resistors or Metrosils are required, unlike the case with high impedance protection.

The formula used by the relay to calculate the required bias quantity is therefore as follows:

$$Ibias = \{(\text{Highest of } Ia, Ib \text{ or } Ic) + (Ineutral \times \text{Scaling Factor})\} / 2$$

The reason for the scaling factor included on the neutral current is explained by referring to Figure 56.

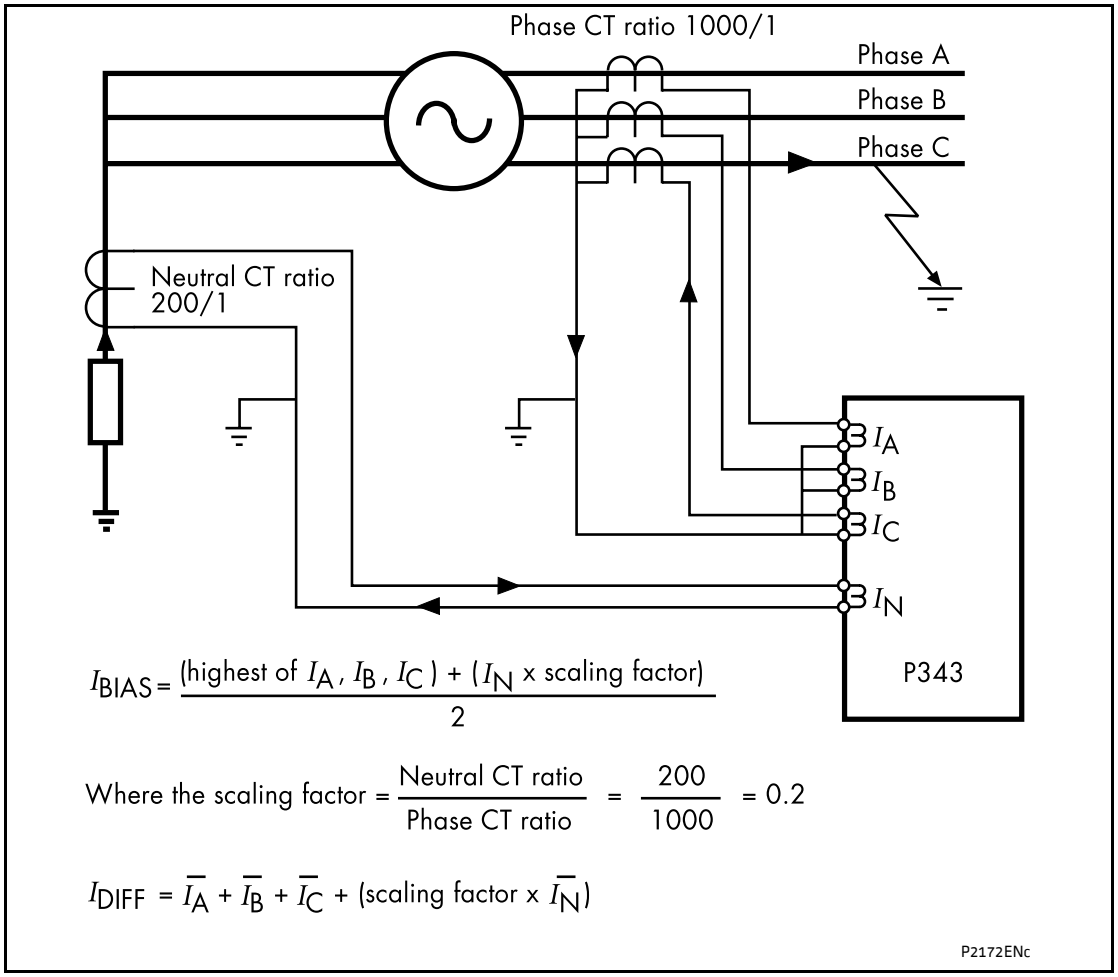


Figure 56: Neutral scaling for biased REF protection

Where it is required that the neutral CT also drives the stator earth fault protection element, it may be a requirement that the neutral CT has a lower ratio than the line CTs in order to provide better earth fault sensitivity. The relay automatically scales the level of neutral current used in the bias calculation by a factor equal to the ratio of the neutral to line CT primary ratings to compensate for any mismatch.

1.20.2 High impedance restricted earth fault protection

The high impedance principle is best explained by considering a differential scheme where one CT is saturated for an external fault, as shown in Figure 57.

If the relay circuit is considered to be a very high impedance, the secondary current produced by the healthy CT will flow through the saturated CT. If CT magnetizing impedance of the saturated CT is considered to be negligible, the maximum voltage across the relay circuit will be equal to the secondary fault current multiplied by the connected impedance, ($R_{L3} + R_{L4} + R_{CT2}$).

The relay can be made stable for this maximum applied voltage by increasing the overall impedance of the relay circuit, such that the resulting current through the relay is less than its current setting. As the impedance of the relay input alone is relatively low, a series connected external resistor is required. The value of this resistor, RST, is calculated by the formula shown in Figure 58.

An additional non-linear resistor, Metrosil, may be required to limit the peak secondary circuit voltage during internal fault conditions.

To ensure the protection will operate quickly during an internal fault the CT's used to operate the protection must have a kneepoint voltage of at least 4 Vs.

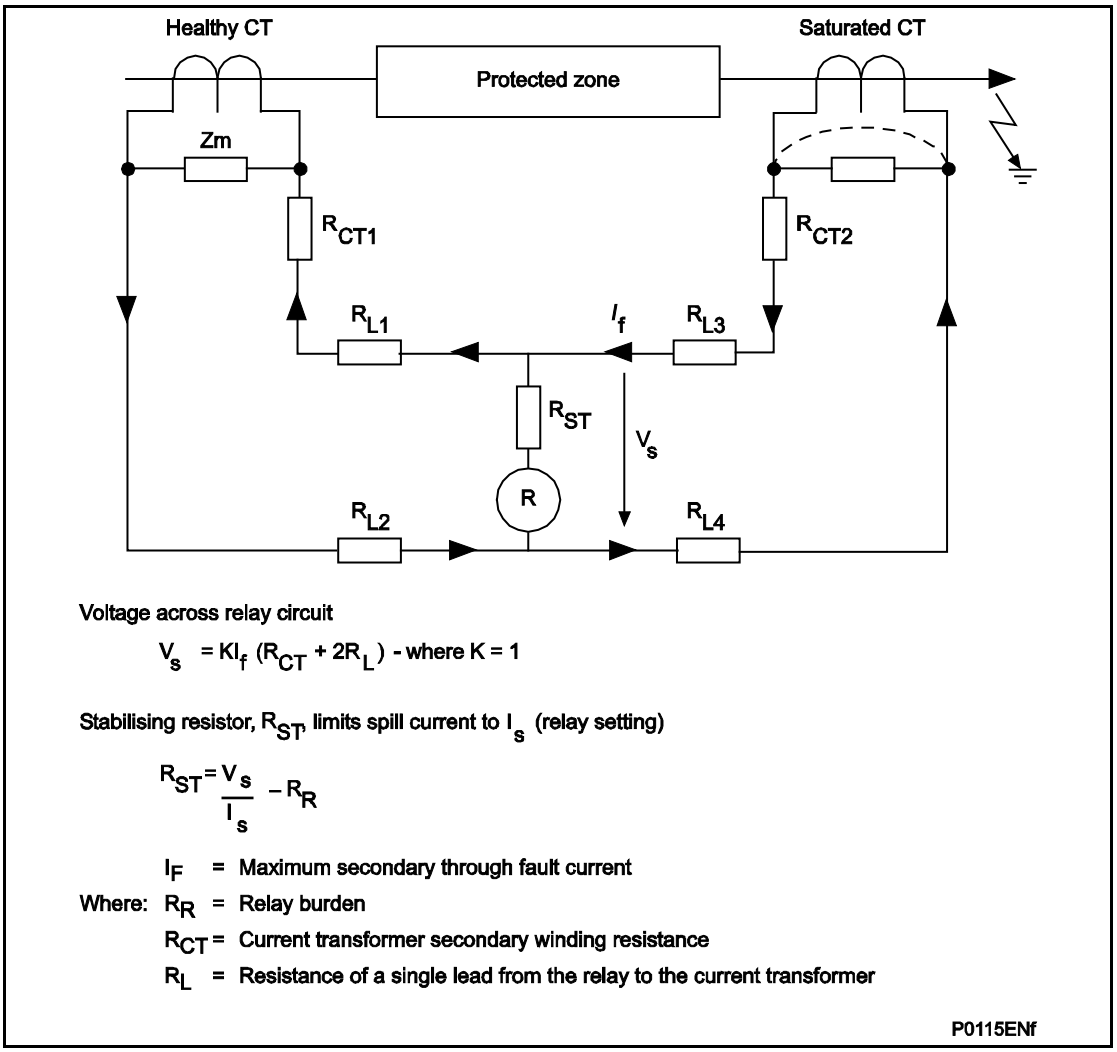


Figure 57: Principle of high impedance differential protection

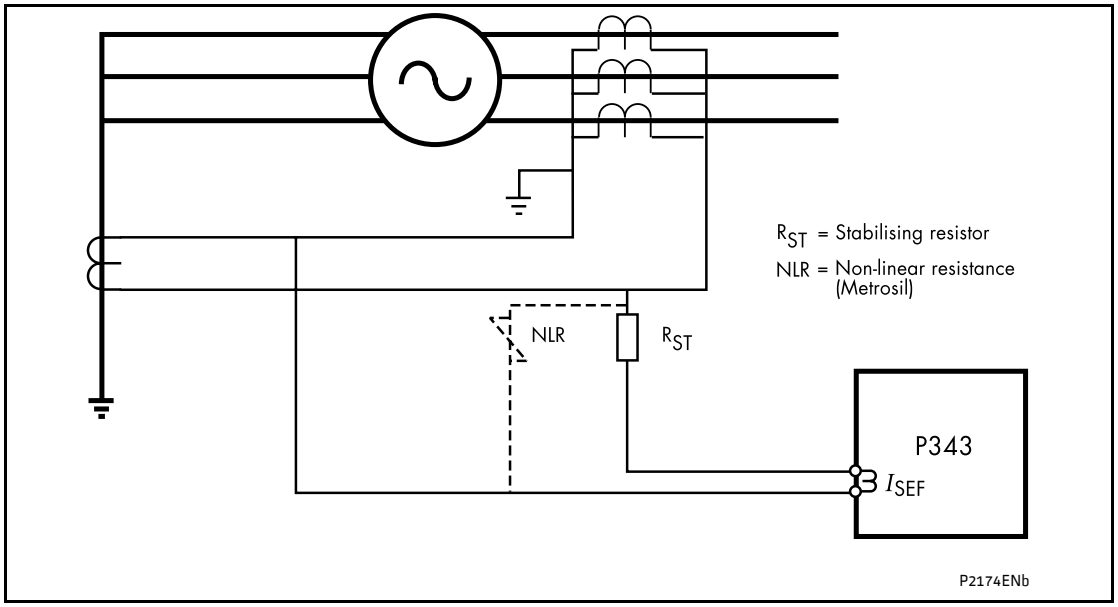


Figure 58: Relay connections for high impedance REF protection

The necessary relay connections for high impedance REF are shown in Figure 58.

The high impedance protection uses an external differential connection between the line CTs and neutral CT. The SEF input is then connected to the differential circuit with a stabilizing resistor in series.

1.21 100% stator earth fault protection (3rd harmonic method) (27TN/59TN)

To detect faults in the last 5% of the generator winding, the P343/4/5/6 relay is provided with a third harmonic undervoltage and overvoltage element. These, together with the residual overvoltage or stator earth fault protection elements, will provide protection for faults over the complete winding.

The third harmonic neutral under voltage element is applicable when the neutral voltage measurement is available at the neutral end of the generator. It is supervised by a three-phase under voltage element, which inhibits the protection when all the phase-phase voltages at the generator terminal are below the threshold, to prevent operation when the machine is dead, interlocking may also be required to prevent false operation during certain conditions. For example, some machines do not produce substantial third harmonic voltage until they are loaded. In this case, the power supervision elements (active, reactive and apparent power) could be used to detect load to prevent false tripping under no load conditions. These power thresholds can be individually enabled and disabled and the setting range is from 2 - 100%Pn.

For applications where the neutral voltage measurement can only be obtained at the generator terminals, from a broken delta VT for example, the under voltage technique cannot be applied. Therefore the third harmonic neutral over voltage element can be used for this application. The blocking features of the under voltage and power elements are not required for the 3rd harmonic neutral over voltage element.

Note: The relay can only select 3rd harmonic neutral under voltage or 3rd harmonic neutral over voltage, but not both.

The logic diagrams of the two protection schemes are shown in Figure 59.

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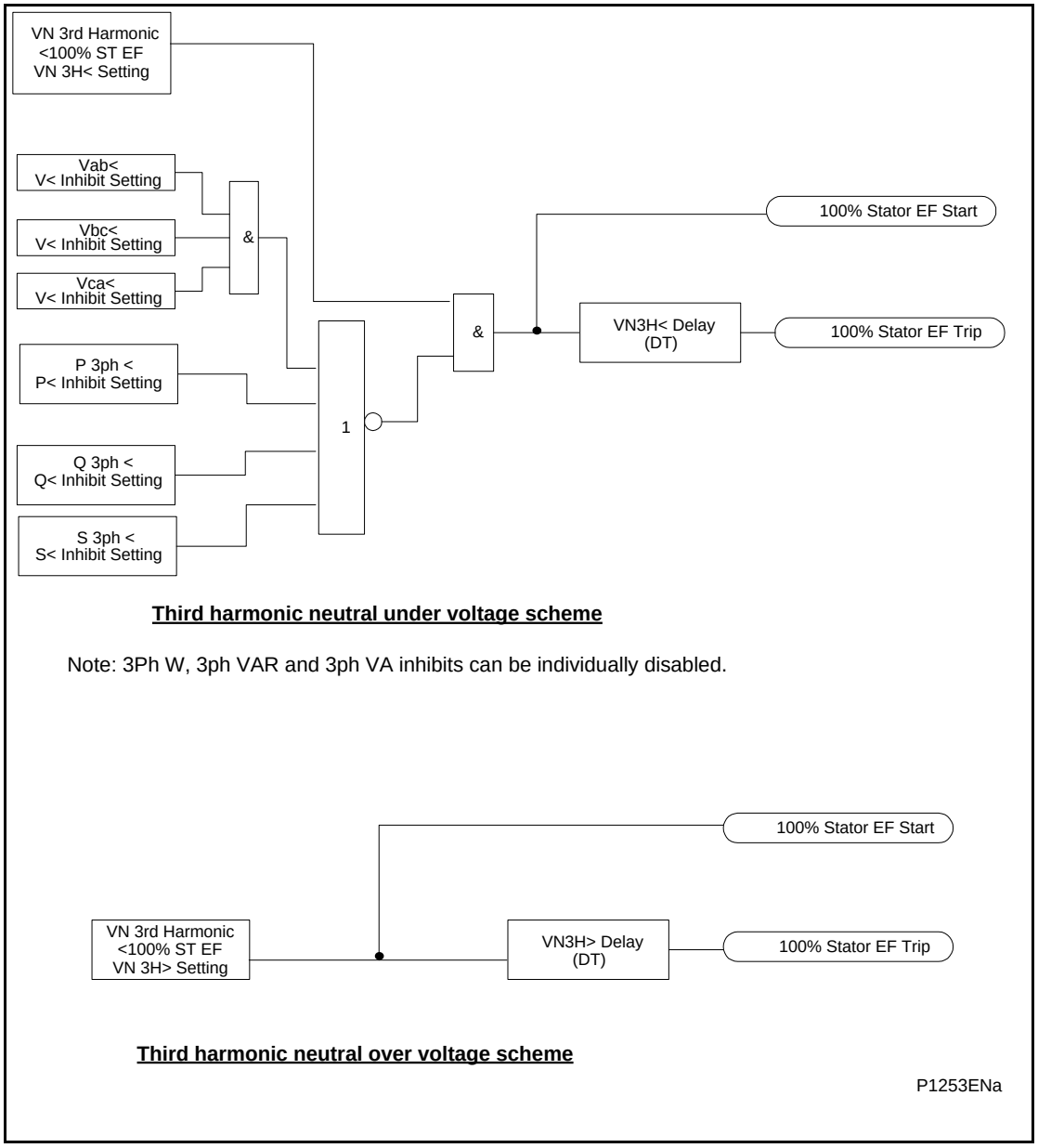


Figure 59: 100% stator earth fault protection block diagram

DDB signals are available to indicate the start and trip of the protection, (Start: DDB 1016, Trip: DDB 777). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The 100% stator earth fault protection start is mapped internally to the ANY START DDB signal – DDB 992.

1.22 100% stator earth fault protection (low frequency injection method) (64S)

The 100% stator earth fault protection using a low frequency injection technique detects earth faults in the entire winding, including the generator neutral point.

100% stator earth fault protection can be provided by injecting an external low frequency alternating voltage into the starpoint or the terminals of the machine. Under normal healthy conditions only a very small current flows via the stator earth capacitance due to the high impedance of this path at low frequencies ($Xc = 1/2\pi fc$). In the event of an earth fault the measured current increases due to the smaller impedance of the earth fault path. From the injected voltage and the fault current the relay can determine the fault resistance. The protection can also detect earth faults at the generator terminals including connected components such as voltage transformers.

A loading device with a low frequency generator is required for implementation. The output of the low frequency signal generator (approx 25 V) is connected via a bandpass filter in parallel with a loading resistor to a neutral transformer at the generator starpoint or an earthing (broken delta) transformer at the terminals of the generator. The bandpass filter provides rounding of the square-wave voltage and energy storage. The higher series resistance of the bandpass filter (approx. 8 Ω at 20 Hz) protects the 20 Hz generator from excessive feedback current if the load resistor carries the full displacement voltage during a terminal phase-earth fault.

The loading resistor is connected in parallel with the low frequency generator to generate a defined neutral current in normal healthy conditions. The voltage to be injected into the generator starpoint depends on the driving 20 Hz voltage (voltage divider: load resistor and bandpass), and on the transformation ratio of the neutral or earthing transformer. To prevent the secondary load resistance from becoming too small (it should be > 0.5 Ω□□where possible) a high secondary voltage, such as 500 V, should be chosen for the neutral or earthing transformer. It is important that the earthing transformer never becomes saturated otherwise ferroresonance may occur. It is sufficient that the transformer knee point voltage be equal to the generator rated line voltage. The low frequency voltage is fed to the relay via a voltage divider and the low frequency measuring current is fed via a miniature current transformer. All interference deviating from the nominal low frequency signal is filtered out.

The 100% stator earth fault protection can also be applied with a primary loading resistor. The 20 Hz voltage is connected via a voltage transformer and the neutral starpoint current is directly measured via a CT, see section 2.21.2.3 (*P34x/EN/AP*).

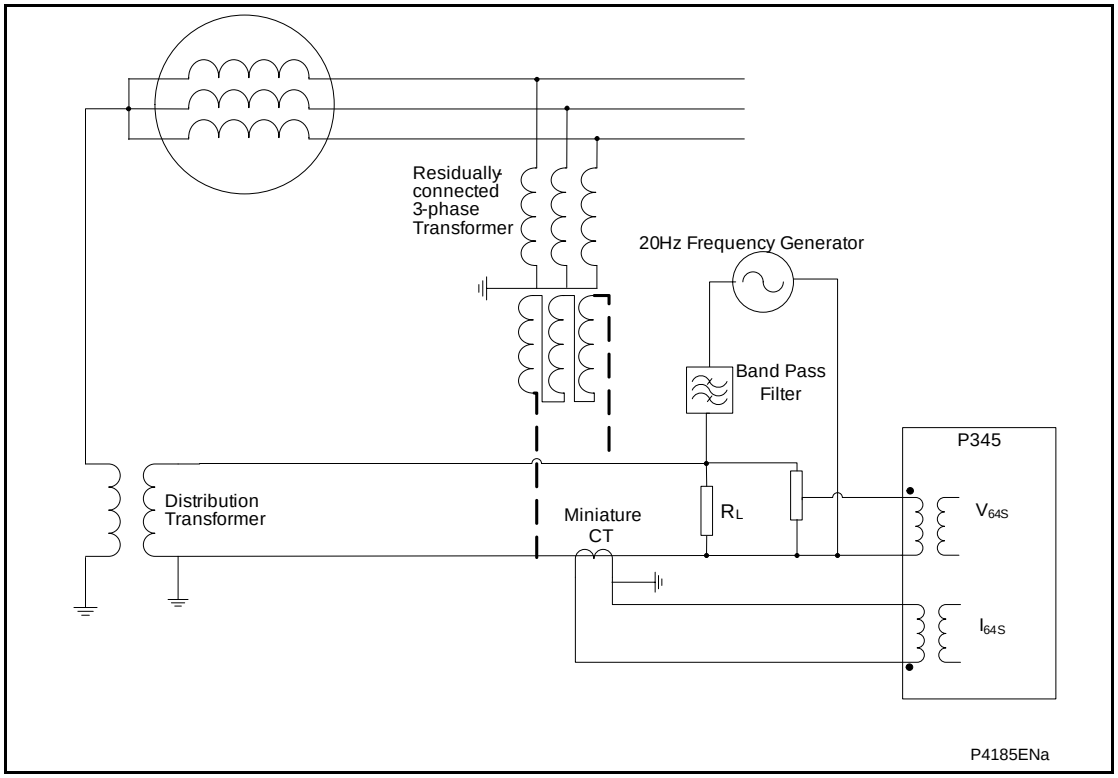
From the measured current and voltage vectors the complex impedance can be calculated and from this the ohmic resistance is determined. This eliminates disturbances caused by the stator earth capacitance and ensures high sensitivity. The relay algorithm can take into account a transfer resistance 64S Series R that may be present at the neutral or earthing voltage transformer. An example of the series resistance is the total leakage resistance of the earthing or neutral transformer, through which the injected voltage is applied to the generator neutral. The algorithm can also account for parallel resistance, 64S Parallel G (G = 1/R), such as the additional loading equipment connected on the LV side of the step-up transformer. Other error factors can be taken into account by the angle error compensation, 64 S Angle Comp.

The relay includes a 20 Hz overcurrent element which can be used as a back-up to the 20 Hz under resistance protection. The overcurrent element is not as sensitive as the under resistance elements as it does not include any transfer resistance compensation or any compensation for capacitance affects.

The 100% stator earth fault protection includes 2 stages of under resistance protection and an overcurrent protection stage. The under resistance protection is designed as a two stage protection system, one alarm stage (64S R<1 Alarm) and one trip stage (64S R<2 Trip), with each stage having a definite time delay setting. The overcurrent stage (64S I> Trip) is a single protection stage with a definite time delay setting. All the protection stages have separate DDB signals to indicate the start and trip of each stage and DDB signals to inhibit operation of each stage.

The protection includes a supervision element to evaluate a failure of the low frequency generator or the low frequency connection. The operation of an undervoltage and an undercurrent element after a time delay are used to indicate a failure. In case of a failure the protection can be blocked and give an alarm using the PSL. There is a 64S Fail signal which is connected to the 64S Fail Alarm signal in the default PSL to raise the alarm led and message and also to inhibit the 64S I>1/R<1/R<2 protection stages. For applications where the 100% stator earth fault 20 Hz generator is powered from a voltage transformer an alarm led and message may not be wanted every time the machine is off line which is why the 64S Fail Alarm signal and 64S Fail signal are separated.

Note: If required the 64S Fail Alarm or a User Alarm (Manual Reset User Alarm 5-16 is DDB 411-399) can be used to provide an alarm on the P345 via an opto-isolated input from the 20 Hz generator faulty output contact.



Where

RL loading resistor

V64S displacement voltage at the protective relay

I64S measuring current at the protective relay

Figure 60: Circuit diagram of the 100% stator earth fault protection with earthing (broken delta) transformer or neutral transformer

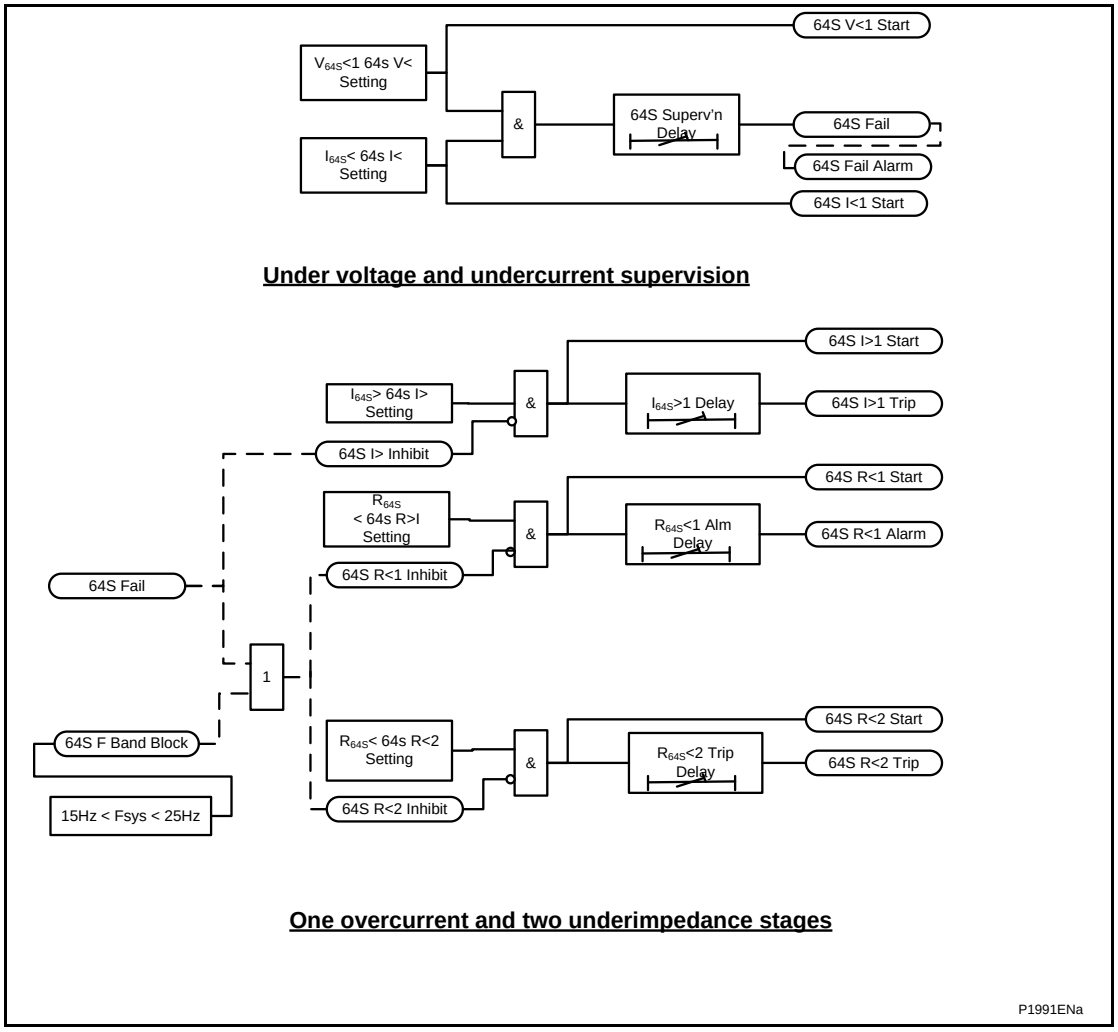


Figure 61: 64S 100% stator earth fault logic diagram

The 64S R<1/R<2/I>1 stages can be independently inhibited by energizing the relevant DDB signal via the PSL (64S I>1/R<1/R<2 Inhibit: DDB 552/553/554). DDB signals are also available to indicate the start, alarm and trip of the protection stages, (64S I>1/R<1/R<2 Start: DDB 1019/1020/1021, 64S R<1 Alarm: DDB 394, 64S I>1/R<2 Trip: DDB 778/780). DDB signals are available for the start of the supervision undercurrent and undervoltage elements (64S I< Start, 64S V<1 Start: DDB 1017/1018) and for the supervision fail and alarm (64S Fail: DDB 1298, 64S Fail Alarm: DDB 383). The 64S Fail DDB is mapped to the 64S I>1/R<1/R<2 inhibit signals and 64S Fail Alarm signal in the default PSL.

The 100% stator earth fault protection starts are mapped internally to the ANY START DDB signal - DDB 992.

1.22.1 Measurements

The relay samples the applied voltage and the circulating current at multiples of 20 Hz. Filtering algorithms are applied to extract the 20 Hz components from these two signals . The voltage and current magnitudes and phase angles, together with the resistance value are calculated.

The voltage and current protection settings and measurements are available only in secondary quantities. The resistance measurements are available in both primary and secondary quantities. The resistance and conductance settings are also subject to the **Primary/Secondary** conversion controlled by the **Setting Values** setting in the Configuration column.

The conversion is via a single **64S R Factor** Setting as follows:

R Primary = R Secondary * R Factor

OP

Examples of the setting calculations for the R Factor are shown in section 2.21.2 (*P34x/EN AP*).

An angle compensation setting, 64S Angle Comp, (θComp) is available to compensate for any CT angle error. The setting causes the current vector to be rotated by an angle θComp as shown.

$$\overline{I'_{64SComp}} = \overline{I_{64S}} \times 1\angle\theta_{Comp}$$

The fault resistance Rf is derived from $\overline{V_{64s}}$ and $\overline{I'_{64s}}$, such that any effect of the series resistance (Rs) and parallel resistance (Rp) within the injection circuitry, together with any reactance in the circuit and the capacitance of the stator windings to ground (Cg) can be eliminated.

The derivation is based on the following model. Both Rs and Rp are user settings, 64S R Series, 64S G Parallel (G = 1/R, the default setting of 0 is equivalent to Rp = infinity). As only the resistive component of the impedance is derived the value of the capacitance to ground and any reactance need not be known, as this information is not required for the Rf calculation.

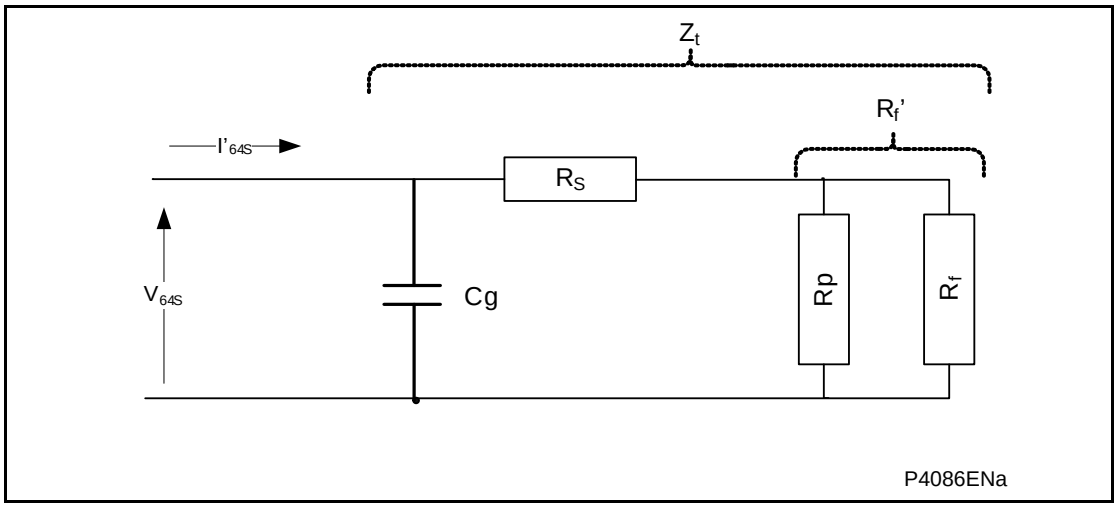


Figure 62: Model for 100% stator earth fault by injection

The calculated fault resistance Rf is used as the operating quantity for the 2-stage definite-time under resistance protection.

A definite-time overcurrent element is available as backup, with the 20 Hz current signal as the operating quantity.

The following measurements are available in the Measurements 3 column. All measurements are based on the 20 Hz components extracted from the voltage and current signals. A magnitude threshold level of 0.05 V and 0.1 mA for the voltage and current is implemented, below which the associated measurements display zero. The 64S R is the compensated resistance in both primary and secondary quantities. The resistance measurement displays a forced value to indicate an invalid measurement if either the voltage or the current magnitude is below the threshold.

MEASUREMENTS 3
64S V Magnitude
64S I Magnitude
64S I Angle
64S R secondary
64S R primary

Table 9: Measurements settings

Condition	Forced value 64S R
Protection disabled	999 MΩ
|V64S| < 100 mV	998 MΩ
|I64S| < 1 mA	997 MΩ
64S G Parallel x 64S R ⩾ 1.0	996 MΩ

Table 10: Forced values for 64S

Note: The above conditions are in descending priority order. The forced value primary scaled equivalent values will have exactly the same values, irrespective of the primary scaling factor setting.

The 64S Voltage signal is always used as the phase reference for the 64S current signal. The measurements are available in the Modbus and DNP3 interfaces. The **64S V Magnitude**, **64S I Magnitude** and **64S R secondary** are also available in the fault records.

The Disturbance recorder analogue input selection (G31) includes V_{64S} and I_{64S}. They are sampled at the recorder's sampling frequency (24 samples/power system cycle).

1.22.1.1 100% Stator earth fault filter characteristics

The P345's 64S protection has a very powerful band pass filter tuned to 20 Hz which is switched in when the system frequency is below 45 Hz. The band pass filter is designed with an attenuation of at least -80 db for frequencies less than 15 Hz and greater than 25 Hz. -80 db is equivalent to a noise rejection capability with a noise-to-signal ratio of 10000 to 1. The band-pass filter introduces an additional delay to the protection, but it is able to prevent low power system frequency components from interfering with the resistance calculation. There is also a low pass filter tuned to filter frequencies >30 Hz which is permanently enabled and is designed with an attenuation of at least -80 dB for frequencies >45 Hz to filter high power system frequency components. The settling time of the band-pass filter is longer than the low pass filter and so to achieve faster trip times when the generator is fully run-up to rated speed the band-pass filter is automatically switched out above 45 Hz. An option is available to switch-in the band-pass filter permanently by energizing the **64S Filter On** DDB. There is also Fourier filtering of the 20 Hz current and voltage inputs based on a fixed tracking frequency of 20 Hz.

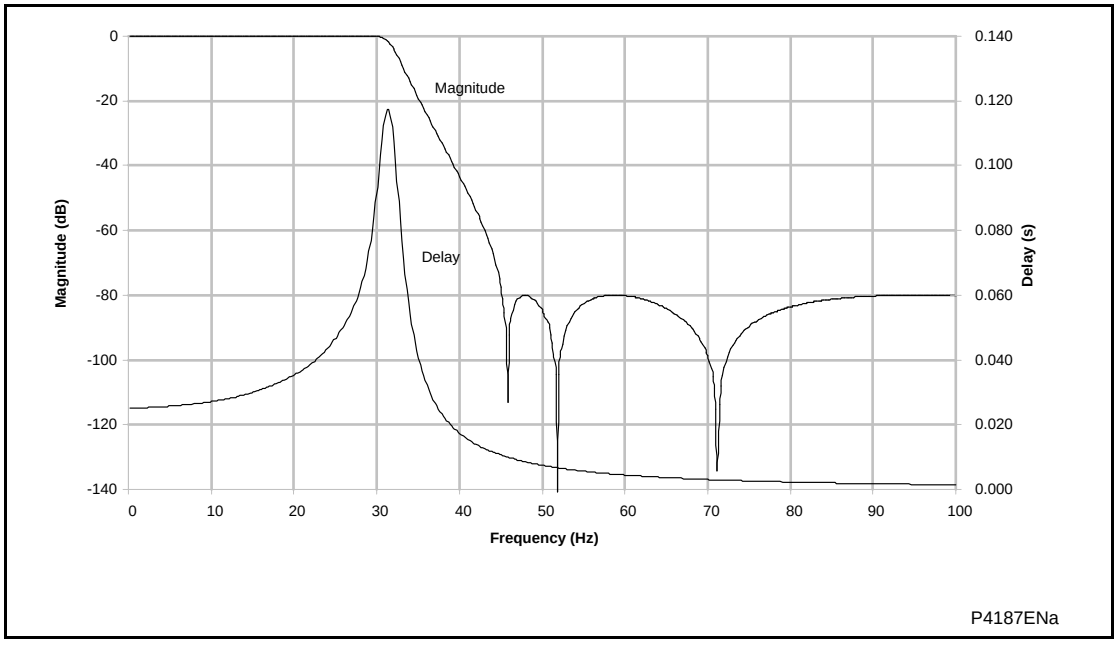


Figure 63: 64S elliptic 8th order low pass filter discrete frequency response

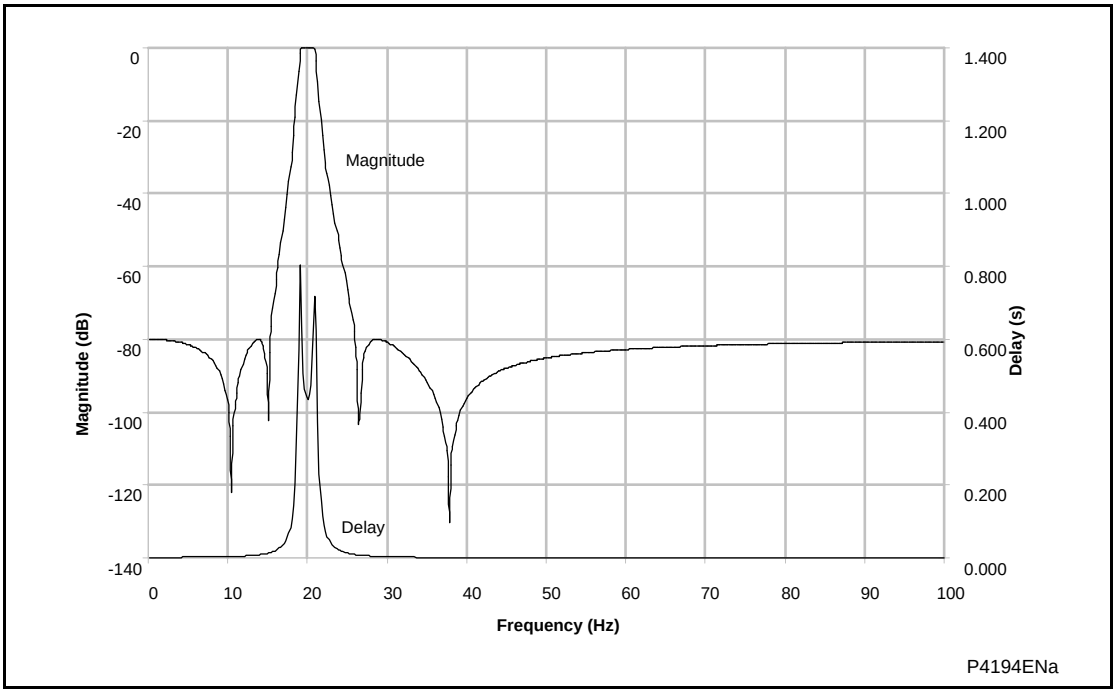


Figure 64: 64S Elliptic 4th order band pass filter discrete frequency response

When the machine is running up and the frequency of the machine coincides with the 20 Hz injected signal, if there is an earth fault at this time then there will be some interference from the 20 Hz fault signal from the machine with the injected 20 Hz signal.

This may cause the 64S measurements to be incorrect which may result in the protection not tripping. However, as the machine speeds up and the machine frequency moves away from 20 Hz then the relay will begin to accurately measure the injected 20 Hz signal and fault resistance. The bandpass filter will nearly fully attenuate any frequencies above 25 Hz so by the time the machine frequency has reached 25 Hz the relay will correctly measure the fault resistance if there is a fault present and trip correctly.

If the 100% stator earth fault protection operates during the generator start up there may be some zero sequence voltage being produced by the machine that coincides and is superimposed onto the 20 Hz injected signal, depending on the type of starting, causing incorrect measurements. The P345 100% stator earth fault protection includes a low pass filter and a bandpass filter which will filter signal frequencies 0-15 Hz and >25 Hz. DDB 1297 64S F Band Block operates when the frequency is between 15-25 Hz and can be used in the Programmable Scheme Logic to indicate a frequency in the target measuring range, 15-25 Hz. DDB signal 1297 can if necessary be used to block the 100% stator earth fault protection between 15-25 Hz via the inhibit signals, DDBs 552 - 64S I> Inhibit, DDB 553 - 64S R<1 Inhibit, DDB 554 - 64S R<2 Inhibit, see Figure 61 above. Note, DDB 1297 64S F Band Block is only active if frequency tracking is active. The frequency is active if any phase voltage is >0.1 Vn or any phase current is >0.05 In, see *P34x/EN F*D, section 3.4.3.

1.23 Overfluxing protection (24)

The P342/3/4/5/6 relays provide a five stage overfluxing element. The element measures the ratio of voltage, (VAB), to frequency, V/Hz, and will operate when this ratio exceeds the setting. One stage can be set to operate with a definite time or inverse time delay (IDMT) or a user curve (Default Curve 1/2/3/4. This stage can be used to provide the protection trip output. There are also 3 other definite time stages which can be combined with the inverse time characteristic to create a combined multi-stage V/Hz trip operating characteristic using PSL or a user curve can be used to create a more complex characteristic.

An inhibit signal is provided for the V/Hz>1 stage 1 only, which has the inverse time characteristic option. This allows a definite time stage to override a section of the inverse time characteristic if required. The inhibit has the effect of resetting the timer, the start signal and the trip signal.

There is also one definite time alarm stage that can be used to indicate unhealthy conditions before damage has occurred to the machine.

The V/Hz>1 stage can be inhibited by energizing the relevant DDB signal via the PSL (V/Hz>1 Inhibit: DDB 625). DDB signals are also available to indicate the start and trip of the protection, (Start: DDB 1068-1171, Trip: DDB 912-915). A further DDB 'V/Hz Alarm' signal is generated from the overfluxing alarm stage (DDB 372). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The overfluxing protection starts are mapped internally to the ANY START DDB signal – DDB 992.

The inverse time characteristic has the following formula:

$$t = \frac{TMS}{(M - 1)^2}$$

Where:

$$M = \frac{V/f}{(\text{V/f Trip Setting})}$$

V = Measured voltage

F = Measured frequency

Note, the IDMT characteristic has been changed in the 31 version software. The new characteristic is compatible with the old one and allows the option of future expansion of the number of characteristics with different exponents of (M-1).

Inverse time characteristic in software version 30 and lower is as shown below:

$$t = 0.8 + \frac{0.18 * TMS}{(M - 1)^2}$$

As well as the standard IDMT curve, it is possible to program up to four custom curves Default Curve 1/2/3/4 using General Electric's User Programmable Curve Tool, described in the MiCOM S1 Agile Setting Application Software User Guide. This is a user-friendly tool by which users can create curves either by formula or by entering data points. Programmable curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves.

The first stages of overfluxing protection in the P342-6 relays are provided with a timer hold facility, which may either be set to zero or to a definite time value. Setting of the timer to zero means that the overfluxing timer for that stage will reset instantaneously once the V/Hz falls below 95% of the setting. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period. When the reset time of the overcurrent relay is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the relay will integrate the fault current pulses, thereby reducing fault clearance time.

A definite time reset timer facility can be found for the V/Hz>1 stages as the setting **V/Hz>1 tRESET**. If an IDMT or DT operating characteristic is chosen, this definite time delay is set via the **V/Hz>1 tRESET** setting. If a user curve operate curve is selected, the reset characteristic may be set to either definite time or a user curve as selected in cell **V/Hz>1 Reset Char**.

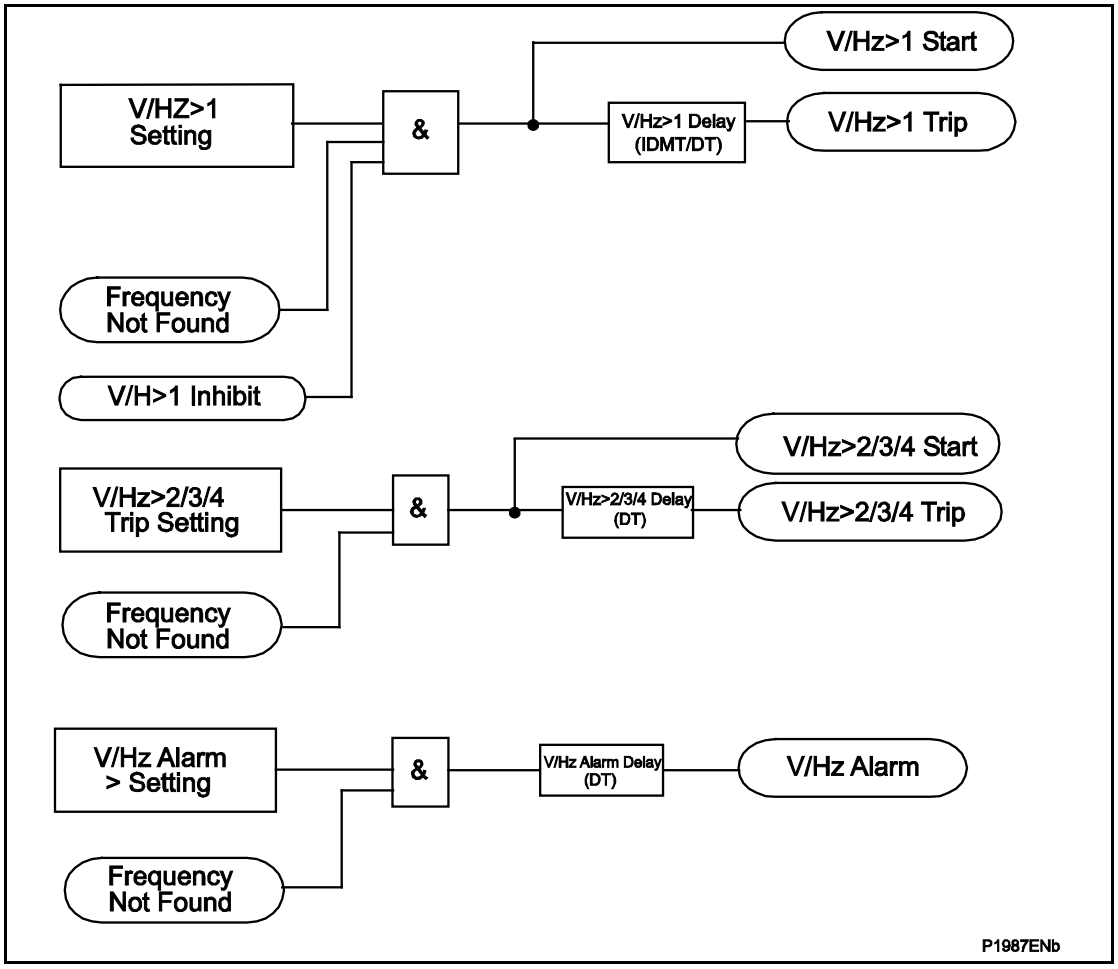


Figure 65: Overfluxing logic diagram

1.24 Rate of change of frequency protection (81R)

The df/dt function can be used to isolate an embedded generator connected to the utility's supply system under 'loss of mains' condition or for load shedding applications. An increase or decrease of the system frequency (df/ft) will be directly related to a sudden change of load on the generator. 4 stages of df/dt protection are included in P34x. The first stage, df/dt>1 is designed for loss of grid applications but can also be used for load shedding. For the first stage only, the user can select a deadband around the nominal frequency, within which this element is blocked. The dead band is defined with high and low frequency settings **df/dt>1 f Low** and **df/dt> f High**. The deadband is eliminated if the high and low frequencies are set the same or the **df/dt> f L/H** setting is set to **Disabled**. The deadband provides additional stability for non loss of grid disturbances which do not affect the machine frequency significantly. Each stage has a direction setting **df/dt>n Dir'n – Negative, Positive, Both**. This setting determines whether the element will react to rising or falling frequency conditions respectively, with an incorrect setting being indicated if the threshold is set to zero. For loss of mains applications the **df/dt>1 Dir'n** should be set to **Both** to match the previous P341 algorithm.

There are some global df/dt settings that affect all protection stages that can be used to smooth out the frequency measurements and provide stable operation of the protection, **df/dt avg cycles** and **df/dt iterations**. These settings enable the user to select the number of cycles the frequency is averaged over and the number of iterations of the averaged cycles before a start is given. Two **Operating Mode** settings are provided: **Fixed Window** and **Rolling Window** which are described below in detail. The **Fixed Window** setting is provided for compatibility with the previous P341 df/dt function which used two consecutive calculations of a 3 cycle fixed window to initiate a start.

The previous software version P341 df/dt element calculated the rate of change of frequency every 3 cycles by calculating the frequency difference over the 3-cycle period as shown below.

$$df/dt = \frac{f_n - f_{n\text{-}3cycle}}{3cycle}$$

Two consecutive calculations must give a result above the setting threshold before a trip decision can be initiated.

The df/dt feature is available only when the **df/dt** option is enabled in the **CONFIGURATION** menu. All the stages may be enabled/disabled by the **df/dt>n Status** cell depending on which element is selected.

1.24.1 Fixed window

The df/dt calculation is based on a user definable fixed window, 2 to 12 cycles. A new value of df/dt is (re)calculated every window. Increasing the window size improves measurement accuracy but has the disadvantage of increasing the measurement calculation time.

The elapsed time between start and end frequency measurements is calculated by summing up all sample interval times (NSamp) within the df/dt window (2 to 12 cycles).

Fault detection delay time (cycles) = df/dt Iterations x df/dt Avg Cycles.

1.24.2 Rolling window

The df/dt calculation is based on a user definable rolling window, 2 to 12 cycles. The window is a rolling buffer, so a new value of df/dt is (re)calculated every protection cycle execution. Increasing the window size improves measurement accuracy but has the disadvantage of increasing the measurement calculation time.

To help improve the accuracy of the df/dt measurement, the value of df/dt calculated is averaged; the length of the averaging buffer is the window size.

The elapsed time between start and end frequency measurements is calculated by summing up all sample interval times (NSamp) within the df/dt window (2 to 12 cycles).

P342/3/4 fault detection delay time (cycles) = df/dt Avg Cycles + (df/dt Iterations-1) x 1/4). Protection scheduler runs every ¼ cycle.

P345 fault detection delay time (cycles) = df/dt Iterations x df/dt Avg Cycles.

1.24.3 Logic diagram

DDB signals are available to indicate starting and tripping of the df/dt element (Start: DDB 1184, 1185, 1186, 1187 Trip: DDB 928, 929, 930, 931). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The df/dt start is mapped internally to the ANY START DDB signal – DDB 992.

The logic diagrams for the df/dt logic are as shown in Figure 66 and Figure 67.

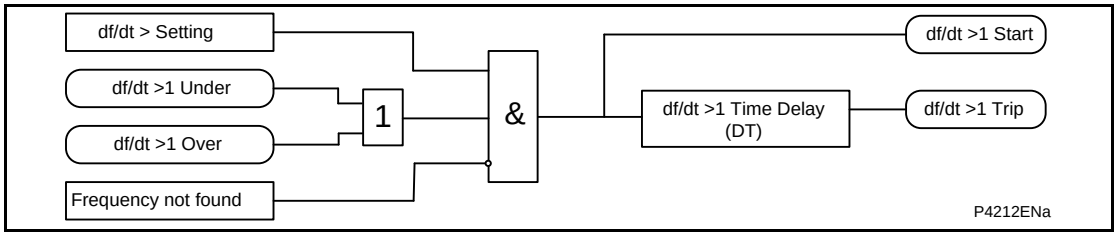


Figure 66: Rate of change of frequency logic diagram for df/dt>1

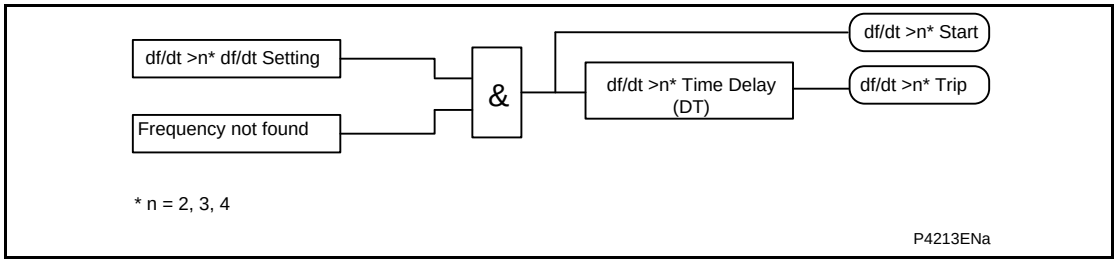


Figure 67: Rate of change of frequency logic diagram for df/dt>2, 3, 4

1.25 Dead machine/unintentional energization at standstill protection (50/27)

To provide fast protection for accidental energization of a generator when the machine is not running condition, the P343/4/5 relay provides an instantaneous overcurrent element that is gated with a three-phase undervoltage detector and is blocked by the VT supervision element. The scheme logic of this function is shown in Figure 68. The 3 phase current source can be selected using the **DM CT Source** – **IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting.

A DDB signal is available to indicate tripping of the dead machine element (Trip: DDB 880). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

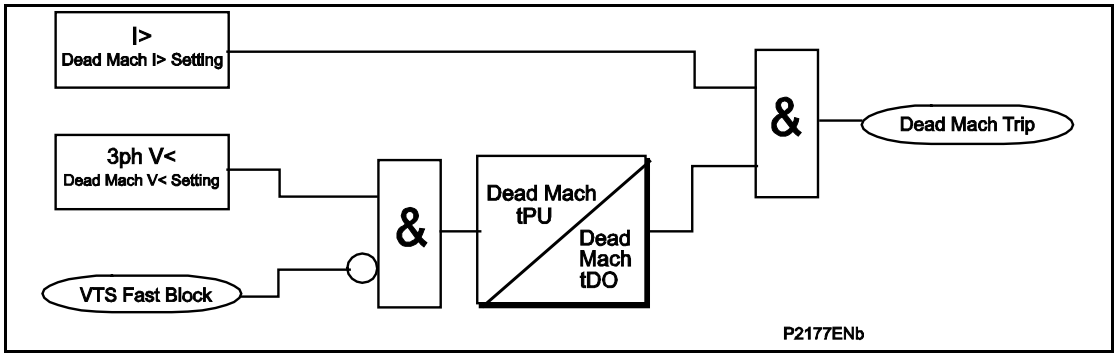


Figure 68: Fixed scheme logic for unintentional energization of standstill protection

1.26 Resistive temperature device (RTD) thermal protection

To protect against any general or localized overheating, the P342/3/4/5/6 relay has the ability to accept inputs from up to 10 - 3 wire Type A PT100 resistive temperature sensing devices (RTD). These are connected as shown in Figure 69.

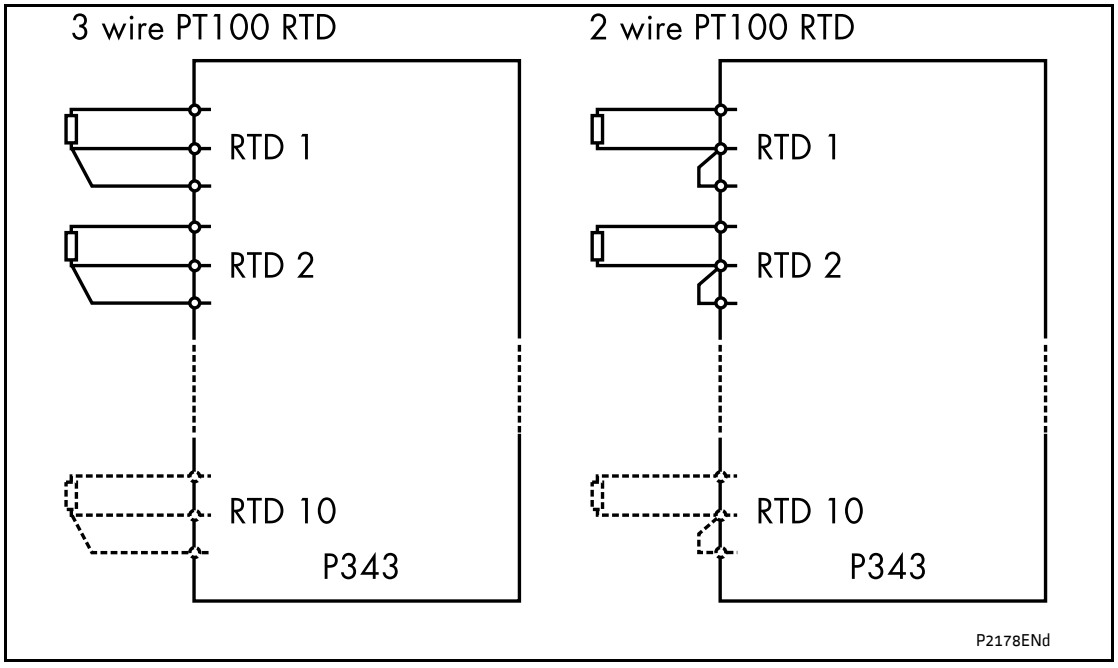


Figure 69: Connection for RTD thermal probes

Such probes can be strategically placed in areas of the machine that are susceptible to overheating or heat damage.

- Typically a PT100 RTD probe can measure temperature within the range –40° to +300°C. The resistance of these devices changes with temperature, at 0°C they have a resistance of 100 Ω

Should the measured resistance be outside of the permitted range, an RTD failure alarm will be raised, indicating an open or short circuit RTD input.

These conditions are signaled via DDB signals available within the PSL (DDB 375-378) and are also shown in the measurements 3 menu.

DDB signals are also available to indicate the alarm and trip of the each and any RTD, (Alarm: DDB 1304-1313, 374 Trip: DDB 976-985, 986). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

See the Installation chapter (*P34x/EN IN*), for recommendations on RTD connections and cables.

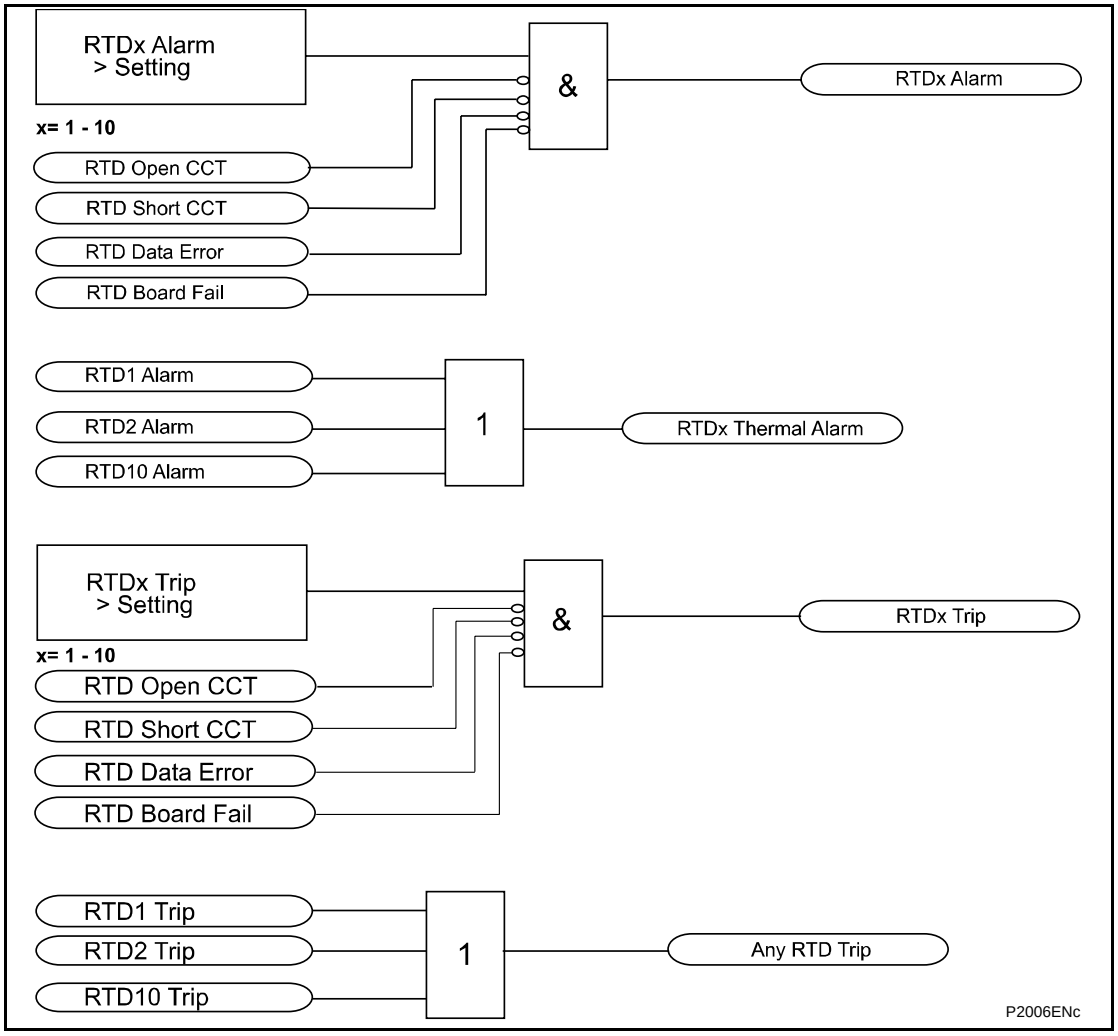


Figure 70: RTD logic diagram

1.26.1 Principle of the RTD connection

The aim of such a connection is to compensate the influence of the r1 and r2 resistors.

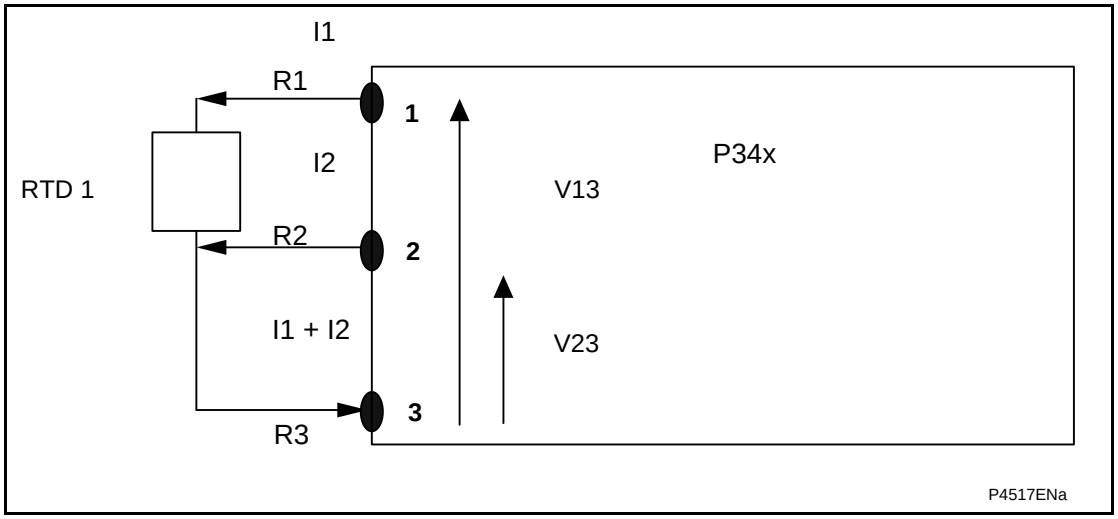


Figure 71: Principle of RTD connection

A constant current is injected by the P34x relay from the connections1 and 2: i1 = i2

V13 = r1 * I1 + R_{rtd} * I1 - r3 * (I1 + I2),

V23 = r2 * I2 - r3 * (I1 + I2),

V13 - V23 = r1 * I1 + R_{rtd} * I1 - r3 * (I1 + I2) - r2 * I2 + r3 * (I1 + I2)

Assuming that the three cables have the same length and are the same material, hence the resistors r1, r2 and r3 are the same:

V13 - V23 = R_{rtd} * I1 = Voltage at the RTD terminals.

1.27 P343/4/5 pole slipping protection (78)

1.27.1 Lenticular scheme

1.27.1.1 Characteristic

The P343/4/5/6 pole slipping characteristic consists of three parts as shown in the R/X diagram of Figure 71. The first part is the lenticular (lens) characteristic. The second is a straight line referred to as the blinder that bisects the lens and divides the impedance plane into the left and right halves. The third is a reactance line which is perpendicular to the blinder.

The inclination of the lens and the blinder, θ, is determined by the angle of the total system impedance. The equivalent impedance of the system and the step-up transformer determines the forward reach of the lens, Z_A, whereas the generator's transient reactance determines the reverse reach Z_B. The width of the lens is varied by the setting of the angle α.

A reactance line, perpendicular to the axis of the lens, is used to distinguish whether the impedance center of the swing is located in the power system or in the generator. It is set by the value of Zc along the axis of the lens, as shown in Figure 71. The reactance line splits the lens into Zone 1 (lens below the line) and Zone 2 (all of the lens).

For the pole slipping protection element the minimum operating current is 2% In and the minimum voltage is 1 V for 100/120 and 4 V for 380/480 V ratings. The pole slipping protection operates from the IA and VA current and voltage inputs to the relay.

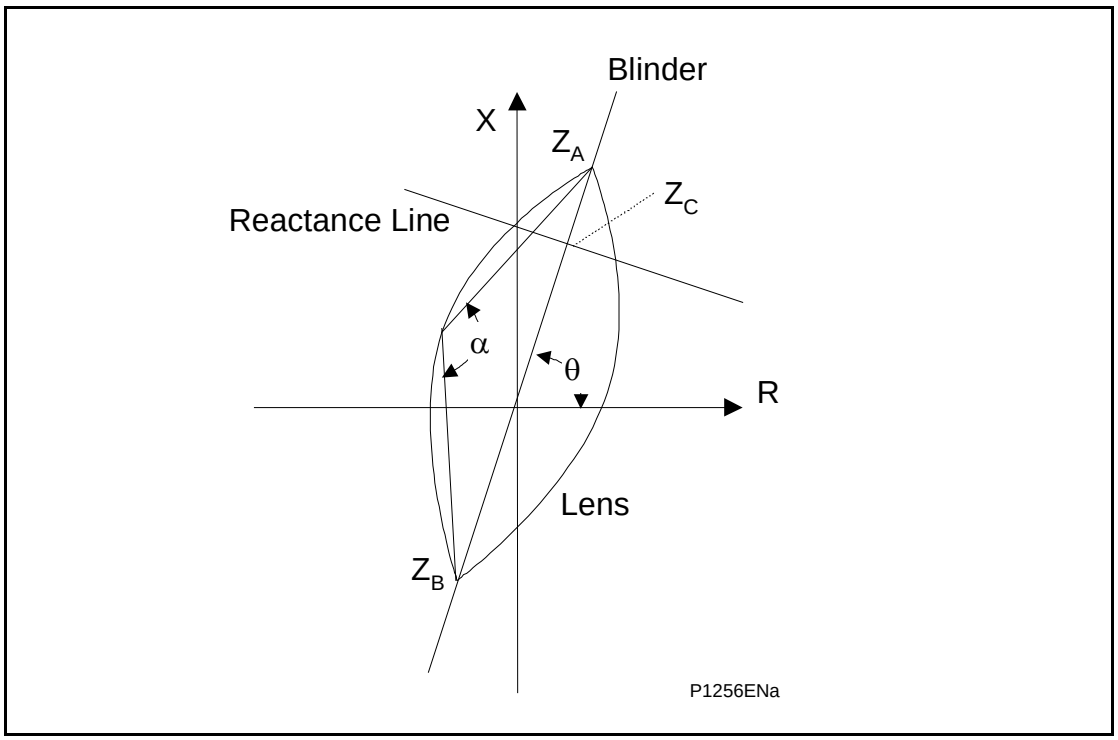


Figure 72: Pole slipping protection using blinder and lenticular characteristic

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1.27.1.2 Generating and motoring modes

When a generator is out of step with the system, the impedance locus is expected to traverse from right to left across the lens and the blinder. However, if the generator is running as a motor, as in the pumping mode of a pump storage generator, the impedance locus is expected to swing from the left to the right. A setting is provided to determine whether the protection operates in a generating mode or in a motoring mode or both.

If the protection is running in the generating mode, the impedance is expected to be at the right hand side of the lens under normal load conditions. During a pole slip the impedance locus traverses across the right half and the left half of the lens. The minimum time spent in each half of the lens can be set with timers T1 for the right hand side and T2 for the left hand side. The relay registers a pole slipping cycle when the locus finally leaves the lens at the opposite end.

If the protection is running in the motoring mode, the impedance is expected to be at the left hand side of the lens under normal load conditions. During a pole slip the impedance locus traverses across the left half and the right half of the lens, again spending at least the time T1 and T2 respectively in each half and leaves the lens at the opposite end.

1.27.2 Pole slipping protection operation

The pole slipping protection algorithm is executed 4 times per power system cycle to obtain accurate timing of the impedance locus traversing the lens.

1.27.2.1 State machine

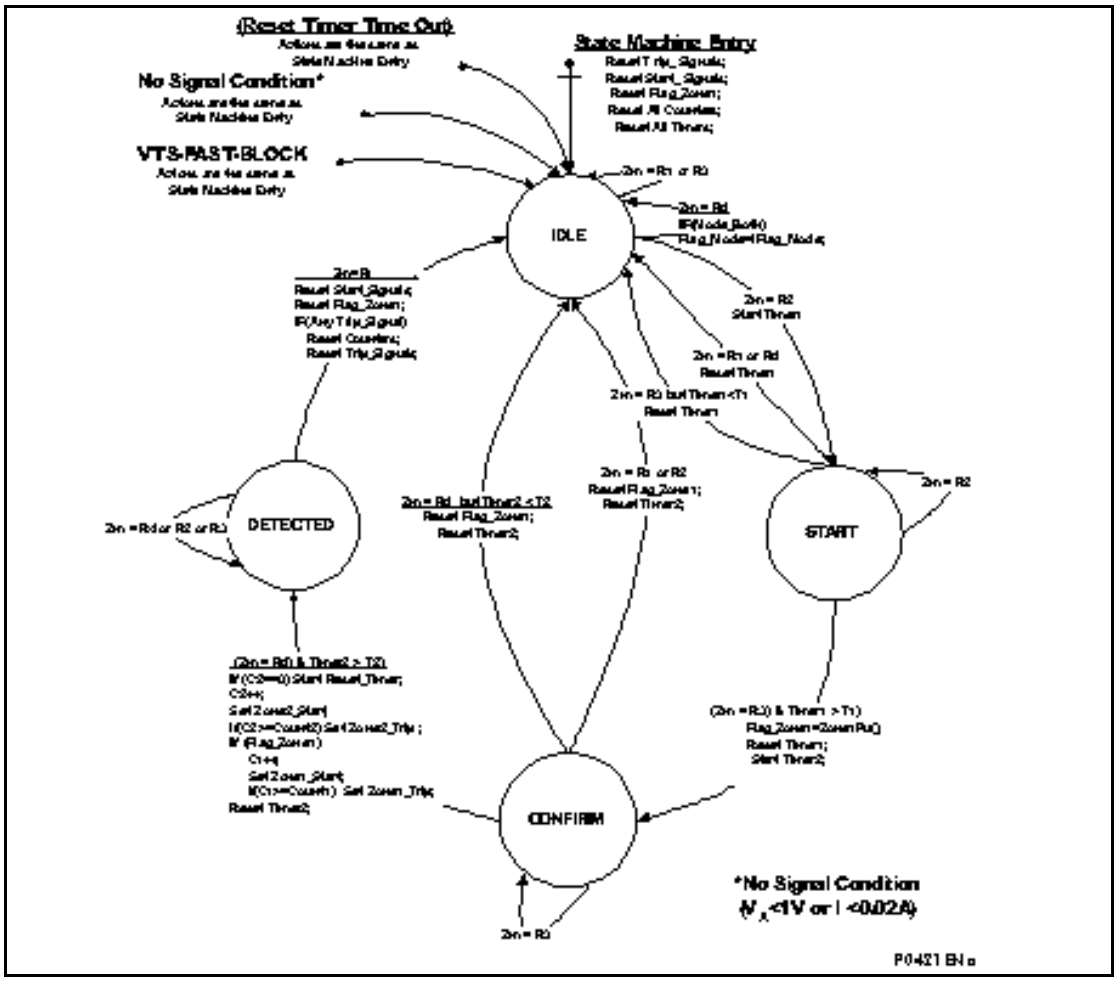


Figure 73: State machine

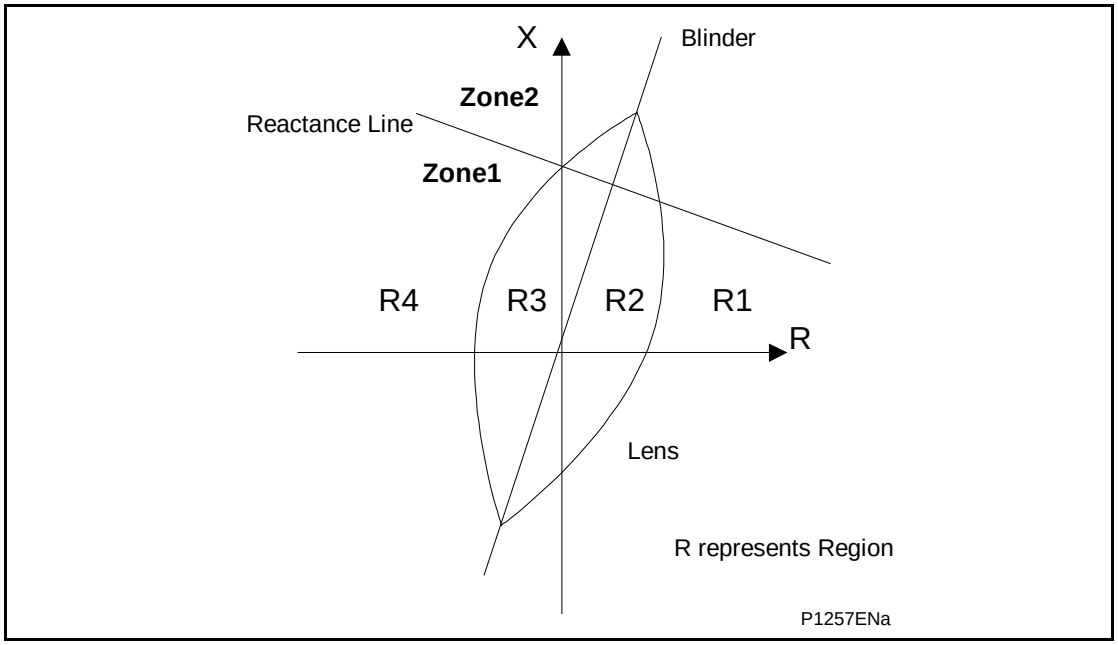


Figure 74: Regions and zones definition (generating mode)

Note: The regions shown in Figure 74 are independent of the reactance line although it is shown in the same diagram (zones are independent of the lens and the blinder).

To track the impedance locus under a pole slipping condition, a 'State Machine' approach is adopted. There are 4 states 'Idle', 'Start', 'Confirm' and 'Detected' used to describe the movement of the impedance locus. Each state has one entrance and one or several exit terminals depending on the state. Exit terminals fall into two categories: 'normal exit' and 'abnormal exit'. There is only one 'normal exit' which leads to the next state when the impedance locus moves into the desired region. Unexpected impedance movement will result in a return to the 'Idle' State or will be ignored depending on where the impedance stays.

- Idle: This is the normal state when the measured impedance is the normal load impedance. The impedance locus of any pole slip should start from here. In this state the 'normal exit' is when the measured impedance moves from R1 to R2. Timer 1 that is used to time the duration of the impedance locus remaining in R2 is started when this change is detected.

If the impedance locus moves to R4 and 'Both' is selected in the 'Mode' setting, a flag (Flag_Mode) indicating the generator operating mode is toggled to indicate 'Motoring'. Note, this does not cause a state transition, refer to section 1.27.2.4 for details about the 'Flag_Mode'.

In this state impedance locus changes to R3 will be ignored.

- Start: This is the state when the impedance locus stays inside R2. Normal exit is taken only if the impedance has stayed in R2 longer than the T1 time delay and moves to R3. Three actions are carried out along with this transition: check the operating status of the reactance line, start Timer 2 and reset Timer 1. The purpose of checking the operating status of the reactance line at this point is to decide whether the pole slip belongs to Zone1 or Zone2. A flag (Flag_Zone1) is latched if Zone1 picks up, which is used later on to differentiate whether counters are incremented for pole slips in zone1 or zone2. Theoretically, this flag is generated at the point where the impedance locus intersects the blinder, which is called the electrical center. Timer2 is used to time the duration of the impedance locus remaining in R3;

If the impedance moves to R1 or R4 or moves to R3 but stays in R2 less than T1, the state machine will be reset to the 'Idle' state. Timer 1 is reset when the impedance leaves R2 via these abnormal exits. Besides pole slipping, a stable power swing or fault occurrence could enter this state as well. The state machine is designed to differentiate these conditions.

- Confirm: This state is reached when the impedance has crossed the blinder and arrived at Region3. Further confirmation is required to see if the impedance stays for at least time T2 and is bound to leave for R4. Otherwise, an abnormal exit will reset the state machine to the 'Idle' state. Actions on abnormal transition include resetting Flag_Zone1 and Timer 2.

Note: As soon as the impedance locus leaves the lens through the normal exit counters of different zones will be updated, depending on the Flag_Zone1 and if the pole slip has completed the pre-set slip cycles setting a trip signal is given. If Flag_Zone1 is set then the Zone 1 counter (C1) will be incremented. Zone 2 is the backup pole slipping stage and so all pole slips increment the Zone2 counter (C2).

The Reset_Timer and reset Timer 2 are started when the normal transition occurs. The Reset_Timer is started only when the first pole slip is detected and will be reset in its time delay (see Reset_Timer time out actions in the state machine diagram).

- Detected: This is the stage where the impedance locus has to complete its full cycle although the counter is updated in the previous confirm stage. Abnormal movements of the impedance locus in this stage will be ignored and this state is kept until the impedance moves to R1 indicating completion of a pole slip cycle. If a trip signal has not been given for this pole slip, only the Start_Signals and Flag_Zone1 are reset in preparation for the next pole slip cycle. However, if a trip signal has been issued, then the Trip_Signals and the counters are both reset.

In general, once the measured impedance has traversed all the 'States' in the normal exit sequence, a pole slip is confirmed. For a stable power swing or fault condition the measured impedance will not satisfy all the exit transition criteria.

The 'State Machine' diagram has been simplified to present an overview of how to detect pole slipping. There are also several supporting protection functions which are explained in the following sections.

1.27.2.2 Protection functions and logic structure

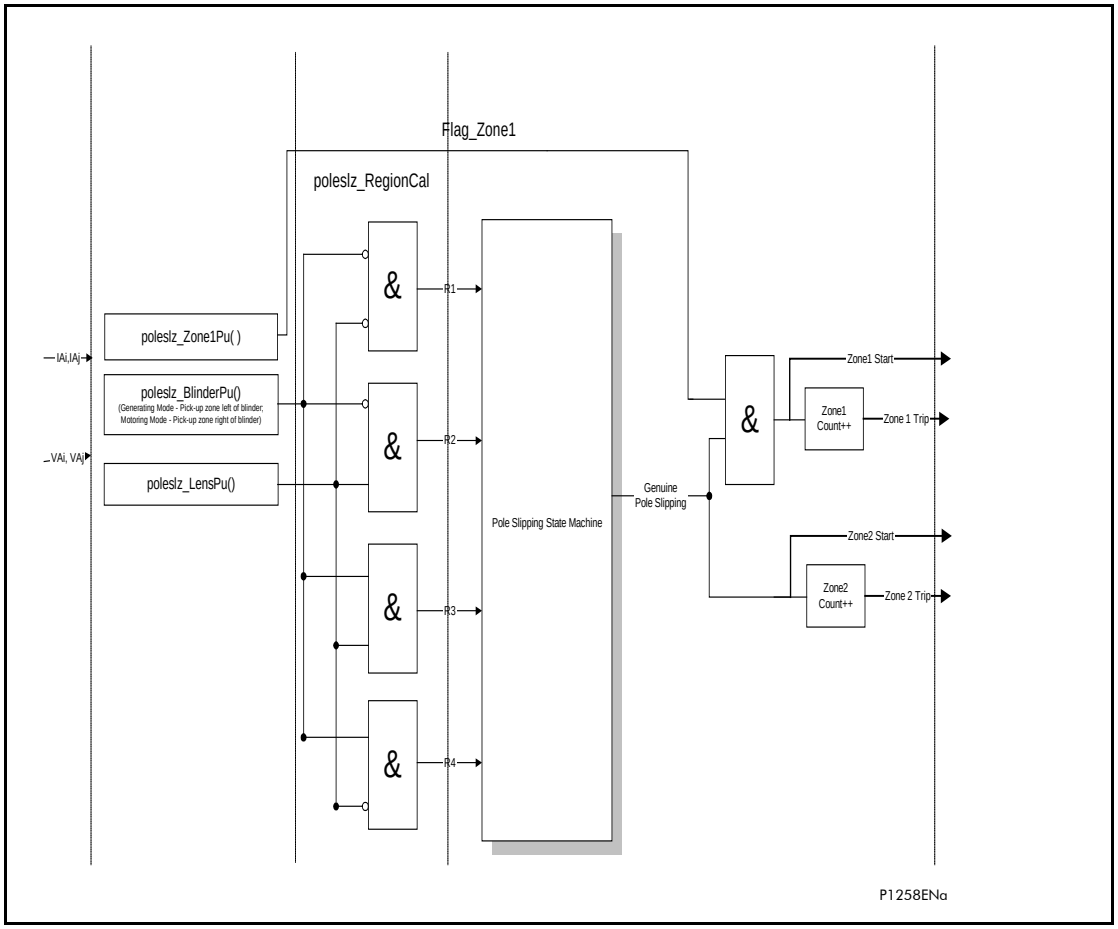


Figure 75: Logic structure of pole slipping module

There are several protection functions called in sequence in the pole slipping detection, as shown in the above diagram, they are:

- poleslz_Zone1Pu
- poleslz_LensPu
- poleslz_BlinderPu
- poleslz_RegionCal

Function poleslz_Zone1Pu(), poleslz_LensPu() and Poleslz_BlinderPu() calculate whether the Reactance Line, Lens and Blinder characteristics have picked up respectively.

At the end of each function, DDBs associated with each characteristic are mapped according to the elements operating status. Outputs from poleslz_LensPu() and Poleslz_BlinderPu() feed into the poleslz_RegionCal() to determine in which 'Region' the locus is present. After the region and zone have been determined the state machine can be evaluated.

For the purpose of discriminating the pole slipping zone, Zone1 or Zone2, it is important to check the result of poleslz_Zone1Pu() when the impedance locus leaves the 'Start' state by the 'normal exit'. A flag is latched if Zone1 picks up, which is used to identify the pole slipping zone later on.

1.27.2.3 Motoring mode

When the 'pole slip mode' setting is set to 'motoring' the protection algorithm is switched to motoring mode. Motoring mode is essentially the same for generating mode except that the pick-up zone for the blinder is changed from the left hand side to the right hand side, as shown in Figure 76. This requires changes to the blinder algorithm in poleslz_BlinderPu().

OP

This automatically changes the region definition on the impedance plane. For example, under normal motoring conditions, both the blinder, which picks up from the left hand side for motoring, and the lens will not be picked up. Therefore the poleslz_RegionCal() will output a region number R1.

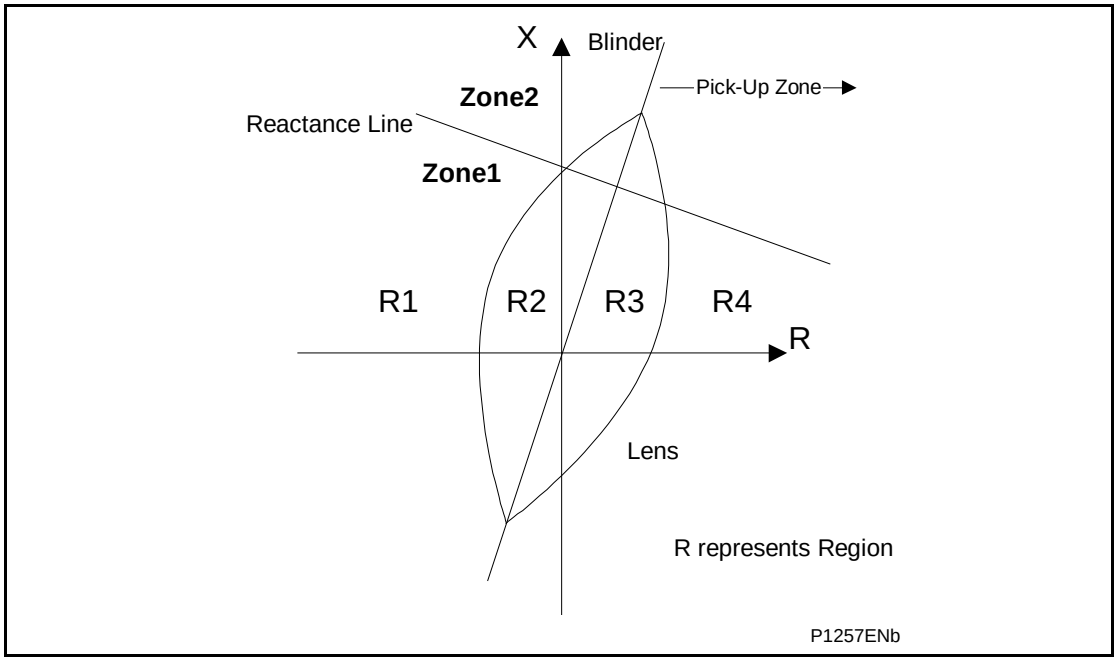


Figure 76: Regions and zones definition (motoring mode)

1.27.2.4 Generating and motoring mode

For a pump storage generator, its operation can switch from generating mode to motoring mode and vice versa. Therefore a facility is provided for the protection to detect the normal running mode of the machine (generating or motoring) and to perform pole slipping detection in either mode.

This facility is enabled when the **Pole Slip Mode** setting is set to **Both**.

Also, when a generator is running at low load, <30% load, due to the presence of heavy system damping during a fault the generator can slow down and result in a motor like slip (negative slip). To detect pole slips for this condition then the 'pole slip mode' should be set to 'Both'.

In the state machine, a flag called 'Flag_Mode' is used to deal with the mode change. During the initialization, the flag is set to 'generating', with the pick up zone of the blinder on the left-hand side. If the impedance traverses the blinder from R1 to R4 in the 'Idle' state, the 'Flag_Mode' is toggled to 'Motoring'. This causes the blinder pick-up zone to change from the left-hand side to right-hand side, therefore automatically redefining the regions numbering on the impedance plane, as discussed previously. Subsequent crossing of the blinder from R1 to R4 in the 'Idle' mode will cause the 'Flag_Mode' to toggle, therefore tracking the normal running operation of the pump storage generator, irrespective of whether it is in generating or motoring mode.

1.27.2.5 DDB output

Apart from the Zone1 and Zone2 start and trip signals, each measuring element also outputs its 'status' onto the DDB. These signals can be used during commissioning testing to determine the shape and the accuracy of the characteristics. The pole slipping Z1 and Z2 protection starts are mapped internally to the ANY START DDB signal – DDB 992.

DDB name	Description
DDB 866 PSlipz Z1 Trip	Pole slipping tripped in Zone1
DDB 867 PSlipz Z2 Trip	Pole slipping tripped in Zone2
DDB 1122 PSlipz Z1 Start	Pole slipping detected in Zone1
DDB 1123 PSlipz Z2 Start	Pole slipping detected in Zone2
DDB 1124 PSlipz LensStart	Measured impedance is within the Lens
DDB 1125 Pslipz BlindStrt	Impedance lies left hand side of Blinder
DDB 1126 PSlipz ReactStrt	Impedance lies in Zone 1 distinguished by Reactance line

Table 11: Pole strip protection DDBs

1.28 Generator Thermal overload protection (49G)

1.28.1 Introduction

The physical and electrical complexity of generator construction results in a complex thermal relationship. Therefore it is not possible to create an accurate mathematical model of the true thermal characteristics of the machine.

However, if a generator is considered to be a homogeneous body, developing heat internally at a constant rate and dissipating heat at a rate directly proportional to its temperature rise, it can be shown that the temperature at any instant is given by:

$T = T_{max} (1-e^{-t/\tau})$

Where:

T_{max} = final steady state temperature

τ = heating time constant

This assumes a thermal equilibrium in the form:

Heat developed = Heat stored + Heat dissipated

Temperature rise is proportional to the current squared:

$T = K I_R^2 (1-e^{-t/\tau})$

$T = T_{max} = K I_R^2$ if $t = \infty$

Where:

IR = the continuous current level which would produce a temperature T_{max} in the generator

For an overload current of 'I' the temperature is given by:

$T = KI^2 (1-e^{-t/\tau})$

For a machine not to exceed T_{max}, the rated temperature, then the time 't' for which the machine can withstand the current 'I' can be shown to be given by:

$T_{max} = KI_R^2 = KI^2 (1-e^{-t/\tau})$

$t = \tau . \text{Loge} (1/(1-(I_R/I)^2))$

An overload protection element should therefore satisfy the above relationship. The value of I_R may be the full load current or a percentage of it depending on the design.

As previously stated it is an oversimplification to regard a generator as an homogeneous body. The temperature rise of different parts or even of various points in the same part may be very uneven. However, it is reasonable to consider that the current-time relationship follows an inverse characteristic. A more accurate representation of the thermal state of the machine can be obtained through the use of temperature monitoring devices (RTDs) which target specific areas. Also, for short time overloads the application of RTDs and overcurrent

protection can provide better protection. Note, that the thermal model does not compensate for the effects of ambient temperature change. So if there is an unusually high ambient temperature or if the machine cooling is blocked RTDs will also provide better protection.

1.28.2 Thermal replica

The P342/3/4/5/6 relay models the time-current thermal characteristic of a generator by internally generating a thermal replica of the machine. The thermal overload protection can be selectively enabled or disabled. The positive and negative sequence components of the generator current are measured independently and are combined together to form an equivalent current, I_{eq}, which is supplied to the replica circuit. The heating effect in the thermal replica is produced by I_{eq}^2 and therefore takes into account the heating effect due to both positive and negative sequence components of current.

Unbalanced phase currents will cause additional rotor heating that may not be accounted for by some thermal protection relays based on the measured current only. Unbalanced loading results in the flow of positive and negative sequence current components. Load unbalance can arise as a result of single-phase loading, non-linear loads (involving power electronics or arc furnaces, etc.), uncleared or repetitive asymmetric faults, fuse operation, single-pole tripping and reclosing on transmission systems, broken overhead line conductors and asymmetric failures of switching devices. Any negative phase sequence component of stator current will set up a reverse-rotating component of stator flux that passes the rotor at twice synchronous speed. Such a flux component will induce double frequency eddy currents in the rotor, which can cause overheating of the rotor body, main rotor windings, damper windings etc. This extra heating is not accounted for in the thermal limit curves supplied by the generator manufacturer as these curves assume positive sequence currents only that come from a perfectly balanced supply and generator design. The P34x thermal model may be biased to reflect the additional heating that is caused by negative sequence current when the machine is running. This biasing is done by creating an equivalent heating current rather than simply using the phase current. The M factor is a constant that relates negative sequence rotor resistance to positive sequence rotor resistance. If an M factor of 0 is used the unbalance biasing is disabled and the overload curve will time out against the measured generator positive sequence current.

Note: The P34x also includes a negative sequence overcurrent protection function based on I_2^2t specifically for thermal protection of the rotor.

The equivalent current for operation of the overload protection is in accordance with the following expression:

$$I_{eq} = \sqrt{(I_1^2 + MI_2^2)}$$

Where:

I1 = Positive sequence current

I2 = Negative sequence current

M = A user settable constant proportional to the thermal capacity of the machine

As previously described, the temperature of a generator will rise exponentially with increasing current. Similarly, when the current decreases, the temperature also decreases in a similar manner. Therefore to achieve close sustained overload protection, the P342/3/4/5/6 relay incorporates a wide range of thermal time constants for heating and cooling.

Furthermore, the thermal withstand capability of the generator is affected by heating in the winding prior to the overload. The thermal replica is designed to take account the extremes of zero pre-fault current, known as the ‘cold’ condition and the full rated pre-fault current, known as the ‘hot’ condition. With no pre-fault current the relay will be operating on the ‘cold curve’. When a generator is or has been running at full load prior to an overload the ‘hot curve’ is applicable. Therefore during normal operation the relay will be operating between these two limits.

The following equation is used to calculate the trip time for a given current. Note that the relay will trip at a value corresponding to 100% of its thermal state.

The thermal time characteristic is given by:

$t = \tau \log_e (I_{eq}^2 - I_P^2)/(I_{eq}^2 - (\text{Thermal } I>)^2$

Where:

t = Time to trip, following application of the overload current, I

τ = Heating time constant of the protected plant

I_{eq} = Equivalent current

Thermal I> = Relay setting current

I_P = Steady state pre-load current before application of the overload

The time to trip varies depending on the load current carried before application of the overload, i.e. whether the overload was applied from 'hot" or "cold".

The thermal time constant characteristic may be rewritten as:

$\exp(-t/\tau) = (\theta - 1)/(\theta - \theta_p)$

$t = \tau \log_e (\theta - \theta_p) / (\theta - 1)$

Where:

$\theta = I_{eq}^2/(\text{Thermal } I>)^2$

and

$\theta p = I_p^2/(\text{Thermal } I>)^2$

Where θ is the thermal state and is θp the pre-fault thermal state.

Note: The thermal model does not compensate for the effects of ambient temperature change.

$t = \tau . \text{Log}_e ((K^2-A^2)/(K^2-1))$

$t_{alarm} = \tau . \text{Log}_e ((K^2-A^2)/(K^2-(\text{Thermal Alarm}/100))$

Where:

$K = I_{eq}/\text{Thermal } I>$ (K^2 = Thermal state, θ)

$A = I_P/\text{Thermal } I>$ (A^2 = Pre-fault thermal state, θ_p)

Thermal Alarm = Thermal alarm setting, 20-80%

The Thermal state of the machine can be viewed in the **Thermal Overload** cell in the **MEASUREMENTS 3** column. The thermal state can be reset by selecting 'Yes' in the **Reset ThermalO/L** cell in **Measurements 3**. Alternatively the thermal state can be reset by energizing DDB 641 **Reset Gen Thermal** via the relay PSL.

A DDB signal **Gen Thermal Trip** is also available to indicate tripping of the element (DDB 945). A further DDB signal **Gen Thermal Alm** is generated from the thermal alarm stage (DDB 371). The state of the DDB signal can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

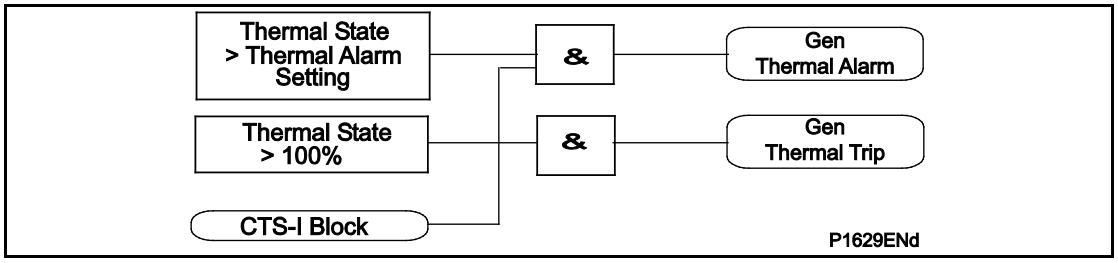


Figure 77: Thermal overload protection logic diagram

The functional block diagram for the thermal overload protection is shown in Figure 77.

1.29 Transformer Thermal overload protection (49T)

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Transformer thermal overload protection is designed to protect the equipment from sustained overload that results in the transformer's thermal rating being exceeded. Thermal overload protection compliments the transformer overcurrent protection by allowing modest but transient overload conditions to occur, while tripping for sustained overloads that the overcurrent protection will not detect.

The thermal overload function is based on the IEEE Standard C57.91-1995. This function can be enabled or disabled in the setting or it can be blocked in the PSL. Two three-stage definite time-delayed trip elements based on hot spot or top oil temperature are available. A pre-trip alarm is offered in the tPre-trip Set setting. This alarm indicates that thermal overload will trip after the settable time if load level remains unchanged.

The monitor winding can be set to HV, LV or biased current. If the monitor winding is set to biased current an overall through loading picture of the transformer is provided.

To calculate the top oil and hot spot winding temperature, the relay takes into consideration the ratio of the ultimate load to the rated load. The rated load is determined by the IB and the rating settings. When the monitored winding is set as the HV winding, the rated load is calculated using the HV Rating and the IB settings. When the monitored winding is set as the LV winding, the rated load is calculated using the LV Rating and the IB settings. When the monitored winding is set as the biased current, the rated load is calculated using the REF Power S and the IB settings. When the monitored winding is set as the HV winding, the rated load is calculated using the HV Rating and the IB settings. When the monitored winding is set as the LV winding, the rated load is calculated using the LV Rating and the IB settings. When the monitored winding is set as the biased current, the rated load is calculated using the REF Power S and the IB settings. The ultimate load is the load that is actually being fed by the transformer.

The biased current used by the thermal protection is not the same as the biased current used by the differential protection. No vector correction or zero sequence filtering is taken into account. The thermal element uses the maximum phase biased current.

The thermal overload model is executed every power cycle. The thermal overload trip can be based on either hot spot temperature or top oil temperature, or both.

1.29.1 Inputs

Signal name	Description
IA-HV, IB-HV, IC-HV, IA-LV, IB-LV, IC-LV,	Phase current levels (raw samples). The currents required by the thermal overload element are the currents of the winding being monitored.
IA-bias, IB-bias, IC-bias	Bias currents
ΘTO	Measured top oil temperature
ΘA	Measured ambient temperature
Reset X thermal (DDB 649)	Reset thermal overload

Signal name	Description
Forced Air Cool (DDB 650)	If DDB 650 = 1 then cooling mode is Forced Air Cooling, if DDB 651 = 1 then cooling mode is Forced Oil Cooling, if DDB 650 and 651 = 1 then cooling mode is Forced Air Oil Cooling, if DDB 650 and 651 = 0 then cooling mode is Natural Cooling.
Forced Oil Cool (DDB 651)	As above

Table 12: VTS inputs

1.29.2 Outputs

Signal name	Description
Top oil >1 start (DDB 1203)	Top oil first stage start
Top oil >2 start (DDB 1204)	Top oil second stage start
Top oil >3 start (DDB 1205)	Top oil third stage start
Top oil >1 trip (DDB 949)	Top oil first stage trip
Top oil >2 trip (DDB 950)	Top oil second stage trip
Top oil >3 trip (DDB 951)	Top oil third stage trip
Hot spot >1 start (DDB 1200)	Hot spot first stage start
Hot spot >2 start (DDB 1201)	Hot spot second stage start
Hot spot >3 start (DDB 1202)	Hot spot third stage start
Hot spot >1 trip (DDB 946)	Hot spot first stage trip
Hot spot >2 trip (DDB 947)	Hot spot second stage trip
Hot spot >3 trip (DDB 948)	Hot spot third stage trip
XThermPretrp Alm (DDB 401)	Tol Pretrip Alm
Ambient T	Ambient temperature measurement
Top oil T	Top oil temperature measurement
Hot spot T	Hot spot temperature measurement
TOL Pre-trip left	Pre-trip time left measurement

Table 13: VTS outputs

1.29.3 Operation

The thermal overload protection in the P34x uses the thermal model given by the equations for hot spot and top oil temperatures. A discrete time thermal replica model is implemented and it is described by the equations for $\Delta\Theta_{TOn}$ and $\Delta\Theta_{Hn}$.

If the top oil temperature is not available as a measured input quantity, it is calculated every cycle by the following equation:

$$\Theta_{TO} = \Theta_A + \Delta\Theta_{TO}$$

Where:

Θ_{TO} = Top oil temperature

Θ_A = Ambient temperature

$\Delta\Theta_{TO}$ = Top oil rise over ambient temperature due to a step load change

The ambient temperature can be measured directly or it can be set in the Average Amb T setting. $\Delta\Theta_{TO}$ is given by the following exponential expression containing an oil time constant:

$$\Delta\Theta_{TOn} = \left(\Delta\Theta_{TO,U} - \Delta\Theta_{TO,n-1}\right)\cdot\left(1 - e^{-\left(\frac{\Delta t}{\tau_{TO}}\right)}\right) + \Delta\Theta_{TO,n-1}$$

Where:

$\Delta\Theta_{TO,U}$ = ultimate top oil rise over ambient temperature for load L

$\Delta\Theta_{TO,n-1}$ = the previous top oil rise over ambient temperature

Δ_t = elapsed time between the ultimate top oil rise and the initial top oil rise

τ_{TO} = oil time constant of the transformer for any load L between the ultimate top oil rise and the initial top oil rise. This parameter is set by the user.

By using power series, top oil rise, $\Delta\Theta_{TOn}$, can be approximated as shown below:

$$\Delta\Theta_{TOn} = \left(\Delta\Theta_{TO,U} - \Delta\Theta_{TO,n-1}\right)\cdot\left(\frac{\Delta t}{\tau_{TO}}\right) + \Delta\Theta_{TO,n-1}$$

The ultimate top oil rise is given by the following equation:

$$\Delta\Theta_{TO,U} = \Delta\Theta_{TO,R}\cdot\left[\frac{K_U^2 R + 1}{R + 1}\right]^n$$

Where:

K^u= the ratio of ultimate load L to rated load

R = the ratio of the load loss at rated load to no load loss. This parameter is set by the user.

n = Oil exponent. This parameter is set by the user.

$\Delta\Theta_{TO,R}$ = top oil rise over ambient temperature at rated load. This parameter is set by the user.

The hot spot temperature can only be obtained by calculation. The following equation is used to calculate the hot spot temperature every cycle:

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

Where:

Θ_H = Hot spot (winding) temperature

Θ_{TO} = Top oil temperature

$\Delta\Theta_H$ = Hot spot rise above top oil temperature

The hot spot temperature rise over top oil temperature, $\Delta\Theta_H$, is given by:

$$\Delta\Theta_{Hn} = \left(\Delta\Theta_{H,U} - \Delta\Theta_{H,n-1}\right)\cdot\left(1 - e^{-\left(\frac{\Delta t}{\tau_w}\right)}\right) + \Delta\Theta_{H,n-1}$$

Where:

$\Delta\Theta_{H,U}$ = ultimate hot spot rise over top oil temperature for load L

$\Delta\Theta_{H,n-1}$ = previous hot spot rise over top oil temperature

Δt = elapsed time between the ultimate hot spot rise and the initial hot spot rise. Δt is one cycle.

τ_W = winding time constant at hot spot location. This parameter is set by the user.

By using power series, hot spot temperature rise, $\Delta\Theta_{Hn}$, can be approximated as shown below:

$$\Delta\Theta_{Hn} = \left(\Delta\Theta_{H,U} - \Delta\Theta_{H,n-1}\right)\cdot\left(\frac{\Delta t}{\tau_w}\right) + \Delta\Theta_{H,n-1}$$

The ultimate hot spot rise over top oil is given by:

$$\Delta\Theta_{H,U} = \Delta\Theta_{H,R}\cdot K_U{}^{2m}$$

Where:

$\Delta\Theta_{H,R}$ = winding hottest spot rise over top oil temperature at rated load. This parameter is set by the user.

K_U = the ratio of ultimate load L to rated load

m = winding exponent. This parameter is set by the user.

The load current used in the calculations is the rms value. The rms current is calculated according to the following equation:

$$L_{rms} = \sqrt{\frac{L_1{}^2 + L_2{}^2 + \ldots + L_{24}{}^2}{24}}$$

Where L_n is the sample, there are 24 sample per cycle.

Hot spot temperature, Top oil temperature and ambient temperature are stored in non-volatile memory. These measurements are updated every power cycle. The thermal state can be reset to zero by any of the following:

- The **Reset X Thermal** cell under the **MEASUREMENT 4** heading on the front panel
- A remote communications interface command
- A status input state change.

The top oil temperature, hot spot temperature, ambient temperature and pre-trip time left are available as a measured value in the **Measurement 4** column.

If a more accurate representation of the thermal state of the transformer is required, the use of temperature monitoring devices (RTDs or CLIO) which target specific areas is recommended. Also, for short time overloads the application of RTDs/CLIO and overcurrent protection can provide better protection.

1.30 Loss of life statistics

Deterioration of insulation is a time function of temperature. Since the temperature distribution is not uniform, the part that is operating at the highest temperature undergoes the greatest deterioration. Therefore the hot spot temperature is considered in loss of life statistics. The loss of life model is executed every cycle.

Two one-stage definite time delay alarm based on aging acceleration factor (F_{AA}) or loss of life (LOL) are available.

A reset command is provided to allow the user to reset the calculated parameters: LOL status, LOL aging factor (F_{AA}), mean aging factor ($F_{AA.m}$), rate of loss of life (Rate of LOL), residual life at F_{AAm} (Lres at $F_{AA,m}$), residual life at designed (Lres at designed).

1.30.1 Inputs

Signal name	Description
IA-HV, IB-HV, IC-HV, IA-LV, IB-LV, IC-LV,	Phase current levels (raw samples). The currents required by the thermal overload element are the currents of the winding being monitored.
IA-bias, IB-bias, IC-bias	Bias currents
Θ_H	Calculated hot spot temperature
Reset LOL	Reset loss of life

Table 14: Loss of life inputs

1.30.2 Outputs

Signal name	Description
FAA Alarm	Aging acceleration factor alarm
Loss of Life Alm	Loss of life alarm
LOL status	Accumulated loss of life (LOL) measurement in hrs
Lres at designed	Residual life at reference hottest spot temperature
Rate of LOL	Rate of loss of life (ROLOL) measurement in %
LOL aging factor	Aging acceleration factor (F_{AA}) measurement
FAA,m	Mean aging acceleration factor ($F_{AA,m}$) measurement
Lres at FAA,m	Residual life hours at $F_{AA,m}$ ($L_{res}(F_{AA,m})$) measurement

Table 15: Loss of life outputs

1.30.3 Operation

As indicated in IEEE Std. C57.91-1995 the aging acceleration factor is the rate at which transformer insulation aging for a given hottest spot temperature is accelerated compared with the aging rate at a reference hottest spot temperature. For 65°C average winding rise transformers, the reference hottest spot temperature is 110°C. For 55°C average winding rise transformers, the reference hottest spot temperature is 95°C. For hottest spot temperatures in excess of the reference hottest spot temperature the aging acceleration factor is greater than 1. For hottest spot temperatures lower than the reference hottest spot temperature, the aging acceleration factor is less than 1.

The model used for loss of life statistics is given by the equations for LOL and F_{AA}. LOL is calculated every hour according to the following formula:

$$LOL = L(\Theta_{H,r}) - L_{res}(\Theta_{H,r})$$

Where:

$L(\Theta_{H,r})$ = life hours at reference winding hottest-spot temperature. This parameter is set by the user.

$L_{res}(\Theta_{H,r})$ = residual life hours at reference winding hottest-spot temperature

The aging acceleration factor F_{AA} is calculated every cycle as follows:

$$F_{AA} = \frac{L(\Theta_{H,r})}{L(\Theta_H)} = \frac{e^{\left[A+\frac{B}{\Theta_{H,r}+273}\right]}}{e^{\left[A+\frac{B}{\Theta_H+273}\right]}} = e^{\left[\frac{B}{\Theta_{H,r}+273}-\frac{B}{\Theta_H+273}\right]}$$

If a 65°C average winding rise transformer is considered, the equation for F_{AA} is as follows:

$$F_{AA} = e^{\left[\frac{B}{383}-\frac{B}{\Theta_H+273}\right]}$$

If a 55°C average winding rise transformer is considered, the equation for F_{AA} is as follows:

$$F_{AA} = e^{\left[\frac{B}{368} - \frac{B}{\Theta_H + 273}\right]}$$

Where:

$L(\Theta_H)$ = life hours at winding hottest-spot temperature

Θ_H = hottest-spot temperature as calculated in thermal overload protection

$\Theta_{H,r}$ = hottest-spot temperature at rated load.

B = constant B from life expectancy curve. This parameter is set by the user. IEEE Std. C57.91-1995 recommends a B value of 15000.

The residual life hours at reference hottest-spot temperature is updated every hour as follows:

$$L_{res}(\Theta_{H,r}) = L_{res,p}(\Theta_{H,r}) - \frac{\sum_{i=1}^{3600} F_{AA,i}(\Theta_H)}{3600}$$

Where:

$L_{res,p}(\Theta H,r)$ = residual life hours at reference temperature one hour ago

$F_{AA,i}(\Theta H)$ = Mean aging acceleration factor, as calculated above. It is calculated every second.

The accumulated loss of life (LOL) will be updated in non-volatile memory once per hour. It will be possible to reset and set a new loss of life figure, in the event that a relay is applied in a new location with a pre-aged resident transformer.

The rate of loss of life (ROLOL) in percent per day is given as follows, and it is updated every day:

$$ROLOL = \frac{24}{L(\Theta_{H,r})} \cdot F_{AA,m}(\Theta_H) \cdot 100\%$$

The mean aging acceleration factor, $F_{AA,m}$, is updated per day, and it is given by:

$$F_{AA,m} = \frac{\sum_{n=1}^{N} F_{AAn} \cdot \Delta t_n}{\sum_{n=1}^{N} \Delta t_n} = \frac{\sum_{n=1}^{N} F_{AAn}}{N}$$

Where:

F_{AAn} is calculated every cycle

Δtn = 1cycle

$F_{AA,\,m}$ states the latest one-day statistics of F_{AA}. When the relay is energized for the first time, $F_{AA,\,m}$ default value is 1.

The residual life in hours at $F_{AA,m}$ is updated per day, and it is given by:

$$L_{res}(F_{AA,m}) = \frac{L_{res}(\Theta_{H,r})}{F_{AA,m}}$$

OP

1.31 Through fault monitoring

Through faults are a major cause of transformer damage and failure. Both the insulation and the mechanical effects of fault currents are considered. The through fault current monitoring function in the P34x gives the fault current level, the duration of the faulty condition, the date and time for each through fault. An I^2t calculation based on the recorded time duration and maximum current is performed for each phase. Cumulative stored calculations for each phase are monitored so that the user may schedule the transformer maintenance based on this data. This may also justify possible system enhancement to reduce through fault level.

One stage alarm is available for through-fault monitoring. The alarm is issued if the maximum cumulative I^2t in the three phases exceeds **the TF I^2t> Alarm** setting. A through fault event is recorded if any of the phase currents is bigger than the TF I> Trigger setting. Set **TF I> Trigge**r greater than the overload capability of the transformer. According to IEEE Std. C57.109-1993, values of 3.5 or less times normal base current may result from overloads rather than faults. IEEE Std. C57.91-1995, states that the suggested limit of load for loading above the nameplate of a distribution transformer with 65°C rise is 300% of rated load during short-time loading (0.5 hours or less). On the other hand, the suggested limit of load for loading above the nameplate of a power transformer with 65°C rise is 200% maximum.

OP

To set **TF I^2t> Alarm** consider the recommendations given in IEEE Std. C57.109-1993 for transformers built beginning in the early 1970s. Consult the transformer manufacturer regarding the short circuit withstand capabilities for transformers built prior the early 1970s.

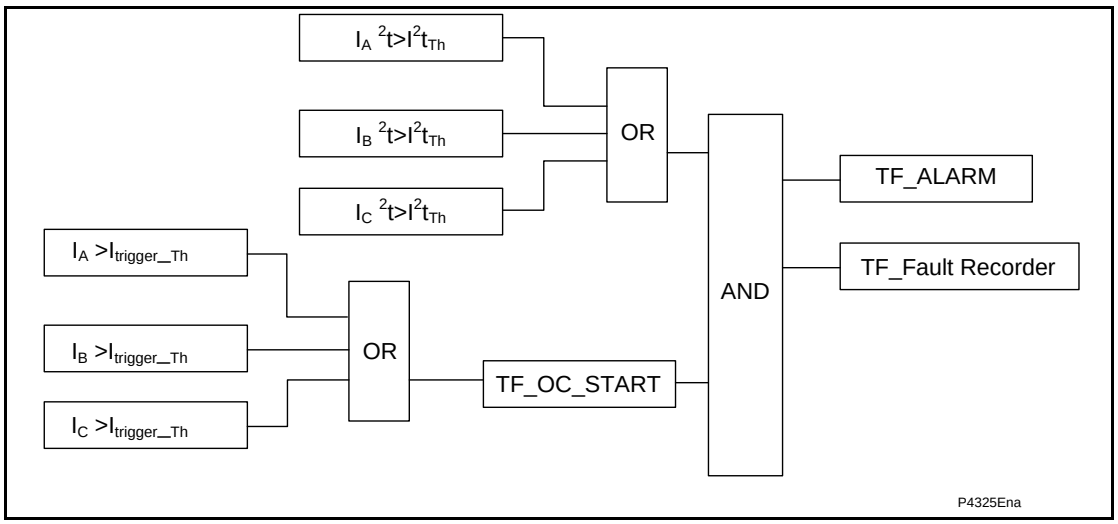


Figure 78: Through fault monitoring logic

1.31.1 Inputs

Signal name	Description
IA-HV, IB-HV, IC-HV or IA-LV, IB-LV, IC-LV	Phase current levels (Fourier magnitudes) of the selected winding

Table 16: Through fault monitoring inputs

1.31.2 Outputs

Signal name	Description
IA peak, IB peak, IC peak	Peak current in the monitor winding in a per phase basis
I2t phase A, I2t phase B, I2t phase C	I2t magnitude in the monitor winding in a per phase basis
Thru fault alarm (DDB399)	Through fault monitoring alarm

Table 17: Through fault monitoring ouputs

IA peak, IB peak, IC peak, I2t phase A, I2t phase B and I2t phase C are given in the VIEW RECORDS menu in the setting file.

1.32 Circuit breaker failure protection (50BF)

The circuit breaker failure protection incorporates two timers, **CB Fail 1 Timer** and **CB Fail 2 Timer**, allowing configuration for the following scenarios:

- Simple CBF, where only **CB Fail 1 Timer** is enabled. For any protection trip, the **CB Fail 1 Timer** is started, and normally reset when the circuit breaker opens to isolate the fault. If breaker opening is not detected, CB Fail 1 Timer times out and closes an output contact assigned to breaker fail (using the programmable scheme logic). This contact is used to backtrip upstream switchgear, generally tripping all infeeds connected to the same busbar section.
- A re-tripping scheme, plus delayed backtripping. Here, **CB Fail 1 Timer** is used to route a trip to a second trip circuit of the same circuit breaker. This requires duplicated circuit breaker trip coils, and is known as re-tripping. Should re-tripping fail to open the circuit breaker, a backtrip may be issued following an additional time delay. The backtrip uses **CB Fail 2 Timer**, which is also started at the instant of the initial protection element trip.

CBF elements **CB Fail 1 Timer** and **CB Fail 2** Timer can be configured to operate for trips triggered by protection elements within the relay or via an external protection trip. The latter is achieved by allocating one of the relay opto-isolated inputs to **External Trip** using the programmable scheme logic.

Resetting of the CBF is possible from a breaker open indication (from the relay's pole dead logic) or from a protection reset. In these cases resetting is only allowed provided the undercurrent elements have also reset. The resetting options are summarized in the following table:

Initiation (menu selectable)	CB fail timer reset mechanism
Current based protection (e.g. 50/51/46/21/87..)	The resetting mechanism is fixed. [IA< operates] & [IB< operates] & [IC< operates] & [IN< operates]
Sensitive earth fault element	The resetting mechanism is fixed. [ISEF< operates]
Non-current based protection (e.g. 27/59/81/32L..)	Three options are available. The user can select from the following options. [All I< and IN< elements operate] [Protection element reset] AND [All I< and IN< elements operate] CB open (all 3 poles) AND [All I< and IN< elements operate]
External protection	Three options are available. The user can select any or all of the options. [All I< and IN< elements operate] [External trip reset] AND [All I< and IN< elements operate] CB open (all 3 poles) AND [All I< and IN< elements operate]

Table 18: CB fail timer reset mechanisms

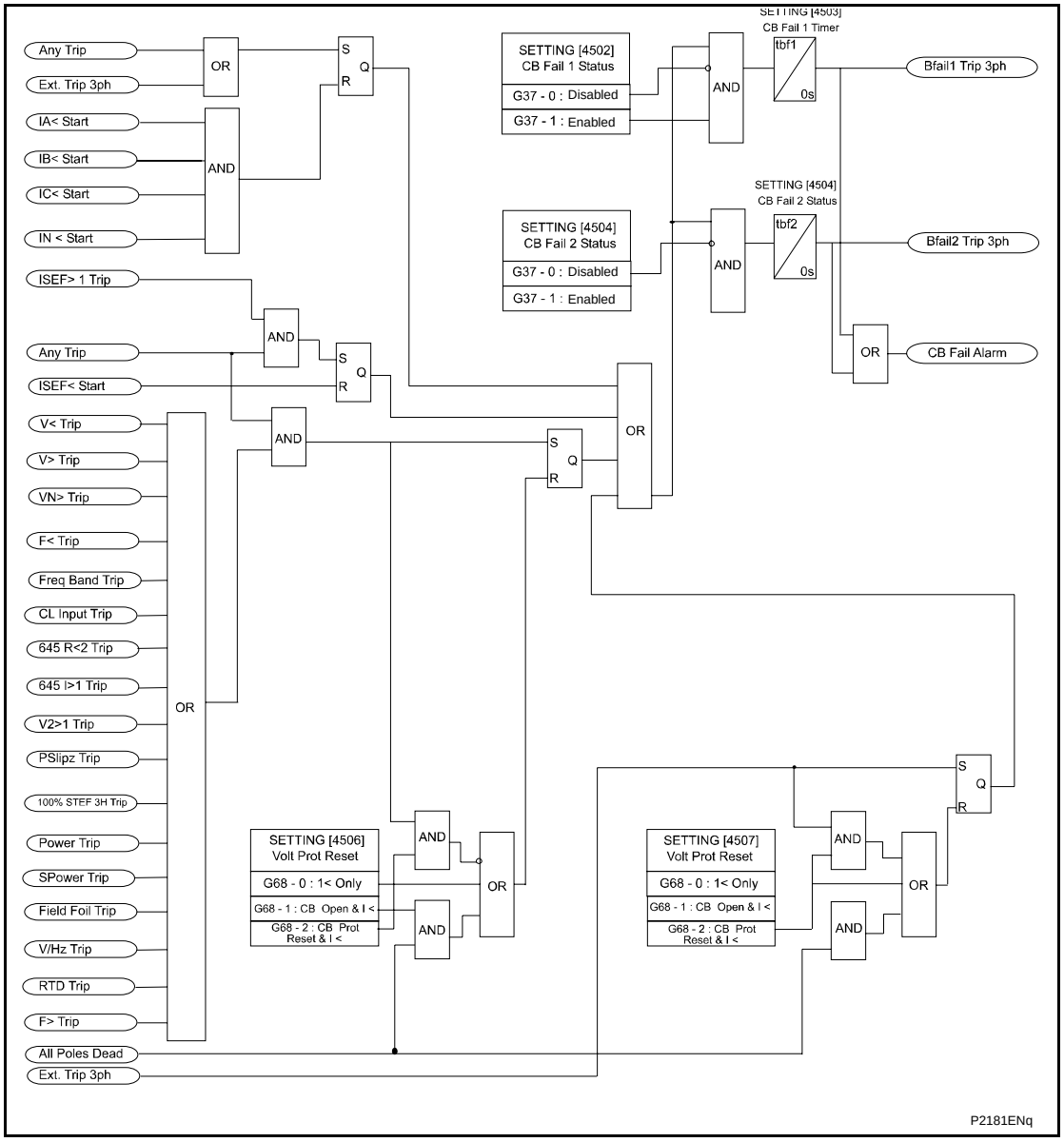


Figure 79: CB fail logic

1.33 Current loop inputs and outputs

1.33.1 Current loop inputs

Four analog (or current loop) inputs are provided for transducers with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA. The analog inputs can be used for various transducers such as vibration monitors, tachometers and pressure transducers. Associated with each input there are two protection stages, one for alarm and one for trip. Each stage can be individually enabled or disabled and each stage has a definite time delay setting.

The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold **Under** or when the input current is above the input value **Over**. The sample interval is nominally 50 ms per input.

The relationship between the transducer measuring range and the current input range is linear. The maximum and minimum settings correspond to the limits of the current input range. This relationship is shown in Figure 80.

Figure 80 also shows the relationship between the measured current and the analog to digital conversion (ADC) count. The hardware design allows for over-ranging, with the maximum ADC count (4095 for a 12-bit ADC) corresponding to 1.0836 mA for the 0 - 1 mA range, and 22.7556 mA for the 0 - 10 mA, 0 - 20 mA and 4 - 20 mA ranges. The relay will

therefore continue to measure and display values beyond the Maximum setting, within its numbering capability (-9999 to 9999).

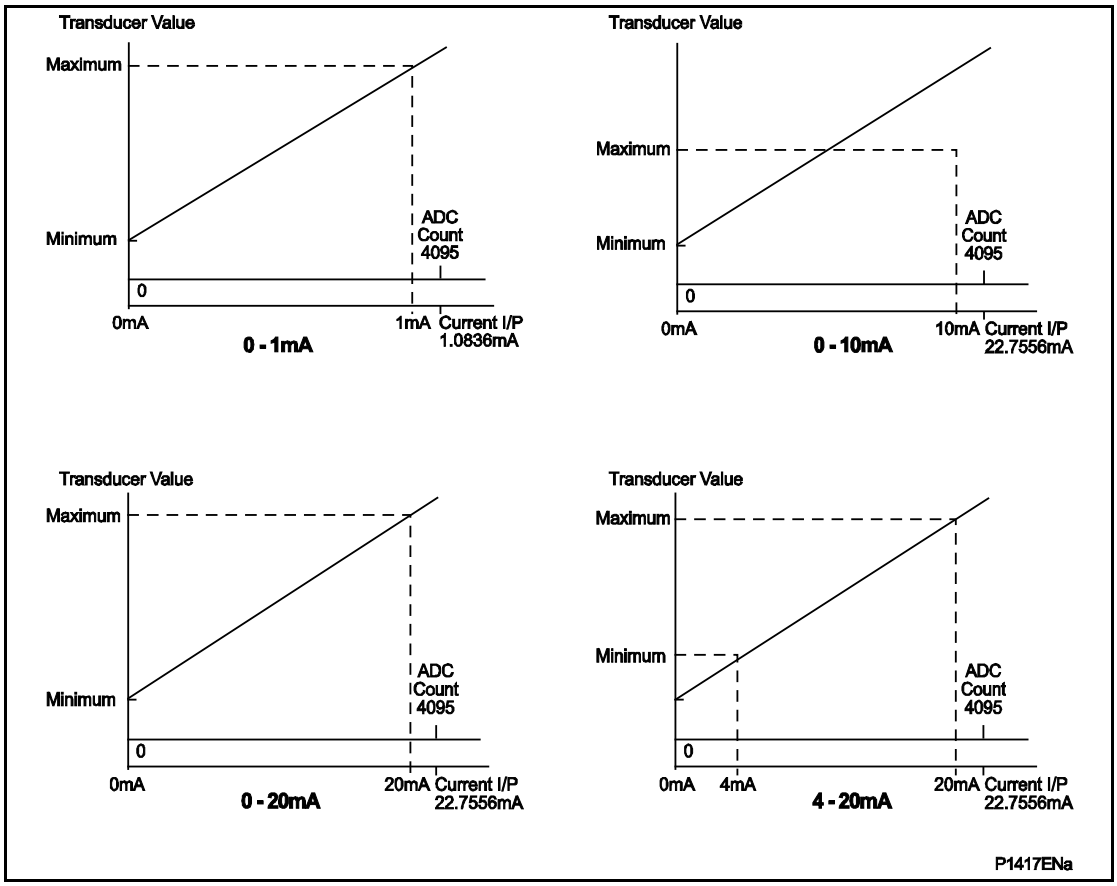


Figure 80: Relationship between the transducer measuring quantity and the current input range

Note: If the Maximum is set less than the Minimum, the slopes of the graphs will be negative. This is because the mathematical relationship remains the same irrespective of how Maximum and Minimum are set, e.g., for 0 - 1 mA range, Maximum always corresponds to 1 mA and Minimum corresponds to 0 mA.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop inputs. When a failure is detected, the protection associated with all the current loop inputs is disabled and a single alarm signal (CL Card I/P Fail, DDB 384) is set and an alarm (CL Card I/P Fail) is raised. A maintenance record with an error code is also recorded with additional details about the type of failure.

For the 4 - 20 mA input range, a current level below 4 mA indicates that there is a fault with the transducer or the wiring. An instantaneous under current alarm element is available, with a setting range from 0 to 4 mA. This element controls an output signal (CLI1/2/3/4 I< Fail Alm., DDB 390-393) which can be mapped to a user defined alarm if required.

Hysteresis is implemented for each protection element. For **Over** protection, the drop-off/pick-up ratio is 95%, for 'Under' protection, the ratio is 105%.

A timer block input is available for each current loop input stage which will reset the CLI timers of the relevant stage if energized, (DDB 656-659). If a current loop input is blocked the protection and alarm timer stages and the 4 - 20 mA undercurrent alarm associated with that input are blocked. The blocking signals may be useful for blocking the current loop inputs when the CB is open for example.

DDB signals are available to indicate starting an operation of the alarm and trip stages of the each current loop inputs, (CLI1/2/3/4 Alarm Start: DDB 1232-1235, CLI1/2/3/4 Trip Start: DDB 1236-1239, CL Input 1/2/3/4 Alarm: DDB 386-389, CLI Input1/2/3/4 Trip: DDB 987-990). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The current loop input starts are mapped internally to the ANY START DDB signal – DDB 992.

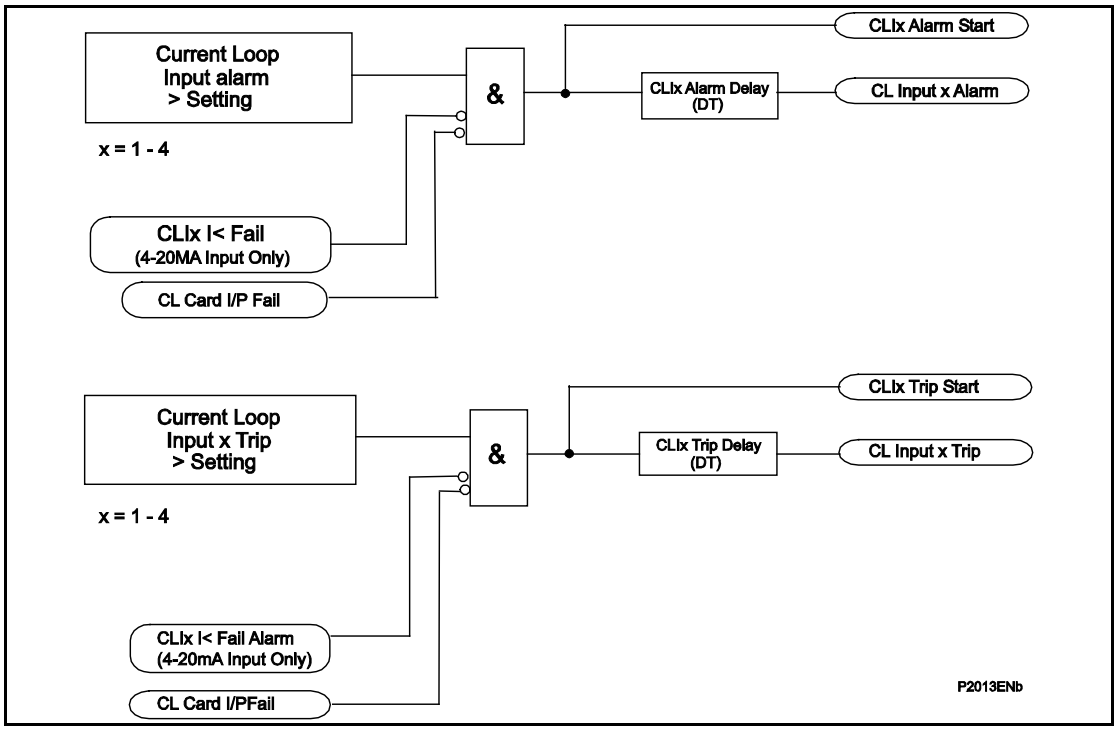


Figure 81: Current loop input logic diagram

1.33.2 Current loop output

Four analog current outputs are provided with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA which can alleviate the need for separate transducers. These may be used to feed standard moving coil ammeters for analog indication of certain measured quantities or into a SCADA using an existing analog RTU.

The CLIO output conversion task runs every 50 ms and the refresh interval for the output measurements is nominally 50 ms. The exceptions are marked with an asterisk in the table of current loop output parameters below. Those exceptional measurements are updated once every second.

The user can set the measuring range for each analog output. The range limits are defined by the Maximum and Minimum settings.

This allows the user to “zoom in” and monitor a restricted range of the measurements with the desired resolution. For voltage, current and power quantities, these settings can be set in either primary or secondary quantities, depending on the **CLO1/2/3/4 Set Values** - **Primary/Secondary** setting associated with each current loop output.

The output current of each analog output is linearly scaled to its range limits, as defined by the Maximum and Minimum settings. The relationship is shown in Figure 82.

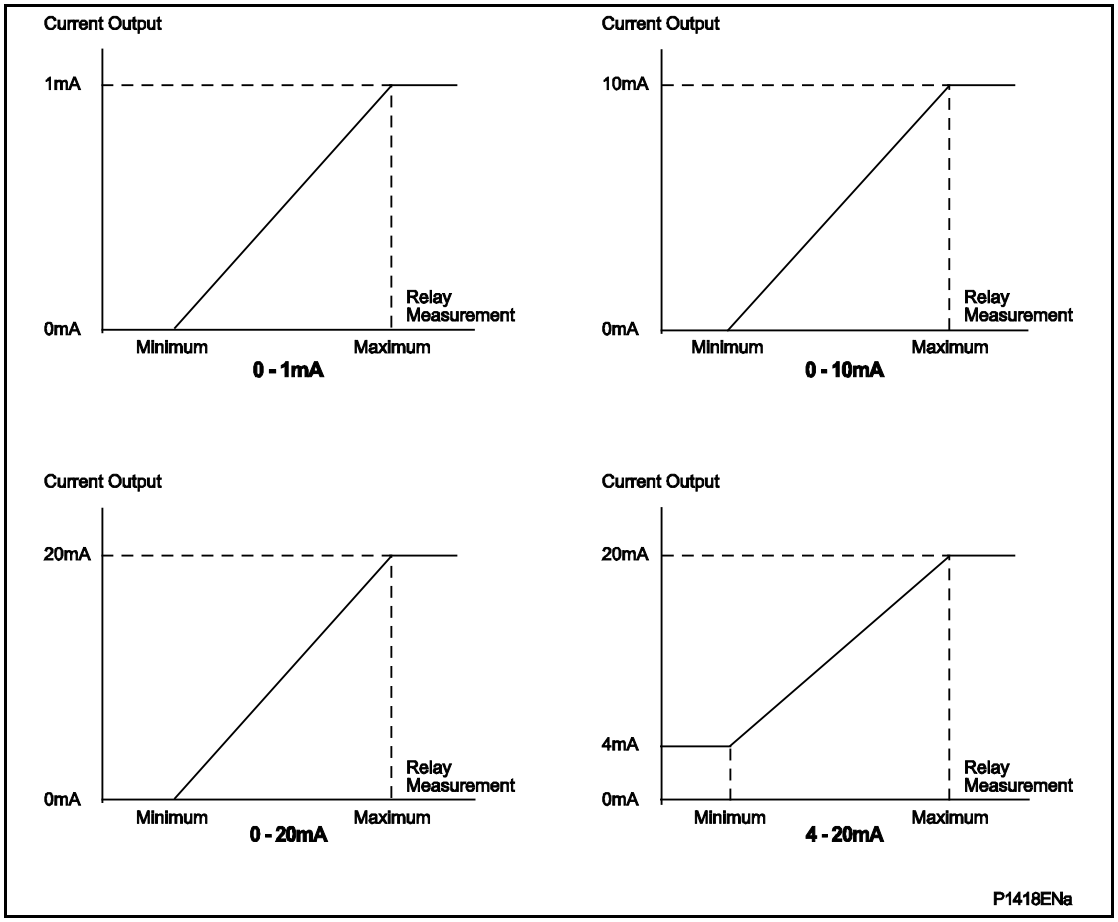


Figure 82: Relationship between the current output and the relay measurement

Note: If the Maximum is set less than the Minimum, the slopes of the graphs will be negative. This is because the mathematical relationship remains the same irrespective of how Maximum and Minimum are set, e.g., for 0 - 1 mA range, Maximum always corresponds to 1 mA and Minimum corresponds to 0 mA.

The P34x transducers are of the current output type. This means that the correct value of output will be maintained over the load range specified. The range of load resistance varies a great deal, depending on the design and the value of output current. Transducers with a full scale output of 10 mA will normally feed any load up to a value of 1000 Ω (compliance voltage of 10 V). This equates to a cable length of 15 km (approximately) for lightweight cable (1/0.6 mm cable). A screened cable earthed at one end only is recommended to reduce interference on the output current signal. The table below gives typical cable impedances/km for common cables. The compliance voltage dictates the maximum load that can be fed by a transducer output. Therefore the 20 mA output will be restricted to a maximum load of 500 Ω approximately.

Cable	1/0.6 mm	1/0.85 mm	1/1.38 mm
CSA (mm2)	**0.28**	**0.57**	**1.50**
R (Ω/km)	**65.52**	**32.65**	**12.38**

Table 19: Cable resistances

The receiving equipment, whether it be a simple moving-coil (DC milli-ammeter) instrument or a remote terminal unit forming part of a SCADA system, can be connected at any point in the output loop and additional equipment can be installed at a later date (provided the compliance voltage is not exceeded) without any need for adjustment of the transducer output.

Where the output current range is used for control purposes, it is sometimes worthwhile to fit appropriately rated diodes, or Zener diodes, across the terminals of each of the units in the series loop to guard against the possibility of their internal circuitry becoming open circuit. In this way, a faulty unit in the loop does not cause all the indications to disappear because the constant current nature of the transducer output simply raises the voltage and continues to force the correct output signal round the loop.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop outputs. When failure is detected, all the current loop output functions are disabled and a single alarm signal (CL Card O/P Fail, DDB 385) is set and an alarm (CL Card O/P Fail) is raised. A maintenance record with an error code is also recorded with additional details about the type of failure.

Current loop output parameters are shown in the following table:

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
Current Magnitude	IA Magnitude (P342-6) IB Magnitude (P342-6) IC Magnitude (P342-6) IN Measured Mag. (P342) IN-1 Measured Mag. (P343/4/5/6) IN-2 Measured Mag. (P343/4/5/6) IA Diff 2H (P343/4/5/6) IB Diff 2H(P343/4/5/6) IC Diff 2H(P343/4/5/6) IA Diff 5H (P343/4/5/6) IB Diff 5H(P343/4/5/6) IC Diff 5H(P343/4/5/6)	A	0 to 16A	0.01A	0A	1.2A
Sensitive Current Input Magnitude	I Sen1 Magnitude (P342-6)	A	0 to 16A	0.01A	0A	1.2A
Phase Sequence Current Components	I1 Magnitude I2 Magnitude I0 Magnitude (P342-6)	A	0 to 16A	0.01A	0A	1.2A
RMS Phase Currents	IA RMS* IB RMS* IC RMS* (P342-6/8)	A	0 to 16A	0.01A	0A	1.2A
P-P Voltage Magnitude	VAB Magnitude VBC Magnitude VCA Magnitude (P342-6)	V	0 to 200 V	0.1 V	0 V	140 V
P-N voltage Magnitude	VAN Magnitude VBN Magnitude VCN Magnitude (P342-6)	V	0 to 200 V	0.1 V	0 V	80 V

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
Neutral Voltage Magnitude	VN1 Measured Mag. (P342-6) VN Derived Mag. VN2 (P342-6) Measured Mag. (P344/5)	V	0 to 200 V	0.1 V	0 V	80 V
3rd Harmonic Neutral Voltage	VN 3rd Harmonic (P343-5)	V	0 to 200 V	0.1 V	0 V	80 V
Phase Sequence Voltage Components	V1 Magnitude* V2 Magnitude* V0 Magnitude* (P342-6)	V	0 to 200 V	0.1 V	0 V	80 V
RMS Phase Voltages	VAN RMS* VBN RMS* VCN RMS* (P342-6/8)	V	0 to 200 V	0.1 V	0 V	80 V
Frequency (Stator Frequency P342-6 and Rotor Frequency P348)	Frequency (P342-6/8)	Hz	0 to 70 Hz	0.01 Hz	45 Hz (P342-6) 0.1 Hz (P348)	65 Hz (P342-6) 10 Hz (P348)
3 Ph Active Power	Three-Phase Watts* (P342-6)	W	-6000 W to 6000 W	1 W	0 W	300 W
3 Ph Reactive Power	Three-Phase VArs* (P342-6)	VAr	-6000 VAr to 6000 VAr	1 VAr	0 VAr	300 VAr
3 Ph Apparent Power	Three-Phase VA* (P342-6)	VA	0 to 6000 VA	1 VA	0 VA	300 VA
3 Ph Power Factor	3Ph Power Factor* (P342-6)	-	-1 to 1	0.01	0	1
Single-Phase Active Power	A Phase Watts* B Phase Watts* C Phase Watts* (P342-6)	W	-2000 W to 2000 W	1 W	0 W	100 W
Single-Phase Reactive Power	A Phase VArs* B Phase VArs* C Phase VArs* (P342-6)	VAr	-2000 VAr to 2000 VAr	1 VAr	0 VAr	100 VAr
Single-Phase Apparent Power	A Phase VA* B Phase VA* C Phase VA* (P342-6)	VA	0 to 2000 VA	1 VA	0 VA	100 VA
Single-Phase Power Factor	APh Power Factor* BPh Power Factor* CPh Power Factor* (P342-6)		-1 to 1	0.01	0	1

OP

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
Three-Phase Current Demands	IA Fixed Demand* IB Fixed Demand* IC Fixed Demand* IA Roll Demand* IB Roll Demand* IC Roll Demand* IA Peak Demand* IB Peak Demand* IC Peak Demand* (P342-6)	A	0 to 16A	0.01A	0A	1.2A
3Ph Active Power Demands	3Ph W Fix Demand* 3Ph W Roll Dem* 3Ph W Peak Dem* (P342-6)	W	-6000 W to 6000 W	1 W	0 W	300 W
3Ph Reactive Power Demands	3Ph VArs Fix Dem* 3Ph VAr Roll Dem* 3Ph VAr Peak Dem* (P342-6)	VAr	-6000 VAr to 6000 VAr	1 VAr	0 VAr	300 VAr
Rotor Thermal State	NPS Thermal (P342-6)	%	0 to 200	0.01	0	120
Stator Thermal State	Thermal Overload (P342-6)	%	0 to 200	0.01	0	120
RTD Temperatures	RTD 1* RTD 2* RTD 3* RTD 4* RTD 5* RTD 6* RTD 7* RTD 8* RTD 9* RTD 10* (P342-6)	°C	-40°C to 300°C	0.1°C	0°C	200°C
Current Loop Inputs	CL Input 1 CL Input 2 CL Input 3 CL input 4 All (P342-6, 8)	-	-9999 to 9999	0.1	0	9999
Flux, V/Hz	Volts/Hz (P342-6)	V/Hz	0-20	0.01	0	4
df/dt	df/dt (P342-6)	Hz/s	-10 to 10 Hz/s	0.01 Hz/s	-1 Hz/s	1 Hz/s
Check Synch Voltages	C/S Voltage Mag C/S Bus Gen-Mag (P342-6)	V	0 to 200 V	0.1 V	0 V	80 V
Slip Frequency	Slip frequency (P342-6)	Hz	0 to 70 Hz	0.01 Hz	-0.5 Hz	0.5 Hz

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
Rotor RMS Phase Currents	IA-1 RMS* IB-1 RMS * IC-1 RMS * (P348)	A	0 to 16A	0.01A	0A	1.2A
Rotor Peak Phase Currents	IA-1 Peak* IB-1 Peak * IC-1 Peak * (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator RMS Phase Currents	IA-2 RMS* IB-2 RMS* IC-2 RMS* (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator RMS Negative Phase Sequence Current	I2 CT2 RMS* (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator Derived RMS Neutral Current	IN-2 Derived RMS* (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator Peak Phase Currents	IA-2 Peak* IB-2 Peak* IC-2 Peak* (P348)	A	0 to 16A	0.01A	0A	1.2A
Stator Peak Negative Phase Sequence Current	I2 CT2 Peak* (P348)	A	0 to 16A	0.01A	0A	1.2A
Rotor RMS Phase Voltages	VA-1 RMS* VB-1 RMS* VC-1 RMS* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Rotor RMS Derived Neutral Voltage	VN-1 Derived RMS* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Rotor Peak Phase Voltages	VA-1 Peak* VB-1 Peak* VC-1 Peak* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Rotor Peak Derived Neutral Voltage	VN-1 Derived Peak* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Rotor RMS Phase-Phase Voltages	VAB-1 RMS* VBC-1 RMS* VCA-1 RMS* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Rotor Peak Phase-Phase Voltages	VAB-1 Peak* VBC-1 Peak* VCA-1 Peak* (P348)	V	0 to 200 V	0.1 V	0 V	80 V

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default max.
Stator Peak Phase Voltages	VA-2 Peak* VB-2 Peak* VC-2Peak* (P348)	V	0 to 200 V	0.1 V	0 V	80 V
Stator Frequency	Frequency 2* (P348)	Hz	0 to 70 Hz	0.01 Hz	45 Hz	65 Hz
A Phase Impedance Magnitude	ZA Mag	Ω	0 to 750 Ω	0.5 Ω	0 Ω	1.2 Ω
Sensitive Single-Phase Active Power	Sen Watts	VAr	-750 W to 750 W	1 W	0 W	37.5 W
Sensitive Single-Phase Reactive Power	Sen VArs	VAr	-750 W to 750 W	1 W	0 W	37.5 W
Sensitive Single-Phase Power Factor	Sen Power Factor	W	-1 to 1	0.01	0	1
Sensitive Current Input 2 Magnitude	I Sen2 Mag (P345)	A	0 to 16A	0.01A	0A	1.2A

Table 20: Current loop output parameters

Note 1: For measurements marked with an asterisk, the internal refresh rate is nominally 1 s, others are 0.5 power system cycle or less.

Note 2: The polarity of Watts, Vars and power factor is affected by the Measurements Mode setting.

Note 3: These settings are for nominal 1A and 100/120 V versions only. For other nominal versions they need to be multiplied accordingly.

Note 4: For the P343/4/5/6, the IA/IB/IC Current magnitudes are IA-1 Magnitude, IB-1 Magnitude, IC-1 Magnitude.

1.34 Rotor earth fault protection (64R)

Rotor earth fault protection is used to detect earth faults in the excitation circuit of synchronous machines. An earth fault in the rotor winding does not cause immediate damage; however, if a second earth fault occurs it constitutes a winding short-circuit of the excitation circuit. The resulting magnetic unbalances can cause extreme mechanical forces which may cause damage to the machine.

The rotor earth resistance is measured using an external low frequency square wave injection, coupling and measurement unit, P391, connected to the rotor circuit. The measurement of the rotor resistance is passed to the P342/3/4/5/6 via a current loop output (0-20 mA) on the P391 connected to one of the 4 current loop inputs (0-20 mA) on the P342/3/4/5/6. The rotor earth fault protection is only available if the relay includes the CLIO hardware option. Two under resistance stages of definite time protection are available for alarm and trip.

1.34.1 Basic Principle

1.34.1.1 Low frequency injection technique

The rotor earth fault protection injects a DC voltage into the rotor circuit; the polarity of the voltage is reversed at low frequencies and the frequency is selectable by the user through a link selection, 0.25 Hz, 0.5 Hz, 1 Hz in the injection, coupling and measurement unit, P391. The voltage source is symmetrically coupled to the excitation circuit via high resistance

resistors. It is also connected to the earthing brush of the rotor via a low resistance measuring shunt. The connection arrangement is a shown in Figure 83.

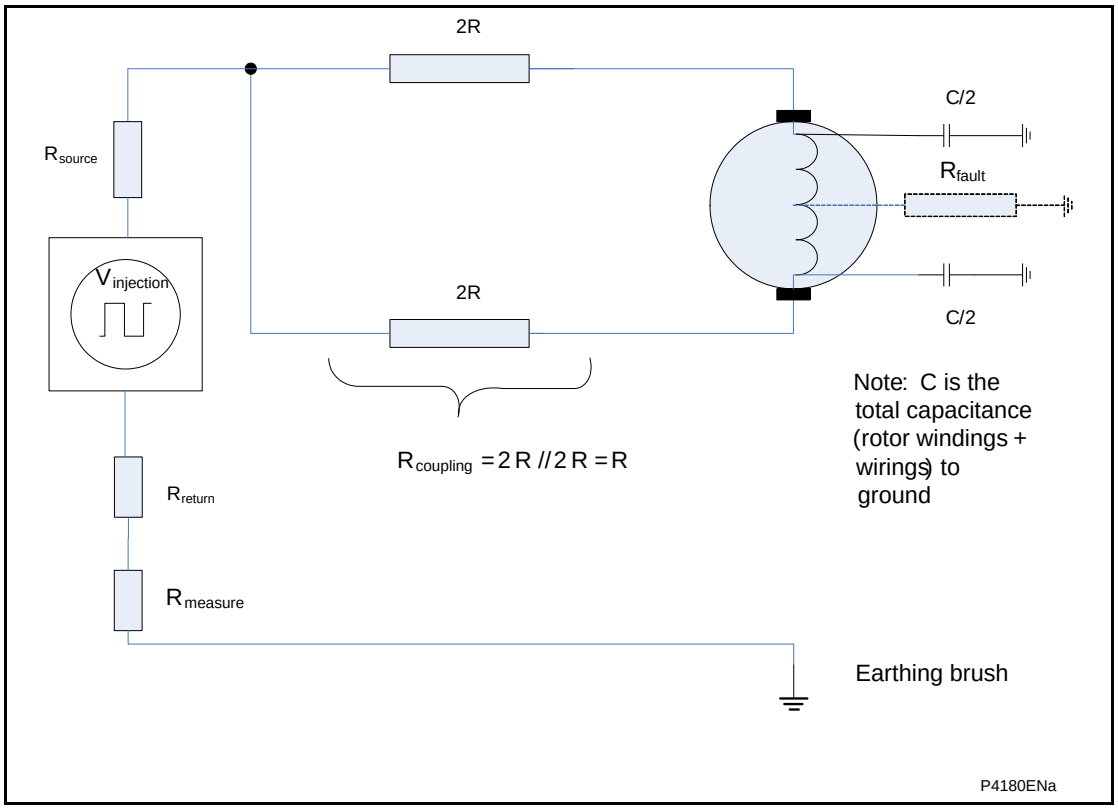


Figure 83: Rotor earth fault protection low frequency injection arrangement

Every time the DC voltage is reversed in polarity, a charging current is applied due to the capacitance of the rotor windings to earth. Under no fault conditions, the charging current should be discharged to zero. If the measurements are made when the current reaches steady state, zero current should be measured indicating that the fault resistance is infinite.

When a rotor earth fault occurs, the steady state current will no longer be zero, the magnitude of which can then be used to calculate the fault resistance. This arrangement is complicated by the fact that, depending on the position of the fault on the excitation winding, the excitation voltage will generate an offset, Ioffset, to the fault current produced, as shown in Figure 84. Therefore the measuring unit measures the steady state current for positive and negative reversal of the injection voltage; calculates the difference between the two and then takes the average. The resultant calculation is equal to the loop current through the equivalent circuit as shown in Figure 85. This eliminates the effect of the capacitance from the excitation windings. It can also achieve a wider fault resistance measuring range compared to the more conventional 50/60 Hz AC injection technique.

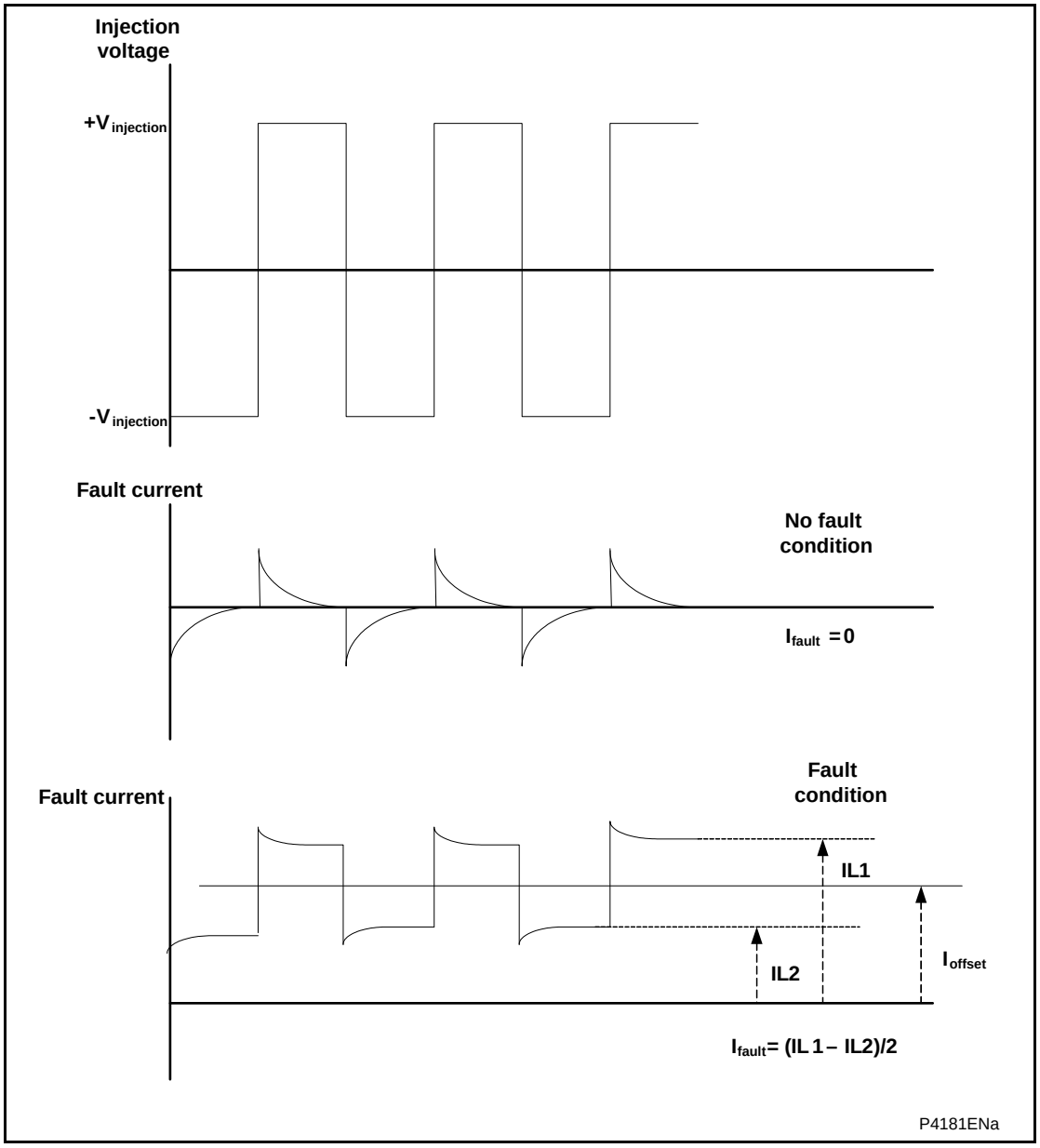


Figure 84: Waveforms for calculating the fault current

Referring to the equivalent circuit in Figure 85, the resistor $R_{measure}$ is used as a shunt for the measurement of the steady-state loop current. By measuring the voltage across the shunt, the loop current can be established, which in turn can be used to calculate the fault resistance.

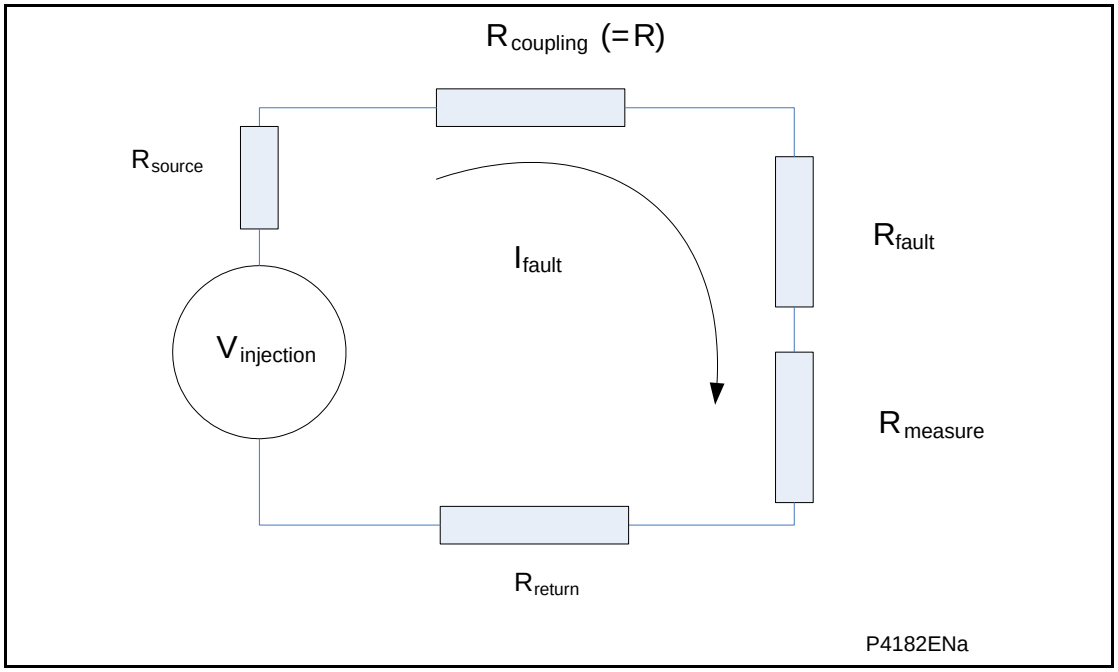


Figure 85: Rotor earth fault equivalent circuit diagram

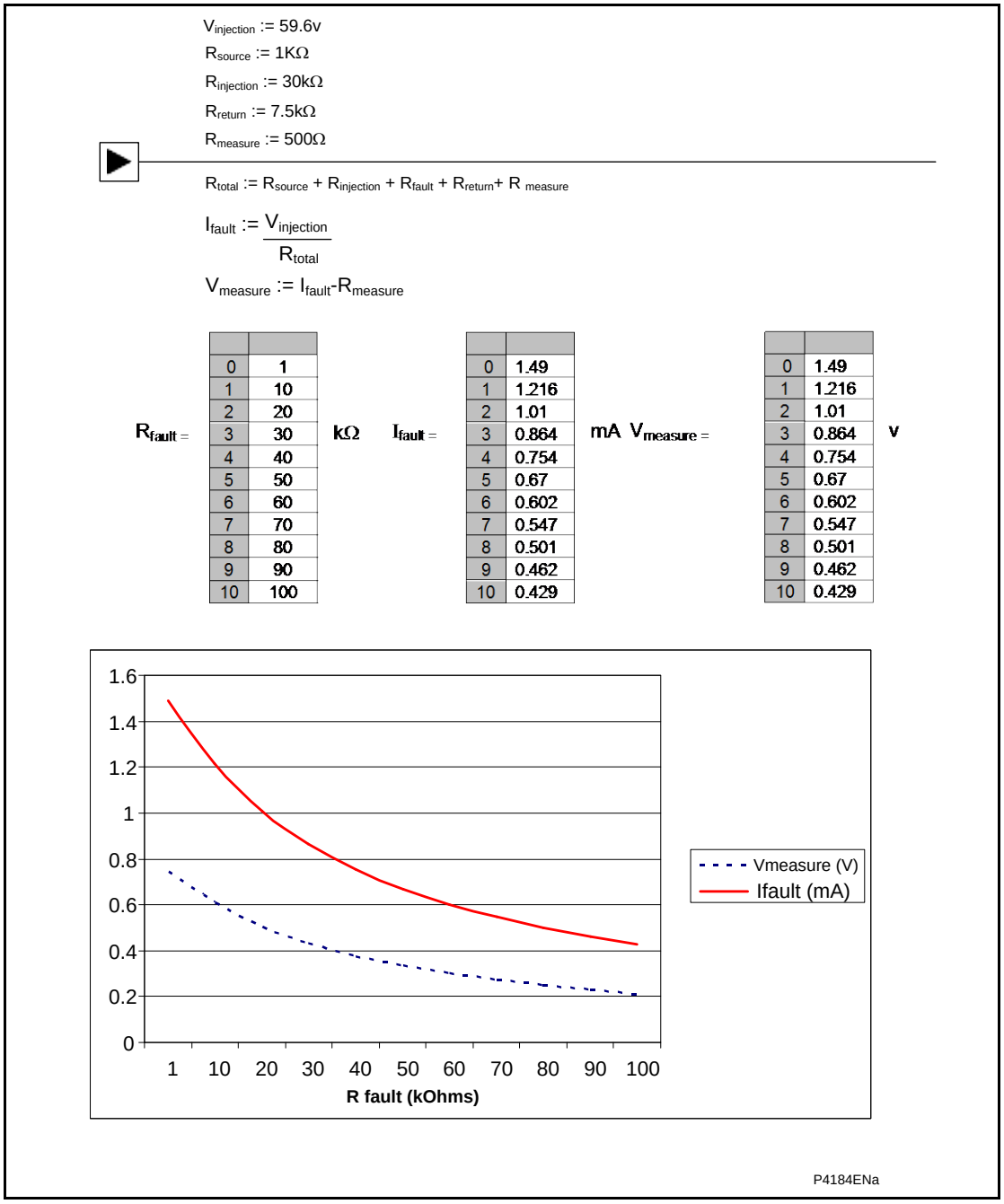
The injection, coupling and the measurement circuitry is implemented as a separate unit, P391, as it is desirable to mount this unit as close as possible to the excitation circuit to minimize any noise pick-up. The communication to the P34x is via a 0-20 mA current loop output on the P391. The voltage drop $V_{measure}$ is passed over as a measuring quantity.

$$V_{measure} = I_{fault} * R_{measure}$$

The P34x calculates the fault resistance, R_{fault}, based on the known configuration of the injection voltage, the coupling resistors, the measuring resistor, plus other resistance values in the measuring circuit (source resistance R_{source} and return path resistance R_{return}).

$$R_{fault} = \frac{V_{injection}}{V_{measure} / R_{measure}} - R_{source} - R_{coupling} - R_{measure} - R_{return}$$

$V_{measure}$ (or Ifault) and R_{fault} have an inverse relationship, as shown in the example in Figure 86. This is handled intrinsically by the P34x calculation.



0	1
1	10
2	20
3	30
4	40
5	50
6	60
7	70
8	80
9	90
10	100

0	1.49
1	1.216
2	1.01
3	0.864
4	0.754
5	0.67
6	0.602
7	0.547
8	0.501
9	0.462
10	0.429

0	1.49
1	1.216
2	1.01
3	0.864
4	0.754
5	0.67
6	0.602
7	0.547
8	0.501
9	0.462
10	0.429

Figure 86: Relationship between fault current and fault resistance

The P391 0-20 mA current loop output has been designed to drive 20 mA through a maximum load of 500Ω. The P34x current loop input resistance is 360 Ω. For redundant rotor earth fault applications a repeater can be used to connect the P391 0-20 mA output to 2 x P34x relays, see Applications Notes for more information on this application.

For 1/0.6 mm lightweight cable (CSA 0.28 mm^2) the cable resistance is 65 Ω/km so for this cable the maximum cable distance between the P391 and P34x can be approx. 1km, (maximum cable length (km) = 140/loop resistance 2Rl = 140/2x65 = 1.07km). It is recommended that a screened cable earthed at one end is used to reduce interference.

1.34.2 Noise filtering

As the injection, coupling and measuring unit performs the I_{fault} (or $V_{measure}$) measurement, it is essential that the filtering capability of the unit is sufficient to reject any noise which could interfere with the measuring process.

For the P34x, it is necessary to ensure that the effect of noise coupled to the current loop input link is minimized to avoid acquisition of erroneous values.

The rate of data update between the injection, coupling and measuring unit and the relay is governed by the injection frequency. Even for the fastest injection frequency of 1 Hz the current loop input is updated only once a second. The sampling interval of the CLIO input is 50 ms (20 Hz sampling rate) therefore there are at least 20 samples for each calculation.

However, the noise immunity is good with a screened cable earthed at one end. There is also a low pass filter with a -3 db cut-off point of 23 Hz installed at the CLIO input.

A count strategy is implemented so as to remove any spikes or sporadic erroneous data acquisition. This supplements the existing security measures consisting of the low pass filter and a properly earthed screen connection. If there is any risk of mal-operation during the start-up and run-down of the generator, for example, then it is recommended that the inhibit signal should be utilized.

The rotor earth fault protection provides a consistency check of two consecutive acquisitions from the CLIO acquisition system before a start decision is made. This will give a delay of around 100 ms (based on the CLIO sampling interval of 50 ms) plus extra time caused by protection scheduling.

1.34.3 Fault Resistance Filtering

To overcome a sudden changes in the fault resistance causing under/overshoot in the input data measurements input filtering is implemented.

When the filter detects an input resistance step change of greater than 5%, the previous CL input and fault resistance values are held (and continue to be produced at the filter's output), until the input data has settled. Two concurrent recovery strategies are implemented:

- Data consistency checking
- Time delay

Data Consistency Checking

To establish if the input data has settled, consistency checking is performed to determine when a certain number of consecutive data samples are consistent, within the required tolerance. This is achieved by recording data samples in a rolling buffer (cyclic buffer), starting when the step change occurs. The number of samples, and thus buffer size, depends on the injection frequency, obtained from the settings (see Table below). The check takes place over a period of $\frac{3}{4f}$. Once enough samples have been captured, the oldest sample is compared with the others. If any differ by more than the required tolerance the oldest sample is rejected and the rolling buffer moves forward when the next sample is obtained. If all the samples are consistent the filter outputs are no longer held and are updated with the 'current' values (effectively the newest value in the sample buffer). The minimum time to achieve consistent data is the time to fill the rolling buffer, for example: at 0.25 Hz the buffer size is 60 samples which takes 3.0 seconds to fill (60 x 50 ms CLIO update time).

Time Delay

A time delay of $\frac{2}{f}$ is waited to allow the inputs to settle (where f is the injection frequency, obtained from the settings). If the $\frac{2}{f}$ delay expires (before the consistency check passes), a 'snapshot' of the 'current' input values is output from the filter, irrespective of the consistency check. When this occurs, the new data values are then held and the timer is immediately restarted. Therefore the consistency check must be passed before consecutive 'current' samples are used, otherwise the timer will expire again and another 'snapshot' of data will be used.

The data is only considered 'settled' when the consistency check is passed. These two strategies complement each other, as the consistency check allows quicker recovery in most circumstances (see Figure 87), while the time delay strategy provides a timeout for the consistency checking, therefore preventing lock up.

When the 'forced' flag input is set, both filter strategies are immediately overridden, as any step change to a forced value is a legitimate change, due to an internal decision, rather than an unwanted overshoot.

The filter parameters for each injection frequency are shown below.

Frequency (Hz)	Hold Timeout $\frac{2}{f}$ (seconds)	Sample buffer size	Time to collect sample buffer size (seconds)
0.25	8	60	3.0
0.5	4	30	1.5
1.0	2	15	0.75

Table 21: Filter parameters for each injection frequency

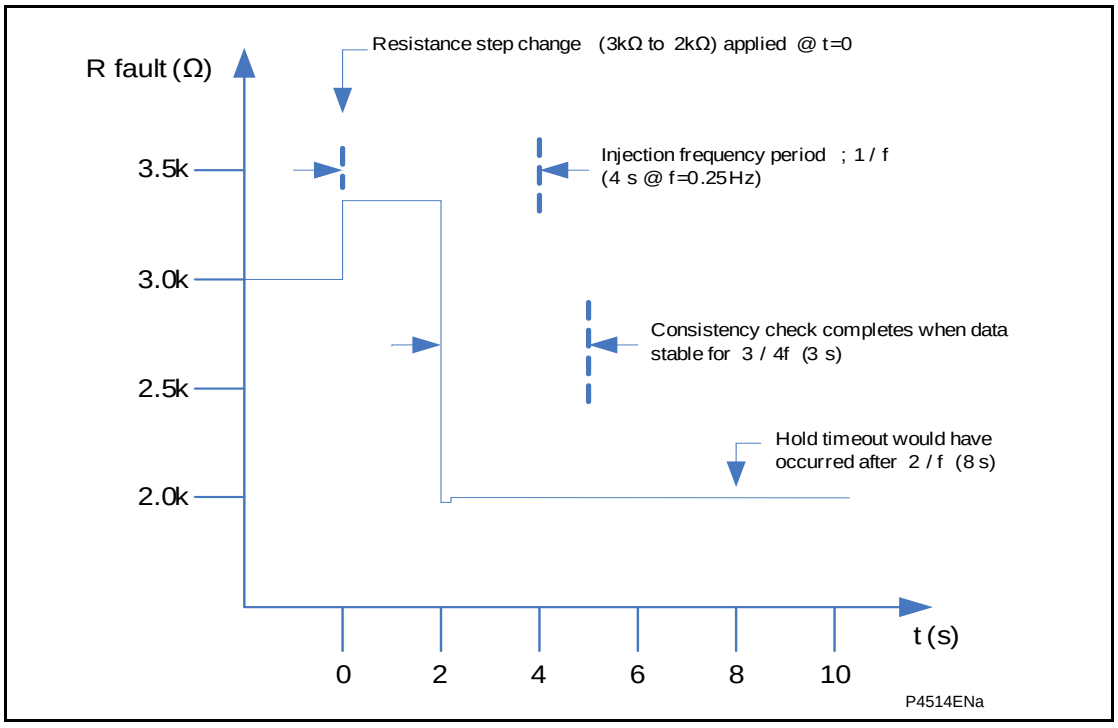


Figure 87: Stability recovery via consistent data @ 0.25 Hz

1.34.4 Description

The rotor earth fault protection uses direct voltage injection, with low frequency polarity reversal as stated above. The low frequency range, 0.25 Hz, 0.5 Hz and 1 Hz, is selected via a link selection inside the injection, coupling and measuring unit P391. This protection is only available if the relay includes the CLIO hardware option.

The method to calculate the fault resistance is based on the equivalent circuit as shown in Figure 85. The injection, coupling and measuring unit measures the voltage across a measuring resistor, as shown in Figure 85. This measured voltage, $V_{measure}$, which is proportional to the fault current, I_{fault}, is passed to the P34x relay through one of the 0-20 mA current loop inputs, selectable by the user.

The coupling resistance, injection voltage, and the measuring resistance values are dependent on the injection, coupling and measurement unit hardware design and are fixed inside the relay. These values are required for the fault resistance calculation. A setting **R Compensation** is included for calibration adjustment during commissioning.

The P34x calculates the fault resistance R_{fault} using the following formula:

$$R_{fault} = \frac{V_{injection}}{V_{measure} / R_{measure}} - R_{source} - R_{coupling} - R_{measure} - R_{return} + R_{Compensation}$$

The rotor earth fault protection includes 2 stages of under resistance protection. The under resistance protection is designed as a two stage protection system, one alarm stage (64R R<1 Alarm) and one trip stage (64R R<2 Trip), with each stage having a definite time delay setting. All the protection stages have separate DDB signals to indicate the start and alarm or trip of each stage and DDB signals to inhibit operation of each stage.

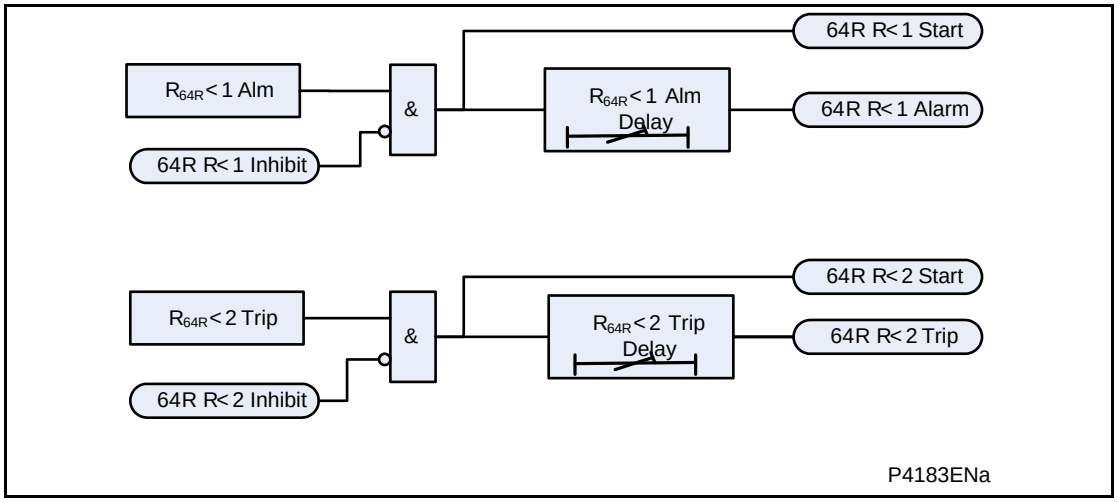


Figure 88: Rotor earth fault protection block diagram

The 64R rotor earth fault 64R R<1/R<2 stages can be independently inhibited by energizing the relevant DDB signal via the PSL (64R R<1/R<2 Inhibit: DDB 556/557). DDB signals are also available to indicate the start, alarm and trip of the protection stages, (64R Start R<1 Alm/64R R<2 Start: DDB 1022/1023, 64R R<1 Alarm: DDB 394, 64R R<2 Trip: DDB 780). A DDB signal is also available to indicate the 64R current loop input failure (64R CL I/P Fail; DDB 395).

The rotor earth fault protection starts are mapped internally to the ANY START DDB signal – DDB 992.

The fault resistance calculation and the protection function is executed twice every power system cycle. Although rotor earth fault is essentially a “slow” protection due to the infrequent update of the input data acquisition, executing the protection twice per cycle provides some improvement to the response time, particularly when the power system frequency is low. A count strategy of 2 is implemented, the start output is asserted only if the fault resistance exceed the threshold for 2 consecutive calculations. A drop-off/pick-up ratio of 105% or 110% (depending on setting) is applied to the settings once the start has operated.

To avoid any overshoot problem when there is a sudden change in fault resistance, an ‘input filter’ is implemented which holds any start/trip and count decisions and measurement values. The ‘hold’ takes place if the resistance value change is greater than 5%. It lasts up to a duration of 2 periods of the injection frequency.

Note: The measurement values in the disturbance records are not filtered.)

An independent CLIO input monitoring element is included to monitor invalid input data from the selected current loop input. Consistent invalid inputs inhibit the protection and cause an alarm (64R CL I/P Fail :DDB 780) to be raised after 1 s.

1.34.5 Measurements

The following are available in the Measurements 3 column:

MEASUREMENTS 3
64R CL Input
64R R Fault

Table 22: Measurements 3

The **64R CL Input** is the 0-20 mA current loop input measured by the relay. This provides monitoring of the current loop signal between the P391 and the P34x. The relay provides a forced value (**CL Input invalid** for the front panel, 0 mA for the remote communications) if the current loop input data is found to be invalid.

The **64R Fault** measurement is the fault resistance calculated by the relay. The relay provides capped values if the fault resistance measurement is beyond the supported range (e.g., 50 ohms to 1M ohms).

The Disturbance recorder analogue input selection includes the **64R CL Input Raw** and **64R R Fault Raw** (unfiltered values) and **64R R Fault** (filtered value) channels. They are sampled at the recorder's sampling frequency, 24 samples/power system cycle.

Forced R_{fault} value	Forced or capped value	Value meaning
9.999 MΩ	Capped	Infinity value (divide by zero prevented).
9.998 MΩ	Forced	CLIO input data invalid
9.997 MΩ	Forced	Rotor EF protection disabled.
9.996 MΩ	Capped	R fault above upper limit (1 MΩ)
0 Ω	Capped	R fault below lower limit (50 Ω).

Table 23: Forced values for 64R

1.35 P348 protection for variable speed machines

1.35.1 Double fed induction machine protection overview

This section describes the operation of the protection functions in a new and innovative protection relay, the P348, for protecting large variable speed Double Fed Induction (DFI) machines for pumped storage plants. The machine's rotor is fed by power electronic converters from the AC system and its speed depends on the frequency of the power fed from the converter. During normal operation the rotor current frequency is very low, during start-up and breaking it varies between zero and rated grid frequency.

For large DFI machines, a standard generator protection relay such as the P345 is not suitable to provide full protection for the rotor and stator therefore the protection scheme must be complemented by a new relay, P348, to mainly provide the rotor protection and stator protection during the start up and run down of the machine.

The new P348 relay has been designed to use Non Conventional Instrument Transformers (NCITs) required to measure a wide range of frequencies in the rotor and stator of DFI machines, 0.1 to 70Hz. The relay includes a process bus IEC61850-9-2 LE port to connect to the NCITs via merging units and primary converters.

The P348 relay includes overcurrent (Peak and RMS) and negative phase sequence overcurrent (RMS) protection for stator protection over the frequency range 0.1 to 70Hz to provide protection during the machine start up, run down and normal running. Stator CT supervision is also provided to supervise the NPS (Negative Phase Sequence) overcurrent protection.

The rotor of a variable speed machine has a 3 phase winding with slip rings supplied with low frequency currents by means of voltage source converters from the AC system. The rotor power supply frequency is generally between 0.1Hz and 6 Hz during normal running and can reach up to the power system frequency (50 or 60 Hz) during machine run-up and run-down.

The P348 includes overcurrent (Peak and RMS), overvoltage (Peak and RMS), neutral voltage (RMS) and overfrequency protection for rotor protection over the frequency range 0.1 to 70Hz to provide protection during the machine start up, run down and normal running. VT supervision using a voltage balance scheme, where redundant rotor VTs are provided, is used to block the rotor neutral voltage protection.

The P348 uses peak protection algorithms using the sampled values directly for overcurrent and overvoltage protection to achieve fast protection. The P348 also uses RMS measurements for overcurrent and overvoltage protection and other protection functions such as NPS overcurrent and neutral voltage protection providing more accurate measurement of the current and voltage signals.

1.35.2 P348 protection relay design for variable speed machines

The main relay development difficulties concerning the rotor protection design are:

- Dynamic frequency variation
- Extremely low frequency
- The effect of the converter power modulation (PWM)

A fundamental change in the P348 relay software from the standard protection models is to replace the frequency tracking with a fixed sampling so that the protection execution rate does not slow down with the tracked rotor frequency, which can be as low as 0.1Hz during normal running. The Fourier algorithms, such as the Discrete Fourier transform (DFT), commonly used in standard protection relays, are unsuitable for this application. This is because the sampling rate must be tuned to track the fundamental frequency before the Fourier methods can correctly calculate the fundamental component and its harmonics. Consequently, the protection algorithms have been redesigned to achieve fast operating times using the sampled values directly for peak protection and improved measurement accuracy using RMS based protection.

As Fourier methods cannot be used, the frequency measurement is based on detecting zero crossings of the current (amps) channels. The measuring channels must therefore be pre-shaped by filtering out unnecessary frequency components before frequency can be measured.

The frequency measurement serves two purposes in the P348:

- To provide rotor overfrequency protection
- To enable RMS calculations

1.35.2.1 Relay sampling rate

The P348 sampling rate is fixed at 1200Hz (equivalent to 24 samples per cycle for 50Hz and 20 samples per cycle for 60Hz).

24 samples per cycle is the current sampling rate of other P34x relays, on which the P348 is based. The sampling rate is not changed in the P348 to reduce processor bandwidth stress and to maintain compatibility with the existing P34x architecture and algorithms which use 24 samples/cycle.

The IEC61850-9-2 LE standard specifies 80 samples/cycle and so the P348 downsamples to 24 samples/cycle. Using 80 samples/cycle and downsampling to 24 sample/cycle does not adversely affect protection operation or measurement accuracy.

Testing has shown the performance in terms of accuracy and protection operating times between standard protection relays with conventional current and voltage transformer inputs and the relays with IEC 61850-9-2 LE inputs is comparable.

1.35.2.2 IEC 61850-9-2 LE anti-alias filter

The analogue channels require an anti-alias filter designed to prevent frequency aliasing for frequencies greater than half the sampling frequency or folding frequency. Since this filtering requirement must be realised prior to the re-sampling process of the IEC 61850-9-2 LE card, a front-end anti-alias filter is implemented in the IEC 61850-9-2 LE card.

The pass band cut-off frequency (500Hz) selected for the P348 anti-alias filter is suitable for the variable speed machine requirement for measuring the frequency components in the PWM waveforms.

1.35.3 Low pass filter and frequency measurement technique

The P348 is operational over a frequency range of 0.1 to 70Hz. The frequency measurement is based on detecting zero crossings of the current channels. The measuring channels therefore must be pre-shaped by filtering out frequency components above a certain threshold before frequency can be measured.

The frequency measurement serves two purposes in the P348:

(i) for providing rotor overfrequency protection and

(ii) for sizing the RMS calculation window.

The group delay of the low pass filters do not form a part of the operate time of any Peak or RMS based protection stage, as both techniques will directly work with the sampled signals, as opposed to after being processed by the filters.

1.35.3.1 Low pass filters

Two low pass filters (LPF) are implemented in the P348.

LPF1, with a pass band frequency of 70Hz, is used for measuring the stator frequency at all times and for measuring the rotor frequency during machine running up and running down. LPF1 is used for removing high frequency noise, mainly PWM frequency and its harmonics from the frequency measurement channel. It also attenuates the 2nd harmonic of the power frequency that may be present in both the stator and rotor currents during fault conditions.

LPF2, with a pass band frequency of 20Hz (this should be the maximum possible rotor slip frequency plus some margin), is used for measuring the rotor frequency during machine normal running. LPF2 is used to remove any frequency components above the maximum rotor frequency during normal running, especially nominal system frequency of 50Hz or 60Hz, which may be present in the rotor currents during some stator faults.

LPF1 or LPF2 will be used for measuring the rotor frequency depending on the state of the **Machine Start** DDB (671).

1.35.3.2 Frequency measuring state machine

The rotor and stator frequencies are measured from the IA-1/IB-1/IC-1 (rotor) and IA-2/ IB-2/IC-2 (stator) filtered current signals. The minimum channel magnitude is 5% of In, below which the channel is disregarded.

On start up, the P348 will search for a suitable channel for measuring the frequency, in the priority order of IA, IB and IC. In the ‘searching’ state, every sampled value of the three phase currents will be checked to see if its absolute value is larger than the minimum magnitude. The highest priority channel will qualify for the measuring source if a sampled value magnitude of that channel is large enough, enabling a transition to the ‘measuring’ state.

Once a channel has been selected as the measuring source, the P348 will only consider another channel if the peak value of the last half cycle of the measuring source channel is below the minimum magnitude, in which case the P348 will transition to the ‘searching’ state from the ‘measuring’ state. During the ‘searching’ state, the ‘Freq Not Found’ DDB 1295 will be set to TRUE, which will block any RMS protection stages and the overfrequency protection.

When the rotor frequency is above 70Hz the ‘Freq High’ DDB 1293 will be set to TRUE, which will block any rotor RMS protection stages and the rotor overfrequency protection. When the rotor frequency is below the **RMS F< Block** threshold in the **System Config** menu the ‘Freq Low’ DDB 1294 will be set to TRUE, which will block any rotor RMS protection stages and the rotor overfrequency protection.

When the stator frequency is above 70Hz the 'Freq2 High' DDB 1315 will be set to TRUE, which will block any stator RMS protection stages. When the stator frequency is below 0.1Hz the 'Freq2 Low' DDB 1316 will be set to TRUE, which will block any stator RMS protection stages.

The frequency measurement is executed in every sample.

1.35.3.3 Peak based protection

The phase overcurrent protection and overvoltage protection provide Peak protection stages using the sampled values directly. To improve the protection stability, a count strategy is applied to all Peak protection stages, where the stage timer does not start until the protection criteria are satisfied for n consecutive protection iterations (the peak stages execute a protection iteration (cycle) every two samples). The count target n is settable for each protection stage using the **SV Iterations** setting.

To ensure fast protection operate times fixed sampling is used and all Peak stages are executed in every protection iteration. The protection task is scheduled to operate every second sample, or every 1.667ms.

From the same point on wave (POW) the operating quantity (i.e. voltage or current) will take longer to reach its peak or a set point at a lower frequency than a higher frequency, as shown by the tF time in Figure 89. The protection operate time will include the t_F into the overall operate time. When the system frequency is around 50Hz, t_F is small but can be much longer for low frequencies as illustrated in Figure 89.

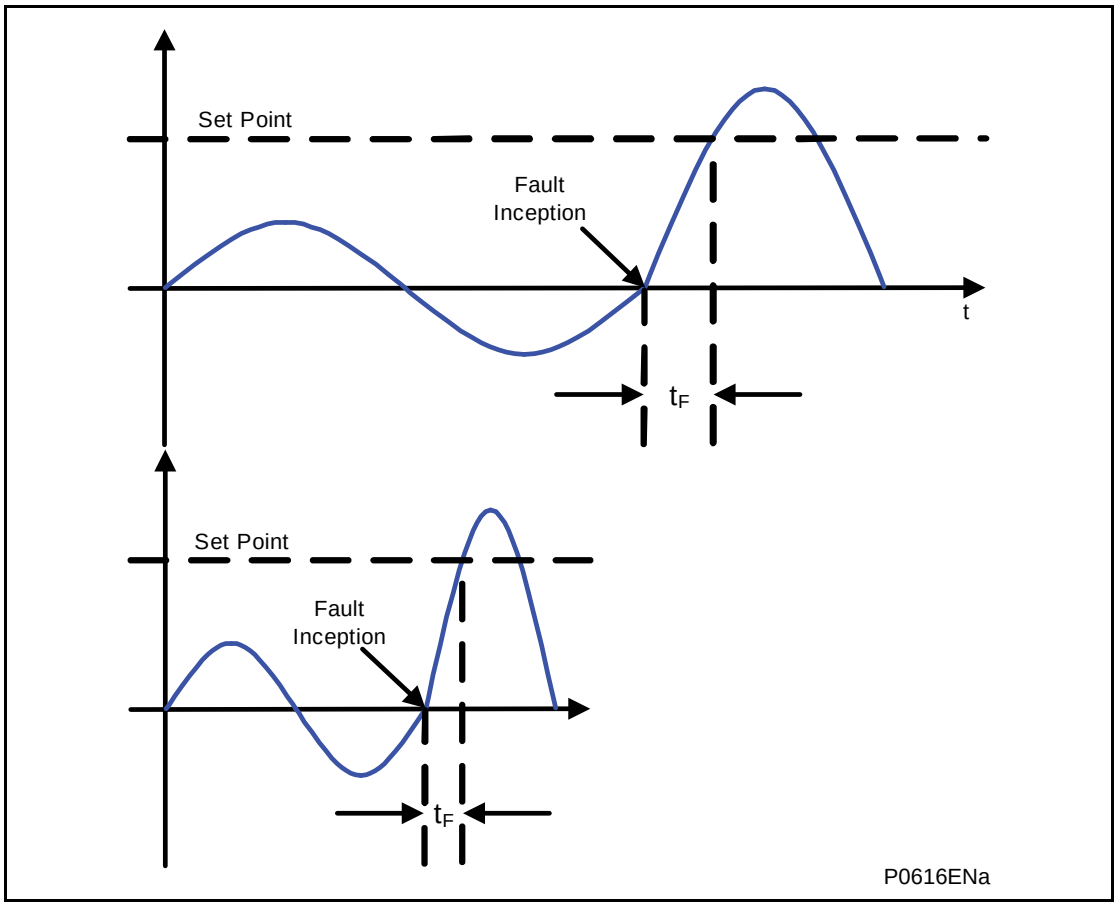


Figure 89: Time taken for the fault current to build up after fault inception at different frequencies

1.35.4 Current and voltage sensor requirements

Current and voltage sensors (NCCT and NCVT) are required for this application to measure high fault currents (e.g. up to 170kA) and medium voltage levels (e.g. up to 12kV) in the frequency range of 0.1Hz to 70Hz. Conventional electromagnetic CTs and VTs are incapable of accurately measuring very low frequency signals. Therefore, non-conventional current and voltage sensors are required to provide these measurements.

For current measurement Rogowski CTs (NCCTs), can be used:

For voltage measurement a resistive voltage divider (NCVT) can be used.

The NCITs output can be converted to a digital signal (PCBUS protocol) by a primary converter unit (PC12 for current and PC14 for voltage) for the Rogowski CT (e.g. Rogoflex CT) and resistive voltage divider sensors. The PC12 and PC14 units can be connected to a merging unit (XMU800) which provides an IEC 61850-9-2 LE digital output. This can then be connected to the P348 IEC 61850-9-2 LE port.

1.35.4.1 NCIT evaluation

The Rogowski CT is an inherent ac sensor, which experiences phase shifts and attenuation when the frequency approaches dc.

The PC12 high pass filter, used with Rogowski CTs, produces a significant phase shift for frequencies <0.1Hz. Despite the phase shift at lower frequencies, when a fault occurs, the fault is observed on the phases almost instantly because the fault has a high di/dt so it is seen as a higher frequency component.

The NCIT resistive voltage divider measurement sensor chain does not produce any significant phase shifts. The phase advance caused by a Rogowski sensor measurement chain with respect to the voltage sensor chain will have no significant effect on the protection, since the P348 protection algorithms such as overcurrent and overvoltage are based on magnitude only and do not use combinations of the current, voltage and the angle between them, e.g. as with power, impedance and directional overcurrent protection.

The performance of the Rogowski sensor chain at lower frequencies is not a problem for the protection performance as although an increased phase advance of 30 degrees is observed at 0.1 Hz, this reduces to a small value at frequencies >1Hz and is negligible when there is a fault. Also, the actual attenuation is less than 0.5 dB at 0.1Hz and considering that a 2 or 3 phase fault current is several per units higher than nominal, an attenuation of 0.5 dB is not significant.

So, Rogowski CTs can be used for this application.

1.35.5 IEC 61850-9-2 LE quality flags and state machine logic

The P348 provides 12 9-2LE input channels: IA-1, IB-1, IC-1 for rotor currents, IA-2, IB-2, IC-2 for stator currents, VA-1, VB-1, VC-1 for rotor voltages and VA-2, VB-2, VC-2 for rotor voltages from a second (duplicated) acquisition chain for voltage sensor supervision purposes only. The relay provides a number of measurement values from these channels.

- The RMS values of IA-1/IB-1/IC-1
- The RMS values of IA-2/IB-2/IC-2
- The RMS values of VA-1/VB-1/VC-1
- The RMS of NVD derived from three phase voltage inputs VA-1/VB-1/VC-1
- The RMS of NPS current derived from IA-2/IB-2/IC-2 inputs
- IA-1/IB-1/IC-1 peak values over the last second
- IA-2/IB-2/IC-2 peak values over the last second
- VA-1/VB-1/VC-1 peak values over the last second
- VA-2/VB-2/VC-2 peak values over the last second

- The peak value over the last second of NVD derived from three phase voltage inputs VA-1/VB-1/VC-1
- The peak value of NPS current derived from IA-2/IB-2/IC-2 inputs
- Frequency 1 (rotor frequency)
- Frequency 2 (stator frequency)

The 9-2LE sample values carry quality flags for each channel. Only the quality flags of the corresponding input channels will affect the function.

The quality flag attached to a 9-2 sample of an analogue input can have three states 'Good', 'Invalid' or 'Questionable'. The Px40 platform software will treat the 'Questionable' state as either 'Good' or 'Invalid' depending on the **Trust Ques Data** setting. The state machine, in the product code, will only see two states of the quality flag 'Good', or 'Invalid'.

There can be up to three states, Normal, Hold and Inhibit, in a state machine, as shown in Table 24.

State	Behaviour
Normal	The function will work as normal.
Hold	The function execution will in effect be bypassed but all internal variables and states will be held for as long as this state lasts. Upon transition to the 'Normal' state, the function will be able to resume.
Inhibit	The function will be reset and inhibited.

Table 24: Behaviours of the state machine

The state machine will start with the 'Normal' state. As soon as the quality flag of a channel's sample is detected as 'Invalid', the state machine of an affected function will transition to the 'Hold' state. If the state machine has been in the 'Hold' state for a specified period of time T_{Hold}, it will transition to the 'Inhibit' state. When the state machine is in either the 'Hold' or the 'Inhibit' state, it will transition to the 'normal' state if all affecting channels have been in a 'Good' state for a specified period of time T_{Good}. The T_{Hold} (48 samples) and T_{Good} (24 samples) are the same for all protection functions.

The frequency measuring module also handles the quality flags. If the quality flag of the frequency measuring channel is detected as 'Invalid', the frequency measuring module will switch to the next available channel. If all the three current channels are marked as 'Invalid', the frequency measurement will be suspended and the 'Freq Not Found' DDB set to TRUE. The frequency measurement will resume once the quality flag has been 'Good' for four zero crossings on any of the three phase currents. The same principle applies to both rotor and stator. See section 1.35.3.2 for more details on the frequency measuring.

1.35.6 Overcurrent protection (50/51S, 50/51R)

The overcurrent protection included in the P348 relay provides four stages of non-directional three-phase RMS and four stages of non-directional three-phase peak (Sampled Values) overcurrent protection with independent definite time delay characteristics. Each peak overcurrent stage has a **SV Iterations** setting for the number of protection iterations required above setting to start. The iteration counter resets to zero for any sample value whose absolute value falls below the drop off threshold. The Start signal is set to high when the iteration count target is reached.

Each rotor RMS overcurrent stage is blocked when the frequency is below the **RMS F< Block** threshold in the **System Config** menu and the 'Freq Low' DDB 1293 is operated. Each stator RMS overcurrent stage is blocked when the frequency is below 0.1Hz and the 'Freq2 Low' DDB 1316 is operated. The rotor RMS protection stages are blocked if any of the DDBs 'Freq Not Found' DDB 1295, 'Freq High' DDB 1293 or 'Freq Low' DDB 1294 are TRUE. The stator RMS protection stages are blocked if any of the DDBs 'Freq2 Not Found' DDB 1317, 'Freq2 High' DDB 1315 or 'Freq2 Low' DDB 1316 are TRUE.

Each Peak and RMS overcurrent stage has a **I>x CT Source** setting used to select the 3 phase current inputs used by the peak overcurrent protection - **IA-1/IB-1/IC-1** (the rotor) or **IA-2/IB-2/IC-2** (the stator) CT inputs.

The first two stages of the RMS overcurrent protection have time-delayed characteristics which are selectable between inverse definite minimum time (IDMT), or definite time (DT) or a user curve (Default Curve 1/2/3/4). The third and fourth RMS overcurrent stages have definite time characteristics only. The four peak overcurrent stages have definite time characteristics only.

Various methods are available to achieve correct relay co-ordination on a system; by means of time alone, current alone or a combination of both time and current. Grading by means of current is only possible where there is an appreciable difference in fault level between the two relay locations on the stator side of the machine. Grading by time is used by some utilities but can often lead to excessive fault clearance times at or near source substations where the fault level is highest. For these reasons the most commonly applied characteristic in coordinating stator overcurrent relays is the IDMT type.

The inverse time delayed characteristics indicated above, comply with the following formula:

IEC curves

$$t = T \times \left(\frac{\beta}{(M^{\alpha} - 1)} + L \right)$$

or IEEE curves

$$t = TD \times \left(\frac{\beta}{(M^{\alpha} - 1)} + L \right)$$

where:

t = Operation time

β = Constant

M = I/Is

K = Constant

I = Measured current

Is = Current threshold setting

α = Constant

L = ANSI/IEEE constant (zero for IEC curves)

T = Time multiplier setting for IEC curves

TD = Time dial setting for IEEE curves

Curve Description	Standard	β constant	α constant	L constant
Standard Inverse	IEC	0.14	0.02	0
Very Inverse	IEC	13.5	1	0
Extremely Inverse	IEC	80	2	0
Long Time Inverse	UK	120	1	0
Rectifier	UK	45900	5.6	0
Moderately Inverse	IEEE	0.0515	0.02	0.114
Very Inverse	IEEE	19.61	2	0.491
Extremely Inverse	IEEE	28.2	2	0.1217
Inverse	US	5.95	2	0.18
Short Time Inverse	US	0.16758	0.02	0.11858

Table 25: Inverse time curves

Note 1: The IEEE and US curves are set differently to the IEC/UK curves with regard to the time setting. A time multiplier setting (TMS) is used to adjust the operating time of the IEC curves and user programmable curves, whereas a time dial setting is employed for the IEEE/US curves. The menu is arranged such that if an IEC/UK/user programmable curve is selected, the **I> Time Dial** cell is not visible and vice versa for the TMS setting.

Note 2: The IEC/UK inverse characteristics can be used with a definite time reset characteristic, however, the IEEE/US curves may have an inverse or definite time reset characteristic. The following equation can used to calculate the inverse reset time for IEEE/US curves:

$$tRESET = \frac{TD \times S}{(1 - M^2)} \text{ in seconds}$$

Where:

TD = Time dial setting for IEEE curves

S = Constant

M = I/Is

Curve Description	Standard	S constant
Moderately Inverse	IEEE	4.85
Very Inverse	IEEE	21.6
Extremely Inverse	IEEE	29.1
Inverse	US	5.95
Short Time Inverse	US	2.261

Table 26: Reset curves

As well as the standard curves as defined by various countries and standardising bodies, it is possible to program up to four custom curves, **Default Curve 1/2/3/4**, using General Electric's User Programmable Curve Tool, described in the MiCOM S1 Agile Setting Application Software User Guide. This is a user-friendly tool by which users can create curves either by formula or by entering data points. Programmable curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves.

1.35.6.1 Timer hold facility

Each RMS overcurrent stage in the P348 relay includes a timer hold facility, which may either be set to zero or to a definite time value. Setting of the timer to zero means that the overcurrent timer for that stage will reset instantaneously once the current falls below 95% of the current setting. Setting of the hold timer to a value other than zero, delays the resetting of the protection element start and timer signals for this period. When the reset time of the overcurrent relay is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the relay will integrate the fault current pulses, thereby reducing fault clearance time. The timer hold facility can be found for all RMS overcurrent stages as settings **I>5/6/7/8 tRESET**.

Each peak overcurrent stage in the P348 relay includes a timer hold facility, which may either be set to zero or to a definite time value. The timer hold facility can be found for all peak overcurrent stages as settings **I>1/2/3/4 tRESET**.

An issue to be considered with the peak overcurrent based protection is that the relay contact can chatter and a large number of event records can be generated for a sinusoidal waveform.

Consider a sinusoidal fault current as shown in Figure 98. The Start signal of an overcurrent protection stage will repeatedly pick up and drop off with the fluctuation of the sample values of the fault current. The peak overcurrent trip signal and the relay contact will follow the same pattern if the stage is set to instantaneous trip. This problem is referred to as 'chattering'. An event record is generated every time the Start or the Trip signal changes state, therefore a large amount of events will be generated by chattering, especially when the signal frequency is high (e.g. 50Hz).

One way of preventing chattering is to set a drop off or reset delay. Each peak overcurrent stage of the P348 has a definite time **I>x tReset setting**. In the standard P342-6 overcurrent protection, the **I>x tReset** setting is referred to as a timer hold facility, which holds the trip timer for the set period after the operating quantity falls below overcurrent drop-off threshold. The P348 extends the **I>x tReset** setting use for the peak overcurrent protection to not only holding the trip timer but also the Start and Trip signals after the operating quantity falls below the overcurrent drop-off threshold to prevent an avalanche of events.

The **I>x tReset** setting should be set to a value larger than half the cycle period of the lowest frequency considered, which is the longest possible 'toff' in Figure 90. Thus, the Start or Trip signal will not reset until the fault has been cleared.

The existing timer hold application used by the RMS overcurrent protection is not changed from the standard P342-6 overcurrent protection, which is designed to allow faster or more reliable tripping for intermittent faults, where multiple fault pulses are integrated towards the set trip delay. Its application, however, is slightly different for the peak overcurrent stages in the P348, in which even a permanent fault will appear intermittent. As a result, for any protection stage with a time-delayed trip, the **I>x tReset** setting should be set to a value larger than half the cycle period of the lowest frequency considered, otherwise the peak overcurrent protection set with a time delay may never trip.

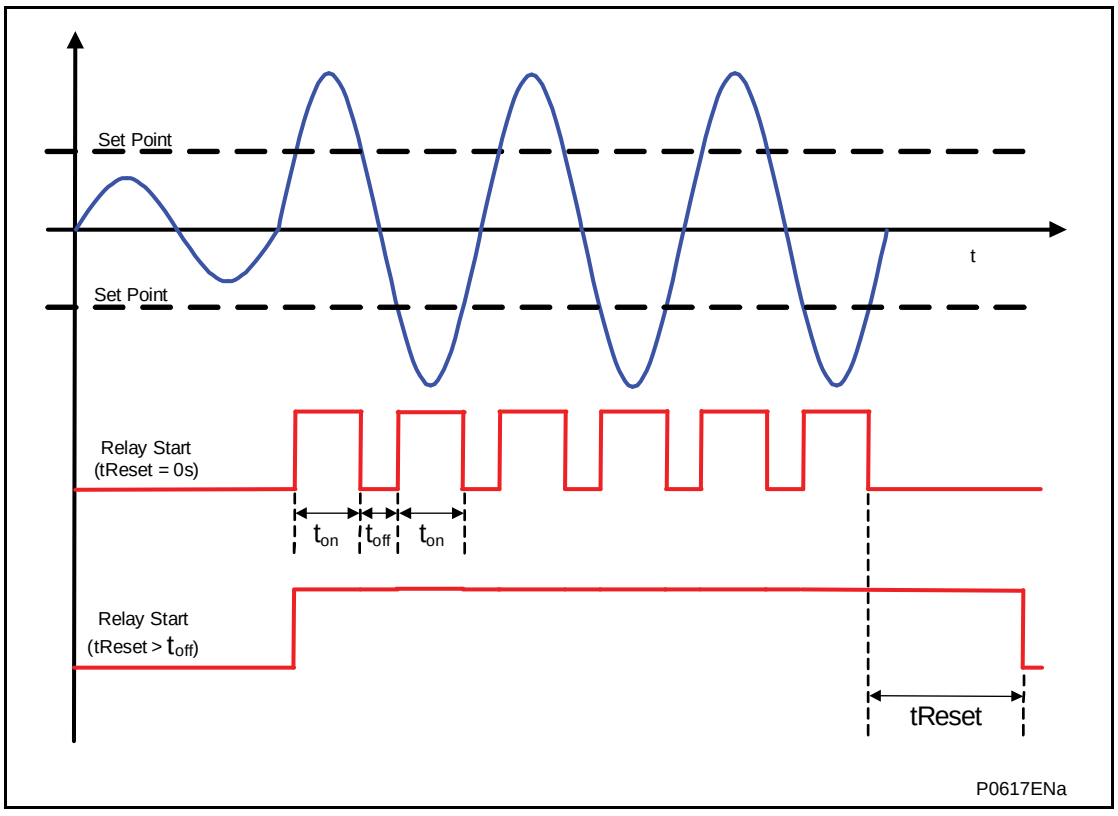


Figure 90: Effect of tReset Setting

1.35.6.2 Logic

The functional logic diagram for the non-directional RMS and Peak overcurrent is shown in Figure 91 and Figure 92.

All Peak and RMS overcurrent stages can be blocked by energizing the inhibit DDB signals via the PSL (I>1/2/3/4 Peak Inhibit: DDB 568-571 and I>5/6/7/8 RMS Inhibit: DDB 572-575). The rotor RMS protection stages are blocked if any of the DDBs 'Freq Not Found' DDB 1295, 'Freq High' DDB 1293 or 'Freq Low' DDB 1294 are TRUE. The stator RMS protection stages are blocked if any of the DDBs 'Freq2 Not Found' DDB 1317, 'Freq2 High' DDB 1315 or 'Freq2 Low' DDB 1316 are TRUE.

DDB signals are also available to indicate the start and trip of each phase of each stage of protection, (Peak Starts: DDB 1024-1039, RMS Starts 1040-1055, Peak Trips: DDB 784-799, RMS Trips 800-815). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Overcurrent protection starts 1/2/3/4 are mapped internally to the ANY START DDB signal – DDB 992.

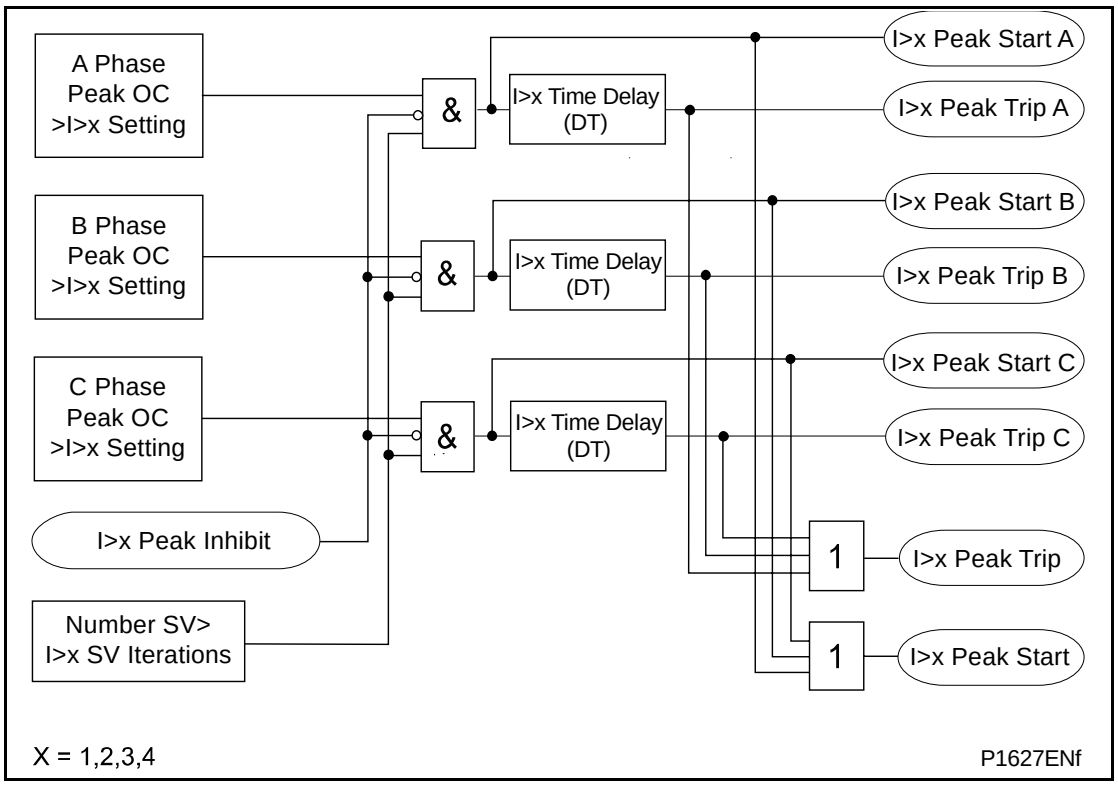


Figure 91: Non-directional peak overcurrent logic diagram

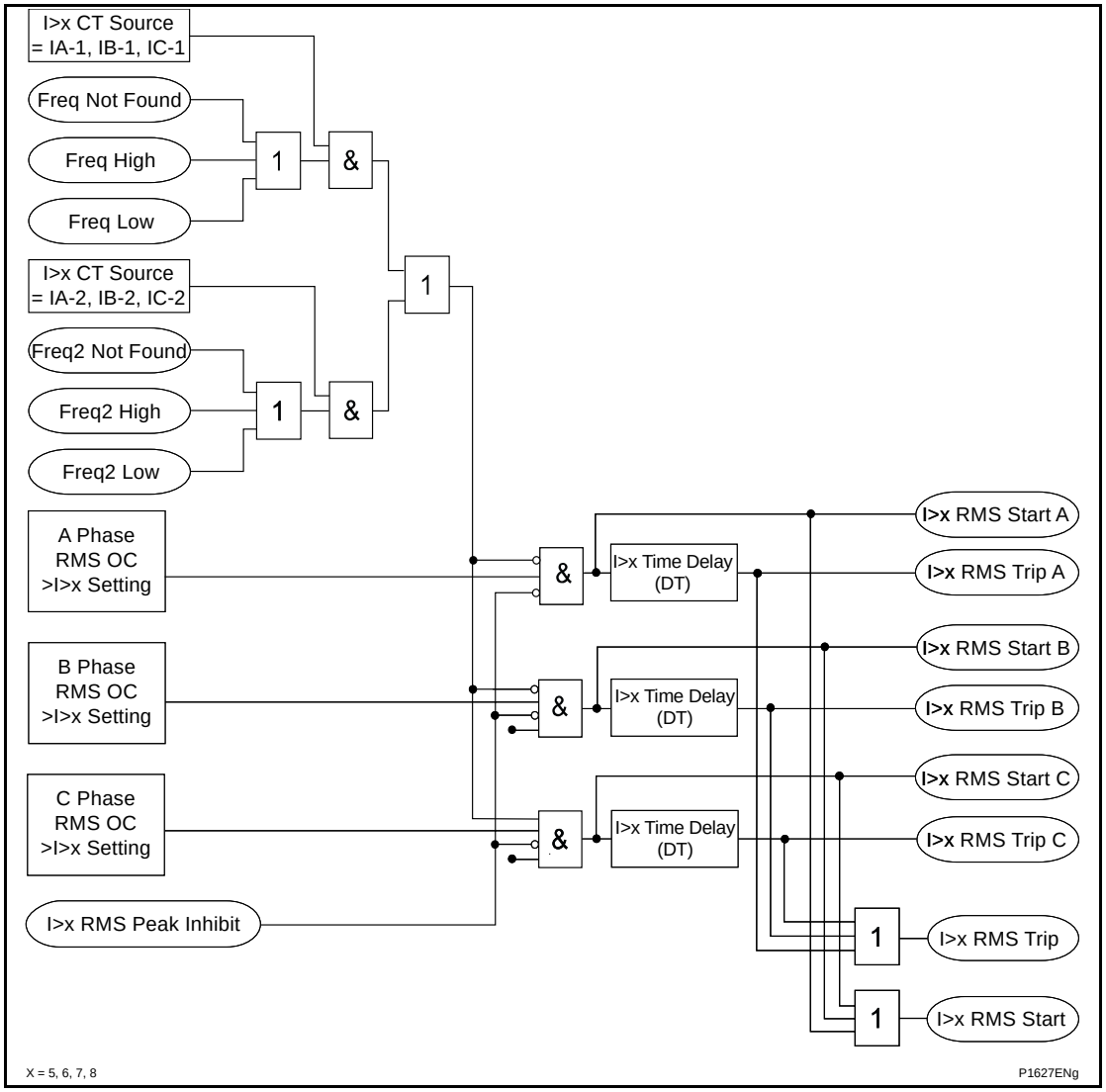


Figure 92: Non-directional RMS overcurrent logic diagram

1.35.7 Negative sequence overcurrent protection (NPS) (46S)

The P348 relays provide four non directional independent stages of RMS negative phase sequence overcurrent protection. Each stage has a current pick up setting **I2>1/2/3/4 Current Set**, and is time delayed in operation by the adjustable timer **I2>1/2/3/4 Time Delay**. The 3 phase current source is fixed to using the **IA-2/IB-2/IC-2** inputs on the stator.

All 4 stages can be blocked by energizing the inhibit DDB signal via the PSL (I2>1/2/3/4 Inhibit: DDB 587-590). All stages are also blocked by the stator CT supervision, CTS-2 Block DDB 1264.

The stator RMS protection stages are blocked if any of the DDBs 'Freq2 Not Found' DDB 1317, 'Freq2 High' DDB 1315 or 'Freq2 Low' DDB 1316 are TRUE.

DDB signals are also available to indicate the start and trip of each stage of protection, (Starts: DDB 1064-1067, Trips: DDB 824-827). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Negative sequence overcurrent protection starts 1/2/3/4 are mapped internally to the ANY START DDB signal - DDB 992.

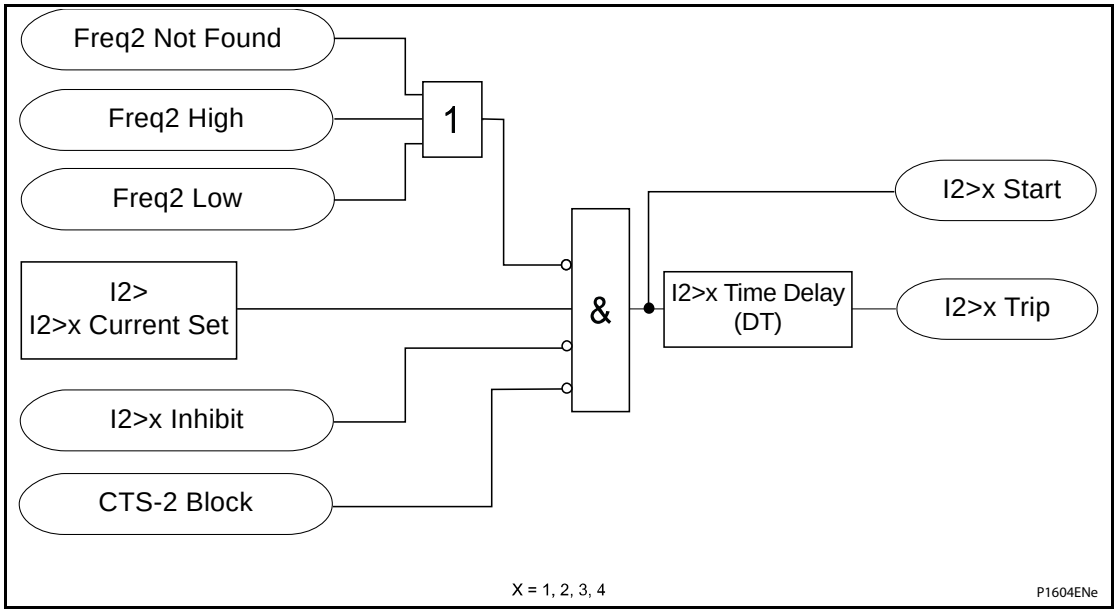


Figure 93: Negative sequence overcurrent operation

1.35.8 Overvoltage protection (59R)

The rotor overvoltage protection included within the P348 relay consists of two independent stages of RMS and two independent stages of peak (sampled values) overvoltage protection. Each peak overvoltage stage has a **SV Iterations** setting for the number of protection iterations required above setting to start. The iteration counter resets to zero for any sample value whose absolute value falls below the drop off threshold. The Start signal is set to high when the iteration count target is reached. The 3 phase voltage source is fixed to using the **VA-1/VB-1/VC-1** inputs on the rotor.

Each rotor RMS overvoltage stage is blocked when the frequency is below the **RMS F< Block** threshold in the **System Config** menu and the 'Freq Low' DDB 1293 is operated. The rotor RMS protection stages are blocked if any of the DDBs 'Freq Not Found' DDB 1295, 'Freq High' DDB 1293 or 'Freq Low' DDB 1294 are TRUE.

The overvoltage protection included within the P348 relays consists of two independent stages configurable as either phase to phase or phase to neutral measuring within the **V>Measur't mode** cell.

Note: If the overvoltage protection is set for phase-phase operation then the DDB signals V>x Peak/RMS Start/Trip A/AB, V>x Peak/RMS Start/Trip B/BC, V>x Peak/RMS Start/Trip C/CA refer to V>x peak/RMS Start/Trip AB and V>x Peak/RMS Start/Trip BC and V>x Peak/RMS Start/Trip CA. If set for phase-neutral then the DDB signals V>x Peak/RMS Start/Trip A/AB, V>x peak/RMS Start/Trip B/BC, V>x Peak/RMS Start/Trip C/CA refer to V>x Peak/RMS Start/Trip A and V>x Peak/RMS Start/Trip B and V>x Peak/RMS Start/Trip C.

The peak overvoltage stages 1 and 2 are DT only and are enabled/disabled in the **V>1/2 status cell**.

The RMS overvoltage stage 1 may be selected as **IDMT**, **Default Curve 1/2/3/4**, **DT** or **Disabled**, within the **V>3 Function** cell. Stage 2 is DT only and is **Enabled/Disabled** in the **V>4 status** cell.

The IDMT characteristic available on the first stage is defined by the following formula:

$t = K/(M - 1)$

Where:

K = Time multiplier setting

t = Operating time in seconds

M = Measured voltage/relay setting voltage (V> Voltage Set)

As well as the standard curves, it is possible to program up to four custom curves **Default Curve 1/2/3/4** using General Electric's User Programmable Curve Tool, described in the MiCOM S1 Agile Setting Application Software User Guide. This is a user-friendly tool by which users can create curves either by formula or by entering data points. Programmable curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves.

Each peak overvoltage stage in the P348 relay includes a timer hold facility, which may either be set to zero or to a definite time value. The timer hold facility can be found for all peak overvoltage stages as settings **V>1/2 tRESET**. The P348 **V>1/2 tRESET** setting holds the trip timer and also the Start and Trip signals after the operating quantity falls below overvoltage drop-off threshold to prevent an avalanche of events similar to that of the peak overcurrent described previously.

All peak and RMS overvoltage stages can be blocked by energizing the inhibit DDB signals via the PSL (V>1/2 Peak Inhibit: DDB 604, 605, V>3/4 RMS Inhibit: DDB 606, 607). The rotor RMS protection stages are blocked if any of the DDBs ‘Freq Not Found’ DDB 1295, ‘Freq High’ DDB 1293 or ‘Freq Low’ DDB 1294 are TRUE.

DDB signals are also available to indicate a three-phase and per phase start and trip, (Peak Starts: DDB 1094-1101, RMS Starts: DDB 1111-1118, Peak Trips: DDB 838-845, RMS Trips: DDB 855-862). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Overvoltage protection starts are mapped internally to the ANY START DDB signal – DDB 992.

The logic diagrams of the peak and RMS overvoltage function is shown in Figure 94 and Figure 95.

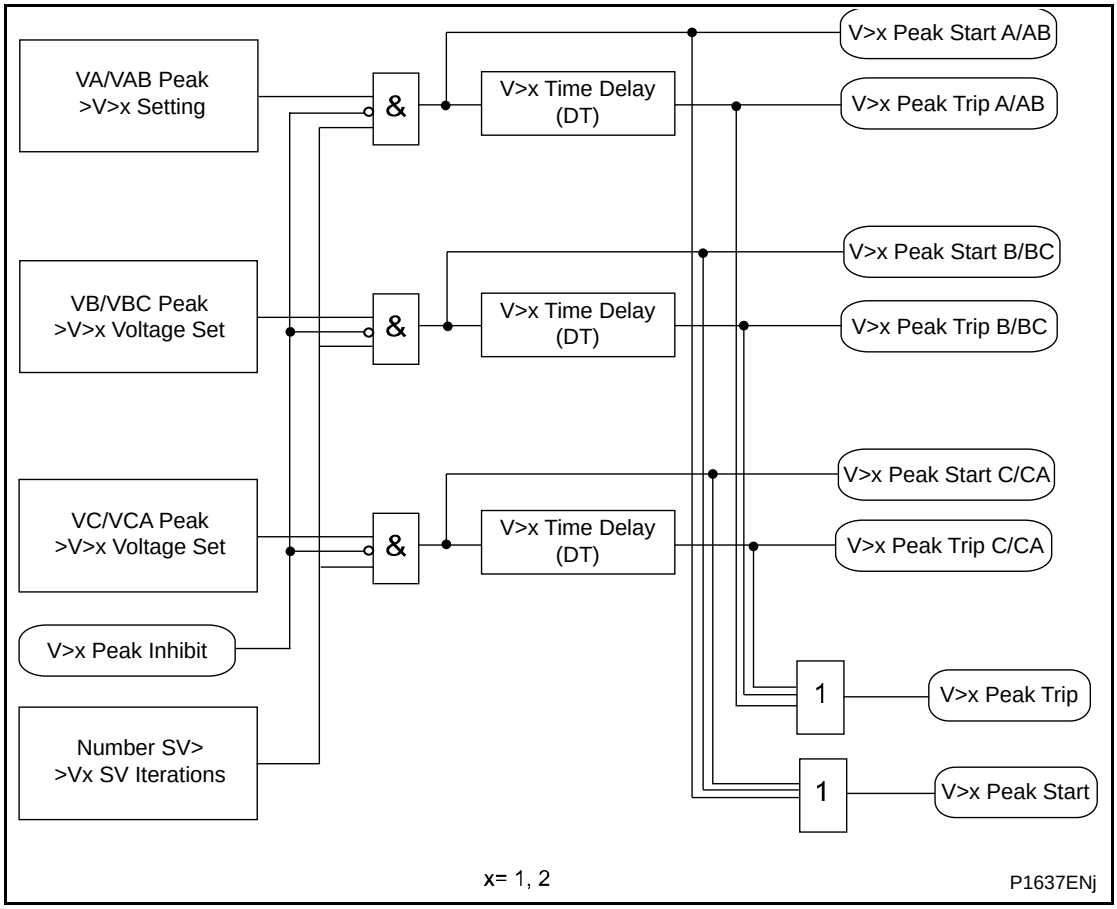


Figure 94: Peak overvoltage - single and three phase tripping mode (single stage)

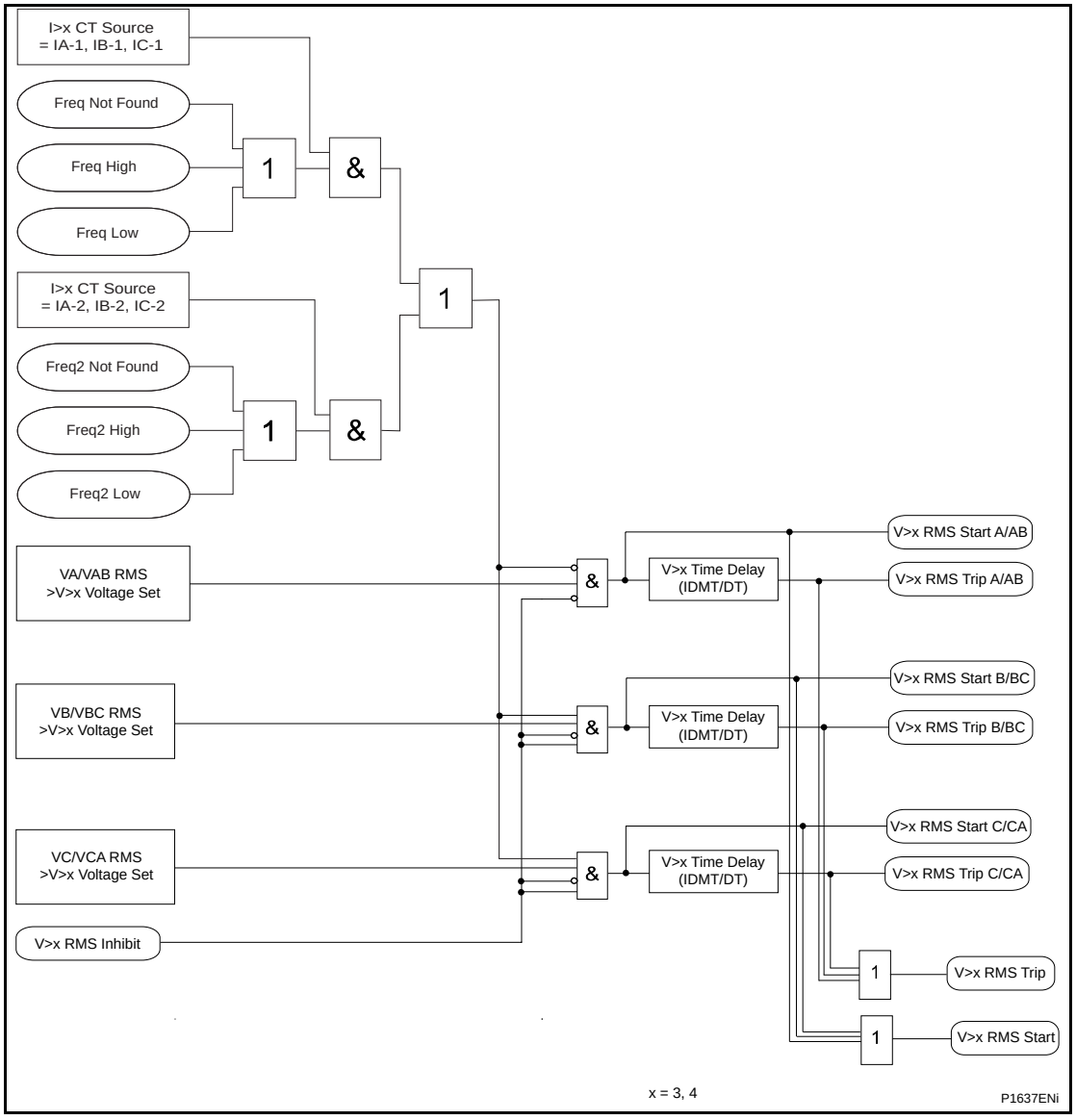


Figure 95: RMS Overvoltage - single and three phase tripping mode (single stage)

1.35.9 Residual overvoltage/neutral voltage displacement protection function (59NR)

The RMS neutral voltage displacement protection function of the P348 consists of two stages of derived (VN>1, VN>2) neutral overvoltage protection with adjustable time delays.

The RMS neutral voltage protection stages are **Enabled/Disabled** in the **VN>1/2 status** cell. All the RMS neutral voltage stages may be selected as **IDMT, Default Curve 1/2/3/4**, **DT** or **Disabled**, within the **VN>1/2 Function** cell.

The relay derives the neutral/residual voltage operating quantity from the rotor three-phase to neutral RMS voltage measurements using the following equation:

Vneutral = VA-1 RMS + VB-1 RMS + VC-1 RMS

The IDMT characteristic available is defined by the following formula:

t = K/(M – 1)

Where:

K = Time Multiplier Setting (**VN>1/2 TMS**)

t = Operating Time in Seconds

M = Measured Residual Voltage/Relay Setting Voltage (**VN>1/2 Voltage Set**)

As well as the standard curves, it is possible to program up to four custom curves, **Default Curve 1/2/3/4,** using General Electric's User Programmable Curve Tool, described in the MiCOM S1 Agile Setting Application Software User Guide. This is a user-friendly tool by which users can create curves either by formula or by entering data points. Programmable curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves.

The neutral voltage displacement protection function is blocked by the VT supervision function.

The functional block diagram of the residual overvoltage protection is shown in Figure 96.

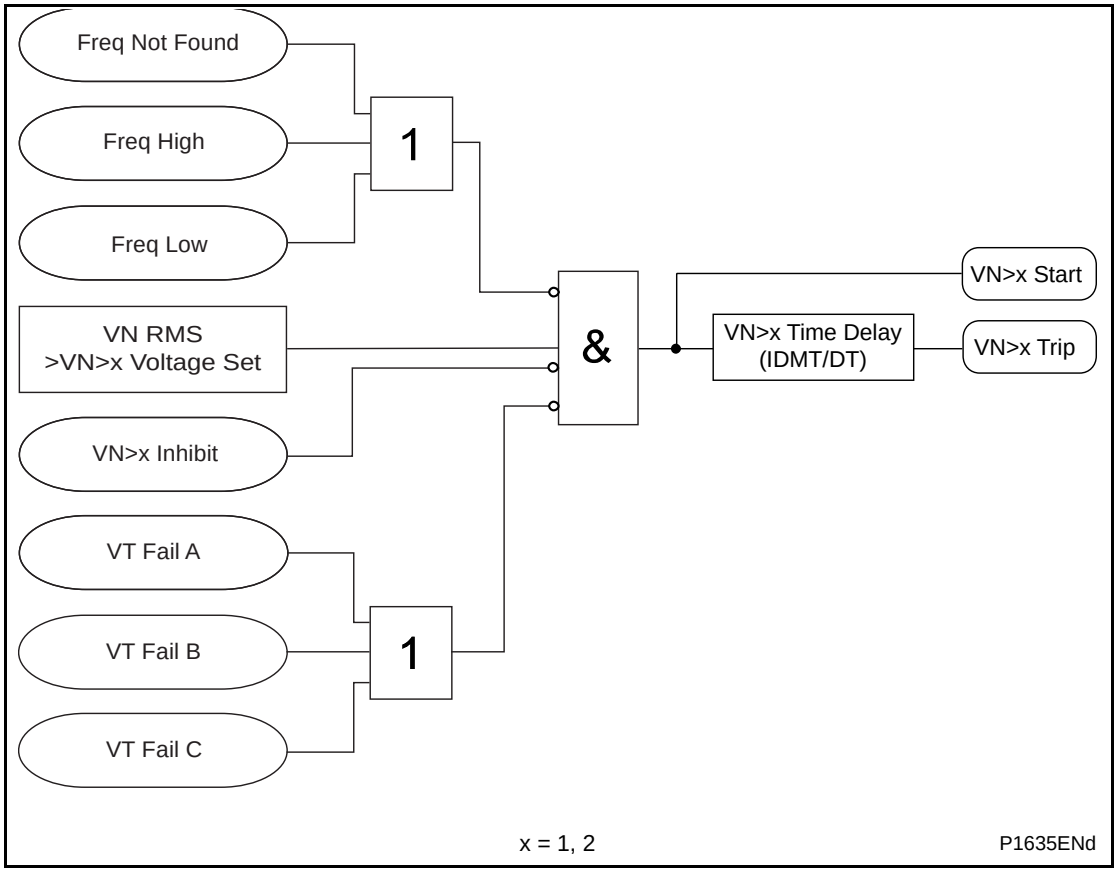


Figure 96: Residual overvoltage logic (single stage)

All neutral overvoltage stages can be blocked by energizing the inhibit DDB signals via the PSL (VN>1/2 Inhibit: DDB 610, 611). The rotor RMS based protection stages are blocked if any of the DDBs 'Freq Not Found', DDB 1295 'Freq High' DDB 1293 or 'Freq Low' DDB 1294 are TRUE. The Freq Low DDB is operated when the frequency is below the **RMS F< Block** threshold in the **System Config** menu.

DDB signals are also available to indicate the start and trip of each stage of protection, (Starts: DDB 1088-1089 Trips: 832-833). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The residual overvoltage fault protection starts are mapped internally to the ANY START DDB signal – DDB 992.

1.35.10 Overfrequency protection (81OR)

The P348 relays include 4 definite time stages of overfrequency protection to detect excessive slip frequencies in the rotor. All the stages may be **Enabled/Disabled** in the **F>n Status** cell depending on which element is selected.

The functional logic diagram for the overfrequency function is as shown in Figure 97.

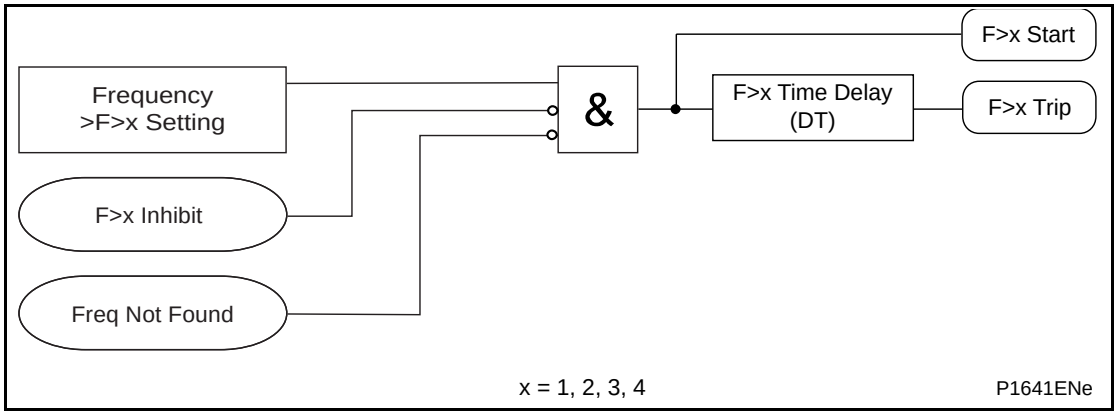


Figure 97: Overfrequency logic (single stage)

OP

All overfrequency stages can be blocked by energizing the inhibit DDB signals via the PSL (F>1/2/3/4 Inhibit: DDB 620, 623). The overfrequency protection is blocked if the 'Freq Not Found' DDB 1295 is TRUE.

DDB signals are also available to indicate start and trip of each stage, (Starts: DDB DDB 1176-1177, Trips: DDB 920-921).

The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The overfrequency protection starts are mapped internally to the ANY START DDB signal – DDB 992.

1.35.11 Current and voltage transformer supervision

See sections 2.4 and 2.8 for information on the P348 NCCT and NCVT supervision.

2 OPERATION OF NON PROTECTION FUNCTIONS

2.1 Check synchronism (25)

2.1.1 Overview

In most situations it is possible for both the **Generator** and **Bus** sides of a circuit breaker to be live when the circuit breaker is open, for example where the Bus has a power source. Therefore when closing the circuit breaker, it is normally necessary to check that the network conditions on both sides are suitable, before giving a CB Close command. This applies to manual circuit breaker closing of any CB and auto-reclosure applications specific to feeder CBs. If a circuit breaker is closed when the generator and bus voltages are both live, with a large phase angle, frequency or magnitude difference between them, the system could be subjected to an unacceptable shock, resulting in loss of stability, and possible damage to connected machines.

System checks involve monitoring the voltages on both sides of a circuit breaker, and, if both sides are live, performing a synchronism check to determine whether the phase angle, frequency and voltage magnitude differences between the voltage vectors, are within permitted limits.

The pre-closing system conditions for a given circuit breaker depend on the system configuration and, for auto-reclosing, on the selected auto-reclose program. For example, on a feeder with delayed auto-reclosing, the circuit breakers at the two line ends are normally arranged to close at different times. The first line end to close usually has a live bus and a dead line immediately before reclosing, and charges the line (dead line charge) when the circuit breaker closes. The second line end circuit breaker sees live bus and live line after the first circuit breaker has re-closed. If there is a parallel connection between the ends of the tripped feeder, they are unlikely to go out of synchronism, i.e. the frequencies will be the same, but the increased impedance could cause the phase angle between the two voltages to increase. Therefore the second circuit breaker to close might need a synchronism check, to ensure that the phase angle has not increased to a level that would cause an unacceptable shock to the system when the circuit breaker closes.

If there are no parallel interconnections between the ends of the tripped feeder, the two systems could lose synchronism, and the frequency at one end could slip relative to the other end. In this situation, the second line end would require a synchronism check comprising both phase angle and slip frequency checks.

If the second line end busbar has no power source other than the feeder that has tripped; the circuit breaker will see a live line and dead bus assuming the first circuit breaker has re-closed. When the second line end circuit breaker closes the bus will charge from the live line (dead bus charge).

For generator applications before closing the CB the frequency and voltage from the machine is varied automatically or manually until the generator voltage is in synchronism with the power system voltage. A check synchronizing relay is used to check the generator voltage is in synchronism with the system voltage in terms of voltage magnitude, voltage difference, phase angle and slip frequency before the generator CB is allowed to close.

2.1.2 VT selection

The P34x has a three-phase **Main VT** input and a single-phase **Check Sync VT** input. Depending on the primary system arrangement, the main three-phase VT for the relay may be located on either the busbar side or the generator side of the circuit breaker, with the check sync. VT being located on the other side. Hence, the relay has to be programmed with the location of the main VT. This is done via the **Main VT Location - Gen/Bus** setting in the **SYSTEM CONFIG** menu. This is required for the voltage monitors to correctly define the Live Gen/Dead Gen and Live Bus/Dead Bus DDBs.

The Check Sync. VT may be connected to either a phase to phase or phase to neutral voltage, and for correct synchronism check operation, the relay has to be programmed with the required connection. The **C/S Input** setting in the **CT & VT RATIOS** menu should be set to **A-N**, **B-N**, **C-N**, **A-B**, **B-C** or **C-A** as appropriate.

The P342/3 uses the neutral voltage input, VNeutral, for the Check Synch VT and so the user can not use check synch and measured neutral voltage (59N) protection (VN>3, VN>4) at the same time. The derived neutral voltage protection (VN>1, VN>2) from the 3 phase voltage input can still be used with the check synchronizing function.

The P344 uses the neutral voltage input, VN2, for the Check Synch VT and so the user can not use check synch and measured neutral voltage (59N) protection from VN2 (VN>5, VN>6) at the same time. The derived neutral voltage protection (VN>1, VN>2) from the 3 phase voltage input and the measured neutral voltage protection (VN>3, VN>4) from the VN1 voltage input can still be used with the check synchronising function.

The P345 uses a dedicated V Check Sync voltage input for the Check Synch VT and so there are no restrictions in using the check synchronising function and other protection functions in the relay.

2.1.3 Basic functionality

System check logic is collectively enabled or disabled as required, by setting **System Checks** in the CONFIGURATION menu. The associated settings are available in **SYSTEM CHECKS**, sub-menus **VOLTAGE MONITORS**, **CHECK SYNC** and **SYSTEM SPLIT**. If **System Checks** is selected to **Disabled**, the associated **SYSTEM CHECKS** menu becomes invisible, and a **Sys checks inactive** DDB signal is set.

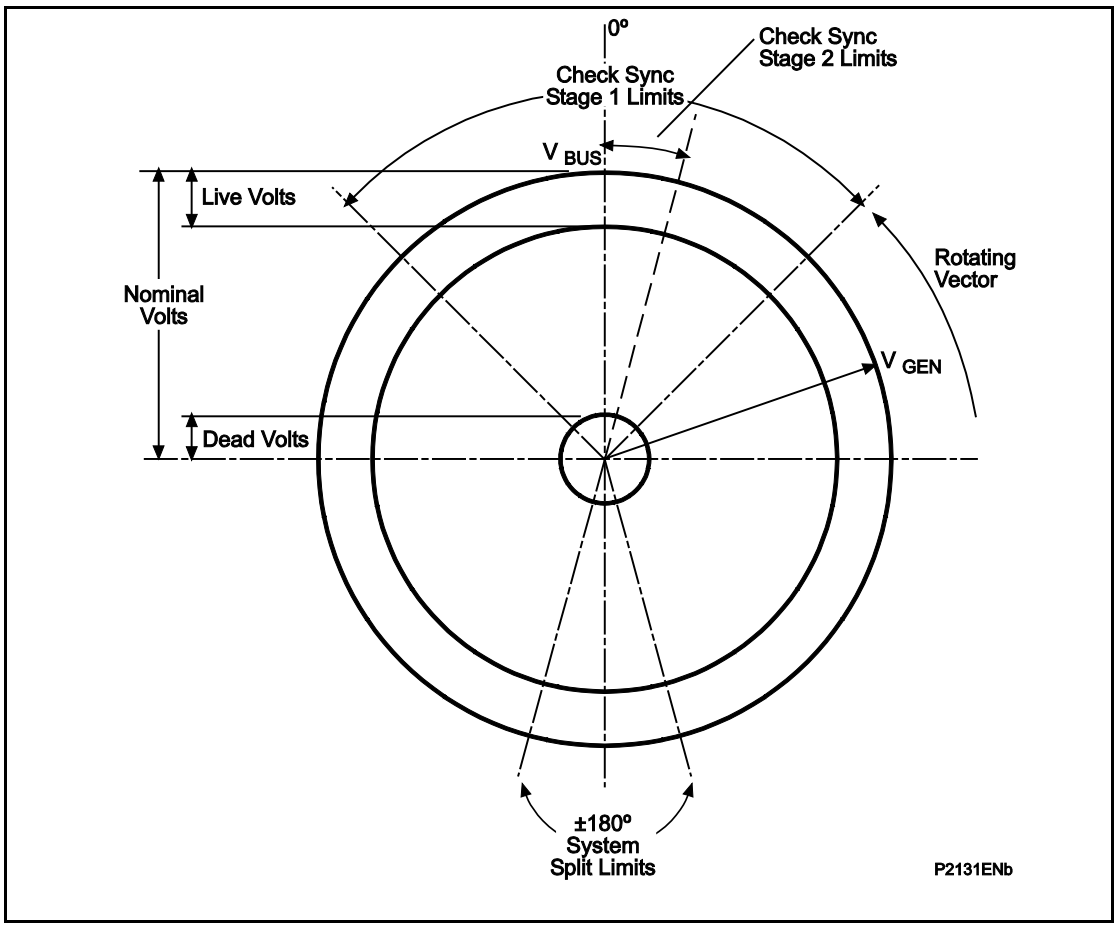


Figure 98: Synchro check and synchro split functionality

The overall **Check Sync** and **System Split** functionality is shown in Figure 98.

In most situations where synchronism check is required, the Check Sync 1 function alone will provide the necessary functionality, and the Check Sync 2 and System Split signals can be ignored.

2.1.3.1 Voltage Monitors

The P34x System Checks function includes voltage monitors to indicate if the generator and system busbar voltages are Live or Dead.

The voltage monitor DDBs, if required, are combined in the PSL to provide the manual CB close check synchronizing logic, eg Dead Line/Live Gen. The DDBs are connected to the Man Check Synch DDB (1362) which provides an input to the CB control logic to indicate a manual check synchronizing condition is satisfied.

When Vgen magnitude is > Live Voltage, the generator is taken as Live (DDB 1328, Live Gen)

When Vgen magnitude is < Dead Voltage, the generator is taken as Dead (DDB 1329, Dead Gen)

When Vbus magnitude is > Live Voltage, the busbar is taken as Live (DDB 1330, Live Bus)

When Vbus magnitude is < Dead Voltage, the busbar is taken as Dead (DDB 1331, Dead Bus)

2.1.3.2 Synchronism check

The P34x System Checks function includes 2 check synchronisation elements, Check Sync 1 and Check Sync 2. The check synch 1 OK (1332) and Check Synch 2 OK (1333) DDBs, if required, are used in the PSL to provide the manual CB close check synchronizing logic. The DDBs are connected to the Man Check Synch DDB (1362) which provides an input to the CB control logic to indicate a manual check synchronising condition is satisfied.

Each check synch element checks that the generator frequency, voltage magnitude, and phase angle match the system frequency, voltage magnitude, and phase angle before allowing the generator breaker to be closed. Each element includes settings for the phase angle difference and slip frequency between the generator and system busbar voltages.

The P34x also includes independent under/over voltage monitors for the generator and system side of the CB as well as a differential voltage monitor applicable to both the Check Sync 1 and 2 elements. The user can select a number of under/over/differential voltage check synchronizing blocking options using the setting **CS Voltage Block** – **None, V<, V>, Vdiff>, V< and V>, V< and Vdiff>, V> and Vdiff>, V< V> Vdiff>.**

The slip frequency used by Check Synch 1/2 can be calculated from the **CS1/2 Phase Angle** and **CS1/2 Slip Timer** settings as described below or can be measured directly from the frequency measurements, slip frequency = |Fgen-Fbus|. The user can select a number of slip frequency options using the settings **CS1 Slip Control** – **None, Timer Only, Frequency Only, Frequency + Timer , Frequency + CB** and **CS2 Slip Control** – **None, Timer, Frequency**.

If Slip Control by **Timer** or **Frequency + Timer**/**Both** is selected, the combination of **CS Phase Angle** and **CS Slip Timer** settings determines an effective maximum slip frequency, calculated as:

$$\frac{2 \times A}{T \times 360}$$ Hz. for Check Sync. 1, or

$$\frac{A}{T \times 360}$$ Hz. for Check Sync. 2

A = Phase Angle setting (°)
T = Slip Timer setting (seconds)

The **Frequency + CB** (Frequency + CB Time Compensation) setting modifies the Check Sync 2 function to take account of the circuit breaker closing time. When set to provide **CB Close Time** compensation, a predictive approach is used to close the circuit breaker ensuring that closing occurs at close to 0º therefore minimising the impact to the power system. The actual closing angle is subject to the constraints of the existing product

architecture, i.e. the protection task runs four times per power system cycle, based on frequency tracking over the frequency range of 5 Hz to 70 Hz.

Check Sync 1 and Check Sync 2 are two synchronism check logic modules with similar functionality, but independent settings (see Figure 98).

For either module to function:

the **System Checks** setting must be **Enabled**

AND

the individual **CS1/2 Status** setting must be **Enabled**

AND

the module must be individually enabled, by activation of DDB signal **CS1/2 Enabled**, mapped in PSL.

When enabled, each logic module sets its output signal when:

Gen volts and bus volts are both live (Gen Live and Bus Live signals both set)

AND

measured phase angle is < **CS1/2 Phase Angle** setting

AND

(for Check Sync 2 only), the phase angle magnitude is decreasing (Check Sync 1 can operate with increasing or decreasing phase angle provided other conditions are satisfied)

AND

if **CS1/2 Slip Control** is set to **Frequency Only** or **Frequency** or **Frequency + Timer**, the measured slip frequency is < **CS1/2 Slip Freq** Setting

AND

if **CS Voltage Block** is set to **V>** or **V< and V>** or **V> and VDiff>** or **V< V> Vdiff>,** both generator voltage and busbar voltage magnitudes are < **Gen Over Voltage** and **Bus Over Voltage** setting respectively

AND

if **CS Voltage Block** is set to **V<**, or **V< and V>** or **V< and Vdiff>** or **V< V> Vdiff>,** generator voltage and busbar voltage magnitudes are > **Gen Under Voltage** and **Bus Under Voltage** setting respectively

AND

if **CS Voltage Block** is set to **Vdiff>** or **V< and Vdiff** or **V> and VDiff>** or **V< V> Vdiff>**, the voltage magnitude difference between generator voltage and busbar voltage is < **CS Diff Voltage** setting

AND

if **CS 1/2 Slip Control** is set to **Timer** or **Frequency + Timer** (CS1) / **Freq + Timer** (CS2), the above conditions have been true for a time > or = **CS 1/2 Slip Timer** setting

2.1.3.3 System split

For the System Split module to function (see Figure 98):

The **System Checks** setting must be **Enabled**

AND

the **SS Status** setting must be **Enabled**

AND

the module must be individually enabled, by activation of DDB signal **Sys Split Enabled**, mapped in PSL.

When enabled, the System Split module sets its output signal when:

Gen volts and bus volts are both live (Line Gen and Bus Live signals both set)

AND

measured phase angle is > **SS Phase Angle** setting

AND

if **SS Volt Blocking** is set to **Enabled**, both gen volts and bus volts magnitudes are > **SS Undervoltage** setting

The System Split output remains set for as long as the above conditions are true, or for a minimum period equal to the **SS Timer** setting, whichever is longer.

The overall system checks functionality and default PSL for the function is shown in Figure 99 respectively.

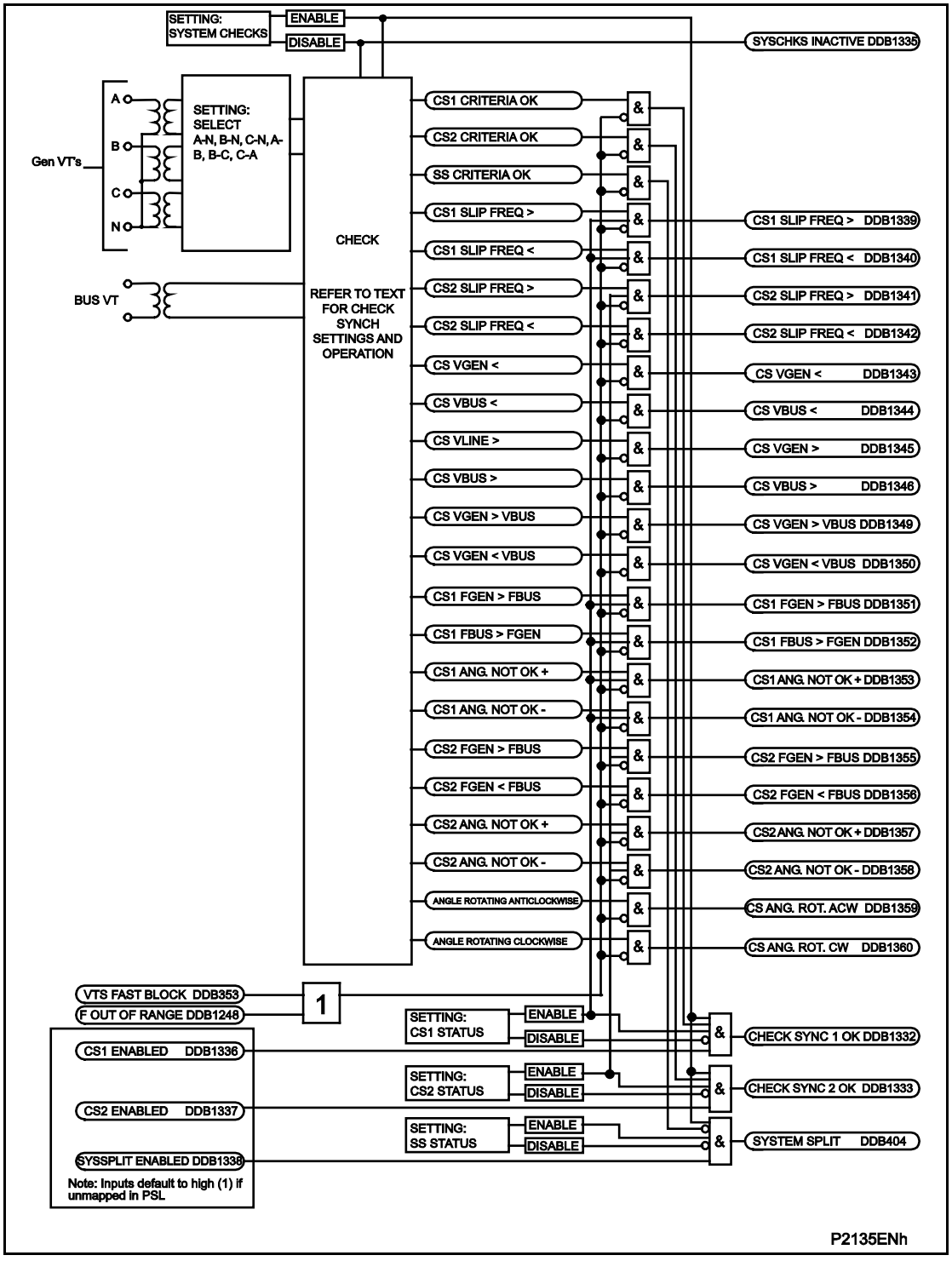


Figure 99: System checks functional logic diagram

2.1.3.4 Voltage and phase angle correction

This **C/S V Ratio Corr** setting in the **SYSTEM CONFIG** menu is used by the **System Check** function to provide magnitude correction to the check synch VT to correct for small differences between the main VT and check synch VT. Magnitude differences may be introduced by unmatched or slightly erroneous voltage transformer ratios, normally the setting is close to 1.0.

The **Main VT Vect Grp** setting in the **SYSTEM CONFIG** menu is used by the **System Check** function to provide vector correction between the main VT and check synch VT caused by the vector group phase shift (eg 30 degree phase shift for a Dy11 or Dy1 transformer vector group) across the generator-transformer.

There are some applications where the main VT is on the generator side of a transformer and the check sync VT is in the transformer LV side or vice-versa where vector group correction may be required.

2.2 VT supervision (P342-6)

The voltage transformer supervision (VTS) feature is used to detect failure of the ac voltage inputs to the relay. This may be caused by internal voltage transformer faults, overloading, or faults on the interconnecting wiring to relays. This usually results in one or more VT fuses blowing. Following a failure of the ac voltage input there would be a misrepresentation of the phase voltages on the power system, as measured by the relay, which may result in mal-operation.

The VTS logic in the relay is designed to detect the voltage failure, and automatically adjust the configuration of protection elements whose stability would otherwise be compromised. A time-delayed alarm output is also available.

There are three main aspects to consider regarding the failure of the VT supply. These are defined below:

1. Loss of one or two-phase voltages
2. Loss of all three-phase voltages under load conditions
3. Absence of three-phase voltages upon line energization

The VTS feature within the P342-6 relays operates on detection of negative phase sequence (NPS) voltage without the presence of negative phase sequence current. This gives operation for the loss of one or two-phase voltages. Stability of the VTS function is assured during system fault conditions, by the presence of NPS current. The use of negative sequence quantities ensures correct operation even where three-limb or 'V' connected VT's are used.

Negative sequence VTS element:

The negative sequence thresholds used by the element are V2 = 10 V (Vn = 100/120 V) or 40 V (Vn = 380/480 V), and I2 = 0.05 to 0.5 In settable (defaulted to 0.05 In).

2.2.1 Loss of all three-phase voltages under load conditions

Under the loss of all three-phase voltages to the relay, there will be no negative phase sequence quantities present to operate the VTS function. However, under such circumstances, a collapse of the three-phase voltages will occur. If this is detected without a corresponding change in any of the phase current signals (which would be indicative of a fault), then a VTS condition will be raised. In practice, the relay detects the presence of superimposed current signals, which are changes in the current applied to the relay. These signals are generated by comparison of the present value of the current with that exactly one cycle previously. Under normal load conditions, the value of superimposed current should therefore be zero. Under a fault condition a superimposed current signal will be generated which will prevent operation of the VTS.

The phase voltage level detectors are fixed and will drop off at 10 V (Vn = 100/120 V), 40 V (Vn = 380/480 V) and pick-up at 30 V (Vn = 100/120 V), 120 V (Vn = 380/480 V).

The sensitivity of the superimposed current elements is fixed at 0.1 In.

2.2.2 Absence of three-phase voltages upon line energisation

If a VT were inadvertently left isolated prior to line energisation, incorrect operation of voltage dependent elements could result. The previous VTS element detected three-phase VT failure by absence of all three-phase voltages with no corresponding change in current. On line energisation there will, however, be a change in current (as a result of load or line charging current for example). An alternative method of detecting three-phase VT failure is therefore required on line energisation.

The absence of measured voltage on all three-phases on line energisation can be as a result of 2 conditions. The first is a three-phase VT failure and the second is a close up three-phase fault. The first condition would require blocking of the voltage dependent function and

the second would require tripping. To differentiate between these 2 conditions an overcurrent level detector (VTS I> Inhibit) is used which will prevent a VTS block from being issued if it operates. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close up three-phase fault. If the line is now closed where a three-phase VT failure is present the overcurrent detector will not operate and a VTS block will be applied. Closing onto a three-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

This logic will only be enabled during a live line condition (as indicated by the relays pole dead logic) to prevent operation under dead system conditions i.e. where no voltage will be present and the VTS I> Inhibit overcurrent element will not be picked up.

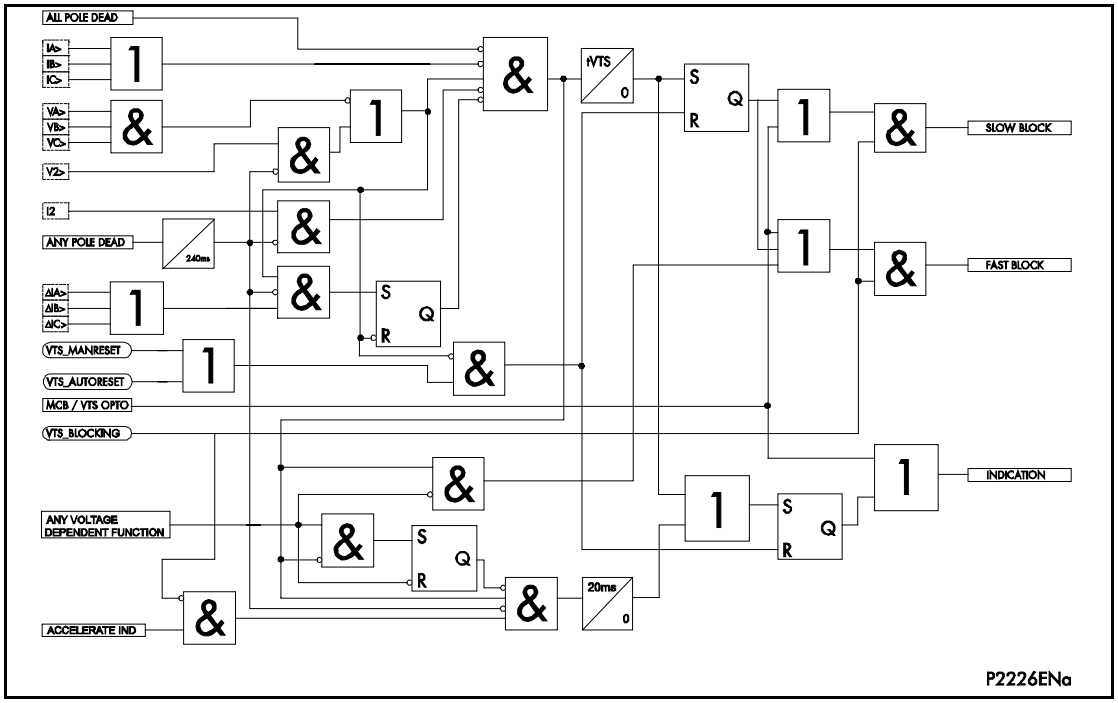


Figure 100: VTS logic

Required to drive the VTS logic are a number of dedicated level detectors as follows:

- IA>, IB>, IC>, these level detectors operate in less than 20 ms and their settings should be greater than load current. This setting is specified as the VTS current threshold. These level detectors pick-up at 100% of setting and drop-off at 95% of setting.
- I2>, this level detector operates on negative sequence current and has a user setting. This level detector picks-up at 100% of setting and drops-off at 95% of setting.
- ΔIIA>, ΔIB>, ΔIC>, these level detectors operate on superimposed phase currents and have a fixed setting of 10% of nominal. These level detectors are subject to a count strategy such that 0.5 cycle of operate decisions must have occurred before operation.
- VA>, VB>, VC>, these level detectors operate on phase voltages and have a fixed setting, Pick-up level = 30 V (Vn = 100/120 V), 120 V (Vn = 380/480 V), Drop Off level = 10 V (Vn = 100/120 V), 40 V (Vn = 380/480 V).
- V2>, this level detector operates on negative sequence voltage, it has a fixed setting of 10 V/40 V depending on VT rating (100/120 or 380/480) with pick-up at 100% of setting and drop-off at 95% of setting.

2.2.2.1 Inputs

Signal name	Description
IA>, IB>, IC>	Phase current levels (Fourier magnitudes)
I2>	I2 level (Fourier magnitude).
ΔIA, ΔIB, ΔIC	Phase current samples (current and one cycle previous)
VA>, VB>, VC>	Phase voltage signals (Fourier magnitudes)
V2>	Negative sequence voltage (Fourier magnitude)
ALL POLE DEAD	Breaker is open for all phases (driven from auxiliary contact or pole dead logic).
VTS_MANRESET	A VTS reset performed via front panel or remotely.
VTS_AUTORESET	A setting to allow the VTS to automatically reset after this delay.
MCB/VTS OPTO	To remotely initiate the VTS blocking via an opto
Any Voltage Dependent Function	Outputs from any function that utilizes the system voltage, if any of these elements operate before a VTS is detected the VTS is blocked from operation. The outputs include starts and trips.
Accelerate Ind	Signal from a fast tripping voltage dependent function used to accelerate indications when the indicate only option is selected
Any Pole Dead	Breaker is open on one or more than one phases (driven from auxiliary contact or pole dead logic)
tVTS	The VTS timer setting for latched operation

Table 27: VTS inputs

2.2.2.2 Outputs

Signal name	Description
VTS Fast Block	Used to block voltage dependent functions
VTS Slow Block	Used to block the Any Pole dead signal
VTS Indication	Signal used to indicate a VTS operation

Table 28: VTS outputs

2.2.3 Operation

The relay may respond as follows to an operation of any VTS element:

- VTS set to provide alarm indication only (DDB 356 VT Fail Alarm);
- Optional blocking of voltage dependent protection elements (DDB 1248 VTS Fast Block, DDB 1249 VTS Slow Block);
- Optional conversion of directional SEF, directional overcurrent and directional NPS overcurrent elements to non-directional protection (available when set to blocking mode only). These settings are found in the function links cell of the relevant protection element columns in the menu.

Time delayed protection elements (Directional NPS Overcurrent, Directional SEF, Power, Sensitive Power, Field Failure) are blocked after the VTS Time Delay on operation of the VTS Slow Block. Fast operating protection elements (Directional overcurrent, Neutral Voltage Displacement, System Backup, Undervoltage, Dead Machine, Pole Slipping, NPS Overpower) are blocked on operation of the VTS Fast Block.

Note: The directional SEF and neutral voltage displacement protection are only blocked by VTS if the neutral voltage input is set to Derived and not Measured.

OP

Other protections can be selectively blocked by customizing the PSL, integrating DDB 1248 VTS Fast Block and DDB 1249 VTS Slow Block with the protection function logic.

The VTS I> Inhibit or VTS I2> Inhibit elements are used to override a VTS block in event of a fault occurring on the system which could trigger the VTS logic. Once the VTS block has been established, however, then it would be undesirable for subsequent system faults to override the block. The VTS block will therefore be latched after a user settable time delay 'VTS Time Delay'. Once the signal has latched then two methods of resetting are available. The first is manually via the front panel interface (or remote communications) provided the VTS condition has been removed and secondly, when in 'Auto' mode, by the restoration of the three-phase voltages above the phase level detector settings mentioned previously.

A VTS indication will be given after the **VTS Time Delay** has expired. In the case where the VTS is set to indicate only the relay may potentially mal-operate, depending on which protection elements are enabled. In this case the VTS indication will be given prior to the VTS time delay expiring if a trip signal is given.

Where a miniature circuit breaker (MCB) is used to protect the voltage transformer ac output circuits, it is common to use MCB auxiliary contacts to indicate a three-phase output disconnection. As previously described, it is possible for the VTS logic to operate correctly without this input. However, this facility has been provided for compatibility with various utilities current practices. Energizing an opto-isolated input assigned to "MCB Open" on the relay will therefore provide the necessary block.

Where directional overcurrent elements are converted to non-directional protection on VTS operation, it must be ensured that the current pick-up setting of these elements is higher than full load current.

The blocking of the VTS logic for a number of different fault conditions is considered below, assuming Vn = 100/120 V.

1. Phase-earth fault

The I2> element should detect phase-earth faults and block the VTS logic when the CB is closed for solidly earthed generators.

For a high impedance earthed system the level of Io, I2 and V2 will be very small <5% for an earth fault. For a generator connected to load if there is a close-up earth fault where the voltage on 1 phase < 10 V and the delta change in current on the faulted phase is >10%In the VTS logic is blocked.

For example if load current is 0.5 In and there is an A-N fault then the current in the faulted phase will drop to say 1%In during an earth fault and so delta IA = 0.49 In which is > 0.1 In delta threshold. So, Delta I = ON, Any Pole Dead = OFF, VA> = OFF (<10 V) for a close up fault and so the VTS is blocked.

During starting of the machine if the CB auxiliary contacts are indicating the CB is open the VTS logic is blocked. However, if a contact is used to indicate the CB is closed during the start up of the machine then the VTS logic will be active.

If there is an A-N fault during the start-up of the machine and the CB is closed and the voltage was >30 V (VA>/VB>/VC>) if the VA> element drops off (<10 V) due to the fault and the delta change in current is <10% In (delta IA>) there could be a potential incorrect operation of the VTS logic.

So, if the load current during the start up period is < 0.1In then there could be a false VTS operation if the relay thinks the CB is closed. If the VTS operates it will block the derived neutral voltage protection but the measured neutral voltage protection is not blocked and will trip correctly during an earth fault.

2. Phase-phase fault

The I2> element should detect phase-phase faults and block the VTS logic when the CB is closed.

3. 3 phase faults

The delta current level detectors should detect the change in current for a close up 3 phase fault when the CB is closed and block the VTS.

The IA>/IB>/IC> level detectors should detect a 3 phase fault when closing the CB onto a fault and block the VTS logic.

2.3 NCVT supervision (P348)

The voltage transformer supervision (VTS) feature is used to detect failure of the rotor ac voltage inputs to the relay. This may be caused by internal voltage transformer faults, overloading, or faults on the interconnecting wiring to the relays or failures in the acquisition chain including the merging unit and primary converter (PC14). Following a failure of the ac voltage input there would be a misrepresentation of the phase voltages on the power system, as measured by the relay, which may result in mal-operation of the neutral voltage protection.

The VTS logic in the relay is designed to detect the voltage failure, and automatically block the neutral voltage protection elements whose stability would otherwise be compromised. A time-delayed alarm output is also available. The IEC 61850-9-2 quality flags and state machine logic will detect loss of a voltage channel but will not be able to distinguish if this is due to a rotor fault or a VT failure. Therefore, the IEC 61850-9-2 quality flags and state machine logic can not be used to block the neutral voltage protection. The VTS function is required to block the neutral voltage protection to provide stability for a NCVT failure.

The VTS feature within the P348 relay operates on the voltage balance principle by detection of a difference between the individual phase voltages from 2 sets of NCVTs (VA-1 RMS/VB-1 RMS/VC-1 RMS and VA-2 RMS/VB-2 RMS/VC-2 RMS) connected to the rotor. If only one set of NCVTs is used then this function needs to be disabled.

Stability of the VTS function is assured during normal operation and system fault conditions as both sets of NCVTs should be measuring the same voltage.

The VTS can be set to block neutral voltage protection or just to provide indication of a VTS or disabled using **VTS Status - Blocking/Indication/Disabled** setting.

Once the VTS block has been established it is undesirable for subsequent system faults to override the block. The VTS block will therefore be latched after a user settable time delay **VTS Time Delay**. Once the signal has latched the VTS is reset automatically when the VTS condition has been removed. A VTS alarm is given after the **VTS Time Delay** has expired.

The VTS can provide an alarm indication only (DDB 356 VT Fail Alarm) or optional blocking of the neutral voltage protection elements (DDB 1252/3/4 VTS Fail A//B/C).

Other protections can be selectively blocked by customizing the PSL, integrating DDB 1252-4 VT Fail A/B/C with the protection function logic. The rotor RMS protection and rotor VT supervision are blocked if any of the DDBs ‘Freq Not Found’ DDB 1295, ‘Freq High’ DDB 1293 or ‘Freq Low’ DDB 1294 are TRUE.

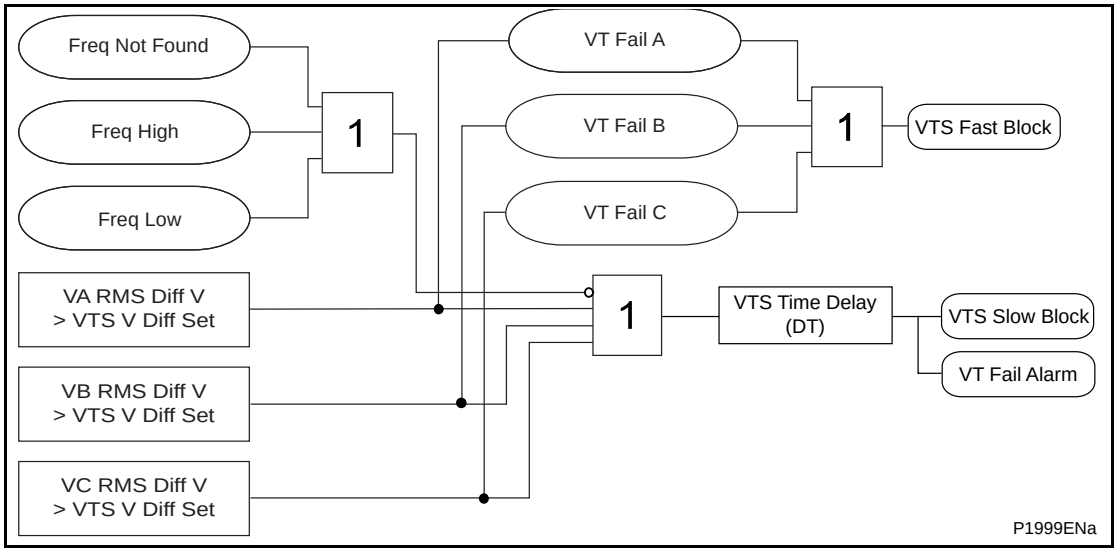


Figure 101: VT supervision diagram

2.4 CT supervision

The standard CT supervision feature in the P342-6 operates on detection of derived residual current, in the absence of corresponding derived or measured residual voltage that would normally accompany it.

The CT supervision can be set to operate from the residual voltage measured at the VNEUTRAL input (VN1 input for P342/3/4/5/6) or the residual voltage derived from the three-phase-neutral voltage inputs as selected by the 'CTS Vn Input' setting.

The voltage transformer connection used must be able to refer residual voltages from the primary to the secondary side. Therefore this element should only be enabled where the three-phase VT is of five limb construction, or comprises three single-phase units, and has the primary star point earthed. A derived residual voltage or a measured residual voltage is available.

There are two stages of CT supervision CTS-1 and CTS-2. The derived neutral current is calculated vectorially from IA, IB, IC for CTS-1 and IA-2, IB-2, IC-2 for CTS-2. The neutral voltage is either measured or derived, settable by the user.

CTS-1 supervises the CT inputs to IA, IB, IC which are used by the biased differential protection and all the power, impedance and overcurrent based protection functions. CTS-2 supervises the CT inputs to IA-2, IB-2, IC-2 which are used by the biased or high impedance differential or interturn protection in the P343/4/5/6. The CTS-2 independent enabled/disabled setting is to prevent CTS-2 from giving unnecessary alarms when the Generator Differential is disabled. For interturn faults, some utilities may isolate the faulted winding section and return the generator to service, therefore producing unbalanced phase currents. Under these circumstances the CTS-2 may also need to be disabled or de-sensitized to prevent a false alarm and a false block

Operation of the element will produce a time-delayed alarm visible on the LCD and event record (plus DDB 357: CT-1 Fail Alarm, DDB 381 CT-2 Fail Alarm), with an instantaneous block (DDB 1263: CTS-1 Block, DDB 1264 CTS-2 Block) for inhibition of protection elements. Protection elements operating from derived quantities, (Negative Phase Sequence (NPS) Overcurrent, NPS Thermal, NPS Overpower, Thermal Overload protection) are always blocked on operation of the CTS-1 supervision element; other protections can be selectively blocked by customizing the PSL, integrating DDB 1263: CTS-1 Block and DDB 1264: CTS-2 Block with the protection function logic. If blocking of the generator differential protection or interturn protection is required from the CT supervision this must be done in PSL by connecting DDB 1263: CTS-1 Block OR DDB 1264: CTS-2 Block to DDB 512: Gen Diff Block.

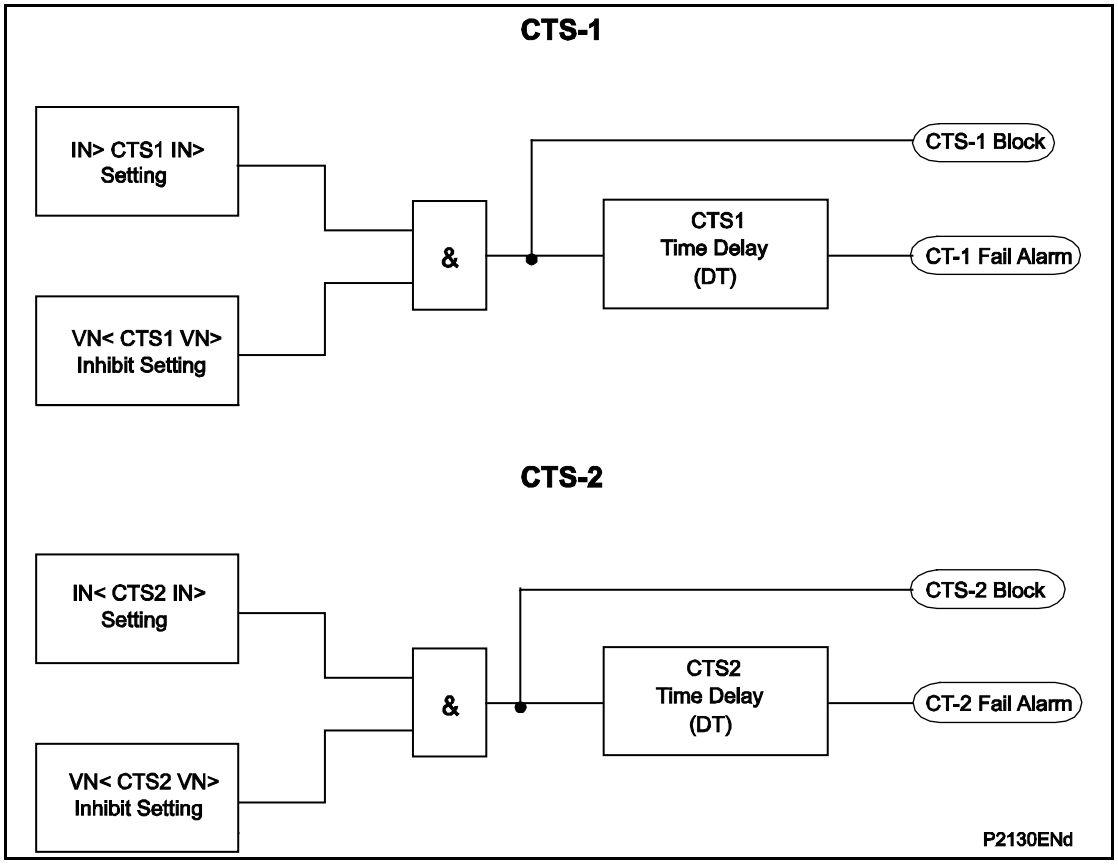


Figure 102: CT supervision diagram

2.5 Differential current transformer supervision (P343/4/5/6)

The differential current transformer supervision is based on the measurement of the ratio of I2/I1 at all ends. When this ratio is not zero, one of the following two conditions may be present:

- An unbalanced fault is present on the system – both I2 and I1 are non-zero
- There is a 1 or 2 phase CT problem – both I2 and I1 are non-zero

If the I2/I1 ratio is greater than the set value, **CTS I2/I1>2**, at all ends, it is almost certainly a genuine fault condition (**CTS I2/I1>2** set above maximum unbalanced load and below the minimum unbalanced fault current). Therefore CTS will not operate. If this ratio is detected at one end only, one of the following conditions may be present:

- A CT problem
- A single end fed fault condition

I1 is used to confirm whether it is a CT problem or not. If I1 is greater than **CTS I1** at all ends, it must be a CT problem and CTS is allowed to operate. If this condition (I1 greater than CTS I1) is detected at only one end, it is assumed that either an inrush condition or a single end fed internal fault is present. Therefore the CTS operation is blocked.

The CTS status under the **CT SUPERVISION** heading can be set either as indication or restraint. In indication mode, the CTS alarm time delay is automatically set to zero. If a CT failure is present, an alarm would be issued without delay, but the differential protection would remain unrestricted. Therefore, the risk of unwanted tripping under load current is present. In restraint mode, the differential protection is blocked for 20 ms after CT failure has been detected. Then the new setting **Is-CTS** is applied to the differential protection, as shown in Figure 103, the restraint region of the bias characteristic increases. The low impedance REF, derived earth fault (P341) and NPS overcurrent protections are internally blocked by CTS when a CT failure is detected in the CT used by each protection function.

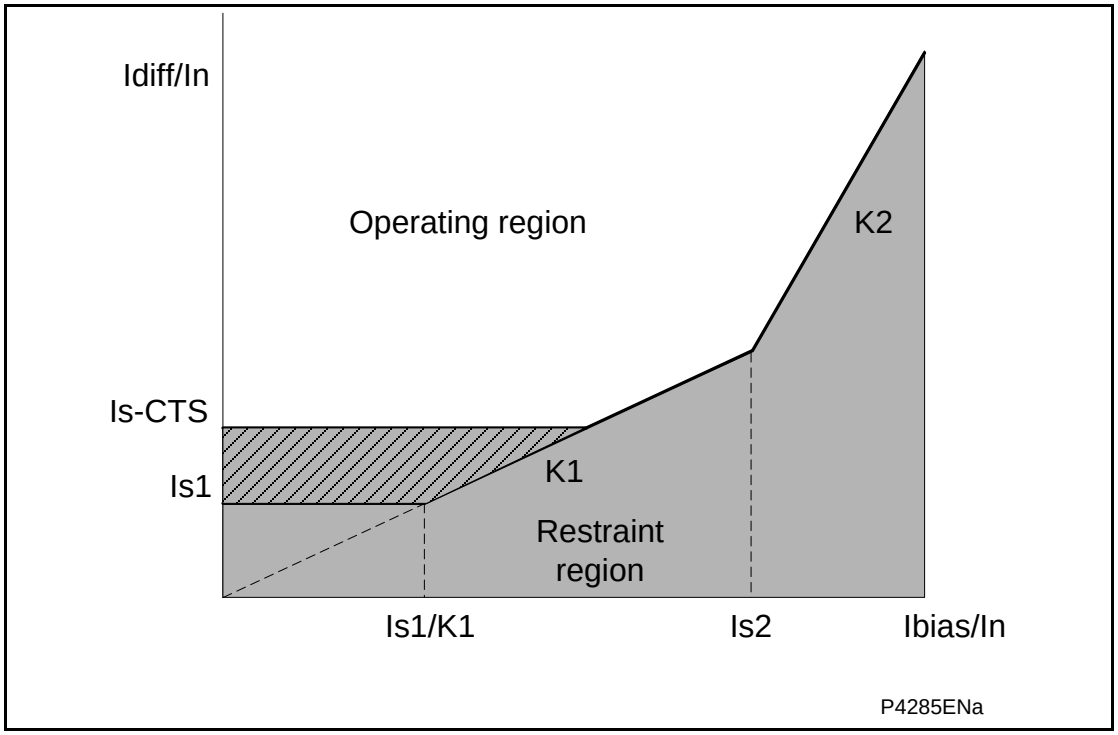


Figure 103: CTS I1 setting applied to the differential protection

The simplified logic diagram of CTS is shown in Figure 104.

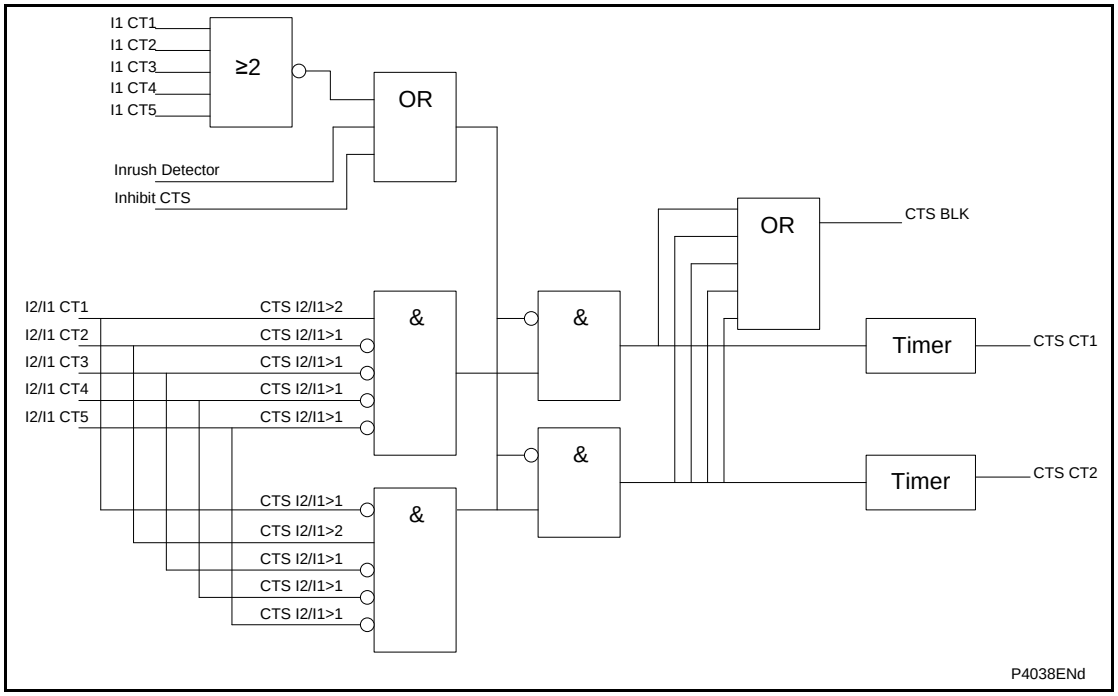


Figure 104: Differential CTS logic diagram

Figure 104 shows the CTS monitors the positive and negative sequence currents of all ends (2). A faulty CT is determined if the following conditions are present at the same time:

- The positive sequence current in at least two current inputs exceeds the set release threshold I1 (**CTS I1** setting under the **SUPERVISON** menu). This also means that CTS can only operate if minimum load current of the protected object is present.
- On exactly one end a high set ratio of negative to positive sequence current, CTS I2/I1>2, is exceeded.

- On all other ends the ratio of negative to positive sequence current is less than a low set value, CTS I2/I1> 1, or no significant current is present (positive sequence current is below the release threshold I1)

Only a single or double phase CT failure can be detected by this logic. The probability of symmetrical three-phase CT failures is very low, therefore in practice this is not a significant problem.

2.6 NCCT supervision (P348)

The P348 current transformer supervision (CTS) feature is used to detect failure of the stator ac current inputs to the relay. This may be caused by internal current transformer faults, overloading, or faults on the interconnecting wiring to the relays or failures in the acquisition chain including the merging unit and primary converter (PC12).

The IEC 61850-9-2 quality flags and state machine logic will also detect loss of a channel and block the appropriate protection functions.

In addition the P348 provides stator CT supervision to detect NCCT failure and block the stator negative phase sequence overcurrent protection. The P348 CT supervision operates in the same way as the P342-6 CT supervision (see section 2.4) by detecting derived residual current in the absence of corresponding derived or measured residual voltage (VN) that would normally accompany it during an unbalanced fault. However, it is not possible to measure stator residual voltage in the P348 as the P348 does not measure the stator voltages. The residual voltage, therefore, needs to come from an external source, for example the stator P34x protection relay.

The voltage transformer connection used must be able to refer residual voltages from the primary to the secondary side. Therefore the residual voltage element should only be enabled where the three-phase VT is of five limb construction, or comprises three single-phase units, and has the primary star point earthed. A derived residual voltage or a measured residual voltage can be used.

There is one stage of CT supervision CTS-2 which supervises the NCCT inputs to IA-2, IB-2, IC-2. The derived neutral current is calculated by summating the sampled values of stator current IA-2, IB-2, IC-2 and then the RMS of the neutral current is calculated. The neutral voltage is either measured or derived by the stator generator protection relay, e.g. a P345. An output contact from the stator generator relay (DDB 1088-1093: VN>x Start) should be connected to a digital input of the P348 (DDB 1268: CTS2 No Vn) to indicate when residual voltage above setting is present. Alternatively, a GOOSE signal could also be used. A fixed time delay of 80ms is used in the P348 CTS logic to allow time for the external digital signal from the residual voltage element to be received and processed by the P348.

Operation of the CTS element will produce a time-delayed alarm visible on the LCD and event record (DDB 381 CT-2 Fail Alarm), with an instantaneous block (DDB 1264 CTS-2 Block) for inhibition of protection elements. Protection elements operating from derived quantities such as NPS Overcurrent are always blocked on operation of the CTS-2 supervision element; other protections can be selectively blocked by customizing the PSL, integrating DDB 1264: CTS-2 Block with the protection function logic. The stator RMS protection and CT supervision are blocked if any of the DDBs ‘Freq2 Not Found’ DDB 1317, ‘Freq2 High’ DDB 1315 or ‘Freq2 Low’ DDB 1316 are TRUE.

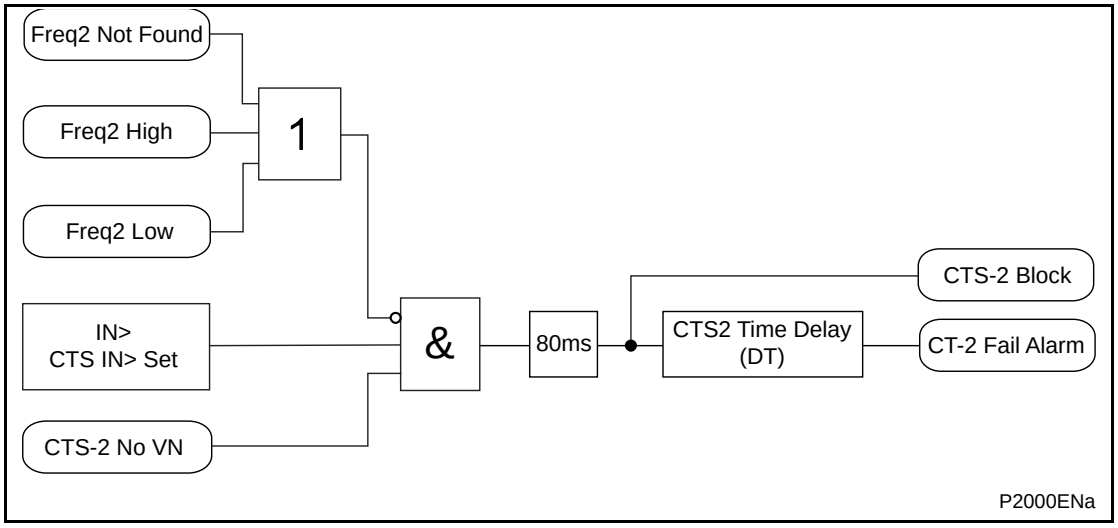


Figure 105: CT supervision diagram

2.7 Circuitry fail alarm (P343/4/5/6)

The circuitry fail alarm logic requires the following settings: **Is-cctfail>**, **K-cctfail** and **Cct Fail Delay**. If the differential current is bigger than **Is-cctfail>** setting and not trip is issued after the **tIs-cctfail>** time delay has elapsed, an alarm would be issued indicating a CT problem.

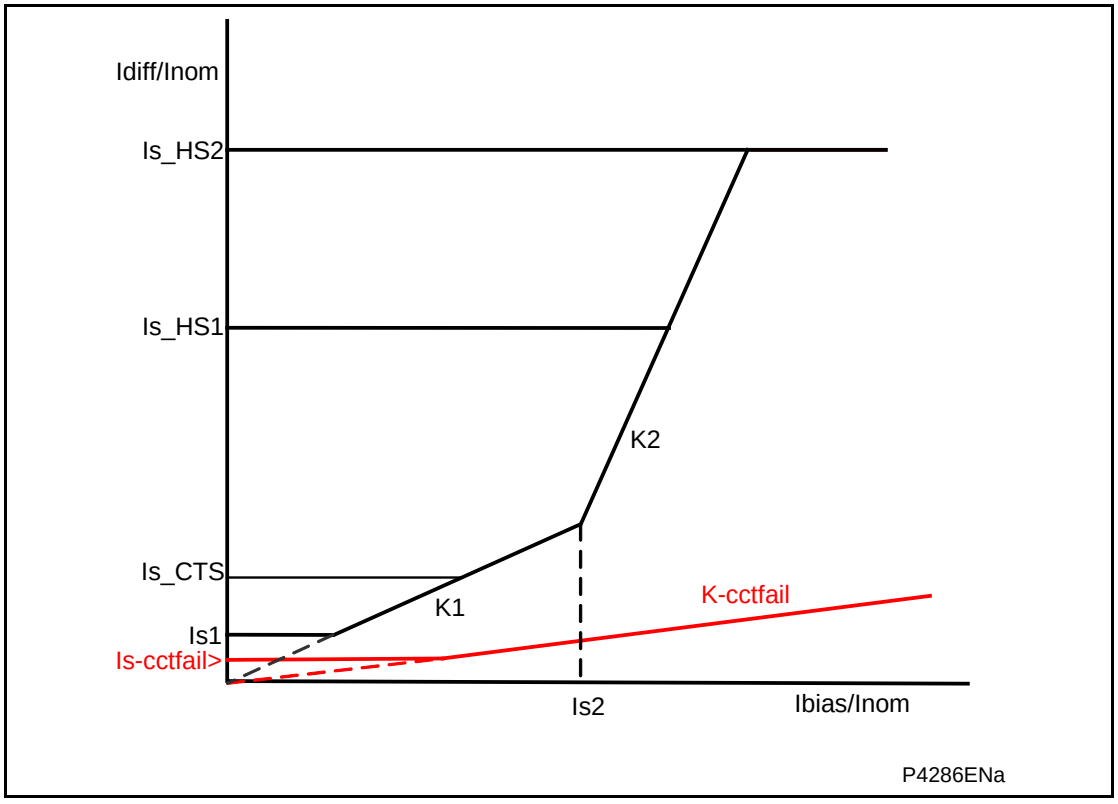


Figure 106: Circuitry fail alarm fault characteristic

2.8 Circuit breaker state monitoring

An operator at a remote location requires a reliable indication of the state of the switchgear. Without an indication that each circuit breaker is either open or closed, the operator has insufficient information to decide on switching operations. The relay incorporates circuit breaker state monitoring, giving an indication of the position of the circuit breaker, or, if the state is unknown, an alarm is raised.

2.8.1 Circuit breaker state monitoring features

MiCOM relays can be set to monitor normally open (52a) and normally closed (52b) auxiliary contacts of the circuit breaker. Under healthy conditions, these contacts will be in opposite states. Should both sets of contacts be open, this would indicate one of the following conditions:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective
- CB is in isolated position

Should both sets of contacts be closed, only one of the following two conditions would apply:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective

If any of the above conditions exist, an alarm will be issued after a 5 s time delay. A normally open/normally closed output contact can be assigned to this function via the programmable scheme logic (PSL). The time delay is set to avoid unwanted operation during normal switching duties.

In the CB CONTROL column of the relay menu there is a setting called ‘CB Status Input’. This cell can be set at one of the following four options:

None

52A

52B

Both 52A and 52B

Where ‘None’ is selected no CB status will be available. This will directly affect any function within the relay that requires this signal, for example CB control, auto-reclose, etc. Where only 52A is used on its own then the relay will assume a 52B signal from the absence of the 52A signal. Circuit breaker status information will be available in this case but no discrepancy alarm will be available. The above is also true where only a 52B is used. If both 52A and 52B are used then status information will be available and in addition a discrepancy alarm will be possible, according to the following table. 52A and 52B inputs are assigned to relay opto-isolated inputs via the PSL. The CB State Monitoring logic is shown in Figure 107).

Auxiliary contact position		CB state detected	Action
52A	52B		
Open	Closed	Breaker Open	Circuit breaker healthy
Closed	Open	Breaker Closed	Circuit breaker healthy
Closed	Closed	CB Failure	Alarm raised if the condition persists for greater than 5 s
Open	Open	State Unknown	Alarm raised if the condition persists for greater than 5 s

Table 29: CB status logic

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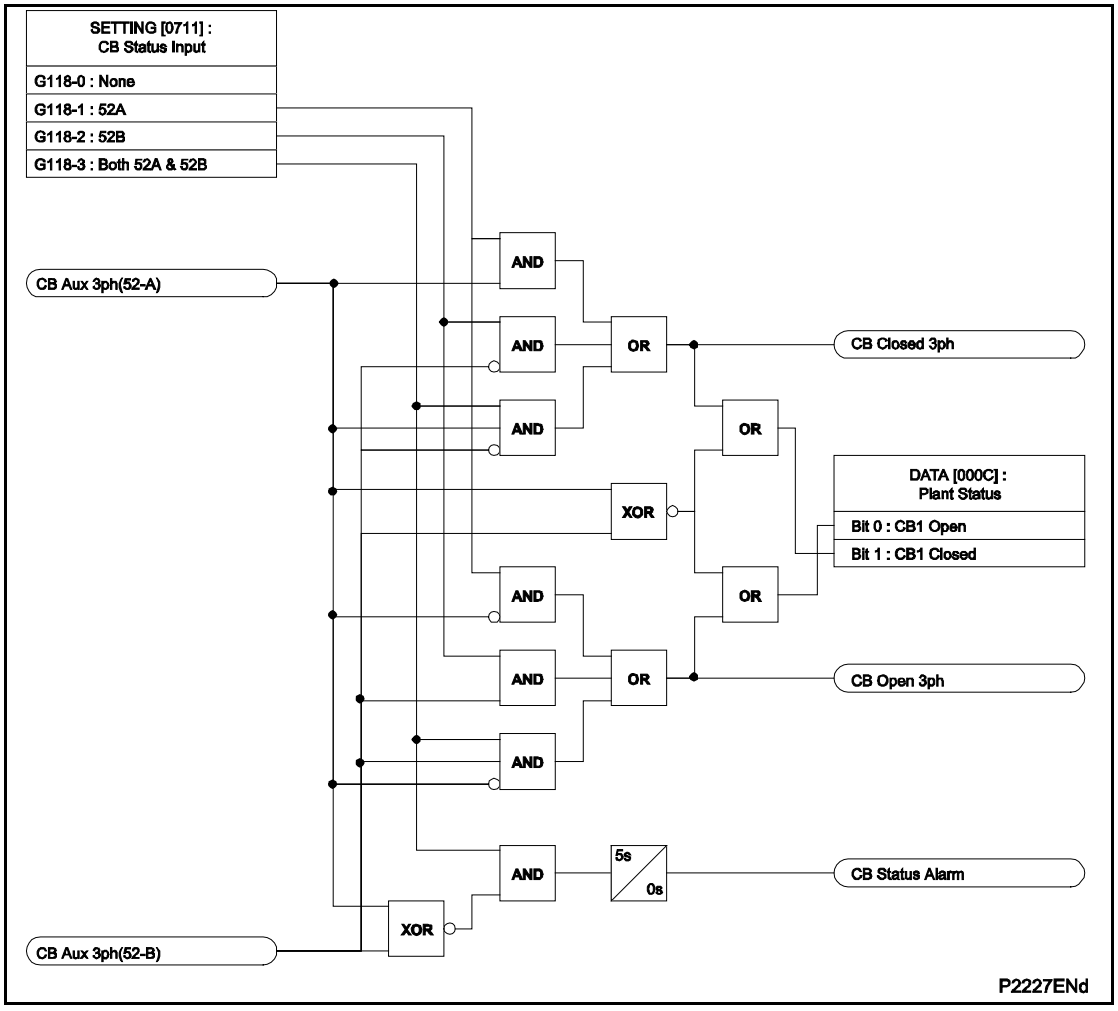


Figure 107: CB state monitoring

2.9 Pole dead logic

The Pole Dead Logic can be used to give an indication if one or more phases of the line are dead. It can also be used to selectively block operation of both the underfrequency, undervoltage and power elements. The undervoltage protection will be blocked by a pole dead condition provided the **Pole Dead Inhibit** setting is enabled. Any of the four under frequency elements can be blocked by setting the relevant **F< function links**. The Power and Sensitive Power protection will be blocked by a pole dead condition provided the **Pole Dead Inhibit** setting is enabled.

A pole dead condition can be determined by either monitoring the status of the circuit breaker auxiliary contacts or by measuring the line currents and voltages. The status of the circuit breaker is provided by the **CB State Monitoring** logic. If a **CB Open** signal (DDB 1042) is given the relay will automatically initiate a pole dead condition regardless of the current and voltage measurement. Similarly if both the line current and voltage fall below a pre-set threshold the relay will also initiate a pole dead condition. This is necessary so that a pole dead indication is still given even when an upstream breaker is opened. The undervoltage (V<) and undercurrent (I<) thresholds have the following, fixed, pickup and drop-off levels:

Settings	Range	Step size
V< Pick-up and drop off	10 V and 30 V (100/120 V) 40 V and 120 V (380/480 V)	Fixed
I< Pick-up and drop off	0.05 In and 0.055 In	Fixed

Table 30: Pole dead logic

If one or more poles are dead the relay will indicate which phase is dead and will also assert the ANY POLE DEAD DDB signal (DDB 1285). If all phases were dead the ANY POLE DEAD signal would be accompanied by the ALL POLE DEAD DDB signal (DDB 1285).

In the event that the VT fails a signal is taken from the VTS logic (DDB 1249 - Slow Block) to block the pole dead indications that would be generated by the undervoltage and undercurrent thresholds. However, the VTS logic will not block the pole dead indications if they are initiated by a **CB Open** signal (DDB 1282).

The pole dead logic diagram is shown below:

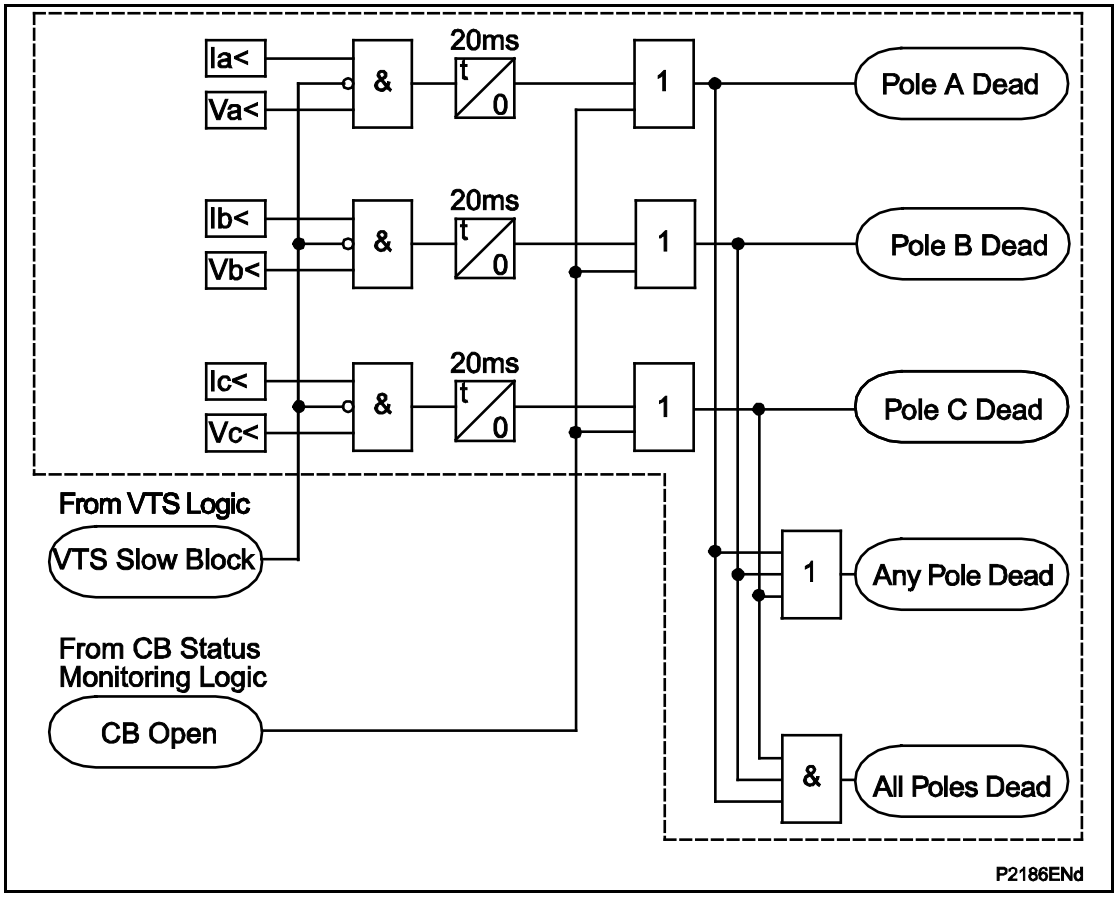


Figure 108: Pole dead logic

2.10 Circuit breaker condition monitoring

The P34x relays record various statistics related to each circuit breaker trip operation, allowing a more accurate assessment of the circuit breaker condition to be determined. These monitoring features are discussed in the following section.

2.10.1 Circuit breaker condition monitoring features

For each circuit breaker trip operation the relay records statistics as shown in the following table taken from the relay menu. The menu cells shown are counter values only. The Min./Max. values in this case show the range of the counter values. These cells can not be set:

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CB Operations {3 pole tripping}	0	0	10000	1
Displays the total number of 3 pole trips issued by the relay.				
Total IA Broken	0	0	25000 In^	1
Displays the total accumulated fault current interrupted by the relay for the A phase.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Total IB Broken	0	0	25000 In^	1
Displays the total accumulated fault current interrupted by the relay for the A phase.				
Total IC Broken	0	0	25000 In^	1 In^
Displays the total accumulated fault current interrupted by the relay for the A phase.				
CB Operate Time	0	0	0.5 s	0.001
Displays the calculated CB operating time. CB operating time = time from protection trip to undercurrent elements indicating the CB is open.				
Reset CB Data	No		Yes, No	
Reset CB Data command. Resets CB Operations and Total IA/IB/IC broken current counters to 0.				

Table 31: CB condition monitoring settings

The above counters may be reset to zero, for example, following a maintenance inspection and overhaul.

The circuit breaker condition monitoring counters will be updated every time the relay issues a trip command. In cases where the breaker is tripped by an external protection device it is also possible to update the CB condition monitoring. This is achieved by allocating one of the relays opto-isolated inputs (via the programmable scheme logic) to accept a trigger from an external device. The signal that is mapped to the opto is called **Ext. Trip 3Ph**, DDB 610.

Note: When in Commissioning test mode the CB condition monitoring counters will not be updated.

2.11 Circuit breaker control

The relay includes the following options for control of a single circuit breaker:

- Local tripping and closing, via the relay menu.
- Local tripping and closing, via relay opto-isolated inputs.
- Remote tripping and closing, using the relay communications.

It is recommended that separate relay output contacts are allocated for remote circuit breaker control and protection tripping. This enables the control outputs to be selected via a local/remote selector switch as shown in Figure 109. Where this feature is not required the same output contact(s) can be used for both protection and remote tripping.

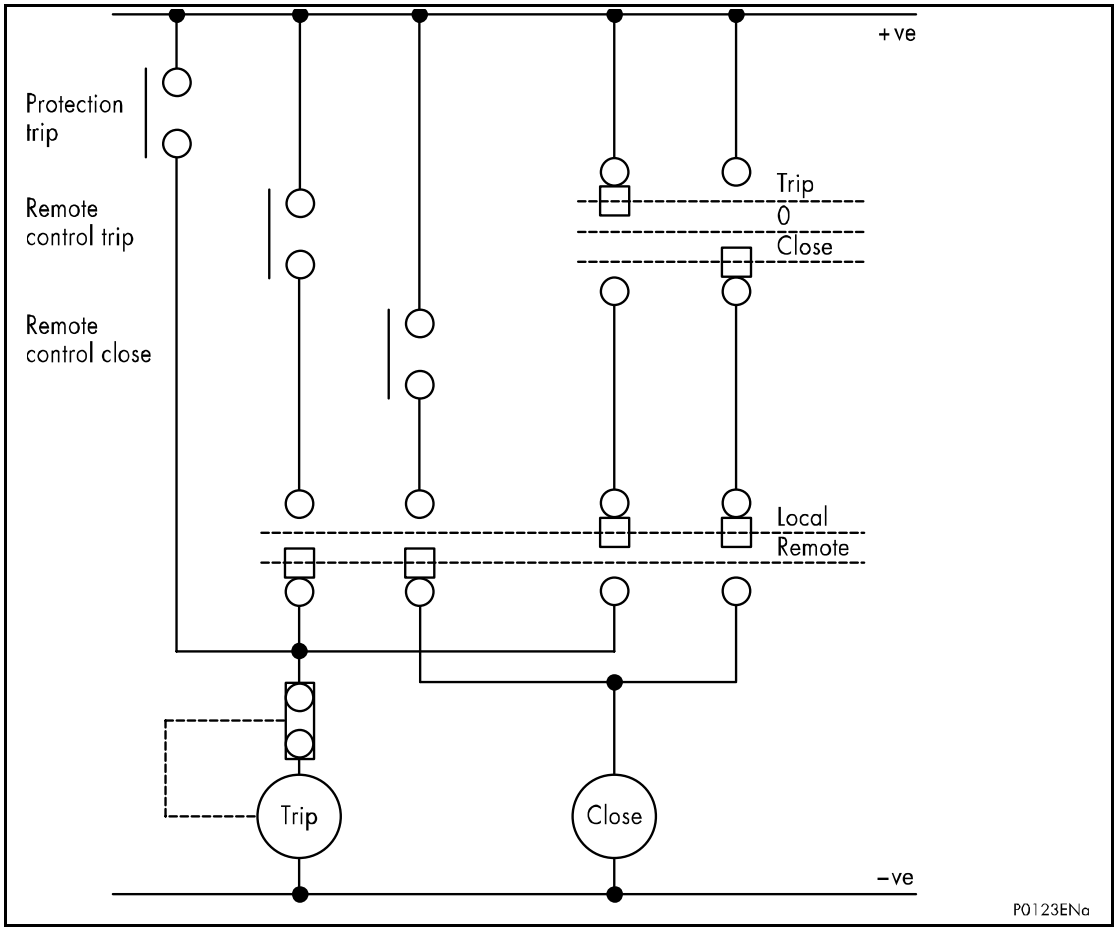


Figure 109: Remote control of circuit breaker

The following table is taken from the relay menu and shows the available settings and commands associated with circuit breaker control. Depending on the relay model some of the cells may not be visible:

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CB control				
CB control by	Disabled	Disabled, Local, Remote, Local+Remote, Opto, Opto+Local, Opto+Remote, Opto+Rem+Local		
Close Pulse Time	0.5 s	0.01 s	10 s	0.01 s
Trip Pulse Time	0.5 s	0.01 s	5 s	0.01 s
Man Close Delay	10 s	0.01 s	600 s	0.01 s
CB Healthy Time	5 s	0.01 s	9999 s	0.01 s
Sys Check Time	5 s	0.01 s	9999 s	0.01 s
Lockout Reset	No	No, Yes		
Reset Lockout By	CB Close	User Interface, CB Close		
Man Close RstDly	5 s	0.01 s	600 s	0.01 s
CB Status Input	None	None, 52A, 52B, Both 52A and 52B		

Table 32: CB control settings

A manual trip will be permitted provided that the circuit breaker is initially closed. Likewise, a close command can only be issued if the CB is initially open. To confirm these states it will be necessary to use the breaker 52A and/or 52B contacts (the different selection options are given from the **CB Status Input** cell above). If no CB auxiliary contacts are available then this cell should be set to **None**. Under these circumstances no CB control (manual or auto) will be possible.

Once a CB Close command is initiated the output contact can be set to operate following a user defined time delay (**Man Close Delay**). This would give personnel time to move away from the circuit breaker following the close command. This time delay will apply to all manual CB Close commands.

The length of the trip or close control pulse can be set via the **Trip Pulse Time** and **Close Pulse Time** settings respectively. These should be set long enough to ensure the breaker has completed its open or close cycle before the pulse has elapsed.

Note: The manual close commands are found in the **SYSTEM DATA** column and the hotkey menu.

If an attempt to close the breaker is being made, and a protection trip signal is generated, the protection trip command overrides the close command.

Where the check synchronism function is set, this can be enabled to supervise manual circuit breaker close commands. A circuit breaker close output will only be issued if the check synchronism criteria are satisfied. A user settable time delay is included (**Sys Check Time**) for manual closure with check synchronizing. If the check sync. criteria are not satisfied in this time period following a close command the relay will lockout and alarm (DDB 403 – Man No Check Synch, DDB 1362 – Man Check Synch).

In addition to a synchronism check before manual re-closure there is also a CB Healthy check if required. This facility accepts an input to one of the relays opto-isolators to indicate that the breaker is capable of closing (circuit breaker energy for example). A user settable time delay is included **CB Healthy Time** for manual closure with this check. If the CB does not indicate a healthy condition in this time period following a close command then the relay will lockout and alarm (DDB 369 – Man CB Unhealthy).

If the CB fails to respond to the control command (indicated by no change in the state of CB Status inputs) a **CB Failed to Trip** or **CB Failed to Close** alarm will be generated after the relevant trip or close pulses have expired. These alarms can be viewed on the relay LCD display, remotely via the relay communications, or can be assigned to operate output contacts for annunciation using the relays programmable scheme logic (PSL).

The **Lockout Reset** and **Reset Lockout** by setting cells in the menu are applicable to CB Lockouts associated with manual circuit breaker closure, CB Condition monitoring (Number of circuit breaker operations, for example).

The lockout alarms can be reset using the **Lockout Reset** command or the by pressing the Clear key after reading the alarm or by closing the CB if the **Reset Lockout By** setting is set to **CB Close** or via an opto input using DDB 690, Reset Lockout. If lockout is reset by closing the CB then there is a time delay after closing the CB to resetting of lockout, the **Man Close RstDly**.

2.11.1 CB control using “hotkeys”

The hotkeys allow direct access to the manual trip and close commands without the need to enter the SYSTEM DATA column. The CB trip and close functionality via the hotkey menu is identical to that of the SYSTEM DATA menu.

IF <<TRIP>> or <<CLOSE>> is selected the user is prompted to confirm the execution of the relevant command. If a trip is executed a screen with the CB status will be displayed once the command has been completed. If a close is executed a screen with a timing bar will appear while the command is being executed. This screen has the option to cancel or restart the close procedure. The timer used is taken from the manual close delay timer setting in the CB Control menu. When the command has been executed, a screen confirming the present status of the circuit breaker is displayed. The user is then prompted to select the next appropriate command or exit – this will return to the default relay screen.

If no keys are pressed for a period of 25 seconds while waiting for the command confirmation, the relay will revert to showing the CB Status. If no key presses are made for a period of 25 seconds while displaying the CB status screen, the relay will revert to the default relay screen. Figure 110 shows the hotkey menu associated with CB control functionality.

To avoid accidental operation of the trip and close functionality, the hotkey CB control commands will be disabled for 10 seconds after exiting the hotkey menu.

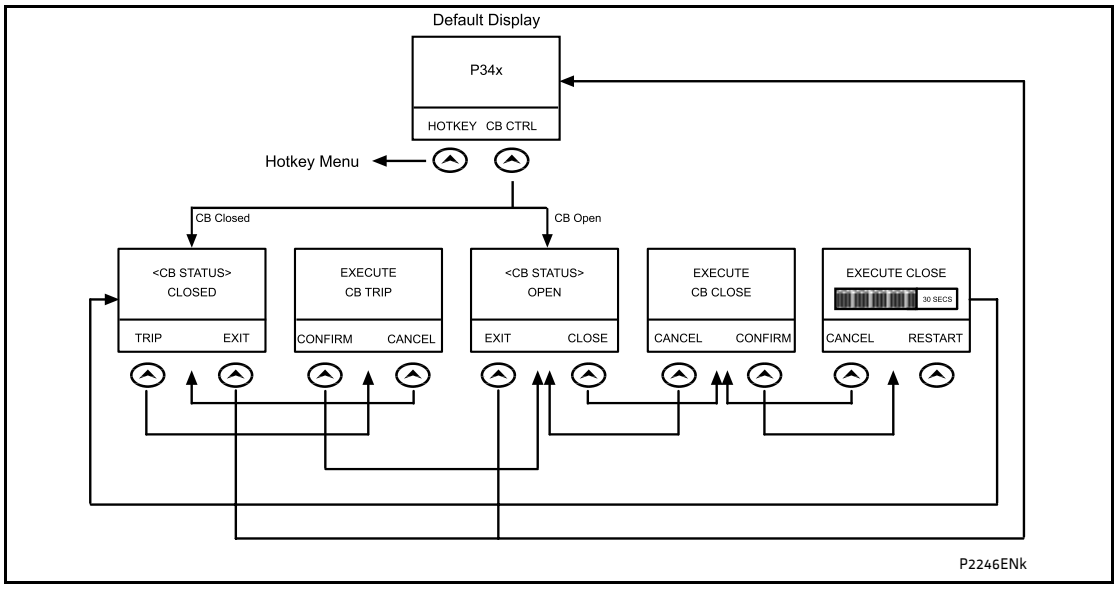


Figure 110: CB control hotkey menu

2.12 Changing setting groups

The setting groups can be changed either via 2 DDB signals or via a menu selection selection or via the hotkey menu. In the Configuration column if **Setting Group - select via DDB** is selected then DDBs 676 (SG Select 1x) and 675 (SG Select x1), which are dedicated for setting group selection, can be used to select the setting group as shown in the table below. These DDB signals can be connected to opto inputs for local selection or control inputs for remote selection of the setting groups. If **Setting Group - select via menu** is selected then in the Configuration column the **Active Settings - Group1/2/3/4** can be used to select the setting group. The setting group can be changed via the hotkey menu providing **Setting Group select via menu** is chosen.

SG select 1x	SG select x1	Selected setting group
0	0	1
1	0	2
0	1	3
1	1	4

Table 33: Setting group selection logic

Note: Setting groups comprise both Settings and Programmable Scheme Logic. Each is independent per group - not shared as common. The settings are generated in the Settings and Records application within S1 Studio, or can be applied directly from the relay front panel menu. The programmable scheme logic can only be set using the PSL Editor application within S1 Studio, generating files with extension ".psl".

It is essential that where the installation needs application-specific PSL that the appropriate PSL file is downloaded (sent) to the relay, for each and every setting group that will be used. If the user fails to download the required PSL file to any setting group that may be brought into service, then factory default PSL will still be resident. This may have severe operational and safety consequences.

2.13 Control inputs

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function that they are connected to as part of the PSL. There are three setting columns associated with the control inputs which

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are: **CONTROL INPUTS**, **CTRL I/P CONFIG** and **CTRL I/P LABELS**. The function of these columns is described in the following table:

Menu text	Default setting	Setting range	Step size
CONTROL INPUTS			
Ctrl I/P Status	00000000000000000000000000000000		
Control Input 1	No Operation	No Operation, Set, Reset	
Control Input 2 to 32	No Operation	No Operation, Set, Reset	

Table 34: Control inputs

The Control Input commands can be found in the **Control Input** menu. In the **Ctrl I/P status** menu cell there is a 32 bit word which represent the 32 control input commands. The status of the 32 control inputs can be read from this 32 bit word. The 32 control inputs can also be set and reset from this cell by setting a 1 to set or 0 to reset a particular control input. Alternatively, each of the 32 Control Inputs can be set and reset using the individual menu setting cells **Control Input 1, 2, 3**, etc. The Control Inputs are available through the relay menu as described above and also via the rear communications.

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In the programmable scheme logic editor 32 Control Input signals, DDB 1152 - 1183, which can be set to a logic 1 or On state, as described above, are available to perform control functions defined by the user.

The status of the Control Inputs are held in non-volatile memory (battery backed RAM) such that when the relay is power-cycled, the states are restored n power-up.

Menu text	Default setting	Setting range	Step size
CTRL I/P CONFIG			
Hotkey Enabled	11111111111111111111111111111111		
Control Input 1	Latched	Latched, Pulsed	
Ctrl Command 1	SET/RESET	SET/RESET, IN/OUT, ENABLED/DISABLED, ON/OFF	
Control Input 2 to 32	Latched	Latched, Pulsed	
Ctrl Command 2 to 32	SET/RESET	SET/RESET, IN/OUT, ENABLED/DISABLED, ON/OFF	

Table 35: Control input configuration

Menu text	Default setting	Setting range	Step size
CTRL I/P LABELS			
Control Input 1	Control Input 1	16 character text	
Control Input 2 to 32	Control Input 2 to 32	16 character text	

Table 36: Control input labels

The **CTRL I/P CONFIG** column has several functions one of which allows the user to configure the control inputs as either **latched** or **pulsed**. A latched control input will remain in the set state until a reset command is given, either by the menu or the serial communications. A pulsed control input, however, will remain energized for 10 ms after the set command is given and will then reset automatically (i.e. no reset command required).

In addition to the latched/pulsed option this column also allows the control inputs to be individually assigned to the "Hotkey" menu by setting '1' in the appropriate bit in the **Hotkey Enabled** cell. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the **CONTROL INPUTS** column. The **Ctrl Command** cell also allows the **SET/RESET** text, displayed in the hotkey menu, to be changed to something more suitable for the application of an individual control input, such as **ON/OFF**, **IN/OUT** etc.

The **CTRL I/P LABELS** column makes it possible to change the text associated with each individual control input. This text will be displayed when a control input is accessed by the hotkey menu, or it can be displayed in the PSL.

Note: With the exception of pulsed operation, the status of the control inputs is stored in battery backed memory. In the event that the auxiliary supply is interrupted the status of all the inputs will be recorded. Following the restoration of the auxiliary supply the status of the control inputs, prior to supply failure, will be reinstated. If the battery is missing or flat the control inputs will set to logic 0 once the auxiliary supply is restored.

2.14 PSL DATA column

The P34x range of relays contains a PSL DATA column that can be used to track PSL modifications. A total of 12 cells are contained in the PSL DATA column, 3 for each setting group. The function for each cell is shown below:

Grp PSL Ref	When downloading a PSL to the relay, the user will be prompted to enter which groups the PSL is for and a reference ID. The first 32 characters of the reference ID will be displayed in this cell. The ◊ and ◊ keys can be used to scroll through 32 characters as only 16 can be displayed at any one time.
18 Nov 2002 08:59:32.047	This cell displays the date and time when the PSL was down loaded to the relay.
Grp 1 PSL ID – 2062813232	This is a unique number for the PSL that has been entered. Any change in the PSL will result in a different number being displayed.

Note: The above cells are repeated for each setting group.

2.15 Auto reset of trip LED indication

The trip LED can be reset when the flags for the last fault are displayed. The flags are displayed automatically after a trip occurs, or can be selected in the fault record menu. The reset of trip LED and the fault records is performed by pressing the □key once the fault record has been read.

Setting **Sys Fn Links** (SYSTEM DATA Column) to logic "1" sets the trip LED to automatic reset. Resetting will occur when the circuit is reclosed and the **Any Pole Dead** signal (DDB 1045) has been reset for three seconds. Resetting, however, will be prevented if the **Any start** signal is active after the breaker closes.

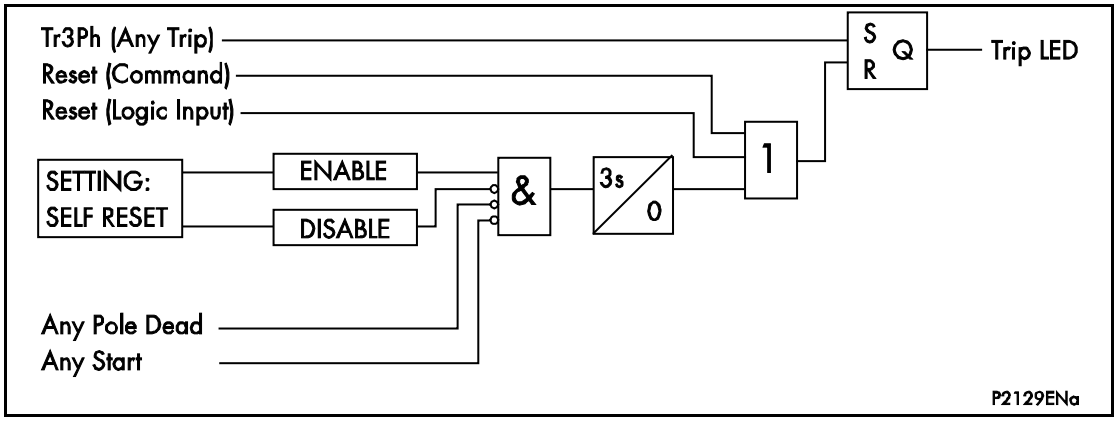


Figure 111: Trip LED logic diagram

2.16 Reset of programmable LEDs and output contacts

The programmable LEDs and output contacts can be set to be latched in the programmable scheme logic. If there is a fault record then clearing the fault record by pressing the □key once the fault record has been read will clear any latched LEDs and output contacts. If there is no fault record, then as long as the initiating signal to the LED or output contact is reset the LEDs and contacts can be reset by one of the two following methods.

1. Via the **View Records - Reset Indications** menu command cell
2. Via DDB 616 'Reset Relays/LED' which can be mapped to an Opto Input or a Control Input for example

2.17 Real time clock synchronization via opto-inputs

In modern protective schemes it is often desirable to synchronize the relays real time clock so that events from different relays can be placed in chronological order. This can be done using the IRIG-B input, if fitted, or via the communication interface connected to the substation control system. In addition to these methods the P34x range offers the facility to synchronize via an opto-input by routing it in PSL to DDB 621 (Time Sync.). Pulsing this input will result in the real time clock snapping to the nearest minute if the pulse input is ± 3 s of the relay clock time. If the real time clock is within 3 s of the pulse the relay clock will crawl (the clock will slow down or get faster over a short period) to the correct time. The recommended pulse duration is 20 ms to be repeated no more than once per minute. An example of the time sync. function is shown below:

Time of "sync. pulse"	Corrected time
19:47:00 to 19:47:29	19:47:00
19:47:30 to 19:47:59	19:48:00

Table 37: Time sync example

Note: The above assumes a time format of hh:mm:ss

To avoid the event buffer from being filled with unnecessary time sync. events, it is possible to ignore any event that generated by the time sync. opto input. This can be done by applying the following settings:

Menu text	Value
RECORD CONTROL	
Opto Input Event	Enabled
Protection Event	Enabled
DDB 63 - 32 (Opto Inputs)	Set "Time Sync." associated opto to 0

Table 38: Event filtering of time sync signal

To improve the recognition time of the time sync. opto input by approximately 10 ms, the opto input filtering could be disabled. This is achieved by setting the appropriate bit to 0 in the **Opto Filter Cntl** cell (OPTO CONFIG column).

Disabling the filtering may make the opto input more susceptible to induced noise. Fortunately the effects of induced noise can be minimized by using the methods described in section 2.3.3 of the Firmware Design chapter (*P34x/EN FD*).

2.18 Any trip

The **Any Trip** DDB (DDB674) has been made independent from Relay 3 in the version 32 software. In Previous versions of software the **Any Trip** signal was the operation of Relay 3. In the version 32 software DDB626 is the **Any Trip** signal and any output contact used for tripping can be connected to the **Any Trip** DDB leaving Relay 3 to be freely assigned for any function. The **Any Trip** signal affects the following functions:

- Operates the Trip LED
- Triggers CB condition maintenance counters
- Used to measure the CB operating time
- Triggers the circuit breaker failure logic
- Used in the Fault recorder logic

In the default PSL, Relay 3 is still mapped to the **Any Trip** DDB and the **Fault REC TRIG** DDB signals. If the user wants to make use of the CB maintenance features, CB failure function etc they should map the output contact(s) assigned for tripping the monitored circuit breaker to the **Any Trip** DDB. The output contact(s) assigned for tripping the monitored circuit breaker should also be connected to the fault record trigger **Fault REC TRIG** DDB 623 for fault record triggering.

Where relay 3 or any other contact is used to initiate the **Any Trip** signal the contact should not be set to latched as the **Any Trip** is used to trigger (on pick-up) and reset (on drop-off) the fault recorder window. So if the **Any Trip** is latched the fault recording window never resets and so you won't see a fault record on the relay front display as the relay thinks the fault is still present.

The default setting for relay 3 is a dwell time of 100 ms, a dwell is the minimum time the contact will be ON and is used for trip functions to ensure a good quality trip signal is obtained. As an example of a dwell timer, a dwell of 100 ms means that if the initiating signal is ON for 10 ms then the output contact is ON for 100 ms and if the initiating signal is ON for 200 ms then the output contact is ON for 200 ms.

2.19 Function keys (P343/4/5/6)

The P343/4/5/6 relay offers users 10 function keys for programming any operator control functionality such as Reset latched Relays/LEDS/Alarms, Select Group 2 etc. via PSL. Each function key has an associated programmable tri-color LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands can be found in the **Function Keys** menu (see Settings chapter, *P34x/EN ST*). In the 'Fn. Key Status' menu cell there is a 10 bit word which represent the 10 function key commands and their status can be read from this 10 bit word.

In the programmable scheme logic editor 10 function key signals, DDB 256 - 265, which can be set to a logic 1 or On state, as described above, are available to perform control functions defined by the user.

The **Function Keys** column has the **Fn Key n Mode** cell which allows the user to configure the function key as either 'Toggled' or 'Normal'. In the 'Toggle' mode the function key DDB signal output will remain in the set state until a reset command is given, by activating the function key on the next key press. In the 'Normal' mode, the function key DDB signal will remain energized for as long as the function key is pressed and will then reset automatically. A minimum pulse duration can be programmed for a function key by adding a minimum pulse timer to the function key DDB output signal.

The **Fn Key n Status** cell is used to enable/unlock or disable the function key signals in PSL. The **Lock** setting has been specifically provided to allow the locking of a function key therefore preventing further activation of the key on consequent key presses.

This allows function keys that are set to **Toggled** mode and their DDB signal active 'high', to be locked in their active state thus preventing any further key presses from deactivating the associated function. Locking a function key that is set to the **Normal** mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical relay functions.

The **Fn Key Labels** cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of the function keys is stored in battery backed memory. In the event that the auxiliary supply is interrupted the status of all the function keys will be recorded. Following the restoration of the auxiliary supply the status of the function keys, prior to supply failure, will be reinstated. If the battery is missing or flat the function key DDB signals will set to logic 0 once the auxiliary supply is restored. Please also note the relay will only recognize a single function key press at a time and that a minimum key press duration of approximately 200 msec. is required before the key press is recognized in PSL. This deglitching feature avoids accidental double presses.

2.20 Read only mode

With IEC 61850 and Ethernet/Internet communication capabilities, security has become a pressing issue. The Px40 relay provides a facility to allow the user to enable or disable the change in configuration remotely. This feature is available only in relays with Courier, Courier with IEC 60870-5-103, Courier with IEC 61850 and IEC 61850 protocol options. In IEC 60870-5-103 protocol, Read Only Mode function is different from the existing Command block feature.

Read Only mode can be enabled/disabled for the following rear ports:

- Rear Port 1 – IEC 60870-5-103 and Courier protocols
- Rear Port 2 (if fitted) - Courier protocol
- Ethernet Port (if fitted) - Courier protocol (“tunneled”)

AP

APPLICATION NOTES

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

AP

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1 INTRODUCTION

1.1 Protection of generators

An ac generator forms the electromechanical stage of an overall energy conversion process that results in the production of electrical power. A reciprocating engine, or one of many forms of turbine, is a prime mover to provide the rotary mechanical input to the alternator.

There are many forms of generating plant that use different sources of energy such as combustion of fossil fuels, hydro dams and nuclear fission. Generation schemes may be provided for base-load production, peak-lopping or for providing standby power.

Electrical protection should quickly detect and initiate shutdown for major electrical faults associated with the generating plant. Electrical protection can also detect abnormal operating conditions which may lead to plant damage.

Abnormal electrical conditions can be caused by a result of a failure in the generating plant, but can also be externally imposed on the generator. Common categories of faults and abnormal conditions that can be detected electrically are listed as follows: (Not all conditions have to be detected for all applications.)

Major electrical faults

- Insulation failure of stator windings or connections

Secondary electrical faults

Insulation failure of excitation system

- Failure of excitation system
- Unsynchronized over voltage
- Abnormal prime mover or control conditions

Failure of prime mover

- Overfrequency
- Overfluxing
- Dead machine energization
- Breaker flashover
- System related
- Feeding an uncleared fault
- Prolonged or heavy unbalanced loading
- Prolonged or heavy overload
- Loss of synchronism
- Overfrequency
- Underfrequency
- Synchronized over voltage
- Overfluxing
- Undervoltage

In addition various types of mechanical protection may be necessary, such as vibration detection, lubricant and coolant monitoring, and temperature detection.

The action required following response of an electrical or mechanical protection is often categorized as follows:

- Urgent shutdown
- Non-urgent shutdown
- Alarm only

An urgent shutdown would be required, for example, if a phase to phase fault occurred within the generator electrical connections. A non-urgent shutdown might be sequential, where the prime mover may be shutdown prior to electrically unloading the generator, in order to avoid over speed. A non-urgent shutdown may be initiated in the case of continued unbalanced loading. In this case, it is desirable that an alarm should be given before shutdown becomes necessary, to allow for operator intervention to remedy the situation.

For urgent tripping, it may be desirable to electrically maintain the shutdown condition with latching protection output contacts, which would require manual resetting. For a non-urgent shutdown, it may be required that the output contacts are self-reset, so that production of power can be re-started as soon as possible.

The P342/3/4/5/6 is able to maintain all protection functions in service over a wide range of operating frequency due to its frequency tracking system (5 - 70 Hz). The P342/3/4/5/6 frequency tracking capability is of particular interest for pumped storage generation schemes, where synchronous machines can be operated from a variable frequency supply when in pumping mode. Additionally, in the case of combined cycle generating plant, it may be necessary to excite and synchronize a steam turbine generating set with a gas turbine set at low frequency, prior to running up to nominal frequency and synchronizing with the power system.

When the P342/3/4/5/6 protection functions are required to operate accurately at low frequency, it will be necessary to use CTs with larger cores. In effect, the CT requirements need to be multiplied by fn/f, where f is the minimum required operating frequency and fn is the nominal operating frequency.

1.2 Protection of generator-transformers

1.2.1 Introduction

The development of modern power systems has been reflected in the advances in transformer design. This has resulted in a wide range of transformers with sizes from a few kVA to several hundred MVA being available for use in a wide variety of applications.

The considerations for transformer protection vary with the application and importance of the transformer. To reduce the effects of thermal stress and electrodynamic forces it is advisable for the overall protection to minimize the time that a fault is present within a transformer.

On smaller transformers, effective and economically justifiable protection can be achieved by using either fuse protection or IDMT/instantaneous overcurrent relays. Due to the requirements of coordination with the downstream power system protection this results in time delayed fault clearance for some low-level faults. Time delayed clearance of major faults is unacceptable on larger distribution, transmission and generator transformers, where the effects on system operation and stability must be considered. High speed protection is desirable for all faults.

Transformer faults are generally classified into four categories:

- Winding and terminal faults
- Core faults
- Abnormal operating conditions such as overvoltage, overfluxing and overload
- Sustained or uncleared external faults

All of the above conditions must be considered individually and the transformer protection designed accordingly.

To provide effective protection for faults within a transformer and security for normal operation and external faults, the design and application of transformer protection must consider factors such as:

- Magnetizing inrush current
- Winding arrangements
- Winding connections
- Connection of protection secondary circuits

The way that the protection of larger transformers is typically achieved is best shown by examining the protective devices associated with common applications.

1.2.2 Transformer connections

There are several possible transformer connections but the more common connections are divided into four main groups:

Group 1	0° Phase displacement	Yy0
		Zd0
		Dd0
Group 2	180° Phase displacement	Yd6
		Dd6
		Dz6
Group 3	30° lag Phase displacement	Dy1
		Yz1
		Yz1
Group 4	30° lead Phase displacement	Yd11
		Dy11
		Yz11

High voltage windings are indicated by capital letters and low voltage windings by lower case letters (reference to high and low is relative). The numbers refer to positions on a clock face and indicate the phase displacement of the low voltage phase to neutral vector with respect to the high voltage phase to neutral vector, for example, Yd1 indicates that the low voltage phase vectors lag the high voltage phase vectors by 30° (-30° phase shift).

Determining transformer connections is best shown with a particular example. The following points should be noted:

The line connections are normally made to the end of the winding which carries the subscript 2, such as: A2, B2, C2 and a2, b2, c2.

The line terminal designation (both letter and subscript) are the same as those of the phase winding to which the line terminal is connected.

Consider the Yd1 connection. The transformer windings shown in Figure 1 should be connected in Yd1 configuration.

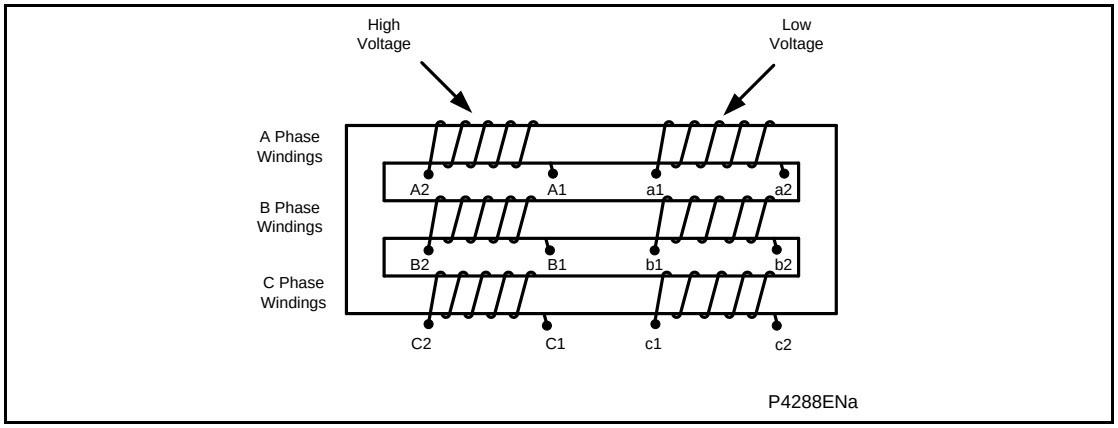


Figure 1: Transformer windings to be connected in Yd1 configuration

The following steps may be followed to connect the transformer windings:

1. Draw the primary and secondary phase to neutral vectors showing the required phase displacement.

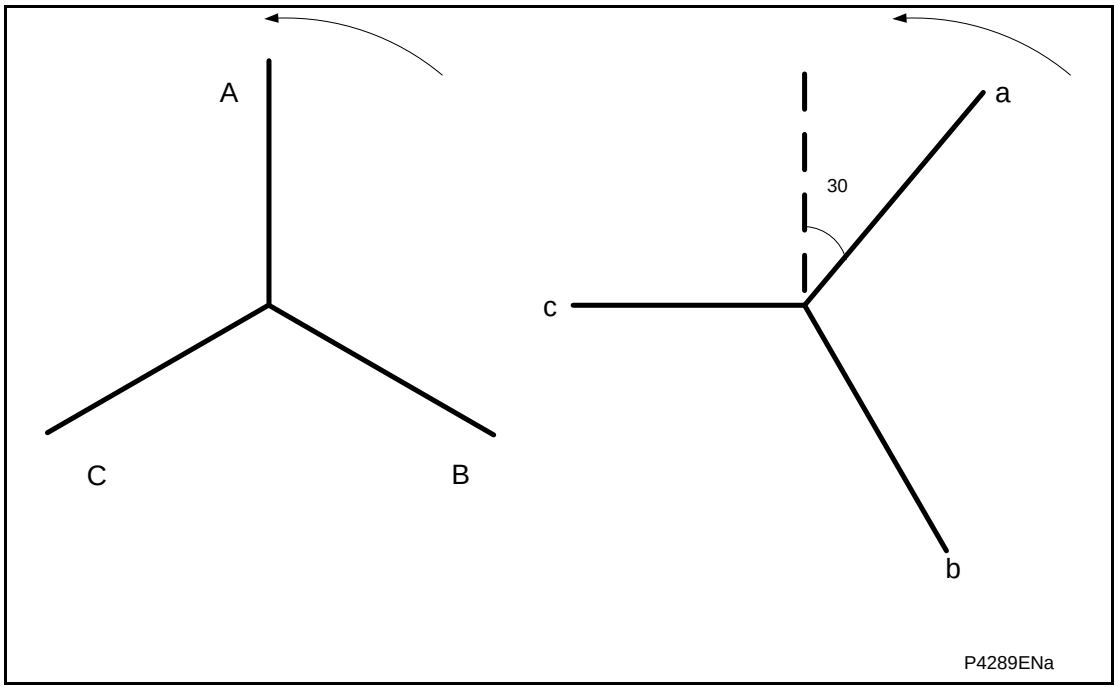


Figure 2: Phase-neutral voltage vectors

2. Complete the delta winding connection on the secondary side and indicate the respective vector directions. Magnetically coupled windings are drawn in parallel, winding “A” in the star side is parallel to winding “a” in the delta side. The same applies for the other two phases.

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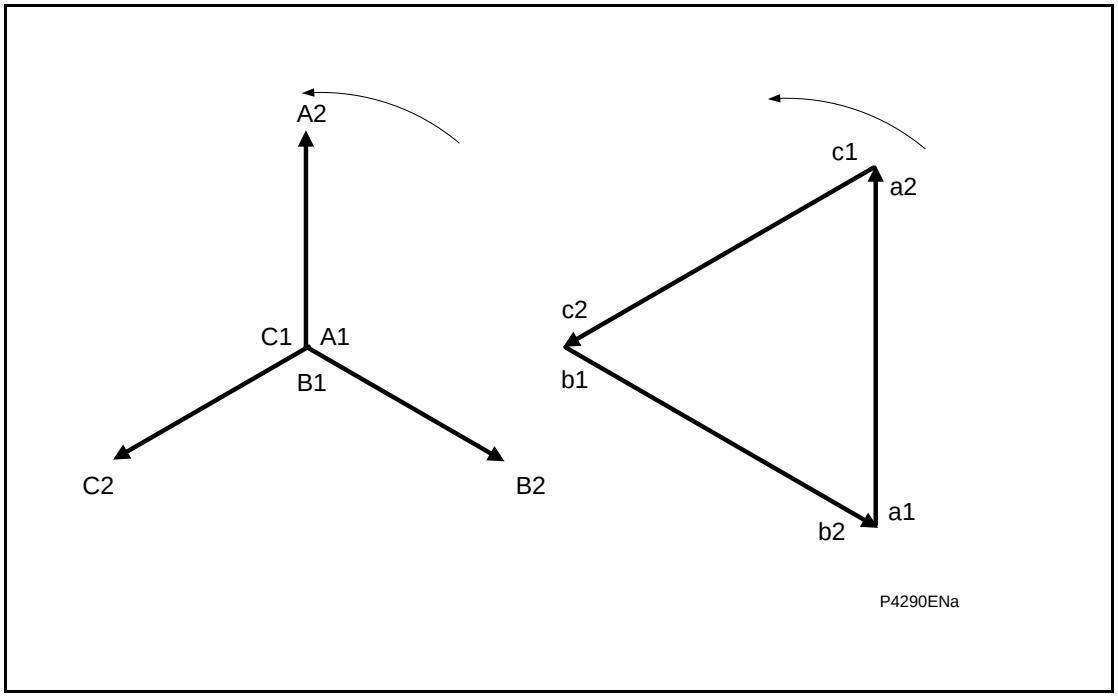


Figure 3: Draw the delta

3. It is now possible to indicate the winding subscript numbers bearing in mind that if the direction of induced voltage in the high voltage winding at a given instant is from A1 to A2 (or vice versa) then the direction of the induced voltage in the low voltage winding at the same instant will also be from a1 to a2.
4. The delta connection should be made by connecting a2 to c1, b2 to a1 and c2 to b1:

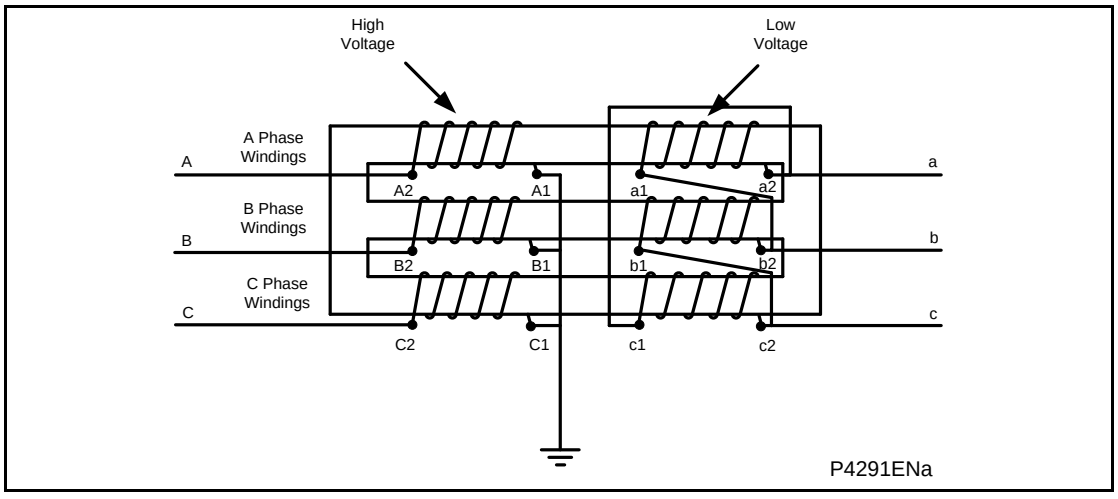


Figure 4: Yd1 transformer configuration

1.2.3 Generator-transformer example

Figure 5 shows typical protection functions for a generator-transformer.

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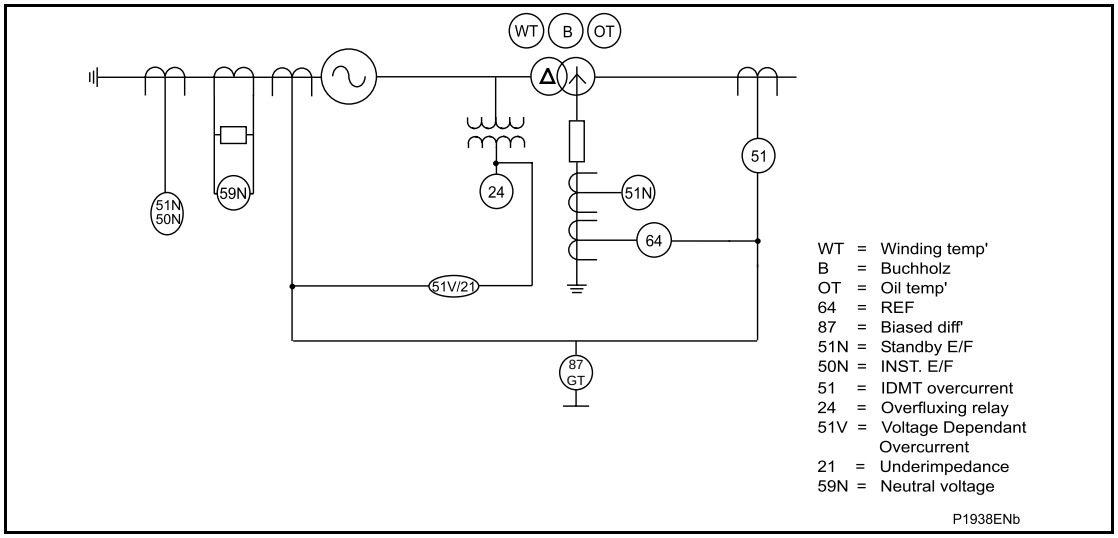


Figure 5: Typical protection package for a generator-transformer

High speed protection is provided for faults on both the HV and LV windings by biased differential protection (87). The relay operates on the basic differential principle that HV and LV CT secondary currents entering and leaving the zone of protection can be balanced under load and through fault conditions, whereas under internal fault conditions balance will be lost and a differential current will cause the relay to trip. The zone of protection is clearly defined by the CT locations and, as the protection is stable for through faults, it can be set to operate without any intentional time delay.

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The application of the P34x differential relay includes software vector group and amplitude matching to provide phase and ratio correction of CT signals in addition to filtering HV zero sequence current to prevent maloperation of the differential element for external HV earth faults. Interposing CTs (ICTs) are no longer required.

More sensitive high speed earth fault protection for the HV star winding is provided by restricted earth fault protection (64). Due to the limitation of phase fault current on the LV side for HV winding earth faults and the fact that any unrestricted earth fault protection in the transformer earth path requires a discriminative time delay, restricted earth fault protection is widely applied.

Earth fault protection is provided on the LV winding and generator by the inherently restricted earth fault protection on the generator. This could be neutral voltage (59N) or current based earth fault protection (50 N) depending on how the generator is earthed. The delta winding of the transformer draws no LV zero sequence current for HV earth faults, hence there is no requirement to grade this element with other earth fault protection and it can be set to operate without any intentional time delay. For delta windings this is known as balanced earth fault protection.

Sustained external HV faults are cleared by the IDMT overcurrent protection (51) on the HV winding or IDMT voltage dependent overcurrent protection or underimpedance protection on the LV winding/generator (51 V/21) or by the standby earth fault protection (51N) in the transformer HV earth connection. The extent of backup protection used will vary according to the transformer installation and application.

Overfluxing protection (24) is commonly applied to generator circuits to prevent generator or transformer damage from prolonged overfluxing conditions.

The protection scheme may be further enhanced by the use of other protective devices associated with the transformer, such as the Buchholz, pressure relief and winding temperature devices. These devices can act as another main protective system for large transformers and they may also provide clearance for some faults which might be difficult to detect by protection devices operating from line current transformers, for example, winding inter turn faults or core lamination faults. These devices are connected to directly trip the breaker in addition to operating auxiliary relays for indication purposes.

Other protection devices will again complement the main relay protection.

2 APPLICATION OF INDIVIDUAL PROTECTION FUNCTIONS

The following sections detail the individual protection functions in addition to where and how they may be applied. Each section also gives an extract from the respective menu columns to demonstrate how the settings are actually applied to the relay.

All the phase current based protection functions (overcurrent, power, impedance protection) use the IA/IB/IC 3 phase current inputs which are connected to the neutral end CTs in the standard connection diagrams except for the high impedance differential and interturn protection which use the IA-2/IB-2/IC-2 current inputs. The overcurrent, restricted earth fault, NPS overcurrent, dead machine protection and CB Fail undercurrent elements can use the IA/IB/IC or IA-2/IB-2/IC-2 current inputs selectable in the settings. The biased differential protection uses both sets of 3 phase current inputs.

2.1 Phase rotation

2.1.1 Description

A facility is provided in the P340 to maintain correct operation of all the protection functions even when the generator is running in a reverse phase sequence. This is achieved through user configurable settings available for the four setting groups.

The default phase sequence for P340 is the clockwise rotation ABC. Some power systems may have a permanent anti-clockwise phase rotation of ACB. In pump storage applications there is also a common practice to reverse two phases to facilitate the pumping operation, using phase reversal switches. However, depending on the position of the switches with respect to the VTs and CTs, the phase rotation may not affect all the voltage and current inputs to the relay. The following sections describe some common scenarios and their effects. In the description, CT1 provides current measurements for all the current based protection (IA-1/IB-1/IC-1), CT2 (IA-2/IB-2/IC-2) is used for the generator differential protection only.

For pump storage applications the correct phase rotation settings can be applied for a specific operating mode and phase configuration in different setting groups. The phase configuration can then be set by selecting the appropriate setting group, see section 2.6 of *P34x/EN OP* for more information of changing setting groups. This method of selecting the phase configuration removes the need for external switching of CT circuits or the duplication of relays with connections to different CT phases. The phase rotation settings should only be changed when the machine is off-line so that transient differences in the phase rotation between the relay and power system due to the switching of phases don't cause operation of any of the protection functions. To ensure that setting groups are only changed when the machine is off-line the changing of the setting groups could be interlocked with the IA/IB/IC undercurrent start signals and an undervoltage start signal in the PSL.

2.1.1.1 Case 1 – phase reversal switches affecting all CTs and VTs

The phase reversal affects all the voltage and current measurements in the same way, irrespective of which two phases are being swapped. This is also equivalent to a power system that is permanently reverse phase reversed.

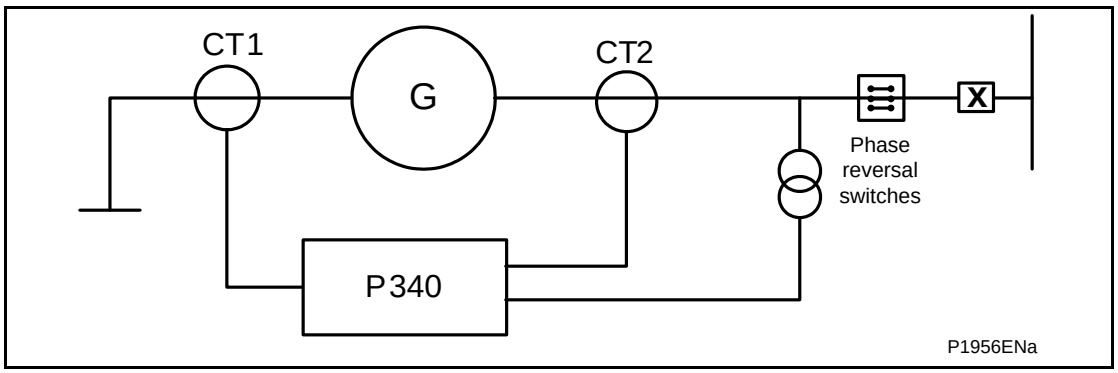


Figure 6: Case 1: Phase reversal switches affecting all CTs and VTs

All the protection functions that use the positive and negative sequence component of voltage and current will be affected (NPS overcurrent and NPS overvoltage, thermal overload, voltage transformer supervision). Directional overcurrent is also affected as the polarizing signal (Vbc, Vca, Vab) is reversed by the change in phase rotation. The generator differential protection is not affected, since the phase reversal applies to CT1 and CT2 in the same way.

The relationship between voltages and currents from CT1 for the standard phase rotation and reverse phase rotation are as shown below.

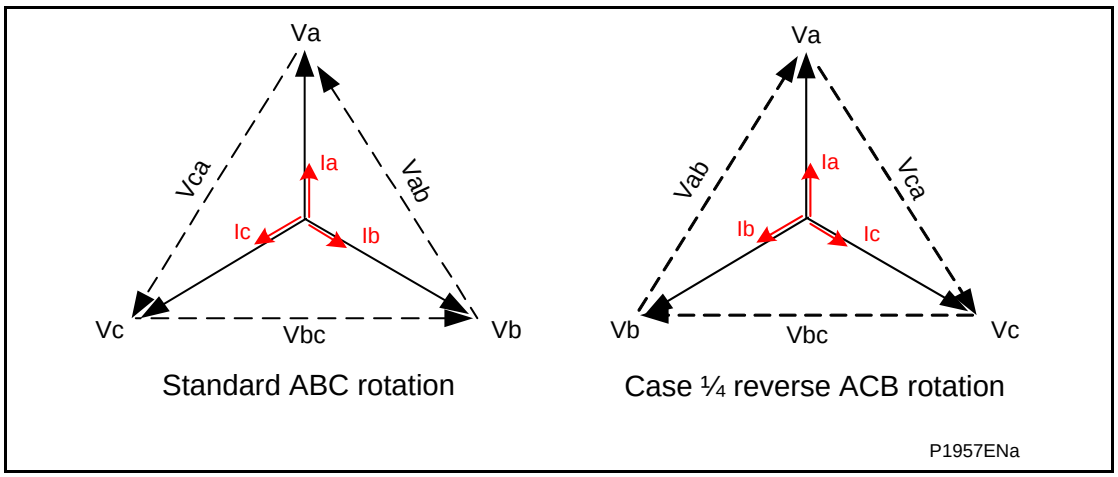


Figure 7: Standard and reverse phase rotation

In the above example, the System Config settings - Standard ABC and Reverse ACB can be used in 2 of the Setting Groups to affect the phase rotation depending on the position of the phase reversal switch.

2.1.1.2 Case 2 – phase reversal switches affecting CT1 only

The phase reversal affects CT1 only. All the protection functions that use CT1 currents and the 3 phase voltages (power, pole slipping, field failure, underimpedance, voltage controlled overcurrent, directional overcurrent) will be affected, since the reversal changes the phase relationship between the voltages and currents. The generator differential protection and protection that use positive and negative sequence current and voltage will also be affected.

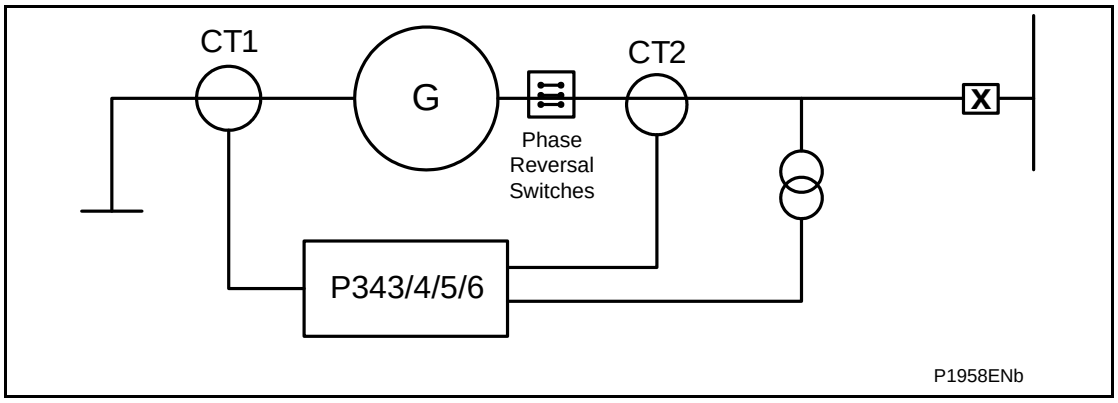


Figure 8: Case 2: Phase reversal switches affecting CT1 only

Note: There are 2 approaches to using the System Config settings where 2 phases are swapped. The settings can be used to maintain a generator view of the phase sequence or a system (or busbar) view of the phase sequence for a generator fault.

For example, in Case 2, for a generator A-phase winding fault, the relay will report a B phase fault if the **CT1 Reversal** setting is set to **A-B Swapped** (system or busbar view of faulted phase). For a busbar fault the correct faulted phase will be given in the fault record.

In the above example, instead of swapping A-B phase of CT1, the user can alternatively set **A-B Swapped** for **CT2 Reversal** and the **VT Reversal** and apply the **Phase Sequence** setting to **Reverse ACB**. With this approach, internal faults (e.g., A-phase winding fault) will give the correct phase information in the fault records (generator view of faulted phase), whereas an external A-phase fault will be presented as a B-phase fault.

So, to obtain a phase sequence maintaining a generator viewpoint for a generator fault the CTs/VTs not affected by the change must have the phase swapping setting to match the external switching. Also, since the machine's sequence rotation has been affected, the Sequence Reversal setting will also need to be applied accordingly.

To obtain a phase sequence maintaining a system viewpoint for a generator fault the CTs/VTs affected by the change must have the phase swapping setting to match the external switching.

The Sensitive Power is a single phase power element using A phase current and voltage. If Sensitive Power is applied and the A phase current only has been swapped, the power calculation will be wrong since the voltage and current inputs are not from the same phase. If for example in Case 2 the A-B phases are swapped and the sensitive CT is on the generator side of the switch. It is possible to use the alternative approach where the CT2 and VT phases are swapped so that the A-phase voltage (from generator's view point) is restored for the correct calculation of the A-phase power. This problem cannot be resolved with the other approach where only CT1 phases are swapped, therefore the protection will need to be disabled or the phase reversal switches arranged such that the A phase is not swapped or the sensitive power CT placed on the same side of the switch as the VT.

2.2 Generator differential protection (87G)

Failure of stator windings, or connection insulation, can result in severe damage to the windings and the stator core. The extent of the damage will depend on the fault current level and the duration of the fault. Protection should be applied to limit the degree of damage in order to limit repair costs. For primary generating plant, high-speed disconnection of the plant from the power system may also be necessary to maintain system stability.

For generators rated above 1 MVA, it is common to apply generator differential protection. This form of unit protection allows discriminative detection of winding faults, with no intentional time delay, where a significant fault current arises. The zone of protection, defined by the location of the CTs, should be arranged to overlap protection for other items of plant, such as a busbar or a step-up transformer.

Heavy through current, arising from an external fault condition, can cause one CT to saturate more than the other, resulting in a difference between the secondary current produced by each CT. It is essential to stabilize the protection for these conditions. Two methods are commonly used. A biasing technique, where the relay setting is raised as through current increases. Alternatively, a high impedance technique, where the relay impedance is such that under maximum through fault conditions, the current in the differential element is insufficient for the relay to operate.

The generator differential protection function available in the P343/4/5/6 relay can be used in either biased differential or high impedance differential mode. Both modes of operation are equally valid; users may have a preference for one over the other. The generator differential protection may also be used for interturn protection. The operating principle of each is described in the Operation chapter, *P34x/EN OP*.

2.2.1 Setting guidelines for biased generator differential protection

The differential setting, **Configuration - Differential**, should be set to **Enabled**. If the winding type in the **SYSTEM CONFIG - Winding Config** is set to **Generator**, then the settings related to Generator differential protection will be displayed in the column **DIFFERENTIAL - Generator Diff**.

To select biased differential protection the **Gen Diff Func** cell should be set to **Biased**.

The differential current setting, **Gen Diff Is1**, should be set to a low setting to protect as much of the machine winding as possible. A setting of 5% of rated current of the machine is generally considered to be adequate. **Gen Diff Is2**, the threshold above which the second bias setting is applied, should be set to 120% of the machine rated current.

The initial bias slope setting, **Gen Diff k1**, should be set to 0% to provide optimum sensitivity for internal faults. The second bias slope may typically be set to 150% to provide adequate stability for external faults.

Note: The default settings for **Gen Diff Is2** (1.2 In), **Gen Diff K1** (0%) and **Gen Diff K2** (150%) should always be used as the CT requirements are based on these settings.

2.2.2 Setting guidelines for high impedance generator differential protection

The differential setting, **Configuration - Differential**, should be set to **Enabled**. If the winding type in the **SYSTEM CONFIG - Winding Config** is set to **Generator**, then the settings related to Generator differential protection will be displayed in the column **DIFFERENTIAL - Generator Diff**.

To select high impedance differential protection the **Gen Diff Func** cell should be set to **High Impedance**.

The differential current setting, **Gen Diff Is1**, should be set to a low setting to protect as much of the machine winding as possible. A setting of 5% of rated current of the machine is generally considered to be adequate. This setting may need to be increased where low accuracy class CTs are used to supply the protection. A check should be made to ensure that the primary operating current of the element is less than the minimum fault current for which the protection should operate.

The primary operating current (Iop) will be a function of the current transformer ratio, the relay operating current (**Gen Diff Is1**), the number of current transformers in parallel with a relay element (n) and the magnetizing current of each current transformer (Ie) at the stability voltage (Vs). This relationship can be expressed in three ways:

1. To determine the maximum current transformer magnetizing current to achieve a specific primary operating current with a particular relay operating current.

$$I_e < \frac{1}{n} \times \left(\frac{I_{op}}{\text{CT ratio}} \text{ - Gen diff REF} > I_{s1} \right)$$

2. To determine the maximum relay current setting to achieve a specific primary operating current with a given current transformer magnetizing current.

$$\text{Gen diff } I_{s1} < \left(\frac{I_{op}}{\text{CT ratio}} - nI_e \right)$$

3. To express the protection primary operating current for a particular relay operating current and with a particular level of magnetizing current.

$$I_{op} = (\text{CT ratio}) \times (\text{Gen diff } I_{s1} + nI_e)$$

To achieve the required primary operating current with the current transformers that are used, a current setting (**Gen Diff Is1**) must be selected for the high impedance element, as detailed in expression (ii) above. The setting of the stabilizing resistor (RST) must be calculated in the following manner, where the setting is a function of the required stability voltage setting (Vs) and the relay current setting (**Gen Diff Is1**).

$$R_{ST} = \frac{Vs}{\text{Gen diff } I_{s1}} = \frac{1.5\, I_F\, (R_{CT} + 2_{RL})}{\text{Gen diff } I_{s1}}$$

Note: The above formula assumes negligible relay burden.

USE OF “METROSIL” NON-LINEAR RESISTORS

Metrosils are used to limit the peak voltage developed by the current transformers under internal fault conditions, to a value below the insulation level of the current transformers, relay and interconnecting leads, which are normally able to withstand 3000 V peak.

The following formulae should be used to estimate the peak transient voltage that could be produced for an internal fault. The peak voltage produced during an internal fault will be a function of the current transformer kneepoint voltage and the prospective voltage that would be produced for an internal fault if current transformer saturation did not occur. This prospective voltage will be a function of maximum internal fault secondary current, the current transformer ratio, the current transformer secondary winding resistance, the current transformer lead resistance to the common point, the relay lead resistance and the stabilizing resistor value.

$$V_p = 2\sqrt{2V_k (V_f - V_k)}$$

$$V_f = I'f (RCT + 2RL + RST)$$

Where:

V_p = Peak voltage developed by the CT under internal fault conditions.

V_k = Current transformer knee-point voltage.

V_f = Maximum voltage that would be produced if CT saturation did not occur.

I'_f = Maximum internal secondary fault current.

R_{CT} = Current transformer secondary winding resistance.

R_L = Maximum lead burden from current transformer to relay.

R_{ST} = Relay stabilizing resistor.

When the value given by the formulae is greater than 3000 V peak, Metrosils should be applied. They are connected across the relay circuit and serve the purpose of shunting the secondary current output of the current transformer from the relay to prevent very high secondary voltages.

Metrosils are externally mounted and take the form of annular discs. Their operating characteristics follow the expression:

$$V = CI^{0.25}$$

Where:

V = Instantaneous voltage applied to the non-linear resistor (“Metrosil”).

C = Constant of the non-linear resistor (“Metrosil”).

I = Instantaneous current through the non-linear resistor (“Metrosil”).

With a sinusoidal voltage applied across the Metrosil, the RMS current would be approximately 0.52x the peak current. This current value can be calculated as follows:

$$I(rms) = 0.52 \left(\frac{Vs\ (rms) \times \sqrt{2}}{C} \right)^4$$

Where:

Vs(rms) = rms value of the sinusoidal voltage applied across the Metrosil.

This is due to the fact that the current waveform through the non-linear resistor (“Metrosil”) is not sinusoidal but appreciably distorted.

For satisfactory application of a non-linear resistor ("Metrosil"), its characteristic should be such that it complies with the following requirements:

1. At the relay voltage setting, the non-linear resistor ("Metrosil") current should be as low as possible, but no greater than approximately 30 mA rms. for 1A current transformers and approximately 100 mA rms. for 5A current transformers.

2. At the maximum secondary current, the non-linear resistor ("Metrosil") should limit the voltage to 1500 V rms or 2120 V peak for 0.25 second. At higher relay voltage settings, it is not always possible to limit the fault voltage to 1500 V rms., so higher fault voltages may have to be tolerated.

The following tables show the typical Metrosil types that will be required, depending on relay current rating, REF voltage setting etc.

Metrosil Units for Relays with a 1 Amp CT

The Metrosil units with 1 Amp CTs have been designed to comply with the following restrictions:

3. At the relay voltage setting, the Metrosil current should less than 30 mA rms.
4. At the maximum secondary internal fault current the Metrosil unit should limit the voltage to 1500 V rms if possible.

The Metrosil units normally recommended for use with 1Amp CTs are shown in Table 1.

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Relay voltage setting	Nominal characteristic		Recommended Metrosil type	
	C	β	Single pole relay	Triple pole relay
Up to 125 V rms	450	0.25	600A/S1/S256	600A/S3/1/S802
125 to 300 V rms	900	0.25	600A/S1/S1088	600A/S3/1/S1195

Table 1: Recommended Metrosil types for 1A CTs

Note: Single pole Metrosil units are normally supplied without mounting brackets unless otherwise specified by the customer.

Metrosil Units for Relays with a 5 Amp CT

These Metrosil units have been designed to comply with the following requirements:

5. At the relay voltage setting, the Metrosil current should less than 100 mA rms (the actual maximum currents passed by the units shown below their type description.

6. At the maximum secondary internal fault current the Metrosil unit should limit the voltage to 1500 V rms for 0.25 secs. At the higher relay settings, it is not possible to limit the fault voltage to 1500 V rms hence higher fault voltages have to be tolerated (indicated by *, **, ***).

The Metrosil units normally recommended for use with 5 Amp CTs and single pole relays are as shown in the following table:

Secondary internal fault current	Recommended METROSIL type			
	Relay voltage setting			
Amps rms	Up to 200 V rms	250 V rms	275 V rms	300 V rms
50A	600A/S1/S1213 C = 540/640 35 mA rms	600A/S1/S1214 C = 670/800 40 mA rms	600A/S1/S1214 C = 670/800 50 mA rms	600A/S1/S1223 C = 740/870* 50 mA rms
100A	600A/S2/P/S1217 C = 470/540 70 mA rms	600A/S2/P/S1215 C = 570/670 75 mA rms	600A/S2/P/S1215 C = 570/670 100 mA rms	600A/S2/P/S1196 = 620/740 100 mA rms *

Secondary internal fault current	Recommended METROSIL type			
	Relay voltage setting			
Amps rms	Up to 200 V rms	250 V rms	275 V rms	300 V rms
150A	600A/S3/P/S1219 C = 430/500 100 mA rms	600A/S3/P/S1220 C = 520/620 100 mA rms	600A/S3/P/S1221 C= 570/670** 100 mA rms	600A/S3/P/S1222 C = 620/740*** 100 mA rms

Table 2: Recommended Metrosil types for 5A CTs

Note: *2400 V peak **2200 V peak ***2600 V peak

In some situations single disc assemblies may be acceptable, contact General Electric for detailed applications.

7. The Metrosil units recommended for use with 5 Amp CTs can also be applied for use with triple pole relays and consist of three single pole units mounted on the same central stud but electrically insulated for each other. To order these units please specify "Triple Pole Metrosil Type", followed by the single pole type reference.
8. Metrosil units for higher relay voltage settings and fault currents can be supplied if required.

For further advice and guidance on selecting METROSILS please contact the Applications department at General Electric.

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2.2.3 Interturn (split phase) protection

For generators with multi-turn stator windings, there is the possibility of a winding inter-turn fault occurring. Unless such a fault evolves to become a stator earth fault, it will not otherwise be detected with conventional protection arrangements. Hydro generators usually involve multi-stator windings with parallel windings.

2.2.3.1 Generator differential interturn protection

One differential scheme using bushing type CTs that is commonly used for interturn protection is shown in Figure 9. In this scheme the circuits in each phase of the stator winding are split into two equal groups and the current of each group are compared. A difference in these currents indicates an unbalance caused by an interturn fault. Since there is normally some current unbalance between windings the protection is set so that it will not respond to this normal unbalance but will pick-up for the unbalance caused by a single turn fault. In some cases the generator may run with a faulted turn until it is repaired and therefore the current pick-up level should be increased to allow operation but still be able to detect a second fault. The P343/4/5/6 IA2/IB2/IC2 current inputs can be used for this type of application and has independent settings per phase (**Interturn Is_A, Interturn Is_B, Interturn Is_C**). Therefore the current setting can be increased on the faulted phase only without affecting the sensitivity of the protection on the other unfaulted phases. A time delay is used to prevent operation on CT transient error currents that may occur during external faults. The problem of CT transient error currents can be eliminated by using core balance (window) type CTs (see Figure 10).

This method of interturn protection will detect phase and some ground faults in the stator winding. However, because of the slow operating time of this protection it is common practice to provide standard high speed differential protection for each phase and separate earth fault protection. If there are main 1 and main 2 P343/4/5/6 protection relays, the IA2/IB2/IC2 inputs could be used for interturn protection on the one relay and used for standard differential protection across the generator in the other relay.

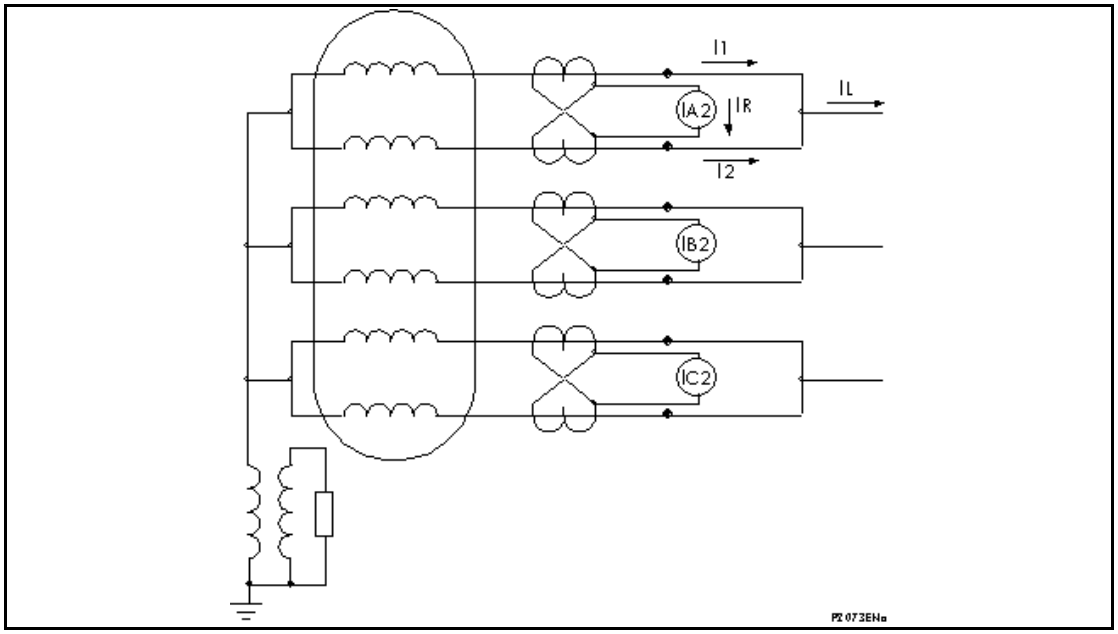


Figure 9: Generator interturn protection using separate CTs

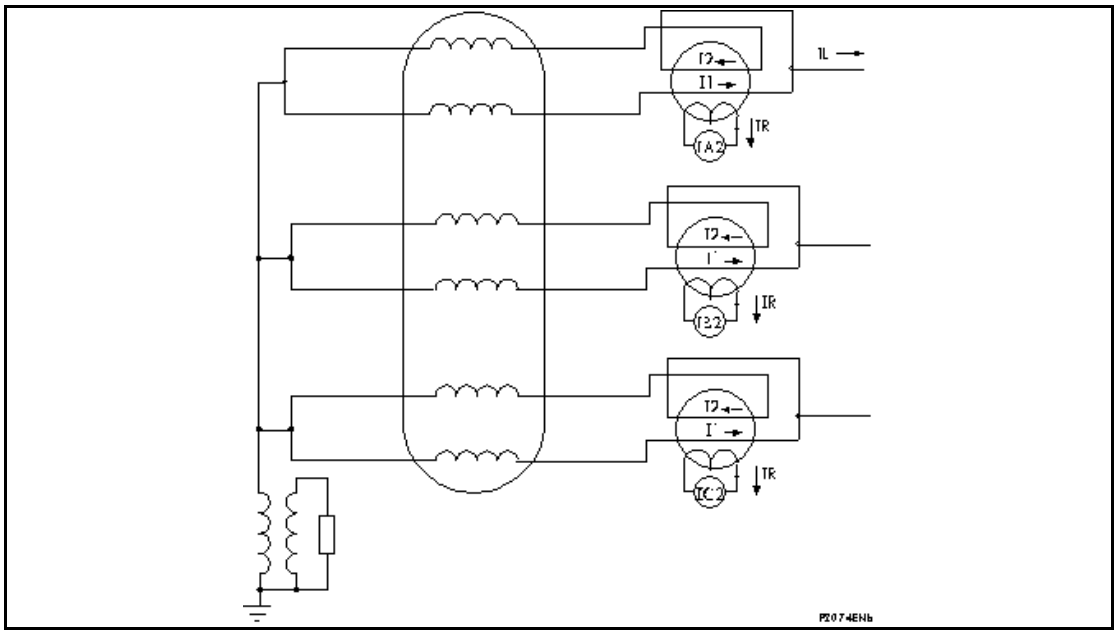


Figure 10: Generator interturn protection using core balance (window) CTs

2.2.3.1.1 Setting guidelines for generator differential interturn protection

The differential setting, **Configuration - Differential**, should be set to **Enabled**. If the winding type in the **SYSTEM CONFIG - Winding Config** is set to **Generator**, then the settings related to Generator differential protection will be displayed in the column **DIFFERENTIAL - Generator Diff**.

To select interturn differential protection the **Gen Diff Func** cell should be set to **Interturn**.

The differential current settings, **Interturn Is_A, Interturn Is_B, Interturn Is_C**, should be set to a low setting to protect as much of the machine winding as possible. A setting of 5% of rated current of the machine is generally considered to be adequate. This setting may need to be increased where low accuracy class CTs are used to supply the protection.

The time delay setting **Interturn ITimeDelay** should be set to prevent operation on CT transient error currents that may occur during external faults. A typical time setting would be 0.1 s.

2.2.3.2 Application of biased generator differential protection for interturn protection

For inter-turn protection applications where the generator stator is wound with 2 or more identical three-phase windings connected in parallel, provided the windings are brought out separately, biased differential protection can be used connected to CTs in the line ends of the 2 or more windings, see Figure 11. In this type of application a biased system should always be used as it is not possible to guarantee in advance that exact current sharing between the windings will take place. A small error in this sharing current would produce instability in an unbiased system at high levels of through fault current. Balanced current in the two windings produces a circulation of current in the current transformer secondary circuit, but any in zone fault, including an interturn fault, will result in a circulation of current between the windings producing an output in the relay operating circuit.

The biased differential protection in the P343/4/5/6 uses both sets of three-phase current inputs and so if the P343/4/5/6 generator differential protection was used for inter-turn protection no other protection function in the P343/4/5/6 would be available. As normally differential protection plus the many other protection functions in the P343/4/5 are required for the generator protection in addition to the interturn protection it is advisable to use a separate biased differential relay for the interturn protection in this application.

Another scheme that could be used on this type of generator is shown in Figure 10. This arrangement is an attempt to get the benefits of inter-turn and differential protection with a saving in CTs and relays. However, this arrangement is not as sensitive as other schemes using separate inter-turn relays or differential relays. The scheme in Figure 10 requires the neutral end CTs having half the turns ratio of the terminal end CTs. The sensitivity of the protection for inter-turn faults is limited by the fact that the two CT ratios applied must be selected in accordance with the generator rated current.

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A P343/4/5/6 could be used for this application with the IA/IB/IC inputs connected to the terminal side CTs as these see the full rated current. Note, the IA/IB/IC inputs feed the current, impedance and power based protection. However, in the case of a single generator feeding an isolated system, back-up protection should use CTs at the neutral end of the machine to ensure internal faults on the generator windings are detected. Therefore for this type of application it is advised that a separate biased differential protection is used for the inter-turn protection. A P342 from separate CTs at the neutral end of the generator could then be used for the rest of the protection.

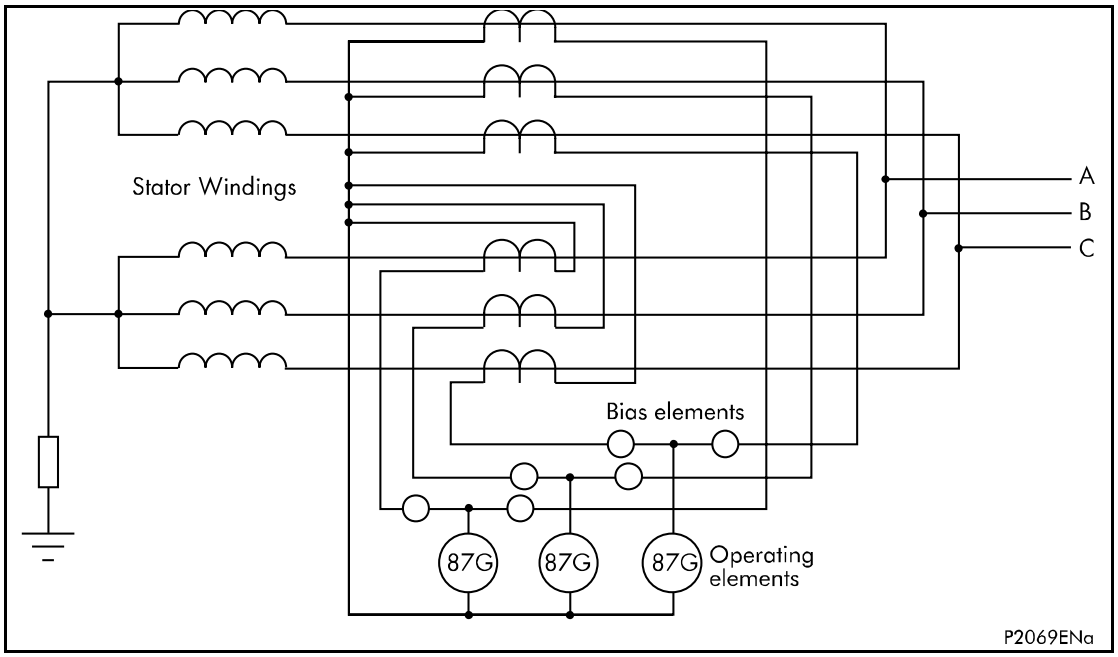


Figure 11: Transverse biased differential protection for double wound machines

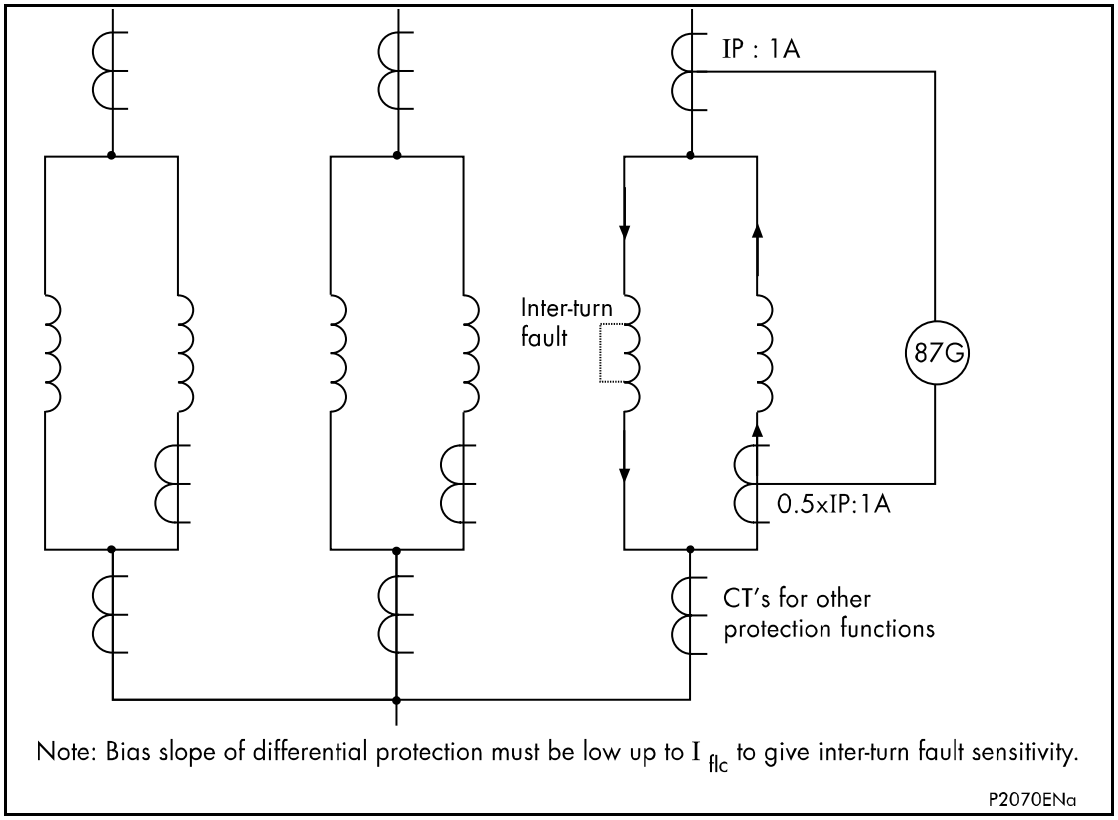


Figure 12: Generator differential and interturn protection

2.2.3.3 Application of overcurrent protection for interturn protection

Another method that could be used for inter-turn protection is to use the current operated stator earth fault protection function using an additional single CT as shown in Figure 13.

In this application the neutral voltage displacement protection (59N) would act as the main stator earth fault protection even though the current based stator earth fault protection could still respond to some stator earth fault conditions. This form of interturn fault protection, using the 51N stator earth fault current operated element (IN>1/2 or ISEF>1) offers the possibility of greater sensitivity compared to the technique shown in Figure 13. This is due to the fact that the required ratio of the single CT for this application is arbitrary. The current setting of the main current operated element (IN>1/2 or ISEF>1) should be set in accordance with the selected CT ratio to provide adequate primary sensitivity for the minimum interturn fault current. For similar reasons the time delay applied should be set similar to that recommended for applications of the main current operated element of normal stator earth fault protection.

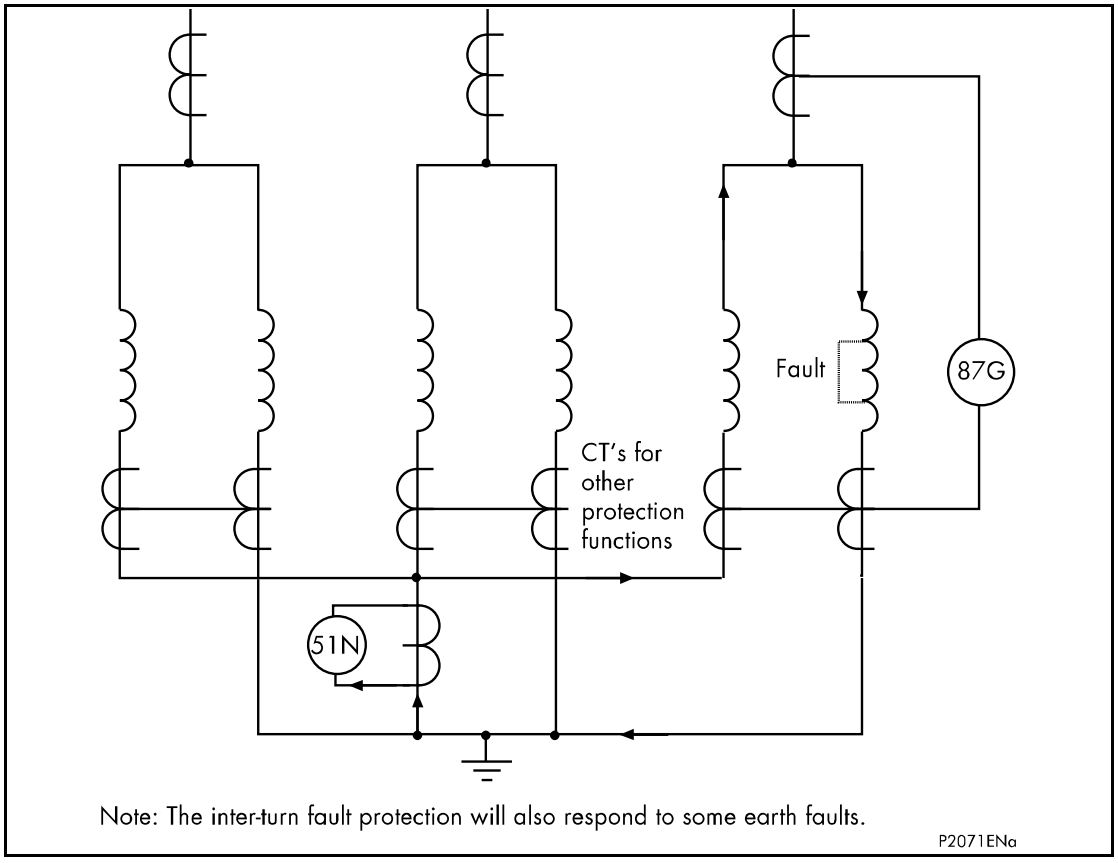


Figure 13: Overcurrent interturn protection

2.2.3.4 Interturn protection by zero sequence voltage measurement

Interturn faults in a generator with a single winding can be detected by observing the zero sequence voltage across the machine. Normally, no zero sequence voltage should exist but a short circuit of one or more turns on one phase will cause the generated emf to contain some zero sequence component. This method of interturn protection can be provided using the neutral voltage displacement protection in the P342/3/4/5/6, see section 2.18.

External earth faults will also produce a zero sequence voltage on a directly connected generator. Most of the voltage will be dropped across the earthing resistor, the drop on the generator being small and the zero sequence component being limited to one or two percent. It is preferable, therefore, to measure the voltage drop across the winding, rather than the zero sequence voltage to earth at the line terminals. This can be done using a voltage transformer connected to the line side of the generator, with the neutral point of the primary winding connected to the generator neutral, above the earthing resistor or earthing transformer. This arrangement is shown in Figure 14. The zero sequence voltage can be measured directly from the voltage transformer broken delta winding connected to the neutral voltage input, VN1 (VN>3/4), on the P342/3 and VN1 (VN>3/4) or VN2 (VN>5/6) on the P344/5. Alternatively, the zero sequence voltage can be derived (VN>1/2) from the three-phase voltage inputs, VA, VB, VC, to the relay.

The 3rd harmonic component of the emf may be larger than the required setting, however, there is no danger of maloperation as the 3rd harmonic component is filtered by the relay's Fourier filter.

With a direct-connected machine it is still possible that a close up earth fault will produce a zero sequence voltage drop greater than that produced by the short circuiting of one turn. It is therefore necessary to apply a short time delay to the tripping element. With a generator-transformer unit an external earth fault can not draw zero sequence current through the delta winding of the transformer. Therefore no residual voltage will be produced from the voltage transformer and so no time delay is required in this case for the trip element.

With this type of VT connection the zero sequence voltage from the VT is small for an external fault. Also, the output from the star connected secondary winding of the VT will not

be able to correctly represent phase-ground voltages (for external faults), only phase-phase voltages will remain accurate. Therefore the sensitive directional earth fault protection and CT supervision element, which use zero sequence voltage, may not operate if the VN polarizing input is set to **Derived**. The VN polarizing input should be set to **Measured** or the function disabled for these functions where the Main VT is used for interturn protection (**Measured** is the VN1 input for P342/3/4/5/6). The under and over voltage protection can be set as phase to phase measurement with this type of VT connection. The underimpedance and the voltage dependent overcurrent use phase-phase voltages anyway, therefore the accuracy should not be affected. The protection functions which use phase-neutral voltages are the power, the loss of excitation and pole slipping protection; all are for detecting abnormal generator operation under three-phase balanced conditions, therefore the accuracy of these protection functions should not be affected.

If the neutral voltage displacement element is required for 95% stator earth fault protection as well as interturn protection a separate VT connection at the terminals of the generator or a distribution transformer at the generator earth is required to obtain the correct zero sequence voltage. The neutral voltage displacement protection in the P342/3 relay can use the measured residual voltage from the VN1 input and the derived residual voltage from the three-phase voltage inputs. So, if the derived residual voltage is used for interturn protection, then the measured residual voltage from a distribution transformer at the generator neutral point can not be used for 95% stator earth fault protection using one relay. The P344/5 has two dedicated neutral voltage displacement inputs, VN1 and VN2, as well as a derived neutral voltage element. So one neutral voltage input can be used for interturn protection and one for 95% stator earth fault protection, see Figure 14. See section 2.18 for more information on the P342/3/4/5/6 neutral voltage displacement protection.

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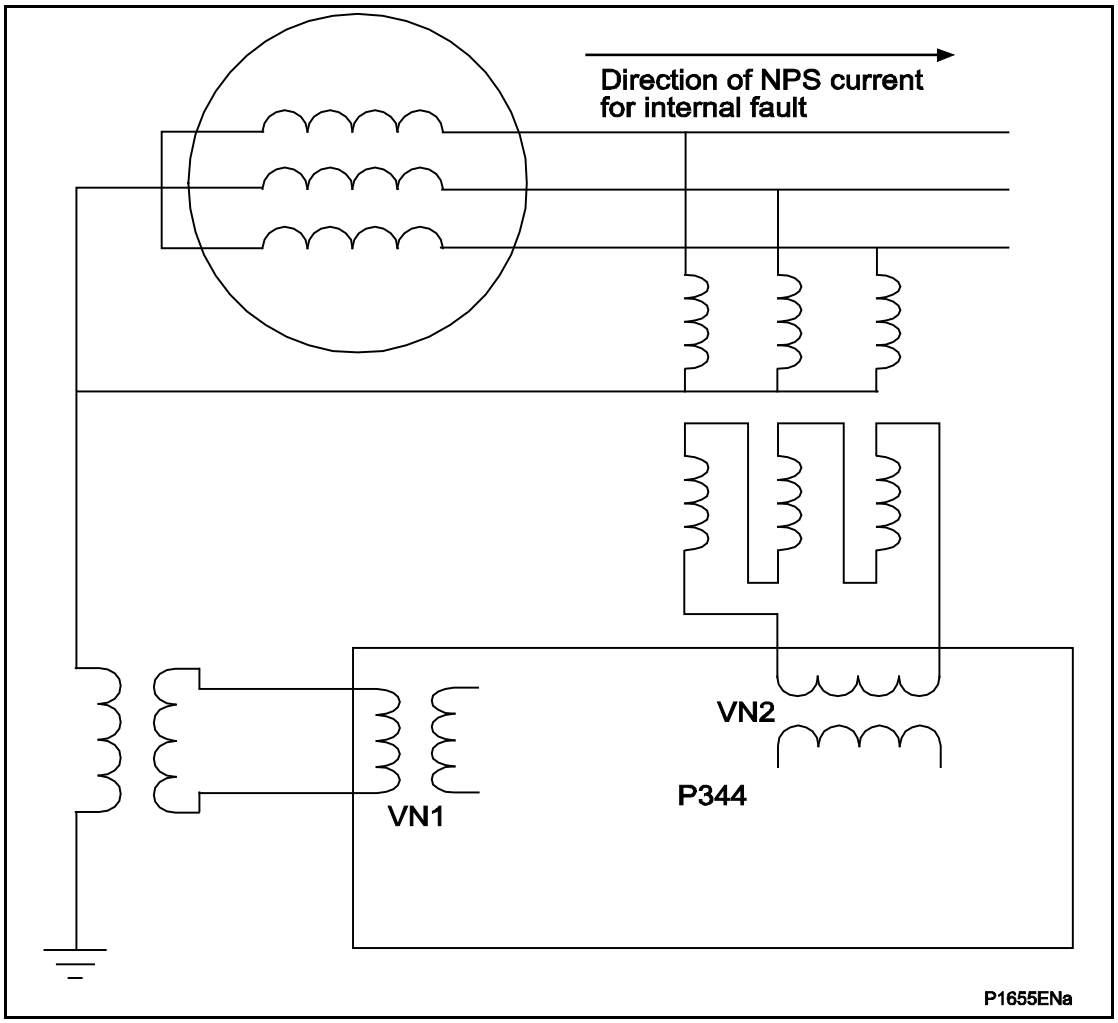


Figure 14: Interturn protection (VN2) and earth fault protection (VN1) by zero sequence voltage measurement

2.2.3.4.1 NPS overpower and NPS overcurrent interlocking for zero sequence voltage interturn protection

To prevent the neutral voltage (zero sequence) element used for interturn protection from maloperation for an external phase-phase or earth fault, the element can be interlocked with a NPS apparent power element (S2 = I2 x V2, non-directional) and a directional NPS overcurrent element looking away from the machine. The trip signal is issued only if all of the elements, VNx>, S2> and I2> operate. An example of the PSL logic for this interlocking is shown in Figure 15.

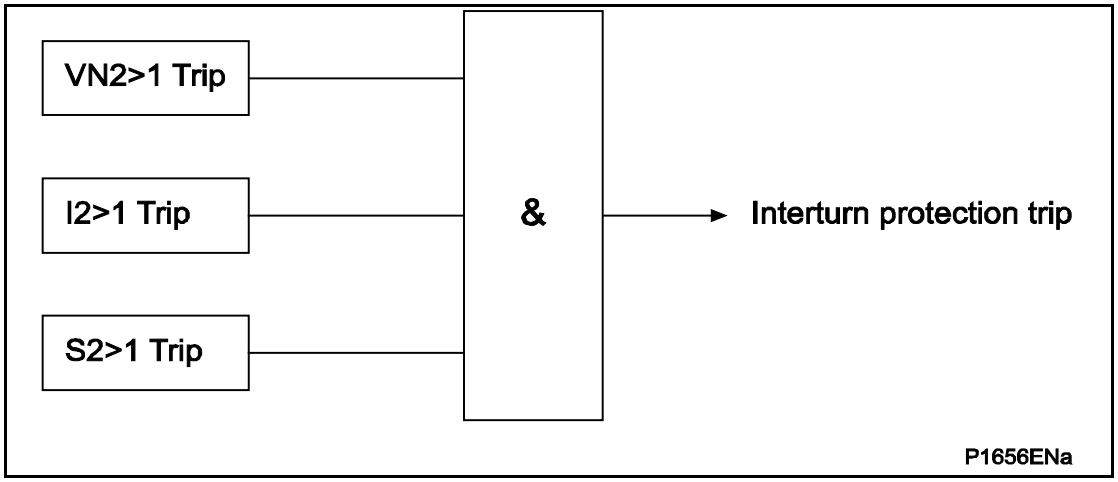


Figure 15: Interturn protection interlocking PSL logic

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See sections 2.4 and 2.6 for more information on the NPS Overpower and directional NPS overcurrent protection.

Figure 16 and Figure 17 show the negative phase sequence fault current direction during an internal fault and external fault for a generator application. Figure 16 and Figure 17 show the direction of negative phase sequence current at the neutral point is always the same for internal and external faults. The direction of the negative phase sequence current is different for internal and faults from the terminal side CTs.

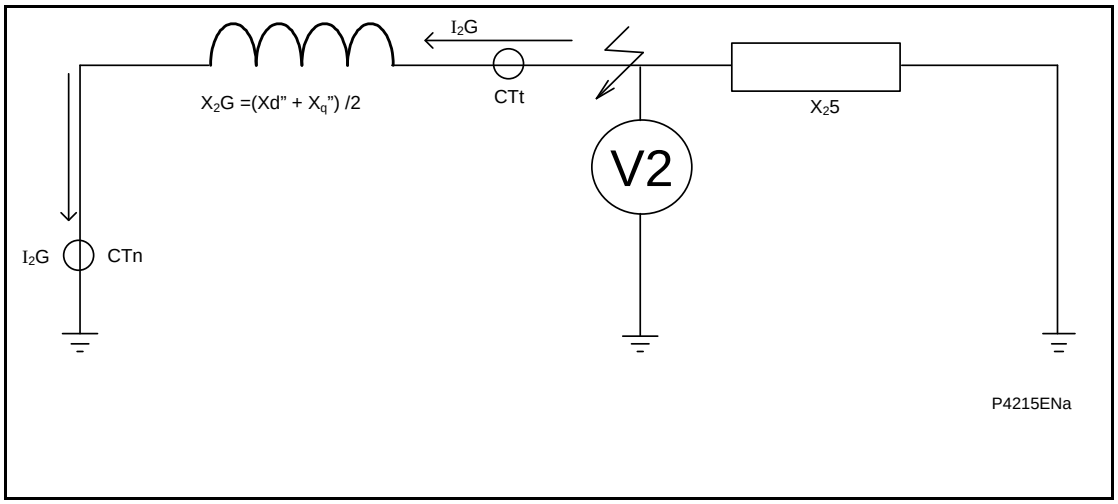


Figure 16: Negative sequence diagram for external fault

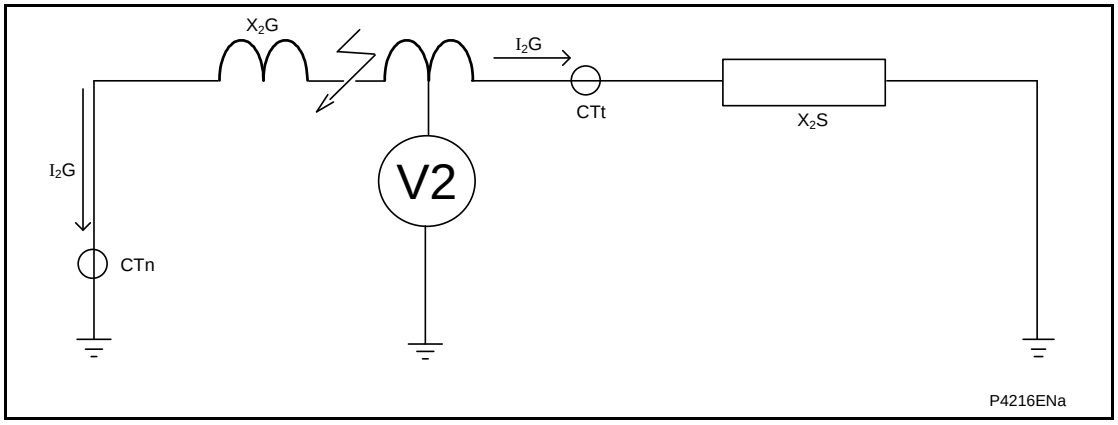


Figure 17: Negative sequence diagram for internal fault

2.3 Generator-Transformer differential protection (87GT)

In applying the well established principles of differential protection to a generator-transformer unit, a variety of considerations have to be taken into account. These include compensation for any phase shift across the transformer, possible unbalance of signals from current transformers either side of windings and the effects of the variety of earthing and winding arrangements. In addition to these factors, which can be compensated for by correct application of the relay, the effects of normal system conditions on relay operation must also be considered. The differential element must be blocked for system conditions which could result in maloperation of the relay, such as high levels of magnetizing current during inrush conditions or during transient overfluxing.

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In traditional transformer differential schemes, the requirements for phase and ratio correction were met by the application of external interposing current transformers, as a secondary replica of the main transformer winding arrangements, or by a delta connection of main CTs (phase correction only). The P343/4/5/6 has settings to allow flexible application of the protection to a wide variety of transformer configurations, or to other devices where differential protection is required, without the need for external interposing CTs or delta connection of secondary circuits.

2.3.1 Biased elements

The P34x percentage bias calculation is performed 4 times per cycle. A triple slope percentage bias characteristic is implemented. Both the flat and the lower slope provide sensitivity for internal faults. Under normal operation steady state magnetizing current and the use of tap changers result in unbalanced conditions and hence differential current. To accommodate these conditions the initial slope, K1, may be set to 30%. This ensures sensitivity to faults while allowing for mismatch when the power transformer is at the limit of its tap range and CT ratio errors. At currents above rated, extra errors may be gradually introduced as a result of CT saturation, so the higher slope may be set to 80% to provide stability under through fault conditions, during which there may be transient differential currents due to saturation effect of the CTs. The through fault current in all but ring bus or mesh fed transformers is given by the inverse of the per unit reactance of the transformer. For most transformers, the reactance varies between 0.05 to 0.2 pu, therefore typical through fault current is given by 5 to 20 In.

The number of biased differential inputs required for an application depends on the transformer and its primary connections. It is recommended that, where possible, a set of biased CT inputs is used for each set of current transformers. According to IEEE Std. C37.110-2007 separate current inputs should be used for each power source to the transformer. If the secondary windings of the current transformers from two or more supply breakers are connected in parallel, under heavy through fault conditions, differential current resulting from the different magnetizing characteristics of the current transformers will flow in the relay. This current will only flow through one current input in the relay and can cause misoperation. If each CT is connected to a separate current input, the total fault current in each breaker provides restraint. It is only advisable to connect CT secondary windings in parallel when both circuits are outgoing loads. In this condition, the maximum through fault level will then be restricted solely by the power transformer impedance. The P343/4/5/6

relays only have 2 biased differential inputs so can only be used to protect 2 winding generator-transformer configurations.

The typical connection for a P34x relay is shown in Figure 18.

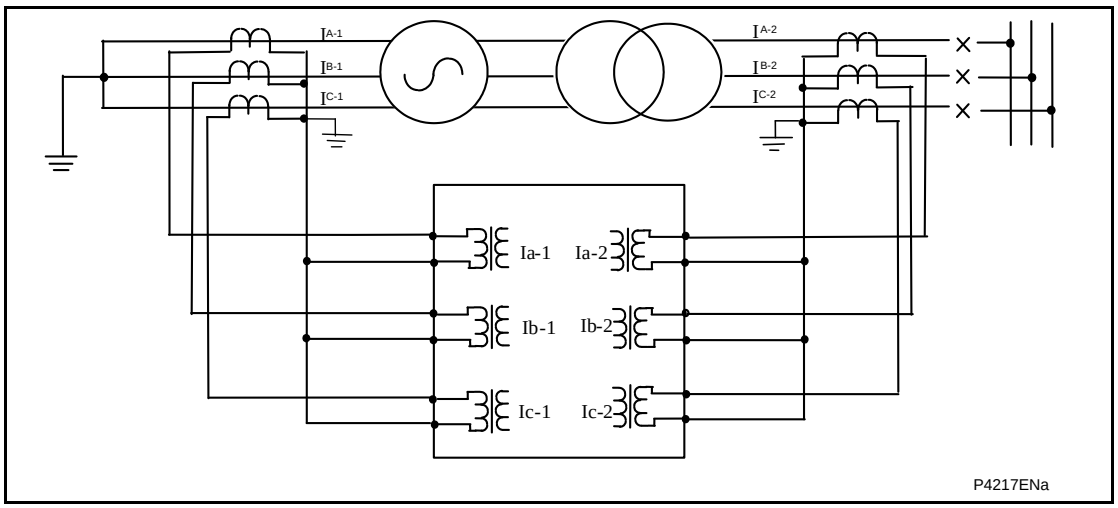


Figure 18: P34x typical connection for generator-transformer unit connection

The P34x relay achieves stability for through faults in two ways, both of which are essential for correct relay operation. The first consideration is the correct sizing of the current transformers; the second is by providing a relay bias characteristic as shown in Figure 19.

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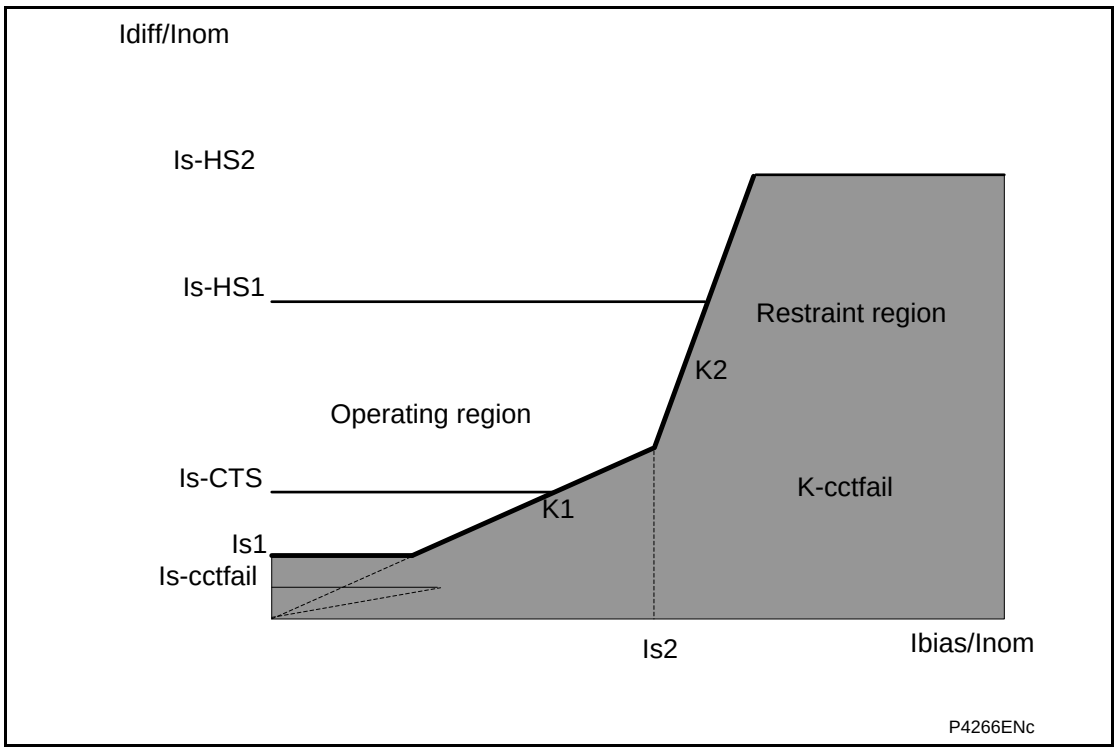


Figure 19: P34x triple slope (flat, K1, K2) biased differential protection

The flat and lower slope, K1, provides sensitivity for internal faults. The higher slope, K2, provides stability under through fault conditions, during which there may be transient differential currents due to asymmetric CT saturation.

The differential and biased current calculations are done on a per phase basis after amplitude, vector group matching and zero sequence filtering are performed. The following equations are valid for uniformly defined current arrows relative to the protected equipment, so the current arrows of all windings point either towards the protected object or away from it.

The differential current, I_{diff}, and the bias current I_{bias} are defined by the following expressions:

$$I_{diff} = \left| \bar{I}_1 + \bar{I}_2 \right|$$

$$I_{bias} = \frac{\left| \bar{I}_1 \right| + \left| \bar{I}_2 \right|}{2}$$

The differential current, I_{diff}, is the vector sum of the phase currents measured at the two ends of the generator-transformer. The mean bias current, I_{bias} is the scalar mean of the magnitude of the currents at the two ends of the generator-transformer.

To provide stability for external faults the following measures are taken on the bias calculations:

- Delayed bias: the bias quantity is the maximum of the bias quantities calculated within the last cycle. This is to maintain the bias level, providing stability during the time when an external fault is cleared. This featured is implemented on a per phase basis
- Transient bias: an additional bias quantity is introduced into the bias calculation, on a per phase basis, if there is a sudden increase in the mean-bias measurement. This quantity will decay exponentially afterwards. The transient bias is reset to zero once the relay has tripped or if the mean-bias quantity is below the Is1 setting. The transient bias algorithm is executed 4 times per cycle.
- Maximum bias: the bias quantity used per phase for the percentage bias characteristic is the maximum delayed bias current calculated from all three phases.

$$Ibias_{(\max)} = Maximum\left[Ia_{bias}, Ib_{bias}, Ic_{bias}\right]$$

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For the P34x relays the restraining effect (bias current) never disappears when there is an internal fault; the restraining effect is even reinforced. However, the restraining current factor ½ means that the differential current Id has twice the value of the restraining current I_{bias}, so that safe and reliable tripping is also guaranteed in the case of multi-end infeed for internal faults.

As shown in Figure 19, the tripping characteristic of the differential protection has two knees. The first knee is dependent on the setting of the basic threshold value Is1. The second knee of the tripping characteristic is defined by the setting Is2.

The basic pick up level of the low set differential element, Is1, is dependant on the item of plant being protected and by the amount of differential current that might be seen during normal operating conditions. A setting of 0.2 pu is generally recommended when the P34x is used to protect a generator-transformer unit.

The flat section of the tripping curve represents the most sensitive region of the tripping characteristic in the form of the settable basic threshold value Is1. The default setting of 0.2 pu takes into account the steady state magnetizing current of the transformer, which flows even in a no-load condition and is generally less than 5% of the nominal transformer current.

Characteristic equation:

For $Ibias < \frac{Is1}{K1}$

$$Idiff \geq Is1$$

The flat and K1 slopes of the tripping curve cover the load current range, so that in these sections we must account for not only the transformer steady state magnetizing current, which appears as differential current, but also with differential currents that can be attributed to the transformation errors of the current transformer sets and on load tap changers.

If we calculate the worst case with IEC class 10P current transformers, the maximum allowable amplitude error according to IEC 60044-1 is 3 % for nominal current. The phase-angle error can be assumed to be 2° for nominal current. The maximum allowable total error for nominal current is then obtained, in approximation, as (0.03 + sin 2°) ≈ 6.5 %. If the current is increased to the nominal accuracy limit current, the total error for Class 10P current transformers can be 10 % maximum, as may be the case under heavy fault conditions. Beyond the nominal accuracy limit current, the transformation error can be of any magnitude.

The dependence of the total error of a current transformer on current is therefore non-linear. In the operating current range (the current range below the nominal accuracy limit current) we can expect a worst case total error of approximately 10 % per current transformer set.

The first slope section of the tripping characteristic forms a straight line, the slope of which should correspond to the cumulative total error of the participating current transformer sets and on load tap changer. The curve slope, K1, can be set. The default setting for K1 is 30%.

Characteristic equation:

For $Idiff > Is1$ AND $Ibias < Is2$

$$Idiff \geq K1 x Ibias$$

The second knee point, Is2, is settable. It has a default setting of 1 pu and must be set in accordance with the maximum possible operating current.

Restraining currents that go beyond the set knee point (Is2) are typically considered as through fault currents. For through fault currents, the third section of the tripping characteristic could therefore be given an infinitely large slope. Since, however, we also need to take into account the possibility that a fault can occur in the transformer differential protected zone, a finite slope K2 is provided for the third section of the tripping curve. The default setting for K2 is 80%.

Characteristic equation:

For $Idiff \geq Is2$

$$Idiff \geq K1 \times Is2 + K2(Ibias - Is2)$$

Note: The default settings for **Xform Is2** (1pu), **Xform K1** (30%) and **Xform K2** (80%) should always be used as the CT requirements are based on these settings.

2.3.2 Ratio correction

To ensure correct operation of the differential element, it is important that under load and through fault conditions the currents into the differential element of the relay balance. In many cases, the HV and LV current transformer primary ratings will not exactly match the transformer winding rated currents. Ratio correction factors are therefore provided. The CT ratio correction factors are applied to ensure that the signals to the differential algorithm are correct.

A reference power, identical for both HV/LV windings, is defined in the Sref setting cell under the **SYSTEM CONFIG** menu heading. The ratio correction factor for each winding of the generator-transformer is calculated by the P34x on the basis of the set reference power, the set primary nominal voltages of the transformer and the set primary nominal currents of the current transformers.

$$K_{amp,n} = \frac{I_{primCT,nom,n}}{\frac{S_{prim,ref}}{\sqrt{3V_{primCT,nom,n}}}}$$

Where:

$K_{amp,n}$ = amplitude matching factor for the respective CT input

$I_{primCT,nom,n}$: primary nominal current for the respective CT input

$V_{primCT,nom,n}$: nominal voltage for the respective CT input. Where on-load tap changing is used, the nominal voltage chosen should be that for the mid tap position.

Sprim,ref: common primary reference value of S for both windings

Therefore the only data needed for ratio correction or amplitude matching calculation done by the relay are the nominal values read from the generator-transformer nameplate.

For the generator-transformer shown in Figure 20, the phase C amplitude matched currents of the HV and LV windings are the same.

$$I_{amp,HV,C} = K_{amp\cdot HV} \times I_{HV,C}$$

$$I_{amp,LV,C} = K_{amp,LV} \times I_{LV,C}$$

Where:

$I_{amp,\ HV,C}$; HV side phase C amplitude matched current

$K_{amp,HV:}$ HV side calculated ratio correction factor

$I_{HV,C}$: HV side phase C current magnitude

$I_{amp,\ LV,C}$; LV side phase C amplitude matched current

$K_{amp,LV:}$ LV side calculated ratio correction factor

$I_{LV,C}$: LV side phase C current magnitude

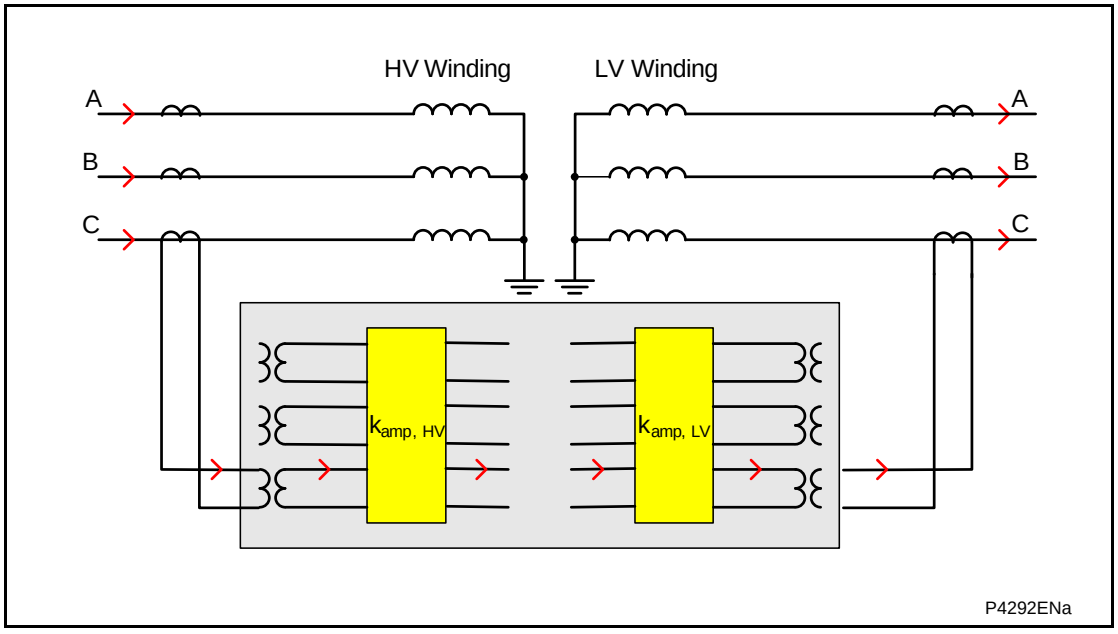


Figure 20: Ratio correction or amplitude matching factor

Matching factors are displayed by the P34x in the **Match Factor HV** and **Match Factor LV** data cells under the **SYSTEM CONFIG** menu heading. The P34x derives amplitude matching factors automatically so that all biased currents are compared on a like for like basis. The range of the calculated matching factors is from 0.05 to 20. Amplitude matching factors above 20 are not recommended since the probability of tripping due to electrical noise is very high.

2.3.3 Vector group correction

To compensate for any phase shift between two windings of a generator-transformer it is necessary to provide vector group correction. This was traditionally provided by the appropriate connection of physical interposing current transformers, as a replica of the main transformer winding arrangements, or by a delta connection of the main CTs.

This matching operation can be carried out regardless of the phase winding connections, since the phase relationship is described unambiguously by the characteristic vector group number.

Vector group matching is therefore performed by mathematical phasor operations on the amplitude-matched phase currents of the low-voltage side in accordance with the characteristic vector group number. The vector group is the clock-face hour position of the LV A-phase voltage, with respect to the A-phase HV voltage at 12-o'clock (zero) reference. Phase correction is provided in the P34x using **SYSTEM CONFIG** then **LV Vector Group** for phase shift between HV and LV windings.

This is shown in the following figure for vector group characteristic number 5, where vector group Yd5 is used as the example:

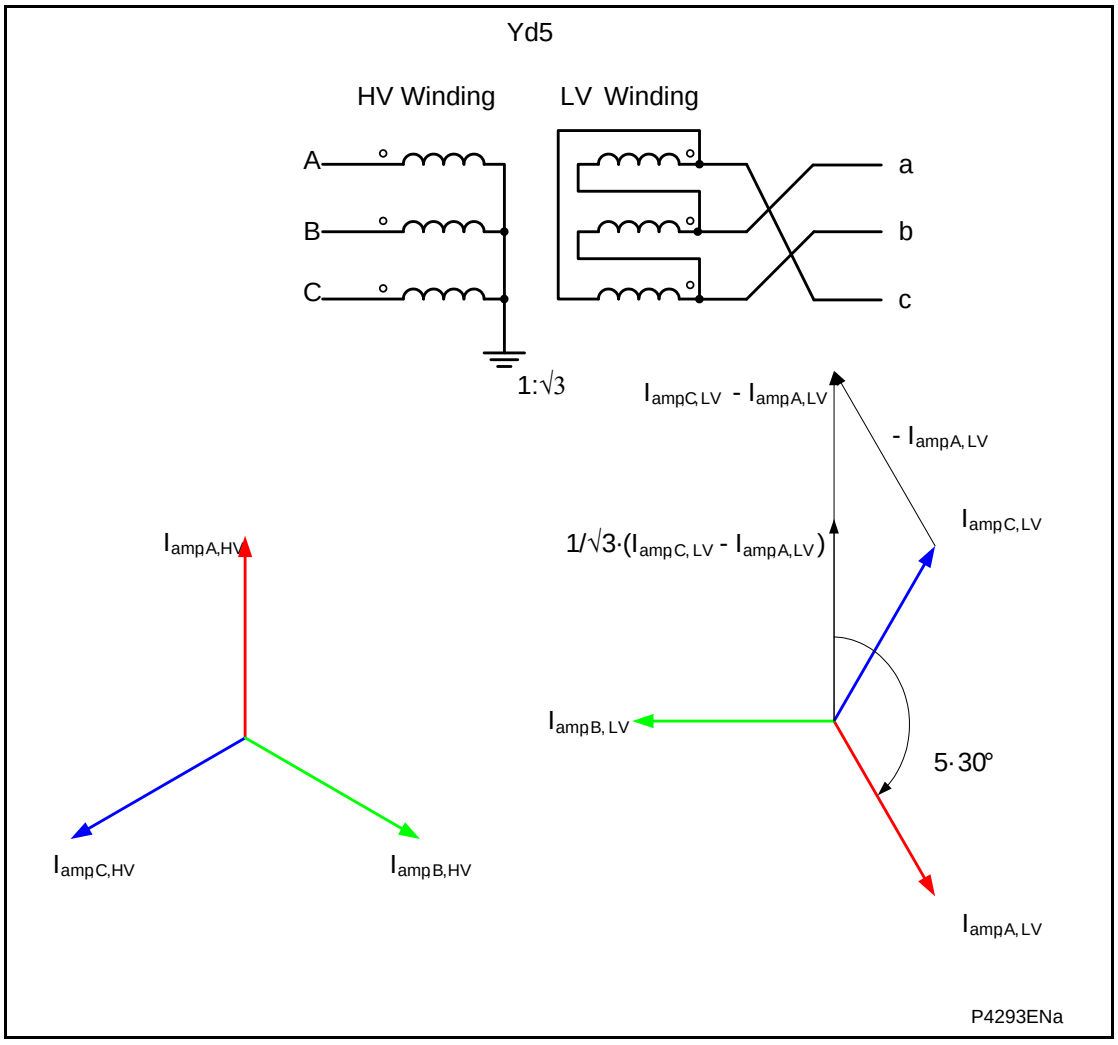


Figure 21: Yd5 transformer example

The angle of positive sequence primary current is used as a default; therefore, no vector correction is applied to the high voltage side.

Figure 21 shows the positive sequence current at the low voltage end is shifted by 150° clockwise for ABC (anti-clockwise) rotation. Therefore the relay setting, **LV Vector Group**, equal to "5" will rotate back the current at the low side for 150° in an anti-clockwise direction. This assures that the primary and secondary currents are in phase for load and external fault conditions. The vector correction also considers amplitude matching. If the vector group is any odd number, the calculated current will be greater by $\sqrt{3}$; therefore; this current will be automatically divided by $\sqrt{3}$. Hence, this effect does not need to be taken into account when CT correction compensation is automatically calculated or set.

Setting the vector group matching function is very simple and does not require any calculations. Only the characteristic vector group number needs to be set in LV Vector Group.

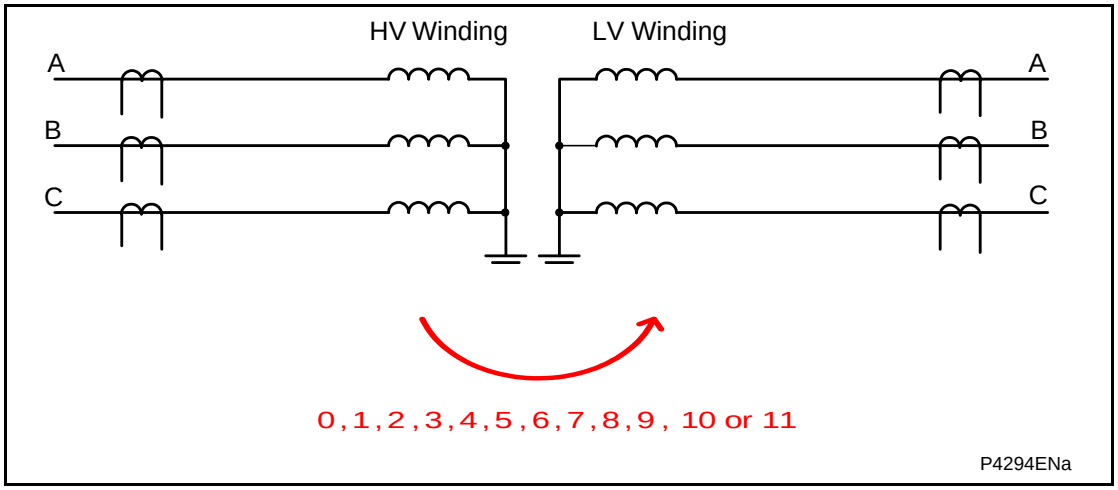


Figure 22: Vector group selection

Other nameplate designations may be used instead of the clock notation - common examples are:

Alternatives		Equivalent standard	LV group setting
DAB/Y	DAB – Y	Dy1	1
DAC/Y	DAC – Y	Dy11	11
Y/Y	Y0 - Y0	Yy0	0
Y/Y –	Y0 - Y6	Yy6	6

Table 3: Vector group designations

2.3.4 Zero sequence filter

In addition to mimicking the phase shift of the protected transformer, it is also necessary to mimic the distribution of primary zero sequence current in the protection scheme. The necessary filtering of zero sequence current has also been traditionally provided by appropriate connection of interposing CTs or by delta connection of main CT secondary windings. In the P34x, the user does not need to decide which windings need zero sequence filtering. The user just needs to set which windings are grounded using a Yn, Zn or in zone-earthing transformer. The relay will adjust itself accordingly. In the advanced setting mode, it is possible to override the self adaptive setting with the zero sequence filtering enabled/disabled setting.

Where a transformer winding can pass zero sequence current to an external earth fault, it is essential that some form of zero sequence current filtering is used. This ensures out of zone earth faults will not cause the relay to maloperate.

An external earth fault on the star side of a Dyn11 transformer will result in zero sequence current flowing in the current transformers associated with the star winding. However, due to the effect of the delta winding, there will be no corresponding zero sequence current in the current transformers associated with the delta winding.

To ensure stability of the protection, the LV zero sequence current must be eliminated from the differential current. Traditionally this has been achieved by either delta connected line CTs or by the inclusion of a delta winding in the connection of an interposing current transformer.

In accordance with its definition, the zero-sequence current is determined as follows from vector and amplitude matched phase currents:

$$\underline{I}_0 = \frac{1}{3} \cdot \left(\underline{I}_{A,vector_comp} + \underline{I}_{B,vector_comp} + \underline{I}_{C,vector_comp} \right)$$

The current that is used in the differential equation is the filtered current per phase:

$$\underline{I}_{A,filtered} = \underline{I}_{A,vector_comp} - \underline{I}_0$$
$$\underline{I}_{B,filtered} = \underline{I}_{B,vector_comp} - \underline{I}_0$$
$$\underline{I}_{C,filtered} = \underline{I}_{C,vector_comp} - \underline{I}_0$$

Setting the zero-sequence current filtering function is very simple and does not require any calculations. Zero-sequence current filtering should only be activated for those ends where there is operational earthing of a neutral point:

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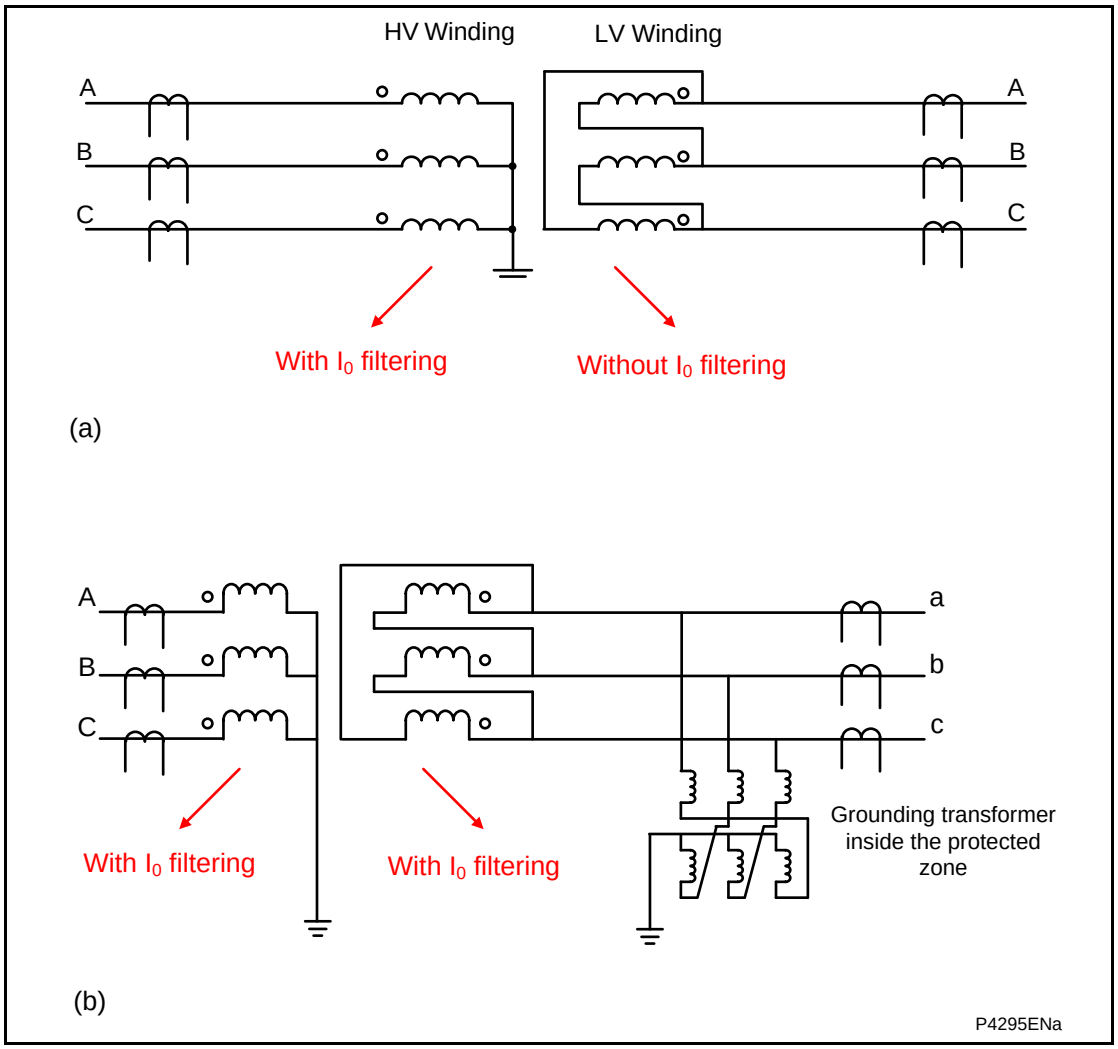


Figure 23: Zero sequence current filtering

Figure 24 shows the current distribution for an AN fault on the delta side of a Yd1 transformer with a grounding transformer inside the protected zone.

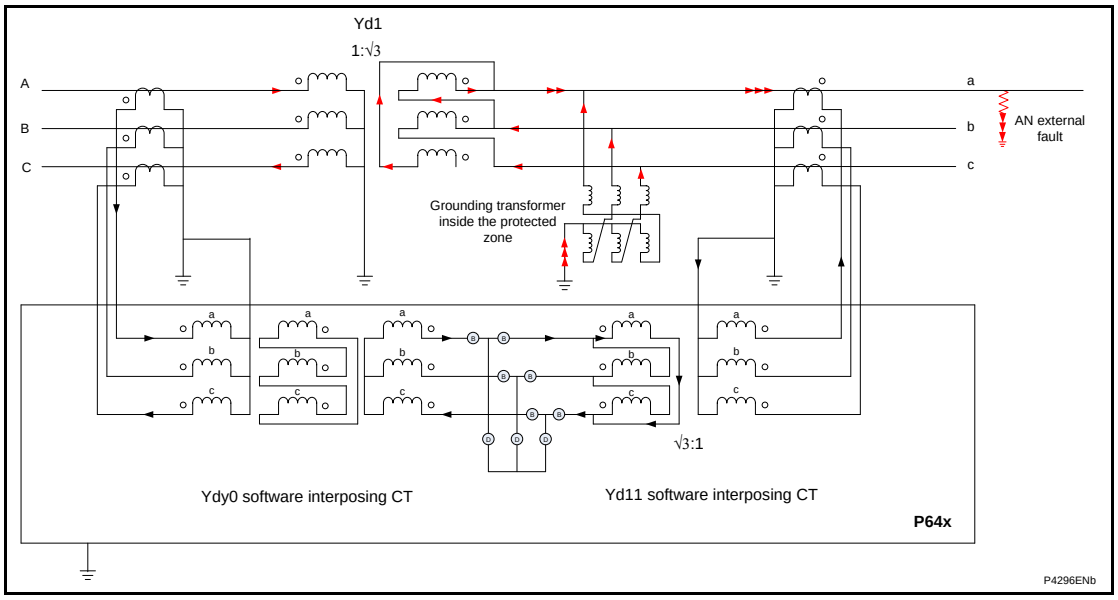


Figure 24: Current distribution for AN external fault on the delta side of a Yd1 transformer

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2.3.5 Magnetizing inrush stabilization

When a transformer is first energized, a transient magnetizing current flows, which may reach instantaneous peaks of 8 to 30 times the full load current. The factors controlling the duration and magnitude of the magnetizing inrush are:

- Size of the transformer bank
- Size of the power system
- Resistance in the power system from the source to the transformer bank
- Residual flux level
- Type of iron used for the core and its saturation level.

There are three conditions which can produce a magnetizing inrush effect:

- First energization
- Voltage recovery following external fault clearance
- Sympathetic inrush due to a parallel transformer being energized.

Figure 24 shows under normal steady state conditions the flux in the core changes from maximum negative value to maximum positive value during one half of the voltage cycle, which is a change of 2.0 maximum.

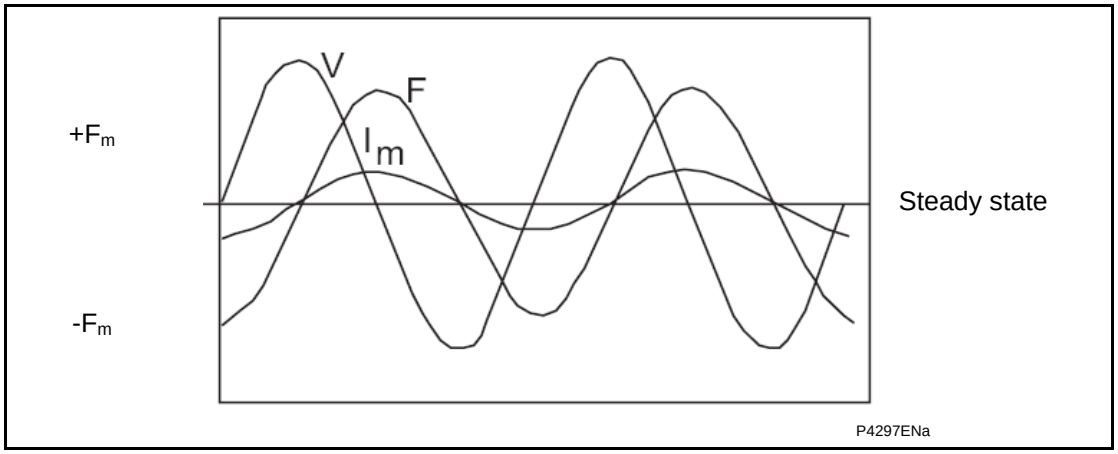


Figure 25: Steady state magnetizing inrush current

If the transformer is energized at a voltage zero when the flux would normally be at its maximum negative value, the flux would rise to twice its normal value over the first half cycle of voltage. To establish this flux, a high magnetizing inrush current is required. The first peak of this current can be as high as 30 times the transformer rated current. This initial rise could be further increased if there was any residual flux in the core at the moment the transformer was energized.

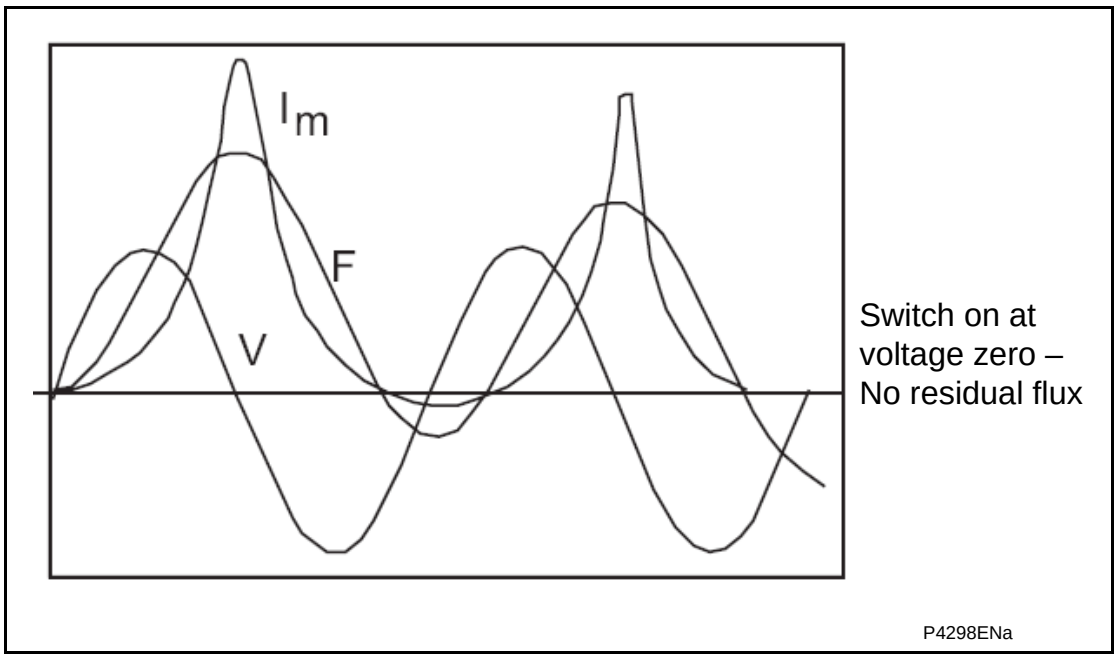


Figure 26: Magnetizing inrush current during energization

As the flux enters the highly saturated portion of the magnetizing characteristic, the inductance falls and the current rises rapidly. Magnetizing impedance is of the order of 2000% but under heavily saturated conditions this can reduce to around 40%, which is an increase in magnetizing current of 50 times normal. This figure can represent 5 or 6 times normal full load current.

Analysis of a typical magnitude inrush current wave shows (fundamental = 100%):

Component	-DC	2nd H	3rd H	4th H	5th H	6th H	7th H
	55%	63%	26.8%	5.1%	4.1%	3.7%	2.4%

The offset in the wave is only restored to normal by the circuit losses. The time constant of the transient can be quite long, typically 0.1 second for a 100 KVA transformer and up to 1 second for larger units. The initial rate of decay is high due to the low value of air core reactance. When below saturation level, the rate of decay is much slower. The following

graph shows the rate of decay of the DC offset in a 50 Hz or 60 Hz system in terms of amplitude reduction factor between successive peaks.

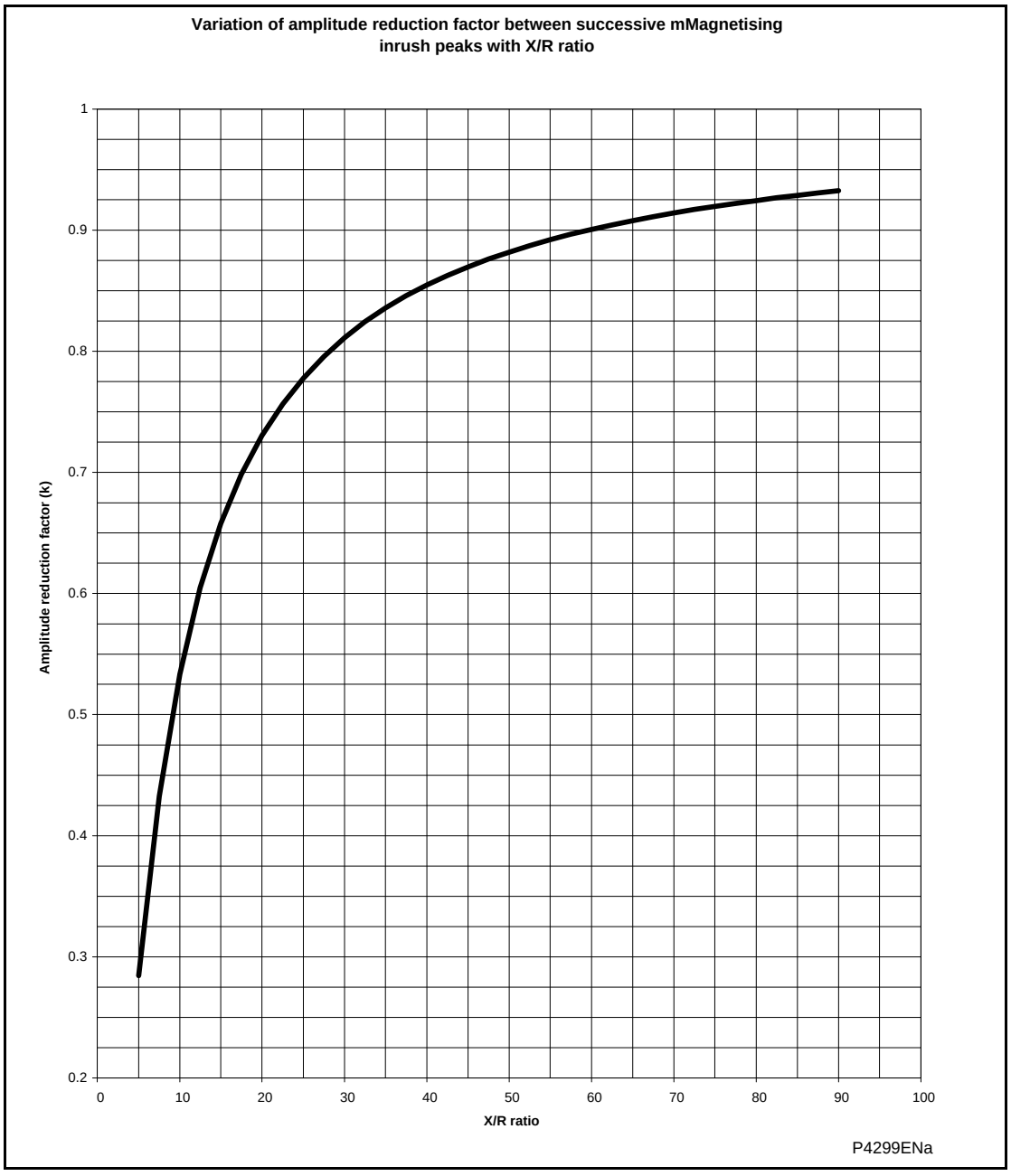


Figure 27: Variation of amplitude reduction factor

The magnitude of the inrush current is limited by the air core inductance of the windings under extreme saturation conditions. A transformer with concentric windings will draw a higher magnetizing current when energized from the LV side, since this winding is usually on the inside and has a lower air core inductance. Sandwich windings have approximately equal magnitude currents for both LV and HV. Resistance in the source will reduce the magnitude current and increase the rate of decay.

The magnetizing inrush phenomenon is associated with a transformer winding which is being energized where no balancing current is present in the other winding(s). This current appears as a large operating signal for the differential protection. Therefore special measures are taken with the relay design to ensure that no maloperation occurs during inrush. The fact that the inrush current has a high proportion of harmonics having twice the system frequency offers a possibility of stabilization against tripping by the inrush current. The second harmonic blocking may not be effective in all applications with all types of transformers. The P34x filters the differential current. The fundamental $I_{diff}(f_0)$ and second

harmonic components $I_{diff}(2*f_0)$ of the differential current are determined. If the ratio $I_{diff}(2*f0)/I_{diff}(f0)$ exceeds a specific adjustable value (typical setting 20%) in at least one phase, the low-set differential element is blocked optionally in one of the following modes:

- Across all three phases if cross blocking is selected
- Selectively for one phase because the harmonic blocking is phase segregated
- There is no blocking if the differential current exceeds the high set thresholds **Is-HS1** or **Is-HS2**

2.3.6 High set operation

The P34x relay incorporates independent transformer differential high set elements, **Xform Is-HS1** and **Xform Is-HS2** to complement the protection provided by the biased differential low set element, the high set could be disabled and enabled individually. The instantaneous high set offers faster clearance for heavy internal faults and it is not blocked for magnetizing inrush or transient overfluxing conditions.

Stability is provided for heavy external faults, but the operating threshold of the high set differential element must be set to avoid operation with inrush current.

When a transformer is energized, a high magnetizing inrush current is drawn. The magnitude and duration of this inrush current is dependant on several factors which include;

- Size and impedance of the transformer
- Point on wave of switching
- Remnant flux in the transformer
- Number of transformers connected in parallel

It is difficult to accurately predict the maximum anticipated level of inrush current. Typical waveform peak values are of the order of 8 - 30x rated current. A worst-case estimation of inrush could be made by dividing the transformer full load current by the per-unit leakage reactance quoted by the transformer manufacturer. In the simple mode, the relay calculates the setting for **Xform Is-HS1** as the reciprocal of the transformer reactance.

A setting range of 2.5 – 16 pu is provided in the P34x relay for **Xform Is-HS1** and **Xform Is-HS2**. Both elements should be set in excess of the anticipated or estimated peak value of inrush current after ratio correction.

The **Xform Is-HS2** element uses the fundamental component of the differential current. This element is not restrained by the bias characteristic, so the P34x will trip regardless of the restraining current. **Xform Is-HS2** should be set so that the relay will not maloperate during external faults. When through fault current is limited by the transformer impedance, **Xform Is-HS2** can be set as $1.3 \times (1/Xt)$. In breaker and a half, ring bus or mesh applications, the through fault current is not limited by the transformer impedance but by the system source impedance. This current can be higher than $1.3 \times (1/Xt)$, therefore the user should consider the actual through fault current when setting **Xform Is-HS2**. To avoid high values of spurious differential current due to CT saturation during through fault conditions, it is important to equalize the burden on the CT secondary circuits.

2.3.7 Setting guidelines for biased differential protection

The differential setting, **Configuration - Differential**, should be set to **Enabled.** If the winding type in the **SYSTEM CONFIG - Winding Config** is set to **Xformer**, then the settings related to Generator-Transformer differential protection will be displayed in the column **DIFFERENTIAL** - **Xformer Diff**.

The basic pick up level of the low set differential element, **Xform Is1**, is variable between 0.1 pu and 2.5 pu in 0.01 pu steps. The setting chosen is dependant on the item of plant being protected and by the amount of differential current that might be seen during normal operating conditions. A default setting of 0.2 pu is generally recommended.

The biased low-set differential protection is blocked under magnetizing inrush conditions and during transient over fluxing conditions if the appropriate settings are enabled. The second harmonic measurement and blocking are phase segregated. If cross blocking is set to enabled, phases A, B and C of the low set differential element are blocked when an inrush condition is detected. The fifth harmonic measurement and blocking are also phase segregated, but no cross blocking is available.

As shown in Figure 28, the first slope is flat and depends on the **Xform Is1** setting. It ensures sensitivity to internal faults. The second slope, **Xform K1**, is user settable. K1 ensures sensitivity to internal faults up to full load current. It allows for the 15% mismatch which can occur at the limit of the transformer's tap-changer range and an additional 5% for any CT ratio errors. The K1 slope should be set above the errors due to CT mismatch, load tap changers and steady state magnetizing current. The errors slope, which is the combined tap changer (T/C) and current transformer (CT) error, should always be below the K1 slope to avoid mal operations. It is recommended to set K1 to 30%, as long as the errors slope is below the K1 slope by a suitable margin. The second slope, **Xform K2**, is also user settable, and it is used for bias currents above the rated current. To ensure stability under heavy through fault conditions, which could lead to increased differential current due to asymmetric saturation of CTs, K2 is set to 80%.

Note: The default settings for Xform Is2 (1pu), Xform K1 (30%) and Xform K2 (80%) should always be used as the CT requirements are based on these settings.

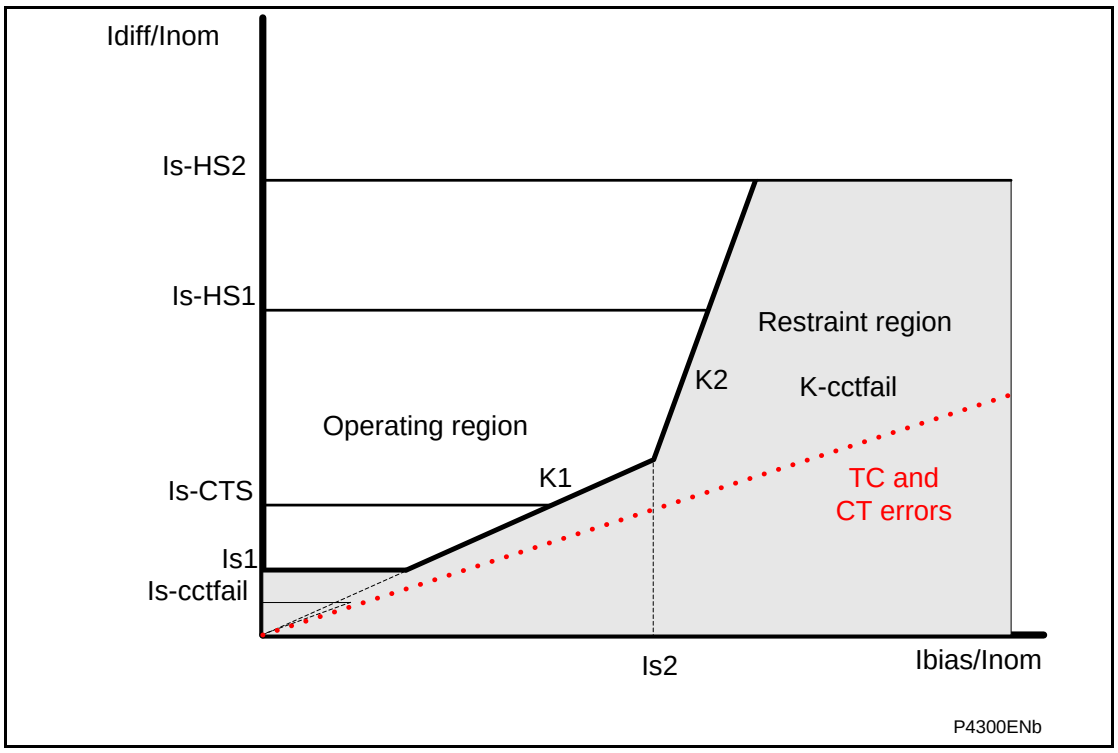


Figure 28: Tap changer and CT combined errors

Example 1: Two winding transformer (P34x) – no tap changer

Figure 29 shows the application of P34x to protect a two winding transformer. The power transformer data is: 90 MVA Transformer, Ynd9, 132/33 kV. The current transformer ratios are as follows: HV CT ratio - 400/1, LV CT ratio - 2000/1.

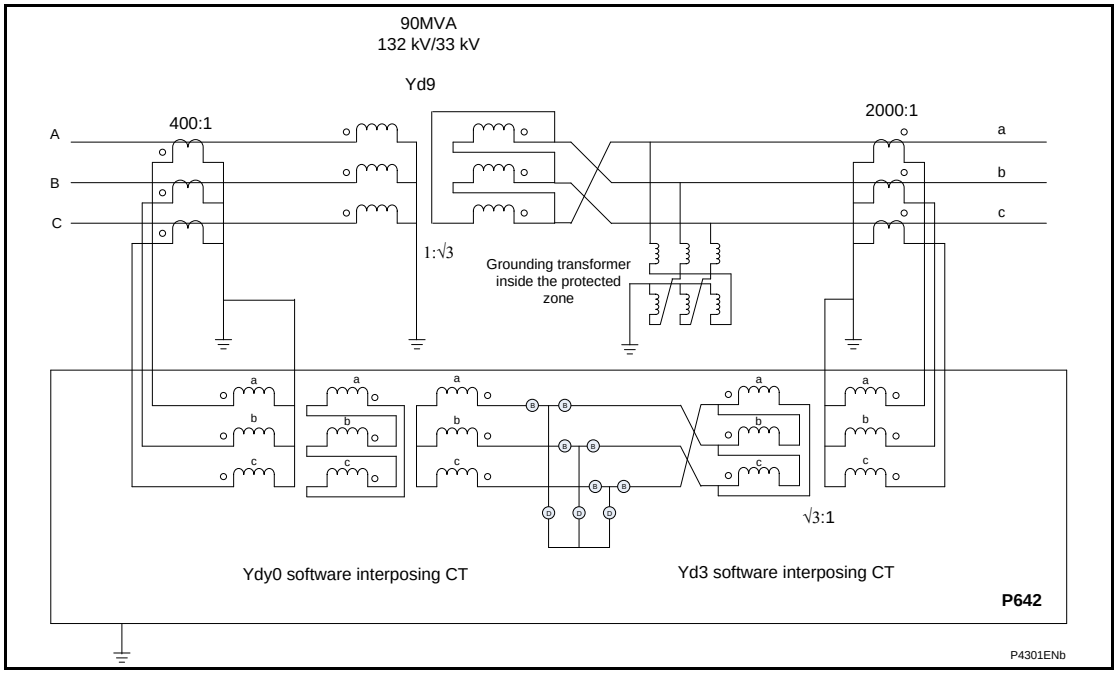


Figure 29: P34x used to protect a Generator-Transformer unit

The relay always calculates and sets the amplitude matching factors. As explained previously no vector correction is applied to the high voltage side. Vector correction is done by setting **SYSTEM CONFIG** then **LV Vector Group to 9**. The zero sequence filtering is done by setting **SYSTEM CONFIG** then **HV Grounding** to **Grounded** and **SYSTEM CONFIG** then **LV Grounding** to **Grounded**. The following screenshot shows the **SYSTEM CONFIG** settings for the P34x.

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Name	Value	Address (C.R)
SYSTEM DATA		
CB CONTROL		
DATE AND TIME		
CONFIGURATION		
CT AND VT RATIOS		
RECORD CONTROL		
DISTURB RECORDER		
MEASURE'T SETUP		
COMMISSION TESTS		
CB MONITOR SETUP		
OPTO CONFIG		
CTRL I/P CONFIG		
FUNCTION KEYS		
SECURITY CONFIG		
CTRL I/P LABELS		
Group 1		
GROUP 1 SYSTEM CONFIG		
Winding Config	Xformer	30.01
Ref Power S	100.0 MVA	30.02
HV Connection	Y-Wye	30.11
HV Grounding	Grounded	30.12
HV Nominal	220.0 kV	30.13
% Reactance	10.00 %	30.20
LV Vector Group	0	30.31
LV Connection	Y-Wye	30.32
LV Grounding	Grounded	30.33
LV Nominal	11.00 kV	30.34
Match Factor HV	1.000 :1	30.40
Match Factor LV	1.000 :1	30.41
Phase Sequence	Standard ABC	30.42
VT Reversal	No Swap	30.43
CT1 Reversal	No Swap	30.44
CT2 Reversal	No Swap	30.45
C/S Input	A-N	30.50
C/S V Ratio Corr	1.000	30.51
C/S VT Vect Grp	0	30.52
Main VT Location	Gen	30.53

Figure 30: P34x SYSTEM CONFIG settings

The ratio correction factors are calculated by the relay as follows:

$$K_{amp,HV} = \frac{I_{nom,HV}}{\frac{S_{ref}}{\sqrt{3}V_{nom,HV}}} = \frac{400}{\frac{90\times10^6}{\sqrt{3}\times132\times10^3}} = 1.016$$

$$K_{amp,LV} = \frac{I_{nom,LV}}{\frac{S_{ref}}{\sqrt{3}V_{nom,LV}}} = \frac{2000}{\frac{90\times10^6}{\sqrt{3}\times33\times10^3}} = 1.270$$

Where:

S_{ref}: common reference power for all ends

K_{am}, HV, LV: ratio correction factor of HV or LV windings
I_{nom}, HV, LV: primary nominal currents of the main current transformers

V_{nom}, HV,LV: primary nominal voltage of HV or LV windings

The recommended settings for the differential function (Xform Is1, Xform Is2, Xform K1, Xform K2, second and fifth harmonic blocking) were discussed in previous sections, and they are as follows:

Name	Value	Address (C.R)
Group 1		
GROUP 1 SYSTEM CONFIG		
GROUP 1 POWER		
GROUP 1 FIELD FAILURE		
GROUP 1 NPS THERMAL		
GROUP 1 SYSTEM BACKUP		
GROUP 1 OVERCURRENT		
GROUP 1 DIFFERENTIAL		
GROUP 1 XFORMER DIFF		37.30
Xform Diff Func	Enabled	37.31
Set Mode	Simple	37.32
Xform Is1	200.0e-3 PU	37.33
Xform K1	30.00 %	37.34
Xform Is2	1.000 PU	37.35
Xform K2	80.00 %	37.36
Xform tDIFF	0 s	37.37
Xform Is-CTS	1.500 PU	37.40
Xform HS1 Status	Enabled	37.41
Xform Is-HS1	10.00 PU	37.42
Xform HS2 Status	Enabled	37.43
Xform Is-HS2	16.00 PU	37.44
Zero seq filt HV	Enabled	37.50
Zero seq filt LV	Enabled	37.51
2nd harm blocked	Enabled	37.52
Xform Ih(2)%>	20.00 %	37.53
Cross blocking	Disabled	37.54
5th harm blocked	Disabled	37.55
Circuitry Fail	Enabled	37.60
Is-cctfail	100.0e-3 PU	37.61
K-cctfail	10.00 %	37.62
CctFail Delay	5.000 s	37.63

Figure 31: P34x Xformer DIFF PROTECTION settings

2.4 NPS overpower (32NP)

For the interturn interlocking logic a single stage negative phase sequence apparent overpower element S2>1 is provided. The 3 phase current source can be selected using the **S2> CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting. In the standard connection diagrams in the installation chapter, *P34x/EN IN*, **IA-1/IB-1/IC-1** is connected to the neutral side CTs and **IA-2/IB-2/IC-2** is connected to the terminal side CTs.

2.4.1 Setting guidelines for NPS overpower

The power pick-up threshold must be set higher than the negative phase sequence apparent power due to the maximum normal load unbalance on the system. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence apparent power, and setting at least 20% above this figure.

This element is applied primarily to provide an interlocking signal for interturn protection. Therefore it is associated with a short time delay, less than the neutral voltage displacement protection operating time. It is recommended that the terminal side CTs should be used for this application.

2.5 Phase fault overcurrent protection (50/51)

A four stage directional/non-directional overcurrent element is provided in the P34x relays. This element can be used to provide time delayed back-up protection for the system and high set protection providing fast operation for machine faults.

In the P343/4/5/6 the 3 phase current source can be selected using the **I> CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting. In the standard connection diagrams in the installation chapter, *P34x/EN IN*, **IA-1/IB-1/IC-1** is connected to the neutral side CTs and **IA-2/IB-2/IC-2** is connected to the terminal side CTs. The overcurrent protection can therefore be selected for the HV or LV winding phase fault protection for generator-transformer applications.

The first two stages have a time delayed characteristic that can be set as either Inverse Definite Minimum Time (IDMT) or Definite Time (DT) or a user curve (Default Curve 1/2/3/4). The third and fourth stages have a definite time delay, which can be set to zero to produce instantaneous operation. Each stage can be selectively enabled or disabled.

2.5.1 Application of timer hold facility

This feature may be useful in certain applications, for example when grading with electromechanical overcurrent relays which have inherent reset time delays. It will also enable the element to become sensitive to a pole slipping condition where the element will cyclically operate as the machine slips successive poles.

Another situation where the timer hold facility may be used to reduce fault clearance times is where intermittent faults may be experienced. When the reset time of the overcurrent relay is instantaneous the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the timer hold facility the relay will integrate the fault current pulses, thereby reducing fault clearance time.

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2.5.2 Setting guidelines for overcurrent protection

The first and second stage of overcurrent protection can be selected by setting **I>1/2 Function** to any of the inverse or DT settings. The first and second stage is disabled if **I>1/2 Function** is set to **Disabled**.

Programmable operate curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves. Programmable reset curves can be used to match more closely the reset characteristic of electromechanical relays. If a user curve **Default 1/2/3/4** is selected for the overcurrent operate or reset characteristic then in the **User Curves** menu the **UserCurve1/2/3/4** Type setting should be chosen to match the template of the curve downloaded from the S1 Agile User Programmable Curve tool. For an overcurrent application the **UserCurve1/2/3/4 Type - Operate 1.0 or Reset 1.1** would normally be selected for the operate or reset characteristic respectively.

The first or second stage can provide back-up protection for faults on the generator and the system. As such it should be coordinated with downstream protection to provide discrimination for system faults, setting the current threshold (**I>1/2 Current Set**), and the time delay.

I>1 TMS – For IEC curves;

I>1 Time Dial – For US/IEEE curves;

I>1 Time Delay – For definite time accordingly.

To provide back-up protection for the generator and system, the element must be supplied from CTs connected in the generator tails (neutral). If terminal end CTs are used, the element will provide protection for the system only, unless the generator is connected in parallel to a second source of supply.

The third and fourth stages of overcurrent protection can be enabled by setting **I>3/4 Function** to DT, providing a definite time operating characteristic. The third and fourth stages are disabled if **I>3/4 Function** is set to **Disabled**. Where terminal CTs are used, the third or fourth stage can be set as an instantaneous overcurrent protection, providing protection against internal faults on the machine. The current setting of the third or fourth

stage, **I>3/4 Current Set**, could be set to 120% of the maximum fault rating of the generator, typically 8 x full load current. The operating time, **I>3/4 Time Delay**, should be set to 0s to give instantaneous operation. The stage will therefore be stable for external faults where the fault current from the generator will be below the stage current setting. For faults within the machine, the fault current will be supplied from the system and will be above the second stage current setting, resulting in fast clearance of the internal fault.

For generator-transformer applications the overcurrent protection can be selected for the HV or LV winding phase fault protection using the **I> CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting.

Directional overcurrent protection is not generally required for generator applications as the generator neutral CTs are normally used for overcurrent protection but it is included for consistency with other products.

2.6 Negative phase sequence (NPS) overcurrent protection (46OC)

When applying traditional phase overcurrent protection, the overcurrent elements must be set higher than maximum load current, thereby limiting the element's sensitivity. Most protection schemes also use an earth fault element, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes.

Any unbalanced fault condition will produce negative sequence current of some magnitude. Therefore a negative phase sequence overcurrent element can operate for both phase-phase and phase-earth faults.

The following section describes how negative phase sequence overcurrent protection may be applied in conjunction with standard overcurrent and earth fault protection to alleviate some less common application difficulties.

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- Negative phase sequence overcurrent elements give greater sensitivity to resistive phase to phase faults, where phase overcurrent elements may not operate. Voltage dependent overcurrent and underimpedance protection is commonly used to provide more sensitive back-up protection for system phase faults on a generator than simple overcurrent protection. However, negative phase sequence overcurrent protection can also be used to provide sensitive back-up protection for phase-phase faults.

  Note: NPS overcurrent protection will not provide any system back-up protection for three-phase faults.

- In certain applications, residual current may not be detected by an earth fault relay due to the system configuration. For example, an earth fault relay applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side.

However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore a negative phase sequence overcurrent element may be employed to provide time-delayed back-up protection for any uncleared asymmetrical faults downstream.

- For rotating machines a large amount of negative phase sequence current can be a dangerous condition for the machine due to its heating effect on the rotor. Therefore a negative phase sequence overcurrent element may be applied to provide back-up protection to the negative phase sequence thermal protection that is normally applied to a rotating machine, see section 2.15.

- It may be required to simply alarm for the presence of negative phase sequence currents on the system. Operators may then investigate the cause of the unbalance.

- A directional negative phase sequence overcurrent element can be used to prevent maloperation of the zero sequence overvoltage protection used to provide interturn protection for a system earth or phase-phase fault, see section 2.2.3.4.

2.6.1 Setting guidelines for NPS overcurrent protection

In the P343/4/5/6 the 3 phase current source can be selected using the **I2> CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting. In the standard connection diagrams in the installation chapter, *P34x/EN IN*, **IA-1/IB-1/IC-1** is connected to the neutral side CTs and **IA-2/IB-2/IC-2** is connected to the terminal side CTs. The NPS overcurrent protection can therefore be selected for the HV or LV winding phase fault protection for generator-transformer applications. When directional NPS overcurrent protection is used with the neutral voltage and NPS overpower for generator interturn protection the terminal side CTs should be used, see section 2.2.3.4.1.

The current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load unbalance on the system. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence current, and setting at least 20% above this figure.

Where the negative phase sequence element is required to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

Note: If the required fault study information is unavailable, the setting must adhere to the minimum threshold previously outlined, employing a suitable time delay for coordination with downstream devices. This is vital to prevent unnecessary interruption of the supply resulting from inadvertent operation of this element.

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As stated above, correct setting of the time delay for this function is vital. It should also be noted that this element is applied primarily to provide back-up protection to other protective devices or to provide an alarm or used in conjunction with neutral voltage displacement protection and NPS overpower protection for interturn protection. Therefore in practice, it would be associated with a long time delay if used to provide back-up protection or an alarm. If this protection is used as a directional NPS overcurrent element in conjunction with neutral voltage displacement and NPS overpower for interturn protection then a short time delay (less than the neutral voltage displacement operating time) is desirable to ensure stability for external earth or phase-phase faults.

Where the protection is used for back-up protection or as an alarm it must be ensured that the time delay is set greater than the operating time of any other protective device (at minimum fault level) on the system which may respond to unbalanced faults, such as:

- Phase overcurrent elements
- Earth fault elements
- System back-up protection - voltage dependent overcurrent/underimpedance
- Broken conductor elements
- Negative phase sequence influenced thermal elements

2.6.2 Directionalizing the negative phase sequence overcurrent element

To determine if a phase-phase or phase-earth fault is internal or external to the machine directional control of the element should be employed.

Directionality is achieved by comparison of the angle between the inverse of the negative phase sequence voltage (-V2) and the negative phase sequence current (I2). The element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (I2> Char. Angle) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (-V2), in order to be at the center of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent on the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the RCA should be set equal to –60°.
- For a distribution system the RCA should be set equal to –45°.

For the negative phase sequence directional elements to operate, the relay must detect a polarizing voltage above a minimum threshold, **I2> V2pol Set**. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the relay.

2.7 System back-up protection (51V/21)

A generator is a source of electrical power and will supply system faults until they are cleared by system protection. Back-up protection must be applied at the generator so that faults are cleared in the event of downstream protection/circuit breakers failing to operate.

The fault current supplied by a generator will vary during a fault condition as indicated by the generator decrement curve, shown in Figure 32. The fault current response is determined by the action of the automatic voltage regulator on the machine. With some generators, fault current initiates an AVR 'boost' circuit that maintains the fault current at a relatively high level. If the voltage regulator is set to manual control or no boost circuit exists, the fault current can be severely restricted, leading to slow operation of back-up protection for system faults. In the worst case the fault current will fall below the full load rating of the machine, so simple overcurrent protection with a setting above full load current, cannot operate.

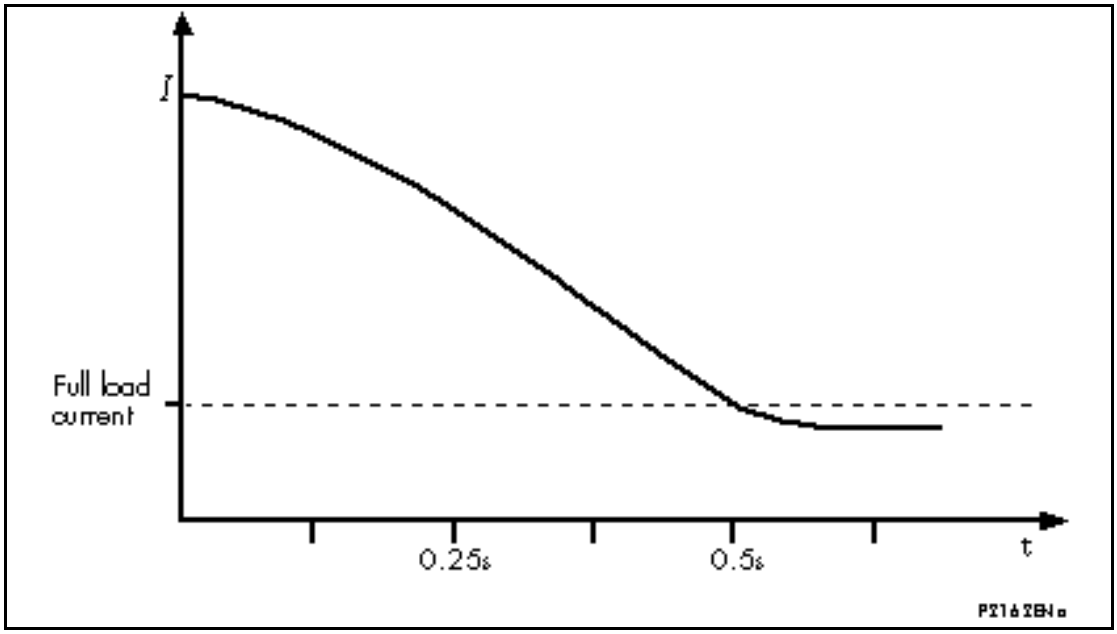


Figure 32: Typical generator fault current decrement curve

System back-up protection must operate quickly during a fault and must not operate for load conditions. To achieve these two objectives, two methods of system back-up protection are commonly used:

1. Voltage dependant overcurrent protection. The presence of a fault is detected by an under voltage element and the relay setting is adjusted accordingly. Voltage dependant overcurrent protection can be operated in a 'voltage controlled' or 'voltage restrained' mode.
2. Under impedance protection. This element is set to monitor the system impedance at the terminals of the machine. If the impedance measured falls below a set threshold then the element will operate.

Customer preference will determine the mode of operation. However, subtle application benefits can be claimed for one form of protection over the other in certain circumstances.

Voltage dependant overcurrent and under impedance are provided in the P34x relay for system back-up protection. The operation of the elements are described in the following sections.

The functions operate from the phase currents measured by the IA, IB and IC measurement inputs on the relay.

2.7.1 Voltage dependant overcurrent protection

The generator terminal voltage will drop during fault conditions and so a voltage measuring element can be used to control the current setting of this element. On detection of a fault the current setting is reduced by a factor K. This ensures faults are cleared in spite of the presence of the generator decrement characteristic. Line voltages are used to control each phase overcurrent element as shown in Table 4.

Phase current	Control voltage
Ia	Vab
Ib	Vbc
Ic	Vca

Table 4: Control voltages for phase currents

A single stage, non-directional overcurrent element is provided. The element has a time delayed characteristic that can be set as either Inverse Definite Minimum Time (IDMT) or Definite Time (DT) or a user curve (Default Curve 1/2/3/4). A user reset curve can also be selected. The element can be fed from CTs at the terminal or neutral end of the generator.

The element can be set in one of two modes, voltage controlled overcurrent or voltage restrained overcurrent. Where the generator is directly connected to a busbar, voltage controlled overcurrent protection may be preferred.

2.7.1.1 Setting guidelines for voltage controlled overcurrent function

Voltage controlled overcurrent protection can be selected by setting **V Dep OC Func** to **Voltage Controlled**. The protection is disabled if **V Dep OC Func** is set to **Disabled**.

The current setting, **V Dep OC I> Set**, should be set to have a primary operating value in excess of the maximum generator load current.

The current setting multiplying factor, **V Dep OC k Set**, governs the protection function setting under low voltage conditions. This should be set to give a primary operating current less than 50% of the minimum steady-state fault current for a multi-phase fault at the remote end of a feeder, with the generator being the only source. This ensures the element will provide adequate back-up protection for an uncleared fault on that feeder.

The voltage-controlled protection fault characteristic should coordinate with outgoing feeder protection for a feeder fault under minimum plant conditions. The operating characteristic, **V Dep OC Char** and the time delay (**V Dep OC TMS** – for IEC curves; **V Dep OC T Dial** – for US/IEEE curves; **V Dep OC Delay** for definite time) should be selected accordingly.

Programmable operate curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves. Programmable reset curves can be used to match more closely the reset characteristic of electromechanical relays. If a user curve **Default 1/2/3/4** is selected for the voltage dependant operate or reset characteristic then in the **User Curves** menu the **UserCurve1/2/3/4 Type** setting should be chosen to match the template of the curve downloaded from the S1 Agile User Programmable Curve tool. For a voltage dependant overcurrent application the **UserCurve1/2/3/4 Type – Operate 1.0 or Reset 1.1** would normally be selected for the operate or reset characteristic respectively.

Where parallel sources are present, a remote feeder fault may not result in a sufficient voltage reduction to enable the fault characteristic. For such applications a time undervoltage element can be used to clear the fault (see section 2.8). Alternatively, negative sequence thermal protection could be used (see section 2.15).

The voltage setting for switching between load and fault characteristics, **V Dep OC V<1 Set**, should be greater than the terminal voltage for a fault where back-up protection is required. On a solidly earthed system the element can be made insensitive to earth faults by ensuring that the voltage setting is below 57%Vn (minimum phase to phase voltage for a single phase to earth fault). A typical setting would be 30%Vn. A voltage setting higher than 57%Vn will allow the relay operating characteristic to change for both phase and earth faults.

More accurate settings may be determined with reference to the following equations.

The minimum fault current for a remote-end multi-phase fault on a feeder can be determined as follows. This calculation is based on no-load excitation being applied and no field-forcing or AVR action during the fault.

Three-phase fault:

$$I_f = \frac{E_n}{\sqrt{(nR_f)^2 + (X_S + nX_f)^2}}$$

Phase to phase fault:

$$I_f = \frac{\sqrt{3E_n}}{\sqrt{(2nR_f)^2 + (X_S + X_2 + 2nX_f)^2}}$$

Where:

I_f = Minimum generator primary current seen for a multi-phase feeder-end fault

E_n = No-load phase-neutral internal e.m.f. of generator

X_s = Direct-axis synchronous reactance of the generator

X_2 = Negative phase sequence reactance of the generator

R_f = Feeder positive phase sequence resistance

X_f = Feeder positive phase sequence reactance

n = Number of parallel generators

The steady-state voltage seen by the relay under external fault conditions can be deduced as follows:

Three-phase fault:

$$V_{\varnothing\text{-}\varnothing} = \frac{E_n \sqrt{3\left((nR_f)^2 + (nX_f)^2\right)}}{\sqrt{(nR_f)^2 + (X_S + nX_f)^2}}$$

Phase-phase fault:

$$V_{\varnothing\text{-}\varnothing} = \frac{2E_n \sqrt{3\left((nR_f)^2 + (nX_f)^2\right)}}{\sqrt{(2nR_f)^2 + (X_S + 2nX_f)^2}}$$

The current setting multiplier, **V Dep OC k Set**, must be set such that **V Dep OC k Set** x **V Dep OC I Set** is less than If as calculated above. The voltage setting, **V Dep OC V<1 Set**, must be greater than. $V_{\varnothing\text{-}\varnothing}$ as calculated above.

The voltage controlled overcurrent protection is provided with a timer hold facility. Setting the hold timer to a value other than zero delays the resetting of the protection element timers for this period.

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2.7.1.2 Voltage vector transformation for use with delta-star transformers

To improve the sensitivity of the voltage dependant overcurrent and underimpedance protection function, for HV phase-phase faults fed via a Yd1 or Yd11 step-up transformer, the appropriate voltage signal transformation facility should be switched in as part of the P34x settings. In the past, such correction of voltage signals has been addressed by adopting phase-neutral voltage measurement or the use of a star/delta interposing VT. Such an approach cannot be adopted with P34x since the relay voltage inputs are common to other protection and measurement functions that would be undesirably affected by voltage signal correction.

If a generator is connected to a busbar through a delta-star step-up transformer, a solid phase-phase fault on the high voltage (HV) busbar will only result in a partial phase-phase voltage collapse at the generator terminals. The voltage dependent overcurrent and underimpedance functions (51 V/21) may not be sensitive enough to detect such faults. On the other hand, a phase-earth fault on the HV side would yield a low phase-phase voltage on the delta side, and the (51 V/21) may respond inappropriately. Such faults should be dealt with by the HV earth fault protection.

In order for the voltage dependent overcurrent function to coordinate correctly with other relays on the system, where there is a delta-star step-up transformer, an internal voltage vector transformation feature is provided. This allows the 51V/21 protection to make use of derived voltages with the same phase-phase relationship as the HV side voltages.

If the **Delta-Star** setting option is selected for the **Vector Rotation** setting, the voltage dependencies for the three voltage dependent overcurrent or underimpedance elements are as follows. The voltage dependencies are for a Yd11 step-up transformer, however, the voltage magnitudes are also applicable for a Yd1, Yd5 or Yd7 step-up transformer application.

For Ia or Za V = magnitude (Vab - Vca)/√3

For Ib or Zb V = magnitude (Vbc - Vab)/√3

For Ic or Zc V = magnitude (Vca - Vbc)/√3

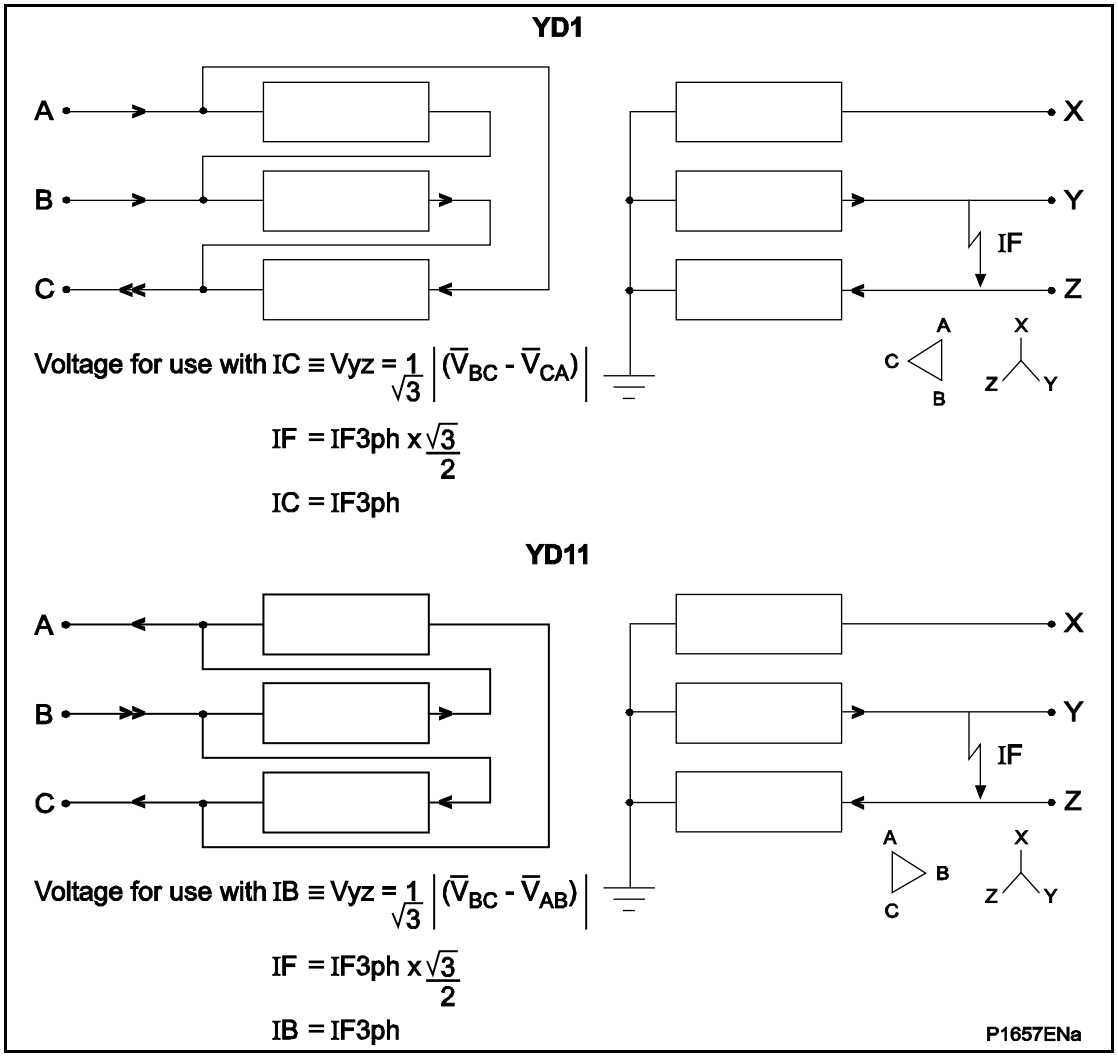


Figure 33: Voltage vector transformation for a delta-star transformer

2.7.1.3 Setting guidelines for voltage restrained overcurrent function

Voltage restrained overcurrent protection can be selected by setting **V Dep OC Func** to **Voltage Restrained**. The protection is disabled if **V Dep OC Func** is set to **Disabled**.

The performance criteria on which the settings of the voltage-restrained overcurrent protection function should be based are similar to those discussed for the voltage controlled mode in section 2.7.1.1. Coordination with downstream protection should be ensured when the relay is on its most sensitive settings i.e. for voltages less than the **V Dep OC V<2 Set** setting. Current threshold, characteristic and time delay can be selected as described for the Voltage Controlled function described in section 2.7.1.1.

The voltage restrained overcurrent function should be able to respond to a remote-end fault on an outgoing feeder. Where the generator is connected via a step up transformer, zero sequence quantities will not be present at the relay location for HV side earth faults. Therefore it would be normal to use negative sequence thermal or NPS overcurrent protection for back-up protection in this case. The negative phase sequence thermal and NPS overcurrent elements will also provide back-up protection for phase to phase faults. For this reason, consideration will only be given to the detection of a remote-end three-phase feeder fault, with the protected machine as the only source.

For a remote-end, three-phase fault, it is possible to calculate the level of current and voltage at the relay location. Ensure the relay current setting, **V Dep OC k Set** x **V Dep OC I Set**, is set to less than 50% of the fault current. Also, set the voltage threshold, **V Dep OC V<2 Set** to a value above the voltage measured at the relay.

There would be no need for further reduction in the current setting for closer faults, which would yield higher currents and lower voltages. Further reduction in the current setting for closer faults may make coordination with local feeder overcurrent protection more difficult (if this is not already a problem).

The steady-state primary current and voltage magnitudes seen for a feeder remote-end three-phase fault are given as follows:

Where:

I_f = Minimum generator primary current seen for a multi-phase feeder-end fault

E_n = No-load phase-neutral internal e.m.f. of generator

X_s = Direct-axis synchronous reactance of the generator

X_2 = Negative phase sequence reactance of the generator

X_t = Step-up transformer reactance

R_f = Feeder positive phase sequence resistance

X_f = Feeder positive phase sequence reactance

n = Number of parallel generators

All above quantities refer to the generator side of the transformer.

The upper voltage threshold setting, **V Dep OC V<1 Set**, should be set below the minimum corrected phase-phase voltage level for a close-up HV earth fault, to ensure that the element is insensitive to the fault. In the case of HV solid earthing, this voltage would be a minimum of 57% of the nominal operating voltage.

The voltage restrained overcurrent protection is provided with a timer hold facility, as described in section 2.7.1.1. Setting the hold timer to a value other than zero, delays the resetting of the protection element timers for this period.

2.7.2 Under impedance protection

Under impedance protection is an alternative to voltage dependent overcurrent protection and is often preferred due to its ease of setting. The definite time delay may be difficult to provide coordination with downstream inverse time overcurrent protections but will be easier to coordinate with distance protection.

The impedance measurement is based on phase-phase voltage and phase-neutral current. This is to make the protection immune to earth faults on the low voltage side of the generator-transformer or for a machine directly connected to the busbars. The main purpose is to provide back-up protection for phase-phase and three-phase faults. Earth fault protection should be allowed to clear earth faults.

The underimpedance protection has 2 stages of impedance protection. For generator transformer applications one stage could be used to reach into the step-up transformer and one stage to reach further into the power system to provide 2 zones of protection.

2.7.2.1 Setting guidelines for under impedance function

Under impedance protection can be selected by setting **Z< Function** to **Enabled**. Each stage can be enabled independently if **Z<1/ Status** is set to **Enabled.** As phase-phase voltage is used in the measurement of impedance the impedance settings should be increased by a factor of √3 to account for this for directly connected machines as well as indirectly (transformer) connected machines. For machines connected to the busbars via a delta-star step-up transformer the **Delta-Star** setting option should be selected in the **Vector Rotation** setting, see section 2.7.1.2.

The first stage impedance setting, **Z<1 Setting**, should be set to 70% of the maximum load impedance. This gives an adequate margin for short time overloads, voltage variation etc., whilst giving adequate back-up protection for generator, generator-transformer and busbar faults.

For example $Z<1 = \sqrt{3} \times 0.7 \times \left(\frac{Vph - n}{Iflc \times 1.2} \right)$

allowing for a 20% overload of the generator full load current.

The second stage impedance setting **Z<2 Setting**, could be set to 50 - 60% of the generator-transformer impedance. This stage can then be used to obtain faster operation for faults closer to the generator.

The time delay, **Z<1 Time Delay** should allow coordination with downstream overcurrent and distance protection devices and with the zone 2 underimpedance protection. The time delay, **Z<2 Time Delay** should allow coordination with generator and transformer LV phase fault protection.

The under impedance protection is provided with a timer hold facility, as described in section 2.7.1.1. Setting the hold timer, **Z< tRESET**, to a value other than zero, delays the resetting of the protection element timer for this period.

2.8 Undervoltage protection function (27)

Undervoltage protection is not a commonly specified requirement for generator protection schemes. However, undervoltage elements are sometimes used as interlocking elements for other types of protection, such as field failure. In the P34x, this type of interlocking can be arranged via the relay scheme logic. Undervoltage protection may also be used for back-up protection where it may be difficult to provide adequate sensitivity with voltage dependant/underimpedance/negative phase sequence elements.

For an isolated generator, or isolated set of generators, a prolonged undervoltage condition could arise for a number of reasons. One reason would be failure of automatic voltage regulation (AVR) equipment. Where an auxiliary transformer is used to supply generator ancillary equipment, such as boiler-feed pumps, air-blowers, lubrication pumps etc., a prolonged undervoltage condition could adversely affect the performance of the machine. If such a situation is envisaged, the application of time-delayed undervoltage protection might be a consideration.

Increased integration of renewable power generation (e.g. wind farms) into power networks has resulted in the evolution of grid codes with new protection requirements. Many new power system transmission codes require generators to remain stable and connected on-line to the network when faults occur on the transmission network. Otherwise, the power system would be exposed to a greater loss of generation and unless enough reserve capacity from other power plants can balance the generation shortfall, the consequences include danger of a rapid drop in system frequency, necessitation of load shedding and ultimately system collapse. This is known as fault ride-through capability (FRT). An example fault ride through characteristic is shown in Figure 73. Generators are required to stay on line while the voltage is depleted for a fault at the Generating Station HV bus or further downstream from the station on the transmission lines. Complete loss of voltage at the generator terminals prevents prime mover power transmission which can only be transient in nature (hundreds of ms).

To match the complex and country specific fault ride through characteristics, new user programmable curves are included in the P34x for undervoltage protection. A user friendly tool is used to create curves either by formula or by entering up to 256 data points which are then downloaded to the relay. Protection functions used to provide back-up protection for system faults such as underimpedance and voltage dependant overcurrent protection can be set with appropriate time delays and settings to prevent operation for fault ride through requirements. Alternatively, the protection timer can be blocked by the the inverted start signal of the FRT undervoltage characteristic in PSL if required.

2.8.1 Setting guidelines for undervoltage protection

Stage 1 may be selected as either **IDMT** (for inverse time delayed operation), **DT** (for definite time delayed operation) or **Default Curve 1/2/3/4** or **Disabled**, within the **V<1 Function** cell. Stage 2 and 3 are definite time only and are Enabled/Disabled in the **V<2/3 Status** cells. The time delay (**V<1 TMS** - for IDMT curve; **V<1 Time Delay**, **V<2 Time Delay, V<3 Time Delay** - for definite time) should be adjusted accordingly.

To match the complex and country specific fault ride through characteristics a user programmable curve (Default Curve 1/2/3/4) can be selected for V<1 operate characteristic. If a user curve **Default 1/2/3/4** is selected for the undervoltage operate characteristic then in the **User Curves** menu the **UserCurve1/2/3/4** Type setting should be chosen to match the template of the curve downloaded from the S1 Agile User Programmable Curve tool. For an undervoltage application the **UserCurve1/2/3/4 Type - UV Operate 4.0** would normally be selected. The protection timer for back-up protection for system faults such as underimpedance and voltage dependant overcurrent protection can be blocked by the the inverted start signal of the FRT undervoltage characteristic in PSL if required.

The undervoltage protection can be set to operate from **Phase to Phase** or **Phase to Neutral** voltage as selected by **V< Measur't Mode**. Single or three-phase operation can be selected in **V<1 Operate Mode**. When **Any Phase** is selected, the element will operate if any phase voltage falls below setting, when **Three-phase** is selected the element will operate when all three-phase voltages are below the setting.

If the undervoltage protection function is to be used for back-up protection, the voltage setting, **V<1 Voltage Set**, should be set above the steady-state phase-phase voltage seen by the relay for a three-phase fault at the remote end of any feeder connected to the generator bus. Allowances should be made for the fault current contribution of parallel generators, which will tend to keep the generator voltage up. If the element is set to operate from phase to phase voltages operation for earth faults can be minimized, i.e. set **V< Measur't. Mode** to **Phase-Phase**. To allow detection of any phase to phase fault, **V< Operate Mode** should be set to **Any-Phase**. Equations for determining the phase-phase voltage seen by the relay under such circumstances are given in section 2.7.1.1

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The operating characteristic would normally be set to definite time, set **V<1 Function** to **DT**. The time delay, **V<1 Time Delay**, should be set to coordinate with downstream protections and the System Back-up protection of the relay, if enabled. Additionally, the delay should be long enough to prevent unwanted operation of the under voltage protection for transient voltage dips. These may occur during clearance of faults further into the power system or by starting of local machines. The required time delay would typically be in excess of 3 s - 5 s.

The second and third stages can be used as alarm stages to warn the user of unusual voltage conditions so that corrections can be made. This could be useful if the machine is being operated with the AVR selected to manual control.

Where the relay is used to provide the protection required for connecting the generator in parallel with the local electricity supply system (e.g. requirements of G59 in the UK), the local electricity supply authority may advise settings for the element. The settings must prevent the generator from exporting power to the system with voltage outside of the statutory limits imposed on the supply authority.

To prevent operation of any under voltage stage during normal shutdown of the generator "poledead" logic is included in the relay. This is facilitated by selecting **V Poledead Inh** to **Enabled**. This will ensure that when a poledead condition is detected (i.e. all phase currents below the undercurrent threshold or CB Open, as determined by an opto isolator and the PSL) the undervoltage element will be inhibited.

2.9 Overvoltage protection (59)

A generator terminal overvoltage condition could arise when the generator is running but not connected to a power system, or where a generator is providing power to an islanded power system. Such an over voltage could arise in the event of a fault with automatic voltage regulating equipment or if the voltage regulator is set for manual control and an operator error is made. Overvoltage protection should be set to prevent possible damage to generator insulation, prolonged overfluxing of the generating plant, or damage to power system loads.

When a generator is synchronized to a power system with other sources, an overvoltage could arise if the generator is lightly loaded supplying a high level of power system capacitive charging current. An overvoltage condition might also be possible following a system separation, where a generator might experience full-load rejection whilst still being connected to part of the original power system. The automatic voltage regulating equipment and machine governor should quickly respond to correct the overvoltage condition in these

cases. However, overvoltage protection is advisable to cater for a possible failure of the voltage regulator or for the regulator having been set to manual control. In the case of Hydro generators, the response time of the speed governing equipment can be so slow that transient over speeding up to 200% of nominal speed could occur. Even with voltage regulator action, such over speeding can result in a transient over voltage as high as 150%. Such a high voltage could result in rapid insulation damage.

2.9.1 Setting guidelines for overvoltage protection

Stage 1 may be selected as either **IDMT** (for inverse time delayed operation), **DT** (for definite time delayed operation) or **Default Curve 1/2/3/4** or **Disabled**, within the **V>1 Function** cell. Stage 2 has a definite time delayed characteristic and is Enabled/Disabled in the **V>2 Status** cell. The time delay (**V>1 TMS** - for IDMT curve; **V>1 Time Delay**, **V>2 Time Delay** - for definite time) should be selected accordingly.

Programmable operate curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves. If a user curve **Default 1/2/3/4** is selected for the overvoltage operate characteristic then in the **User Curves** menu the **UserCurve1/2/3/4 Type** setting should be chosen to match the template of the curve downloaded from the S1 Agile User Programmable Curve tool. For an overvoltage application the **UserCurve1/2/3/4 Type – Operate 1.0** would normally be selected for the operate characteristic.

The overvoltage protection can be set to operate from **Phase to Phase** or **Phase to Neutral** voltage as selected by **V> Measur't Mode** cell. Single or three-phase operation can be selected in **V> Operate Mode** cell. When **Any Phase** is selected the element will operate if any phase voltage is above setting, when **Three-phase** is selected the element will operate when all three-phase voltages are above the setting.

Generators can typically withstand a 5% overvoltage condition continuously. The withstand times for higher overvoltages should be declared by the generator manufacturer.

To prevent operation during earth faults, the element should operate from the phase-phase voltages, to achieve this **V>1 Measur't Mode** can be set to **Phase-Phase** with **V>1 Operating Mode** set to **Three-phase**. The overvoltage threshold, **V>1 Voltage S**et, should typically be set to 100% - 120% of the nominal phase-phase voltage seen by the relay. The time delay, **V>1 Time Delay**, should be set to prevent unwanted tripping of the delayed overvoltage protection function due to transient over voltages that do not pose a risk to the generating plant; e.g. following load rejection where correct AVR/Governor control occurs. The typical delay to be applied would be 1 s - 3 s, with a longer delay being applied for lower voltage threshold settings.

The second stage can be used to provide instantaneous high-set over voltage protection. The typical threshold setting to be applied, **V>2 Voltage Set**, would be 130 - 150% of the nominal phase-phase voltage seen by the relay, depending on plant manufacturers' advice. For instantaneous operation, the time delay, **V>2 Time Delay**, should be set to 0 s.

Where the relay is used to provide the protection required for connecting the generator in parallel with the local electricity supply system (e.g. requirements of G59 in the UK), the local electricity supply authority may advise settings for the element. The settings must prevent the generator from exporting power to the system with voltages outside of the statutory limits imposed on the supply authority.

If phase to neutral operation is selected, care must be taken to ensure that the element will grade with downstream protections during earth faults, where the phase-neutral voltage can rise significantly.

2.10 Negative phase sequence (NPS) overvoltage protection (47)

Where an incoming feeder is supplying a switchboard that is feeding rotating plant (e.g. a motor), correct phasing and balance of the ac supply is essential. Incorrect phase rotation could result in any connected machines rotating in the wrong direction. For some hydro machines two-phases can be swapped to allow the machine to rotate in a different direction to act as a generator or a motor pumping water.

Any unbalanced condition occurring on the incoming supply will result in the presence of negative phase sequence (NPS) components of voltage. In the event of incorrect phase rotation, the supply voltage would effectively consist of 100% negative phase sequence voltage only.

For such applications the P34x relay includes a negative phase sequence overvoltage element. This element monitors the input voltage rotation and magnitude (normally from a bus connected voltage transformer). This element could be used as a check for hydro machines that the phase rotation is correct to operate the machine in the selected mode as a generator or motor.

The NPS overvoltage element can also be used to provide an additional check to indicate a phase-earth or phase-phase fault is present for voltage controlled overcurrent protection in the PSL. In this application the NPS overvoltage protection can be accelerated when the CB is closed. Typically, the operating time of the NPS overvoltage start is slowed (typical operating time is <60 ms) to prevent incorrect operation when closing the CB due to pole scattering. However, when the CB is closed there is no need to inherently slow the protection start (typical accelerated operating time is <40 ms). The V2>1 Accelerate: DDB 554 signal connected to the CB Closed 3 Ph: DDB 1043 signal can be used to accelerate the protection start.

2.10.1 Setting guidelines

As the primary concern is normally the detection of incorrect phase rotation (rather than small unbalances), a sensitive setting is not required. In addition, it must be ensured that the setting is above any standing NPS voltage that may be present due to imbalances in the measuring VT, relay tolerances etc. A setting of approximately 15% of rated voltage may be typical.

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Note: Standing levels of NPS voltage (V2) will be displayed in the **Measurements 1** column of the relay menu, labeled **V2 Magnitude**.

Hence, if more sensitive settings are required, they may be determined during the commissioning stage by viewing the actual level that is present.

The operation time of the element will be highly dependent on the application. A typical setting would be in the region of 5 s.

2.11 Underfrequency protection (81U)

Underfrequency operation of a generator will occur when the power system load exceeds the prime mover capability of an islanded generator or group of generators. Power system overloading can arise when a power system becomes split, with load left connected to a set of ‘islanded’ generators that is in excess of their capacity. Such events could be compensated for by automatic load shedding. In this case, underfrequency operation would be a transient condition. In the event of the load shedding being unsuccessful, the generators should be provided with back-up underfrequency protection.

An underfrequency condition, at nominal voltage, may result in some over fluxing of a generator and its associated electrical plant. However, the more critical considerations would be in relation to blade stresses being incurred with high-speed turbine generators; especially steam-driven sets. When not running at nominal frequency, abnormal blade resonance’s can be set up that, if prolonged, could lead to turbine disc component fractures. Such effects can be accumulative and so operation at frequencies away from nominal should be limited as much as possible, to avoid the need for early plant inspections/overhaul. Underfrequency running is difficult to contend with, since there is little action that can be taken at the generating station in the event of overloading, other than to shut the generator down.

Four independent definite time-delayed stages of underfrequency protection are offered. Two additional overfrequency stages can also be reconfigured as underfrequency protection by reprogramming the Programmable Scheme Logic. As well as being able to initiate generator tripping, the underfrequency protection can also be arranged to initiate local load-shedding, where appropriate. Selectable fixed scheme logic is provided to allow each stage

of underfrequency protection to be disabled when the outgoing CB is open, to prevent unnecessary load tripping.

2.11.1 Setting guidelines for underfrequency protection

Each stage of underfrequency protection may be selected as **Enabled** or **Disabled**, within the **F<x Status** cells. The frequency pickup setting, **F<x Setting**, and time delays, **F<x Time Delay**, for each stage should be selected accordingly.

The protection function should be set so that declared frequency-time limits for the generating set are not infringed. Typically, a 10% underfrequency condition should be continuously sustainable.

For industrial generation schemes, where generation and loads may be under common control/ownership, the P34x underfrequency protection function could be used to initiate local system load shedding. Four stage underfrequency/load shedding can be provided. The final stage of underfrequency protection should be used to trip the generator.

Where separate load shedding equipment is provided, the underfrequency protection should coordinate with it. This will ensure that generator tripping will not occur in the event of successful load shedding following a system overload. Two stages of underfrequency protection could be set-up, as shown in Figure 34, to coordinate with multi-stage system load shedding.

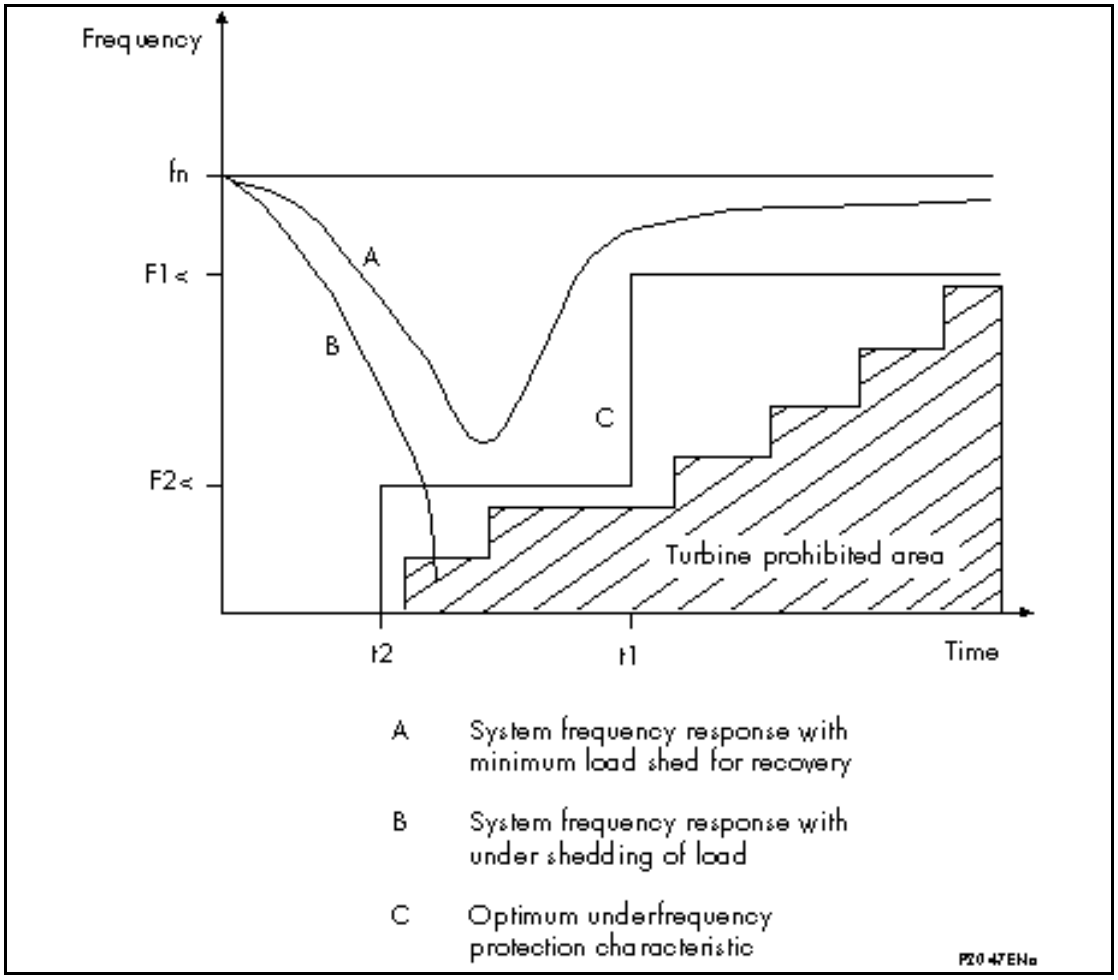


Figure 34: Coordination of underfrequency protection function with system load shedding

To prevent operation of any underfrequency stage during normal shutdown of the generator "poledead" logic is included in the relay. This is facilitated for each stage by setting the relevant bit in **F< Function Link**. For example if **F< Function Link** is set to 0111, Stage 1, 2 and 3 of underfrequency protection will be blocked when the generator CB is open. Selective blocking of the frequency protection stages in this way will allow a single stage of

protection to be enabled during synchronization or offline running to prevent unsynchronized overfluxing of the machine. When the machine is synchronized, and the CB closed, all stages of frequency protection will be enabled providing a multi-stage load shed scheme if desired.

Where the relay is used to provide the protection required for connecting the generator in parallel with the local electricity supply system (e.g. requirements of G59 in the UK), the local electricity supply authority may advise settings for the element. The settings must prevent the generator from exporting power to the system with frequency outside of the statutory limits imposed on the supply authority. Where the local external load exceeds the generator capacity, underfrequency protection may be used to provide 'Loss of Mains' protection.

2.12 Overfrequency protection function (81O)

Overfrequency running of a generator arises when the mechanical power input to the alternator is in excess of the electrical load and mechanical losses. The most common occurrence of overfrequency is after substantial loss of load. When a rise in running speed occurs, the governor should quickly respond to reduce the mechanical input power, so that normal running speed is quickly regained. Overfrequency protection may be required as a back-up protection function to cater for governor or throttle control failure following loss of load or during unsynchronized running.

Moderate overfrequency operation of a generator is not as potentially threatening to the generator and other electrical plant as underfrequency running. Action can be taken at the generating plant to correct the situation without necessarily shutting down the generator.

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Severe overfrequency operation of a high-speed generating set could result in plant damage, as described in section 2.16, as a result of the high centrifugal forces that would be imposed on rotating components.

Two independent time-delayed stages of overfrequency protection are provided.

2.12.1 Setting guidelines for overfrequency protection

Each stage of overfrequency protection may be selected as **Enabled** or **Disabled**, within the **F>x Status** cells. The frequency pickup setting, **F>x Setting**, and time delays, **F>x Time Delay**, for each stage should be selected accordingly.

The P34x overfrequency settings should be selected to coordinate with normal, transient overfrequency excursions following full-load rejection. The generator manufacturer should declare the expected transient overfrequency behavior that should comply with international governor response standards. A typical overfrequency setting would be 10% above nominal.

Where the relay is used to provide the protection required for connecting the generator in parallel with the local electricity supply system (e.g. requirements of G59 in the UK), the local electricity supply authority may advise settings for the element. The settings must prevent the generator from exporting power to the system with frequency outside of the statutory limits imposed on the supply authority.

2.13 Generator turbine abnormal frequency protection (81AB)

Generator sets are normally rated for a lifetime of operation within a defined operating frequency band. Operation outside of this "normal" region can produce mechanical stress in the turbine blades due to their natural resonance and reduce the useful life of the generator. Turbine manufacturers provide accumulative time limits for abnormal frequency operation, usually in the form of a permissible operating time within a specified frequency band. This calls for the use of accumulative time measurements for storing the time spent in running at abnormal speed within each band. These turbine capability limitations generally apply to steam turbine generators.

Six bands of generator abnormal protection are provided within the P34x relays. Each band has its own frequency limit settings and an individual accumulative time measurement. Operation within each of these bands is monitored and the time added to a cumulative timer, stored within the battery backed RAM. This ensures that on loss of auxiliary supply to the relay, the information is not lost. An individual dead band time delay setting is provided for each band. Within this dead band time delay, the frequency is allowed to stay inside the

band without initiating the accumulative time measurement. This delay allows the blade's resonance during under frequency conditions to be established first, therefore avoiding unnecessary accumulation of time. The delay therefore does not contribute to the accumulated time. It is recommended by the IEEE Guide for Abnormal Frequency Protection for Power Generating Plants (IEEE C37.106) to be around 10 cycles. Note that the dead band delay has no effect on the initiation of the start signals. Therefore the start signals can be used during commissioning and maintenance (by setting the dead times temporarily or switching to a different setting group with a high value) to test the frequency band's pick-up and drop-off without adding to the accumulated times. Time accumulation will stop and all the start signals will be reset if the Frequency Not Found DDB 1068 is set.

It is normally recommended that the turbine abnormal frequency protection system should be in-service whenever the unit is synchronized to the system, or while separated from the system but supplying auxiliary load. An inhibit signal is available to inhibit the time accumulation when the generator is off-line, i.e. the circuit breaker is open.

The trip output is latched and can only be reset only if any of the following conditions occur:

1. The accumulative time is reset, or
2. The corresponding band is disabled, or
3. The entire abnormal frequency protection is disabled, or
4. The Inhibit DDB **Turbine F Inh** is energized.

2.13.1 Setting guidelines

The withstand of the generator for abnormal speeds is normally given by the generator manufacturer. Default settings have been provided as a guide for setting the relay.

It is recommended by the IEEE Guide for Abnormal Frequency Protection for Power Generating Plants (IEEE C37.106) that the dead band time delay should be around 10 cycles. This delay allows the blade's resonance during under frequency conditions to be established first, therefore avoiding unnecessary accumulation of time.

The trip signals of the element can be used as either an operator alarm or for shutting down the generator.

2.14 Field failure protection function (40)

Complete loss of excitation may arise as a result of accidental tripping of the excitation system, an open circuit or short circuit occurring in the excitation DC circuit, flashover of any slip rings or failure of the excitation power source. The field failure protection of the P34x consists of two definite time impedance elements, a directional line and a power factor alarm element.

When the excitation of a synchronous generator fails, its internal e.m.f. will decay. This results in the active power output of the machine falling and in an increasing level of reactive power being drawn from the power system. As the active power output falls, the mechanical drive can accelerate the machine so that it will gently pole slip and run at a super synchronous speed. This results in slip frequency currents being induced in the rotor body, damper windings and in the field windings. The slip-induced, low frequency rotor currents will result in a rotor flux being produced. The machine would then be excited from the power system and hence be operating as an induction generator. The ability to reach such a stabilized state will be dependent on the machine’s effective speed-torque characteristic when operating as an induction generator, and also on the power system being able to supply the required reactive power without severe voltage depression.

Stable operation as an induction generator might be achieved at low slip (0.1 - 0.2% above synchronous speed), particularly in the case of salient pole machines. The machine may be able to maintain an active power output (perhaps 20 - 30% of rating) while drawing reactive power from the power system (generating at a highly leading power factor). This condition could probably be sustained for many minutes without rotor damage being incurred and may not be detectable by traditional field failure impedance characteristic elements. The P34x, however, offers a power factor alarm element in the field failure protection which can operate when the generator is running in this condition. A large impedance characterisitc supervised with a directional line may also help to detect this condtion.

Cylindrical rotor machines have a much lower output capability when operating as an induction generator under excitation failure conditions. They are more likely to be pushed over the peak torque level of their induction generator speed-torque characteristic. If the peak induction generator torque level is exceeded, a machine can stabilize at a much higher level of slip (perhaps 5% above synchronous speed). When this happens, the machine will draw a very high reactive current from the power system and a stator winding current as high as 2.0 p.u. may be reached. The slip-frequency rotor currents could lead to rotor core or winding damage if the condition is sustained.

Operation as an induction generator under field failure conditions relies on the ability of the rest of the system being able to supply the required reactive power to the machine. If the system cannot supply enough reactive power the system voltage will drop and the system may become unstable. This could occur if a large generator running at high power suffers a loss of field when connected to a relatively weak system. To ensure fast tripping under this condition one of the impedance elements can be used with a short time delay. This can trip the machine quickly to preserve system stability. This element should have a small diameter to prevent tripping under power swinging conditions. A second impedance element, set with a larger diameter, can provide detection of field failure under lightly loaded conditions. This second element should be time delayed to prevent operation during power swing conditions. If the second impedance element is set very large with a positive reactance offset then a directional line can be used to supervise this element to to avoid unwanted operation during close-in system faults.

The field failure protection impedance elements are also provided with an adjustable delay on reset (delayed drop off) timer. This time delay can be set to avoid delayed tripping that may arise as a result of cyclic operation of the impedance measuring element, during the period of pole slipping following loss of excitation. Some care would need to be exercised in setting this timer, since it could make the field failure protection function more likely to give an unwanted trip in the case of stable power swinging. The impedance element trip time delay should therefore be increased when setting the reset time delay.

The delay on reset timer might also be set to allow the field failure protection function to be used for detecting pole slipping of the generator when excitation is not fully lost; e.g. following time-delayed clearance of a nearby power system fault. This subject is discussed in more detail in section 2.27.

For certain loss of field conditions, the impedance may come in and out of the impedance characteristic several times in a short time not long enough to cause tripping. Therefore, a PSL counter and some PSL logic can be used to count the number of entries of the impedance into the smaller negative offset impedance characteristic. A trip is produced if the number of entries exceeds a count threshold in a set time delay, see section 2.14.2.

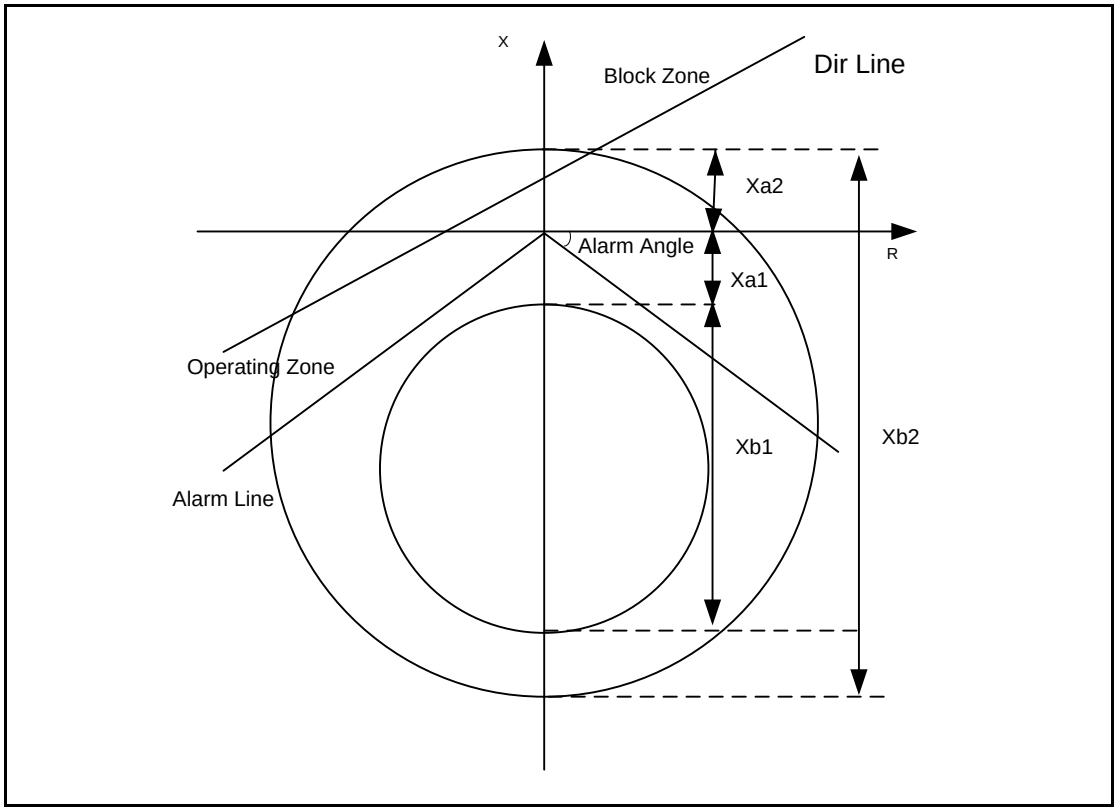


Figure 35: Field failure protection characteristics

2.14.1 Setting guidelines for field failure protection

Each stage of field failure impedance elements and the directional line may be selected as **Enabled** or **Disabled,** within the **FFail1 Status, FFail2 Status** and FFail Dirn Line cells. The power factor alarm element may be selected as Enabled or Disabled within the **FFail Alm Status** cell.

The settings for 2 common field failure protection schemes are described below. Scheme 1 uses 2 negative offset impedance characteristics and scheme 2 uses one positive and one negative offset impedance characteristic supervised by a directional line.

2.14.1.1 Impedance element 1 - Scheme 1

To quickly detect a loss-of field condition, the diameter of the field failure impedance characteristic (**FFail1 Xb1**) should be set as large as possible, without conflicting with the impedance that might be seen under normal stable conditions or during stable power swing conditions.

Where a generator is operated with a rotor angle of less than 90° and never at a leading power factor, it is recommended that the diameter of the impedance characteristic, **FFail1 Xb1**, is set equal to the generator direct-axis synchronous reactance. The characteristic offset, **FFail1 Xa1** should be set with a negative offset equal to half the direct-axis transient reactance (0.5 Xd') in secondary ohms.

FFail1 Xb1 = Xd

FFail1 Xa1 = -0.5 Xd'

Where:

Xd = Generator direct-axis synchronous reactance in ohms

Xd' = Generator direct-axis transient reactance in ohms

Where high-speed voltage regulation equipment is used it may be possible to operate generators at rotor angles up to 120°. In this case, the impedance characteristic diameter, **FFail1 Xb1**, should be set to 50% of the direct-axis synchronous reactance (0.5 Xd) and the offset, **FFail1 Xa1**, should be set with a negative offset equal to 75% of the direct axis transient reactance (0.75 Xd').

FFail1 Xb1 = 0.5 Xd

FFail1 Xa1 = -0.75 Xd'

The field failure protection time delay, **FFail1 Time Delay**, should be set to minimize the risk of operation of the protection function during stable power swings following system disturbances or synchronization. However, it should be ensured that the time delay is not so long that stator winding or rotor thermal damage will occur. A typical stator winding should be able to withstand a current of 2.0 p.u. for the order of 15 s. It may also take some time for the impedance seen at the generator terminals to enter the characteristic of the protection. A time delay less than 10 s would typically be applied. The minimum permissible delay, to avoid problems of false tripping due to stable power swings with the above impedance settings, would be of the order of 0.5 s.

The protection reset (delayed drop off) timer, **FFail1 DO Timer**, would typically be set to 0 s to give instantaneous reset of the stage. A setting other than 0 s can be used to provide an integrating function for instances when the impedance may cyclically enter and exit the characteristic. This can allow detection of pole slipping conditions, for more information see section 2.27. When settings other than 0 s are used the protection pick-up time delay, **FFail1 Time Delay**, should be increased to prevent mal-operation during stable power swing conditions.

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2.14.1.2 Impedance element 2 - Scheme 1

The second impedance element can be set to give fast operation when the field fails under high load conditions. The diameter of the characteristic, **FFail2 Xb2**, should be set to 1 p.u. The characteristic offset, **FFail2 Xa2**, should be set with a negative offset equal to half the direct-axis transient reactance (0.5 Xd').

$$\text{FFail2 Xb2} = \frac{kV^2}{MVA}$$

FFail2 Xa2 = -0.5 Xd'

This setting will detect a field failure condition from full load to about 30% load.

The time delay, **FFail2 Time Delay**, can be set to instantaneous, i.e. 0 s.

The protection reset (delayed drop off) timer, **FFail2 DO Timer**, would typically be set to 0 s to give instantaneous reset of the stage. A setting other than 0 s can be used to provide an integrating function for instances when the impedance may cyclically enter and exit the characteristic. This can allow detection of pole slipping conditions, for more information see section 2.27. When settings other than 0 s are used the protection pick-up time delay, **FFail2 Time Delay**, should be increased to prevent mal-operation during stable power swing conditions.

2.14.1.3 Impedance element 1 and 2 and directional line - Scheme 2

Figure 36 gives an overview of the logic of scheme 2.

The impedance element 2 characteristic is set to coordinate with the steady-state stability limit and the minimum excitation limiter. Typically, the impedance element 2 characteristic has a positive offset equal to the system impedance and a diameter equal to 1.1 Xd.

Ffail2 Xb2 = 1.1Xd

Ffail2 Xa2 = Xs

Xs = System impedance beyond the terminals of the machine.

Since the impedance characteristic has a positive offset, it is supervised by a directional line in PSL to prevent pickup for close-up faults on the system. The directional Line is ON when the impedance is above the line and can be used to block the impedance elements in PSL as shown in Figure 36. The field failure directional line includes a reactance offset, **Line Offset** and **Line Angle** setting. Typically, the offset is set to zero ohms and line angle is -13°.

Line Offset = 0Ω

Line Angle = -13°

In this scheme during abnormally low excitation conditions, such as might occur following a failure of the minimum excitation limiter, the impedance characteristic below the directional line operates and sounds an alarm, allowing a station operator to correct the condition, In the PSL logic below the FFail2 Start operates the alarm and the FFail2 Inh signal operated from the FFail Line Start signal blocks the FFail2 Start. In many cases, this also starts a timer to trip the unit (Field Fail2 Trip) if the condition cannot be corrected before the unit goes unstable or is damaged. Normally a trip occurs after a 1 minute delay (**FFail2 Time Delay** = 60s).

Should a low-voltage condition also exist, indicating a complete loss-of-field condition where the connected system is not capable of supplying adequate reactive power, an undervoltage element will operate and initiate tripping with a time delay of 0.25s to 1.0s. The shorter time is used if there is no impedance element 1. The longer time is used if two impedance characteristics are used. The undervoltage element is typically set to 0.8 pu to 0.9 pu of machine rating. An undervoltage start signal, V<1 Start, and a PSL timer T1 can be used for this logic, see Figure 36.

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A modification of the undervoltage element is applied for hydro generators. If the generator is in a synchronous condenser application then the machine is operated underexcited and draws reactive power from the system. To prevent unnecessary operation, an undervoltage element may be used to supervise the impedance scheme. In such an application the undervoltage element is set to 90% to 95% of rated voltage and the undervoltage start signal is set to block the field failure trip and the reset is set to permit the trip. This combination will provide protection for almost all loss-of-field conditions but may not trip when the generator is operating at light load, since the voltage reduction may not be sufficient to cause an undervoltage reset. This logic can be applied using the PSL if required but is not shown in the PSL below.

Impedance element 1 (Field Fail 1 Trip) is co-ordinated with the steady state stability limit of the generator and the settings of this element are similar to those of impedance element 2 in scheme 1. The diameter of the characteristic, **FFail1 Xb2,** should be set to 1 p.u. The characteristic offset, **FFail2 Xa1**, should be set with a negative offset equal to half the direct-axis transient reactance (0.5 Xd').

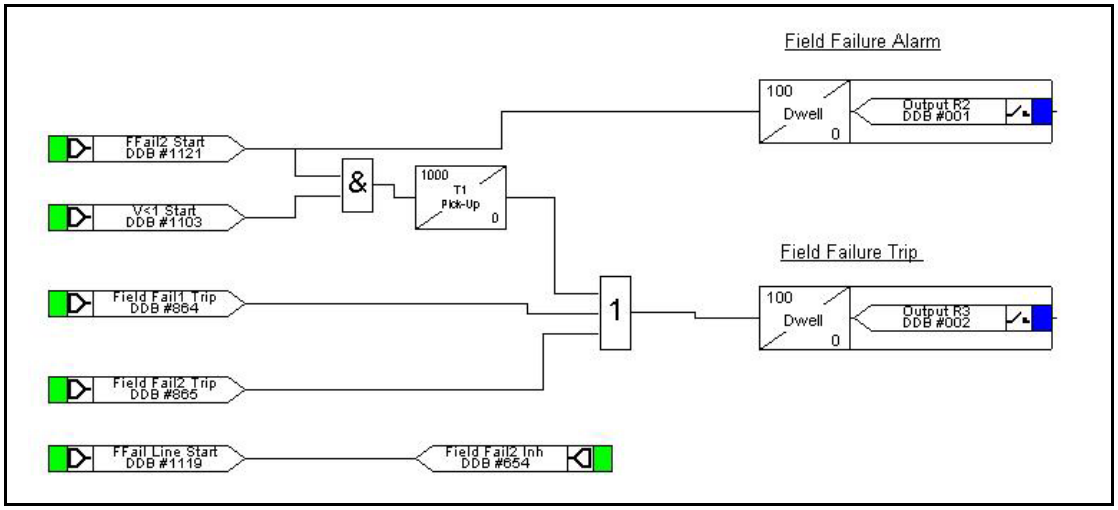


Figure 36: Field failure tripping and alarm logic - Scheme 2

2.14.2 Field failure counting scheme logic

For certain loss of field conditions, the impedance may come in and out of the impedance characteristic several times in a short time not long enough to cause tripping. Therefore, a PSL counter and some PSL logic can be used to count the number of entries of the impedance into the smaller negative offset impedance characteristic. A trip is produced if the number of entries exceeds the count threshold in a set time delay (Timer 1, T1). The Timer 1 typical setting range is 10s to 120s and the Counter 1 typical setting range is 1-50 for this application.

An example of the PSL counting logic using the FFail1 element is shown below. The same logic can be used using the FFail 2 element also if required.

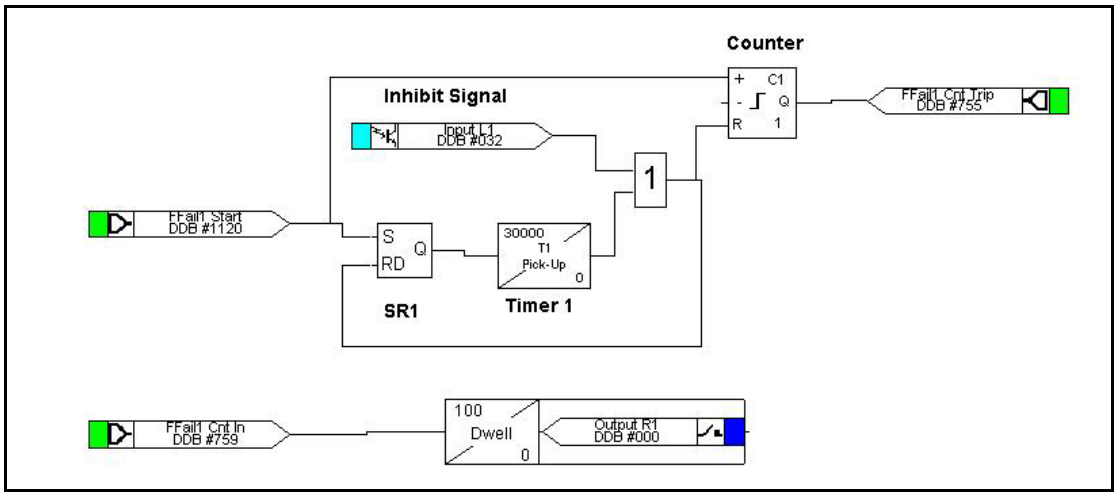


Figure 37: Field failure protection using a counter

The PSL logic is shown in Figure 37. The logic is described below.

1. A counter pulse is triggered via the field failure 1 start signal (DDB 1120, FFail1 Start).
2. The Inhibit signal can be from a digital input, e.g. Input 1 in the PSL example.
3. Counter1 is used to count the number of entries into the FFail1 impedance characteristic. The counter output triggers the alarm signal (DDB755 FFail1 Cnt Trip). This signal will operate the alarm if the counter value is equal or greater than the threshold. It is reset by the inhibit signal and Timer1. The FFail1 Cnt Trip (DDB755) triggers an alarm message in the fault record and triggers the DDB 759, FFail1 Cnt In, which can be used to operate an output contact.
4. Timer1 is the counting window (T1). It is initiated by the first entry into FFail1 element. Counter1 will reset if Timer1 expires.
5. Set-Reset gate, SR1 is to latch the first FFail1 start signal and the output starts the Timer1. It is reset by the inhibit signal and Timer1.

2.14.2.1 Power factor element

Salient pole machines can run continuously as induction generators generating significant power and operation under these conditions may not be detectable by an impedance characteristic. The power factor alarm can be used to signal to the operator that excitation has failed under these conditions.

The angle setting, **FFail Alm. Angle**, should be set to greater than any angle that the machine could be operated at in normal running. A typical setting would be 15°, equivalent to a power factor of 0.96 leading. The power factor element time delay, **FFail Alm Delay**, should be set longer than the impedance element time delay setting (**FFail1 Time Delay**). This is to prevent operation of the alarm element under transient conditions such as power swinging and to provide discrimination where a field failure condition may not be detected by conventional field failure impedance elements.

2.15 Negative phase sequence thermal protection (46T)

Unbalanced loading results in the flow of positive and negative sequence current components. Load unbalance can arise as a result of single-phase loading, non-linear loads (involving power electronics or arc furnaces, etc.), uncleared or repetitive asymmetric faults, fuse operation, single-pole tripping and reclosing on transmission systems, broken overhead line conductors and asymmetric failures of switching devices. Any negative phase sequence component of stator current will set up a reverse-rotating component of stator flux that passes the rotor at twice synchronous speed. Such a flux component will induce double frequency eddy currents in the rotor, which can cause overheating of the rotor body, main rotor windings, damper windings etc.

Where a machine has a high continuous negative phase sequence current withstand level (I_2 amp), as in the case of typical salient-pole machines, it would not be essential to enable the NPS protection function. The NPS protection function can, however, offer a better method of responding to an uncleared asymmetric fault remote from the generator bus. As mentioned in section 2.7.1.3, it may be difficult to set the voltage dependant overcurrent protection function to detect a remote fault and co-ordinate with feeder backup protection for a close-up three-phase fault.

For high levels of negative phase sequence current, eddy current heating can be considerably in excess of the heat dissipation rate. Therefore virtually all the heat acquired during the period of unbalance will be retained within the rotor. With this assumption, the temperature attained within any critical rotor component will be dependent on the duration of the unbalance (t seconds) and the level of NPS current (I_2 per unit) and is proportional to I_2^2t. Synchronous generators are assigned a per-unit I_2^2t thermal capacity constant (Kg) to define their short time NPS current withstand ability, see column 3 in Table 1. Various rotor components have different short time thermal capacities and the most critical (lowest value of I_2^2t) should form the basis of the generator manufacturer's short time I_2^2t withstand claim.

Many traditional forms of generator NPS thermal protection relays have been designed with an extremely inverse (I_2^2t) operating time characteristic. Where the operating time of the characteristic is dependent solely on the instantaneous magnitude of negative phase sequence current present. This characteristic would be set to match the claimed generator thermal capacity. This is satisfactory when considering the effects of high values of negative phase sequence current.

For intermediate levels of NPS current, the rate of heating is slower. As a result, heat dissipation should be considered.

The basic expression of $t = K/I_2cmr$ does not cater for the effects of heat dissipation or for low standing levels of negative phase sequence current. The latter resulting in an increase in rotor temperature which remains within the machines design limits. An existing, tolerable, level of negative phase sequence current ($I_2<I_{2cmr}$), has the effect of reducing the time to reach the critical temperature level, if the negative phase sequence current level should increase beyond I_{2cmr}. The P34x NPS thermal replica is designed to overcome these problems by modeling the effects of low standing levels of negative phase sequence currents.

When the protected generator sees a reduction in negative phase sequence current, metallic rotor components will decrease in temperature. The relay is provided with a separate thermal capacity setting **(I2>2 KRESET**), used when there is a reduction in I_2.

The negative sequence protection element will respond to system phase to earth and phase to phase faults. Therefore the element must be set to grade with downstream earth and phase fault protections. To aid grading with downstream devices a definite minimum operating time for the operating characteristic can be set. The definite minimum time setting should be set to provide an adequate margin between the operation of the negative phase sequence thermal protection function and external protection. The coordination time margin used should be in accordance with the usual practice adopted by the customer for backup protection coordination.

For levels of negative phase sequence current that are only slightly in excess of the thermal element pick-up setting, there will be a noticeable deviation between the P34x negative phase sequence thermal protection current-time characteristic and that of the simple I_2^2t

characteristic. For this reason, a maximum negative phase sequence protection trip time setting is provided. This maximum time setting also limits the tripping time of the negative phase sequence protection for levels of unbalance where there may be uncertainty about the machine's thermal withstand.

A time delayed negative sequence overcurrent alarm stage is provided to give the operator early warning of an unbalanced condition that may lead to generator tripping. This can allow corrective action to be taken to reduce the unbalance in the load.

2.15.1 Setting guidelines for negative phase sequence thermal protection

The alarm and trip stages of the negative phase sequence thermal protection may be selected as **Enabled** or **Disabled**, within the **I2therm>1 Alarm** and **I2therm>2 Trip** cells respectively.

Synchronous machines will be able to withstand a certain level of negative phase sequence stator current continuously. All synchronous machines will be assigned a continuous maximum negative phase sequence current (I_{2cmr} per-unit) rating by the manufacturer. For various categories of generator, minimum negative phase sequence current withstand levels have been specified by international standards, such as IEC 60034-1 and ANSI C50.13-1977 [1]. The IEC 60034-1 figures are given in Table 5.

Generator type		Maximum I_2/I_n for continuous operation	Maximum $(I_2/I_n)^2t$ for operation under fault conditions, Kg
Salient-pole:			
Indirectly cooled		0.08	20
Directly cooled (inner cooled) stator and/or field		0.05	15
Cylindrical rotor synchronous:			
Indirectly cooled rotor			
Air cooled		0.1	15
Hydrogen cooled		0.1	10
Directly cooled (inner cooled) rotor			
350 > 900 > 1250	350 MVA 900 MVA 1250 MVA 1600 MVA	0.08 * * 0.05	8 ** 5 5
* For these generators, the value of I_2/I_n is calculated as follows:			
$\frac{I_2}{I_n} = 0.8 - \frac{S_n - 350}{3 \times 10^4}$			
** For these generators, the value of $(I_2/I_n)^2t$ is calculated as follows:			
$\left(\frac{I_2}{I_n}\right)^2 t = 8 - 0.00545\ (S_n - 350)$			
where Sn is the rated power in MVA			

Table 5: IEC 60034-1 Minimum negative sequence current withstand levels

To obtain correct thermal protection, the relay thermal current setting, **I2therm>2 Set**, and thermal capacity setting, **I2therm>2 k**, should be set as follows:

$$\text{I2therm>2 Set} = I_{2cmr} \times \left(\frac{I_{flc}}{I_p}\right) x\ In$$

$$\text{I2therm>2 k} = \left(\frac{I_{flc}}{I_p}\right)^2 x\ Kg$$

Where:

I_{2cmr} = Generator per unit I2 maximum withstand

K_g = Generator thermal capacity constant(s), see Table 5 for guidance

I_{flc} = Generator primary full-load current (A)

I_p = CT primary current rating (A)

I_n = Relay rated current (A)

Unless otherwise specified, the thermal capacity constant setting used when I2 is reducing, **I2therm>2 kRESET**, should be set equal to the main time constant setting, **I2therm>2 k Setting**. A machine manufacturer may be able to advise a specific thermal capacity constant when I2 is reducing for the protected generator.

The current threshold of the alarm stage, **I2therm>1 Set** should be set below the thermal trip setting, **I2therm>2 Set**, to ensure that the alarm operates before tripping occurs. A typical alarm current setting would be 70% of the trip current setting. The alarm stage time setting, **I2therm>1 Delay**, must be chosen to prevent operation during system fault clearance and to ensure that unwanted alarms are not generated during normal running. A typical setting for this time delay would be 20 s.

To aid grading with downstream devices a definite minimum operating time for the operating characteristic can be set, **I2therm>2 tMIN**. This definite minimum time setting should be set to provide an adequate margin between the operation of the negative phase sequence thermal protection function and external protection. The coordination time margin used should be in accordance with the usual practice adopted by the customer for back-up protection coordination.

A maximum operating time for the negative phase sequence thermal characteristic may be set, **I2therm>2 tMAX**. This definite time setting can be used to ensure that the thermal rating of the machine is never exceeded.

2.16 Power protection (32P/Q)

2.16.1 Low forward power protection function

When the machine is generating and the CB connecting the generator to the system is tripped, the electrical load on the generator is cut. This could lead to generator over-speed if the mechanical input power is not reduced quickly. Large turbo-alternators, with low-inertia rotor designs, do not have a high over speed tolerance. Trapped steam in the turbine, downstream of a valve that has just closed, can rapidly lead to over speed. To reduce the risk of over speed damage to such sets, it is sometimes chosen to interlock non-urgent tripping of the generator breaker and the excitation system with a low forward power check. This ensures that the generator set circuit breaker is opened only when the output power is sufficiently low that over speeding is unlikely. The delay in electrical tripping, until prime mover input power has been removed, may be deemed acceptable for ‘non-urgent’ protection trips; e.g. stator earth fault protection for a high impedance earthed generator. For ‘urgent’ trips, e.g. stator current differential protection the low forward power interlock should not be used. With the low probability of ‘urgent’ trips, the risk of over speed and possible consequences must be accepted.

The low forward power protection can be arranged to interlock ‘non-urgent’ protection tripping using the relay scheme logic. It can also be arranged to provide a contact for external interlocking of manual tripping, if desired.

To prevent unwanted relay alarms and flags, a low forward power protection element can be disabled when the circuit breaker is opened via ‘poledead’ logic.

The low forward power protection can also be used to provide loss of load protection when a machine is motoring. It can be used for example to protect a machine which is pumping from becoming unprimed or to stop a motor in the event of a failure in the mechanical transmission.

A typical application would be for pump storage generators operating in the motoring mode, where there is a need to prevent the machine becoming unprimed which can cause blade and runner cavitation. During motoring conditions, it is typical for the relay to switch to another setting group with the low forward power enabled and correctly set.

2.16.1.1 Low forward power setting guideline

Each stage of power and sensitive protection can be selected to operate as a low forward power stage by selecting the **Power1/2/3/4 3Ph Watts/Sen Power1/2/3/4 Func** cell to **Under**.

When required for interlocking of non-urgent tripping applications, the threshold setting of the low forward power protection function, **Power1/2/3/4 3Ph Watts/Sen Power1/2/3/4 1Ph Watts/Sen Power1/2/3/4 3Ph Watts** (P345 only), should be less than 50% of the power level that could result in a dangerous over speed transient on loss of electrical loading. The generator set manufacturer should be consulted for a rating for the protected machine. The **Power1/2/3/4 Dirn** or **Sen Power1/2/3/4 Dirn** cell should be set to **Forward** for this application.

When required for loss of load applications, the threshold setting of the low forward power protection function, **Power1/2/3/4 3Ph Watts/Sen Power1/2/3/4 1Ph Watts/Sen Power1/2/3/4 3Ph Watts** (P345 only), is system dependent, however, it is typically set to 10 - 20% below the minimum load. For example, for a minimum load of 70%Pn, the setting needs to be set at 63% - 56%Pn. The **Power1/2/3/4 Dirn** or **Sen Power1/2/3/4 Dirn** cell should be set to **Reverse** for this application.

For interlocking non-urgent trip applications the time delay associated with the low forward power protection function, **Power1/2/3/4 TimeDelay/Sen Power1/2/3/4 Delay**, could be set to zero. However, some delay is desirable so that permission for a non-urgent electrical trip is not given in the event of power fluctuations arising from sudden steam valve/throttle closure. A typical time delay for this reason is 2s.

For loss of load applications the pick up time delay, **Power1/2/3/4 TimeDelay/Sen Power1/2/3/4 Delay**, is application dependent but is normally set in excess of the time between motor starting and the load being established. Where rated power can not be reached during starting (for example where the motor is started with no load connected) and the required protection operating time is less than the time for load to be established then it will be necessary to inhibit the power protection during this period. This can be done in the PSL using AND logic and a pulse timer triggered from the motor starting to block the power protection for the required time.

The delay on reset timer, **Power1/2/3/4 DO Timer**, would normally be set to zero when selected to operate low forward power elements.

To prevent unwanted relay alarms and flags, a low forward power protection element can be disabled when the circuit breaker is open via ‘poledead’ logic. This is controlled by setting the power protection, inhibit cells, **P1/2/3/4 Poledead Inh** to **Enabled**.

2.16.2 Reverse power protection function

A generator is expected to supply power to the connected system in normal operation. If the generator prime mover fails, a generator that is connected in parallel with another source of electrical supply will begin to ‘motor’. This reversal of power flow due to loss of prime mover can be detected by the reverse power element.

The consequences of generator motoring and the level of power drawn from the power system will be dependent on the type of prime mover. Typical levels of motoring power and possible motoring damage that could occur for various types of generating plant are given in Table 6.

Prime mover	Motoring power	Possible damage (percentage rating)
Diesel Engine	5% - 25%	Risk of fire or explosion from unburned fuel
Motoring level depends on compression ratio and cylinder bore stiffness. Rapid disconnection is required to limit power loss and risk of damage.		
Gas Turbine	10% - 15% (Split-shaft) >50% (Single-shaft)	With some gear-driven sets, damage may arise due to reverse torque on gear teeth.
Compressor load on single shaft machines leads to a high motoring power compared to split-shaft machines. Rapid disconnection is required to limit power loss or damage.		
Hydraulic Turbines	0.2 - >2% (Blades out of water) >2.0% (Blades in water)	Blade and runner cavitation may occur with a long period of motoring
Power is low when blades are above tail-race water level. Hydraulic flow detection devices are often the main means of detecting loss of drive. Automatic disconnection is recommended for unattended operation.		
Steam Turbines	0.5% - 3% (Condensing sets) 3% - 6% (Non-condensing sets)	Thermal stress damage may be inflicted on low-pressure turbine blades when steam flow is not available to dissipate windage losses.
Damage may occur rapidly with non-condensing sets or when vacuum is lost with condensing sets. Reverse power protection may be used as a secondary method of detection and might only be used to raise an alarm.		

Table 6: Table showing motor power and possible damage for various types of prime mover

In some applications, the level of reverse power in the case of prime mover failure may fluctuate. This may be the case for a failed diesel engine. To prevent cyclic initiation and reset of the main trip timer, and consequent failure to trip, an adjustable reset time delay is provided (**Power1/2/3/4 DO Timer**). This delay would need to be set longer than the period for which the reverse power could fall below the power setting (**Power1/2/3/4 3Ph Watts/Sen Power1/2/3/4 1Ph Watts/Sen Power1/2/3/4 3Ph Watts** (P345 only)). This setting needs to be taken into account when setting the main trip time delay. It should also be noted that a delay on reset in excess of half the period of any system power swings could result in operation of the reverse power protection during swings.

Reverse power protection may also be used to interlock the opening of the generator set circuit breaker for 'non-urgent' tripping, as discussed in 2.16.1. Reverse power interlocks are preferred over low forward power interlocks by some utilities.

2.16.2.1 Reverse power setting guideline

Each stage of power and sensitive protection can be selected to operate as a reverse power stage by selecting the **Power1/2/3/4 Function** or **Sen Power1/2/3/4 Func** cell to **Over** and the **Power1/2/3/4 Dirn** or **Sen Power1/2/3/4 Dirn** cell to **Reverse**.

The power threshold setting of the reverse power protection **Power1/2/3/4 3Ph Watts/Sen Power1/2/3/4 1Ph Watts/Sen Power1/2/3/4 3Ph Watts** (P345 only), should be less than 50% of the motoring power, typical values for the level of reverse power for generators are given in previous table.

The reverse power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronization.

A time delay setting, **Power1/2/3/4 TimeDelay/Sen Power1/2/3/4 Delay**, of 5 s should be applied typically.

The delay on reset timer, **Power1/2/3/4 DO Timer**, would normally be set to zero. When settings of greater than zero are used for the reset time delay, the pick up time delay setting may need to be increased to ensure that false tripping does not result in the event of a stable power swinging event.

2.16.3 Overpower protection

The overpower protection can be used as overload indication, as a back-up protection for failure of governor and control equipment, and would be set above the maximum power rating of the machine.

2.16.3.1 Overpower setting guideline

Each stage of power and sensitive protection can be selected to operate as an over power stage by selecting the **Power1/2/3/4 Function** or **Sen Power1/2/3/4 Func** cell to **Over** and the **Power1/2/3/4 Dirn** or **Sen Power1/2/3/4 Dirn** cell to **Forward** or **Reverse** depending on the operating mode of the machine.

The power threshold setting of the over power protection, **Power1/2/3/4 3Ph Watts/Sen Power1/2/3/4 1Ph Watts**/**Sen Power1/2/3/4 3Ph Watts** (P345 only), should be set greater than the machine full load rated power.

A time delay setting, **Power1/2/3/4 TimeDelay**/**Sen Power1/2/3/4 Delay** should be applied.

The delay on reset timer, **Power1/2/3/4 DO Timer**, would normally be set to zero.

2.16.4 Reactive power protection

Some applications provide underexcitation protection using negative reactive power elements. This is popular for synchronous motors and small generators.

2.16.4.1 Reactive power setting guideline

Each stage of power and sensitive protection can be selected to operate as a reverse reactive power stage by selecting the **Power1/2/3/4 Function** or **Sen Power1/2/3/4 Func** cell to **Over** and the **Power1/2/3/4 Dirn** or **Sen Power1/2/3/4 Dirn** cell to **Reverse**.

The power threshold setting of the negative reactance power protection, **Power1/2/3/4 3Ph VARs/Sen Power1/2/3/4 1Ph VArs**/**Sen Power1/2/3/4 3Ph VArs** (P345 only), should be set to supervise the steady state and dynamic stability limits for under excitation protection, Figure 38 shows an example of the typical settings, Q1 and Q2.

The disadvantage of this method is that the measurement is not very sensitive during low voltage operation of the generator. The reactive power elements can be blocked in the PSL from an undervoltage start signal if this is a problem. This method is less secure secure than the impedance method and therefore is often used just to alarm.

If the static limit characteristic Q1 is exceeded, the voltage regulator must first have the opportunity of increasing the excitation. For this reason, a time delayed trip of typically 5-10s is used **(Power1/2/3/4 TimeDelay**/**Sen Power1/2/3/4 Delay)**. A shorter delay e.g. 0.5s can be used for Q2.

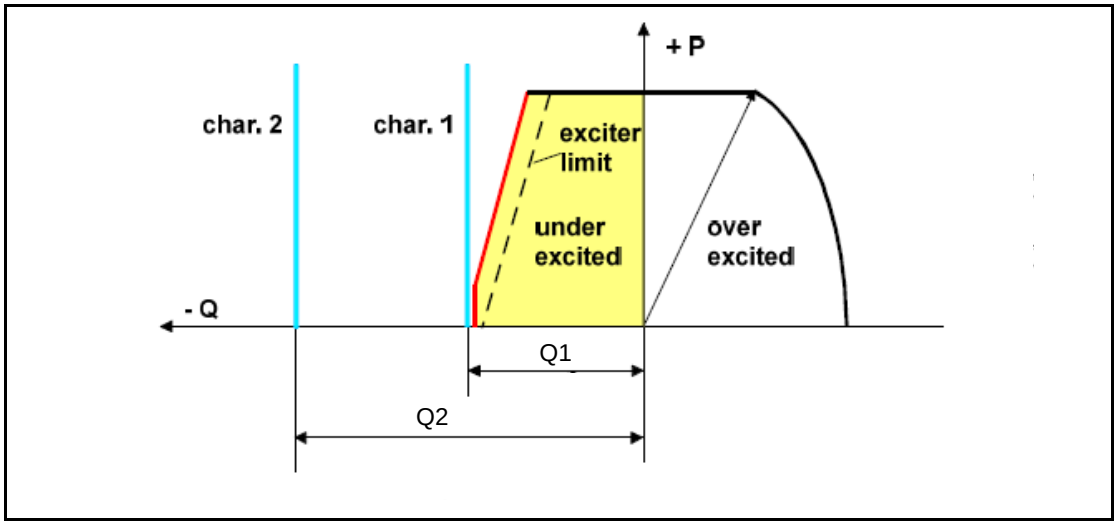


Figure 38: Reactive power protection for underexcitation protection

Q1 = VN^2/Xd

Q2 > = $2\ VN^2/Xd$

Where:

VN = Machine nominal voltage

Xd = Generator direct-axis synchronous reactance in ohms

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2.17 Stator earth fault protection function (50N/51N)

Low voltage generators will be solidly earthed, however to limit the damage that can be caused due to earth faults, it is common for HV generators to be connected to earth via an impedance. This impedance may be fitted on the secondary side of a distribution transformer earthing arrangement. The earthing impedance is generally chosen to limit earth fault current to full load current or less.

There is a limit on the percentage of winding that can be protected by a stator earth fault element. For earth faults close to the generator neutral, the driving voltage will be low, and hence the value of fault current will be severely reduced. In practice, approximately 95% of the stator winding can be protected. For faults in the last 5% of the winding, the earth fault current is so low that it cannot be detected by this type of earth fault protection. In most applications this limitation is accepted as the chances of an earth fault occurring in the last 5% of the winding, where the voltage to earth is low, is small.

The percentage of winding covered by the earth fault protection can be calculated as shown below, with reference to Figure 39.

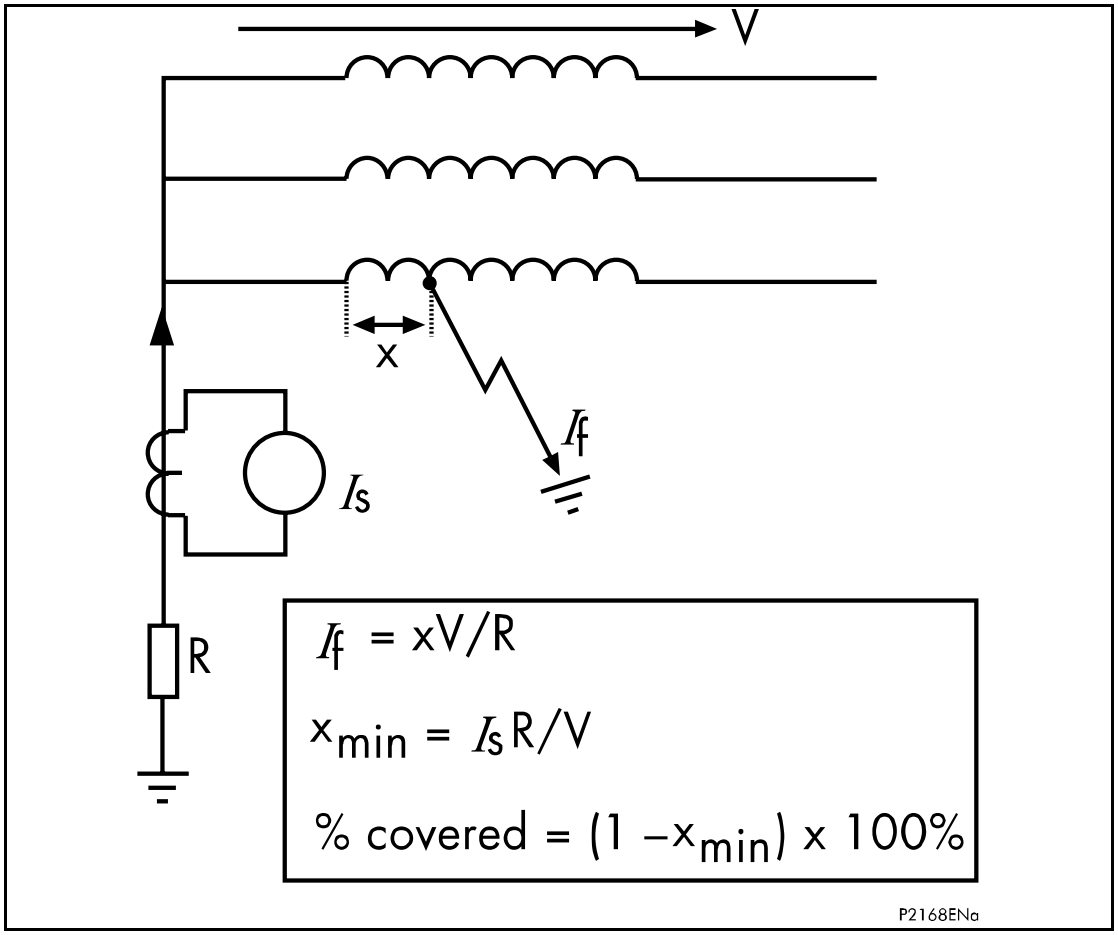


Figure 39: Effective coverage of stator earth fault protection

A two stage non-directional earth fault element is provided. The first stage has an inverse time or definite time delay or a user curve characteristic and can incorporate a reset time delay or user reset curve characteristic to improve detection of intermittent faults. The second stage has a definite time characteristic that can be set to 0 s to provide instantaneous operation.

Where impedance or distribution transformer earthing is used the second stage of protection may be used to detect flashover of the earthing impedance. The second stage may also be used to provide instantaneous protection where grading with system protection is not required. See setting guidelines for more details.

Each stage of protection can be blocked by energizing the relevant DDB signal via the PSL (DDB 544, DDB 545). This allows the earth fault protection to be integrated into busbar protection schemes as shown in section 2.33, or can be used to improve grading with downstream devices.

The Stator Earth Fault element is powered from the In CT input on the relay. This input should be supplied from a CT fitted into the generator earth path so that the element provides earth fault protection for the generator and back-up protection for system faults. Alternatively, the element may be supplied from a CT fitted on the secondary side of a distribution transformer earthing system.

2.17.1 Setting guidelines for stator earth fault protection

The first stage of earth fault protection can be selected by setting **IN>1 Function** to any of the inverse or user curve or DT settings. The first stage is disabled if **IN>1 Function** is set to **Disabled**. The second stage of earth fault protection can be selected by setting **IN>2 Function** to **Enabled**. The second stage is disabled if **IN>2 Function** is set to **Disabled**.

Programmable operate curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves. Programmable reset curves can be used to match more

closely the reset characteristic of electromechanical relays. If a user curve **Default 1/2/3/4** is selected for the earth fault operate or reset characteristic then in the **User Curves** menu the **UserCurve1/2/3/4 Type** setting should be chosen to match the template of the curve downloaded from the S1 Agile User Programmable Curve tool. For an earth fault application the **UserCurve1/2/3/4 Type – Operate 1.0 or Reset 1.1** would normally be selected for the operate or reset characteristic respectively.

For a directly connected machine the stator earth fault protection must co-ordinate with any downstream earth fault protections. The first stage current setting, **IN>1 Current**, should typically be set to less than 33% of the machine earth fault contribution or full load current, whichever is lower. The time delay characteristic of the element (selected via **IN>1 Function** and **IN>1 Time Delay**, **IN>1 TMS** or **IN>1 Time Dial**) should be set to time grade with any downstream earth fault protection. Where the element is required to protect 95% of the generator winding a current setting of 5% of the limited earth fault current should be used.

Where impedance or distribution transformer earthing is used the second stage may be used to detect flashover of the earthing impedance. In such a case the second stage current setting, **IN>2 Current**, could be set to approximately 150% of the limited earth fault current and the time delay, **IN>2 Time Delay**, would be set to 0 s, to provide instantaneous operation.

For a machine connected to the system via a step-up transformer there is no need to grade the stator earth fault element with system earth fault protections. In this case the first stage should be set to 5% of the limited earth fault current to provide protection for 95% of the machine winding. The time delay characteristic of the stage should grade with VT fuses for VT earth faults. A transient generator earth fault current may also occur for a HV earth fault due to transformer inter-winding capacitance. Correct grading under these conditions can be provided by using a definite time delay of between 0.5 - 3 s. Experience has shown that it is possible to apply an instantaneous stator earth fault element on a indirectly connected machine if a current setting of ≥10% of the limited earth fault current is used. Therefore the second stage can be set to give this instantaneous protection.

2.18 Residual overvoltage/neutral voltage displacement protection function (59N)

On a healthy three-phase power system, the addition of each of the three-phase to earth voltages is nominally zero, as it is the vector addition of three balanced vectors at 120° to one another. However, when an earth fault occurs on the primary system this balance is upset and a 'residual' voltage is produced.

This could be measured, for example, at the secondary terminals of a voltage transformer having a "broken delta" secondary connection. Hence, a residual voltage measuring relay can be used to offer earth fault protection on such a system. Note that this condition causes a rise in the neutral voltage with respect to earth that is commonly referred to as "neutral voltage displacement" or NVD.

Alternatively, if the system is impedance or distribution transformer earthed, the neutral displacement voltage can be measured directly in the earth path via a single-phase VT. This type of protection can be used to provide earth fault protection irrespective of whether the generator is earthed or not, and irrespective of the form of earthing and earth fault current level. For faults close to the generator neutral the resulting residual voltage will be small. Therefore, as with stator earth fault protection, only 95% of the stator winding can be reliably protected.

Note: Where residual overvoltage protection is applied to a directly connected generator, such a voltage will be generated for an earth fault occurring anywhere on that section of the system and so the NVD protection must coordinate with other earth fault protections.

The neutral voltage displacement protection function of the P342/3/6 relays consist of two stages of derived and two stages of measured neutral overvoltage protection with adjustable time delays. The P344/5 has an additional two stages of measured neutral overvoltage protection as it has a dedicated second neutral voltage input.

Two stages are included for the derived and measured elements to account for applications that require both alarm and trip stages, for example, an insulated system. It is common in such a case for the system to have been designed to withstand the associated healthy phase overvoltages for a number of hours following an earth fault. In such applications, an alarm is generated soon after the condition is detected, which serves to indicate the presence of an earth fault on the system. This gives time for system operators to locate and isolate the fault. The second stage of the protection can issue a trip signal if the fault condition persists.

2.18.1 Setting guidelines for residual overvoltage/neutral voltage displacement protection

All stages may be selected as either IDMT (inverse time operating characteristic), DT (definite time operating characteristic) or **Default Curve 1/2/3/4** (user programmable curve) within the **VN>x Function** cell. All stages are Enabled/Disabled in the **VN>x Status** cell. The time delay. (VN>x TMS - for IDMT curve; **V>x Time Delay** - for definite time) should be selected in accordance with normal relay co-ordination procedures to ensure correct discrimination for system faults.

Programmable operate curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves. If a user curve **Default 1/2/3/4** is selected for the neutral voltage operate characteristic then in the **User Curves** menu the **UserCurve1/2/3/4 Type** setting should be chosen to match the template of the curve downloaded from the S1 Agile User Programmable Curve tool. For a neutral voltage application the **UserCurve1/2/3/4 Type – Operate 1.0** would normally be selected for the operate characteristic.

The VN>1/2 protection stages use the residual/neutral voltage derived from the phase-neutral voltage inputs (P342-8). The VN>3/4 protection stages use the residual/neutral voltage measured by the VN input (P342/3/4) or VN1 input (P344/5). The VN>4/5 protection stages use the residual/neutral voltage measured by the VN2 input (P344/5).

For a directly connected machine the neutral voltage displacement protection must coordinate with any downstream earth fault protections. To ensure coordination the voltage setting of the neutral voltage displacement protection function should be set higher than the effective setting of current operated earth fault protection in the same earth fault zone. The effective voltage setting of a current operated earth fault protection may be established from the following equations:

Veff = (Ipoc x Ze) / (1/3 x V1/V2) for an open delta VT

Veff = (Ipoc x Ze) / (V1/V2) for a single-phase star point VT

Where:

Veff = Effective voltage setting of current operated protection

Ipoc = Primary operating current of current operated protection

Ze = Earthing impedance

V1/V2 = VT turns ratio

It must also be ensured that the voltage setting of the element is set above any standing level of residual voltage that is present on the system. A typical setting for residual overvoltage protection is 5 V.

The second stage of protection can be used as an alarm stage on unearthed or very high impedance earthed systems where the system can be operated for an appreciable time under an earth fault condition.

Where the generator is connected to the system via a transformer, co-ordination with system earth fault protections is not required. In these applications the NVD voltage setting should typically be set to 5% of rated voltage. This will provide protection for 95% of the stator winding.

2.19 Sensitive earth fault protection function (50N/51N/67N/67W)

If a generator is earthed through a high impedance, or is subject to high ground fault resistance, the earth fault level will be severely limited. Consequently, the applied earth fault protection requires both an appropriate characteristic and a suitably sensitive setting range in order to be effective. A separate sensitive earth fault element is provided within the P34x relay for this purpose, this has a dedicated CT input allowing very low current setting thresholds to be used.

An alternative use for the sensitive earth fault input is on a multiple earthed system where it is advantageous to apply a directional earth fault relay at the machine terminals. The directional relay, operating for current flowing into the machine, will be stable for external faults but can operate quickly for generator faults when fault current is fed from the system.

Where several machines are connected in parallel, it is common for only one machine to be earthed at any time. This prevents the flow of third harmonic currents that could overheat the machine. This may be the only earth connection for this part of the system. Non-directional earth fault protection could be applied at the terminals of the unearthed machines in such cases since an unearthed generator cannot source earth fault current. However, as any of the machines can be earthed, it is prudent to apply directional protection at the terminals of all the machines. There is also a risk that transient spill current can cause operation of a non-directional, terminal fed, earth fault relay for an external phase fault, hence directional elements have an added degree of security. When applied in this way the directional earth fault elements will operate for faults on the unearthed machines but not the earthed machine. Therefore additional stator earth fault or residual overvoltage/NVD protection should be used to protect the earthed machine. Such a scheme will provide stable, fast, earth fault protection for all machines, no matter which generator is earthed.

A single stage definite time sensitive earth fault protection element is provided in the P34x relay, this element can be set to operate with a directional characteristic when required. Where Petersen Coil earthing is used, users may wish to use Wattmetric Directional Earth Fault protection or an Icosϕ characteristic. Settings to enable the element to operate as a wattmetric element are also provided. For insulated earth applications, it is common to use the Isinϕ characteristic. See the P140 technical guide P14x/EN T for more details on the application of directional earth fault protection on insulated and Petersen coil systems.

2.19.1 Setting guidelines for sensitive earth fault protection

The operating function of the sensitive earth fault protection can be selected by setting **SEF/REF Options** cell. The SEF protection is selected by setting **ISEF>1 Function** to **Enabled**. To provide sensitive earth fault or sensitive directional earth fault protection the **SEF/REF Options** cell should be set to **SEF**. For SEF cosϕ and SEF sinϕ earth fault protection **SEF/REF Options** cell should be set to **SEF Cos (PHI)** or **SEF Sin (PHI)**. The SEF cosϕ and SEF sinϕ options are not available with low impedance REF protection. For wattmetric earth fault protection **SEF/REF Options** cell should be set to **Wattmetric**. The other options for **SEF/REF Options** relate to restricted earth fault protection, for more details see section 2.20.

The directionality of the element is selected in the **ISEF> Direction** setting. If **ISEF> Direction** is set to **Directional Fwd** the element will operate with a directional characteristic and will operate when current flows in the forward direction, i.e. when current flows into the machine with the relay connected as shown in the standard relay connection diagram. If **ISEF> Direction** is set to **Directional Rev** the element will operate with a directional characteristic and will operate when current flows in the opposite direction, i.e. current flow out of the machine into the system. If **ISEF> Direction** is set to **Non-Directional** the element will operate as a simple overcurrent element. If either of the directional options are chosen additional cells to select the characteristic angle of the directional characteristic and polarizing voltage threshold will become visible.

The operating current threshold of the Sensitive Earth Fault protection function, **ISEF>1 Current**, should be set to give a primary operating current down to 5% or less of the minimum earth fault current contribution to a generator terminal fault.

The directional element characteristic angle setting, **ISEF> Char Angle**, should be set to match as closely as possible the angle of zero sequence source impedance behind the relaying point. If this impedance is dominated by an earthing resistor, for example, the angle setting would be set to 0°. On insulated or very high impedance earthed systems the earth fault current measured by an SDEF element is predominantly capacitive hence the RCA should be set to –90°.

The polarizing voltage threshold setting, **ISEF> VNpol Set**, should be chosen to give a sensitivity equivalent to that of the operating current threshold. This current level can be translated into a residual voltage as described for the residual overvoltage protection in section 2.18.

When the element is set as a non-directional element the definite time delay setting **ISEF>1 Delay** should be set to coordinate with downstream devices that may operate for external earth faults. For an indirectly connected generator the SEF element should coordinate with the measurement VT fuses, to prevent operation for VT faults. For directional applications when the element is fed from the residual connection of the phase CTs a short time delay is desirable to ensure stability for external earth faults or phase/phase faults.

A time delay of 0.5 s will be sufficient to provide stability in the majority of applications. Where a dedicated core balance CT is used for directional applications an instantaneous setting may be used.

2.20 Restricted earth fault protection (64)

Earth faults occurring on a machine winding or terminal may be of limited magnitude, either due to the impedance present in the earth path or by the percentage of stator winding that is involved in the fault. As stated in section 2.16.1, it is common to apply stator earth fault protection fed from a single CT in the machine earth connection - this can provide time delayed protection for a stator winding or terminal fault. On larger machines, typically >2 MW, where phase CTs can be fitted to both neutral end and terminal ends of the stator winding, phase differential protection may be fitted. For small machines, however, only one set of phase CTs may be available making phase differential protection impractical. For smaller generators earth fault differential protection can be applied to provide instantaneous tripping for any stator or terminal earth fault. In application the operating zone of earth fault differential protection is restricted to faults within the boundaries of the CTs supplying the relay, hence this type of element is referred to as restricted earth fault protection.

When applying differential protection such as REF, some suitable means must be employed to give the protection stability under external fault conditions, therefore ensuring that relay operation only occurs for faults on the transformer winding/connections. Two methods are commonly used; percentage bias or high impedance. The biasing technique operates by measuring the level of through current flowing and altering the relay sensitivity accordingly. The high impedance technique ensures that the relay circuit is of sufficiently high impedance such that the differential voltage that may occur under external fault conditions is less than that required to drive setting current through the relay.

The REF protection in the P34x relays may be configured to operate as either a high impedance differential or a low impedance biased differential element.

In the P343/4/5/6 the 3 phase current source for the low impedance REF can be selected using the **IREF> CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting. In the standard connection diagrams in the installation chapter, *P34x/EN IN*, **IA-1/IB-1/IC-1** is connected to the neutral side CTs and **IA-2/IB-2/IC-2** is connected to the terminal side CTs. By selecting the terminal side CTs for the 3 phase currents the low impedance REF protection can be used to provide REF protection of the transformer LV star winding for generator-transformer applications or for REF protection of the generator.

Note: CT requirements for REF protection are included in section 4.

2.20.1.1 Setting guidelines for low impedance biased REF protection

To select low impedance biased REF protection **SEF/REF Option** should be selected to **Lo Z REF**. If REF protection is required to operate alongside sensitive earth fault protection, **SEF/REF Option** should be selected to **Lo Z REF + SEF or Lo Z REF + Wattmet** (if Wattmetric earth fault protection is required).

Two bias settings are provided in the REF characteristic of the P34x. The **IREF> k1** level of bias is applied up to through currents of **IREF> Is2**, which is normally set to the rated current of the machine. **IREF> k1** should normally be set to 0% to give optimum sensitivity for internal faults. However, if any differential spill current is present under normal conditions due to CT mismatch, then **IREF> k1** may be increased accordingly, to compensate.

IREF> k2 bias is applied for through currents above **IREF> Is2** and may typically be set to 150% to ensure adequate restraint for external faults.

The neutral current scaling factor which automatically compensates for differences between neutral and phase CT ratios relies on the relay having been programmed with the correct CT ratios. Ensure these CT ratios are entered into the relay, in the **CT RATIOS** menu, for the scheme to operate correctly.

The differential current setting **IREF> Is1** should typically be set to 5% of the limited earth fault current level.

In the P343/4/5/6 select the terminal side CTs with the **IREF> CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting to provide REF protection of the transformer LV star winding for generator-transformer applications or for REF protection of the generator. In the standard connection diagrams in the installation chapter, *P34x/EN IN*, **IA-1/IB-1/IC-1** is connected to the neutral side CTs and **IA-2/IB-2/IC-2** is connected to the terminal side CTs.

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2.20.1.2 Setting guidelines for high impedance REF protection

From the **Sens E/F Option** cell, **Hi Z REF** must be selected to enable High Impedance REF protection. The only setting cell then visible is **IREF> Is**, which may be programmed with the required differential current setting. This would typically be set to give a primary operating current of either 30% of the minimum earth fault level for a resistance earthed system or between 10 and 60% of rated current for a solidly earthed system.

The primary operating current (Iop) will be a function of the current transformer ratio, the relay operating current **(IREF> Is**) the number of current transformers in parallel with a relay element (n) and the magnetizing current of each current transformer (Ie) at the stability voltage (Vs). This relationship can be expressed in three ways:

1. To determine the maximum current transformer magnetizing current to achieve a specific primary operating current with a particular relay operating current.

$$I_e < \frac{1}{n} \times \left(\frac{I_{op}}{\text{CT ratio}} \text{ - Gen diff REF > Is1} \right)$$

2. To determine the maximum relay current setting to achieve a specific primary operating current with a given current transformer magnetizing current.

$$\text{IREF Is1} < \left(\frac{I_{op}}{\text{CT ratio}} - nI_e \right)$$

3. To express the protection primary operating current for a particular relay operating current and with a particular level of magnetizing current.

$$I_{op} = (\text{CT ratio}) \times (\text{IREF} > \text{Is1} + nI_e)$$

To achieve the required primary operating current with the current transformers that are used, a current setting **IREF> Is** must be selected for the high impedance element, as detailed in expression (ii) above. The setting of the stabilizing resistor (RST) must be calculated in the following manner, where the setting is a function of the required stability voltage setting (VS) and the relay current setting **IREF> Is**.

$$R_{ST} = \frac{Vs}{IREF > Is1} = \frac{I_F (R_{CT} + 2_{RL})}{IREF > Is1}$$

Note: The above equation assumes negligible relay impedance.

The stabilizing resistor supplied is continuously adjustable up to its maximum declared resistance.

USE OF “METROSIL” NON-LINEAR RESISTORS

Metrosils are used to limit the peak voltage developed by the current transformers under internal fault conditions, to a value below the insulation level of the current transformers, relay and interconnecting leads, which are normally able to withstand 3000 V peak.

The following formulae should be used to estimate the peak transient voltage that could be produced for an internal fault. The peak voltage produced during an internal fault will be a function of the current transformer kneepoint voltage and the prospective voltage that would be produced for an internal fault if current transformer saturation did not occur. This prospective voltage will be a function of maximum internal fault secondary current, the current transformer ratio, the current transformer secondary winding resistance, the current transformer lead resistance to the common point, the relay lead resistance and the stabilizing resistor value.

$$Vp = 2\sqrt{2\,V_k\,(V_f - V_k)}$$

$$V_f = I'f\,(RCT + 2RL + RST)$$

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Where:

V_p = Peak voltage developed by the CT under internal fault conditions

V_k = Current transformer knee-point voltage

V_f = Maximum voltage that would be produced if CT saturation did not occur

I'_f = Maximum internal secondary fault current

R_{CT} = Current transformer secondary winding resistance

R_L = Maximum lead burden from current transformer to relay

R_{ST} = Relay stabilizing resistor

When the value given by the formulae is greater than 3000 V peak, Metrosils should be applied. They are connected across the relay circuit and serve the purpose of shunting the secondary current output of the current transformer from the relay in order to prevent very high secondary voltages.

Metrosils are externally mounted and take the form of annular discs. Their operating characteristics follow the expression:

$$V = CI^{0.25}$$

Where:

V = Instantaneous voltage applied to the non-linear resistor (“Metrosil”)

C = Constant of the non-linear resistor (“Metrosil”)

I = Instantaneous current through the non-linear resistor (“Metrosil”)

With a sinusoidal voltage applied across the Metrosil, the RMS current would be approximately 0.52x the peak current. This current value can be calculated as follows:

$$I(rms) = 0.52\left(\frac{Vs\,(rms) \times \sqrt{2}}{C}\right)^4$$

Where:

Vs(rms) = rms value of the sinusoidal voltage applied across the Metrosil

This is due to the fact that the current waveform through the non-linear resistor (“Metrosil”) is not sinusoidal but appreciably distorted.

For satisfactory application of a non-linear resistor (“Metrosil”), its characteristic should be such that it complies with the following requirements:

4. At the relay voltage setting, the non-linear resistor (“Metrosil”) current should be as low as possible, but no greater than approximately 30 mA rms for 1A current transformers and approximately 100 mA rms for 5A current transformers.

5. At the maximum secondary current, the non-linear resistor (“Metrosil”) should limit the voltage to 1500 V rms or 2120 V peak for 0.25 second. At higher relay voltage settings, it is not always possible to limit the fault voltage to 500 V rms, so higher fault voltages may have to be tolerated.

The following tables show the typical Metrosil types that will be required, depending on relay current rating, REF voltage setting etc.

Metrosil Units for Relays with a 1 Amp CT

The Metrosil units with 1 Amp CTs have been designed to comply with the following restrictions:

6. At the relay voltage setting, the Metrosil current should less than 30 mA rms

7. At the maximum secondary internal fault current the Metrosil unit should limit the voltage to 1500 V rms if possible.

The Metrosil units normally recommended for use with 1Amp CTs are shown in Table 7.

Relay voltage setting	Nominal characteristic		Recommended Metrosil type	
	C	β	Single pole relay	Triple pole relay
Up to 125 V rms	450	0.25	600A/S1/S256	600A/S3/1/S802
125 to 300 V rms	900	0.25	600A/S1/S1088	600A/S3/1/S1195

Table 7: Recommended Metrosil types for 1 A CTs

Note: Single pole Metrosil units are normally supplied without mounting brackets unless otherwise specified by the customer

Metrosil Units for Relays with a 5 Amp CT

These Metrosil units have been designed to comply with the following requirements:

8. At the relay voltage setting, the Metrosil current should less than 100 mA rms (the actual maximum currents passed by the units shown below their type description).

9. At the maximum secondary internal fault current the Metrosil unit should limit the voltage to 1500 V rms for 0.25secs. At the higher relay settings, it is not possible to limit the fault voltage to 1500 V rms hence higher fault voltages have to be tolerated (indicated by *, **, ***).

The Metrosil units normally recommended for use with 5 Amp CTs and single pole relays are shown in Table 8.

Secondary internal fault current	Recommended METROSIL type			
	Relay voltage setting			
Amps rms	Up to 200 V rms	250 V rms	275 V rms	300 V rms
50A	600A/S1/S1213 C = 540/640 35 mA rms	600A/S1/S1214 C = 670/800 40 mA rms	600A/S1/S1214 C =670/800 50 mA rms	600A/S1/S1223 C = 740/870* 50 mA rms
100A	600A/S2/P/S1217 C = 470/540 70 mA rms	600A/S2/P/S1215 C = 570/670 75 mA rms	600A/S2/P/S1215 C = 570/670 100 mA rms	600A/S2/P/S1196 C =620/740* 100 mA rms
150A	600A/S3/P/S1219 C = 430/500 100 mA rms	600A/S3/P/S1220 C = 520/620 100 mA rms	600A/S3/P/S1221 C = 570/670** 100 mA rms	600A/S3/P/S1222 C =620/740*** 100 mA rms

Table 8: Recommended Metrosil types for 5 A CTs

Note: *2400 V peak **2200 V peak ***2600 V peak

In some situations single disc assemblies may be acceptable, contact General Electric for detailed applications.

10. The Metrosil units recommended for use with 5 Amp CTs can also be applied for use with triple pole relays and consist of three single pole units mounted on the same central stud but electrically insulated for each other. To order these units please specify "Triple Pole Metrosil Type", followed by the single-pole type reference.

11. Metrosil units for higher relay voltage settings and fault currents can be supplied if required.

For further advice and guidance on selecting METROSILS please contact the Applications department at General Electric.

2.21 100% stator earth fault protection (3rd harmonic method) (27TN/59TN)

As stated in sections 2.16.1 and 2.18, standard residual current or residual overvoltage protection elements can provide earth fault protection for 95% of the generator stator winding.

Earth faults in the final 5% of the winding will result in such a low fault current or such a small imbalance in voltage that conventional protection cannot be relied on to detect the fault. In most applications this limitation is accepted due to the low probability of a fault occurring in the 5% of the stator winding closest to the star point, where the voltage to earth is lowest. However, for large generators 100% stator earth fault protection is commonly specified to cover all winding earth faults. Faults close to the star point can occur as a consequence of mechanical damage such as creepage of the conductors and loosening of bolts.

Most generators will produce third harmonic voltage to some degree due to non-linearities in the magnetic circuits of the generator design. Under normal operating conditions the distribution of the third harmonic voltage along the stator windings corresponds to Figure Figure 40a. The maxima occur at the star point N and the terminal T. The values increase with generator load. For a stator earth fault at the star point, Figure 40b, the amplitude of the third harmonic in the voltage at the terminals is approximately doubled both when the generator is off load prior the fault (U'TE) and when it is fully loaded (U"TE). The same third harmonic values can be measured in the star point voltages U'NE and U"NE for an earth fault at the generator terminals, Figure 40c.

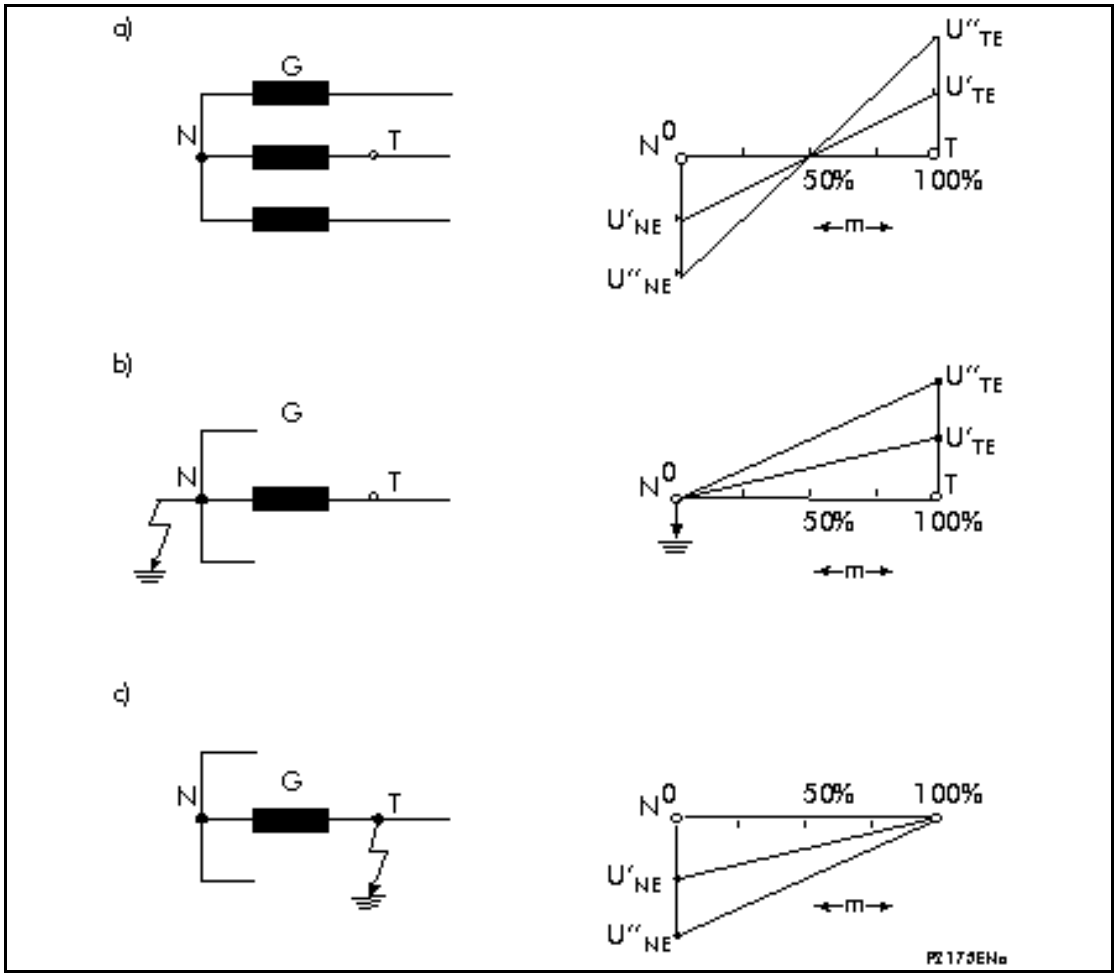


Figure 40: Distribution of the 3rd harmonic component along the stator winding of a large generator, (a) normal operation, (b) stator earth fault at the star point (c), stator earth fault at the terminals

m = relative number of turns

To detect faults in the last 5% of the generator winding, the P343/4/5/6 relay is provided with a third harmonic undervoltage and overvoltage element. These, together with the residual overvoltage or stator earth fault protection elements, will provide protection for faults over the complete winding.

The third harmonic neutral under voltage element is applicable when the neutral voltage measurement is available at the neutral end of the generator.

It is supervised by a three-phase under voltage element, which inhibits the protection when all the phase-phase voltages at the generator terminal are below the threshold, to prevent operation when the machine is dead, interlocking may also be required to prevent false operation during certain conditions. For example, some machines do not produce substantial third harmonic voltage until they are loaded. In this case, the power supervision elements (active, reactive and apparent power) could be used to detect load to prevent false tripping under no load conditions. These power thresholds can be individually enabled and disabled and the setting range is from 2 - 100%Pn.

For applications where the neutral voltage measurement can only be obtained at the generator terminals, from a broken delta VT for example, the undervoltage technique cannot be applied. Therefore the third harmonic neutral overvoltage element can be used for this application. The blocking features of the undervoltage and power elements are not required for the 3rd harmonic neutral over voltage element.

Note: The relay can only select 3rd harmonic neutral undervoltage or 3rd harmonic neutral over voltage, but not both.

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A normal level of third harmonic voltage of 1% is sufficient to ensure that third harmonic undervoltage or overvoltage and residual overvoltage protection functions will overlap hence providing 100% coverage for earth faults on the stator winding. In general, third harmonic undervoltage protection alone can provide coverage for faults on 30% of the generator winding.

The 3rd harmonic undervoltage element operates from the same input as the neutral voltage displacement protection (VN1 input for P343/4/5/6) and must be supplied from a VT connected in the generator earth connection as shown in Figure 41. The 3rd harmonic overvoltage element operates from the neutral voltage measurement at the generator terminals, via an open-delta VT, for example as shown in Figure 41. For applications where parallel machines are directly connected to the busbars discrimination of an earth fault between the machines usually can not be achieved. For applications where machines are connected to the busbars via a delta/star transformer the delta winding blocks the 3rd harmonic currents from other machines so correct discrimination can be achieved for earth faults.

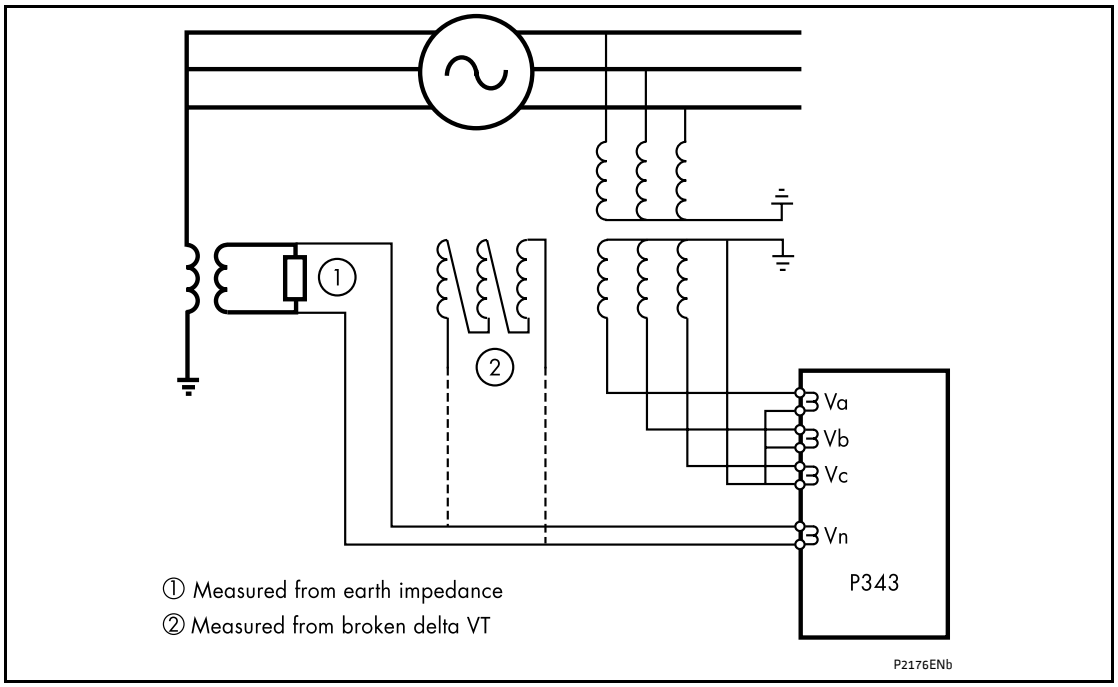


Figure 41: Connection for 3rd harmonic undervoltage and overvoltage for 100% stator earth fault protection

2.21.1 Setting guidelines for 100% stator earth fault protection

The 100% stator earth fault protection element can be selected by setting the **100% St. EF Status** cell to **Enabled**.

The third harmonic undervoltage threshold, **100% St. EF VN3H<**, must be set below the level of third harmonic voltage present under normal conditions. This voltage can be determined by viewing the **VN 3rd Harmonic** cell in the **MEASUREMENTS 3** menu. A typical value for this threshold could be 0.5 V.

The third harmonic overvoltage threshold, **100% St. EF VN3H>**, must be set above the level of third harmonic voltage present under normal conditions. This voltage can be determined by viewing the **VN 3rd Harmonic** cell in the **MEASUREMENTS 3** menu. A typical value for this threshold could be 1 V.

A time delay for these elements can be set in the **VN3H< Delay** and **VN3H> Delay** cells.

The terminal voltage interlock threshold, used to prevent operation of the element when the machine is not running, **100% St. EF V<Inh**, should typically be set to 80% of machine rated voltage.

The power interlock thresholds, used to prevent operation of the element until there is sufficient load current, **P<Inhibit set, Q<Inhibit set, S<Inhibit**, should be enabled if required to prevent operation under no load conditions. One or more of the thresholds can be used as an interlock. They should be set during commissioning by increasing the load current until the 3rd harmonic undervoltage element is reset and setting the power thresholds above the measured power values. The power values can be determined by viewing the **three-phase Watts**, **three-phase Vars**, **three-phase VA** cells in the **MEASUREMENTS 2** menu.

Note: Other earth fault protection (residual overvoltage or current operated stator earth fault protection) must also be enabled to provide coverage for earth faults across the complete stator winding.

2.22 100% stator earth fault protection (low frequency injection method) (64S)

The 100% stator earth fault protection using a low frequency injection technique detects earth faults in the entire winding, including the generator neutral point. If an earth fault in the generator starpoint or close to the starpoint is not detected the generator is effectively running with a low impedance earth bypassing the high impedance earth typically used on large machines. A second earth fault can then cause a very high current to flow which can cause a lot of damage to the machine. This is why 100% stator earth fault protection is a common requirement for large machines.

The low frequency injection technique can be used to provide protection for 100% of the stator winding compared to only 20-30% of the winding using the 3rd harmonic technique. Also, the low frequency injection technique provides protection when the machine is stopped and running and also when the machine is running up and down. The 3rd harmonic technique has to be blocked or is not operational when the machine is stopped and when the machine is running up and down. Also, some machines only produce a low level of 3rd harmonic voltage (<1% Vn) and for these machines the 3rd harmonic method of 100% stator earth fault protection can not be used. So in these applications only the low frequency injection method can provide 100% stator earth fault protection.

100% stator earth fault protection can be provided by injecting an external low frequency alternating voltage into the starpoint or the terminals of the machine. Under normal healthy conditions only a very small current flows via the stator earth capacitance due to the high impedance of this path at low frequencies ($Xc = 1/2\pi fc$). In the event of an earth fault the measured current increases due to the smaller impedance of the earth fault path. From the injected voltage and the fault current the relay can determine the fault resistance. The protection can also detect earth faults at the generator terminals including connected components such as voltage transformers.

A loading device with a low frequency generator is required for implementation. The output of the low frequency signal generator (approx 25 V) is connected via a bandpass filter in parallel with a loading resistor to a neutral transformer at the generator starpoint or an earthing (broken delta) transformer at the terminals of the generator.

The loading resistor is connected in parallel with the low frequency generator to generate a defined neutral current in normal healthy conditions.

The voltage to be injected into the generator starpoint depends on the driving 20 Hz voltage (voltage divider, load resistor and bandpass), and on the transformation ratio of the neutral or earthing transformer. To prevent the secondary load resistance from becoming too small (it should be > 0.5 Ω where possible to minimize measurement errors) a high secondary voltage, such as 500 V, should be chosen for the neutral or earthing transformer.

Note: The voltage withstand of the bandpass filter voltage divider is 550 V ac for ≤ 30s

It is important that the earthing transformer never becomes saturated otherwise ferroresonance may occur. It is sufficient that the transformer knee point voltage be equal to the generator rated line voltage. The low frequency voltage is fed to the relay via a voltage divider and the low frequency measuring current is fed via a miniature current transformer. All interference deviating from the nominal low frequency signal is filtered out.

The 100% stator earth fault protection can also be applied with a primary loading resistor. The 20 Hz voltage is connected via a voltage transformer and the neutral starpoint current is directly measured via a CT, see section 2.22.2.3.

From the measured current and voltage vectors the complex impedance can be calculated and from this the ohmic resistance is determined. This eliminates disturbances caused by the stator earth capacitance and ensures high sensitivity. The relay algorithm can take into account a transfer resistance 64S Series R, that may be present at the neutral or earthing voltage transformer. An example of the series resistance is the total leakage resistance of the earthing or neutral transformer, through which the injected voltage is applied to the generator neutral. The algorithm can also account for parallel resistance, 64S Parallel G (G = 1/R), such as an additional earthing transformer connected on the LV side of the step-up transformer. Other error factors can be taken into account by the angle error compensation, 64S Angle Comp.

The relay includes a 20 Hz overcurrent element which can be used as a back-up to the 20 Hz under resistance protection. The overcurrent element is not as sensitive as the under resistance elements as it does not include any transfer resistance compensation or any compensation for capacitance affects.

In addition to the determination of the earth resistance, the relay also includes 95% stator earth fault protection as a back-up to the 100% stator earth fault protection. The neutral voltage protection from the measured earthing/neutral transformer or calculated neutral voltage from the 3 phase voltage input can be used to provide 95% stator earth fault protection and is active during the run-up and run-down of the generator.

AP

The 100% stator earth fault protection includes 2 stages of under resistance protection for alarm and trip and an overcurrent protection stage, with each stage having a definite time delay setting. The protection includes a supervision element to evaluate a failure of the low frequency generator or the low frequency connection.

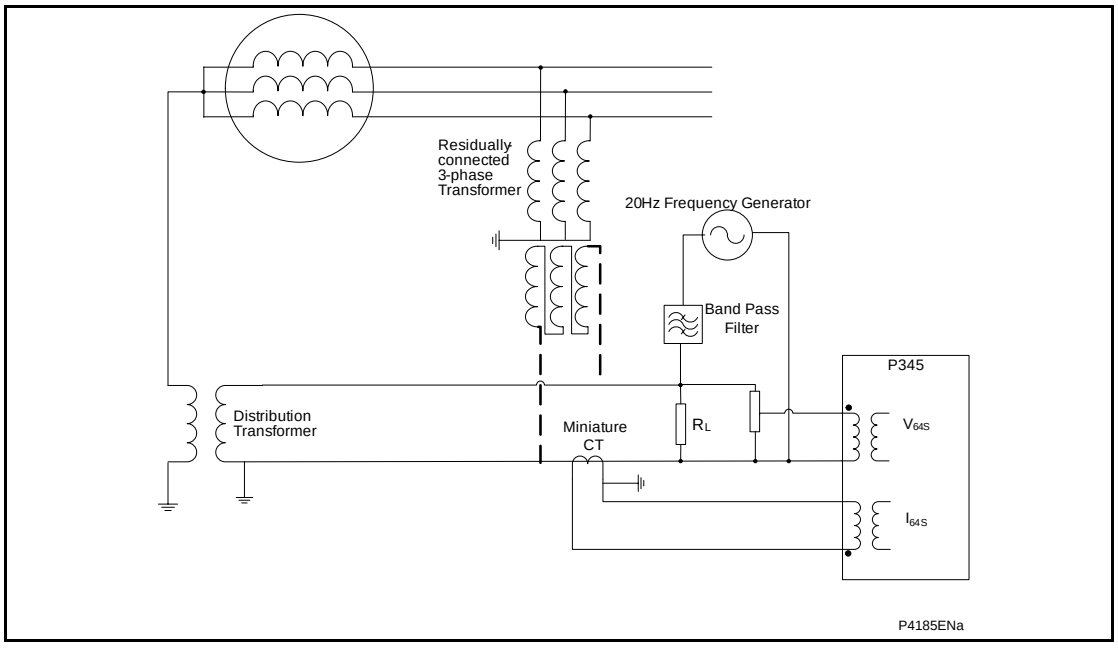


Figure 42: Circuit diagram of the 100% stator earth fault protection with earthing (broken delta) transformer or neutral transformer

Where

R_L loading resistor

V_{64S} displacement voltage at the protective relay

I_{64S} measuring current at the protective relay

2.22.1 Setting guidelines for 100% stator earth fault protection

The 100% stator earth fault protection element can be selected by setting the 64S 100%St EF cell to Enabled.

The 64S R Factor is set as described in section 2.22.2 – Setting Calculation for the R Factor.

The under resistance alarm threshold, 64S Alarm Set, must be set below the level of resistance present under normal conditions. This resistance can be determined by viewing the 64S R cell in the MEASUREMENTS 3 menu. A typical value for the primary fault resistance alarm setting is between 3-8 kΩ .

The under resistance trip threshold, 64S R<2 Trip Set, must be set below the level of resistance present under normal conditions. This resistance can be determined by viewing the 64S R cell in the MEASUREMENTS 3 menu. A typical value for the primary fault resistance trip setting is between 1-2 kΩ .

The overcurrent trip threshold, 64S I>1 Trip Set, must be set above the 20 Hz level of current present under normal conditions. This secondary current can be determined by viewing the 64S I Magnitude cell in the MEASUREMENTS 3 menu.

The P345's 64S protection has a very powerful band pass filter tuned to 20 Hz. The band pass filter is designed with an attenuation of at least -80 db for frequencies less than 15 Hz and greater than 25 Hz. -80 db is equivalent to a noise rejection capability with a noise-to-signal ratio of 10000 to 1. However, it is not possible for the filter to reject all the 'noises' around 20 Hz. When the power system frequency is at 20 Hz, the relay will not be able to distinguish the power system frequency signal and the injected signal.

Under no fault conditions, the influence of the 20 Hz power system components is practically negligible. So there is no risk of relay mal-operation under system frequency conditions, from 0 Hz to 70 Hz. The current measured will effectively be the capacitive current plus the current through the parallel resistance. The 64S I>1 should be set higher than this quiescent current.

For earth faults occurring 0 – 15 Hz and 25 - 70 Hz at any point on the stator windings both the under resistance (64S R<) and overcurrent protection (64S I>) work correctly under these power system frequency conditions due to the relay filtering. The power system frequency components will be removed by the band pass filter and will have no influence on the protection measurements.

The influence of the power system signals depend on the position of the fault. At the star point, the influence is negligible. Therefore both the under resistance (64S R<) and overcurrent protection (64S I>) work correctly under the complete range of power system frequencies from 0 to 70 Hz when the faults occur at the star-point.

For faults not at the star point where the power system frequency signals are at or close to 20 Hz the power system 20 Hz signals become more and more dominant as the fault position moves towards the terminal of the generator. For these faults there is a possibility the R< elements can overreach. In most cases the current is 180° out of phase with the voltage.

The 64S current (I64S(P345)) under fault conditions consists of two components, the 20 Hz current component from the 20 Hz injection system, (I64S(20)) and the 20 Hz current component produced by the neutral displacement voltage, (I64S(G)). At or around 20 Hz, the I64S(G) cannot be filtered off and therefore contributes in magnitude to the I64S(P345), which improves the fault detection capability of the 64S I>1 protection function.

Therefore the 64S I> element can be used to provide back-up protection for faults that occur when the machine is running at 20 Hz. The I64S I>1 Trip can be set as a back-up element 15-25 Hz to the 64S R<1/R<2 elements by setting a longer trip time.

If required the R<1 and R<2 protection can be blocked at around 20 Hz. The 64S F Band Block (operates when the measured frequency is in the range 15-25 Hz) and can be used to inhibit/block the 64S R<1, R<2 protection.

A time delay for these elements can be set in the 64S R<1 Alm Dly, 64S R<2 Trip Dly and 64S I>1 Trip Dly cells. The default time delays provide typical values.

If the 20 Hz voltage drops below the voltage supervision threshold, 64S V<1 Set and the 20 Hz current remains below the current supervision threshold, 64S I< Set, there must be a problem with the 20 Hz connection. The default settings for 64S Supervision element, 64S V<1 Set (1 V) and 64S I<1 Set (10 mA) will be adequate for most applications. Where the loading resistor is less than 1 Ω, the supervision voltage threshold, 64S V<1 Set, must be reduced to 0.5 V, the supervision current threshold, 64S I<1 Set, can be left at 10 mA.

The Comp Angle setting is used to compensate the angle errors between the CT and earthing or neutral transformer. The setting can be found from primary testing.

The 64S Series R setting is used to account for the transfer resistance of the earthing or neutral voltage transformer. The default setting will be zero as the resistance of the voltage transformer is normally negligible. The resistance of the voltage transformer is not negligible if the low frequency voltage is fed to a primary side resistor via the voltage transformer. The setting can be estimated from calculation or from primary testing, see section 2.22.3.

AP

In large power units with a generator CB, applications can be found where there is some additional loading equipment such as an earthing transformer on the low voltage side of the unit transformer to reduce the influence of zero sequence voltage when the generator CB is open. If the low frequency source is connected via the neutral transformer in the generator starpoint, when the generator CB is closed the protection measures the loading resistance on the unit transformer side which can be mistaken for an earth resistance.

The 64S Parallel G setting can be used to account for this additional parallel loading resistance. The default setting is 0, no additional loading resistor.

The neutral transformer-resistor at the star point should produce a resistive current equal to the capacitive current for an earth fault at rated voltage. The transformer, resistor and injection devices should withstand this condition for 10 seconds.

To prevent the secondary load resistance from becoming too small (it should be > 0.5 Ω where possible to minimize measurement errors) a high secondary voltage, such as 500 V, should be chosen for the neutral or earthing transformer. It is important that the earthing transformer never becomes saturated otherwise ferroresonance may occur. It is sufficient that the transformer knee point voltage be equal to the generator rated line voltage.

For a generator earthed with a primary resistor in the generator starpoint the lead resistance between the earthing transformer and the 20 Hz generator/bandpass filter can have a significant affect on the accuracy of the measured resistance by the relay. So if the 20 Hz generator and bandpass filter are mounted in the protection cubicle the loop lead resistance should ideally be kept below 0.5 Ω. If the 20 Hz generator and bandpass filter are mounted near the earthing transformer then this will keep the errors to a minimum. The lead resistance from the 20 Hz generator/banpass filter to the relay does not significantly affect the accuracy of the measured resistance.

For configurations with an earthing transformer and secondary loading resistance the lead resistance does not have a significant affect on the measured resistance by the relay.

Note: Other earth fault protection functions such as residual overvoltage, earth fault or sensitive earth fault protection can be connected in parallel or series with to the 100% stator earth fault protection measurement inputs to provide back-up to the 100% stator earth fault protection.

There will be some measurement of the injected 20 Hz injected and circulating current under normal healthy conditions on the VN1/2, I Sensitive and IN inputs used by these protection functions. For most applications under no fault conditions the 20 Hz voltage measured by the relay across the potential divider in the external filter box and loading resistor will small and be much less than 5% of rated voltage. The 20 Hz current under normal conditions should be very close to zero. So settings can be used to protect 95% of the stator winding in most applications. When commissioning the relay the level of 20 Hz neutral voltage or earth current should be checked to make sure it is less than half the setting value of any protection enabled to provide stability under normal operating conditions. There will be some fluctuation of the 20 Hz neutral voltage and earth current measured by the VN1/2, ISensitive and IN inputs under no fault conditions due to the 50/60 Hz frequency tracking of these inputs.

It is not recommended that the 3rd harmonic method of 100% stator earth fault protection is used in parallel with the 20 Hz injection method as there will be some measurement of the 20 Hz signal by the VN1 input used by the 3rd harmonic protection which could interfere with the correct operation of this sensitive function.

2.22.2 Setting calculations for the R factor

The R Factor calculation depends on the earthing arrangement of the generator and the location of the CT for the 64S current measurement.

2.22.2.1 Generator earthed via earthing transformer

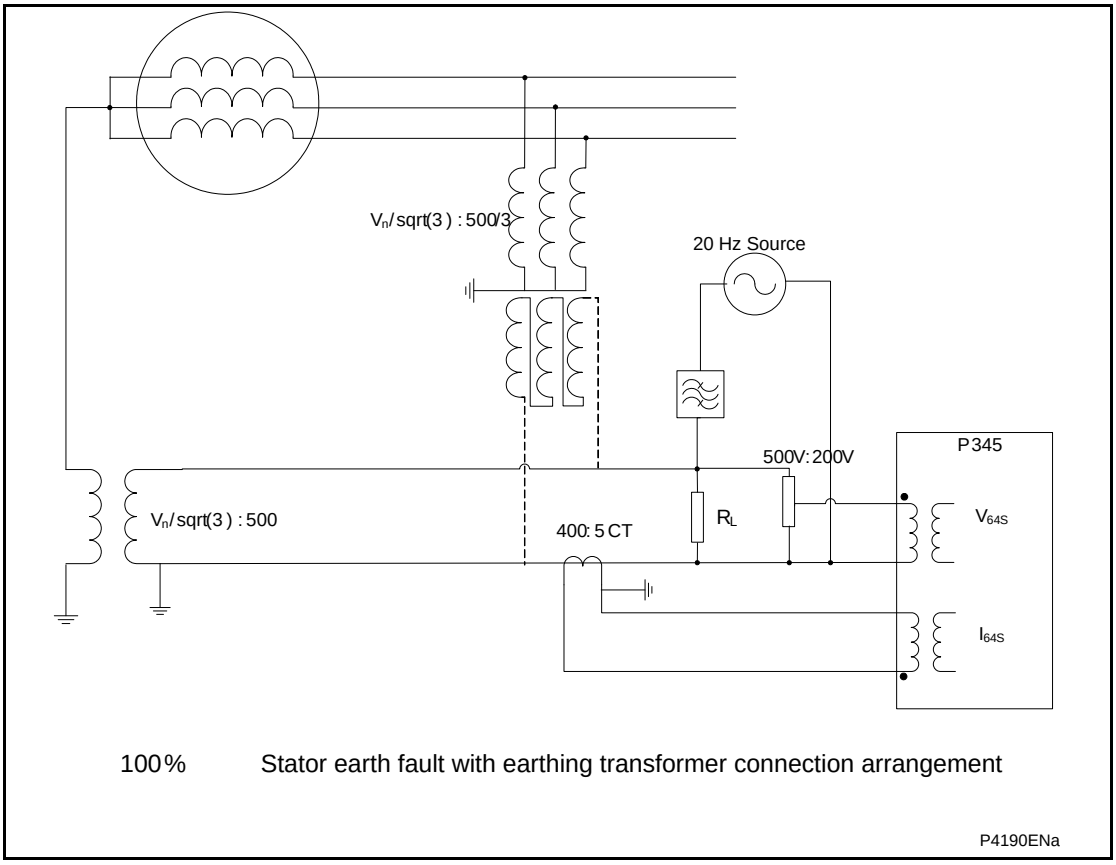


Figure 43: 64S Connection for generators earthed via earthing transformer

With this arrangement, the injected voltage is applied through the secondary of the earthing transformer, which can either be a distribution transformer located at the neutral of the generator, or a three-phase, five limb voltage transformer with the secondary windings connected in broken delta. The current is also measured on the secondary transformer circuit. Therefore the relay is measuring the secondary fault resistance reflected through the earthing transformer. The primary fault resistance is related to the secondary resistance based on the following relationship:

$$\frac{R_{Primary}}{R_{Secondary}} = \frac{V_{Primary}^{2}}{V_{Secondary}^{2}}$$

It is also necessary to take into account the potential divider and the CT ratio. Therefore the primary resistance is calculated from the secondary resistance as follows:

$$R_{Primary} = (\frac{V_{Primary}}{V_{Secondary}})^2 x \frac{V_{Divider\ Ratio}}{CT_{Ratio}} xR_{Secondary}$$

Where $\frac{V_{Primary}}{V_{Secondary}} = \frac{1}{3} \cdot \frac{\frac{V_{n\ Primary}}{\sqrt{3}}}{\frac{V_{n\ Secondary}}{3}}$ for the open-delta VT,

or, $\frac{V_{Primary}}{V_{Secondary}} = \frac{\frac{V_{n\ Primary}}{\sqrt{3}}}{V_{n\ Secondary}}$ for earthing transformer connected at the generator neutral.

Using the data shown in the diagram above as an example and assuming the 1A rated current input is used,

$$R_{Primary} = (\frac{V_n / \sqrt{3}}{500})^2 x \frac{5}{2} x \frac{5}{400} xR_{Secondary}$$

Therefore,

$$R_{Factor} = (\frac{V_n / \sqrt{3}}{500})^2 x \frac{5}{2} x \frac{5}{400}$$

2.22.2.2 Generator earthed via primary resistor in generator starpoint

In some power systems the generators have a load resistor installed directly in the generator starpoint to reduce interference. The following diagram shows the connection of the 20 Hz generator, band pass filter and protection device. The 20 Hz voltage is injected into the generator starpoint via a powerful voltage transformer across the primary load resistor. In the presence of an earth fault, an earth current flows through the CT in the starpoint. The protection detects this current in addition to the 20 Hz voltage.

A two pole isolated voltage transformer must be used with low primary/secondary impedance. This applies for the 20 Hz frequency.

Primary voltage: Vn,Generator /√3 (non-saturated up to Vn,Generator)

Secondary voltage: 500 V

Type and class: 3000 VA (for 20 s), class 0.5 (50 Hz or 60 Hz)

Primary – secondary impedance (ZPS) - ZPS <RL (ZPS <1000 Ω)

The CT is installed directly in the starpoint on the earth side, downstream of the load resistor.

Type: 15 VA 5P10 or 5P15

Rated secondary current: 5 A

Transformation Ratio: 1 (5A/5A)

As the transformation ratio is 1:1, a current transformer with a maximum number of ampere windings must be chosen.

Notes: The linear range of the 100% stator earth fault input is up to 2 In. So if the earth fault current is limited to <2A then the 100% stator earth fault 1A input can be used. For earth fault currents 2-10A the relay 5A current input can be used.

For the 5A inputs the 64S I Magnitude measurement in the Measurements 3 menu will show 5 times lower current than being injected. There is no CT ratio setting for the 100% stator earth fault current input, however the resistance measurement and 64SR<1/2 protection can be compensated by the 64S R Factor setting if the 5A input is used by multiplying the CT ratio by 5 in the formula for the R factor. If the 64S I>1 protection is used then the setting needs to be divided by a factor of 5 when using the 5A input.

During the primary test the correction angle (64S Angle Comp) and the ohmic transfer resistance (R factor) of the voltage transformer must be determined and set.

The primary resistance and conversion factor for the resistance (R Factor) is calculated as follows:

$$R_{Primary} = VT_{Ratio} x \frac{V_{Divider\ Ratio}}{CT_{Ratio}} x R_{Secondary}$$

Where the VT ratio is

$$VT_{Ratio} = \frac{V_{n\ Primary} / \sqrt{3}}{V_{n\ Secondary}}$$

Using the data shown in the diagram as an example and assuming the 5A rated current input is used,

$$R_{Primary} = (\frac{V_n / \sqrt{3}}{500}) x \frac{5}{2x5} x R_{Secondary}$$

Therefore,

$$R_{Factor} = (\frac{V_n / \sqrt{3}}{500}) x \frac{5}{10}$$

Note: Due to the transfer resistance, there may not be an ideal transformation ratio of the voltage transformers. For this reason major deviations of the **R Factor** can occur. It is recommended to measure the transformation ratio with 20 Hz infeed when the machine is at standtill. This value should then be set, see Commissioning chapter, *P34x/EN CM*.

2.22.2.3 Setting example with generator earthed via a primary resistor in generator starpoint

Voltage transformer rating: 10.5 kV/ √3/500 V, 3000 VA (for 20 s) class 0.5 (non-saturated up to Vn,Generator)

Voltage divider: 5:2

Current transformer: 5A/5A, 15 VA 5P10

The maximum primary earth fault current should be limited by the primary resistor to <10A, preferably 4-8A. If the primary earth fault current is limited to 5A then the primary load resistor is 1212 Ω.

Primary Load Resistor: $RL = \frac{10.5kV / \sqrt{3}}{5} = 1212\ \Omega$

AP

The resistor as well as limiting the earth fault current to a suitable value prevents high transient overvoltages in the event of an arcing earth fault. For this reason the equivalent resistance in the stator circuit should not exceed the impedance at system frequency of the total summated capacitance of the three phases.

The linear range of the 100% stator earth fault input is up to 2 In. So if the earth fault current is limited to <2 A then the 100% stator earth fault 1A input can be used. For earth fault currents 2-10 A the relay 5 A current input can be used.

For the 5A inputs the 64S I Magnitude measurement in the Measurements 3 menu will show 5 times lower current than being injected. There is no CT ratio setting for the 100% stator earth fault current input, however the resistance measurement and 64SR<1/2 protection can be compensated by the 64S R Factor setting if the 5 A input is used by multiplying the CT ratio by 5 in the formula for the R factor. If the 64S I>1 protection is used then the setting needs to be divided by a factor of 5 when using the 5A input.

$$R_{Factor} = (\frac{10.5kV/\sqrt{3}}{500})x\frac{5}{10} = 6.06$$

Voltage across the resistor during an earth fault is 10.5 kV/√3 = 6.1 kV and with field forcing may be 1.3 x 6.1 = 8 kV. So, 8 kV insulation will be satisfactory.

Typical trip and alarm settings for the 100% stator earth fault under resistance elements are:

Trip stage: primary 2 kΩ, secondary 330 Ω

Alarm stage: primary 4 kΩ, secondary 660 Ω

AP

The IN current input used by the stator earth fault protection can also be connected to the earth CT to provide back-up stator earth fault protection for the generator.

To provide 95% stator earth fault protection

IN>1 Current = 0.05 x 5 = 0.25A

The VN1 voltage input used by the residual overvoltage/NVD protection can also be connected across the voltage divider to provide back-up stator earth fault protection for the generator. The voltage divider in the filter device can be used to provide a 5:1 divider to connect 100 V rated voltage to the VN1 input (Vn=100/120 V). Connections 1A1-1A2 on the filter provides a 5:1 divider to connect 100 V rated voltage to the VN1 input.

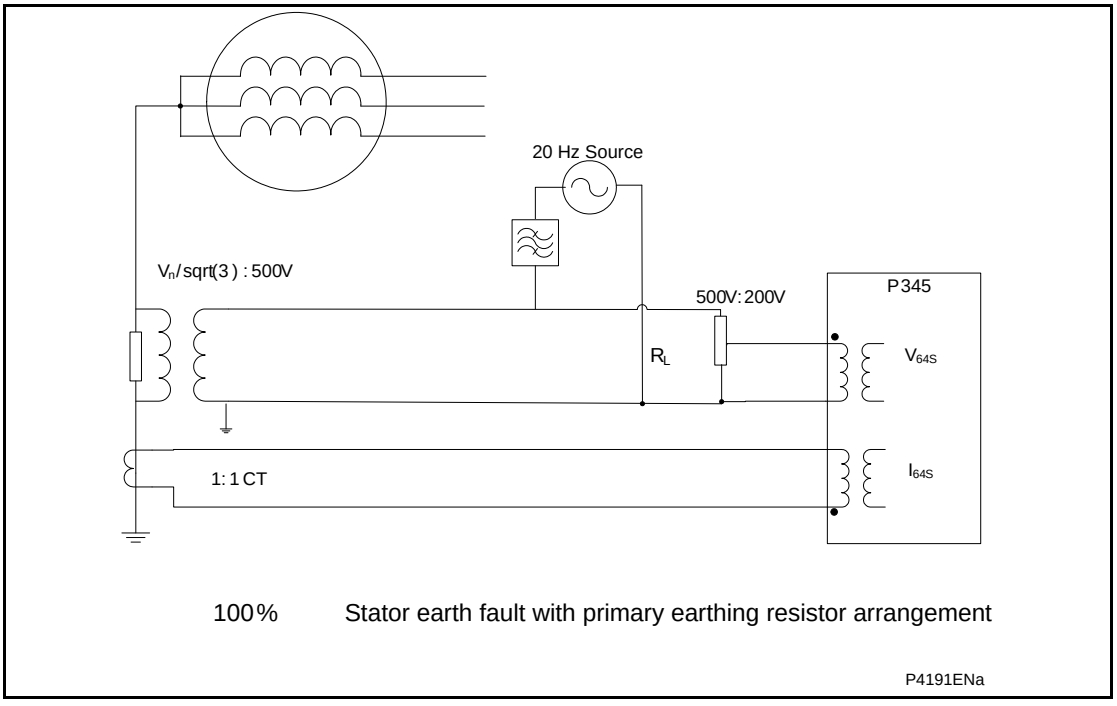


Figure 44: 64S Connection for generators earthed via primary resistor

2.22.2.4 Setting example with generator earthed via earthing transformer and secondary resistor at the terminals of the generator

Voltage transformer rating: 10.5 kV/√3 / 500/3 V (non-saturated up to $Vn_{,Generator}$)

Voltage divider: 5:2

Current transformer: 200/5

The transformation ratio of the miniature CT 400 A:5 A can been halved to 200:5A by passing the primary conductor twice through the transformer window.

The maximum primary earth fault current should be limited by the primary resistor to <10A, preferably 4-8A.

If the primary earth fault current is limited to 5A then primary load resistor is 1212 Ω.

The resistor as well as limiting the earth fault current to a suitable value prevents high transient overvoltages in the event of an arcing earth fault. For this reason the equivalent resistance in the stator circuit should not exceed the impedance at system frequency of the total summated capacitance of the three phases.

$$\frac{R_{Primary}}{R_{Secondary}} = \frac{V_{Primary}^{2}}{V_{Secondary}^{2}}$$

Secondary Load Resistor: $RL = 1212 \times \left(\frac{3x\sqrt{3}x500}{10.5kVx3} \right)^{2} = 8.25\ \Omega$

Voltage transformer secondary maximum earth fault current is 60A so with a 200:5A CT the secondary current at the relay is 1.5A.

The linear range of the 100% stator earth fault input is up to 2 In. So if the earth fault current is limited to <2 A then the 100% stator earth fault 1 A input can be used. For earth fault currents 2-10A the relay 5 A current input can be used.

$$R_{Factor} = (\frac{10.5kV/\sqrt{3}}{500})^{2} x \frac{5}{2} x \frac{5}{200} = 27.563$$

Assuming the transformer is from 3 single phase transformers

The transformer VA rating for 10 s per phase is 1.3 x 1/3 x 5 x 10500 / √3 = 13 KVA for 3 single phase transformers. The 1.3 accounts for an overvoltage factor from field forcing.

For a 20 s rating the VA rating is 9 KVA (13 x √10/√20)

For a 3 phase transformer the VA rating is 3 times higher, 27 KVA for 20 s.

Typical trip and alarm settings for the 100% stator earth fault under resistance elements are:

Trip stage: primary 2 kΩ, secondary 66Ω

Alarm stage: primary 5 kΩ, secondary 165 Ω

The VN1 voltage input used by the residualovervoltage/NVD protection can also be connected across the voltage divider to provide back-up stator earth fault protection for the generator. The voltage divider in the filter device can be used to provide a 5:1 divider to connect 100 V rated voltage to the VN1 input which is typically rated for 100/120 V. Connections 1A1-1A2 on the filter provides a 5:1 divider to connect 100 V rated voltage to the VN1 input.

2.22.2.5 Setting example with generator earthed via earthing transformer and secondary resistor at the starpoint of the generator

Voltage transformer rating: 10.5 kV/ √3/500 V (non-saturated up to $Vn_{,Generator}$)

Voltage divider: 5:2

AP

Current transformer: 200/5

The transformation ratio of the miniature CT 400 A:5 A can been halved to 200:5A by passing the primary conductor twice through the transformer window.

The maximum primary earth fault current should be limited by the primary resistor <10 A, preferably 4-8A.

If the primary earth fault current is limited to 5A then primary load resistor is 1212 Ω.

The resistor as well as limiting the earth fault current to a suitable value prevents high transient overvoltages in the event of an arcing earth fault. For this reason the equivalent resistance in the stator circuit should not exceed the impedance at system frequency of the total summated capacitance of the three phases.

$$\frac{R_{Primary}}{R_{Secondary}} = \frac{V_{Primary}^{2}}{V_{Secondary}^{2}}$$

Secondary Load Resistor: $RL = 1212 \times \left(\frac{\sqrt{3}x500}{10.5kV}\right)^{2} = 8.25\ \Omega$

Voltage transformer secondary maximum earth fault current is 60 A so with a 200:5A CT the secondary current at the relay is 1.5A.

AP

The linear range of the 100% stator earth fault input is up to 2 In. So if the earth fault current is limited to <2 A then the 100% stator earth fault 1A input can be used. For earth fault currents 2-10 A the relay 5 A current input can be used.

$$R_{Factor} = \left(\frac{10.5kV/\sqrt{3}}{500}\right)^{2} x \frac{5}{2} x \frac{5}{200} = 27.563$$

The transformer VA rating for 10 s per phase is 1.3 x 5 x 10500 / √3 = 39 KVA. The 1.3 accounts for an overvoltage factor from field forcing.

For a 20 s rating the VA rating is 27 KVA (39 x √10/√20)

Typical trip and alarm settings for the 100% stator earth fault under resistance elements are:

Trip stage: primary 2 kΩ, secondary 66 Ω

Alarm stage: primary 5 kΩ, secondary 165 Ω

The VN1 voltage input used by the residual overvoltage/NVD protection can also be connected across the voltage divider to provide back-up stator earth fault protection for the generator.

The voltage divider in the filter device can be used to provide a 5:1 divider to connect 100 V rated voltage to the VN1 input which is typically rated for 100/120 V. Connections 1A1-1A2 on the filter provides a 5:1 divider to connect 100 V rated voltage to the VN1 input.

2.22.3 Methods to establish the series settings for 64S

The series resistance **64S Series R** is normally set as the total leakage resistance of the earthing transformer, through which the injection equipment is connected. It can either be set by calculations based on the transformer parameters, or by measurements during commissioning. The P345 measurements feature will be able to assist for the latter. See the Commissioning chapter, *P34x/EN CM*, section 6.3.4.5 for the measurement method.

2.22.3.1 By Calculation

Given that the per unit quantity of the total leakage impedance of the transformer is $R_{pu}+jX_{pu}$, the transformer resistance parameters can be calculated as follows.

For the open-delta 3-phase voltage transformer connected at the generator terminal:

$$R_{Primary} = R_{PU} \times \frac{V_{n\,primary}(kV)^2}{\text{Transformer kVA (3ph)}}$$

For an earthing transformer connected to the generator neutral and for generator earthed via a resistor,

$$R_{Primary} = R_{PU} \times \frac{\left(V_{n\,primary}(kV)/\sqrt{3}\right)^2}{\text{Transformer kVA}}$$

2.23 Overfluxing protection (24)

Overfluxing or overexcitation of a generator, or transformer connected to the terminals of a generator, can occur if the ratio of voltage to frequency exceeds certain limits. High voltage or low frequency, causing a rise in the V/Hz ratio, will produce high flux densities in the magnetic core of the machine or transformer. This could cause the core of the generator or transformer to saturate and stray flux to be induced in un-laminated components that have not been designed to carry flux. The resulting eddy currents in solid components (e.g. core bolts and clamps) and end of core laminations can cause rapid overheating and damage.

Overfluxing is most likely to occur during machine start up or shut down whilst the generator is not connected to the system. Failures in the automatic control of the excitation system, or errors in the manual control of the machine field circuit, could allow excessive voltage to be generated. It is also possible for overfluxing to occur during parallel operation when the generator has been synchronized with the local supply network. Sudden loss of load could cause an overvoltage condition, in such circumstances, if the generator excitation system does not respond correctly.

The P342/3/4/5/6 relays provide a five stage overfluxing element. One stage can be set to operate with a definite time or inverse time delay (IDMT) or a user curve, this stage can be used to provide the protection trip output. There are also 3 other definite time stages which can be combined with the inverse time characteristic to create a combined multi-stage V/Hz trip operating characteristic using PSL or a user curve can be used to create a more complex characteristic. An inhibit signal is provided for the V/Hz>1 stage 1 only, which has the inverse time characteristic option. This allows a definite time stage to override a section of the inverse time characteristic if required. The inhibit has the effect of resetting the timer, the start signal and the trip signal. Figure 45, Figure 46, Figure 47 and Figure 48 give examples of the V/Hz settings and PSL logic to achieve a combined multi-stage V/Hz characteristic for a large and small machine.

There is also one definite time alarm stage that can be used to indicate unhealthy conditions before damage has occurred to the machine.

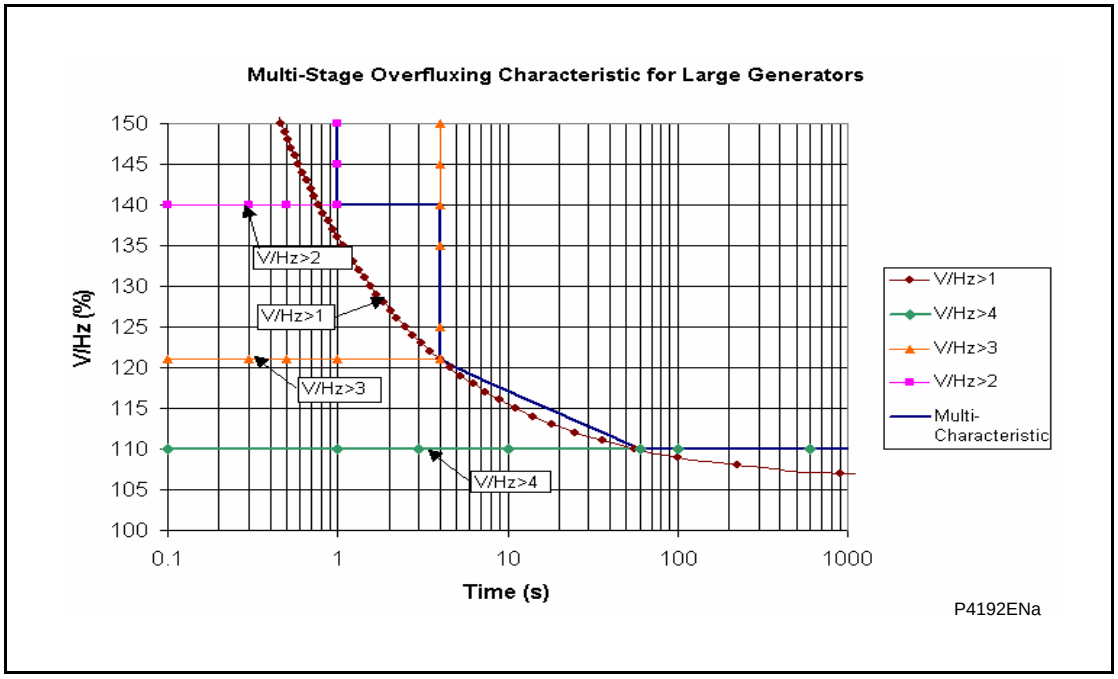


Figure 45: Multi-stage overfluxing characteristic for large generators

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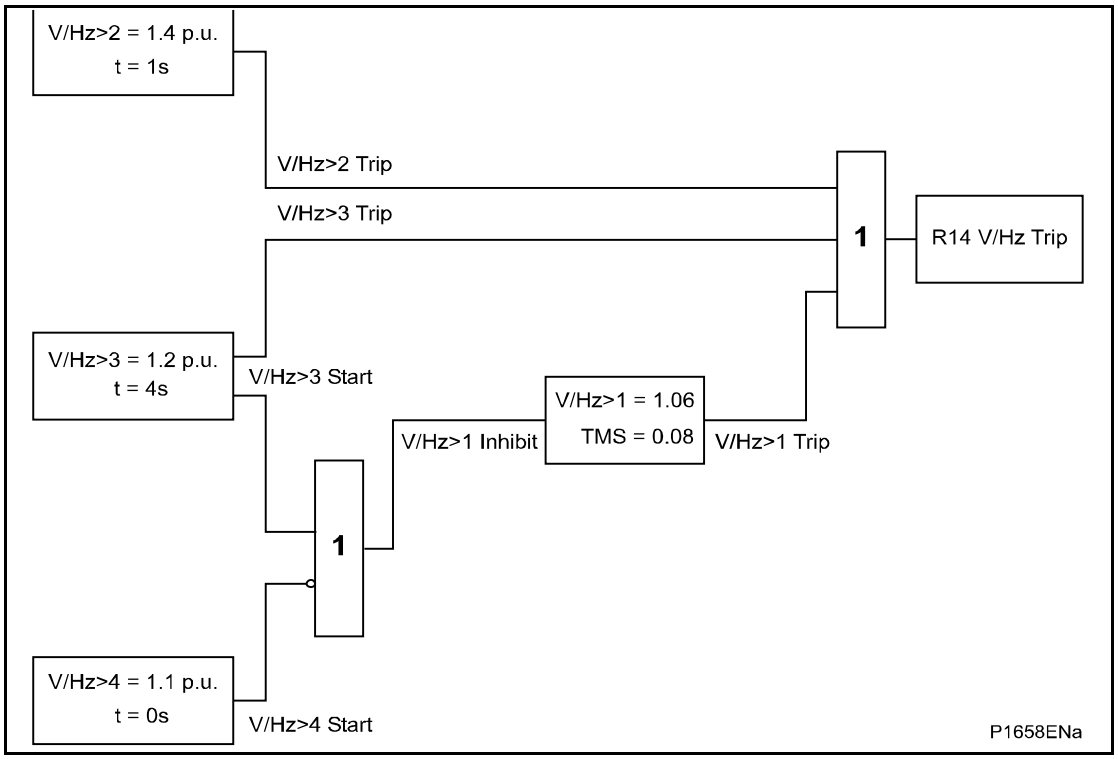


Figure 46: Scheme logic for large generator multi-stage overfluxing characteristic

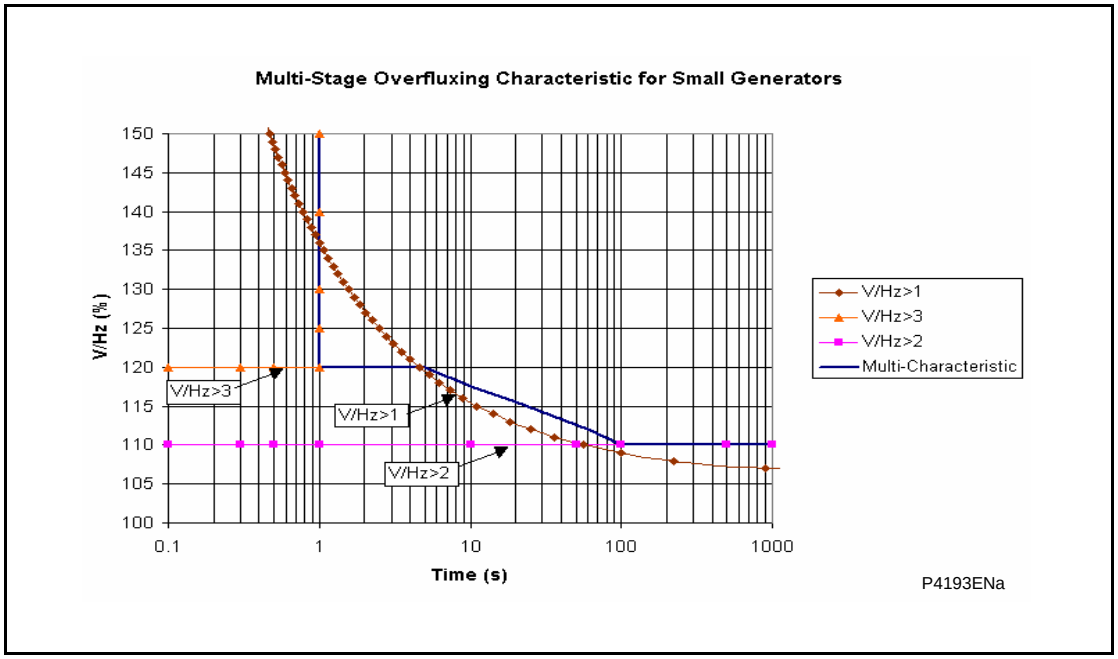


Figure 47: Multi-stage overfluxing characteristic for small generators

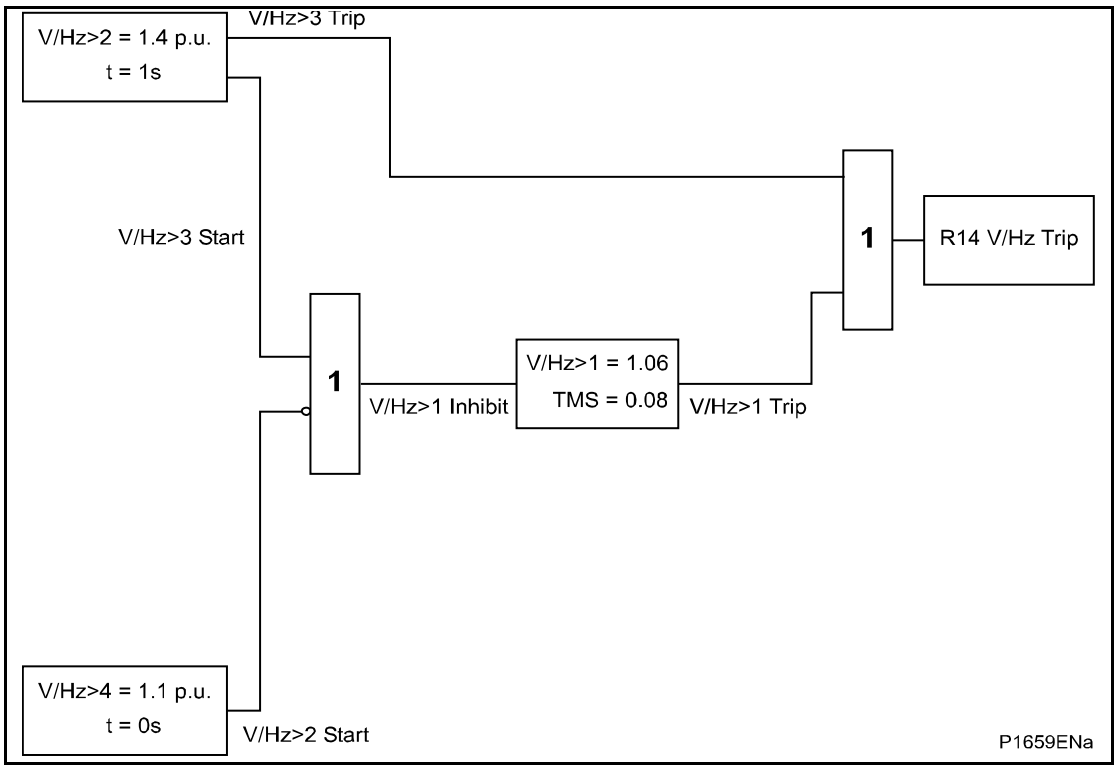


Figure 48: Scheme logic for small generator multi-stage overfluxing characteristic

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2.23.1 5th Harmonic blocking

The 5th Harmonic blocking feature is available for possible use to prevent unwanted operation of the low set differential element under transient overfluxing conditions.

When overfluxing occurs, the transformer core becomes partially saturated and the resultant magnetizing current waveforms increase in magnitude and become harmonically distorted. Such waveforms have a significant 5th harmonic content, which can be extracted and used as a means of identifying the abnormal operating condition.

The 5th harmonic blocking threshold, **Xform Ih(5)**%> in the **DIFFERENTIAL** menu, is adjustable between 0 - 100% differential current. The threshold should be adjusted so that

blocking will be effective when the magnetizing current rises above the chosen threshold setting of the low-set differential protection.

For example, when a load is suddenly disconnected from a power transformer the voltage at the input terminals of the transformer may rise by 10-20% of the rated value. Since the voltage increases, the flux, which is the integral of the excitation voltage, also increases. As a result, the transformer steady state excitation current becomes higher. The resulting excitation current flows in one winding only and therefore appears as differential current which may rise to a value high enough to operate the differential protection. A typical differential current waveform during such a condition is shown in Figure 49. A typical setting for **Xform Ih(5)**%> is 35%

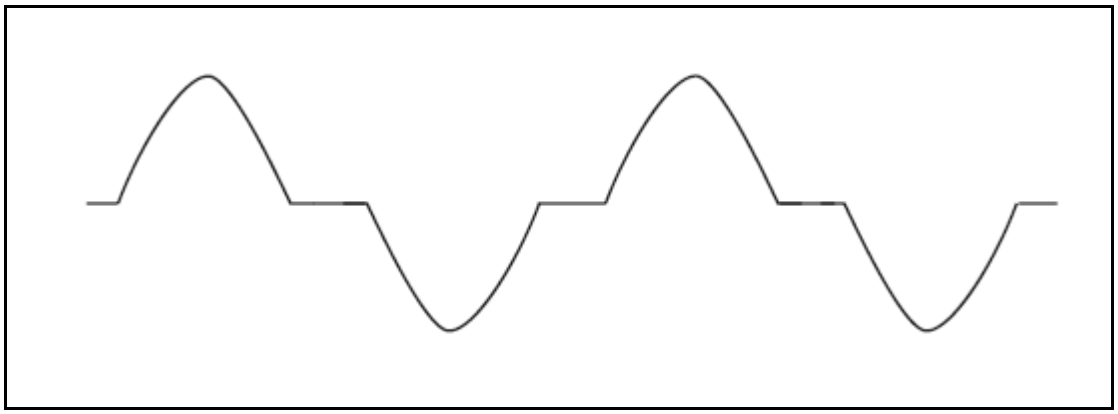


Figure 49: Typical overflux current waveform

To offer some protection against damage due to persistent overfluxing that might be caused by a geomagnetic disturbance, the 5th harmonic blocking element (DDB 1275/1276/1277, 5th Harm Blk A/B/C) can be routed to an output contact using an associated PSL timer. Operation of this element could be used to give an alarm to the network control centre. If such alarms are received from a number of transformers, they could serve as a warning of geomagnetic disturbance so that operators could take some action to safeguard the power system. Alternatively this element can be used to initiate tripping in the event of prolonged pick up of a 5th harmonic measuring element. It is not expected that this type of overfluxing condition would be detected by the AC overfluxing protection. This form of time delayed tripping should only be applied in regions where geomagnetic disturbances are a known problem and only after proper evaluation through simulation testing.

2.23.2 Setting guidelines for overfluxing protection

The V/Hz>1 overfluxing protection element trip stage can be selected by setting the **V/Hz Trip Func** cell to the required time delay characteristic; **DT** for definite time operation, **IDMT**, for inverse time operation or **Default Curve 1/2/3/4** for a user operate curve.

Programmable operate curves can help to match more closely older relays using non standard curves or to match more closely the withstand characteristics of the electrical equipment than standard curves. Programmable reset curves can be used to match more closely the cooling characteristic of the electrical equipment. If a user curve **Default 1/2/3/4** is selected for the V/Hz operate or reset characteristic then in the **User Curves** menu the **UserCurve1/2/3/4 Type** setting should be chosen to match the template of the curve downloaded from the S1 Agile User Programmable Curve tool. For an overfluxing application the **UserCurve1/2/3/4 Type – V/Hz Operate 3.0 or V/Hz Reset 3.1** would normally be selected for the operate or reset characteristic respectively.

The four overfluxing protection trip stages can be **Enabled/Disabled** in the **V/Hz>x Status** cells.

The overfluxing protection alarm stage may be **Enabled/Disabled** in the **V/Hz Alarm Status** cell.

In general, a generator or generator transformer overflux condition will occur if the V/Hz ratio exceeds 1.05 p.u. i.e. a 5% overvoltage condition at rated frequency.

The element is set in terms of the actual ratio of voltage to frequency; the overfluxing threshold setting, **V/Hz>x Trip Setting**, can therefore be calculated as shown below:

A 1.05 p.u. setting = 110/50 x 1.05 = 2.31

Where:

- The VT secondary voltage at rated primary volts is 110 V
- The rated frequency is 50 Hz

The overfluxing alarm stage threshold setting, **V/Hz Alarm Set**, can be set lower than the trip stage setting to provide an indication that abnormal conditions are present and alert an operator to adjust system parameters accordingly.

The time delay settings should be chosen to match the withstand characteristics of the protected generator or generator/transformer. If an inverse time characteristic is selected, the time multiplier setting, **V/Hz>1 Trip TMS**, should be chosen so the operating characteristic closely matches the withstand characteristic of the generator or generator/transformer. If a definite time setting is chosen for the trip stages the time delay is set in the **V/Hz>x Trip Delay** cells. The alarm stage time delay is set in the **V/Hz Alarm Delay** cell.

The 3 definite time stages and 1 DT/IDMT stage can be combined to create a combined multi-stage V/Hz trip operating characteristic using PSL or a user curve can be used to create a more complex characteristic, see examples above.

A definite time reset timer facility can be found for the V/Hz>1 stages as the setting **V/Hz>1 tRESET**. If an IDMT or DT operating characteristic is chosen, this definite time delay is set via the **V/Hz>1 tRESET** setting. If a user curve operate curve is selected, the reset characteristic may be set to either definite time or a user curve as selected in cell **V/Hz>1 Reset Char**. The reset characteristic should be set to match the cooling characteristic/time of the generator or generator transformer.

Reference should be made to manufacturers withstand characteristics before formulating these settings.

2.24 Rate of change of frequency protection (81R)

The two main applications for df/dt protection are network decoupling (loss of mains/loss of grid) and load shedding.

2.24.1 Load shedding

Generated and required active power need to be well balanced in any industrial, distribution or transmission network. As load increases, the generation needs to be stepped up to maintain frequency of the supply because there are many frequency sensitive electrical apparatus that can be damaged when network frequency departs from the allowed band for safe operation. At times, when sudden overloads occur, the frequency drops at a rate decided by the system inertia constant, magnitude of overload, system damping constant and various other parameters. Unless corrective measures are taken at the appropriate time, frequency decay can go beyond the point of no return and cause widespread network collapse. In a wider scenario, this can result in “Blackouts”. To put the network back into a healthy condition, a considerable amount of time and effort is required to re-synchronize and re-energize.

Protective relays that can detect a low frequency condition are generally used in such cases to disconnect unimportant loads in order to save the network, by re-establishing the “generation-load equation”. However, with such devices, the action is initiated only after the event and while some salvaging of the situation can be achieved, this form of corrective action may not be effective enough and cannot cope with sudden load increases, causing large frequency decays in very short times. In such cases a device that can anticipate the severity of frequency decay and act to disconnect loads before the frequency actually reaches dangerously low levels, can become very effective in containing damage.

During severe disturbances, the frequency of the system oscillates as various generators try to synchronize on to a common frequency. The frequency decay needs to be monitored over a longer period of time and time delayed df/dt can be used to make the correct decision for load shedding or provide early warning to the operator on a developing frequency problem. Additionally, the element could also be used as an alarm to warn operators of unusually high system frequency variations.

In the load shedding scheme below, it is assumed under falling frequency conditions that by shedding a stage of load, the system can be stabilized at frequency f2. For slow rates of decay, this can be achieved using the underfrequency protection element set at frequency f1 with a suitable time delay. However, if the generation deficit is substantial, the frequency will rapidly decrease and it is possible that the time delay imposed by the underfrequency protection will not allow for frequency stabilization. In this case, the chance of system recovery will be enhanced by disconnecting the load stage based on a measurement of rate of change of frequency and bypassing the time delay.

A time delayed rate of change of frequency monitoring element that operates independently from the under and over frequency protection functions could be used to provide extra flexibility to a load shedding scheme in dealing with such a severe load to generation imbalance. A more secure load shedding scheme could be implemented using f + df/ft by supervising the df/dt element with under frequency elements.

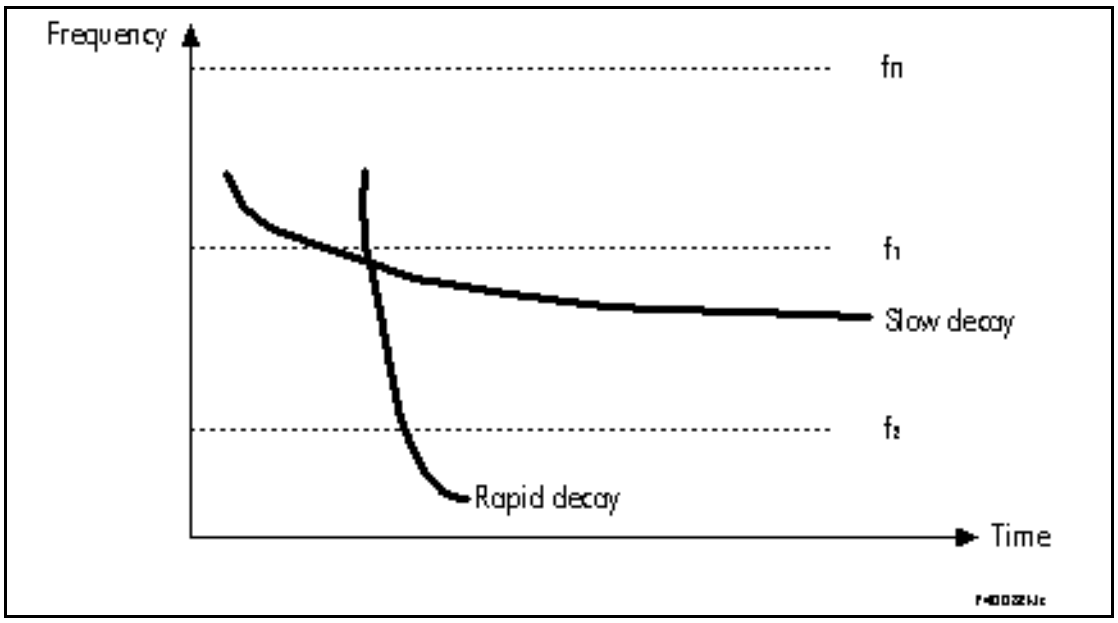


Figure 50: Rate of change of frequency protection

2.24.2 Loss of mains protection

If the capacity of an embedded generator exceeds the locally connected load it is conceivable that it could supply the local load in island mode. Fault clearance may disconnect part of the public supply system from the main source of supply resulting in the embedded generation feeding the local loads, i.e. a ‘Loss of Mains’ or ‘Loss of Grid’ condition. This is shown in Figure 51. A fault at F will result in the tripping of CB1 disconnecting substations S1, S2 and S3 from the main source of supply. Also note that transformer T1 was supplying the earth connection for S1, S2 and S3, this earth connection is lost when CB1 opens. Should the load at substations S1 and S2 greatly exceed the rating of EG1, the generator will slow down quickly and underfrequency and/or undervoltage relays could operate to disconnect EG1 from the system. The worst scenario is when the external load is smaller than the generator rating; in this case the generator can continue to operate normally supplying the external loads. The local system will now be operating unearthed and overcurrent protection may be inoperative at S1 and S2 due to the low fault supplying capacity of generator EG1. The embedded generator may also lose synchronism with the main system supply leading to serious problems if CB1 has auto reclosing equipment.

An even more serious problem presents itself if manual operation of distribution switchgear is considered. System Operation staff may operate circuit breakers by hand. In these circumstances it is essential that unsynchronized reclosure is prevented as this could have very serious consequences for the operator, particularly if the switchgear is not designed, or rated, to be operated when switching onto a fault. To protect personnel, the embedded machine must be disconnected from the system as soon as the system connection is broken, this will ensure that manual unsynchronized closure is prevented.

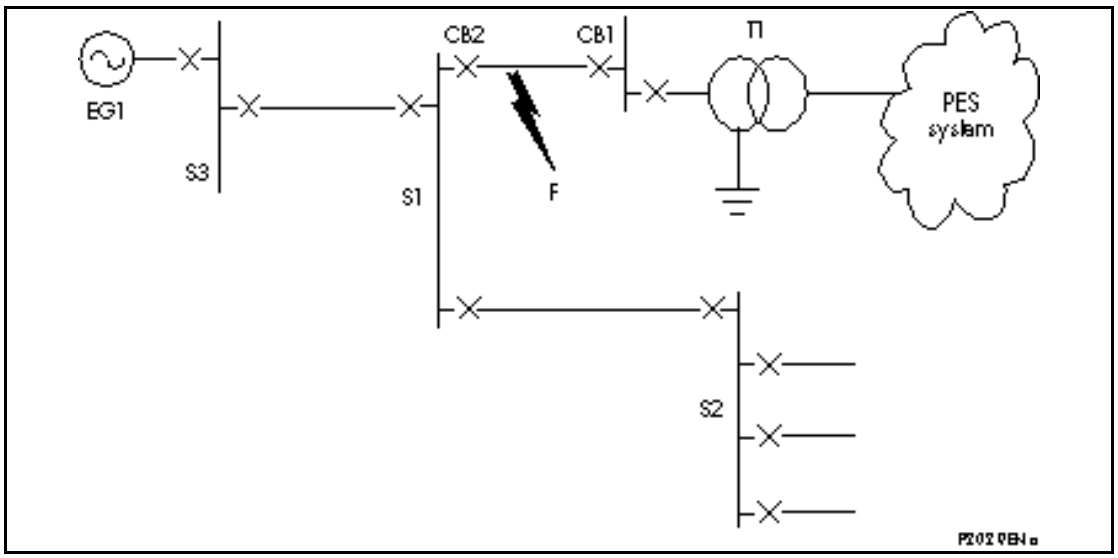


Figure 51: Typical system with embedded generation

Where the embedded generator does not export power under normal conditions it may be possible to use directional power or directional overcurrent protection relays to detect the export of power under loss of mains conditions. If export of power into the system is allowed it may not be possible to set directional relays using settings sensitive enough to detect the loss of the mains connection. In such circumstances a rate of change of frequency protection can be applied. This detects the slight variation in generator speed that occurs when the main supply connection is disconnected and the generator experiences a step change in load.

The type of protection required to detect Loss of Mains conditions will depend on a number of factors, e.g. the generator rating, size of local load, ability to export power, and configuration of supply network etc. Protection requirements should be discussed and agreed with the local Public Electricity Supplier before permission to connect the embedded generator in parallel with the system is granted.

A number of protection elements that may be sensitive to the Loss of Mains conditions are offered in the P34x relay; rate of change of frequency, overpower protection, directional overcurrent protection, frequency protection, voltage Protection. Application of each of these elements is discussed in more detail in the P341 manual.

When a machine is running in parallel with the main power supply the frequency and hence speed of the machine will be governed by the grid supply. When the connection with the grid is lost, the islanded machine is free to slow down or speed up as determined by the new load conditions, machine rating and governor response. Where there is a significant change in load conditions between the synchronized and islanded condition the machine will speed up or slow down before the governor can respond.

The rate of change of speed, or frequency, following a power disturbance can be approximated by:

$$df/dt = \frac{\Delta P.f}{2GH}$$

Where

P = Change in power output between synchronized and islanded operation

f = Rated frequency

G = Machine rating in MVA

H = Inertia constant

This simple expression assumes that the machine is running at rated frequency and that the time intervals are short enough that AVR and governor dynamics can be ignored. From this equation it is clear that the rate of change of frequency is directly proportional to the change in power output between two conditions. Provided there is a small change in load between the synchronized and islanded (loss of mains) condition the rate of change of frequency as the machine adjusts to the new load conditions can be detectable. The change in speed of the machine is also proportional to the inertia constant and rating of the machine and so will be application dependent.

Care must be taken in applying this type of protection as the prime consideration is detecting the loss of grid connection. Failure to detect this condition may result in unsynchronized re-connection via remote re-closing equipment. However, if too sensitive a setting is chosen there is a risk of nuisance tripping due to frequency fluctuations caused by normal heavy load switching or fault clearance. Guidance can be given for setting a rate of change of frequency element but these settings must be thoroughly tested on site to prove their accuracy for a given machine and load.

The element also allows the user to set a frequency band within which the element is blocked. This provides additional stability for non loss of grid disturbances which do not affect the machine frequency significantly.

2.24.3 Setting guidelines for df/dt protection

There are some global df/dt settings that affect all protection stages that can be used to smooth out the frequency measurements and provide stable operation of the protection, **df/dt avg cycles** and **df/dt iterations**. These settings enable the user to select the number of cycles the frequency is averaged over and the number of iterations of the averaged cycles before a start is given. Two **Operating Mode** settings are provided: **Fixed Window** and **Rolling Window**. The **Fixed Window** setting is mainly provided for compatibility with the previous P341 df/dt function which used two consecutive calculations of a 3 cycle fixed window to initiate a start.

The previous software version P341 df/dt element calculated the rate of change of frequency every 3 cycles by calculating the frequency difference over the 3-cycle period as shown below.

$$df/dt = \frac{f_n - f_{n-3cycle}}{3cycle}$$

Two consecutive calculations must give a result above the setting threshold before a trip decision can be initiated.

For loss of grid applications it is recommended that **df/dt avg cycles** = 3 and **df/dt iterations** = 2 and the **Operating Mode = Fixed Window** as per the original P341 algorithm.

For load shedding applications the **df/dt avg cycles** and **df/dt iterations** and the **Operating Mode, Fixed Window/Rolling Window** will depend on the operating time and stability requirements. The df/dt measurement will provide more stability to power system oscillations when the number of iterations and averaging cycles is high but this will make the function slower. Typical settings for load shedding applications are **df/dt avg cycles = 5, df/dt iterations = 1** and the **Operating Mode = Rolling Window**. For load shedding applications with low df/dt settings < 0.5 Hz/s higher settings for the averaging cycles and iterations should be considered to provide better stability.

The df/dt feature is available only when the **df/dt** option is enabled in the **CONFIGURATION** menu. All four stages may be enabled/disabled by the **df/dt>n Status** cell depending on which element is selected.

Each stage has a direction setting **df/dt>n Dir'n – Negative, Positive, Both**. This setting determines whether the element will react to rising or falling frequency conditions respectively, with an incorrect setting being indicated if the threshold is set to zero. For loss of mains applications the **df/dt>1 Dir'n** should be set to **Both** to match the previous P341 algorithm.

A sudden disconnection of loads leads to a surplus of active power. The frequency rises and causes a positive frequency change. A failure of generators, on the other hand, leads to a deficit of active power. The frequency drops and leads to a negative frequency change. For load shedding applications the **df/dt>1 Dir'n** is typically set to **Negative** for falling frequencies.

For loss of mains applications the **df/dt>1** setting threshold should be set such that the loss of mains condition can be detected; this can be determined by system switching during initial commissioning. A typical setting for **df/dt>1 Setting** is 0.2 to 0.6 Hz/s. For df/dt>1 only, the user can select a deadband around the nominal frequency, within which this element is blocked. The dead band is defined with high and low frequency settings **df/dt>1 f Low** and **df/dt> f High**. The deadband is eliminated if the high and low frequencies are set the same or the **df/dt> f L/H** setting is set to **Disabled**. The deadband provides additional stability for non loss of grid disturbances which do not affect the machine frequency significantly.

System simulation testing has shown that the following settings can provide stable operation for external faults, and load switching events, whilst operating for a loss of mains event which causes a 10% change in the machine output, for a typical 4 MW machine. These can be used as a guide but will by no means be acceptable in all applications. Machine rating, governor response, local load and system load, will all affect the dynamic response of a machine to a loss of mains event.

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df/dt>1 Setting – 0.2 Hz/s

df/dt Time Delay – 0.5 s

df/dt>1 f High – 50.5 Hz

df/dt>1 f Low – 49.5 Hz

df/dt>1 Dir'n – Both

Once installed, the settings should be periodically reviewed to ensure that they are adequate to detect a loss of grid connection event, but not too sensitive such that unwanted tripping occurs during normal fault clearance, or load switching, that does not lead to the loss of mains condition. Safety of personnel is paramount and this should be kept in mind when optimizing settings; non-synchronized manual operation of circuit breakers must be prevented by disconnection of the embedded machine when the system becomes separated.

For load shedding the **df/dt>n setting** value depends on the application and is determined by power system conditions. In most cases, a network analysis will be necessary. The under/overfrequency start DDBs can be used to supervise the df/dt elements using the df/dt>1/2/3/4 Tmr Blk DDBs, if required to provide a more secure load shedding scheme.

The following can be used as an example for estimation of the df/dt settings. This applies for the change rate at the beginning of a frequency change (approx. 1 second).

$$df/dt = \frac{\Delta P.f}{2GH}$$

For hydro-electric generators (salient-pole machines) H = 1.5 s to 6 s

For turbine-driven generators (cylindrical-rotor machines) H = 2 s to 10 s

For industrial turbine-generators H = 3 s to 4 s

f = nominal frequency

H = 3 s

Case 1: ΔP/G = 0.12

Case 1: ΔP/G = 0.48

Case 1: df/dt = -1 Hz/s

Case 2: df/dt = -4 Hz/s

The time delay setting, **df/dt>n Time Delay**, can be used to provide a degree of stability against normal load switching events which will cause a change in the frequency before governor correction.

2.25 Dead machine/unintentional energization at standstill protection (50/27)

Accidental energization of a generator when the machine is not running can cause severe damage to the machine. If the breaker is closed, when the machine is at standstill, the generator will begin to act as an induction motor with the surface of the rotor core and the rotor winding slot wedges acting as the rotor current conductors. This abnormal current in the rotor can cause arcing between components, e.g. slot wedge to core, and results in rapid overheating and damage.

To provide fast protection for this condition, the P343/4/5 relay provides an instantaneous overcurrent element that is gated with a three-phase undervoltage detector.

AP

The element is enabled when the machine is not running, i.e. not generating any voltage, or when the breaker is open. Therefore the element can have a low current setting, resulting in high speed operation when required. For the element to operate correctly the relay voltage input must be from a machine side VT; busbar VTs cannot be used.

In the P343/4/5 the 3 phase current source for the low impedance dead machine protection can be selected using the **DM CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting. In the standard connection diagrams in the installation chapter, *P34x/EN IN*, **IA-1/IB-1/IC-1** is connected to the neutral side CTs and **IA-2/IB-2/IC-2** is connected to the terminal side CTs.

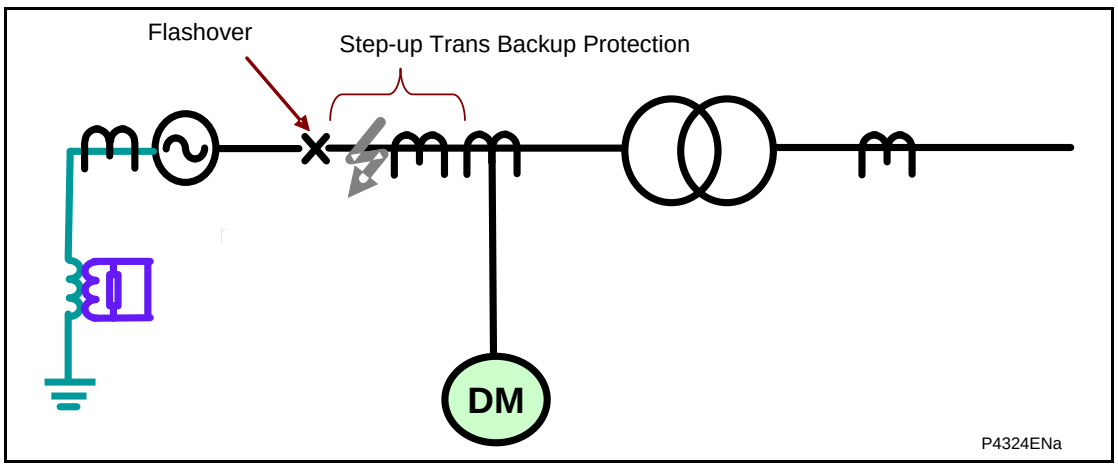


Figure 52: GCB flashover and transformer back-up protection

If the CT inputs of the dead machine protection are selected to use the generator terminal side CTs as shown above, after the generator CB is open, the protection can also act as the generator CB flashover and back-up protection for the step-up transformer. Otherwise the fault as shown in the figure above has to be cleared by the overcurrent protection located on the main transformer HV side. The HV overcurrrent protection is not as sensitive or as fast as the dead machine protection which can be set instantaneous and with a sensitive current setting for this application.

2.25.1 Setting guidelines for dead machine protection

The dead machine protection element can be selected by setting the **Dead Mach Status** cell to **Enabled**.

In the P343/4/5 select the the 3 phase current source for the low impedance dead machine protection using the **DM CT Source – IA-1/IB-1/IC-1** or **IA-2/IB-2/IC-2** setting. In the standard connection diagrams in the installation chapter, *P34x/EN IN***, IA-1/IB-1/IC-1** is connected to the neutral side CTs and **IA-2/IB-2/IC-2** is connected to the terminal side CTs. For most applications either the neutral or terminal side CTs can be used.

The overcurrent threshold, **Dead Mach I>,** can be set to less than full load current as the element will not be enabled during normal machine operation. A setting of 10% of full load current can typically be used.

The undervoltage threshold, **Dead Mach V<,** should typically be set at 50% of the nominal voltage to ensure that the element is enabled when the machine is not running.

The pick-up time delay, **Dead Mach tPU**, which provides a small time delay to prevent initialization of the element during system faults, should typically be set to 5 s, or at least in excess of the protection clearance time for a close up phase to phase fault.

The drop off time delay, **Dead Mach tDO**, ensures that the element remains initialized following accidental closure of the circuit breaker, when the undervoltage detector could reset. A delay of 500 ms will ensure that the element can operate when required.

2.26 Resistive temperature device (RTD) thermal protection

Prolonged overloading of generators may cause their windings to overheat, resulting in premature ageing of the insulation, or in extreme cases, insulation failure. Worn or unlubricated bearings can also generate localized heating within the bearing housing. To protect against any general or localized overheating, the P342/3/4/5/6 relay has the ability to accept inputs from up to 10 - 3 wire Type A PT100 resistive temperature sensing devices (RTD).

Such probes can be strategically placed in areas of the machine that are susceptible to overheating or heat damage. Where power transformers are located close to the protected machine, certain RTD probes could be assigned to provide overtemperature protection for the transformer(s). This could protect against winding hot spot overheating or overtemperature in the bulk of the insulating oil.

Typically a PT100 RTD probe can measure temperature within the range –40° to +300°C. The resistance of these devices changes with temperature, at 0°C they have a resistance of 100 Ω. The temperature at each probe location can be determined by the relay, and is available for:

- Temperature monitoring, displayed locally, or remotely via the relay communications
- Alarming, should a temperature threshold be exceeded for longer than a set time delay
- Tripping, should a temperature threshold be exceeded for longer than a set time delay

Should the measured resistance be outside of the permitted range, an RTD failure alarm will be raised, indicating an open or short circuit RTD input.

Note: Direct temperature measurement can provide more reliable thermal protection than devices that use a thermal replica energized from phase current. The latter is susceptible to inaccuracies in time constants used by the replica model, and also inaccuracies due to the variation in ambient temperature.

See the Installation chapter (*P34x/EN IN*), for recommendations on RTD connections and cables.

2.26.1 Setting guidelines for RTD thermal protection

Each RTD can be enabled by setting the relevant bit in **Select RTD**. For example if Select RTD is set to 0000000111, then RTD1, RTD2 and RTD3 would be enabled and the associated settings would be visible in the menu.

The temperature setting for the alarm stage for each RTD can be set in the **RTD x Alarm Set** cells and the alarm time delay in the **RTD x Alarm Dly** cell.

The temperature setting for the trip stage for each RTD can be set in the **RTD x Trip Set** cells and the trip stage time delay in the **RTD x Trip Dly** cell.

Typical operating temperatures for protected plant are given in the table below. These are provided as a guide, actual figures must be obtained from the equipment manufacturers:

Parameter	Typical service temperature	Short term overloading at full load
Bearing temperature generators	60 - 80°C, depending on the type of bearing.	60 - 80°C+
Top oil temperature of transformers	80°C (50 - 60°C above ambient).	A temperature gradient from winding temperature is usually assumed, such that top oil RTDs can provide winding protection
Winding hot spot temperature	98°C for normal ageing of insulation. Cyclic overloading might give	140°C+ during emergencies

Table 9: Typical operating temperatures of plant.

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2.27 P342 pole slipping protection (78)

A generator might pole slip, or fall out-of-step with other power system sources, in the event of failed or abnormally weak excitation or as a result of delayed system fault clearance. This can be further aggravated when there is a weak (high reactance) transmission link between the generator and the rest of the power system.

The process of pole slipping following excitation failure is discussed in section 2.14. The P342 field failure protection function should respond to such situations to give a time delayed trip. The electrical/mechanical power/torque oscillations following excitation failure may be relatively gentle. If pole slipping occurs with maximum excitation (generator e.m.f. >2.0 p.u.), the power/torque oscillations and power system voltage fluctuations following loss of stability can be much more severe. For large machines there may be a requirement to provide protection to trip the generator under such circumstances, to prevent plant damage or remove the disturbance to the power system.

Pole slipping protection is frequently requested for relatively small generators running in parallel with strong public supplies. This might be where a co-generator runs in parallel with the distribution system of a public utility, which may be a relatively strong source, but where high-speed protection for distribution system faults is not provided. The delayed clearance of system faults may pose a stability threat for the co-generation plant.

With the P342 relay there is no specific pole slipping protection function, but a number of the protection functions provided can offer a method of ensuring delayed tripping, if appropriately applied.

2.27.1 Reverse power protection

During a pole slipping event the machine will cyclically absorb and export power as the machine rotor slips with respect to the power system. Therefore, any power element selected to operate from reverse power can pick-up during the pole slip. Reverse power protection tripping is usually time delayed and this time delay will prevent the element from tripping during a pole slip. However, each power protection stage in the P342 relay has an associated delay on drop off, or reset, timer (**Power1 DO Timer**, **Power2 DO Timer**). This can be used to prevent resetting of the reverse power stage during a pole slipping event, leading to eventual tripping if the event continues.

2.27.2 System back-up protection function

In a similar manner to the power protection function, the system back-up protection function would operate cyclically with the periodic high levels of stator current that would arise during pole slipping. These peaks of current may also be accompanied by coincident drops in generator terminal voltage, if the generator is near the electrical center of swinging.

As discussed in section 2.7, the system back-up protection function is provided with a timer characteristic timer-hold setting, **V Dep OC tRESET**, **Z< tRESET**, which can be used to ensure that the protection function will respond to cyclic operation during pole slipping. In a similar manner, some operators of small, unmanned hydro-generators have relied on the integrating action of induction disc overcurrent protection to ensure disconnection of a persistently slipping machine.

2.27.3 Field failure protection function

Slightly faster pole slipping protection might be assured in many applications by appropriately applying the field failure protection function and associated scheme logic timers.

Where the power system source impedance is relatively small in relation to the impedance of a generator during pole slipping, the electrical center of slipping is likely to lie within the generator. This would be 'behind' the relaying point, as defined by the location of the voltage transformer. Such a situation is likely to exist for co-generation schemes and might also be the case for some fairly large utility generation schemes connected to a densely interconnected transmission system. The dynamic impedance of the generator during pole slipping (Xg) should lie between the average value of the direct and quadrature axis transient reactance's (Xd' and Xq') and the average value of the direct/quadrature axis synchronous reactance's (Xd and Xq). However neither extreme would actually be reached. During low-slip periods of a pole slip cycle, the synchronous reactance's would apply, whereas the transient impedance's would apply during periods of relatively high slip.

Figure 53 shows how the impedance seen at the generator protection relaying point may vary during pole slipping for a relatively small co-generator directly connected to a relatively strong distribution power system. The behavior of a generator during pole slipping may be further complicated by intervention of an automatic voltage regulator and by the response of any speed-dependent excitation source (e.g. shaft-driven exciter).

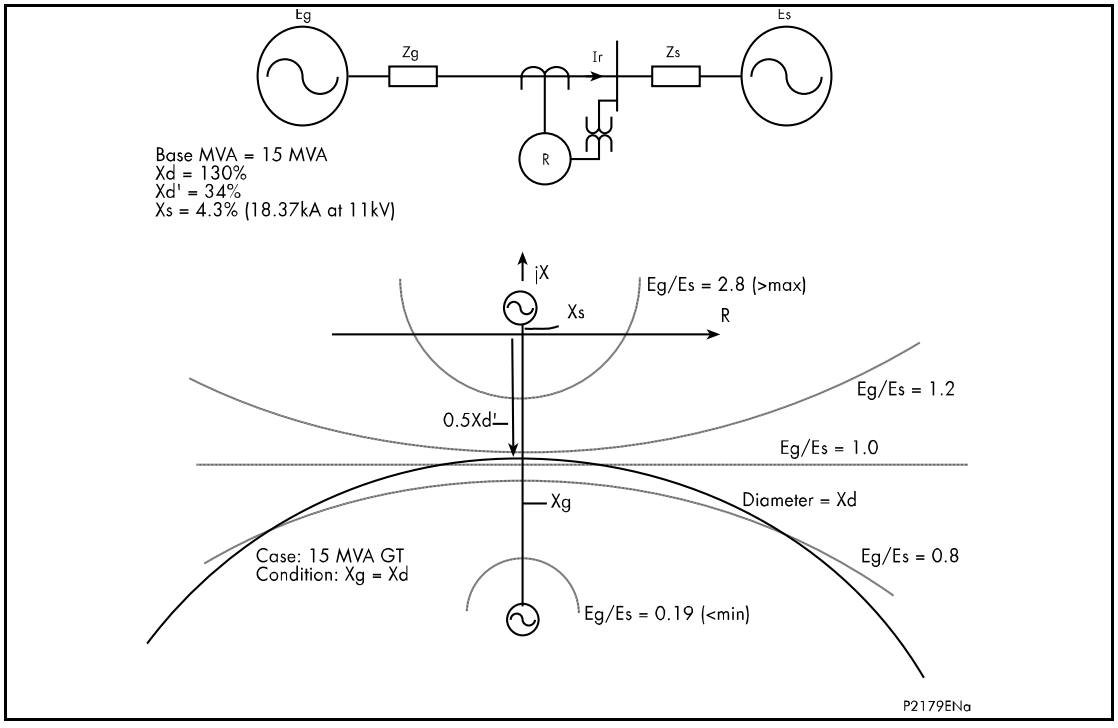


Figure 53: Field failure protection function characteristics (small co-generator)

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It can be seen from the simple analysis of Figure 53 that the field failure protection function may respond to the variation in impedance seen during pole slipping for some applications. However the impedance characteristic offset might have to be reduced to guarantee response for the theoretical lower range of dynamic generator impedance (Xg). The lack of the normally recommended characteristic offset should not pose any problem of unwanted protection function response during the normal range of operation of a machine (with rotor angles kept below 90°), but a longer trip time delay might be required to prevent unwanted protection response during stable power swings caused by system disturbances.

The most marginal condition to detect is where the generator is fully loaded, with maximum excitation applied. Even if the impedance characteristic offset is not reduced, impedance element pick up should still occur during part of a slip cycle, when the machine impedance is high and where the rotor angle is high. More careful consideration might have to be given to the reset time delay setting (**FFail1 DO Timer**) required in such circumstances.

During pole slipping, any operation of the field failure protection function will be cyclic and so it would be necessary to set the reset time delay (**FFail1 DO Timer**) to be longer than the time for which the impedance seen will cyclically lie outside the field failure characteristic. A typical delay setting might be 0.6 s, to cover slip frequencies in excess of 2 Hz. When the timer **FFail1 DO Timer** is set, the field failure trip time delay (**FFail1 Time Delay**) must be increased to be greater than the setting of **FFail1 DO Timer**.

Sometimes pole slipping protection must be guaranteed, especially in the case of a larger utility generator connected to a relatively weak transmission system. In such applications, and where fast tripping is required, or where the pole slipping response of field failure protection function is otherwise uncertain, a stand-alone protection scheme, such as used in the P343/4/5/6 should be used. The delayed detection and tripping offered by the P34x Field Failure protection function should, however, be adequate for many applications.

For further details regarding setting of field failure protection for time delayed pole slipping detection, contact General Electric.

2.28 P343/4/5 pole slipping protection (78)

2.28.1 Introduction

Sudden changes or shocks in an electrical power system such as line switching operations, large jumps in load or faults may lead to power system oscillations which appear as regular variations of the currents, voltages and angular separation between systems. This phenomenon is referred to as a power swing.

In a recoverable situation, the power swing will decay and finally disappear in a few seconds. Synchronism will be regained and the power system will recover to stable operation. In a non-recoverable situation, the power swing becomes so severe that synchronism is lost between the generator and system, a condition recognized as out-of-step or pole slipping from the view of a generator. If such a loss of synchronism does occur, it is imperative to separate the asynchronous areas from the rest of the system before generators are damaged or before a widespread outage can occur.

Pole slipping occurs when the prime mover input power of a generator exceeds the electrical power absorbed by the system. The condition results from the mismatch in the operating frequencies of two or more machines. During pole slipping the machine produces alternatively generating and motoring torque of high magnitudes with corresponding current peaks and voltage dips.

During normal system operation the following events can lead to the generator pole slipping condition.

- The occurrence of an abnormality such as:

A transient system fault.

The failure of the generator governor.

The failure of the generator excitation control (asynchronous running).

Reconnection of an 'islanded' system without synchronization.

- The transient change in the system requirements of real and reactive power components sets the generator rotor to oscillate around the new equilibrium point.
- If the initial transient disturbance is severe enough and for a sufficiently long duration the rotor swing may exceed the maximum stability limit causing the generator to slip poles.
- For a weak system switching transients may also result in pole slipping.

Nowadays, with the advent of EHV systems, large conductor-cooled generators and with the expansion of the transmission system, system and generator impedances have changed considerably. System impedances have decreased while generator and step-up transformer impedances have increased. This trend has resulted in the impedance center during a power swing appearing inside the step-up transformer or inside the generator that is generally out of the protection zone of conventional out-of-step relays installed in the system. Therefore separate relaying should be applied to protect the machine against pole slipping.

Relays employing impedance-measuring elements for the detection of the pole slipping condition utilize the generator terminal voltage and current signals as inputs. During a generator pole slip the system voltage and current go through slip frequency variations of extremely high amplitude. These variations are reflective of the corresponding apparent changes in the generator terminal impedance. The relay will be able to detect the condition only after the generator has actually slipped poles. The conventional technique employs measurement of generator terminal impedance to determine pole slipping conditions. Directional and blinder elements are used together with a mho element to obtain the desired relay characteristics.

2.28.2 Loss of synchronism characteristics

Before any further discussion, it is necessary to have a brief review of the loss of synchronism characteristic that is used in the analysis of generator pole slipping.

A common method used to detect a loss of synchronism is to analyze the apparent impedance as measured at the generator terminals. According to the simplified representation of a machine and system shown in Figure 54, the impedance presented to the relay ZR (installed at point A) under a loss of synchronism (recoverable power swing or pole slipping) condition can be described by equation1:

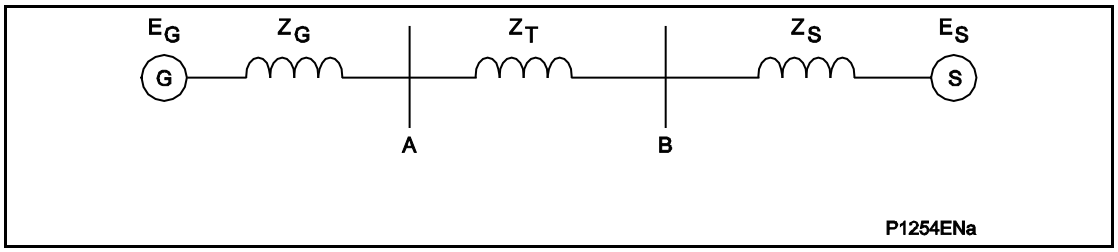


Figure 54: Simplified two machine system

Where:

EG = The generator terminal voltage

ZG = The generator impedance

ZT = The impedance of step-up transform

ZS = The impedance of the power system connected to the generation unit

ES = The system voltage

$$Z_R = \frac{(Z_G + Z_T + Z_S)\, n\, (n - \cos\delta - j \sin\delta)}{(n - \cos\delta)^2 + \sin^2 \delta} - Z_G$$ ---------- Equation 1

Where:

$n = \frac{E_G}{E_S}$ = magnitude ratio of generator terminal voltage to the system voltage

$\delta = \arg \frac{\dot{E}_G}{\dot{E}_S}$ = rotor angle by which generator terminal voltage leads system voltage

The apparent impedance as viewed at the generator terminals (Point A) will vary as a function of the ratio n and the angular separation δ between the machine and the system. With the aid of the R/X impedance diagram, a set of impedance loci representing a loss of synchronism along with the system impedances are plotted as shown in Figure 55.

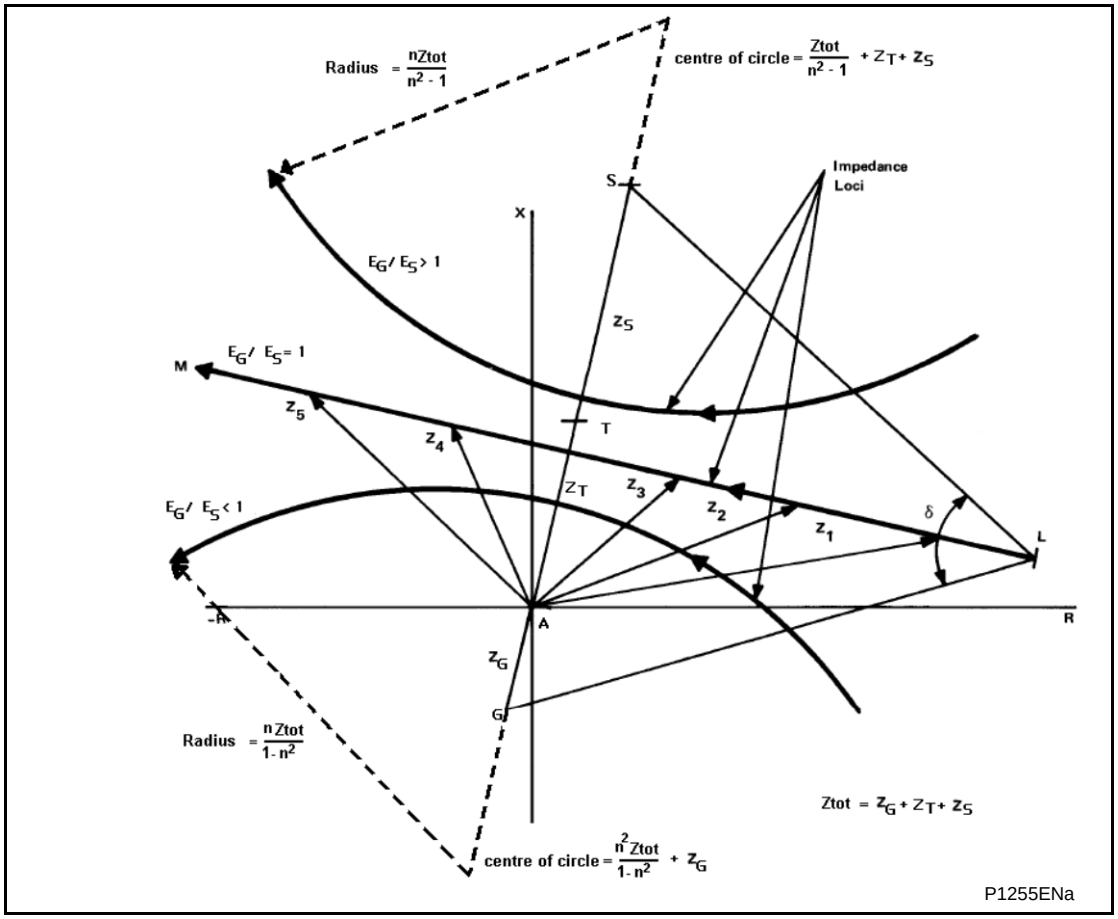


Figure 55: Apparent impedance loci viewed at the generator terminal (point A)

It has been well proven that the locus of the impedance as measured at the generator terminals (point A) is either a straight line or circular depending on whether E_G and E_S are of equal or different magnitudes. The impedance locus is a straight line which is a perpendicular bisector of the total system impedance between G and S when EG / ES = 1. When $E_G / E_S > 1$, the circular locus is located above the bisector with its center on the extension of the total impedance line GS. When $E_G / E_S < 1$, the impedance locus is situated below the bisector with its center on the extension of the total impedance line SG.

The diameters and centers of these circles are a function of the voltage ratio E_G / E_S and the total impedance, as shown in Figure 55. It is not always necessary to go into the detail of plotting the circular characteristic to identify the loss of synchronism. In most cases, it is only necessary to simply draw the perpendicular bisector to the total impedance line to locate the point on the system where the swing will traverse which is sufficiently accurate for relaying purposes.

The angle formed by the intersection of lines SL and GL on line ML is the angle of separation δ between the generator and system. During an unrecoverable power swing, δ oscillates between 0 and 360 degrees according to the points L and M on the bisector. There are several points of interest along line LM. The first is the point where the separation reaches 90 degrees. If we draw a circle whose diameter is the total impedance, line GS, the intersection of the circle and line LM will be the point where δ=90 degrees. If the swing locus does not go beyond this point the system will be able to regain synchronism. However, if the locus reaches 120 degrees or more, the system is not likely to recover. When the impedance locus intersects the total impedance, line GS, the generator and system are 180 degree out of phase, which is known as the electrical center or impedance center of the system. As the locus crosses this point and enters the left hand side of the line GS, the generator and system will become more in phase. A slip cycle has been completed when the locus reaches the point where the swing started.

Note: The following assumptions have been made in this simplified approach:

- E_G/E_S is assumed to remain constant during the swing
- Initial transients and effects of generator saliency are neglected
- Transient changes in impedance due to a fault or clearance of fault have subsided
- Effect of regulator and governor are neglected

2.28.3 Generator pole slipping characteristics

As noted previously, generator and system impedances have changed in the past few decades. In many instances, the electrical center or impedance center lies within the generator or step-up transformer. Also, for most machine loadings, the equivalent internal machine voltage will be less than 1.0 per unit and so less than the equivalent system voltage. Therefore the pole slipping characteristics viewed at the generator terminals will generally follow the loss of synchronism characteristic where the voltage ratio $E_G/E_S < 1$ which is below the impedance center. See the locus $E_G/E_S < 1$ in Figure 55 for example.

In reality the impedance loci as viewed at the generator terminals may be distorted compared with the ideal loci. The following discussion illustrates the impact on the pole slipping characteristic when other factors are taken into account.

2.28.3.1 What happens if EG/ES has different values less than one (1)?

For a given total impedance, as the voltage ratio decreases below one (1), the circle also decreases in diameter and the center moves closer to the origin. Therefore, a decreased internal voltage results in the impedance loci having a smaller diameter. The radius and circular center calculations using the equation shown in Figure 55 shows these trends.

During a fault, if the voltage regulator is out of service the internal machine voltage will decay and will remain at the resulting lower level after the fault is cleared. If the effects of the voltage regulator during a fault is included, the impedance locus circles are larger in diameter but will still be in the generator zone.

2.28.3.2 What happens if different system impedances are applied?

System impedance also plays a part in the determination of the circle diameter and location. If the system impedance decreases, the locus decreases in diameter and moves closer to the origin.

The impedance center of the system is not a fixed point due to the variation of system impedance under different operating conditions. Therefore the impedance loci should be determined at the maximum and minimum systems impedances.

2.28.3.3 How to determine the generator reactance during a pole slipping condition?

Since the generator reactance plays a role in the determination of the pole slipping impedance locus, it is crucial to use proper reactance values when we plot these loci. At zero slip X_G is equal to the synchronous reactance (Xd), and at 100% slip X_G is equal to sub-transient reactance (X''_d). The impedance in a typical case has been shown to be equal to

the transient reactance X'_d at 50% slip, and to $2X'_d$ with a slip of 0.33%. As most slips are likely to be experienced at low asynchronous speed running, perhaps 1%, it is sufficient to take the value $X_G=2X'_d$ when assessing pole slipping.

2.28.3.4 How to determine the slip rate of pole slipping

The rate of slip between the generator and power system is a function of the accelerating torque and inertia of the systems. In general, the slip rate can not be obtained analytically. It is recommended to determine the slip rate by transient stability studies where the angular excursion of the system is plotted versus time. Although the slip rate will not be constant during a pole slipping condition, it is reasonable to assume a constant for the first half slip cycle which is of interest to the relay. For the tandem generator, it is in the range of 250 to 400 degrees/sec. For the cross compound units, the average initial slip will be 400 to 800 degrees/sec.

2.28.4 General requirements for pole slipping protection

Having got some ideas about the characteristics of pole slipping, general rules for pole slipping protection could be obtained as listed below:

- On the whole, the pole slipping protection must remain stable under all fault conditions and recoverable power swings other than a genuine non-recoverable pole slipping condition.
- For a particular loss of synchronism condition, if the impedance center happens to lie in the generator/step-up transformer zone, it is recommended the generator be tripped without delay, preferably during the first half slip cycle of a loss of synchronism condition. If the center lies outside of the zone, then the pole slipping relay should not trip immediately, but should allow time for tripping to take place at some other location external to the power station. Only if this should fail must the pole slipping protection respond in stage II, i.e. after a pre-set number of slips, to isolate the generator.
- To reduce the damage to the generator during a pole slip, it must reliably detect the first and subsequent slips of a synchronous machine within a wide range (slipping frequency 0.1% to 10% of fn).
- The tripping should avoid the point where the generator and the system are 180 degrees out-of-phase, when the currents reach the maximum value and subject the circuit breaker to a maximum recovery voltage during interruption.
- Since pole slipping is essentially a balanced three-phase phenomenon, only a single-phase element need be implemented in the protection relay.

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2.28.5 Lenticular scheme

2.28.5.1 Characteristic

The P343/4/5/6 pole slipping characteristic consists of three parts as shown in the R/X diagram of Figure 56. The first part is the lenticular (lens) characteristic. The second is a straight line referred to as the blinder that bisects the lens and divides the impedance plane into the left and right halves. The third is a reactance line which is perpendicular to the blinder.

The inclination of the lens and the blinder, θ, is determined by the angle of the total system impedance. The equivalent impedance of the system and the step-up transformer determines the forward reach of the lens, Z_A, whereas the generator's transient reactance determines the reverse reach Z_B. The width of the lens is varied by the setting of the angle α. A reactance line, perpendicular to the axis of the lens, is used to distinguish whether the impedance center of the swing is located in the power system or in the generator. It is set by the value of Zc along the axis of the lens, as shown in Figure 56. The reactance line splits the lens into Zone 1 (lens below the line) and Zone 2 (all of the lens).

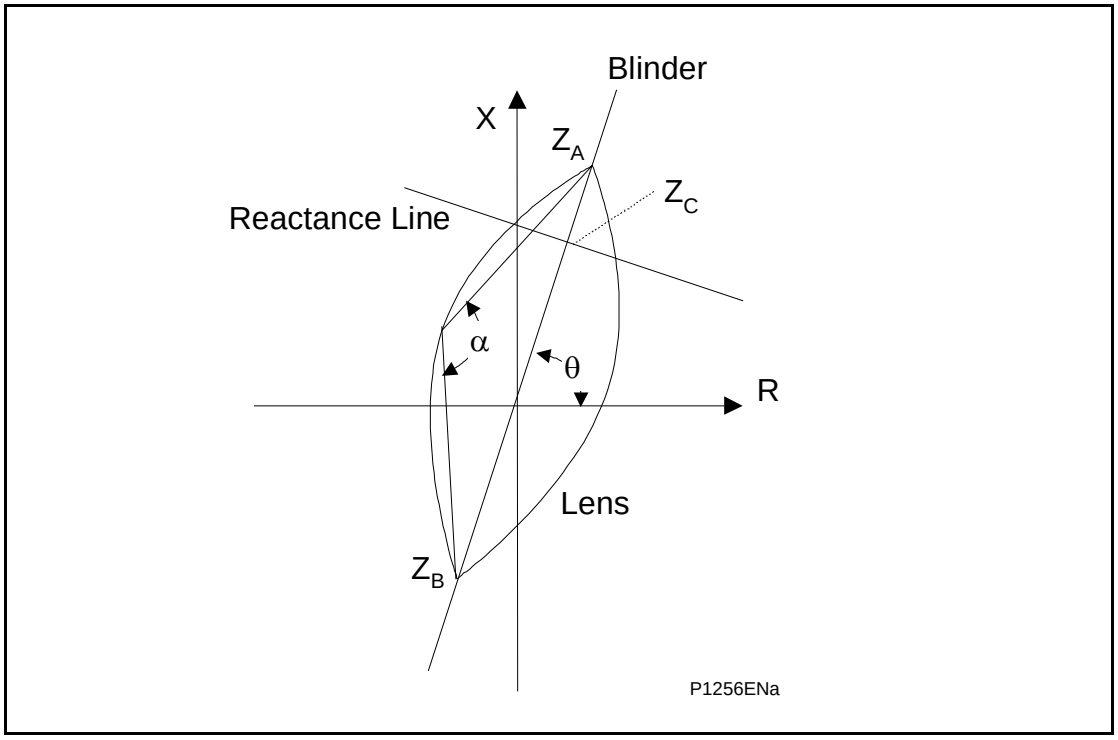


Figure 56: Pole slipping protection using blinder and lenticular characteristic

2.28.5.2 Generating and motoring modes

When a generator is out of step with the system, the impedance locus is expected to traverse from right to left across the lens and the blinder. However, if the generator is running as a motor, as in the pumping mode of a pump storage generator, the impedance locus is expected to swing from the left to the right. A setting is provided to determine whether the protection operates in a generating mode or in a motoring mode or both. Also, when a generator is running at low load, <30% load, due to the presence of heavy system damping during a fault the generator can slow down and result in a motor like slip (negative slip). To detect pole slips for this condition then the **Pole slip mode** should be set to **Both**.

If the protection is running in the generating mode, the impedance is expected to be at the right hand side of the lens under normal load conditions. During a pole slip the impedance locus traverses across the right half and the left half of the lens. The minimum time spent in each half of the lens can be set with timers T1 for the right hand side and T2 for the left hand side. The relay registers a pole slipping cycle when the locus finally leaves the lens at the opposite end.

If the protection is running in the motoring mode, the impedance is expected to be at the left hand side of the lens under normal load conditions. During a pole slip the impedance locus traverses across the left half and the right half of the lens, again spending at least the time T1 and T2 respectively in each half and leaves the lens at the opposite end.

2.28.6 Setting guidelines for pole slipping protection

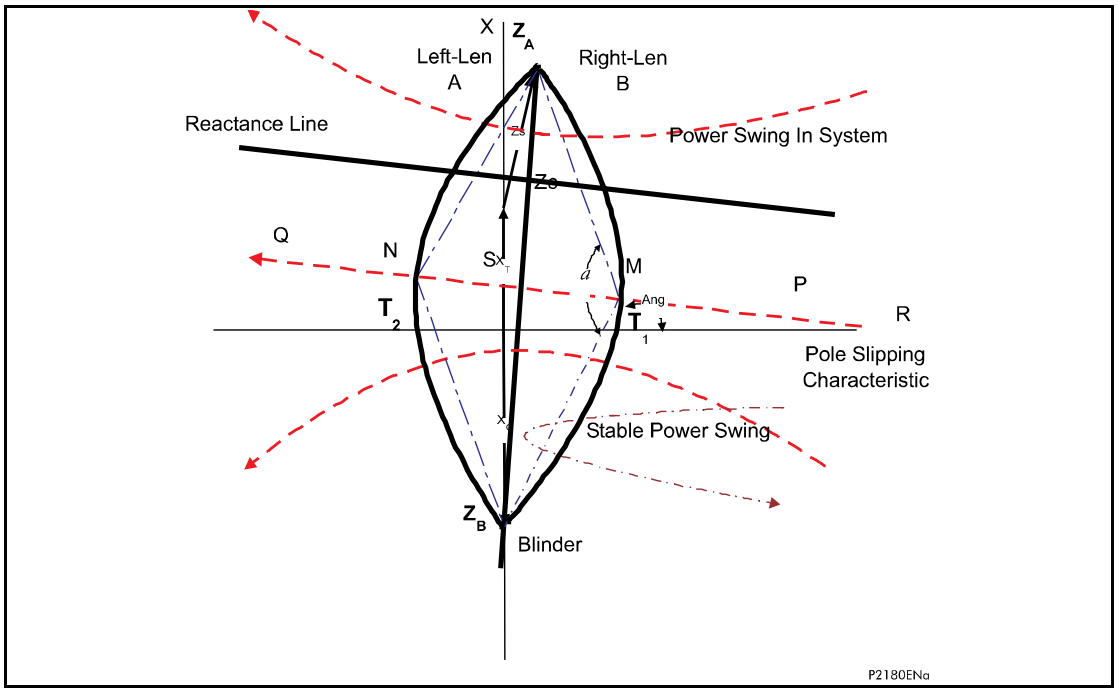


Figure 57: Lenticular scheme characteristic

1. Forward reach and reverse reach Z_A, Z_B.

As noted previously, the best setting for the lens is when the point ZA and ZB coincide with the system impedance (ZT+ZS) and the generator reactance (XG), see Figure 57. The angle α of the lens corresponds in this case to the angle α between the emfs EG and ES at which the impedance enters the lens, see Figure 57.

As most slips are likely to be experienced at low asynchronous speed running, perhaps 1%, it is sufficient to take the value XG=2X'd when assessing pole slipping, see section 2.28.3.3.

Where the values of ZS and the generator reactance XG vary, ZA and ZB should be set according to the corresponding maximum values.

Large differences between EG and ES, see Figure 57 and sections 2.28.3.1, can cause the loci of impedance circle to becomes smaller and smaller. Therefore there is the possibility of the circular loci of the pole slip crossing the blinder and lens twice with large ZA and ZB settings producing a long lens. However, the state machine logic will prevent 2 pole slips from being counted for this condition and so there is no maximum limit to the ZA and ZB settings.

2. Lens inclination θ

The inclination of the lens should be kept consistent with the system impedance angle, vector GS in Figure 57.

3. angle α.

The width of the lens is proportional to the angle α. Two factors should be considered to determine the proper angle α:

- Under all conditions, the load impedance remains safely outside the lens.
- The tripping point, limited by the left side of the lens for generating should be the point when the angular separation between the system and the generator is small. Although CBs are rated to break twice the system voltage i.e. when the machines are in anti-phase, it is recommended that the trip command is issued at the smallest phase shift possible. For this reason the angle α should be chosen as small as possible (setting range is 90° to 150°).

The construction of the lens can be seen in Figure 58, ZR is the maximum width of half the lens. The minimum resistive component of the load should be at least 130% of the reach of the lens, ZR, in the transverse direction. ZR can be determined by calculation as follows:

ZR = (ZA + ZB) /2 x tan (90° - α/2)

For a given minimal load resistance RLmin the minimum permissible setting of α is:

αmin = 180° – 2 x tan-1 (1.54 x RLmin / (ZA + ZB))

RLmin is then at least 1.3 ZR

Note: The minimum relay setting for α is 90° as this defines the largest size of the characteristic, a circle.

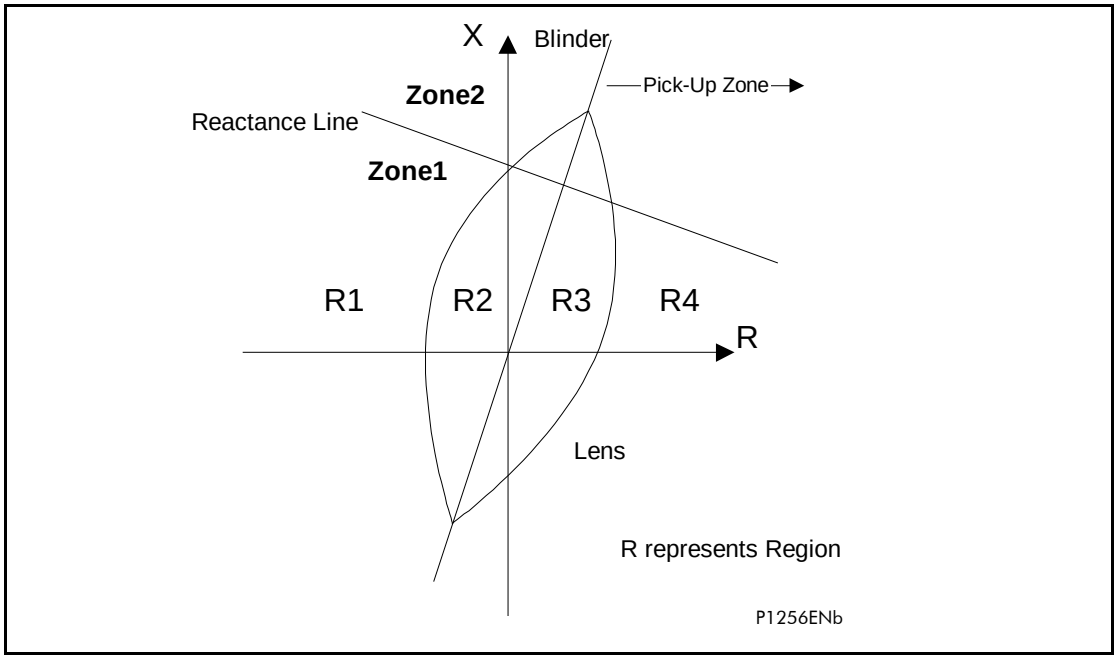


Figure 58: Pole slipping protection using blinder and lenticular characteristic

4. Reactance setting

The value of Zc

The value of Zc determines the distance of the reactance line from the origin. The reactance line provides a means of discrimination of the pole slipping within the generator or power swing within the HV power system. It should be set to encompass the step-up transformer and generator reactance with sufficient margin.

5. Pole slipping counters

Counters are available for both Zone1 and Zone2 to count the number of pole slip cycles before the trip signal is issued. A user-settable reset timer is available to reset the counters when the pole slipping condition is cleared by other relays in the system.

6. Timers T1 and T2

During a pole slip the impedance locus traverses across the lens spending at least time T1 in region 2 and time T2 in region 3, see Figure 58. From simulation testing it has been proved that pole slips up to 10 Hz can be detected with an angle α setting of 120° and time settings of 15 ms for T1 and T2. Therefore, it is recommended that T1 and T2 be set to 15 ms.

7. Reset timer

The reset time should be set longer than the maximum expected time for the machine to go through the set number of pole slips for zone1 or zone2. The reset time is required to reset the counters for pole slips that are cleared by external protection. For example if the Z2 counter is set to operate after 2 pole slips in the power system and after a count of 1 the condition is cleared by other protection in the system the counters will need to be reset to zero.

8. Pole slip mode

When a generator is out of step with the system, the impedance locus is expected to traverse from right to left across the lens and the blinder. However, if the generator is running as a motor, as in the pumping mode of a pump storage generator, the impedance locus is expected to swing from the left to the right. A pole slip mode setting is provided to determine whether the protection operates in a **generating** mode or in a **motoring** mode or **both**.

For a pump storage generator, its operation can switch from generating mode to motoring mode and vice versa. Therefore, a facility is provided for the protection to detect the normal running mode of the machine, generating or motoring and to perform pole slipping detection in either mode. This facility is enabled when the pole slip mode setting is set to both.

Also, when a generator is running at low load, <30% load, due to the presence of heavy system damping during a fault the generator can slow down and result in a motor like slip (negative slip). To detect pole slips for low load and normal load conditions then the pole slip mode should be set to **both**.

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2.28.6.1 Pole slipping setting examples

The impedances in the P343/4/5/6 can be set in terms of primary or secondary quantities, however, for simplicity all the impedance values used in the examples are in primary quantities.

2.28.6.2 Example calculation

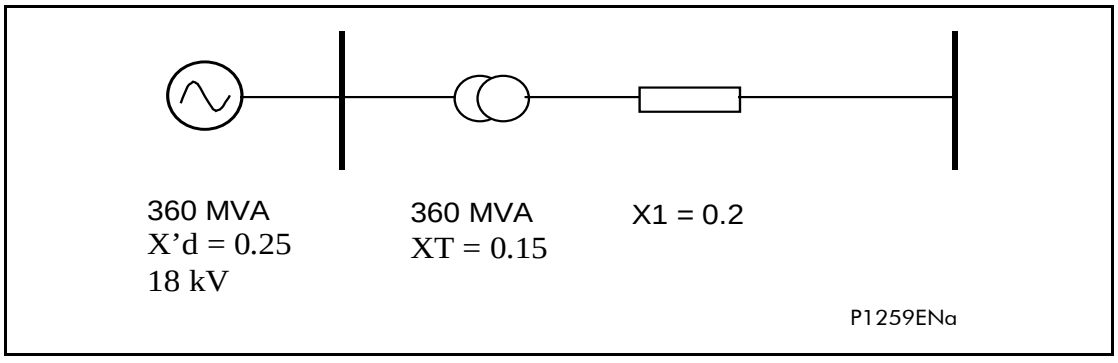


Figure 59: Example system configuration

Data of the generator and step up transformer:

Base power	Pn	=	360 MVA
Base voltage	Vn	=	18000 kV
Min. load resistance	RLmin	=	0.77 Ω
System impedance angle	≥ 80°		
Generator impedance	0.25 pu		
Transformer impedance	0.15 pu		
System impedance	0.2 pu		

The location of the pole slipping relay is at the generator terminals. The direction of ZA and Zc is towards the step up transformer and the rest of the system. The reactance line is required to distinguish between power swings with electrical centers within the generator/transformer zone and those outside.

The base impedance is:

Zbase = Vn2/Pn = 182/360 = 0.9 Ω

ZA = (XT + X1) Zbase = (0.15+0.2) x 0.9 = 0.315 Ω

ZB = 2X'd x Zbase = 2 x 0.25 x 0.9 = 0.45 Ω

Zc is set to 90% of the transformer reactance

Zc = 0.9 x (XT) Zbase = 0.9 x 0.15 x 0.9 = 0.122 Ω

The minimum suitable angle α which defines the lens limit in relation to the minimum load resistance is:

αmin = 180° – 2 x tan-1 (1.54 x RLmin / (ZA + ZB))

αmin = 180° – 2 x tan-1 (1.54 x 0.77 / (0.315 + 0.45))

αmin = 65.7°

The minimum setting for α on the relay is 90° so this is the setting used.

T1 and T2 are set to 15 ms and θ is set to the system impedance angle of 80°.

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2.29 P34x pole slipping protection equivalent to TP2xx (78)

The TP2xx relay, which is now obsolete, included 2 methods for pole slipping (desynchronisation) protection:

(1) Detection of an excessive internal phase angle

(2) Feedback of active power

These methods are described below.

2.29.1 TP2 detection of an excessive internal phase angle

The internal phase angle is the phase difference between the line voltage and the EMF. The EMF phase can be measured by a sensor triggered by a component mounted on the shaft. Alternatively, a phase alternator can be used. A counting pulse is generated if the internal angle exceeds two thresholds, located at 180°, in the same direction of variation.

2.29.2 TP2 feedback of active power

Active power is measured (single-phase or three-phase). The average value of the active power is compared to two thresholds, one positive (2-20%Pn, 2% steps) and one negative (-2 to -20%Pn, 2% steps). These two thresholds define a dead band.

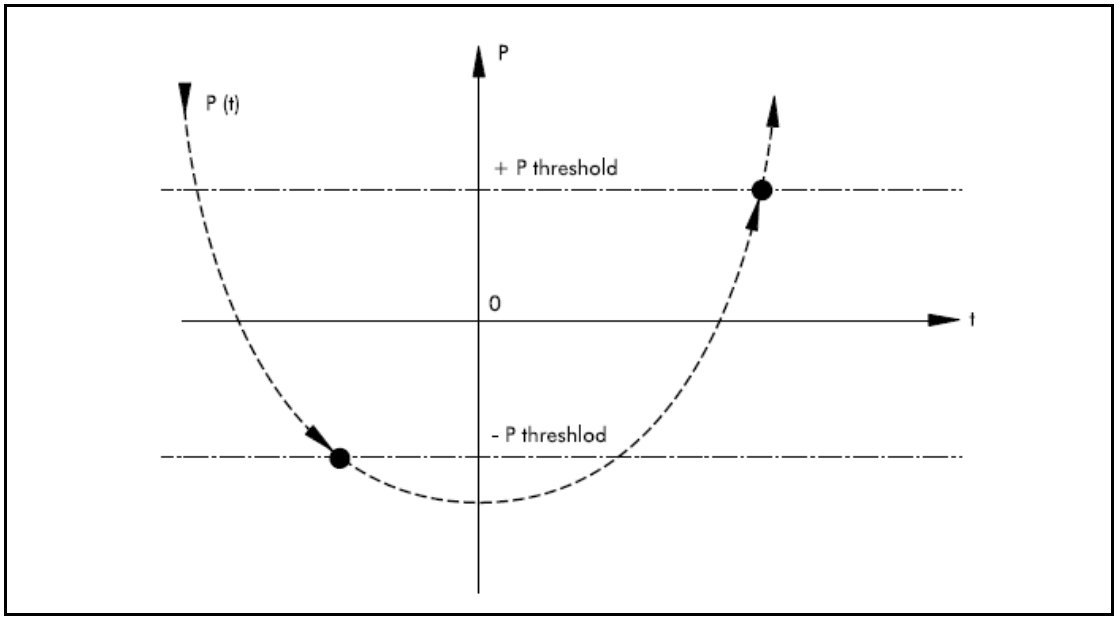


Figure 60: Active power logic

A counter pulse is transmitted whenever power (which is positive when synchronised) moves outside the dead band, as shown on the figure above.

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2.29.3 TP2 counting logic

The pulses generated by the power and internal angle channels are fed to two Counters (Internal angle channel: 2, 4, 6, 12, 20, 30 and Power channel: 2, 4, 6, 12, 20, 30). A number of pulses are selected for each counter. The first pulse output by either channel starts a timer T1 (T1 = 1, 2, 3, 4 or 5 min). If either of the counters reaches its threshold, it locks the other counter at its current value and generates a signal output command. If the count threshold is not reached before T1 elapses, both counters are reset at the end of T1.

2.29.4 P34x pole slipping protection logic based on phase angle

There are two methods to initiate the pole slipping based on angle measurement. One method is via a digital input from an external phase angle measurement device which provides an output contact when a set phase angle difference between the rotor and stator (eg 150 o) is exceeded. The other method uses the check synch voltage input and function to measure the EMF phase angle difference from a shaft mounted alternator and the 3 phase generator stator voltage.

Two stages of angle based pole slipping can be used for alarm and tripping using the PSL as described below. A typical setting for the alarm and trip angle settings are 120° and 150°. A typical setting range for the counter is 1-10 and the counting window is 10s-120s. The typical range for the interval time between 2 angle rotations is 100-600ms.

2.29.4.1 Excessive internal phase angle using a digital input method

A P34x digital input with PSL counters and timing logic can be configured using PSL to provide a 1 or 2 stage pole slipping protection for alarm and/or trip stages equivalent to the TP2xx pole slipping excessive internal phase angle method.

The PSL logic is shown in Figure 61. The logic is described below.

1. A counter pulse is transmitted via an external device output contact to energise a digital input (Input 1) when the phase angle is greater than a set threshold.
2. The Inhibit signal can be from a digital input, e.g. Input 2 in the PSL example.

3. Counter1 is used to count the pulses for the alarm. It will operate the alarm signal (DDB405 PSlip Angle Alm) if the counter value is equal or greater than the threshold. It is reset by the inhibit signal, Timer1 and Timer2. The PSlip Angle Alm (DDB405) signal triggers an alarm message in the fault record and triggers the DDB 761, PSlip Ang Alm In, which can be used to operate an output contact.
4. Counter2 is used to count the pulses for the trip. It will operate the trip signal (DDB753 PSlip Angle Trip) if the counter value is equal or greater than the threshold. It is reset by the inhibit signal, Timer1 and Timer2. The PSlip Angle Trip (DDB753) signal triggers an alarm message in the fault record and triggers the DDB 757, PSlip Angle In, which can be used to operate an output contact.
5. Timer1 is the combination of the Pulse timer (T1) and Drop-off timer (T2). It is used for the interval time between two count pulses. The Counter1/2 is reset if the interval time between two pulses exceed Timer 1 (Timer 1 = T1 Pulse setting + T2 Drop-off setting).
6. Timer2 (T3) is the counting window. It is initiated by the first pulse. The Counter1/2 will reset if Timer2 expires.
7. Set-Reset gate, SR1 is to latch the first pulse signal to start the Timer2. It is reset by the inhibit signal, Timer1 and Timer2.

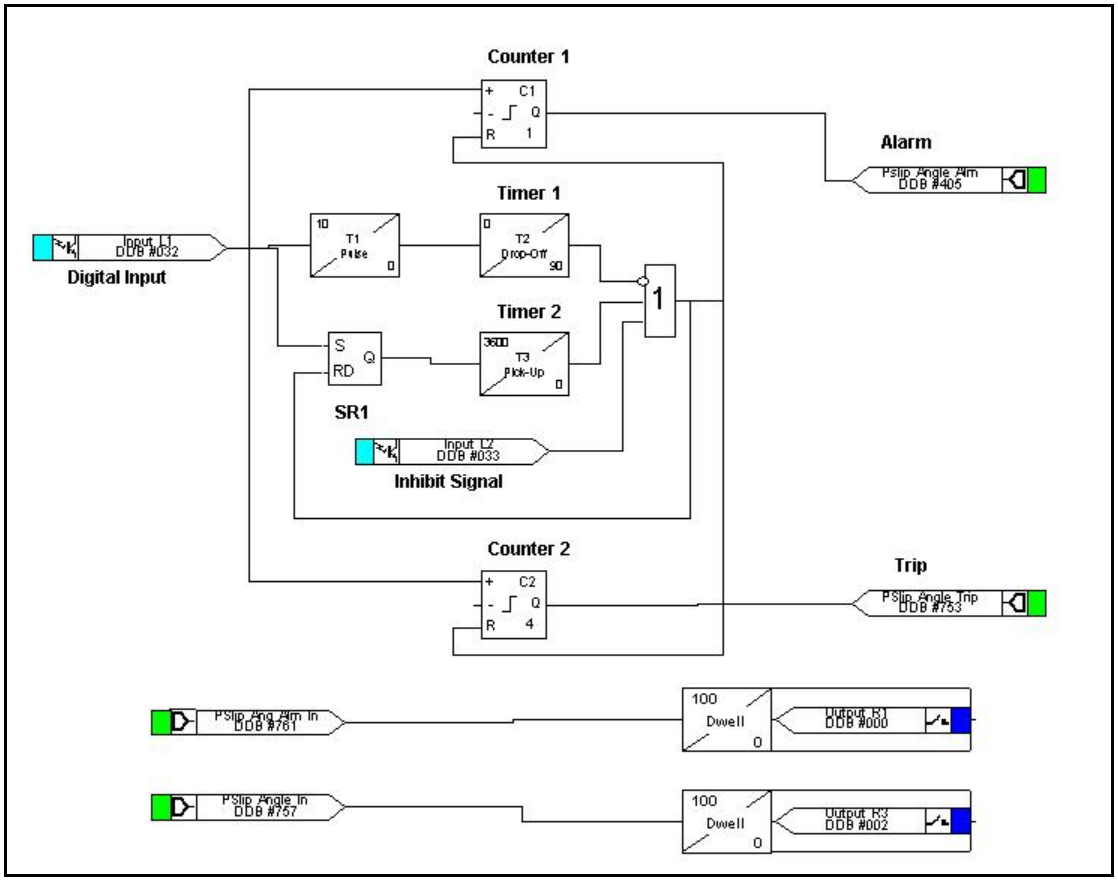


Figure 61: Pole slipping with digital input method logic

2.29.4.2 Excessive internal phase angle using a check synchronising element method

The P34x check synchronizing/system split signals with PSL counters and timing logic can be configured using PSL to provide a 1 or 2 stage pole slipping protection for alarm and/or trip stages equivalent to the TP2xx pole slipping excessive internal phase angle method.

The PSL logic is shown in Figure 62. The logic is described below and is similar to the digital input method except for the start signal.

Note: It is not feasible to use the Check Synch 2 element (CS2 Phase Angle setting, 5 - 90°) in this scheme.

- The system split alarm signal (DDB 404) is used as the trigger signal for the alarm stage. (SS Phase Angle setting, 90-175°).
- The 'CS1 Ang Not OK +' (DDB 1353) and 'CS1 Ang Not OK -' (DDB 1354) with an OR gate and Drop Off timer are used as the trigger signal for the trip stage. The Drop-off timer ensures a smooth transition between the drop-off and pick-up of the CS1 Ang Not OK + and CS1 Ang Not OK - signals and so prevents wrong counting. (CS1 Phase Angle setting, 5 -175°)
- The function of other timer and counter components is the same as described above for the digital input method.

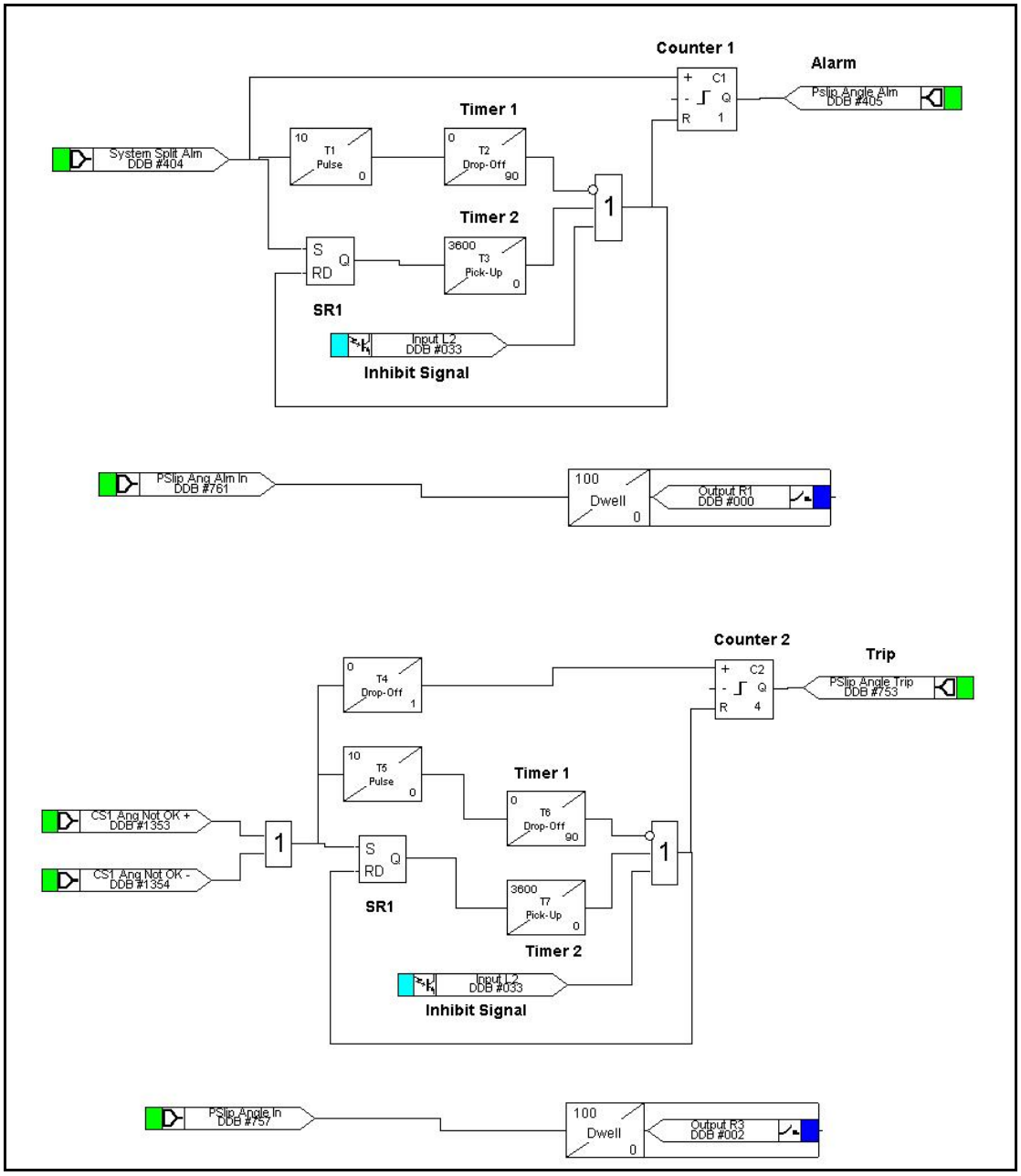


Figure 62: Pole slipping with check synch method logic

2.29.5 P34x pole slipping protection logic based on active power

The P34x power protection with PSL counters and timing logic can be configured using PSL to provide a 1 or 2 stage pole slipping protection for alarm and/or trip stages equivalent to the TP2xx pole slipping active power method.

Two power or sensitive power protection stages are used to create the power band. The example PSL below uses the sensitive power protection. The reverse and forward power setting ranges for this application are typically, 0.02 to 0.2Pn. A typical setting is 10%Pn.

A typical setting range for the counter is 2-20 and the counting window is 10s-120s. The typical range for the interval time between successive crossings of the power thresholds is 20-200ms and between two power reversals 50-500ms.

The PSL logic is shown in Figure 63. The logic is described below.

- +P Trip is the output DDB of the sensitive power trip signal, SPower1 Trip (DDB884) set to operate in the Forward direction and for Over operation. The time delay should be set to 0 for this application. The sensitive power protection start signals could also be used.
- -P Trip is the output DDB of the sensitive power trip signal, SPower2 Trip (DDB885) set to operate in the Reverse direction and for Over operation. The time delay should be set to 0 for this application. The sensitive power start signals could also be used.
- The counter is triggered when the power moves outside the –P threshold and then outside the +P threshold.
- The Inhibit signal can be from a digital input, e.g. Input 2 in the PSL example.
- Counter1 is used to count the pulses for the alarm. It will operate the alarm signal (DDB406 PSlip Power Alm) if the counter value is equal or greater than the threshold. It is reset by the inhibit signal, Timer1 and Timer2. The PSlip Power Alm (DDB406) triggers an alarm message in the fault record and triggers the DDB 762, PSlip Pow Alm In, which can be used to trigger an output contact.
- Counter2 is used to count the pulses for the trip. It will operate the trip signal (DDB754 PSlip Power Trip) if the counter value is equal or greater than the threshold. It is reset by the inhibit signal, Timer1 and Timer2. The PSlip Power Trip (DDB754) triggers an alarm message in the fault record and triggers the DDB 758, PSlip Power In, which can be used to trigger an output contact.
- Timer1 is the combination of the Pulse timer (T1) and Drop-off timer (T3) and is initiated by the –P Trip. It is used to detect the interval time between two –P Trip signals. The Counter1/2 is reset if the interval between two pulses exceeds Timer1 (Timer 1 = Pulse setting (T1) + Drop-off setting (T3)).
- Timer2 (T4) is the counting window. It is initiated by the first –P Trip. The Counter1/2 is reset if the counter value does not reach the threshold in time Timer2.
- Timer3 is the combination of the Pulse timer (T1) and Drop-off timer (T2) and is initiated by the –P Trip. It is used to detect the interval time between successive crossing of -P thresholds and +P thresholds.
- Set-Reset gate, SR1 is to latch the first –P Trip signal to start the Timer2. It is reset by the inhibit signal, Timer1 and Timer2.

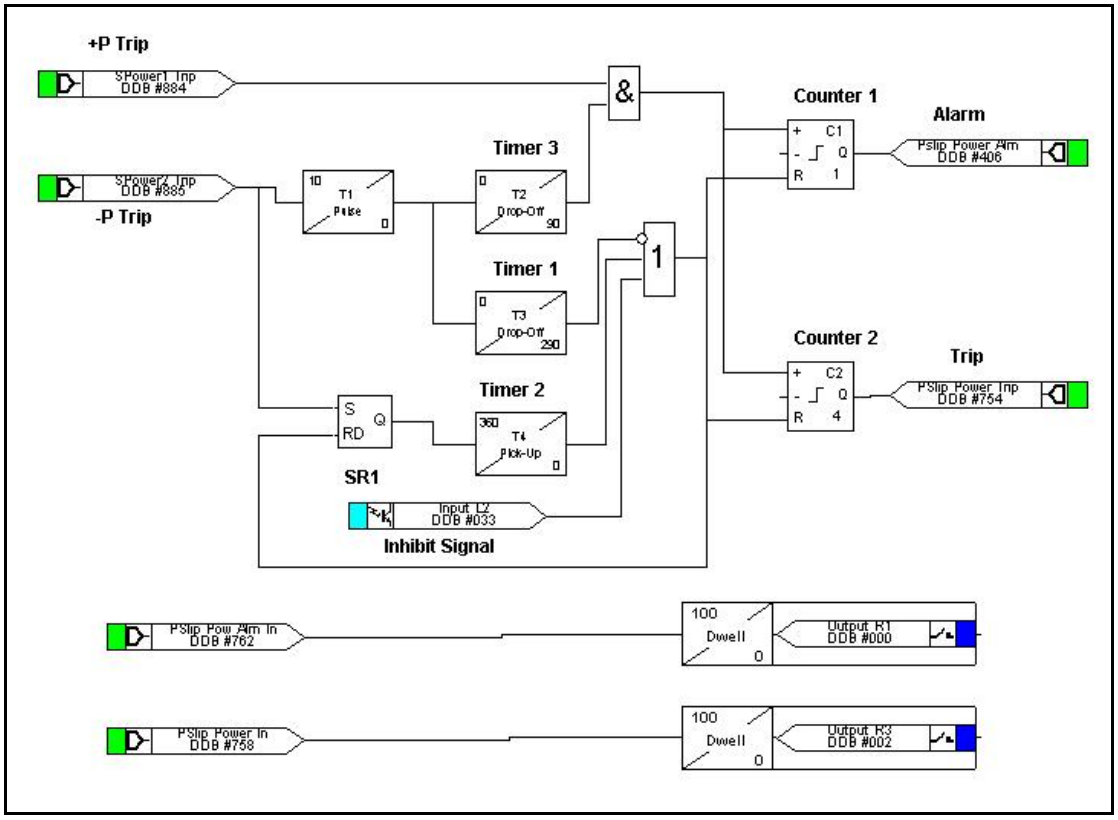


Figure 63: Active power pole slipping logic

2.30 Generator Thermal overload protection (49G)

2.30.1 Introduction

Overloads can result in stator temperature rises which exceed the thermal limit of the winding insulation. Empirical results suggest that the life of insulation is approximately halved for each 10°C rise in temperature above the rated value. However, the life of insulation is not wholly dependent on the rise in temperature but on the time the insulation is maintained at this elevated temperature. Due to the relatively large heat storage capacity of an electrical machine, infrequent overloads of short duration may not damage the machine. However, sustained overloads of a few percent may result in premature ageing and failure of insulation.

The physical and electrical complexity of generator construction result in a complex thermal relationship. It is not possible to create an accurate mathematical model of the true thermal characteristics of the machine.

However, if a generator is considered to be a homogeneous body, developing heat internally at a constant rate and dissipating heat at a rate directly proportional to its temperature rise, it can be shown that the temperature at any instant is given by a time-current thermal replica charactertic.

As previously stated it is an oversimplification to regard a generator as an homogeneous body. The temperature rise of different parts or even of various points in the same part may be very uneven. However, it is reasonable to consider that the current-time relationship follows an inverse characteristic. A more accurate representation of the thermal state of the machine can be obtained through the use of temperature monitoring devices (RTDs) which target specific areas. Also, for short time overloads the application of RTDs and overcurrent protection can provide better protection. The thermal model does not compensate for the effects of ambient temperature change. So if there is an unusually high ambient temperature or if the machine cooling is blocked RTDs will also provide better protection.

2.30.2 Generator Thermal replica

The P342/3/4/5/6 relay models the time-current thermal characteristic of a generator by internally generating a thermal replica of the machine.

The positive and negative sequence components of the generator current are measured independently and are combined together to form an equivalent current, I_{eq}, which is supplied to the replica circuit. The heating effect in the thermal replica is produced by $I_{eq}2$ and therefore takes into account the heating effect due to both positive and negative sequence components of current.

Unbalanced phase currents will cause additional rotor heating that may not be accounted for by some thermal protection relays based on the measured current only. Unbalanced loading results in the flow of positive and negative sequence current components. Load unbalance can arise as a result of single-phase loading, non-linear loads (involving power electronics or arc furnaces, etc.), uncleared or repetitive asymmetric faults, fuse operation, single-pole tripping and reclosing on transmission systems, broken overhead line conductors and asymmetric failures of switching devices. Any negative phase sequence component of stator current will set up a reverse-rotating component of stator flux that passes the rotor at twice synchronous speed. Such a flux component will induce double frequency eddy currents in the rotor, which can cause overheating of the rotor body, main rotor windings, damper windings etc. This extra heating is not accounted for in the thermal limit curves supplied by the generator manufacturer as these curves assume positive sequence currents only that come from a perfectly balanced supply and generator design. The P34x generator thermal model may be biased to reflect the additional heating that is caused by negative sequence current when the machine is running. This biasing is done by creating an equivalent heating current rather than simply using the phase current. The M factor is a constant that relates negative sequence rotor resistance to positive sequence rotor resistance. If an M factor of 0 is used the unbalance biasing is disabled and the overload curve will time out against the measured generator positive sequence current. Note, the P34x also includes a negative sequence overcurrent protection function based on I_2^2t specifically for thermal protection of the rotor.

The equivalent current for operation of the overload protection is in accordance with the following expression:

$$I_{eq} = \sqrt{(I_1^2 + MI_2^2)}$$

Where:

I1 = Positive sequence current

I2 = Negative sequence current

M = A user settable constant proportional to the thermal capacity of the machine

As previously described, the temperature of a generator will rise exponentially with increasing current. Similarly, when the current decreases, the temperature also decreases in a similar manner. Therefore, in order to achieve close sustained overload protection, the P342/3/4/5/6 relay incorporates a wide range of thermal time constants for heating and cooling.

Furthermore, the thermal withstand capability of the generator is affected by heating in the winding prior to the overload. The thermal replica is designed to take account the extremes of zero pre-fault current, known as the ‘cold’ condition and the full rated pre-fault current, known as the ‘hot’ condition. With no pre-fault current the relay will be operating on the ‘cold curve’. When a generator is or has been running at full load prior to an overload the ‘hot curve’ is applicable. Therefore, during normal operation the relay will be operating between these two limits.

2.30.3 Setting guidelines

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the plant item/CT ratio.

The heating thermal time constant should be chosen so that the overload curve is always below the thermal limits provided by the manufacturer. This will ensure that the machine is tripped before the thermal limit is reached.

The relay setting, **T-heating**, is in minutes.

The cooling thermal time constant should be provided by the manufacturer. However, unless otherwise specified, the cooling time constant, **T-cooling**, setting should be set equal to the main heating time constant setting, **T-heating**. The cooling time constant is applied when the machine is running and the load current is decreasing. It is therefore practical to assume the cooling time constant is similar to the heating time constant if information is not available from the manufacturer. When the machine is not turning the machine will normally cool significantly slower than when the rotor is turning. The relay setting, **T-cooling**, is in minutes.

An alarm can be raised on reaching a thermal state corresponding to a percentage of the trip threshold. A typical setting might be **Thermal Alarm** = 70% of thermal capacity. The thermal alarm could also be used to prevent restarting of the generator until the alarm level resets. For this application a typical setting may be 20%.

The **M Factor** is used to increase the influence of negative sequence current on the thermal replica protection due to unbalanced currents. If it is required to account for the heating effect of unbalanced currents then this factor should be set equal to the ratio of negative phase sequence rotor resistance to positive sequence rotor resistance at rated speed. When an exact setting can not be calculated a setting of 3 should be used. This is a typical setting and will suffice for the majority of applications. If an M factor of 0 is used the unbalance biasing is disabled and the overload curve will time out against the measured generator positive sequence current.

Note: The extra heating caused by unbalanced phase currents is not accounted for in the thermal limit curves supplied by the generator manufacturer as these curves assume positive sequence currents only that come from a perfectly balanced supply and generator design, so the default setting is 0.

2.31 Transformer Thermal overload protection (49T)

Transformer overheating can be caused due to failures of the cooling system, external faults that are not cleared promptly, overload and abnormal system conditions. These abnormal conditions include low frequency, high voltage, non-sinusoidal load current, or phase-voltage unbalance.

Overheating shortens the life of the transformer insulation in proportion to the duration and magnitude of the high temperature. Overheating can generate gases that could result in electrical failure. Furthermore, excessive temperature may result in an immediate insulation failure. Also, the transformer coolant may be heated above its flash temperature, therefore a fire can be caused.

Results suggest that the life of insulation is approximately halved for each 10°C rise in temperature above the rated value. However, the life of insulation is not wholly dependent on the rise in temperature but on the time the insulation is maintained at this elevated temperature. Due to the relatively large heat storage capacity of a transformer, infrequent overloads of short duration may not damage it. However, sustained overloads of a few percent may result in premature ageing and failure of insulation.

The thermal overload protection in the P34x is based on IEEE Standard C57.91-1995. Thermal overload trip can be based on hot spot temperature, Θ_H, or top oil temperature, Θ_{TO}. Top oil temperature can be calculated or can be measured directly when either CLIO or RTD are available. Hot spot temperature is only calculated.

It is important to consider ambient temperature to determine the load capability of a transformer. The ambient temperature is the temperature of the air in contact with the transformer's radiators. To determine the operating temperature, the temperature rise due to load is added to the ambient temperature. IEEE Standard C57.91-1995 states that transformer ratings are based on 24 hour average ambient temperature of 30°C. If the ambient temperature can be measured, then it should be averaged over a 24 hour period. In

the P34x relays, the ambient temperature, Θ_A, can be measured directly or an average value can be set by the user.

The simplest application of overload protection employs I^2t characteristic. Time constants such as the winding time constant at hot spot location, τ_W, and top oil rise time constant, τ_{TO}, are set, so that the thermal model can follow the correct exponential heating and cooling profile, replicating the winding hotspot temperature. Transformer loads are becoming increasingly non-linear; hence, the P34x uses rms current values to replicate the winding hotspot temperature.

2.31.1 Setting guidelines

The following tables are examples of the thermal data given by the transformer manufacturer. This data is required to set the thermal overload function.

Thermal characteristic 735 MVA 300 kV +7% to -18% / 23 kV ODWF cooled generator transformer	
No load losses (core losses)	340 kW
Load losses at nominal tap	1580 kW
Load losses at maximum current tap	1963 kW
Oil time constant	2.15 hr
Oil exponent	1.0
Top oil rise over ambient temperature at rated load	33.4 K
Winding time constant at hot spot location	14 mins
Winding hottest spot rise over top oil temperature at rated load	30.2 K
Winding exponent	2.0

Table 10: Thermal characteristic MVA 300 kV +7% to -18% / 23 kV ODWF cooled generator transformer

Note: OD (oil directed) indicates that oil from heat exchangers (radiators) is forced to flow through the windings. WF states that the oil is externally cooled by pumped water.

Thermal characteristic 600 MVA 432/23.5 kV ODWF cooled generator transformer	
No load losses (core losses)	237 kW
Load losses at nominal tap	1423 kW
Load losses at maximum current tap	1676 kW
Oil time constant	2.2 hr
Oil exponent	1.0
Top oil rise over ambient temperature at rated load	46.6 K
Winding time constant at hot spot location	9 mins
Winding hottest spot rise over top oil temperature at rated load	33.1K
Winding exponent	2.0

Table 11: Thermal characteristic 600 MVA 432/23.5 kV ODWF cooled generator transformer

Thermal characteristic IEC 60354 figures based on medium-large power transformers OD cooled	
Oil time constant	1.5 hr
Oil exponent	1.0
Top oil rise over ambient temperature at rated load	49 K
Winding time constant at hot spot location	5-10 mins
Winding hottest spot rise over top oil temperature at rated load	29 K
Winding exponent	2.0

Table 12: Thermal characteristic IEC 60354 figures based on medium-large power transformers OD cooled

The monitor winding can be set either to HV, LV, or biased current. It is recommended to set it to biased current so an overall thermal condition of the transformer is provided. The ambient temperature can be set to average (average ambient temperatures covers 24 hour time periods), or it can be measured directly using a CLI or RTD input. Top oil temperature may be set as calculated or measured. IB is the load in pu, and it is recommended to set it at rated load, of 1.0 pu. The following parameters should be provided by the transformer manufacturer:

- The ratio of load loss at rated load to no load loss (Rated NoLoadLoss). For example, if the no load losses are 340 kW and load losses at rated are 1580 kW, the rated NoLoadLoss is 1580/340 = 4.6.

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The losses in a transformer are shown in the following diagram:

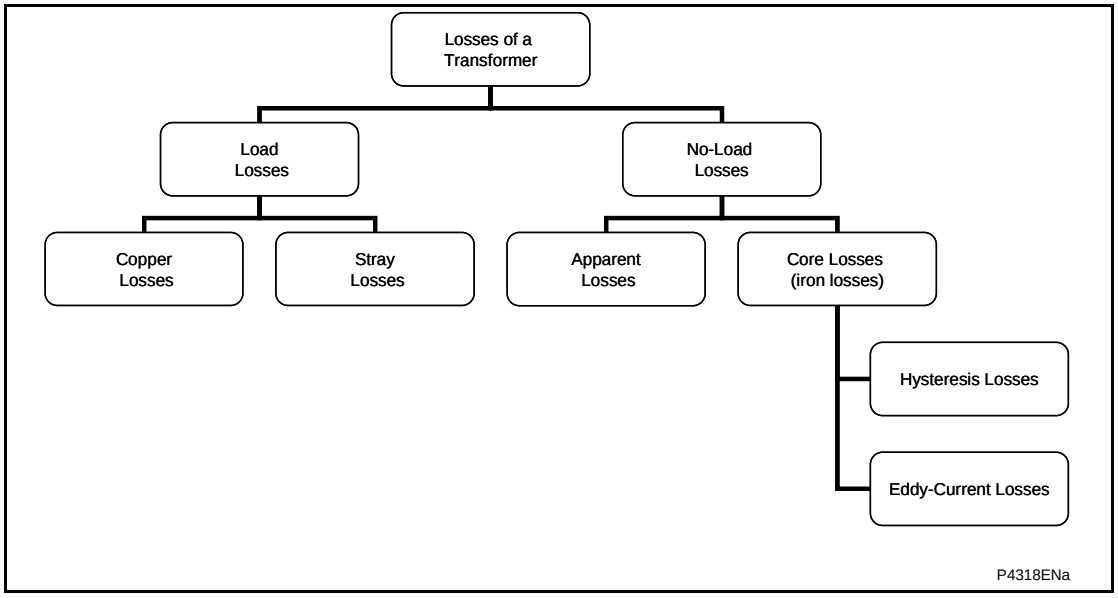


Figure 64: Transformer losses

No-load losses are mainly iron losses. The loss that is due to the magnetizing current in the primary winding is called the apparent loss. The flow of the magnetizing current through the resistance of the winding does create a real I^2R loss and voltage drop, although both are generally quite small. Time-varying fluxes produce losses in ferromagnetic materials, known as core losses. These iron losses are divided into hysteresis losses and eddy-current losses.

The sum of copper losses and the stray losses is called the load losses. Copper losses are due to the flow of load currents through the primary and secondary windings. They are equal to I^2R, and they heat up the wires and cause voltage drops. Stray losses are due to the stray capacitance and leakage inductance. Stray capacitance exists between turns, between one winding and another, and between windings and the core.

- Winding hottest-spot rise over top oil at rated load (Hot Spot overtop)
- Top oil rise over ambient temperature at rated load (Top Oil overamb). It can also be determined by actual test per IEEE Std. C57.12.90-1993.
- Winding exponent (Winding exp m) and oil exponent (Oil exp n)

As indicated in the IEEE Std. C57.91-1995, the following are suggested winding and oil exponents.

Type of cooling	m (winding exponent)	n (oil exponent)
OA	**0.8**	**0.8**
FA	**0.8**	**0.9**
Non-directed FOA or FOW	**0.8**	**0.9**
Directed FOA or FOW	**1.0**	**1.0**

Table 13: IEEE Std C57.91-1995 winding and oil exponents

These exponents are empirically derived and are required to calculate the variation of $\Delta\Theta_H$ and $\Delta\Theta_{TO}$ with load changes. The value of m has been selected for each mode of cooling to approximately account for effects of changes in resistance and off viscosity with changes in load. The value of n has been selected for each mode of cooling to approximately account for effects of change in resistance with change in load.

The **Cooling Mode** setting - **Natural, Forced Air, Forced Oil, Forced Air Oil, Select via PSL** specifies which kind of cooling mode is used to cool the transformer. If **Select Via PSL** then DDB inputs (650 Frcd Air Cool and 651 Frcd Oil Cool) can be used to select the cooling mode **Winding exp m** and **Oil exp n** settings. If DDB 650 = 1 then cooling mode is Forced Air Cooling, if DDB 651 = 1 then cooling mode is Forced Oil Cooling, if DDB 650 and 651 = 1 then cooling mode is Forced Air Oil Cooling, if DDB 650 and 651 = 0 then cooling mode is Natural Cooling.

- Winding time constant at hot spot location (**Hot spot rise co**). It may also be estimated from the resistance cooling curve during thermal tests.
- Oil time constant (**Top oil rise co**)

The P34x has up to three hot spot stages and up to three top oil stages. The tripping signal, **Top Oil T>x Trip**, is asserted when the top oil (measured or calculated) temperature is above the setting, **Top Oil>x Set**, and the time delay, **tTop Oil>x Set** has elapsed. Also, the tripping signal, **Hot Spot>x Trip**, is asserted when the hottest-spot (calculated only) temperature is above the setting, **Hot Spot>x Set**, and the time delay, **tHot Spot>x Set** has elapsed.

When setting the hot spot and top oil stages take into consideration the suggested temperature limits (IEEE Std. C57.91-1995):

Suggested limits of temperature for loading above nameplate distribution transformers with 65°C rise	
Top oil temperature	120°C
Hot spot conductor temperature	200°C
Suggested limits of temperature for loading above nameplate power transformers with 65°C rise (refer to IEEE Std. C57.91-1995 to consider the four types of loading)	
Top oil temperature	110°C
Hot spot conductor temperature	180°C

Table 14: Suggested limits of temperature for loading above nameplate distribution transformers with 65°C rise

2.32 Loss of life

As stated in IEEE Std. C57.91-1995, aging of insulation is a time function of temperature, moisture and oxygen content. The moisture and oxygen contributions to insulation deterioration are minimized due to modern oil preservation systems. Therefore temperature is the key parameter in insulation ageing. Temperature distribution is not uniform; the part with the highest temperature undergoes the greatest deterioration. Therefore the hottest spot temperature is considered in loss of life calculations.

2.32.1 Setting guidelines

Set the life hours at reference hottest spot temperature. According to IEEE Std. C57.91-1995, the normal insulation life at the reference temperature in hours or years must be arbitrarily defined. The following table extracted from IEEE Std. C57.91-1995 gives values of normal insulation life for a well-dried, oxygen-free 65°C average winding temperature rise insulation system at the reference temperature of 110°C.

Basis	Normal insulation life	
	Hours	Years
50% retained tensile strength of insulation (former IEEE Std C57.92-1981 criterion)	65000	7.42
25% retained tensile strength of insulation	135000	15.41
200 retained degree of polymerization in insulation	150000	17.12
Interpretation of distribution transformer functional life test data (former IEEE Std. C57.91-1981)	180000	20.55
NOTES: Tensile strength or degree of polymerization (D.P.) retention values were determined by sealed tube aging on well-dried insulation samples in oxygen-free oil. Refer to I.2 in annex I of the IEEE Std. C57.91-1995 for discussion of the effect of higher values of water and oxygen and also for the discussion on the basis given above.		

Table 15: Normal insulation life

The **Designed HS temp** should be set to 110°C if the transformer is rated 65°C average winding rise. If the transformer is rated 55°C average winding rise, set the **Designed HS temp** to 95°C.

As recommended by IEEE Std. C57.91-1995, the **Constant B Set** should be set to 15000 based on modern experimental data.

If the ageing acceleration factor calculated by the relay is greater than the setting **FAA> Set** and the time delay **tFAA> Set** has elapsed, the **FAA alarm** (DDB 479) would be activated.

If the loss of life calculated by the relay is greater than the setting **LOL>1 Set** and the time delay **tLOL> Set** has elapsed, the **LOL alarm** (DDB 480) would be activated.

The following is an example on how to set the loss of life function. Consider a new 65°C average winding rise rated transformer whose life hours at designed hottest spot temperature is 180,000 hrs. As a result, **Life Hours at HS** is set to 180,000, and the **Designed HS temp** is set to 110.0°C. The **Constant B Set** is 15,000 as recommended by IEEE from experimental data. The aging acceleration factor takes into consideration the constant B and the hottest spot temperature calculated by the thermal function. For a distribution transformer, IEEE suggests 200°C as the limit for the hottest spot temperature (refer to the thermal overload function to determine the hottest spot temperature for a power transformer). The aging acceleration factor alarm may be asserted when 70% of the 200°C is reached. The aging acceleration factor is calculated as follows:

$$FAA = e^{\left[\frac{B}{383} - \frac{B}{hottest-spot-tempt+273}\right]} = e^{\left[\frac{B}{383} - \frac{B}{0.7\times 200+273}\right]} = 17.2$$

Therefore **FAA>set** is 17.2. The **tFAA> Set** may be set to 10.00 min. The **LOL>1 Set** may be set to 115,000 hrs, if it is considered that the transformer has 65,000 hrs left (**Life Hours at HS** – hours left = 180,000 – 65,000 = 115,000 hrs). The **tLOL> Set** may be set to 10.00 min. Finally the **Reset Life Hours** setting determines the value of the LOL measurement once the Reset LOL command is executed. The default value is zero because considering a new transformer, after testing the thermal function in the P34x, the LOL measurement should be reset to zero.

Certain tests should be performed to determine the age of an old transformer. Advice from the transformer manufacturer should be requested.

2.33 Circuit breaker failure protection (50BF)

Following inception of a fault one or more main protection devices will operate and issue a trip output to the circuit breaker(s) associated with the faulted circuit. Operation of the circuit breaker is essential to isolate the fault, and prevent damage/further damage to the power system. For transmission/sub-transmission systems, slow fault clearance can also threaten system stability. It is therefore common practice to install circuit breaker failure protection, which monitors that the circuit breaker has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, breaker failure protection (CBF) will operate.

CBF operation can be used to back-trip upstream circuit breakers to ensure that the fault is isolated correctly. CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

2.33.1 Reset mechanisms for breaker fail timers

It is common practice to use low set undercurrent elements in protection relays to indicate that circuit breaker poles have interrupted the fault or load current, as required. This covers the following situations:

- Where circuit breaker auxiliary contacts are defective, or cannot be relied on to definitely indicate that the breaker has tripped.
- Where a circuit breaker has started to open but has become jammed. This may result in continued arcing at the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance severely limit fault current, the initiating protection element may reset. Therefore reset of the element may not give a reliable indication that the circuit breaker has opened fully.

For any protection function requiring current to operate, the relay uses operation of undercurrent elements (I<) to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting circuit breaker fail in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the protected circuit would always have load current flowing. Detecting drop-off of the initiating protection element might be a more reliable method.
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again using I< would rely on the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, and hence drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

2.33.1.1 Breaker fail timer settings

Typical timer settings to use are as follows:

CB fail reset mechanism	tBF time delay	Typical delay for 2½ cycle circuit breaker
Initiating element reset	CB interrupting time + element reset time (max.) + error in tBF timer + safety margin	50 + 50 + 10 + 50 = 160 ms
CB open	CB auxiliary contacts opening/closing time (max.) + error in tBF timer + safety margin	50 + 10 + 50 = 110 ms
Undercurrent elements	CB interrupting time+ undercurrent element (max.) + safety margin operating time	50 + 12 + 50 = 112 ms

Table 16: CB fail typical timer settings

Note: All CB Fail resetting involves the operation of the undercurrent elements. Where element reset or CB open resetting is used the undercurrent time setting should still be used if this proves to be the worst case.

The examples above consider direct tripping of a 2½ cycle circuit breaker.

Note: Where auxiliary tripping relays are used, an additional 10 - 15 ms must be added to allow for trip relay operation.

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2.33.2 Breaker fail undercurrent settings

The phase undercurrent settings (I<) must be set less than load current, to ensure that I< operation indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20% In, with 5% In common for generator circuit breaker CBF.

The sensitive earth fault protection (SEF) and standby earth fault (SBEF) undercurrent elements must be set less than the respective trip setting, typically as follows:

ISEF< = (ISEF> trip)/2

IN< = (IN> trip)/2

For generator applications the undercurrent elements should be measuring current from CTs on the terminal side of the generator. This is because for an internal fault on the generator after the CB has tripped the generator will still be supplying some fault current which will be seen by undercurrent elements measuring current from CTs on the neutral side of the generator. This could therefore give false indication of a breaker fail condition.

The voltage dependent overcurrent protection and underimpedance protection used for back-up protection of system faults are usually connected to the neutral side CTs so that the generator is in the zone of protection. These protection functions use the IA, IB, IC current inputs in the P343/4/5/6. Therefore, if the IA, IB, IC inputs are connected to neutral side CTs then the IA-2, IB-2, IC-2 inputs should be selected for the undercurrent elements using the setting I< Current Input - IA-1, IB-1, IC-1/IA-2, IB-2, IC-2.

2.34 Breaker flashover protection

Prior to generator synchronization, or just following generator tripping, where the protected generator could be slipping with respect to a power system, it is possible to establish at least twice rated phase-neutral voltage across the generator circuit breaker. An even higher voltage might briefly be established just after generator tripping for prime mover failure, where the pre-failure level of excitation might be maintained until AVR action takes place. Whilst generator circuit breakers must be designed to handle such situations, the probability of breaker interrupter breakdown or breakdown of open terminal switch gear insulators is increased and such failures have occurred.

This mode of breaker failure is most likely to occur on one phase initially and can be detected by a neutral current measuring element. If the generator is directly connected to

the power system, the second stage of stator earth fault protection **(IN>2**...) could be applied as an instantaneous element by setting the time delay **IN>2 TimeDelay** to 0 s, to quickly detect the flashover. To prevent loss of co-ordination this stage must be blocked when the circuit breaker is closed. This can be programmed by correct configuration of the programmable scheme logic and can be integrated into the circuit breaker fail logic, as shown in Figure 65.

Where the machine is connected to the system via a step-up transformer a similar scheme can be arranged. The P34x relay standby earth fault protection element can be connected to measure the transformer HV earth fault current to provide the breaker flashover protection, via suitable scheme logic. The machine earth fault protection can be provided by the P34x sensitive earth fault protection element, as shown in Figure 66.

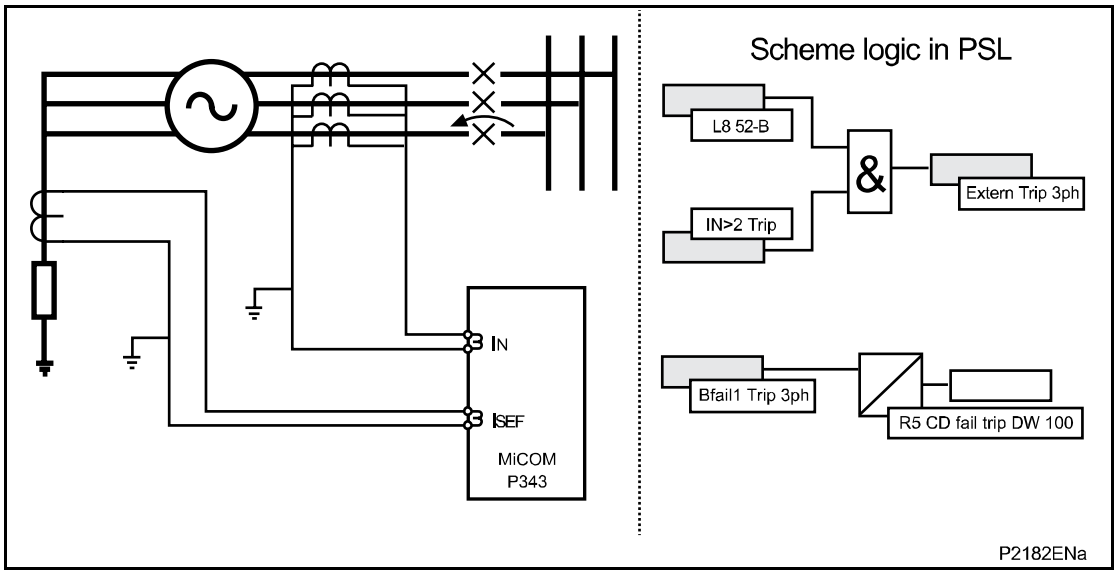


Figure 65: Breaker flashover protection for directly connected machine

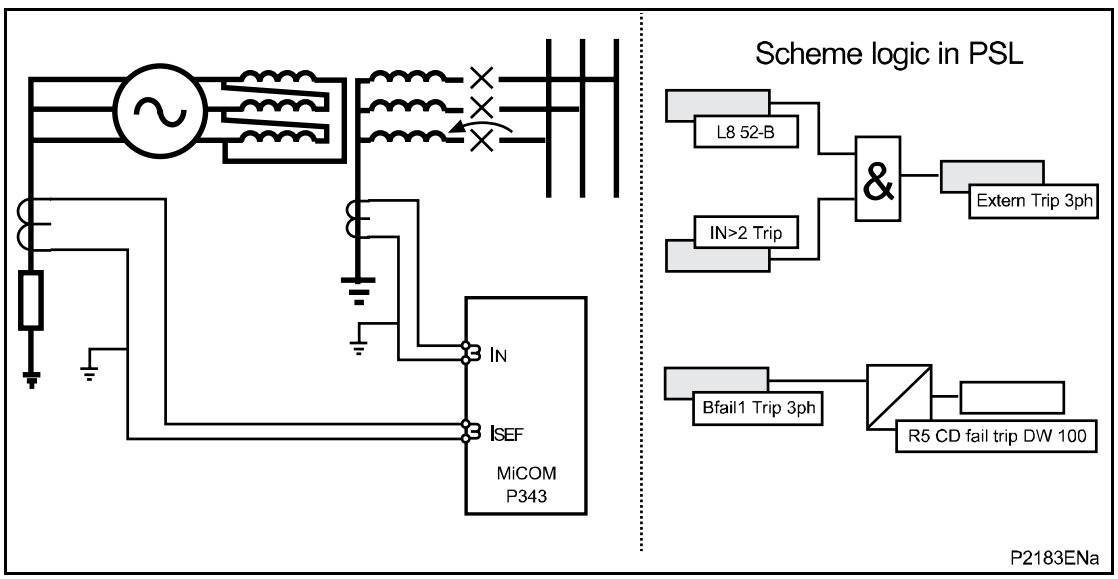


Figure 66: Breaker flashover protection for indirectly connected machine

2.35 Blocked overcurrent protection

Blocked overcurrent protection involves the use of start contacts from downstream relays wired onto blocking inputs of upstream relays. This allows identical current and time settings to be employed on each of the relays involved in the scheme, as the relay nearest to the fault does not receive a blocking signal and hence trips discriminatively. This type of scheme therefore reduces the amount of required grading stages and consequently fault clearance times.

The principle of blocked overcurrent protection may be extended by setting fast acting overcurrent elements on the incoming feeders to a substation which are then arranged to be blocked by start contacts from the relays protecting the outgoing feeders. The fast acting element is therefore allowed to trip for a fault condition on the busbar but is stable for external feeder faults by means of the blocking signal. This type of scheme therefore provides much reduced fault clearance times for busbar faults than would be the case with conventional time graded overcurrent protection. The availability of multiple overcurrent and earth fault stages means that back-up time graded overcurrent protection is also provided. This is shown in Figure 67 and Figure 68.

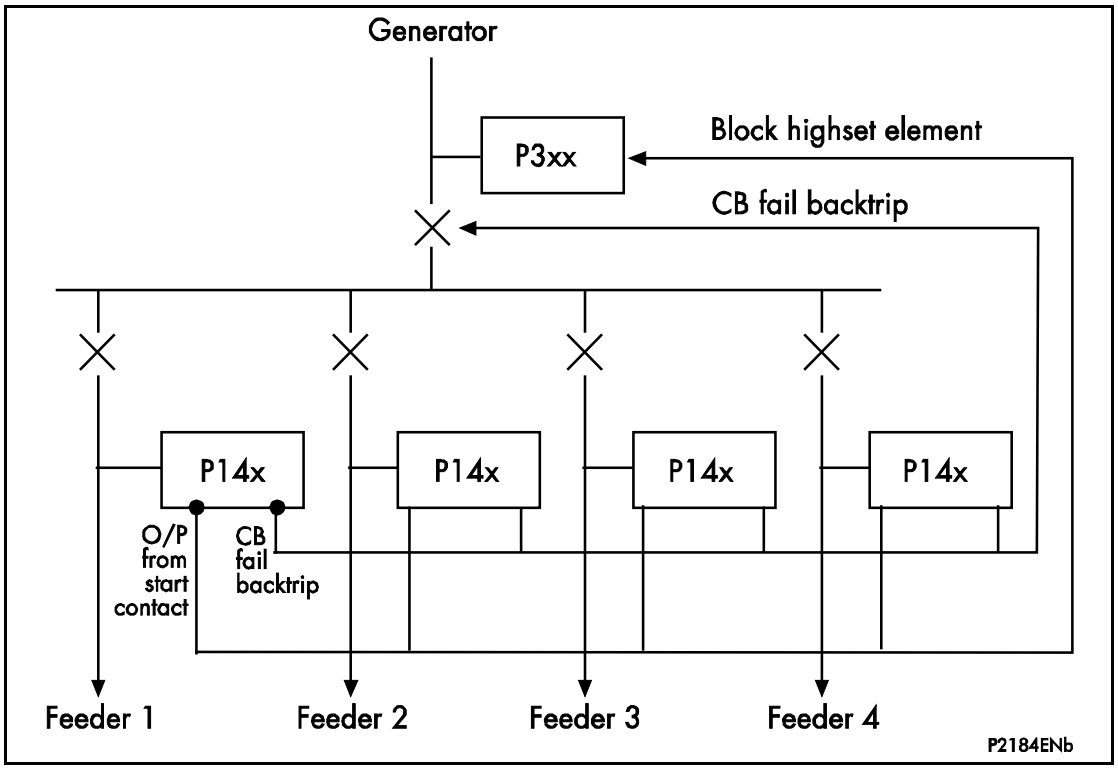


Figure 67: Simple busbar blocking scheme (single incomer)

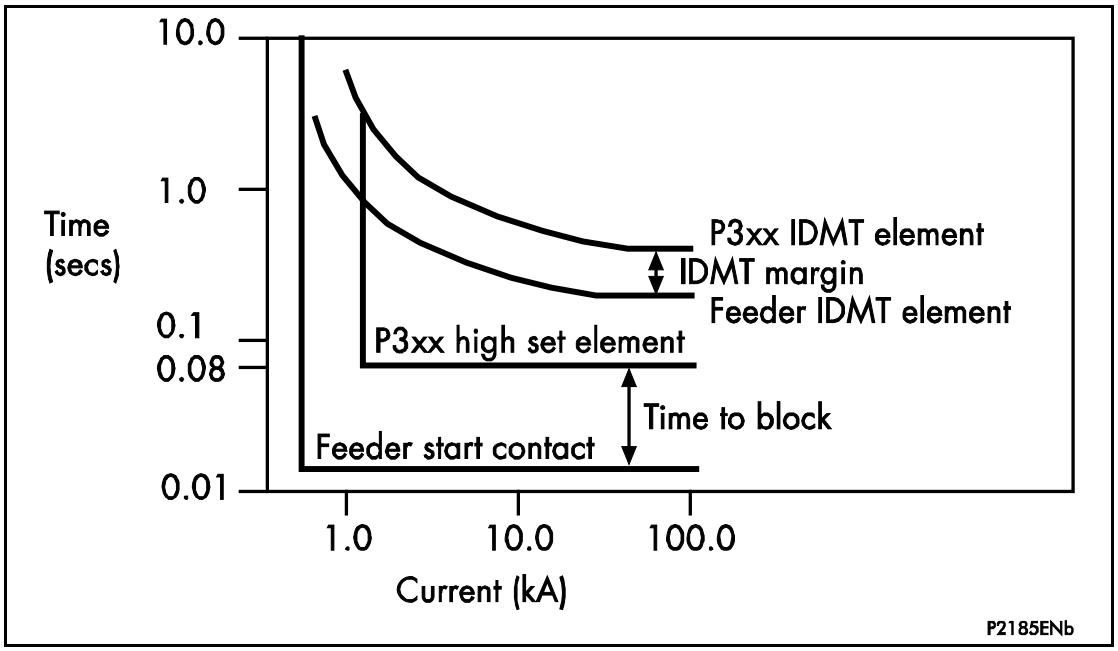


Figure 68: Simple busbar blocking scheme (single incomer)

The P140/P34x relays have start outputs available from each stage of each of the overcurrent and earth fault elements, including sensitive earth fault. These start signals may then be routed to output contacts by programming accordingly. Each stage is also capable of being blocked by being programmed to the relevant opto-isolated input.

The P34x relays provide a 50 V field supply for powering the opto-inputs. Hence, in the unlikely event of the failure of this supply, blocking of that relay would not be possible. For this reason, the field supply is supervised and if a failure is detected, it is possible, via the relays programmable scheme logic, to provide an output alarm contact.

This contact can then be used to signal an alarm within the substation. Alternatively, the relays scheme logic could be arranged to block any of the overcurrent/earth fault stages that would operate non-discriminatively due to the blocking signal failure.

For further guidance on the use of blocked overcurrent schemes refer to General Electric.

2.36 Current loop inputs and outputs

2.36.1 Current loop inputs

Four analog (or current loop) inputs are provided for transducers with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA. The analog inputs can be used for various transducers such as vibration monitors, tachometers and pressure transducers. Associated with each input there are two protection stages, one for alarm and one for trip. Each stage can be individually enabled or disabled and each stage has a definite time delay setting. The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold **Under** or when the input current is above the input value **Over**.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop inputs.

For the 4 - 20 mA input range, a current level below 4 mA indicates that there is a fault with the transducer or the wiring. An instantaneous under current alarm element is available, with a setting range from 0 to 4 mA. This element controls an output signal (CLI1/2/3/4 I< Fail Alm., DDB 390-393) which can be mapped to a user defined alarm if required.

2.36.2 Setting guidelines for current loop inputs

For each analog input, the user can define the following:

- The current input range: 0 - 1 mA, 0 - 10 mA, 0 - 20 mA, 4 - 20 mA
- The analog input function and unit, this is in the form of a 16-character input label
- Analog input minimum value (setting range from –9999 to 9999)
- Analog input maximum value (setting range from –9999 to 9999)
- Alarm threshold, range within the maximum and minimum set values
- Alarm function - over or under
- Alarm delay
- Trip threshold, range within maximum and minimum set values
- Trip function - over or under
- Trip delay

Each current loop input can be selected as Enabled or Disabled as can the Alarm and Trip stage of each of the current loop input. The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold **Under** or when the input current is above the input value **Over** depending on the application. One of four types of analog inputs can be selected for transducers with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA.

The Maximum and Minimum settings allow the user to enter the range of physical or electrical quantities measured by the transducer. The settings are unit-less; however, the user can enter the transducer function and the unit of the measurement using the 16-character user defined CLI Input Label. For example, if the analog input is used to monitor a power measuring transducer, the appropriate text could be “Active Power(MW)”.

The alarm and trip threshold settings should be set within the range of physical or electrical quantities defined by the user. The relay will convert the current input value into its corresponding transducer measuring value for the protection calculation.

For example if the CLI Minimum is –1000 and the CLI Maximum is 1000 for a 0 - 10 mA input, an input current of 10 mA is equivalent to a measurement value of 1000, 5 mA is 0 and 1 mA is –800. If the CLI Minimum is 1000 and the CLI Maximum is -1000 for a 0 - 10 mA input, an input current of 10 mA is equivalent to a measurement value of –1000, 5 mA is 0 and 1 mA is 800. These values are available for display in the **CLIO Input 1/2/3/4** cells in the **MEASUREMENTS 3** menu. The top line shows the CLI Input Label and the bottom line shows the measurement value.

2.36.3 Current loop outputs

Four analog current outputs are provided with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA which can alleviate the need for separate transducers. These may be used to feed standard moving coil ammeters for analog indication of certain measured quantities or into a SCADA using an existing analog RTU.

The outputs can be assigned to any of the following relay measurements:

- Magnitudes of IA, IB, IC, IN, IN Derived, I Sensitive
- Magnitudes of I1, I2, I0
- IA RMS, IB RMS, IC RMS
- Magnitudes of VAB, VBC, VCA, VAN, VBN, VCN, VN Measured, VN Derived
- Magnitudes of V1, V2 and V0
- VAN RMS, VBN RMS, VCN RMS
- Frequency
- Single-phase active, reactive and apparent power, single-phase power factor
- Three-phase active, reactive and apparent power, single-phase power factor
- VN 3rd harmonic (P343/4/5 only)
- Stator thermal state
- Rotor (NPS) thermal state (P342/P343/P344/P345/6 only)
- RTD temperatures (P342/P343/P344/P345/6 only)
- Analog inputs

The user can set the measuring range for each analog output. The range limits are defined by the Maximum and Minimum settings. This allows the user to “zoom in” and monitor a restricted range of the measurements with the desired resolution. For voltage, current and power quantities, these settings can be set in either primary or secondary quantities, depending on the **CLO1/2/3/4 Set Values - Primary/Secondary** setting associated with each current loop output.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop outputs.

2.36.4 Setting guidelines for current loop outputs

Each current loop output can be selected as Enabled or Disabled. One of four types of analog output can be selected for transducers with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA. The 4 - 20 mA range is often used so that an output current is still present when the measured value falls to zero. This is to give a fail safe indication and may be used

to distinguish between the analog transducer output becoming faulty and the measurement falling to zero.

The Maximum and Minimum settings allow the user to enter the measuring range for each analog output. The range, step size and unit corresponding to the selected parameter is shown in the table in the Operating chapter, *P34x/EN OP*. This allows the user to "zoom in" and monitor a restricted range of the measurements with the desired resolution.

For voltage, current and power quantities, these settings can be set in either primary or secondary quantities, depending on the **CLO1/2/3/4 Set Values - Primary/Secondary** setting associated with each current loop output.

The relationship of the output current to the value of the measurand is of vital importance and needs careful consideration. Any receiving equipment must, of course, be used within its rating but, if possible, some kind of standard should be established.

One of the objectives must be to have the capability to monitor the voltage over a range of values, so an upper limit must be selected, typically 120%. However, this may lead to difficulties in scaling an instrument.

The same considerations apply to current transducers outputs and with added complexity to watt transducers outputs, where both the voltage and current transformer ratios must be taken into account.

Some of these difficulties do not need to be considered if the transducer is only feeding, for example, a SCADA outstation. Any equipment which can be programmed to apply a scaling factor to each input individually can accommodate most signals. The main consideration will be to ensure that the transducer is capable of providing a signal right up to the full-scale value of the input, that is, it does not saturate at the highest expected value of the measurand.

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2.37 Earth fault detection in the startup converter

If an earth fault occurs in the startup converter circuit, a current flows through all earthed parts of the system because of the DC voltage. The thermal load is the highest on the earthing and neutral transformers as these have a lower ohmic resistance than the voltage transformers.

The DC current can be converted into a DC voltage using a shunt and the DC voltage can be measured by a DC voltage transducer such as an i4DB ISTAT400. In the example below the i4DB would be with a DC voltage range 0+/-50mV to 0+/-1V programmed to a scale 0-150mV/4-20mA. The 4-20mA output of the transducer can be connected to the 4-20mA current loop input of the P34x to provide a time delayed earth fault trip.

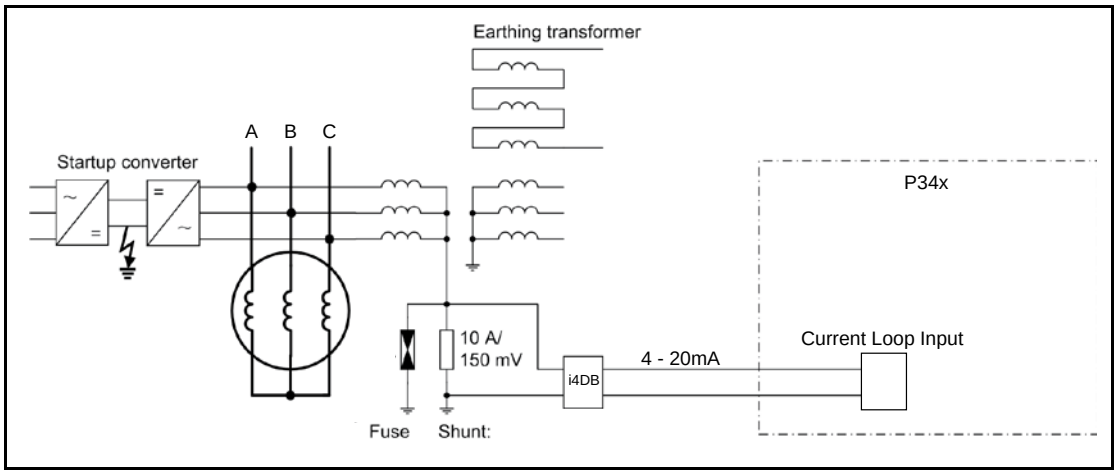


Figure 69: DC voltage protection to detecting an earth fault in the startup converter

For earth fault protection of the the startup converter of a gas turbine set, in the case of an earth fault in the DC circuit, half of the DC voltage is present between the transformer starpoint and the earth if the transformer starpoint is not earthed. This voltage can be considered as the voltage feeding the earth fault current. As the transformer starpoints are

earthed, the current flowing is determined by the fault voltage and the ohmic resistance of all transformers that are galvanically connected to the converter set and earthed. The DC earth fault current is normally between about 3 and 4A.

For a startup converter with a startup transformer of $V_{N\,ST} \approx 1.4$ kV and for a 6-pulse bridge circuit, the DC voltage, $V_{DC} \approx 1.35 \times V_{N\,ST} = 1.89$ kV. In the case of an earth fault in the intermediate circuit, the 'displacement voltage' will be half of the DC voltage (V_{DC} fault = 0.5 V_{DC} = 945 V).

If we assume that the earthing transformer has an ohmic winding resistance of R ≈ 150Ω, a DC current of I_0 = 945 V/150Ω = 6.3 A will flow through its starpoint.

Note: The ohmic winding resistances of earthing and neutral transformers can vary widely depending on the type and so data should be obtained from the manufacturer, or determined by measurements.

If not tripped, the earth fault current could cause a temperature overload that would damage the wye-connected voltage transformers and the earthing transformer. To ensure that the protection will pick up reliably, it should be set to a value of less than half the fault current, for example 2 A. With the shunt and i4D transducer used in the example, this current produces a secondary current of 7.2 mA (fault current ≈ 6 A, selected pickup value = 2 A, setting value = 7.2 mA).

For the startup earth fault current protection the tripping time delay is determined by the permissible temperature load of the earthing and/or neutral transformer. A value of 2 s or less is quite common.

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2.38 Rotor earth fault protection (64R)

Rotor earth fault protection is used to detect earth faults in the excitation circuit of synchronous generators.

The field circuit of a synchronous generator, comprising the winding, the exciter and the field circuit breaker, is a DC circuit which is not normally earthed. If an earth fault occurs, no steady state fault current will flow and no damage will be incurred. If a second earth fault occurs at a separate point in the field system, this constitutes a winding short-circuit of the excitation circuit where part of the field winding is by-passed, and the current through the remaining portion may be increased.

The field current from a large machine can be high causing serious damage to the rotor and the exciter. If a large part of the field winding is short-circuited, the flux may result in an attracting force which is strong on one pole and weak on the opposite one. The result is an unbalanced force causing violent vibrations. This may damage the bearings or even displace the rotor which in turn may damage the stator.

After the first earth fault occurs, the risk of a second earth fault increases, since the first fault establishes an earthed reference for the voltage induced in the field by stator transients. These transients increase the stress to earth at other points in the field winding.

2.38.1 Setting guidelines for rotor earth fault protection

The rotor earth resistance is measured using an external low frequency square wave injection, coupling and measurement unit, P391, connected to the rotor circuit. The measurement of the rotor resistance is passed to the P342/3/4/5/6 via a current loop output (0-20 mA) on the P391 connected to one of the 4 current loop inputs (0-20 mA) on the P342/3/4/5/6. The rotor earth fault protection is only available if the relay includes the CLIO hardware option. Two under resistance stages of definite time protection are available for alarm and trip.

The rotor earth fault protection element can be selected by setting the **Rotor E/F** cell in the Configuration column to Enabled.

The rotor earth fault protection uses one of the four current loop (transducer) inputs to provide the rotor resistance measured by the P391 injection, coupling and measuring unit. The current loop input used for rotor earth fault protection is selected using the setting **CL I/P select – Current Loop CL1/CL2/CL3/CL4** in the **Rotor EF** menu settings.

The under resistance alarm (**64R R<1 Alarm**) and trip (**64R R<2 Trip**) stages can be independently enabled or disabled. The under resistance alarm threshold, **64R R<1 Alm Set**, and trip threshold, **64R R<2 Trip Set** must be set below the level of resistance present under normal conditions. This resistance can be determined by viewing the **64R R Fault** cell in the **MEASUREMENTS 3** menu. A typical value for the fault resistance alarm setting is 40 kΩ and the trip setting is 5 kΩ. These values can be changed depending on the insulation resistance and the coolant. Care must be taken to allow a sufficient margin between the setting value and the actual insulation resistance. As interference from the excitation system cannot be excluded, the setting for the warning stage can be finally established during primary tests.

During a generator start-up or during system transient conditions, intermittent earths can be produced by moisture or copper dusting, which could give nuisance operations, particularly if instantaneous operation is used. A time delay is recommended to avoid nuisance tripping. A time delay for the 64R R<1/2 elements can be set in the **64R R<1 Alm Dly**, **64R R<2 Trip Dly** cells. The default time delays, 1s for trip and 10s for the alarm, provide typical values. The set times are additional time delays not including the operating time of the protective function.

The **Injection Frequency** setting, **0.25 Hz / 0.5 Hz / 1 Hz** must be set to match the frequency set on the P391 coupling unit which is selected with jumper links, see P391 connection diagrams for jumper link positions in the Installation Chapter, *P34x/EN IN*.

The **R Compensation** setting is used to compensate any resistance errors. The setting can be found during commissioning testing.

The P34x rotor earth fault protection does not discriminate between one point of insulation breakdown and multiple points of insulation breakdown. When a device such as a generator vibration detector is used for the detection of multiple points of insulation breakdown then the P34x can be used to alarm only and to trip under supervision of the vibration device. When a vibration detector is not used, it is recommended to trip from the P34x rotor earth fault protection for the first fault detected.

The P391 can be connected to a single end or to two ends of the field winding, see Installation section connection diagrams, *P34x/EN IN*. The 2 end connection is recommended where possible as this connection provides more stable and steady measurements.

2.38.2 Redundant rotor earth fault protection

To provide redundant rotor earth fault protection one P391 can be be connected to two P34x relays.

The P391 current loop output voltage was designed to drive 20 mA through a maximum load of 500 ohms but the input impedance of one P34x 0-20 mA current loop input is 360 ohms. So the P391 can not directly drive two current loop inputs with the P391 current loop output.

However, this problem can be overcome by using a repeater between the P391 and P34x relays which provides 2 x 0-20 mA outputs. A repeater such as the PR 5104A from Omni Instruments, (http://www.omniinstruments.co.uk) has been tested and can be used for this type of application. The 5104A current input resistance is 10 ohms and each 0-20 mA output maximum load is 600 ohms.

Note: For 1/0.6 mm lightweight cable (CSA 0.28 mm^2) the cable resistance is 65 Ω/km so for this cable the maximum cable distance between the P391 and P34x can be approx. 1km, (maximum cable length (km) = 140/loop resistance 2Rl = 140/2x65 = 1.07km). It is recommended that a screened cable earthed at one end is used to reduce interference.

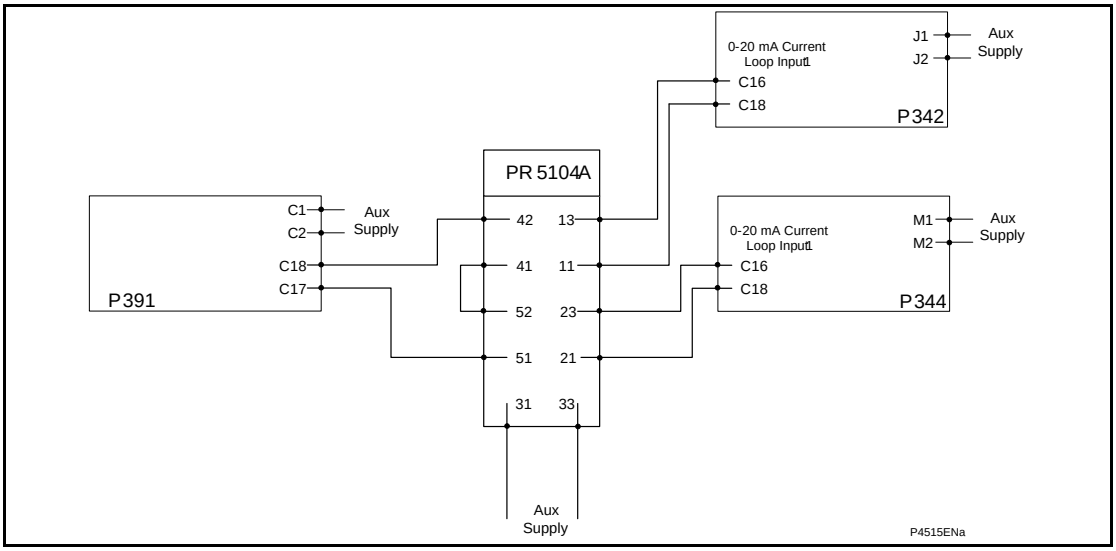


Figure 70: Redundant rotor earth fault connection

2.39 Protection for variable speed machines

Power management and stability of the grid are a growing concern. Increased use of renewable energy generation systems, such as wind turbines and solar plants, has led to more gas turbines being installed as spinning and secondary reserve because these intermittent sources of renewable electrical generation cannot be easily and effectively dispatched to meet the demand.

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This is not a long-term solution to reduce future CO2 emissions. To overcome this problem, efficient and economic technologies to store large amounts of electrical energy are needed. Pumped storage is still the most efficient and flexible form of large-scale electricity storage. Pumped storage is developing towards variable speed pump turbine technology, which offers greater efficiency and dynamic power adjustment both during consumption and production modes.

This section describes the application of the protection functions in a new and innovative protection system for protecting large variable speed Double Fed Induction (DFI) machines for pumped storage plants. The rotor of a variable speed machine has a 3 phase winding with slip rings supplied with low frequency currents by means of voltage source converters from the AC system and its speed depends on the frequency of the power fed from the converter. During normal operation the rotor current frequency is very low (typically 0.1 to 6Hz), during start-up and breaking it varies between zero and the rated grid frequency (50 or 60 Hz). The variable speed motor generators require construction of a fully independent protection system to guarantee the plant's safety in all conditions.

Currently, the market offers no protection relay for the extremely low frequency currents and voltages in the variable speed rotor and stator during the initial start-up and run down. The new protection system will measure and monitor these signals, while taking into account the specifics of the start, stop and operation in both pump and generator modes. Cutting edge "Digital Substation" technology, which incorporates Non-Conventional Instrument Transformers (NCIT: Non-Conventional Current Transformers (NCCT) and Non-Conventional Voltage Transformers (NCVT)) with IEC 61850-9-2 LE digital process bus communications to the protection relays, is used to measure the low frequency current and voltage signals.

The main development difficulties for the protection relate to the rotor protection design and comprise:

- Dynamic frequency variation
- Extremely low frequency
- Modulation of the rotor's voltage supply (PWM: Pulse Width Modulation) by the VSI converter

2.39.1 Double fed induction machine protection introduction

For large DFI machines, the standard generator protection relay such as the P345 is not suitable to provide full protection for the rotor and stator therefore the protection scheme must be complemented by a new relay, P348, to mainly provide the rotor protection and stator protection during the start up and run down of the machine, see Figure 71.

The standard P345 generator protection relay can provide adequate stator protection for the variable speed machine using conventional CTs and VTs to provide protection over the frequency range 5-70Hz. The new P348 relay has been designed to use Non Conventional Instrument Transformers (NCITs) required to measure a wide range of frequencies in the rotor and stator of DFI machines, 0.1 to 70Hz. The relay includes a process bus IEC 61850-9-2 LE port to connect to the NCITs via merging units and primary converters.

In the protection scheme, as for a conventional machine, 100% stator earth fault protection is provided using a low frequency injection technique with the P345-1 Main 1 stator protection relay. The rotor earth fault protection is also using the same low frequency injection technique using the P345-2 Main 2 stator protection relay. The single line diagram in Figure 71 shows an overview of a typical protection scheme.

Redundancy of the protective circuits imposes duplication of the relays (P348-1 + P348-2 and P345-1 + P345-2) as well as the acquisition chain (double NCCT and NCVT) in the same way as for a standard protection scheme.

The new P348 relay uses the IEC 61850-9-2 LE digital process bus protocol to interface with the NCITs required to measure the low frequency signals via a merging unit (XMU800) and primary converters (PC12/14).

The relays IEC 61850-9-2 architecture proposed is a point to point connection between the NCITs, merging unit and relay IEC 61850-9-2 port in Figure 71. This is equivalent to a conventional hardwired scheme between the CTs/VTs and the relay. Dependability can be achieved by using duplicate or redundant relays, merging units, primary converters and NCITs in a similar way to a conventional scheme where redundant protection relays are connected to separate CTs and VTs to avoid common mode failures.

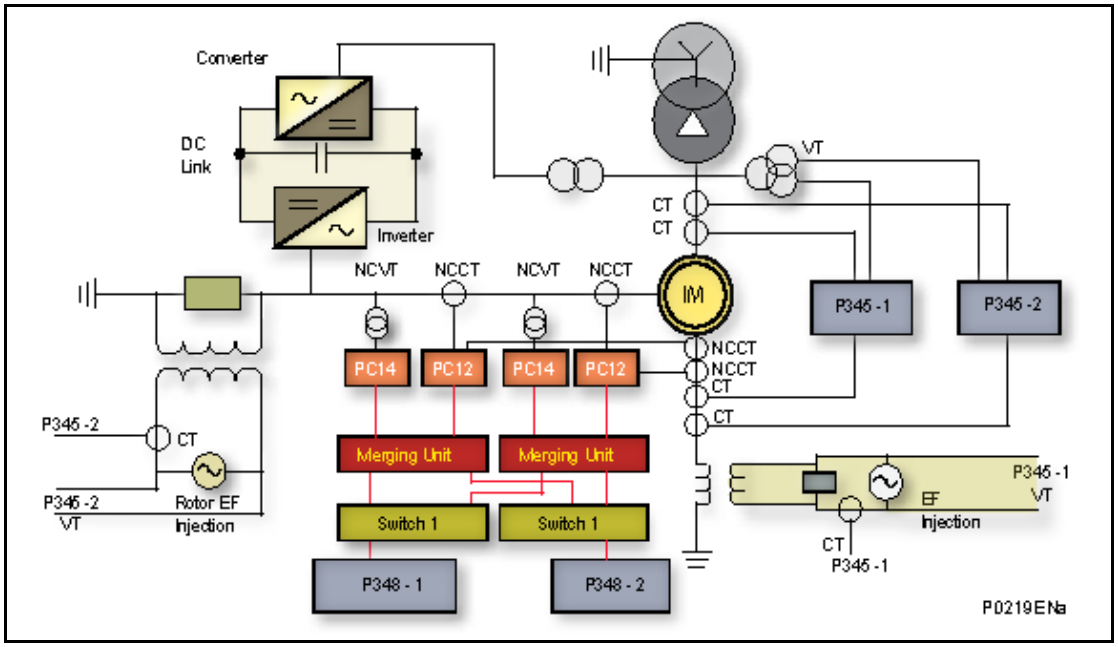


Figure 71: Single line diagram of typical protection scheme

- NCVT: Non-Conventional Voltage Transformer (voltage sensor)
- NCCT: Non-Conventional Current Transformer (current sensor)
- PC 12 and PC14 Primary Converters: Analog to digital signal converter (PCBUS protocol)

- Merging unit (XMU800): Digital signal (PC BUS or IEC 61850-9-2) to IEC 61850-9-2 digital signal converter including time synchronising (1 Pulse Per Second or IEEE1588 protocol)
- EF: Rotor Earth Fault protection devices
- Hardwired connection:
- Digital connection:

Depending on the substation layout, a large amount of layouts are possible using the PC1X primary converters. A typical layout with a PC12 and PC14 primary converter, a P348 protection relay and a supervising computer is shown in the example below.

See the separate XMU800 and PC12/14 user guides for more information on connecting and setting up these devices (PC1x Primary Converter for NCIT User Guide and XMU8xx Merging Unit for NCIT User Guide).

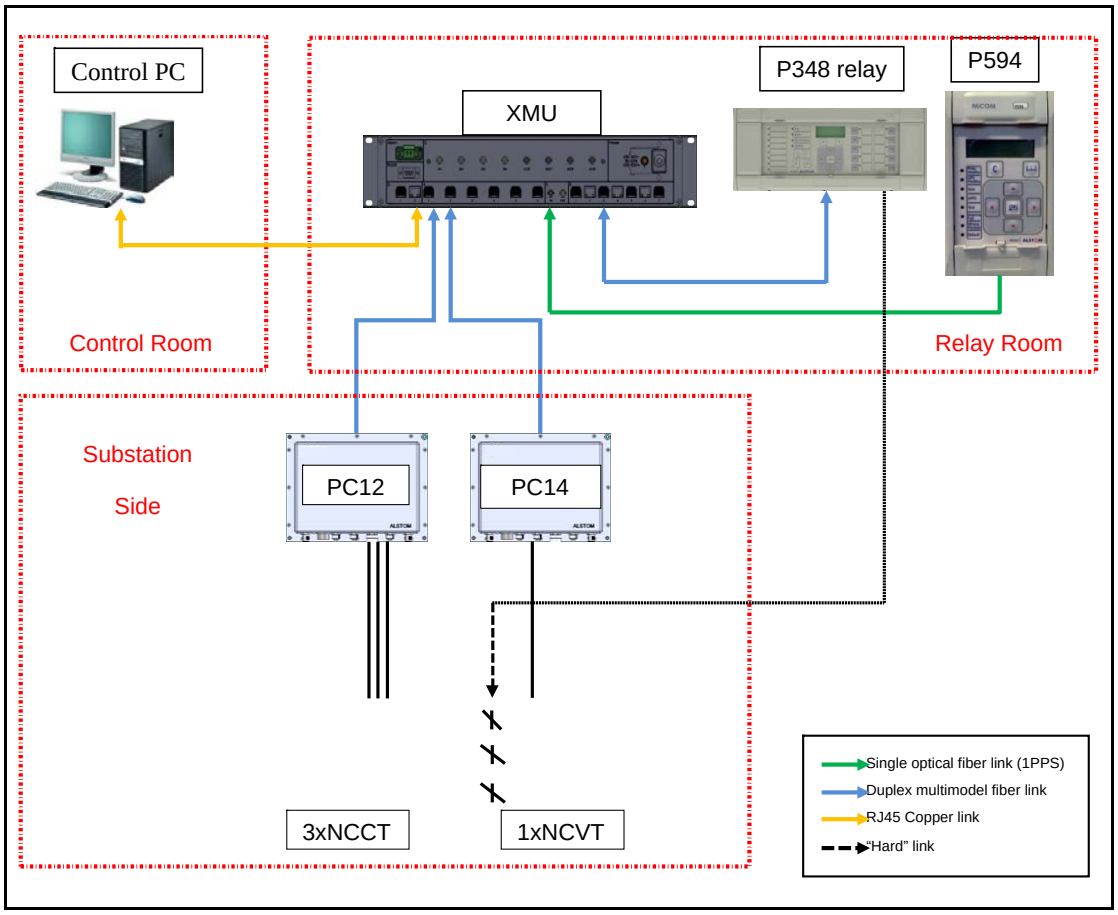


Figure 72: Typical scheme layout

The following components are used in the layout:

- **P594**: GPS Receiver device. Connected through a single fiber to the XMU to send the 1 PPS synchronisation signal.
- **P348 relay**: 61850.9-2 compliant relay. Connected to the XMU port B3 through a duplex fiber (LC ⇔ LC connectors).
- **PC14** (PC14 Voltage Primary Converter): Connected to the XMU port A2 through a duplex fiber (LC ⇔ LC connectors). Converts analog signal from NCIT Voltage Sensor (NCVT). Only 1 voltage channel is used in this case.
- **PC12** (Current Primary Converter): Connected to the XMU port A1 through a duplex fiber (LC ⇔ LC connectors). Converts analog signal from NCIT Current Sensors (NCCT). The 3 input channels of PC12 are used in this case.

- **Control PC**: Computer equipped with Telnet and/or a web-browser to set parameters on the XMU. Connected to the XMU port D2 through RJ45/RJ45 cable.

Note: The PC1x is installed “in the field” as close as possible to the current/voltage sensor, due to the low magnitude of the output signals from the NCIT sensors.

2.39.2 Time synchronisation between multiple merging units

As discussed in the Operation chapter the IEC 61850-9-2LE sampled values carry quality flags for each channel to report any detectable sample quality issues. The quality flags also take into account the synchronisation between multiple logic nodes (LNs). The P348 software provides a setting **Synchro Alarm** in the **IEC 61850-9-2 LE** menu. This configures the synchronisation level of the relay using the settings **Global 1 PPS, Local 1 PPS** and **No SYNC CLK**. If the synchronisation flag of a sampled value frame from a LN is below (**Local 1 PPS** is considered below **Global 1 PPS**) this setting, the synchronisation between this LN and the others will be considered to have been lost by the IEC 61850-9-2 LE card, which will mark the quality flags of all analogue channels from this LN as ‘Invalid’.

Figure 71 shows a possible redundancy architecture of P348 relays, where the two sets of three phase voltages used in a P348 for VTS are from two merging units (MUs). In this case as the P348 VTS uses RMS calculated values of phase voltages there is no need to have time synchronization between the merging units as the RMS values will be very close with or without time synchronization of the samples.

If two or more merging units are required to have a common time reference this common time reference can be the 1 pulse per second (1pps) signal converted from a global GPS signal by an appropriate device such as the P594, or alternatively can be any local common time reference the two MUs can be synchronised to. The **Synchro Alarm** setting for this application should therefore be set to **Local 1 PPS**. This, however, means that in the event a MU loses synchronisation with the other all analogue channels from this MU and all protection and non-protection functions that use any of the channels (for example Overvoltage protection and NVD protection) will be affected.

There is no need for time synchronizing between the two sets of voltages from 2 MUs to a single P348. Therefore, the **Synchro Alarm** setting for this application should be set to **No SYNC CLK**, meaning that no synchronisation check will be carried out. Also, if only one set of 3 phase voltages is used and all the voltages and currents needed by the P348 are provided by a single merging unit the **Synchro Alarm** setting for this application should be set to **No SYNC CLK**, meaning that no synchronisation check will be carried out.

In all applications, the VTS function will be blocked if any of quality flags of the 6 voltage channels is ‘Invalid’.

2.39.3 DFI machine start-up

The start-up of the induction machine in motor mode is done with the converter feeding the rotor with the stator short circuited. The difficulty of this operating condition is the high rotor voltage of the induction machine. The induction machine must be started-up with a very high flux weakening not to exceed the maximum output voltage of the inverter and the rotor insulation. At such high flux weakening the maximum torque is limited by the pull out torque of the machine. Due to the high flux weakening the pull out torque is in the same order of magnitude as when the machine is reaching its nominal speed. During this start-up period the stator frequency is low (typically <5Hz) and the rotor frequency is ramping up from DC to near nominal speed. The time needed for starting up the machine depends on the available pull out torque, the load torque and the inertia of the drive train. Once the machine speed is reaching the minimum speed for the doubly-fed operation mode, the machine is demagnetized and the inverter pulses are inhibited for a short time to bring the stator current to zero. After this is achieved the stator ground switch is opened and the inverter magnetizes the machine completely from the rotor side and synchronizes the stator voltage with the grid voltage very quickly (<0.5s) and then the stator switch is closed and normal operation is started.

When the machine is started, the stator is short circuited and the converters feed the rotor, so the machine is operating like an inverse squirrel cage induction motor. During the

start-up condition of the machine in pump mode the stator currents will be negative phase sequence because there is 'negative' torque (nr > ns). During the start-up condition of the machine in generator mode the stator current will be positive phase sequence because there is positive torque (nr < ns).

Slip = (ns-nr)/ns

ns = stator frequency

nr = mechanical rotor frequency

2.39.4 Stator protection overview

2.39.4.1 Stator protection (P342-6)

The stator side protection requirements of a variable speed machine are very similar to a conventional synchronous machine. Some protection functions need to be modified; for example, the pole slipping can be disabled and the field failure protection settings need more consideration.

The standard generator protection relay provides adequate stator protection for the variable speed machine using conventional CTs and VTs to provide protection over the frequency range 5-70Hz. The relay can also be used where low frequency injection 100% stator earth fault protection is required. This provides earth fault protection when the machine is at standstill and during start-up/run- down.

In addition to standard protection requirements, increased integration of renewable power generation (e.g. wind farms) into power networks has resulted in the evolution of grid codes with new protection requirements. Many new power system transmission codes require generators to remain stable and connected on-line to the network when faults occur on the transmission network. Otherwise, the power system would be exposed to a greater loss of generation and unless enough reserve capacity from other power plants can balance the generation shortfall, the consequences include danger of a rapid drop in system frequency, necessitation of load shedding and ultimately system collapse. This is known as fault ride-through capability (FRT). An example fault ride through characteristic is shown in Figure 73. Generators are required to stay on line while the voltage is depleted for a fault at the Generating Station HV bus or further downstream from the station on the transmission lines. Complete loss of voltage at the generator terminals prevents prime mover power transmission which can only be transient in nature (hundreds of ms).

To match the complex and country specific fault ride through characteristics, new user programmable curves are included in the P34x for undervoltage protection, see section 2.8. A user friendly tool is used to create curves either by formula or by entering up to 256 data points which are then downloaded to the relay. Protection functions used to provide back-up protection for system faults such as underimpedance and voltage dependant overcurrent protection can be set with appropriate time delays and settings to prevent operation for fault ride through requirements. Alternatively, the protection timer can be blocked by the the inverted start signal of the FRT undervoltage characteristic in PSL if required.

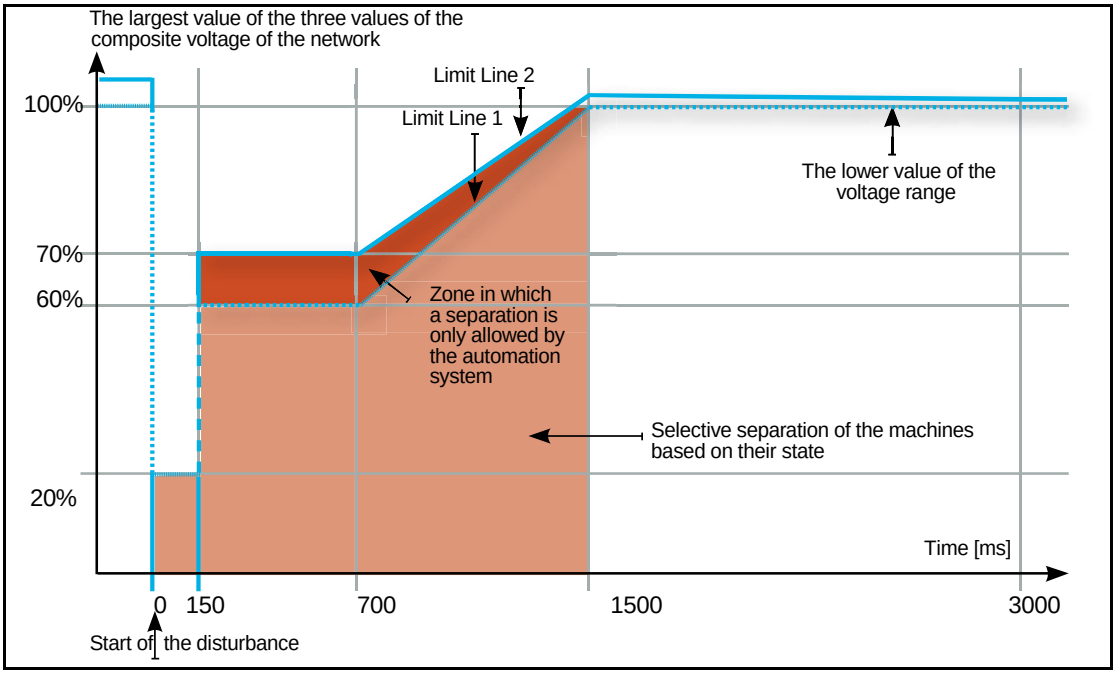


Figure 73: Example transmission code fault ride through limits

2.39.4.2 Stator protection (P348)

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Relays and electromagnetic instrument transformers commonly available on the market are unable to provide suitable generator protection at frequencies lower than 5Hz. To achieve low frequency measurements <5Hz requires NCITs which are connected to the relay using an IEC 61850-9-2 LE interface. Also, new filtering, frequency tracking and protection algorithms (Peak and RMS) are required for the low frequency signal acquisition, see Operation chapter.

A new relay, P348, has been designed to use NCITs, which includes stator Peak and RMS overcurrent and RMS negative phase sequence overcurrent protection for frequencies of 0.1 to 70Hz and which provides protection during machine start-up, run-down where the standard generator protection is not active and also during normal operation. Stator CT supervision is also provided to supervise the NPS (Negative Phase Sequence) overcurrent protection. See sections 2.39.6.2, 2.39.6.3 and 3.3.3 for more information on these functions.

2.39.5 Rotor protection overview (P348)

Variable speed machine rotors have a three-phase winding with slip rings supplied with low frequency currents by means of voltage source converters from the AC system. The rotor power supply frequency is generally between 0.1Hz and 6 Hz during normal running and can reach up to the power system frequency (50 or 60 Hz) during machine run-up and run-down.

For the rotor protection, NCITs are required to achieve low frequency measurements <5Hz, the same as for the low frequency stator protection. New filtering, frequency tracking and protection algorithms have also been developed for the low frequency signal relay, P348, acquisition, see Operation chapter.

A new relay has been designed to use NCITs to provide rotor Peak and RMS overcurrent, Peak and RMS overvoltage, RMS neutral voltage and overfrequency protection from 0.1Hz to 70Hz. Non-conventional rotor NCVT supervision using a voltage balance scheme, where redundant rotor VTs are provided, is used to block the rotor neutral voltage protection. See sections 2.39.6.2, 2.39.6.3, 2.39.6.4, 2.39.6.5, 2.39.6.6 and 3.2.2 for more information on these functions.

Rotor thermal protection can be provided with rotor temperature monitoring sensors connected to the P34x 4-20mA inputs.

Rotor earth fault protection can be provided using the P345 via a low frequency (LF) injection technique as used for 100% stator earth fault. See section 2.39.6.1, for more information on this function.

2.39.6 Protection functions for variable speed machines

2.39.6.1 100% rotor earth fault protection (64R)

Rotor earth fault protection can be provided using the P345 via a low frequency (LF) injection technique as used for 100% stator earth fault. This provides protection for the entire rotor winding and all electrically connected equipment (including rotor leads, isolated phase bus between VSI and Rotor) against ground faults. It also provides earth fault protection while the machine is at standstill up to normal running. The signal injection frequency (20Hz) has been chosen to prevent interference between the normal rotor slip frequency and converter supply frequency.

The protection system injects a 20Hz voltage at the neutral grounding device located between the VSI and the rotor winding and measures the injected 20Hz voltage and the 20Hz current flowing in the neutral to ground resistance, RN.

During normal operating conditions (without ground faults), only a small amount of 20Hz current will flow in the neutral grounding device as a result of high impedance of the rotor circuit phase-to-ground capacitance at low frequencies ($Xc = 1/2\pi fc$). When a ground fault occurs in the machine rotor windings (or an adjacent component), the 20Hz current will increase due to the lower impedance earth path and the resulting insulation resistance will decrease. From the injected voltage and fault current the relay can determine the fault resistance.

From the measured current and voltage vectors the complex impedance can be calculated and from this the ohmic resistance is determined. This eliminates disturbances caused by the rotor earth capacitance and ensures high sensitivity. The relay algorithm can take into account a transfer resistance **64S Series R**, that may be present at the neutral or earthing voltage transformer. An example of the series resistance is the total leakage resistance of the earthing transformer, through which the injected voltage is applied to the generator neutral. The algorithm can also account for parallel resistance, **64S Parallel** G (G = 1/R). Other error factors can be taken into account by the angle error compensation, **64S Angle Comp**.

The relay includes a 20Hz overcurrent element which can be used as a back-up to the 20Hz under resistance protection. The overcurrent element is not as sensitive as the under resistance elements as it does not include any transfer resistance compensation or any compensation for capacitance affects.

In addition to the determination of the earth resistance, the P348 relay also includes neutral voltage protection as a back-up to the 100% stator earth fault protection, see section 2.39.6.5. The neutral voltage protection is calculated from the 3 phase voltage inputs and can be used to provide rotor earth fault protection and is active during the run-up and run-down of the generator.

The 100% rotor earth fault protection includes 2 stages of under resistance protection for alarm and trip and an overcurrent protection stage, with each stage having a definite time delay setting. The protection includes a supervision element to evaluate a failure of the low frequency generator or the low frequency connection.

The neutral grounding circuit is composed of 4 resistances (3 phase-to-neutral resistances - RP and 1 neutral to ground resistance - RN), see Figure 74. The calculation of the resistances RP and RN is described below.

The relay earth fault current and voltage inputs have a dedicated band pass filter and low pass filter which provides aggressive filtering of the low frequency rotor signals and PWM voltage signal in particular. The bandpass filter is normally automatically disabled after the machine start-up (frequency >45Hz) but should be permanently enabled for this application as there are many harmonics present from the PWM signals. DDB 555, 64S Filter On should be ON to enable the bandpass filter permanently in the PSL.

Note: A brush is required to ground the rotor shaft. This brush should be sized to accommodate 20 Hz injected current otherwise this current will flow through the bearings.

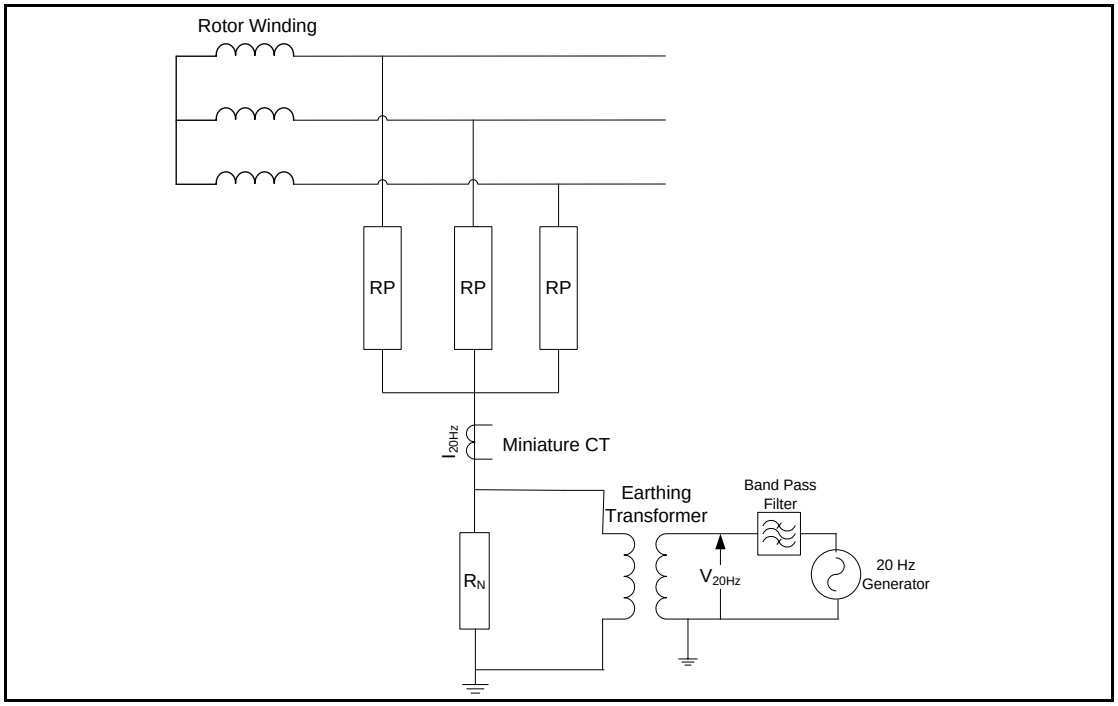


Figure 74: Rotor earth fault injection circuit

Where

R_P Loading resistor

R_N Earthing resistor

V_{20Hz} Displacement voltage at the protective relay

I_{20Hz} Measuring current at the protective relay

2.39.6.1.1 Calculation of R_P and R_N

Figure 74 shows the connection diagram for the rotor earth fault protection by low frequency injection scheme. The resistances values R_P and R_N must fulfill the following condition in order to limit the transient overvoltage to <300% of the peak phase-to-ground rotor voltage during an intermittent rotor earth fault condition (IEEE Standard C62.92 Part 2: Grounding of synchronous generator systems):

$R_P + 3 \times R_N < 2Xc$

Where $Xc = 1/2\pi fC$, where C is the total phase-to-ground capacitance of the rotor circuit.

Also, R_P and R_N are selected to limit the maximum voltage across the neutral resistance to 500V during rotor earth faults.

As an example if C = 2.88µF

The minimum capacitive reactance of the rotor circuit is obtained at 50Hz and is:

$Xc = 1/2\pi \times 50 \times 2.88 \times 10^{-6} = 1.15K\Omega$

Therefore, $R_P + 3 \times R_N < 2.3\ K\Omega$

To limit the maximum voltage across the neutral resistance to <500V.

$V_{ph-G} \times 3R_N/(3R_N + R_P) < 500V$

If $V_{ph-G} = 4000/\sqrt{3}$ (maximum phase-ground voltage during start-up)

$R_N < (500/4000/\sqrt{3}) \times 2300/3 = 166\Omega$

If $R_N = 140\Omega$

Then $R_P = 2300 - (3 \times 140) = 1880\Omega$

Phase resistance characteristics (R_P)

The selected value of the phase resistance is 1880Ω.

The losses dissipated in the 3 phase resistances R_P during normal operation (assuming the maximum rated phase voltage, Vmax is 3kV rms ph-ph, during normal operation) are:

P (kW) = 1000 x $(3kV)^2$/1880 = 4.8kW (3 phase value)

The losses dissipated temporarily in the phase resistances R_P during the starting sequence when the maximum rotor voltage is 4 kV are:

P (kW) = 1000 x $(4kV)^2$/1880 = 8.5kW (3 phase value)

The maximum current in the phase resistances, Ip, during normal operating conditions (Vmax = 3 kV rms ph-ph) is:

Ip = 3kV/(√3 x1880) = 0.92A

Selected continuous rating is 2A

Neutral resistance characteristics (RN)

The selected value of the neutral resistance is 140Ω

During rotor earth fault conditions, the maximum current in the neutral resistance is equal to 2.3A

The selected current rating is 5 A (Duration: 10s)

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2.39.6.1.2 Neutral CT requirements

The current transformer which is located in the grounding connection of the neutral grounding device is used to measure the 20 Hz current. This CT is designed not to saturate during rotor earth fault conditions when the voltage across the neutral resistance increases. Class 5P is recommended for this CT.

If the maximum rotor frequency when the unit is connected to the HV grid is 4 Hz and at this frequency the rotor voltage is 3 kV (rms ph-ph).

If a rotor earth fault occurs during such operating conditions, the zero sequence component V_N of the rotor voltage will be:

V_N = 3000/√3 = 1732 V

Consequently, the voltage across the neutral resistance, Vneutral, will be:

Vneutral = V_N x 3 R_N / (3 R_N + R_P) = 1732 x 3 x 140 / (3 x 140 + 1880) = 316 V.

Therefore, the neutral current, Ineutral, (at 4Hz) will be:

Ineutral = Vneutral / R_N = 316/140 = 2.3 A.

The CT characteristics required to avoid the saturation of the neutral CT are:

V_K = 2 x (R_{CT} + 2 R_L + R_R) x Ifn

Where:

V_K = Neutral CT knee-point voltage

R_{CT} = Neutral CT secondary winding resistance, R_{CT} = 0.1 Ohm (Assumed value)

R_L = Wiring resistance (between CT and relay), 2 x RL = 0.33 Ohm (Considering wiring length : 2 x 50 meters - Wiring cross section : 6 mm^2)

R_R = P345 Relay input impedance, R_R < 0.04 Ohm (1A)

Ifn = Maximum secondary earth fault current

Primary current of CT must be chosen greater than the maximum neutral current. In this example, Ineutral maximum is 2.3 A. Therefore, primary current is selected to be 20 A and secondary current is selected to be 5A.

Ifn = 2.3 x 5/20 = 0.575A (The P345 64S,1A relay input can be used as the linear range of the current input is 0-2In).

Notes: The linear range of the 100% rotor earth fault input is up to 2 In. So if the earth fault current is limited to <2A then the 100% stator earth fault 1A input can be used. For earth fault currents 2-10A the relay 5A current input can be used.

For the 5A inputs the 64S I Magnitude measurement in the Measurements 3 menu will show 5 times lower current than being injected. There is no CT ratio setting for the 100% stator earth fault current input, however the resistance measurement and 64SR<1/2 protection can be compensated by the 64S R Factor setting if the 5A input is used by multiplying the CT ratio by 5 in the formula for the R factor. If the 64S I>1 protection is used then the setting needs to be divided by a factor of 5 when using the 5A input.

Therefore, the minimum required knee-point voltage is:

V_K = 2 x (0.1 + 0.33 + 0.0.4) x 0.575 = 0.54 V.

This condition must be fulfilled at 4 Hz.

The characteristics of the neutral current transformer are:

CT Ratio = 20/5A, VA = 10VA, 5P10, R_{CT} = 0.1 Ohm.

The knee-point voltage at 50 Hz of this current transformer is:

V_K = (VA x ALF) / In + ALF x In x RCT = (10 x 10) / 5 + 10 x 5 x 0.1 = 25 V

where ALF is the Accuracy Limit Factor.

As the knee-point voltage is proportional to the power frequency, the knee-point voltage of this CT at 4 Hz will be equal to:

V_K = 25 x 4 / 50 = 2V > 0.54 V required.

Therefore, the CT will not saturate and is suitable for this application.

Note: If a rotor earth fault occurs at a lower frequency (< 4 Hz), the neutral current and the CT knee-point voltage that the CT can deliver will be reduced as the frequency reduces and the non saturation condition will still be fulfilled. This is because the rotor voltage varies with the rotor frequency and in a similar way the CT knee point voltage is also proportional to the frequency.

2.39.6.1.3 Neutral VT requirements

A VA rating of 3kVA (20s), accuracy class 0.5 is recommended the same as for stator 100% earth fault applications.

As seen from Figure 74, the 20Hz current I_{20Hz} is measured from the primary side of the neutral VT and the 20Hz voltage V_{20Hz} from the secondary side. An assumption taken in calculating the fault resistance from the I_{20Hz} and the V_{20Hz} is that the impedance between the primary and secondary windings, which is the VT leakage reactance, is negligible. The VA rating of 3000VA has been selected to minimize the leakage reactance.

The ratio of the VT is selected to 500/200V to limit the maximum voltage to the P345 voltage inputs <200V during rotor earth fault conditions. The P345 relay voltage inputs have a linear range 0-200V and can withstand continuously 2Vn.

The reference frequency for the voltage rating of the neutral VT is based on the maximum rotor frequency in operation (4Hz in the example).

2.39.6.1.4 Setting guidelines for 100% rotor earth fault protection – Does this need to be separate or together from section above?

The settings guidelines for the 100% rotor earth fault protection are practically the same as for the 100% stator earth fault protection described in section 2.21.1.

The main difference is that the bandpass filter (DDB 555, 64S Filter On) should be permanently enabled in the PSL.

The 100% rotor earth fault protection element can be selected by setting the **64S 100%St EF** cell to **Enabled**.

The **64S R Factor** is set as described below.

During the primary tests the correction angle (**64S Angle Comp**) and the ohmic transfer resistance (**R Factor**) of the voltage transformer must be determined and set.

The primary resistance and conversion factor for the resistance (**R Factor**) is calculated as follows:

$$R_{Primary} = VT_{Ratio} x \frac{V_{Divider\ Ratio}}{CT_{Ratio}} x R_{Secondary}$$

Using the data shown in the example above, VT ratio is 500/200V, CT ratio is 20/5, voltage divider is 1:1 and assuming the 1A rated current input is used,

$$R_{Primary} = (\frac{500}{200}) x \frac{5}{20} x R_{Secondary}$$

Therefore,

$$R_{Factor} = 0.625$$

The under resistance alarm threshold, **64S Alarm Set**, must be set below the level of resistance present under normal conditions. This resistance can be determined by viewing the **64S R** cell in the **MEASUREMENTS 3** menu. A typical value for the primary fault resistance alarm setting is between 200-300 Ω.

The under resistance trip threshold, **64S R<2 Trip Set**, must be set below the level of resistance present under normal conditions. This resistance can be determined by viewing the **64S R** cell in the **MEASUREMENTS 3** menu. A typical value for the primary fault resistance trip setting is between 100-200 Ω .

The overcurrent trip threshold, **64S I>1 Trip Set**, must be set above the 20Hz level of current present under normal conditions. This secondary current can be determined by viewing the **64S I Magnitude** cell in the **MEASUREMENTS 3** menu.

A time delay for these elements can be set in the **64S R<1 Alm Dly, 64S R<2 Trip Dly** and **64S I>1 Trip Dly** cells. The default time delays provide typical values.

If the 20 Hz voltage drops below the voltage supervision threshold, **64S V<1 Set** and the 20 Hz current remains below the current supervision threshold, **64S I< Set**, there must be a problem with the 20 Hz connection. The default settings for 64S Supervision element, **64S V<1 Set** (1 V) and **64S I<1 Set** (10 mA) will be adequate for most applications. Where the earthing resistor is less than 1 Ω, the supervision voltage threshold, **64S V<1 Set**, must be reduced to 0.5 V, the supervision current threshold, **64S I<1 Set**, can be left at 10 mA.

The **Comp Angle** setting is used to compensate the angle errors between the CT and earthing or neutral transformer. The setting can be found from primary testing.

The **64S Series R** setting is used to account for the transfer resistance of the earthing or neutral voltage transformer and the phase resistance RP of the rotor grounding circuit. The setting can be estimated from calculation or from primary testing, see section 2.22.3. The **64S Parallel G** setting can be used to account for additional parallel loading resistance. The default setting is 0, no additional loading resistor which will normally be the situation for rotor earth fault applications.

For rotor earth fault protection the lead resistance between the earthing transformer and the 20 Hz generator/bandpass filter can have a significant affect on the accuracy of the measured resistance by the relay. So if the 20 Hz generator and bandpass filter are mounted in the protection cubicle the loop lead resistance should ideally be kept below 0.5 Ω. If the 20 Hz generator and bandpass filter are mounted near the earthing transformer then this will keep the errors to a minimum. The lead resistance from the 20 Hz generator/banpass filter to the relay does not significantly affect the accuracy of the measured resistance.

2.39.6.2 Phase fault overcurrent protection (50/51)

Four stages of non-directional Peak overcurrent and four stages of RMS overcurrent protection are provided in the P348 relay. Each stage can be selected to measure the rotor (**IA-1/IB-1/IC-1**) or stator (**IA-2/IB-2/IC-2**) 3 phase current inputs using the **I>x CT Source** setting.

The first two RMS stages have a time delayed characteristic that can be set as either Inverse Definite Minimum Time (IDMT) or Definite Time (DT) or a user curve. The third and fourth stages have a definite time delay, which can be set to zero to produce instantaneous operation. Each stage can be selectively enabled or disabled.

Each of the four Peak stages have a definite time delay, which can be set to zero to produce instantaneous operation. Each stage can be selectively enabled or disabled. To improve the protection stability, a count strategy is applied to all Peak protection stages, where the stage timer does not start until the protection criteria are satisfied for n consecutive protection iterations (the peak stages execute a protection iteration (cycle) every two samples). The count target n is settable for each protection stage using the **SV Iterations** setting.

Each rotor RMS overcurrent stage is blocked when the frequency is below the **RMS F< Block** threshold in the **System Config** menu.

The P348 stator RMS and Peak overcurrent stages can be used to provide time delayed back-up protection for system and generator faults and high set fast operating protection for machine faults. The Peak overcurrent stages if set to instantaneous can provide faster protection than the RMS overcurrent protection in the P348 and Fourier based overcurrent protection used in other Px4x relays. Typically, voltage dependant overcurrent, underimpedance, NPS overcurrent and overcurrent protection are also used in the main stator protection (e.g. P345) for time delayed back-up protection of power system phase faults and machine phase faults.

The rotor Peak and RMS overcurrent stages can be used to provide time delayed protection and high set fast protection for rotor 3 phase and phase to phase faults.

2.39.6.2.1 Application of timer hold/reset time facility

The timer hold/reset feature may be useful in certain applications of the RMS protection (I>5/6), for example when grading with electromechanical overcurrent relays which have inherent reset time delays.

Another situation where the timer hold facility may be used to reduce fault clearance times is where intermittent faults may be experienced. When the reset time of the RMS overcurrent relay is instantaneous the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the timer hold facility the RMS protection will integrate the fault current pulses, thereby reducing fault clearance time.

Each peak overcurrent stage in the P348 relay includes a timer hold facility, which may either be set to zero or to a definite time value. The timer hold facility can be found for all peak overcurrent stages as settings **I>1/2/3/4 tRESET**.

An issue to be considered with the peak overcurrent based protection is that the relay contact can chatter and a large number of event records can be generated for a sinusoidal waveform. One way of preventing chattering is to set a drop off or reset delay.

The **I>x tReset** setting should be set to a value larger than half the cycle period of the lowest frequency considered, which is the longest possible off time. Thus, the Start or Trip signal will not reset until the fault has been cleared.

2.39.6.2.2 Setting guidelines for stator overcurrent protection (50/51S)

The first and second stage of RMS overcurrent protection can be selected by setting **I>5/6 Function** to any of the inverse or DT or user curve settings or disabled. The third and fourth definite time RMS overcurrent stages can be enabled or disabled using the **I>7/8 Status** setting **Enabled**, **Disabled**. Each definite time Peak overcurrent stage can be enabled or disabled using the **I>1/2/3/4 Status** setting **Enabled**, **Disabled**.

The **I>x CT Source** setting should be set to IA-2/IB-2/IC-2 for any RMS or Peak overcurrent stages used for stator overcurrent protection.

The **SV Iterations** setting for the Peak overcurrent protection stages should be set so that the protection doesn't operate for spurious very short spikes. The default value of 3 iterations is recommended.

One of the stator RMS overcurrent (I>5/6/7/8) and one of the stator Peak overcurent stages (I>1/2/3/4) can be used to provide back-up protection for stator faults on the generator and the system. As such it should be coordinated with downstream protection and back-up protection in the main stator protection relay (eg P345) to provide discrimination for system faults, setting the current threshold (**I>5/6 Current Set** (RMS) and **I>1/2/3/4 Current Set** (Peak)), and the time delay accordingly.

I>5/6 TMS – For IEC curves;

I>5/6 Time Dial – For US/IEEE curves;

I>1/2/3/4 Time Delay (Peak), **I>5/6 Time Delay** (RMS) – For definite time.

If a non standard time characteristic is required a user programmable curve can be used for I>5/6 RMS overcurrent protection stages.

Typically, voltage dependant overcurrent, underimpedance, NPS overcurrent and overcurrent protection are used in the main P34x stator protection for time delayed back-up protection of power system phase faults and machine phase faults.

For the Peak overcurrent protection the **I>x tReset** setting should be set to a value larger than half the cycle period of the lowest frequency considered to prevent chattering.

To provide back-up protection for the generator and system, the element must be supplied from CTs connected in the generator tails (neutral). If terminal end CTs are used, the element will provide protection for the system only, unless the generator is connected in parallel to a second source of supply.

Where terminal CTs are used, one of the stator RMS overcurrent (I>5/6/7/8) and one of the stator Peak overcurent stages (I>1/2/3/4) can be set as an instantaneous overcurrent protection, providing protection against internal faults on the machine. The current setting **I>x Current Set**, could be set to 120% of the maximum fault rating of the generator, typically 8 x full load current. The operating time, **I>x Time Delay**, should be set to 0s to give instantaneous operation. The protection will therefore be stable for external faults where the fault current from the generator will be below the stage current setting. For faults within the machine, the fault current will be supplied from the system and will be above the current setting, resulting in fast clearance of the internal fault.

During the machine start-up in motor mode the stator is normally shorted so the stator overcurrent protection is not sensitive to any faults on the stator.

2.39.6.2.3 Setting guidelines for rotor overcurrent protection (50/51R)

The RMS overcurrent (I>5/6/7/8) and Peak overcurrent protection can be set to provide rotor protection in a similar way to the stator protection decribed above.

The RMS is calculated over a one-cycle rolling window. So at lower frequencies, the RMS current will take longer to ramp up to above the setting especially for lower fault currents. If very fast operating time is required, then the Peak stages are better.

The **I>x CT Source** setting should be set to **IA-1/IB-1/IC-1** for any RMS or Peak overcurrent stages used for rotor overcurrent protection.

For the Peak overcurrent protection the **I>x tReset** setting should be set to a value larger than half the cycle period of the lowest frequency considered to prevent chattering.

The **SV Iterations** setting for the Peak overcurrent protection stages should be set so that the protection operates only for prolonged fault currents. The default value of 3 iterations is recommended.

When the machine is connected to the grid during a rotor or stator or close up power system 3 phase or phase to phase fault the rotor and stator currents will both increase to many multiples of load current. So, it is difficult to achieve discrimination for stator and rotor faults using the current setting alone.

The stator fault currents vary according to the slip frequency during rotor faults increasing with rotor frequency. So it is difficult for the stator protection to discriminate between a stator fault and rotor fault using the current setting alone especially at high rotor slip frequencies.

The rotor and stator are usually both high impedance earthed so an earth fault on the stator or rotor will not cause a noticeable change in the stator or rotor currents and so these faults can not be detected by the overcurrent protection.

During a phase-phase rotor fault the healthy phase may also see some fault current due to the mutual inductance between the three rotor phases. The current on the healthy phase induced by the faulted phases is linearly dependant on the slip frequency. Thus, the rotor overcurrent protection may not be able to discriminate between phase-phase and 3 phase faults.

The rotor RMS and Peak overcurrent protection can be used as back-up protection and time delayed to co-ordinate with the stator system back-up and stator protection to avoid tripping for system and stator faults in a similar way to the stator overcurrent protection described above. The current setting **I>x Current Set** should be set >120% of maximum rotor current.

During a rotor phase fault the rotor voltage will reduce to a small value on the faulted phase and during a stator phase fault the rotor voltage will increase to a large value and will probably cause the crowbar to operate. For a fault on a grid the rotor voltage may also increase to a value that may cause the crowbar to operate if the protection does not trip quickly. Therefore, discrimination between stator and rotor phase faults can be achieved by blocking the rotor overcurrent protection with a signal from the peak rotor overvoltage protection in PSL. Thus, fast operating rotor Peak and RMS overcurrent protection can be achieved for rotor phase faults by blocking the rotor Peak and RMS overcurrent protection using **I>x Peak/RMS Inhibit** signals (DDB 568-575) with a start signal from the rotor peak overvoltage protection, **V>1/2 Peak Start** (DDB 1094, 1098) in the PSL. It is recommended the **V>1/2 SV Iterations** setting should be set to 3 so that the **V>1/2 Peak Start** operates quickly before the crowbar. A short delay on drop-off time should be applied to the **V>1/2 Peak Start** signals to coordinate with stator and system protection to ensure rotor overcurrent blocking is maintained until the stator/system protection has operated. The drop-off time delay should also take into account the rotor fault current withstand time. The **V>1/2 Voltage Set** should be set to 120% of the nominal phase-phase voltage at maximum normal rotor frequency. The overvoltage protection should be set to operate from **Phase to Phase** voltage as selected by **V> Measur't Mode** cell. Single phase operation can be selected in **V> Operate Mode** cell by selecting the **Any Phase** setting so that the element will operate if any phase voltage is above setting. The operating time, **I>x Time Delay**, should be set to at least 10ms to give time for the overvoltage blocking logic to operate before the overcurrent trip for stator faults.

During the machine start-up in motor mode a 3 phase and phase-phase fault on the rotor will cause the rotor and stator currents to reduce quickly over a few seconds to a small value as there will be a short on the stator for starting and a short on the rotor from the fault. So, the stator and rotor overcurrent protection are not sensitive to rotor phase faults and can be disabled during the machine start-up.

2.39.6.3 Stator negative phase sequence (NPS) overcurrent protection (46S)

The P348 relays provide four non directional independent stages of RMS negative phase sequence stator overcurrent protection. Each stage has a current pick up setting **I2>1/2/3/4 Current Set**, and is time delayed in operation by an adjustable timer **I2>1/2/3/4 Time Delay**. The 3 phase current source is fixed to using the **IA-2/IB-2/IC-2** inputs on the stator. Each stator RMS NPS overcurrent stage is blocked when the frequency is below the **RMS F< Block** threshold in the **System Config** menu.

When applying traditional phase overcurrent protection, the overcurrent elements must be set higher than maximum load current, thereby limiting the element's sensitivity. Most protection schemes also use an earth fault element, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes.

Any unbalanced fault condition will produce negative sequence current of some magnitude. Therefore a negative phase sequence overcurrent element can operate for both phase-phase and phase-earth faults (solidly earthed systems). For variable speed machines the stator is usually high impedance earthed so an earth fault on the stator will not cause a noticeable change in stator currents and NPS currents.

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The following section describes how negative phase sequence overcurrent protection may be applied in conjunction with standard overcurrent and earth fault protection to alleviate some less common application difficulties.

- Negative phase sequence overcurrent elements give greater sensitivity to resistive phase to phase faults, where phase overcurrent elements may not operate. Voltage dependent overcurrent and underimpedance protection is commonly used to provide more sensitive back-up protection for system phase faults on a generator than simple overcurrent protection. However, negative phase sequence overcurrent protection can also be used to provide sensitive back-up protection for phase-phase faults.

  Note: NPS overcurrent protection will not provide any system back-up protection for three-phase faults.

- In certain applications, residual current may not be detected by an earth fault relay due to the system configuration. For example, an earth fault relay applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side.

  However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore a negative phase sequence overcurrent element may be employed to provide time-delayed back-up protection for any uncleared asymmetrical faults downstream.

- For rotating machines a large amount of negative phase sequence current can be a dangerous condition for the machine due to its heating effect on the rotor. Therefore a negative phase sequence overcurrent element may be applied to provide back-up protection to the negative phase sequence thermal protection that is normally applied to a rotating machine, see section 2.15.

- It may be required to simply alarm for the presence of negative phase sequence currents on the system. Operators may then investigate the cause of the unbalance.

For variable speed machines the NPS stator overcurrent protection in the P348 can be used to provide back-up to the NPS stator overcurrent protection in main stator protection relay e.g. P345, when the machine is connected to the grid.

The main use of the NPS stator overcurrent protection is to provide detection of phase-phase faults in the rotor and open circuit faults in the stator when the machine is starting. When the machine is starting the stator currents may be standard phase rotation or reverse phase rotation depending on if the machine is starting in pump or generator mode. The System Config settings - Standard ABC and Reverse ACB can be used in 2 of the

Setting Groups to change the phase rotation depending on the starting mode of the machine. In this way the NPS current calculation can be correctly calculated so that it is small during the start-up sequence and will increase for a phase-phase fault. See section 2.39.3 for more information on variable speed machine starting.

2.39.6.3.1 Setting guidelines for stator NPS overcurrent protection

Each definite time NPS overcurrent stage can be enabled/disabled using the **I2>1/2/3/4 Status** setting **Enabled, Disabled**.

The current pick-up threshold setting, **I2>1/2/3/4 Current Set**, must be set higher than the negative phase sequence current due to the maximum normal load unbalance on the system when used as back-up to the main stator NPS overcurrent protection for detection of power system faults. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence current (**I2 CT2 RMS**), and setting at least 20% above this figure.

Where the negative phase sequence element is required to operate for specific uncleared asymmetric system faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

If the required fault study information is unavailable, the setting must adhere to the minimum threshold previously outlined, employing a suitable time delay for coordination with downstream devices. This is vital to prevent unnecessary interruption of the supply resulting from inadvertent operation of this element.

As stated above, correct setting of the time delay, **I2>1/2/3/4 Time Delay**, for this function is vital. It should also be noted that this element is applied primarily to provide back-up protection to other protective devices or to provide an alarm. Therefore in practice, it would be associated with a long time delay if used to provide back-up protection or an alarm.

Where the protection is used for back-up protection or as an alarm it must be ensured that the time delay is set greater than the operating time of any other protective device (at minimum fault level) on the system which may respond to unbalanced faults, such as:

- Phase overcurrent elements
- Earth fault elements
- System back-up protection - voltage dependent overcurrent/underimpedance
- Broken conductor elements
- Negative phase sequence influenced thermal elements

For stator 3 phase and phase-phase faults if there is a large DC offset in the fault current this can cause large NPS current to be measured by the P348 sample based NPS overcurrent algorithm. The conventional Fourier based stator NPS overcurrent protection in the main stator protection relay such as the P345 can provide protection 5-70Hz and the Fourier algorithm will provide better accuracy with filtering of the DC component. So it is recommended that if NPS overcurrent protection is required when the machine is connected to the grid, the P342-6 NPS overcurrent protection is used as the main protection and the P348 NPS overcurrent protection is disabled or set with a long time delay to co-ordinate with other other protective device (at minimum fault level) on the system which may respond to unbalanced and balanced faults.

During the machine start-up in motor mode the stator is normally shorted so the stator overcurrent and NPS overcurrent protection will not be able to detect any stator short circuit faults. However, the stator NPS overcurrent protection can be used to detect stator open circuit and rotor phase-phase fault conditions. The current pick-up threshold, **I2>1/2/3/4 Current Set**, must be set higher than the negative phase sequence current due to the maximum unbalance during machine start-up when used for machine start-up rotor protection. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence current (**I2 CT2**

RMS), and setting at least 20% above this figure. NPS current similar in magnitude to a phase-phase fault can be measured by the NPS sample based algorithm for a 3 phase rotor fault due the DC offset of the 3 phase fault and the way the sample value based algorithm works. The stator phase currents and NPS currents decay after a few seconds for a 3 phase and phase-phase rotor fault. Therefore, to provide fast protection for stator open circuit and rotor short circuit faults, a short time delay, <1s, e.g. 0s, **I2>1/2/3/4 Time Delay**, should be used. However, as explained above discrimination between detection of 3 phase and phase-phase faults will not be possible.

To avoid coordination problems with the stator and system backup protection when the machine is connected to the grid the NPS overcurrent protection should be blocked or disabled or the pick-up and operating time settings changed after the start-up sequence before synchronizing with the grid. Disabling the NPS overcurrent protection or changing the settings after the start-up sequence can be achieved by changing setting groups.

When the machine is starting the stator currents may be standard phase rotation or reverse phase rotation depending on if the machine is starting in pump or generator mode. During the start-up sequence the **System Config** settings - Standard **ABC** or **Reverse ACB** can be selected as required in 2 of the Setting Groups to change the phase rotation. See Operation chapter, section 2.12 for more information on changing setting groups.

2.39.6.4 Rotor overvoltage protection (59R)

The rotor overvoltage protection included within the P348 relay consists of two independent stages of RMS (V>3/4) and two independent stages of peak (V>1/2) overvoltage protection. Each peak overvoltage stage has a **SV Iterations** setting for the number of protection iterations required above setting to start.

AP

Each rotor RMS overvoltage stage is blocked when the frequency is below the **RMS F< Block** threshold in the **System Config** menu.

In variable speed machines a large voltage increase of 3-5 times the pre-fault voltage level can occur in the rotor for stator phase to phase faults and three phase faults, which will probably cause the crowbar to operate. For a fault on a grid the rotor voltage may also increase to a value that may cause the crowbar to operate if the protection does not trip quickly. The rotor phase to neutral voltage also increases up to the phase to phase level for rotor earth faults as the rotor is usually high impedance earthed.

The rotor voltage increases with rotor frequency and so the overvoltage is higher for stator faults at higher rotor frequencies. All phases have similar increases in voltage for stator 3 phase and phase to phase faults. During a phase to phase stator fault the healthy rotor phase sees the same fault voltage as the other phases due to the mutual inductance between the three rotor phases.

The P348 overvoltage protection should be set to prevent possible damage to generator rotor insulation. The power electronic converter protection includes overvoltage protection which operates a crowbar as a last resort to short out the rotor to protect the power electronic converter. The P348 is required to provide overvoltage protection for the machine rotor primarily.

During the machine start-up a rotor phase-phase or 3 phase fault will cause an undervoltage condition in 2 or more phases of the rotor. One of the RMS overvoltage protection stages V>3/4 can be used to detect this condition by inverting the overvoltage start signal in PSL and using this element for undervoltage protection. This functionality can be enabled by using different PSL for the machine start-up using the setting groups which can be changed using a digital input. This protection logic used during machine start-up will need to be blocked when the machine is offline.

2.39.6.4.1 Setting guidelines for rotor overvoltage protection

The peak overvoltage stages 1 and 2 (V>1/2) are DT only and are **Enabled/Disabled** in the **V>1/2 status** cell.

The RMS is calculated over a one-cycle rolling window. So at lower frequencies, the RMS voltage will take longer to ramp up to above the setting. If very fast operating time is

required, then the Peak stages are better. It is unlikely RMS stages will be faster than the crowbar operation.

The **SV Iterations** setting for the Peak overcurrent protection stages should be set so that the protection operates only for prolonged fault currents. The default value of 3 iterations is recommended.

The RMS overvoltage stage 1, (V>3) may be selected as **IDMT**, **Default Curve 1/2/3/4**, **DT** or **Disabled**, within the **V>3 Function** cell. Stage 2 (V>4) is DT only and is **Enabled/Disabled** in the **V>4 status** cell. The time delay for RMS overvoltage (**V>3 TMS** - for IDMT curve; **V>3/4 Time Delay**, for definite time) and Peak overvoltage definite time delay, **V>1/2 Time Delay**, should be selected as required.

For the rotor RMS protection (RMS overcurrent, RMS overvoltage, NVD) the blocking frequency setting **RMS F< Block** in the **System Config** menu should be selected for the required frequency range of protection operation. The measurement sensor accuracy at lower frequencies may be a consideration for this frequency level. The NPS overcurrent protection is also less accurate at very low frequencies for fast changes of frequency. The default setting of 1Hz will be adequate for most applications. The Peak overcurrent and Peak overvoltage protection are not affected by the **RMS F< Block** setting. The Peak overcurrent and Peak overvoltage protection are not affected by this setting.

For the Peak overvoltage protection the **V>1/2 tReset** setting should be set to a value larger than half the cycle period of the lowest frequency considered to prevent chattering.

The overvoltage protection can be set to operate from Phase-Phase or Phase-Neutral voltage as selected by **V> Measur't Mode** cell. Single or three-phase operation can be selected in **V> Operate Mode** cell. When **Any Phase** is selected the element will operate if any phase voltage is above setting, when **Three-phase** is selected the element will operate when all three-phase voltages are above the setting.

Generator insulation can typically withstand a 5% overvoltage condition continuously. The rotor withstand times for higher overvoltages should be declared by the generator manufacturer.

To prevent operation during rotor earth faults, the element should be set to operate from the phase-phase voltages, to achieve this **V>1 Measur't Mode** can be set to **Phase-Phase**. The **V>1 Operating Mode** should be set to **Any Phase** to detect any phase to phase overvoltage.

One stage of the Peak overvoltage threshold, **V>1 Voltage Set** and RMS overvoltage threshold **V>3 Voltage Set** would typically be set to 120% of the nominal phase-phase voltage at maximum normal rotor frequency. The time delay, **V>1 Time Delay**, should be set to prevent unwanted tripping of the delayed overvoltage protection function due to transient over voltages that do not pose a risk to the rotor; e.g. following faults on the power system. The typical delay to be applied would be 1 s - 3 s, with a longer delay being applied for lower voltage threshold settings. For the Peak overvoltage protection the **V>1/2 tReset** setting should be set to a value larger than half the cycle period of the lowest frequency considered to prevent chattering.

Normally, the crowbar will operate very quickly to short out the rotor for large overvoltage conditions. The second stage Peak overvoltage threshold, **V>2 Voltage Set** and RMS overvoltage threshold **V>4 Voltage Set** can be used to provide instantaneous high-set over voltage protection as back-up to the crowbar. The typical threshold setting to be applied, **V>2/4 Voltage Set**, would be similar to the crowbar setting and depend on plant manufacturers' advice. For instantaneous operation, the time delay, **V>2/4 Time Delay**, should be set to 0 s. If phase to neutral operation is selected, care must be taken to ensure that the element will grade with rotor earth faults, where the phase-neutral voltage on healthy phases can rise significantly up to the phase to phase voltage level.

During the machine start-up a rotor phase-phase or 3 phase fault will cause an undervoltage condition in 2 or more phases of the rotor. The RMS overvoltage protection can be configured in PSL to operate as an undervoltage function by inverting the start output DDB to detect these fault conditions. To make this element less sensitive during rotor earth faults, the element should be set to operate from the phase-phase voltages, to achieve this **V>1 Measur't Mode** can be set to **Phase-Phase**. The **V>1 Operating Mode** should be set to

Any Phase to detect any phase to phase undervoltage. The RMS overvoltage threshold V>3/4 can be used to provide instantaneous undervoltage protection. The threshold setting, **V>2/4 Voltage Set**, can be set low, e.g. 20%Vn to detect as many faults as possible over the start-up cycle. The time delay, **V>3/4 Time Delay**, should be set to 0 s. If time delayed tripping is required then a PSL timer can be connected to the **V>3/4 RMS Start** DDBs (DDB 1111, 1115). The voltage remains low during the initial start-up of the machine. Therefore the undervoltage tripping would need to be blocked using a PSL timer during this initial phase, which can be evaluated during commissioning.

One of the Peak overvoltage stages can be used to provide blocking logic for the rotor overcurrent protection. See section 2.39.6.2.3 for more information.

2.39.6.5 Rotor residual overvoltage/neutral voltage displacement protection function (59NR)

On a healthy three-phase power system, the addition of each of the three-phase to earth voltages is nominally zero, as it is the vector addition of three balanced vectors at 120° to one another. Normally, there will be a small amount of standing neutral voltage on the rotor. The normal neutral voltage does not vary significantly between rotor frequencies but is highest at the highest rotor frequency. However, when an earth fault occurs on the rotor this balance is upset and a large 'neutral' voltage is produced as the rotor is usually high impedance earthed. The rotor phase voltages increase with increased rotor frequency. So the neutral voltage for an earth fault will also increase with rotor frequency.

Significant rotor neutral voltage can also be produced on a variable speed machine rotor during stator/grid phase to phase and three phase faults. The reason is related to the behaviour of the converter control, which can produce some frequency components of the PWM signal in zero sequence such as 3rd harmonics and harmonics of multiple of 3.

For stator/grid phase faults the rotor voltage will increase to a large value but these faults should be cleared before the crowbar operates limiting any rotor phase and neutral voltage. For a rotor earth fault, the crowbar does not operate as the phase to phase voltages does not change so the large neutral voltage is not limited. An earth fault on the stator does not produce a large change in the rotor neutral voltage.

The neutral voltage is calculated from the rotor three-phase to neutral RMS voltage measurements. An earth fault condition causes a rise in the neutral voltage with respect to earth that is commonly referred to as "neutral voltage displacement" or NVD.

For faults close to the rotor winding neutral the residual voltage will be small. Therefore, as with stator earth fault protection, typically only 95% of the rotor winding can be reliably protected. The percentage of winding protected will depend on the rotor frequency as the neutral voltage is higher at higher rotor frequencies.

The neutral voltage displacement protection function of the P348 relays consist of two stages of derived RMS neutral overvoltage protection with adjustable time delays. Two stages are included to account for applications that require both alarm and trip stages.

The main rotor earth fault protection is provided by the 100% rotor earth fault protection described in section 2.39.6.1 and the neutral voltage protection is a back-up earth fault protection.

2.39.6.5.1 Setting guidelines for rotor residual overvoltage/neutral voltage displacement protection

VN>1, may be selected as either **IDMT** (inverse time operating characteristic), **DT** (definite time operating characteristic) or **Disabled**, within the **VN>1 Function** cell. VN>2, operates with a definite time characteristic and is **Enabled/Disabled** in the **VN>2 Status** cell. The time delay, (**VN>1 TMS** - for IDMT curve; **VN>1 Time Delay**, **VN>2 Time Delay** - for definite time) should be selected to provide stability for stator phase faults. Significant rotor neutral voltage can be produced on a variable speed machine rotor during stator/grid phase to phase and three phase faults. However, stator and grid faults should be cleared quickly by their own main protection which will limit the neutral voltage to a low value. If the main protection is slow then the crowbar will probably operate during a stator or grid phase fault which will limit the neutral voltage to low value. Therefore, a short time delay longer than the crowbar operation can be used.

The neutral voltage threshold setting, **VN>1 Voltage Set**, must be set higher than the neutral voltage on the rotor under normal running conditions at maximum rotor frequency. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing neutral voltage (**VN-1 Derived RMS**), and setting at least 20% above this figure.

The neutral voltage across the earthing resistor during an earth fault can be calculated as shown in section 2.39.6.1.2.

2.39.6.6 Overfrequency protection function (81OR)

The rotor of a variable speed machine will have a maximum allowed frequency during normal operation when connected to the grid. Overfrequency protection can be used to detect when the rotor frequency exceeds this limit.

The frequency can transiently increase during fault conditons

Action can be taken at the generating plant to correct the situation without necessarily shutting down the generator.

Two independent time-delayed stages of overfrequency protection are provided. Two stages are included to account for applications that require both alarm and trip stages.

2.39.6.6.1 Setting guidelines for overfrequency protection

Each stage of overfrequency protection may be selected as **Enabled/Disabled**, in the **F>1/2/3/4 Status** cells. The frequency pickup setting, **F>x Setting** should be selected above the maximum allowed rotor frequency during normal running. Lower settings could be used to provide alarms. The maximum rotor frequency during normal running should be declared by the generator manufacturer.

The overfrequency time delay settings, **F>1/2/3/4 Time Delay**, should be selected to coordinate with normal, transient overfrequency excursions in the rotor during normal running and fault conditons. The generator manufacturer should declare the expected transient overfrequency behaviour. Typcially, a 1s time delay will be adequate to provide stability for transient overfrequency conditions caused by a rotor or stator fault.

The overfrequency protection should be blocked using **F>1/2/3/4/ Inhibit** DDBs (DDB 620-623) when the machine is running up and down. This is because the rotor frequency will be ramping from zero up to near nominal frequency (50 or 60Hz) during the machine start up for example.

DDB 671 **Machine Start** should be set ON after the machine has been synchronized with the grid. This DDB is used to switch on the low pass filter 2 after machine start-up to enable accurate measurement of the rotor frequency when the machine is running. See the Operation chapter for more information on the P348 filtering.

2.39.6.7 Field failure protection for detecting rotor open circuit faults (40)

Rotor short circuit faults can be easily detected by rotor/stator overcurrent protection. However, rotor open circuit faults can not be easily detected other than by using the P345 field failure impedance elements.

For two or three phase open circuit faults, the field failure protection with negative reactance offset, **FFail1 Xa1** = -1pu and a diameter setting, **FFail1 Xb1** = Xd is capable of detecting these faults. The field failure protection time delay, **FFail1 Time Delay**, should be set to minimize the risk of operation of the protection function during stable power swings following system disturbances or synchronization. A time delay less than 10 s would typically be applied. The minimum permissible delay, to avoid problems of false tripping due to stable power swings with the above impedance settings, would be of the order of 0.5 s.

For a single phase open circuit condition the measured impedances on all the three phases travel in circles on the X/R plane, which is a result of the oscillatory envelope of the stator currents, similar to that seen under a pole slipping condition. The frequency of the current oscillation is twice the rotor slip frequency.

The field failure protection reset (delayed drop off) timer, **FFail1 DO Timer**, can be used to provide an integrating function when the impedance is cyclically entering and exiting the characteristic, see section 2.27.3.

To achieve faster tripping a rotor single phase open circuit fault can be detected by using counters in the PSL to count the number of times the impedance comes in and out of the field failure characteristics in a given time, see section 2.14.2. The impedance cycle time is typically twice the rotor slip frequency so could be 0.1s for 5Hz and 2.5s for 0.2Hz. Care needs to be taken to avoid maloperation for power swings using the PSL counter by setting an appropriate count strategy eg >2 counts in 5s. Alternatively the pole slipping function in the P345 can also be used, which should have better stability for power swings as the impedance needs to cross the whole operating characteristic, see section 2.28.

3 APPLICATION OF NON-PROTECTION FUNCTIONS

3.1 Check synchronization

3.1.1 Basic principle

If a circuit breaker is closed when the generator and bus voltages are both live, with a large phase angle, frequency or magnitude difference between them, the system could be subjected to an unacceptable shock, resulting in loss of stability, and possible damage to the connected generator and generator-transformer.

System checks involve monitoring the voltages on both sides of a circuit breaker, and if both sides are live, performing a synchronism check to determine whether the phase angle, frequency and voltage magnitude differences between the voltage vectors, are within permitted limits.

The pre-closing system conditions for a given circuit breaker depend on the system configuration and for auto-reclosing depend on the selected auto-reclose program. For example, on a feeder with delayed auto-reclosing, the circuit breakers at the two line ends are normally arranged to close at different times. The first line end to close usually has a live bus and a dead line immediately before reclosing, and charges the line (dead line charge) when the circuit breaker closes. The second line end circuit breaker sees live bus and live line after the first circuit breaker has re-closed. If there is a parallel connection between the ends of the tripped feeder, they are unlikely to go out of synchronism, i.e. the frequencies will be the same, but the increased impedance could cause the phase angle between the two voltages to increase. Therefore the second circuit breaker to close might need a synchronism check, to ensure that the phase angle has not increased to a level that would cause an unacceptable shock to the system when the circuit breaker closes.

If there are no parallel interconnections between the ends of the tripped feeder, the two systems could lose synchronism, and the frequency at one end could slip relative to the other end. In this situation, the second line end would require a synchronism check comprising both phase angle and slip frequency checks.

If the second line end busbar has no power source other than the feeder that has tripped; the circuit breaker will see a live line and dead bus assuming the first circuit breaker has re-closed. When the second line end circuit breaker closes the bus will charge from the live line (dead bus charge).

For generator applications before closing the CB the frequency and voltage from the machine is varied automatically or manually until the generator voltage is in synchronism with the power system voltage. A check synchronizing relay is used to check the generator voltage is in synchronism with the system voltage in terms of voltage magnitude, voltage difference, phase angle and slip frequency before the generator CB is allowed to close.

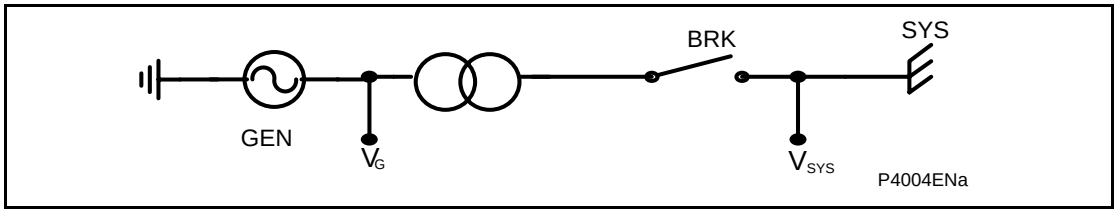


Figure 75: Typical connection between system and generator-transformer unit

3.1.2 VT selection

The P34x has a three-phase **Main VT** input and a single-phase **Check Sync VT** input. Depending on the primary system arrangement, the main three-phase VT for the relay may be located on either the busbar side or the generator side of the circuit breaker, with the Check Sync VT being located on the other side. Hence, the relay has to be programmed with the location of the main VT. This is done via the **Main VT Location - Gen/Bus** setting in the **SYSTEM CONFIG** menu. This is required for the voltage monitors to correctly define the Live Gen/Dead Gen and Live Bus/Dead Bus DDBs.

The Check Sync VT may be connected to either a phase to phase or phase to neutral voltage, and for correct synchronism check operation, the relay has to be programmed with the required connection. The **C/S Input** setting in the **CT & VT RATIOS** menu should be set to **A-N**, **B-N**, **C-N**, **A-B**, **B-C** or **C-A** as appropriate.

The P342/3 uses the neutral voltage input, VNeutral, for the Check Synch VT and so the user can not use the check synchronizing and the measured neutral voltage (59N) protection (VN>3, VN>4) at the same time. However, the derived neutral voltage protection (VN>1, VN>2) from the 3 phase voltage input can still be used with the check synchronising function.

The P344 uses the neutral voltage input, VN2, for the Check Synch VT and so the user can not use the check synchronizing and measured neutral voltage (59N) protection from VN2 (VN>5, VN>6) at the same time. However, the derived neutral voltage protection (VN>1, VN>2) from the 3 phase voltage input and the measured neutral voltage protection (VN>3, VN>4) from the VN1 voltage input can still be used with the check synchronising function.

The P345 uses a dedicated V Check Sync voltage input for the Check Synch VT and so there are no restrictions in using the check synchronising function and other protection functions in the relay.

3.1.3 Voltage and phase angle correction

3.1.3.1 CS VT ratio correction

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Differences in the busbar voltage and the generator voltage magnitude may be introduced by unmatched or slightly erroneous voltage transformer or step-up transformer ratios. These differences should be small, but they may be additive and therefore be significant. To compensate magnitude differences between the busbar voltage and the generator voltage the generator voltage can be adjusted by a multiplying factor, **C/S V Ratio Corr** to correct for any mismatch.

The voltage correction factor can be calculated as shown below:

$$\frac{TVR \times VTG}{VTB}$$

where

TVR = step-up transformer voltage ratio (HV nominal /LV nominal)

VTG = generator voltage transformer ratio (Main VT Primary/Main VT Sec'y)

VTB = busbar voltage transformer ratio (C/S VT Prim'y/C/S VT Sec'y)

For example,

IF TVR = 38.5 kV /10.5 kV, VTG = 10 kV/100 V, VTB = 35 kV/100 V AND Vgen = VGab, Vbus = VBab

Then, Vgen = 10500/100 = 105 V (secondary voltage), Vbus = 38500/350 = 110 V, and:

$$\textbf{C/S V Ratio Corr} = \frac{TVR \times VTG}{VTB} = 1.0476$$

So: Vgen' = Vgen x **C/S V Corr** = 110 V = Vbus

3.1.3.2 CS VT vector correction

If the generator CB is on the HV side the generator step-up transformer typically with the synch VT on the transformer HV side, the P34X uses the **Main VT Vect Grp** setting to compensate the phase shift between the generator VTs and the synch VT introduced by the transformer connections:

$$V_{gen,angle_comp} = V_{gen} e^{jN30^{\circ}}$$

Here, N = Main VT Vector Group, N = 0, 1,…11.

The generator voltage, Vgen, compensated phase shift is $N \times 30^{\circ}$. In most cases, N is 1, 11 and 0, and the corresponding compensated phase shift is +30°, -30° (330°) and 0°. The vector group (N) is 0 for the Main VT and synch VT on the generator side of the transformer or if there is no step-up transformer.

For example, when the step-up transformer connection type is Yd11, the LV Clock Vector is at 11 o'clock, the connection and vector diagrams are as below. Usually, the Main VT is on the generator LV side of the transformer so the **Main VT Vect Grp** matches the vector group of the transformer, eg **Main VT Vect Grp** = 11 for a Yd11 transformer.

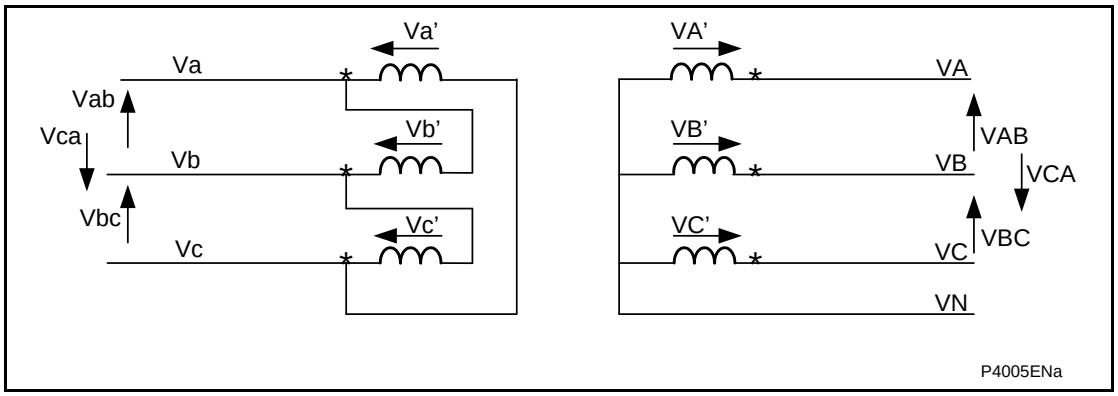


Figure 76: Typical connection between system and generator-transformer unit Transformer connection

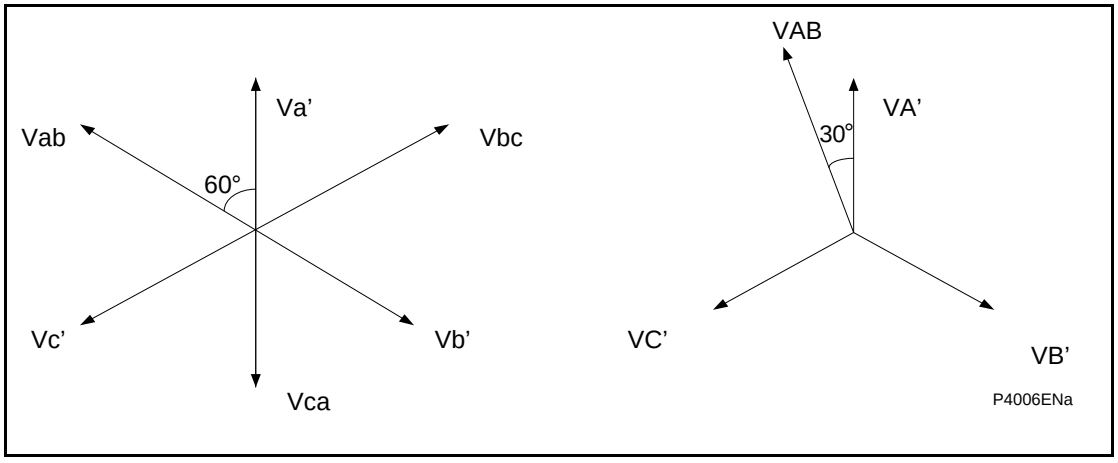


Figure 77: Transformer vector diagram

It can been seen that, $Vab = Vb$, the vector Vab is forward to VAB 30º, so the compensated phase shift should be -30°, that is vector Vab should be rotated 30° clockwise, **Main VT Vect Grp** = 11, assuming Main VT is on transformer LV side.

3.1.4 Voltage monitors

The P34x System Checks function includes voltage monitors to indicate if the generator and system busbar voltages are Live or Dead. The voltage monitor signals are not usually used for the closing logic of a generator CB, the check synch logic is generally only used for this application. The voltage monitor signals are typically used in feeder autoreclose applications where the first feeder CB to close may use the voltage monitor signals to check for Live Bus/Dead Line for example. The default settings are typical values, Dead = 0.2 Vn and Live = 0.5 Vn.

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The voltage monitor DDBs, if required, are combined in the PSL to provide the manual CB close check synchronizing logic, eg Dead Line/Live Gen (The P34x does not include autoreclose logic). The DDBs are connected to the Man Check Synch DDB (1362) which provides an input to the CB control logic to indicate a manual check synchronizing condition is satisfied.

The voltage monitor signals can be useful in generator applications to give indication if the generator or system busbar voltages are Live or Dead or can be used with timers in the PSL to provide additional under/overvoltage protection.

When Vgen magnitude is > Live Voltage, the generator is taken as Live (DDB 1328, Live Gen)

When Vgen magnitude is < Dead Voltage, the generator is taken as Dead (DDB 1329, Dead Gen)

When Vbus magnitude is > Live Voltage, the busbar is taken as Live (DDB 1330, Live Bus)

When Vbus magnitude is < Dead Voltage, the busbar is taken as Dead (DDB 1331, Dead Bus)

3.1.5 Check synchronization

The P34x System Checks function includes 2 check synchronization elements, Check Sync 1 and Check Sync 2. The check synch 1 OK (1332) and Check Synch 2 OK (1333) DDBs, if required, are used in the PSL to provide the manual CB close check synchronizing logic. The DDBs are connected to the Man Check Synch DDB (1362) which provides an input to the CB control logic to indicate a manual check synchronising condition is satisfied.

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Each check synch element checks that the generator frequency, voltage magnitude, and phase angle match the system frequency, voltage magnitude, and phase angle before allowing the generator breaker to be closed. Each element includes settings for the phase angle difference and slip frequency between the generator and system busbar voltages.

The P34x also includes independent under/over voltage monitors for the generator and system side of the CB as well as a differential voltage monitor applicable to both the Check Sync 1 and 2 elements. The user can select a number of under/over/differential voltage check synchronizing blocking options using the setting **CS Voltage Block** – **None, V<, V>, Vdiff>, V< and V>, V< and Vdiff>, V> and Vdiff>, V< V> Vdiff>.**

3.1.5.1 Slip control

The slip frequency used by Check Synch 1/2 can be calculated from the **CS1/2 Phase Angle** and **CS1/2 Slip Timer** settings as described below or can be measured directly from the frequency measurements, slip frequency = |Fgen-Fbus|. The user can select a number of slip frequency options using the settings **CS1 Slip Control** – **None, Timer Only, Frequency Only, Both** and **CS2 Slip Control** – **None, Timer, Frequency, Timer + Freq, Freq + CB Comp**.

If Slip Control by **Timer** or **Frequency + Timer**/**Both** is selected, the combination of **CS Phase Angle** and **CS Slip Timer** settings determines an effective maximum slip frequency, calculated as:

$$\frac{2 \times A}{T \times 360}$$ Hz. for Check Sync. 1, or

$$\frac{A}{T \times 360}$$ Hz. for Check Sync. 2

A = Phase Angle setting (°)
T = Slip Timer setting (seconds)

For example, for Check Sync 1 with **CS 1 Phase Angle** setting 30° and **CS 1 Slip Timer** setting 3.3 sec., the "slipping" vector has to remain within ±30° of the reference vector for at least 3.3 seconds. Therefore, a synchronism check output will not be given if the slip is greater than 2 x 30° in 3.3 seconds. Using the formula: 2 x 30 ÷ (3.3 x 360) = 0.0505 Hz (50.5 mHz).

For Check Sync 2, with **CS2 Phase Angle** setting 10° and **CS2 Slip Timer** setting 0.1 sec., the slipping vector has to remain within 10° of the reference vector, with the angle decreasing, for 0.1 sec. When the angle passes through zero and starts to increase, the synchronism check output is blocked. Therefore an output will not be given if slip is greater than 10° in 0.1 second. Using the formula: 10 ÷ (0.1 x 360) = 0.278 Hz (278 mHz).

Slip control by **Timer** is not practical for "large slip/small phase angle" applications, because the timer settings required are very small, sometimes < 0.1 s. For these situations, slip control by **Frequency** is recommended.

If **CS Slip Control** by **Frequency + Timer** (CS1) or **Both** (CS2) is selected, for an output to be given, the slip frequency must be less than BOTH the set **CS1/2 Slip Freq** value and the value determined by the **CS1/2 Phase Angle** and **CS1/2 Slip Timer** settings.

3.1.5.2 CB closing time compensation

The **CS2 Slip Control** – **Freq + Comp** (Frequency + CB Time Compensation) setting modifies the Check Sync 2 function to take account of the circuit breaker closing time. By measuring the slip frequency, and using the **CB Close Time** setting, the relay will issue the close command so that the circuit breaker closes at the instant the slip angle is equal to the **CS2 Phase Angle** setting.

The equation below describes the relationship between the compensated angle δ_K and the lead time to CB closing t_K for the circuit breaker to close at the instant the slip angle is equal to the CS2 phase angle setting, assuming the slip frequency is constant.

$$\delta_{MEA} - CS2\,phaseangle = \delta_K = \Delta\omega \times t_K$$

$$t_K = \frac{\delta_{MEA} - CS2\,phaseangle}{\Delta\omega} = \frac{\delta_{MEA} - CS2\,phaseangle}{Slip.Freq. \times 360^o}$$

δ_{MEA} = Mea.Angle

$\Delta\omega$ = slip angle velocity

δ_K = compensated angle

t_K = lead time to CB close

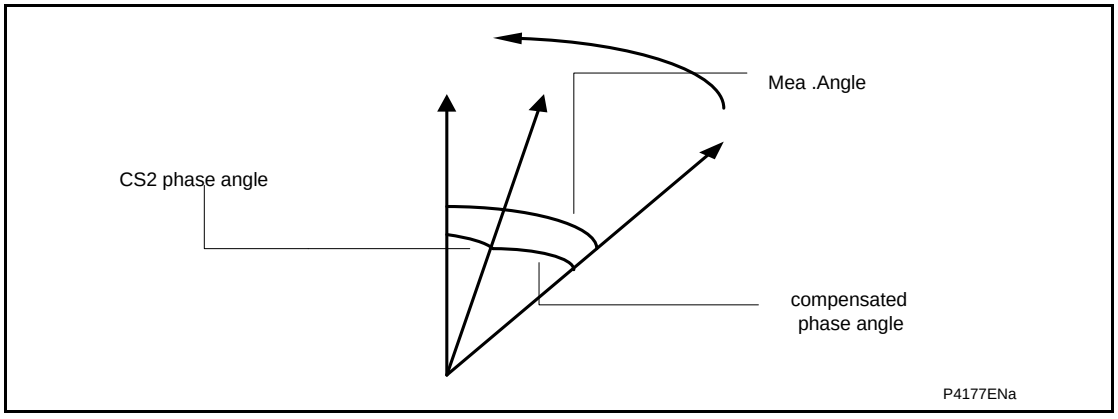


Figure 78: Check synch. 2 phase angle diagram

Unlike Check Sync 1, Check Sync 2 only permits closure for decreasing angles of slip, therefore the circuit breaker should always close within the limits defined by Check Sync 2. When CS2 phase angle = 0, the breaker should be closed just when the voltages are in phase with each other.

The **CB Close Time** measurement is available in the **CB Condition** menu for the last CB close. The relay calculates the **CB Close Time** from the time the close command is given to the time the CB is closed as indicated by the 3 pole dead logic. The **CB close Time** measurement can be useful when setting the **CB Close Time** compensation setting in the **System Checks** menu.

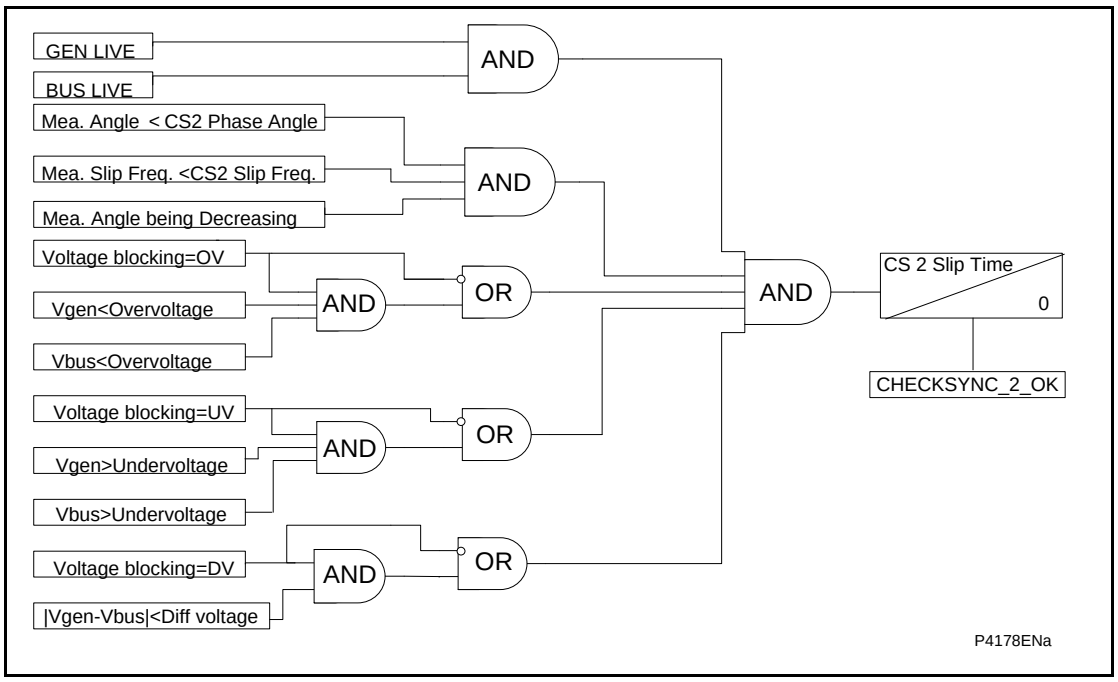


Figure 79: Check synch. 2 functional diagram

3.1.5.3 Check Sync 2 and system split

Check Sync 2 and system split functions are included for situations where the maximum permitted slip frequency and phase angle for synchronism check can change according to actual system conditions. A typical application is on a closely interconnected system, where synchronism is normally retained when a given feeder is tripped, but under some circumstances, with parallel interconnections out of service, the feeder ends can drift out of synchronism when the feeder is tripped. Depending on the system and machine characteristics, the conditions for safe circuit breaker closing could be, for example:

Condition 1: For synchronized systems, with zero or very small slip:

Slip ≦50 mHz; phase angle <30°

Condition 2: For unsynchronized systems, with significant slip:

Slip ≦250 mHz; phase angle <10° and decreasing

By enabling both Check Sync 1, set for condition 1, and Check Sync 2, set for condition 2, the P34x can be configured to allow CB closure if either of the two conditions is detected.

For manual circuit breaker closing with synchronism check, some utilities might prefer to arrange the logic to check initially for condition 1 only. However, if a System Split is detected before the condition 1 parameters are satisfied, the relay will switch to checking for condition 2 parameters instead, based on the assumption that a significant degree of slip must be present when system split conditions are detected. This can be arranged by suitable PSL logic, using the system check DDB signals.

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3.1.5.4 Generator check synchronizing

For generator CB closing applications generally there is only one synchronism check element required and so Check Sync 1 or Check Sync 2 is used.

The Check Sync 2 element includes CB closing time compensation and unlike Check Sync 1, Check Sync 2 only permits closure for decreasing angles of slip.

There are several synchronizing methods that may be used to minimize the possibility of damaging a generator when closing the generator CB:

- Automatic synchronizing
- Semi-automatic synchronizing
- Manual synchronizing

Synchronizing check relays are often applied with all these schemes to supervise the closing of the CB.

To avoid damaging a generator during synchronizing, the generator manufacturer will generally provide synchronizing limits in terms of breaker closing angle and voltage matching. Typical limits are:

1. Breaker closing angle: ±10 electrical degrees. The closing of the circuit breaker should ideally take place when the generator and the system are at or close to zero degrees phase angle with respect to each other. To accomplish this, the breaker should be set to close in advance of the phase angle coincidence taking into account the breaker closing time.
2. Voltage matching: 0% to +5%. The voltage difference should be minimized and not exceed 5%. This aids in maintaining system stability by ensuring some VAR flow into the system. Additionally, if the generator voltage is excessively lower than the grid when the breaker is closed, sensitive reverse power relays may trip.
3. Slip frequency: <0.067 Hz. The slip frequency should be minimized to the practical control/response limitations of the given prime mover. A large frequency difference causes rapid load pickup or excessive motoring of the machine. This could cause power swings on the system and mechanical torques on the machine. Additionally, if the machine is motored, sensitive reverse power relays may trip.

Slip frequency limits applied for certain machine types are based on the ruggedness of the turbine generator under consideration and the controllability of the turbine generator and MVA.

To prevent power flow from the system to the generator, some large steam turbine generators require that a low, positive slip be present when the generator breaker is closed. In contrast, Diesel generators may require that a zero or negative slip be present to unload the machine shaft and crank briefly when the generator breaker is closed. The DDBs CS1/2 Slipfeq>, CS1/2 Slipfeq<, CS Ang Rot ACW and CS Ang Rot CW can be used as interlocking signals to the ManCheck Synch DDB for these applications.

3.1.6 Frequency/Voltage control

The DDBs, CS Vgen>Vbus, CS Vgen<Vbus, CS1 Fgen>Fbus, CS1 Fgen<Fbus, CS2 Fgen>Fbus and CS2 Fgen<Fbus can be used for simple frequency control and voltage control outputs or for indication purposes. Pulsed outputs can be achieved using PSL if required.

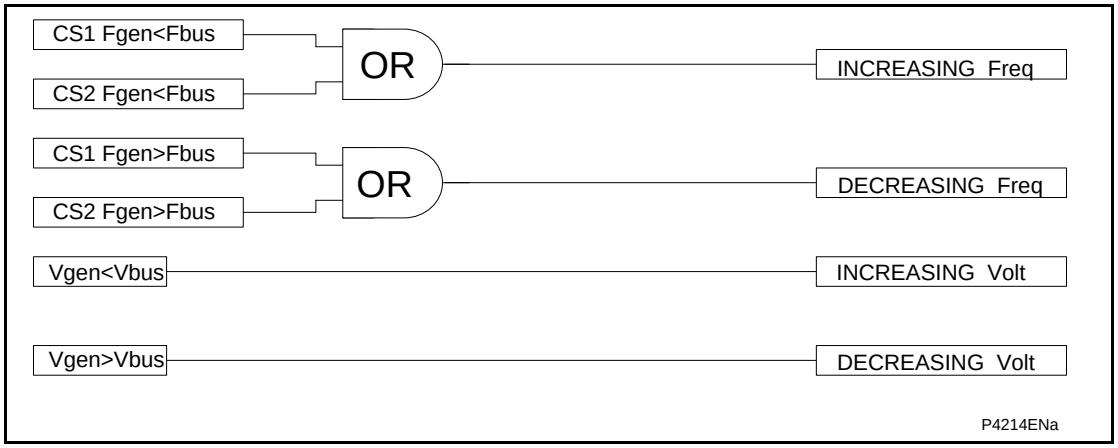


Figure 80: Freq/Volt control functional diagram

3.2 VT supervision

The voltage transformer supervision (VTS) feature is used to detect failure of the ac voltage inputs to the relay. This may be caused by internal voltage transformer faults, overloading, or faults on the interconnecting wiring to relays. This usually results in one or more VT fuses blowing. Following a failure of the ac voltage input there would be a misrepresentation of the phase voltages on the power system, as measured by the relay, which may result in mal-operation.

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The VTS logic in the relay is designed to detect the voltage failure, and automatically adjust the configuration of protection elements whose stability would otherwise be compromised. A time-delayed alarm output is also available.

3.2.1 Setting the VT supervision element (P342-6)

The **VTS Status** setting **Blocking/Indication** determines whether the following operations will occur on detection of VTS.

- VTS set to provide alarm indication only.
- Optional blocking of voltage dependent protection elements.
- Optional conversion of directional overcurrent elements to non-directional protection (available when set to blocking mode only). These settings are found in the function links cell of the relevant protection element columns in the menu.

The VTS block will be latched after a user settable time delay **VTS Time Delay**. Once the signal has latched then two methods of resetting are available. The first is manually via the front panel interface (or remote communications) when the **VTS Reset Mode** is set to **Manual**. The second method is automatically when **VTS Reset Mode** is set to **Auto** mode, provided the VTS condition has been removed and the 3 phase voltages have been restored above the phase level detector settings for more than 240 ms.

The **VTS I> Inhibit** overcurrent setting is used to inhibit the voltage transformer supervision in the event of a loss of all 3 phase voltages caused by a close up 3 phase fault occurring on the system following closure of the CB to energize the line. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close up three-phase fault.

This **VTS I2> Inhibit** NPS overcurrent setting is used to inhibit the voltage transformer supervision in the event of a fault occurring on the system with negative sequence current above this setting

The NPS current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load unbalance on the system. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence current, and setting at least 20% above this figure.

3.2.2 Setting the VT supervision element (P348)

The **VTS Status** setting **Blocking/Indication/Disabled** determines whether the following operations will occur on detection of VTS.

- VTS set to provide alarm indication only
- Optional blocking of voltage dependent protection elements (Neutral voltage protection)
- VTS is disabled

Once the VTS block has been established it is undesirable for subsequent system faults to override the block. The VTS block will therefore be latched after a user settable time delay **VTS Time Delay**. Once the signal has latched the VTS is reset automatically when the VTS condition has been removed. A VTS alarm is given after the **VTS Time Delay** has expired.

The VTS feature within the P348 relay operates on the voltage balance principle by detection of a difference voltage, **VTS V Diff Set**, between the individual phase voltages from 2 sets of VTs (VA-1 RMS/VB-1 RMS/VC-1 RMS and VA-2 RMS/VB-2 RMS/VC-2 RMS) connected to the rotor. If only one set of VTs is used then this function needs to be disabled using the **VTS Status - Disabled** setting.

The **VTS V Diff Set** pick-up threshold should be set to a voltage difference of 5V secondary unless the VTs are of dissimilar ratios or a voltage unbalance exists during normal operation.

The voltage unbalance can be checked at the commissioning stage, making use of the relay measurement function to display the standing phase voltages (VA-1 RMS/VB-1 RMS/VC-1 RMS and VA-2 RMS/VB-2 RMS/VC-2 RMS) and checking the setting is at least 20% above the maximum differential voltage per phase between Vx-1 RMS and Vx-2 RMS.

3.3 CT supervision

The current transformer supervision feature is used to detect failure of one or more of the ac phase current inputs to the relay. Failure of a phase CT or an open circuit of the interconnecting wiring can result in incorrect operation of any current operated element. Additionally, interruption in the ac current circuits risks dangerous CT secondary voltages being generated.

3.3.1 Setting the CT supervision element (P342-6)

The residual voltage setting, **CTS1/2 Vn< Inhibit** and the residual current setting, **CTS1/2 In> set**, should be set to avoid unwanted operation during healthy system conditions.

For example **CTS1/2 Vn< Inhibit** should be set to 120% of the maximum steady state residual voltage. The **CTS1/2 In> set** will typically be set below minimum load current. The time-delayed alarm, **CTS1/2 Time Delay**, is generally set to 5 seconds.

Where the magnitude of residual voltage during an earth fault is unpredictable, the element can be disabled to prevent a protection elements being blocked during fault conditions.

3.3.2 Setting the differential CT supervision element (P343-6)

The positive sequence current in at least two current inputs exceeds the **CTS I1** setting. The **CTS I1** setting should be below the minimum load current of the protected object. Therefore, 10% of the rated current might be used.

The high set ratio of negative to positive sequence current, **CTS I2/I1>2**, should be set below the ratio of negative sequence to positive sequence current for the minimum unbalanced fault current. A typical setting of 40% might be used.

The low set ratio of negative to positive sequence current, **CTS I2/I1> 1**, should be set above the maximum load unbalance. In practice, the levels of standing negative phase sequence current present on the system govern this minimum setting. This can be determined from a system study, or by making use of the relay measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during

maximum system load conditions, to ensure that all single-phase loads are accounted for. A 20% setting might be used.

If the following information is recorded by the relay during commissioning:

Ifull load = 500 A

I2 = 50 A

Therefore I2/I1 ratio is given by I2/I1 = 50/500 = 0.1

To allow for tolerances and load variations a setting of 20% of this value may be typical. Therefore set CTS I2/I1>1 = 20%.

Since sensitive settings have been used a long time delay is necessary to ensure a true CT failure. A 60 second time delay setting may be typical.

3.3.3 Setting the CT supervision element (P348)

The **CTS2 Status** setting, **Enabled/Disabled** can be used to enable or disable the stator CT supervision function.

The residual voltage setting and the residual current setting, **CTS2 In> Set**, should be set to avoid unwanted operation during healthy system conditions.

It is not possible to measure stator residual voltage in the P348 as the P348 does not measure the stator voltages. The residual voltage, therefore, needs to come from an external source, for example the stator P34x protection relay (VN>x Start DDB). An output contact from the stator generator relay (DDB 1088-1093: **VN>x Start**) should be connected to a digital input of the P348 (DDB 1268: **CTS2 No Vn**) to indicate when the residual voltage above setting is present. Alternatively, a GOOSE signal could also be used. A fixed time delay of 80ms is implemented in the P348 CTS logic to allow time for the external digital signal from the residual voltage element to be received and processed by the P348.

The stator voltage transformer connection used must be able to refer residual voltages from the primary to the secondary side. Therefore, if a 3 phase VT is used to derive the neutral voltage the residual voltage element should only be enabled where the three-phase VT is of five limb construction, or comprises three single-phase units, and has the primary star point earthed. A derived residual voltage or a measured residual voltage can be used.

The residual voltage (**VN>x Start** in the P34x) should typically be set to 120% of the maximum steady state residual voltage. The **CTS2 In> Set** will typically be set below minimum load current. The time-delayed alarm, **CTS2 Time Delay**, is typcially set to 5s.

Where the magnitude of residual voltage during an earth fault is unpredictable, the element can be disabled to prevent the protection element being blocked during fault conditions.

3.4 Circuit breaker condition monitoring

Periodic maintenance of circuit breakers is necessary to ensure that the trip circuit and mechanism operate correctly and also that the interrupting capability has not been compromised due to previous fault interruptions. Generally, such maintenance is based on a fixed time interval, or a fixed number of fault current interruptions. These methods of monitoring circuit breaker condition give a rough guide only and can lead to excessive maintenance.

3.4.1 Setting guidelines

3.4.1.1 Setting the Σ I^ thresholds

Where overhead lines are prone to frequent faults and are protected by oil circuit breakers (OCB's), oil changes account for a large proportion of the life cycle cost of the switchgear. Generally, oil changes are performed at a fixed interval of circuit breaker fault operations. However, this may result in premature maintenance where fault currents tend to be low, and hence oil degradation is slower than expected. The Σ I^ counter monitors the cumulative severity of the duty placed on the interrupter allowing a more accurate assessment of the circuit breaker condition to be made.

For OCB's, the dielectric withstand of the oil generally decreases as a function of ΣI^2t. This is where 'I' is the fault current broken, and 't' is the arcing time within the interrupter tank (not the interrupting time). As the arcing time cannot be determined accurately, the relay would normally be set to monitor the sum of the broken current squared, by setting 'Broken I^' = 2.

For other types of circuit breaker, especially those operating on higher voltage systems, practical evidence suggests that the value of 'Broken I^' = 2 may be inappropriate. In such applications 'Broken I^' may be set lower, typically 1.4 or 1.5. An alarm in this instance may be indicative of the need for gas/vacuum interrupter HV pressure testing, for example.

The setting range for 'Broken I^' is variable between 1.0 and 2.0 in 0.1 steps. It is imperative that any maintenance program must be fully compliant with the switchgear manufacturer's instructions.

3.4.1.2 Setting the number of operations thresholds

Every operation of a circuit breaker results in some degree of wear for its components. Therefore routine maintenance, such as oiling of mechanisms, may be based on the number of operations. Suitable setting of the maintenance threshold will allow an alarm to be raised, indicating when preventative maintenance is due. Should maintenance not be carried out, the relay can be set to lockout the auto-reclose function on reaching a second operations threshold. This prevents further reclosure when the circuit breaker has not been maintained to the standard demanded by the switchgear manufacturer's maintenance instructions.

Certain circuit breakers, such as oil circuit breakers (OCB's) can only perform a certain number of fault interruptions before requiring maintenance attention. This is because each fault interruption causes carbonizing of the oil, degrading its dielectric properties. The maintenance alarm threshold **No CB Ops. Maint** may be set to indicate the requirement for oil sampling for dielectric testing, or for more comprehensive maintenance.

Again, the lockout threshold **No CB Ops. Lock** may be set to disable auto-reclosure when repeated further fault interruptions could not be guaranteed. This minimizes the risk of oil fires or explosion.

3.4.1.3 Setting the operating time thresholds

Slow CB operation is also indicative of the need for mechanism maintenance. Therefore alarm and lockout thresholds (CB Time Maint./CB Time Lockout) are provided and are settable in the range of 5 to 500 ms. This time is set in relation to the specified interrupting time of the circuit breaker.

3.4.1.4 Setting the excessive fault frequency thresholds

A circuit breaker may be rated to break fault current a set number of times before maintenance is required. However, successive circuit breaker operations in a short period of time may result in the need for increased maintenance. For this reason it is possible to set a frequent operations counter on the relay which allows the number of operations **Fault Freq**. **Count** over a set time period **Fault Freq Time** to be monitored. A separate alarm and lockout threshold can be set.

3.5 Trip circuit supervision (TCS)

The trip circuit, in most protective schemes, extends beyond the relay enclosure and passes through components such as fuses, links, relay contacts, auxiliary switches and other terminal boards. This complex arrangement, coupled with the importance of the trip circuit, has led to dedicated schemes for its supervision.

Several trip circuit supervision schemes with various features can be produced with the P34x range. Although there are no dedicated settings for TCS, in the P34x, the following schemes can be produced using the programmable scheme logic (PSL). A user alarm is used in the PSL to issue an alarm message on the relay front display. If necessary, the user alarm can be re-named using the menu text editor to indicate that there is a fault with the trip circuit.

3.5.1 TCS scheme 1

3.5.1.1 Scheme description

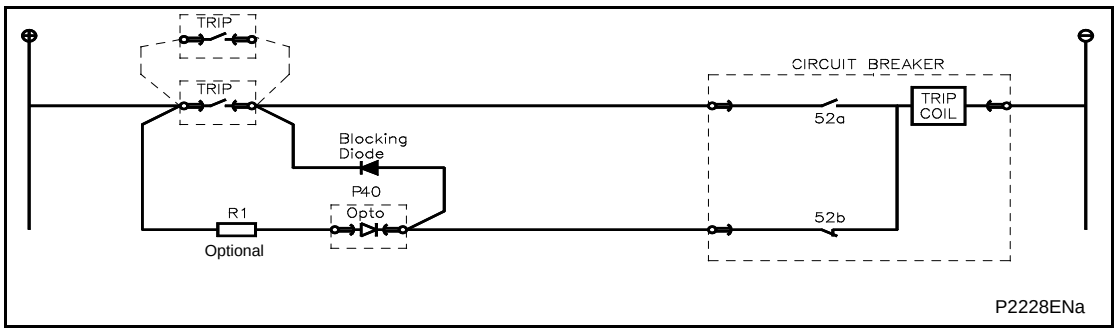


Figure 81: TCS scheme 1

This scheme provides supervision of the trip coil with the breaker open or closed, however, pre-closing supervision is not provided. This scheme is also incompatible with latched trip contacts, as a latched contact will short out the opto for greater than the recommended DDO timer setting of 400 ms. If breaker status monitoring is required a further 1 or 2 opto inputs must be used.

Note: A 52a CB auxiliary contact follows the CB position and a 52b contact is the opposite.

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When the breaker is closed, supervision current passes through the opto input, blocking diode and trip coil. When the breaker is open current still flows through the opto input and into the trip coil via the 52b auxiliary contact.

Hence, no supervision of the trip path is provided whilst the breaker is open. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

Resistor R1 is an optional resistor that can be fitted to prevent mal-operation of the circuit breaker if the opto input is inadvertently shorted, by limiting the current to <60 mA. The resistor should not be fitted for auxiliary voltage ranges of 30/34 volts or less, as satisfactory operation can no longer be guaranteed. The table below shows the appropriate resistor value and voltage setting (OPTO CONFIG menu) for this scheme.

This TCS scheme will function correctly even without resistor R1, since the opto input automatically limits the supervision current to less that 10 mA. However, if the opto is accidentally shorted the circuit breaker may trip.

Auxiliary voltage (Vx)	Resistor R1 (ohms)	Opto voltage setting with R1 fitted
24/27	-	-
30/34	-	-
48/54	1.2 k	24/27
110/250	2.5 k	48/54
220/250	5.0 k	110/125

Table 17: Resistor values for TCS scheme 1

Note: When R1 is not fitted the opto voltage setting must be set equal to supply voltage of the supervision circuit.

3.5.2 Scheme 1 PSL

Figure 82 shows the scheme logic diagram for the TCS scheme 1. Any of the available opto inputs can be used to indicate whether or not the trip circuit is healthy. The delay on drop off timer operates as soon as the opto is energized, but will take 400 ms to drop off/reset in the event of a trip circuit failure. The 400 ms delay prevents a false alarm due to voltage dips caused by faults in other circuits or during normal tripping operation when the opto input is

shorted by a self-reset trip contact. When the timer is operated the NC (normally closed) output relay opens and the LED and user alarms are reset.

The 50 ms delay on pick-up timer prevents false LED and user alarm indications during the relay power up time, following an auxiliary supply interruption.

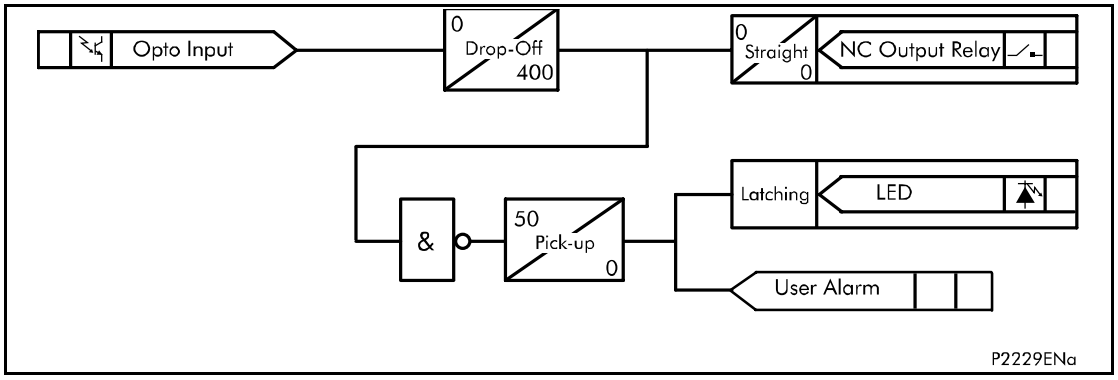


Figure 82: PSL for TCS schemes 1 and 3

3.5.3 TCS scheme 2

3.5.3.1 Scheme description

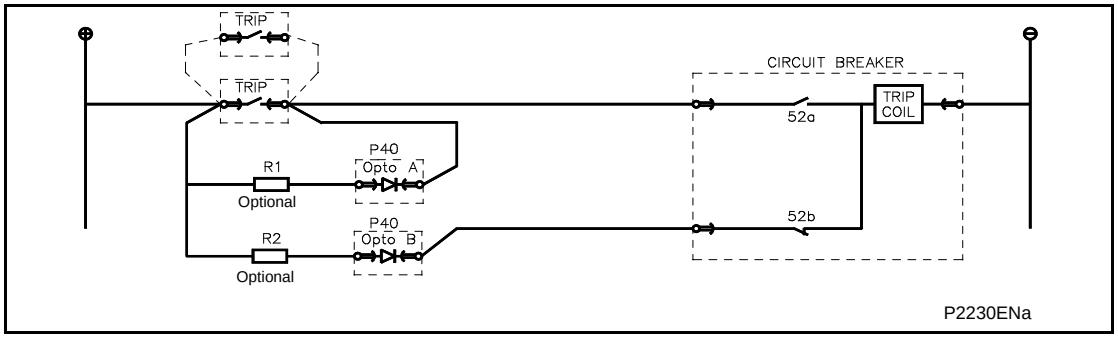


Figure 83: TCS scheme 2

Much like scheme 1, this scheme provides supervision of the trip coil with the breaker open or closed and also does not provide pre-closing supervision. However, using two opto inputs allows the relay to correctly monitor the circuit breaker status since they are connected in series with the CB auxiliary contacts. This is achieved by assigning Opto A to the 52a contact and Opto B to the 52b contact. Provided the **Circuit Breaker Status** is set to **52a and 52b** (**CB CONTROL** column) and opto's A and B are connected to CB Aux 3ph (52a) (DDB 611) and CB Aux 3ph (52b) (DDB 612) the relay will correctly monitor the status of the breaker. This scheme is also fully compatible with latched contacts as the supervision current will be maintained through the 52b contact when the trip contact is closed.

When the breaker is closed, supervision current passes through opto input A and the trip coil. When the breaker is open current flows through opto input B and the trip coil. As with scheme 1, no supervision of the trip path is provided whilst the breaker is open. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

As with scheme 1, optional resistors R1 and R2 can be added to prevent tripping of the CB if either opto is shorted. The resistor values of R1 and R2 are equal and can be set the same as R1 in scheme 1.

3.5.4 Scheme 2 PSL

The PSL for this scheme (Figure 84) is practically the same as that of scheme 1. The main difference being that both opto inputs must be off before a trip circuit fail alarm is given.

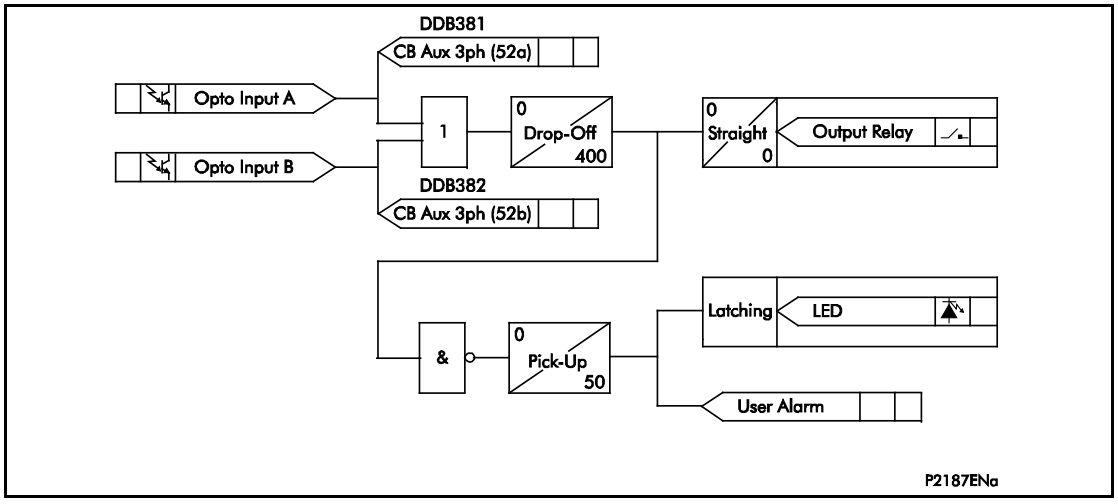


Figure 84: PSL for TCS scheme 2

3.5.5 TCS scheme 3

3.5.5.1 Scheme description

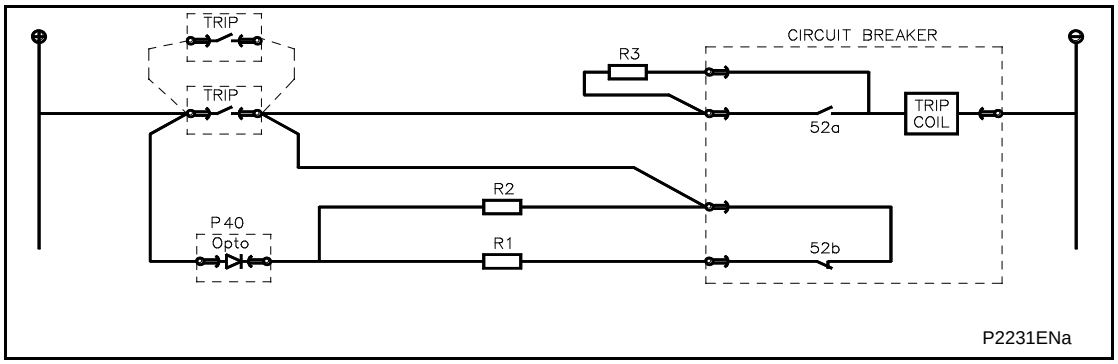


Figure 85: TCS scheme 2

Scheme 3 is designed to provide supervision of the trip coil with the breaker open or closed, but unlike schemes 1 and 2, it also provides pre-closing supervision. Since only one opto input is used, this scheme is not compatible with latched trip contacts. If circuit breaker status monitoring is required a further 1 or 2 opto inputs must be used.

When the breaker is closed, supervision current passes through the opto input, resistor R2 and the trip coil. When the breaker is open current flows through the opto input, resistors R1 and R2 (in parallel), resistor R3 and the trip coil. Unlike schemes 1 and 2, supervision current is maintained through the trip path with the breaker in either state, therefore giving pre-closing supervision.

As with schemes 1 and 2, resistors R1 and R2 are used to prevent false tripping, if the opto-input is accidentally shorted. However, unlike the other two schemes, this scheme is dependent on the position and value of these resistors. Removing them would result in incomplete trip circuit monitoring. The table below shows the resistor values and voltage settings required for satisfactory operation.

Auxiliary voltage (Vx)	Resistor R1 & R2 (ohms)	Resistor R3 (ohms)	Opto voltage setting
24/27	-	-	-
30/34	-	-	-
48/54	1.2 k	0.6 k	24/27
110/250	2.5 k	1.2 k	48/54
220/250	5.0 k	2.5 k	110/125

Table 18: Resistor values for TCS scheme 2

Note: Scheme 3 is not compatible with auxiliary supply voltages of 30/34 volts and below.

3.5.6 Scheme 3 PSL

The PSL for scheme 3 is identical to that of scheme 1 (see Figure 81).

3.6 VT connections

3.6.1 Open delta (vee connected) VT's

The P342/3/4/5/6 relay can be used with vee connected VTs by connecting the VT secondaries to C19, C20 and C21 input terminals, with the C22 input left unconnected (see Figures 2 and 18 in document *P34x/EN IN*).

This type of VT arrangement cannot pass zero-sequence (residual) voltage to the relay, or provide any phase to neutral voltage quantities. Therefore any protection that is dependent on zero sequence voltage measurements should be disabled unless a direct measurement can be made via the measured VN1 input (C23 - C24). Therefore, neutral displacement protection, sensitive directional earth fault protection and CT supervision should be disabled unless the residual voltage is measured directly from the secondary of the earthing transformer or from a broken delta VT winding on a 5 limb VT.

The under and overvoltage protection can be set as phase to phase measurement with vee connected VTs. The underimpedance and the voltage dependent overcurrent use phase-phase voltages anyway, therefore the accuracy should not be affected. The protection functions which use phase-neutral voltages are the power, the loss of excitation and pole slipping protection; all are for detecting abnormal generator operation under 3-phase balanced conditions, therefore the 'neutral' point, although 'floating' will be approximately at the center of the three-phase voltage vectors.

The accuracy of single-phase voltage measurements can be impaired when using vee connected VT’s. The relay attempts to derive the phase to neutral voltages from the phase to phase voltage vectors. If the impedance of the voltage inputs were perfectly matched the phase to neutral voltage measurements would be correct, provided the phase to phase voltage vectors were balanced. However, in practice there are small differences in the impedance of the voltage inputs, which can cause small errors in the phase to neutral voltage measurements. This may give rise to an apparent residual voltage. This problem also extends to single-phase power and impedance measurements that are also dependent on their respective single-phase voltages.

The phase to neutral voltage measurement accuracy can be improved by connecting 3, well matched, load resistors between the phase voltage inputs (C19, C20, C21) and neutral C22, therefore creating a ‘virtual’ neutral point. The load resistor values must be chosen so that their power consumption is within the limits of the VT. It is recommended that 10 kΩ ±1% (6 W) resistors are used for the 110 V (Vn) rated relay, assuming the VT can supply this burden.

3.6.2 VT single point earthing

The P34x range will function correctly with conventional three-phase VT’s earthed at any one point on the VT secondary circuit. Typical earthing examples being neutral earthing and yellow phase earthing.

4 CURRENT TRANSFORMER REQUIREMENTS

The current transformer requirements for each current input will depend on the protection function with which they are related and whether the line current transformers are being shared with other current inputs. Where current transformers are being shared by multiple current inputs, the kneepoint voltage requirements should be calculated for each input and the highest calculated value used.

The P342/3/4/5/6 is able to maintain all protection functions in service over a wide range of operating frequency due to its frequency tracking system (5 - 70 Hz).

When the P342/3/4/5/6 protection functions are required to operate accurately at low frequency, it will be necessary to use CT's with larger cores. In effect, the CT requirements need to be multiplied by fn/f, where f is the minimum required operating frequency and fn is the nominal operating frequency.

4.1 Generator differential function

4.1.1 Biased differential protection

The kneepoint voltage requirements for the current transformers used for the current inputs of the generator differential function, with settings of Is1 = 0.05 In, k1 = 0%, Is2 = 1.2 In, k2 = 150%, and with a boundary condition of through fault current ≤ 10 In, is:

For phase-earth faults

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$V_k \geq 50I_n (R_{ct} + 2R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R <120 If <10 In

$V_k \geq 30I_n (R_{ct} + 2R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R < 40 If < 10 In

Where the generator is impedance earthed and the maximum secondary earth fault current is less than I_n then the CT knee point voltage requirements are:

For phase-phase, 3 phase faults

$V_k \geq 25I_n (R_{ct} + R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R <60 If <10 In

$V_k \geq 30I_n (R_{ct} + R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R <100 If <10In, X/R <120 If <5In

$V_k \geq 40I_n (R_{ct} + R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R <120 If <10 In

Where:

V_k = Minimum current transformer kneepoint voltage for through fault stability

I_n = Relay rated current

R_{ct} = Resistance of current transformer secondary winding (Ω)

R_L = Resistance of a single lead from relay to current transformer (Ω)

R_r = Resistance of any other protective relays sharing the current transformer (Ω)

If = maximum through fault current

For Class-X current transformers, the excitation current at the calculated kneepoint voltage requirement should be less than 2.5 I_n (<5% of the maximum perspective fault current 50 In, on which these CT requirements are based). For IEC standard protection class current transformers, it should be ensured that class 5P are used.

4.1.2 High impedance differential protection

If the generator differential protection function is to be used to implement high impedance differential protection, then the current transformer requirements for phase faults are:

$R_s = [1.5 * (If) * (R_{CT} + 2R_L)] / IS1$

$V_s = 1.5 \, If \, (R_{CT} + 2R_L)$

$V_K \geq 2 * Is1 * Rs = 2 \, Vs$

Where:

R_s = Value of stabilizing resistor (ohms)

If = Maximum secondary through fault current level (amps)

V_K = CT knee point voltage (volts)

I_{S1} = Current setting of differential element (amps)

R_{CT} = Resistance of current transformer secondary winding (ohms)

R_L = Resistance of a single lead from relay to current transformer (ohms)

V_s = Stability voltage

AP

4.2 Generator-transformer differential function

4.2.1 Biased differential protection

The kneepoint voltage requirements for the current transformers used for the current inputs of the generator-transformer differential function, with settings of Is1 = 0.2 In, k1 = 30%, Is2 = 1.0 In, k2 = 80%, and with a boundary condition of through fault current ≤ 16 In, is:

For phase-earth faults

$V_k \geq 80 I_n (R_{ct} + 2R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R <120 If <16 In, X/R <600 If <10 In

$V_k \geq 30 I_n (R_{ct} + 2R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R < 120 If < 10 In

$V_k \geq 110 I_n (R_{ct} + 2R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R <600 If <16 In

Where the generator is impedance earthed and the maximum secondary earth fault current is less than I_n then the CT knee point voltage requirements are:

For phase-phase, 3 phase faults

$V_k \geq 25 I_n (R_{ct} + R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R <60 If <10 In

$V_k \geq 30 I_n (R_{ct} + R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R <100 If <10 In, X/R <120 If < 5 In

$V_k \geq 40 I_n (R_{ct} + R_L + R_r)$ with a minimum of $\frac{60}{In}$ for X/R <120 If <10 In

Where:

V_k = Minimum current transformer kneepoint voltage for through fault stability

I_n = Relay rated current

R_{ct} = Resistance of current transformer secondary winding (Ω)

R_L = Resistance of a single lead from relay to current transformer (Ω)

R_r = Resistance of any other protective relays sharing the current transformer (Ω)

If = Maximum through fault current

For Class-X current transformers, the excitation current at the calculated kneepoint voltage requirement should be less than 2.5 I_n (<5% of the maximum perspective fault current 50 In, on which these CT requirements are based). For IEC standard protection class current transformers, make sure that class 5P are used.

4.3 Voltage dependent overcurrent, field failure, thermal overload, pole slipping, underimpedance and negative phase sequence protection functions

When determining the current transformer requirements for an input that supplies several protection functions, it must be ensured that the most onerous condition is met. This has been taken into account in the formula given below. The formula is equally applicable for current transformers mounted at either the neutral-tail end or terminal end of the generator.

$V_k \geq 20 I_n (R_{ct} + 2R_L + R_r)$

Where:

V_k = Minimum current transformer kneepoint voltage for through fault stability

I_n = Relay rated current

R_{ct} = Resistance of current transformer secondary winding (Ω)

R_L = Resistance of a single lead from relay to current transformer (Ω)

R_r = Resistance of any other protective relays sharing the current transformer (Ω)

4.4 Sensitive directional earth fault protection function residual current input

4.4.1 Residually connected line current transformers

With reference to section 2.19, the sensitive directional earth fault input current transformer could be driven by three residually connected line current transformers.

It has been assumed that the sensitive directional earth fault protection function will only be applied when the stator earth fault current is limited to the stator winding rated current or less. Also assumed is that the maximum X/R ratio for the impedance to a bus earth fault will be no greater than 10. The required minimum kneepoint voltage will therefore be:

$V_k \geq 6 I_n (R_{ct} + 2R_L + R_r)$

Where:

V_k = Minimum current transformer kneepoint voltage for through fault stability

I_n = Relay rated current

R_{ct} = Resistance of current transformer secondary winding (Ω)

R_L = Resistance of a single lead from relay to current transformer (Ω).

R_r = Resistance of any other protective relays sharing the current transformer (Ω).

4.4.2 Core balanced current transformers

Unlike a line current transformer, the rated primary current for a core balanced current transformer may not be equal to the stator winding rated current. This has been taken into account in the formula:

$V_k > 6NIn (Rct + 2RL + Rr)$

Where:

V_k = Minimum current transformer kneepoint voltage for through fault stability

$$N = \frac{\text{Stator earth fault current}}{\text{Core balanced current transformer rated primary current}}$$

I_n = Relay rated current

R_{ct} = Resistance of current transformer secondary winding (Ω)

R_L = Resistance of a single lead from relay to current transformer (Ω)

R_r = Resistance of any other protective relays sharing the current transformer (Ω)

Note: N should not be greater than 2. The core balance current transformer ratio should be selected accordingly.

4.5 Stator earth fault protection function

The earth fault I_n current input is used by the stator earth fault protection function.

AP

4.5.1 Non-directional definite time/IDMT earth fault protection

CT requirements for time-delayed earth fault overcurrent elements

$V_K \geq Icn/2 * (RCT + 2RL + Rrn)$

4.5.2 Non-directional instantaneous earth fault protection

CT requirements for instantaneous earth fault overcurrent elements

$V_K \geq Isn (RCT + 2RL + Rrn)$

Where:

V_K = Required CT knee-point voltage (volts)

Icn = Maximum prospective secondary earth fault current or 31 times I> setting (whichever is lower) (amps)

Isn = Earth fault setting (amps)

R_{CT} = Resistance of current transformer secondary winding (ohms)

R_L = Resistance of a single lead from relay to current transformer (ohms)

R_{rn} = Impedance of the relay neutral current input at In (ohms)

4.6 Restricted earth fault protection

4.6.1 Low impedance

VK ≥ 24 * In * (RCT + 2RL) for X/R < 40 and If < 15 In

VK ≥ 48 * In * (RCT + 2RL) for X/R < 40, 15 In < If < 40 In and 40 <X/R < 120, If < 15 In

Where:

V_K = Required CT knee point voltage (volts)

I_n = rated secondary current (amps)

R_{CT} = Resistance of current transformer secondary winding (Ω)

R_L = Resistance of a single lead from relay to current transformer (Ω)

I_f = Maximum through fault current level (amps)

4.6.2 High impedance

The High Impedance Restricted Earth Fault element shall maintain stability for through faults and operate in less than 40 ms for internal faults provided the following equations are met in determining CT requirements and the value of the associated stabilizing resistor:

$Rs = (If) * (R_{CT} + 2R_L) / IS1$

$V_s = 1.5\ If\ (R_{CT} + 2R_L)$

$V_K \geq 4 * Is1 * Rs = 4\ Vs$

Where:

Rs = Value of Stabilizing resistor (ohms)

If = Maximum secondary through fault current level (amps)

V_K = CT knee point voltage (volts)

I_{S1} = Current setting of REF element (amps)

R_{CT} = Resistance of current transformer secondary winding (ohms)

R_L = Resistance of a single lead from relay to current transformer (ohms)

V_s = Stability voltage

4.7 Reverse and low forward power protection functions

For both reverse and low forward power protection function settings greater than 3% Pn, the phase angle errors of suitable protection class current transformers will not result in any risk of mal-operation or failure to operate. However, for the sensitive power protection if settings less than 3% are used, it is recommended that the current input is driven by a correctly loaded metering class current transformer.

4.7.1 Protection class current transformers

For less sensitive power function settings (>3%Pn), the phase current input of the P34x should be driven by a correctly loaded class 5P protection current transformer.

To correctly load the current transformer, its VA rating should match the VA burden (at rated current) of the external secondary circuit through which it is required to drive current.

4.7.2 Metering class current transformers

For low Power settings (<3%Pn), the I_n Sensitive current input of the P34x should be driven by a correctly loaded metering class current transformer. The current transformer accuracy class will be dependent on the reverse power and low forward power sensitivity required. The table below indicates the metering class current transformer required for various power settings below 3%Pn.

To correctly load the current transformer, its VA rating should match the VA burden (at rated current) of the external secondary circuit through which it is required to drive current. Use of the P34x sensitive power phase shift compensation feature will help in this situation.

Reverse and low forward power settings %Pn	Metering CT class
0.5	0.1
0.6	0.1
0.8	0.2
1.0	0.2
1.2	0.2
1.4	0.2
1.6	0.5
1.8	0.5
2.0	0.5
2.2	0.5
2.4	0.5
2.6	0.5
2.8	0.5
3.0	1.0

Table 19: Sensitive power current transformer requirements

4.8 100% stator earth fault protection function 20 Hz inputs (P345)

4.8.1 Line current transformers

AP

4.8.1.1 Generator earthed via a primary resistor in generator starpoint

It has been assumed that the 100% stator earth fault protection function will only be applied when the stator earth fault current is limited to <2x rated current or less as the linear range of the sensitve current input is 2 In. Class 5P CTs are recommended. The required minimum kneepoint voltage is:

$V_k \geq fn/20 \times 2\ I_n (R_{ct} + 2R_L + Rr)$

Where:

V_k = Minimum current transformer kneepoint voltage for through fault stability

I_n = Relay rated current

R_{ct} = Resistance of current transformer secondary winding (Ω)

R_L = Resistance of a single lead from relay to current transformer (Ω).

Rr = Resistance of any other protective relays sharing the current transformer (Ω).

f_n = Fundamental frequency 50 or 60 Hz (fn/20 is to account for operation at 20 Hz)

4.8.1.2 Generator earthed via earthing transformer and secondary resistor at the terminals or star point of the generator

A 400/5A CT can be ordered for this application.

4.8.2 Earthing transformers

To prevent the secondary load resistance from becoming too small (it should be > 0.5 Ω where possible) a high secondary voltage, such as 500 V, should be chosen for the neutral or earthing transformer.

It is important that the earthing transformer never becomes saturated otherwise ferroresonance may occur. It is sufficient that the transformer knee point voltage be equal to the generator rated line voltage, Vn.

4.8.2.1 Generator earthed via a primary resistor in generator starpoint

Voltage transformer rating: Vn/√3 / 500 V, 3000 VA (for 20 s) class 0.5 (non-saturated up to Vn,Generator)

Vn = rated generator line voltage (phase-phase)

4.8.2.2 Generator earthed via earthing transformer and secondary resistor at the terminals of the generator

Voltage transformer rating: Vn/√3 / 500/3 V (non-saturated up to Vn,Generator)

The transformer VA rating for 20 s per phase = 1.3 x 1/3 x If x Vn x √3 x √10/√20

for 3 single phase transformers.

If = primary fault current

The 1.3 accounts for an overvoltage factor from field forcing.

The √10/√20 increases the rating from 10 to 20 s.

For a 3 phase transformer the VA rating is 3 times higher.

4.8.2.3 Generator earthed via earthing transformer and secondary resistor at the starpoint of the generator

Voltage transformer rating: Vn/√3 / 500 V (non-saturated up to Vn, Generator)

AP

The transformer VA rating for 20 s per phase = 1.3 x If x Vn x √3 x √10/√20

The 1.3 accounts for an overvoltage factor from field forcing.

The √10/√20 increases the rating from 10 to 20 s.

4.9 100% rotor earth fault protection function 20 Hz inputs for variable speed machines (P345)

4.9.1 Earth current transformer

It has been assumed that the 100% rotor earth fault protection function will only be applied when the rotor earth fault current is limited to <2x rated current or less as the linear range of the sensitve current input is 2 In. Class 5P CTs are recommended. The required minimum kneepoint voltage is:

$V_k \geq 2\ If_n\ (R_{ct} + 2R_L + Rr)$

Where:

V_k = Minimum current transformer kneepoint voltage for through fault stability

R_{ct} = Resistance of current transformer secondary winding (Ω)

R_L = Resistance of a single lead from relay to current transformer (Ω).

Rr = Resistance of any other protective relays sharing the current transformer (Ω).

If_n = Maximum secondary earth fault current

4.9.2 Earthing transformer

Voltage transformer rating: 500V/200 V, 3000 VA (for 20 s) class 0.5 (non-saturated up to Vn,Generator)

The ratio of the VT is selected to 500/200V to limit the maximum voltage to the P345 voltage inputs <200V during rotor earth fault conditions. The P345 relay voltage inputs have a linear range 0-200V and can withstand continuously 2Vn.

4.10 Converting an IEC185 current transformer standard protection classification to a kneepoint voltage

The suitability of an IEC standard protection class current transformer can be checked against the kneepoint voltage requirements specified previously.

If, for example, the available current transformers have a 15 VA 5P 10 designation, then an estimated kneepoint voltage can be obtained as follows:

$$V_k = \frac{VA \times ALF}{In} + ALF \times I_n \times R_{ct}$$

Where:

V_k = Required kneepoint voltage

VA = Current transformer rated burden (VA)

ALF = Accuracy limit factor

I_n = Current transformer secondary rated current (A)

R_{ct} = Resistance of current transformer secondary winding (Ω)

If R_{ct} is not available, then the second term in the above equation can be ignored.

Example: 400/5A, 15VA 5P 10, R_{ct} = 0.2 Ω

$$V_k = \frac{15 \times 10}{5} + 10 \times 5 \times 0.2$$

$$= 40 \text{ V}$$

AP

4.11 Converting IEC185 current transformer standard protection classification to an ANSI/IEEE standard voltage rating

The Px40 series protection is compatible with ANSI/IEEE current transformers as specified in the IEEE C57.13 standard. The applicable class for protection is class "C", which specifies a non air-gapped core. The CT design is identical to IEC class P, or British Standard class X, but the rating is specified differently.

The ANSI/IEEE “C” Class standard voltage rating required will be lower than an IEC knee point voltage. This is because the ANSI/IEEE voltage rating is defined in terms of useful output voltage at the terminals of the CT, whereas the IEC knee point voltage includes the voltage drop across the internal resistance of the CT secondary winding added to the useful output. The IEC/BS knee point is also typically 5% higher than the ANSI/IEEE knee point.

Therefore:

Vc = [Vk - Internal voltage drop] / 1.05

= [Vk - (In . RCT . ALF)] / 1.05

Where:

Vc = “C” Class standard voltage rating

Vk = IEC Knee point voltage required

In = CT rated current = 5A in USA

R_{CT} = CT secondary winding resistance
(for 5A CTs, the typical resistance is 0.002 ohms/secondary turn)

ALF = The CT accuracy limit factor, the rated dynamic current output of a "C" class CT (Kssc) is always 20 x In

The IEC accuracy limit factor is identical to the 20 times secondary current ANSI/IEEE rating.

Therefore:

$Vc = [Vk - (100 . R_{CT})]/1.05$

5 AUXILIARY SUPPLY FUSE RATING

In the Safety section of this manual, the maximum allowable fuse rating of 16A is quoted. To allow time grading with fuses upstream, a lower fuselink current rating is often preferable. Use of standard ratings of between 6A and 16A is recommended. Low voltage fuselinks, rated at 250 V minimum and compliant with IEC 60269-2 general application type gG are acceptable, with high rupturing capacity. This gives equivalent characteristics to HRC "red spot" fuses type NIT/TIA often specified historically.

Table 20 recommends advisory limits on relays connected per fused spur. This applies to The Px40 series devices with hardware suffix C and higher, as these have inrush current limitation on switch-on, to conserve the fuse-link.

Maximum number of Px40 relays recommended per fuse				
Battery nominal voltage	6A	10A fuse	15 or 16A fuse	Fuse rating > 16A
24 to 54 V	2	4	6	Not permitted
60 to 125 V	4	8	12	Not permitted
138 to 250 V	6	10	16	Not permitted

Table 20: Maximum number of Px40 relays recommended per fuse

Alternatively, miniature circuit breakers (MCB) may be used to protect the auxiliary supply circuits.

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PROGRAMMABLE LOGIC

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 PROGRAMMABLE LOGIC

1.1 Overview

The purpose of the programmable scheme logic (PSL) is to allow the relay user to configure an individual protection scheme to suit their own particular application. This is achieved through the use of programmable logic gates and delay timers.

The input to the PSL is any combination of the status of opto inputs. It is also used to assign the mapping of functions to the opto inputs and output contacts, the outputs of the protection elements, e.g. protection starts and trips, and the outputs of the fixed protection scheme logic. The fixed scheme logic provides the relay's standard protection schemes. The PSL itself consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, e.g. to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven; the logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL; even with large, complex PSL schemes the relay trip time will not lengthen.

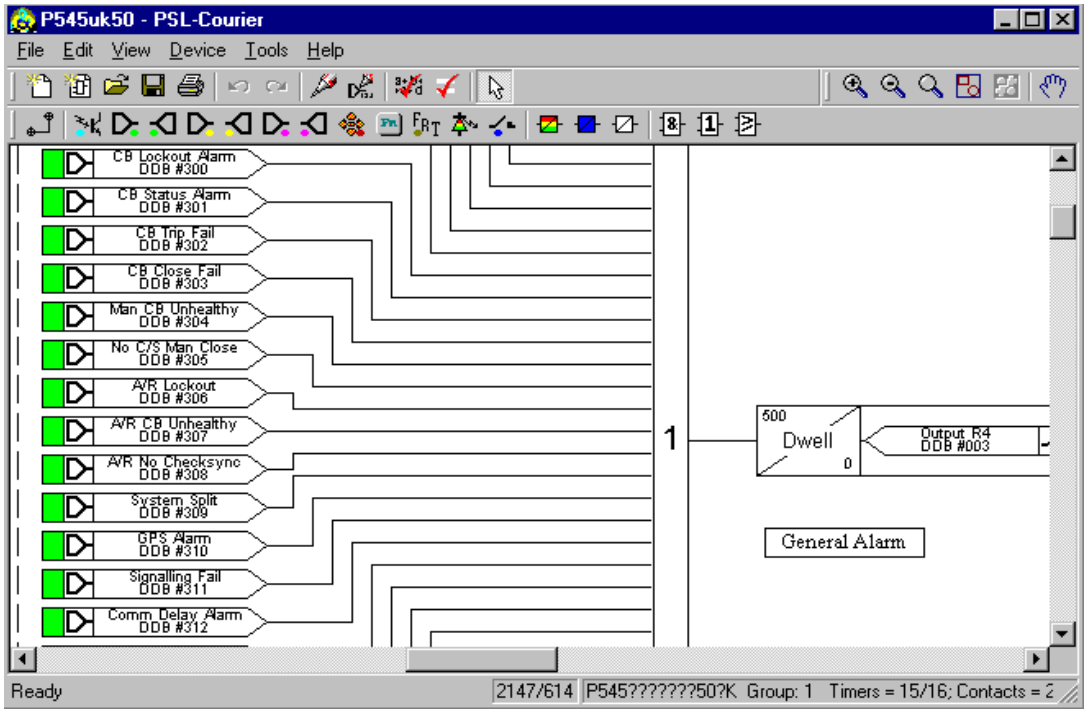
This system provides flexibility for the user to create their own scheme logic design. However, it also means that the PSL can be configured into a very complex system, hence setting of the PSL is implemented through the PC support package S1 Agile.

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1.2 S1 Agile Px40 PSL editor

To access the Px40 PSL Editor menu click on 

The PSL Editor module enables you to connect to any device front port, retrieve and edit its Programmable Scheme Logic files and send the modified file back to a Px40 device.



1.3 How to use Px40 PSL editor

- The Px40 PSL editor can:
- Start a new PSL diagram
- Extract a PSL file from a Px40 IED
- Open a diagram from a PSL file
- Add logic components to a PSL file
- Move components in a PSL file
- Edit link of a PSL file
- Add link to a PSL file
- Highlight path in a PSL file
- Use a conditioner output to control logic
- Download PSL file to a Px40 IED
- Print PSL files

See the *S1 Agile program online help* or 'MiCOM P40 Agile Modular and Compact Ranges, Settings Application Software User Guide', P40-M&CR-UG for more detailed information on how to use these functions.

1.4 Warnings

Before the scheme is sent to the relay checks are done. Various warning messages may be displayed as a result of these checks.

The Editor first reads in the model number of the connected relay, and then compares it with the stored model number. A "wildcard" comparison is used. If a model mismatch occurs then a warning is generated before sending starts. Both the stored model number and that read-in from the relay are displayed along with the warning. However, the user must decide if the settings to be sent are compatible with the connected relay. Wrongly ignoring the warning could lead to undesired behavior in the relay.

If there are any potential problems of an obvious nature then a list is generated. The types of potential problems that the program attempts to detect are:

- One or more gates, LED signals, contact signals, and/or timers have their outputs linked directly back to their inputs. An erroneous link of this sort could lock up the relay, or cause other more subtle problems to arise.
- Inputs To Trigger (ITT) exceeds the number of inputs. A programmable gate has its ITT value set to greater than the number of actual inputs; the gate can never activate. Note that there is no lower ITT value check. A 0-value does not generate a warning.
- Too many gates. There is a theoretical upper limit of 256 gates in a scheme, but the practical limit is determined by the complexity of the logic. In practice the scheme would have to be very complex, and this error is unlikely to occur.
- Too many links. There is no fixed upper limit to the number of links in a scheme. However, as with the maximum number of gates, the practical limit is determined by the complexity of the logic. In practice the scheme would have to be very complex, and this error is unlikely to occur.

1.5 Toolbar and commands

There are several toolbars available for easy navigation and editing of PSL.

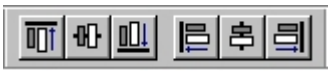
1.5.1 Standard tools

- For file management and printing.



1.5.2 Alignment tools

- To snap logic elements into horizontally or vertically aligned groupings.



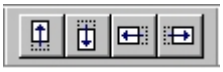
1.5.3 Drawing tools

- To add text comments and other annotations, for easier reading of PSL schemes.



1.5.4 Nudge tools

- To move logic elements.



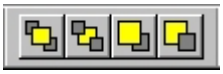
1.5.5 Rotation tools

- Tools to spin, mirror and flip.



1.5.6 Structure tools

- To change the stacking order of logic components.



1.5.7 Zoom and pan tools

- For scaling the displayed screen size, viewing the entire PSL, or zooming to a selection.



1.5.8 Logic symbols

- P343/4/5/6 logic symbols



- P342 logic symbols



This toolbar provides icons to place each type of logic element into the scheme diagram. Not all elements are available in all devices. Icons will only be displayed for those elements available in the selected device.

PL

Link 

Create a link between two logic symbols.

Opto Signal 

Create an opto signal.

Input Signal 

Create an input signal.

Output Signal 

Create an output signal.

GOOSE In 

Create an input signal to logic to receive an IEC 61850 GOOSE message transmitted from another IED.

GOOSE Out 

Create an output signal from logic to transmit an IEC 61850 GOOSE message to another IED.

Control In 

Create an input signal to logic that can be operated from an external command.

Function Key 

Create a function key input signal.

Trigger Signal 

Create a fault record trigger.

LED Signal 

Create an LED input signal that repeats the status of tri-color LED (P343/4/5/6).

Create an LED input signal that repeats the status of red LED (P342). 

Contact Signal 

Create a contact signal.

LED Conditioner 

Create an LED conditioner for tri-color LED (P343/4/5/6) 

Create an LED conditioner for red LED (P342)

Contact Conditioner 

Create a contact conditioner.

Timer 

Create a timer.

AND Gate 

Create an AND Gate.

OR Gate

Create an OR Gate.

Programmable Gate

Create a programmable gate.

Counter

Create a Counter.

1.6 PSL logic signals properties

The logic signal toolbar is used for the selection of logic signals.

Performing a right-mouse click on any logic signal will open a context sensitive menu and one of the options for certain logic elements is the **Properties…** command. Selecting the Properties option will open a Component Properties window, the format of which will vary according to the logic signal selected.

Properties of each logic signal, including the Component Properties windows, are shown in the following sub-sections:

Signal properties menu

The **Signals List** tab is used for the selection of logic signals.

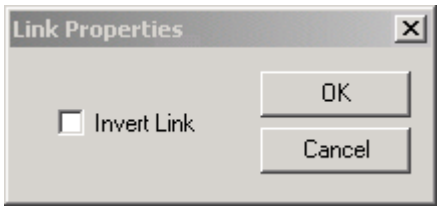
The signals listed will be appropriate to the type of logic symbol being added to the diagram. They will be of one of the following types:

PL

1.6.1 Link properties

Links form the logical link between the output of a signal, gate or condition and the input to any element.

Any link that is connected to the input of a gate can be inverted via its properties window. An inverted link is indicated with a “bubble” on the input to the gate. It is not possible to invert a link that is not connected to the input of a gate.



Links can only be started from the output of a signal, gate, or conditioner, and can only be ended on an input to any element.

Signals can only be an input or an output. To follow the convention for gates and conditioners, input signals are connected from the left and output signals to the right. The Editor will automatically enforce this convention.

A link attempt will be refused where one or more rules would otherwise be broken. A link will be refused for the following reasons:

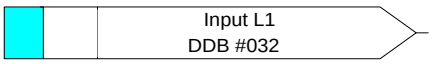
- An attempt to connect to a signal that is already driven. The cause of the refusal may not be obvious, since the signal symbol may appear elsewhere in the diagram. Use “Highlight a Path” to find the other signal.
- An attempt is made to repeat a link between two symbols. The cause of the refusal may not be obvious, since the existing link may be represented elsewhere in the diagram.

1.6.2 Opto signal properties

Opto Signal

Each opto input can be selected and used for programming in PSL. Activation of the opto input will drive an associated DDB signal.

For example activating opto input L1 will assert DDB 032 in the PSL.

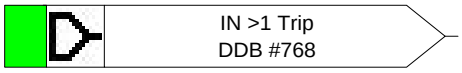


1.6.3 Input signal properties

Input Signal

Relay logic functions provide logic output signals that can be used for programming in PSL. Depending on the relay functionality, operation of an active relay function will drive an associated DDB signal in PSL.

For example DDB 768 will be asserted in the PSL should the active earth fault 1, stage 1 protection operate/trip.

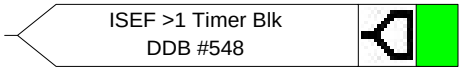


1.6.4 Output signal properties

Output Signal

Relay logic functions provide logic input signals that can be used for programming in PSL. Depending on the relay functionality, activation of the output signal will drive an associated DDB signal in PSL and cause an associated response to the relay function

For example, if DDB 548 is asserted in the PSL, it will block the sensitive earth function stage 1 timer.



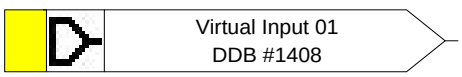
1.6.5 GOOSE input signal properties

GOOSE In

The Programmable Scheme Logic interfaces with the GOOSE Scheme Logic (see S1 users manual) by means of 32 Virtual inputs. The Virtual Inputs can be used in much the same way as the Opto Input signals.

The logic that drives each of the Virtual Inputs is contained within the relay's GOOSE Scheme Logic file. It is possible to map any number of bit-pairs, from any enrolled device, using logic gates onto a Virtual Input (see S1 Users manual for more details).

For example DDB 1408 will be asserted in PSL should virtual input 1 and its associated bit pair operate.



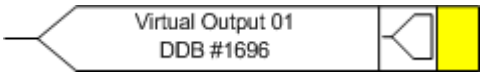
1.6.6 GOOSE output signal properties

GOOSE Out

The Programmable Scheme Logic interfaces with the GOOSE Scheme Logic by means of 32 Virtual outputs.

It is possible to map virtual outputs to bit-pairs for transmitting to any enrolled devices (see S1 Users manual for more details).

For example if DDB 1696 is asserted in PSL, Virtual Output 32 and its associated bit-pair mappings will operate.



1.6.7 Control input signal properties

Control Inputs

There are 32 control inputs which can be activated via the relay menu, 'hotkeys' or via rear communications. Depending on the programmed setting i.e. latched or pulsed, an associated DDB signal will be activated in PSL when a control input is operated.

For example operate control input 1 to assert DDB 1376 in the PSL.



1.6.8 Function key properties (P343/4/5/6/8 only)

Function Key

Each function key can be selected and used for programming in PSL. Activation of the function key will drive an associated DDB signal and the DDB signal will remain active depending on the programmed setting i.e. toggled or normal. Toggled mode means the DDB signal will remain latched or unlatched on key press and normal means the DDB will only be active for the duration of the key press.

For example operate function key 1 to assert DDB 256 in the PSL.

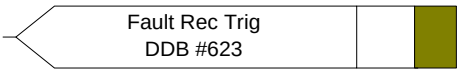


1.6.9 Fault recorder trigger properties

Fault Record Trigger

The fault recording facility can be activated, by driving the fault recorder trigger DDB signal.

For example assert DDB 623 to activate the fault recording in the PSL.

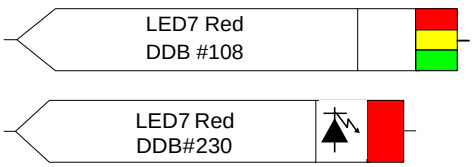


1.6.10 LED signal properties

LED

All programmable LEDs will drive associated DDB signal when the LED is activated.

For example DDB 108 will be asserted when tri-color LED 7 is activated (P343/4/5/6/8) and DDB 230 for red LED 7 (P342).



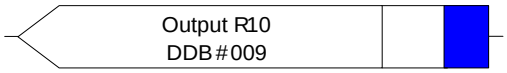
1.6.11 Contact signal properties

Contact Signal

All relay output contacts will drive associated DDB signal when the output contact is activated.

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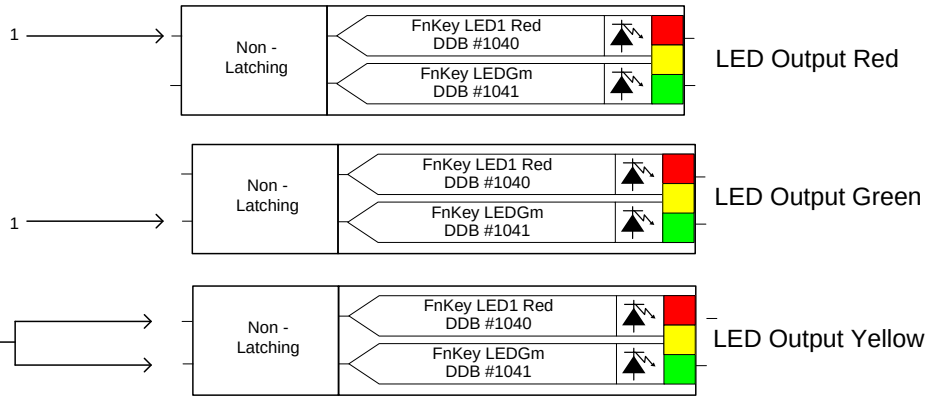
For example DDB 009 will be asserted when output R10 is activated.



1.6.12 LED conditioner properties

Tri-color LED Conditioner (P343/4/5/6/8)

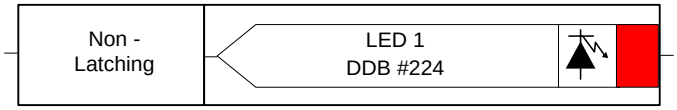
1. Select the **LED name** from the list (only shown when inserting a new symbol).
2. Configure the LED output to be Red, Yellow or Green.
3. Configure a Green LED by driving the Green DDB input.
4. Configure a RED LED by driving the RED DDB input.
5. Configure a Yellow LED by driving the RED and GREEN DDB inputs simultaneously.



6. Configure the LED output to be latching or non-latching.

Red LED Conditioner (P342)

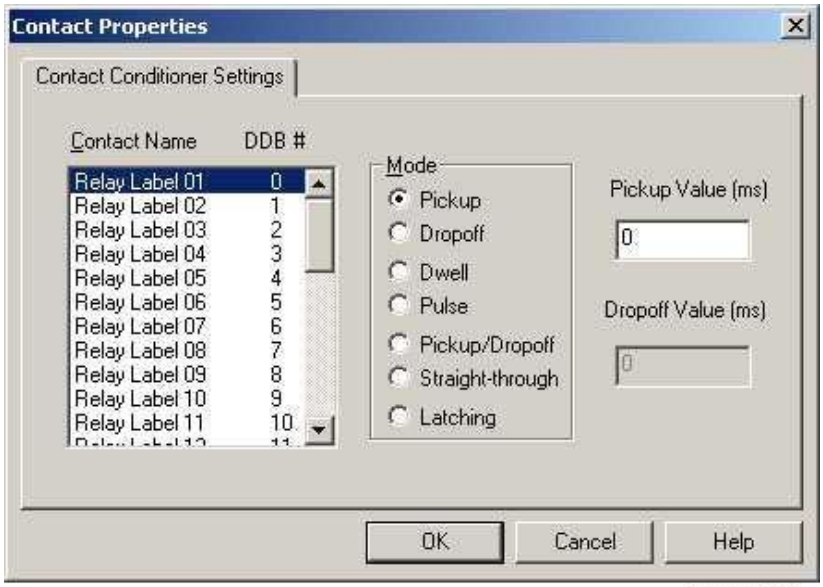
1. Select the LED name from the list (only shown when inserting a new symbol).
2. Configure the LED output to be latching or non-latching



1.6.13 Contact conditioner properties

Each contact can be conditioned with an associated timer that can be selected for pick up, drop off, dwell, pulse, pick-up/drop-off, straight-through, or latching operation.

“Straight-through” means it is not conditioned in any way whereas “latching” is used to create a sealed-in or lockout type function.



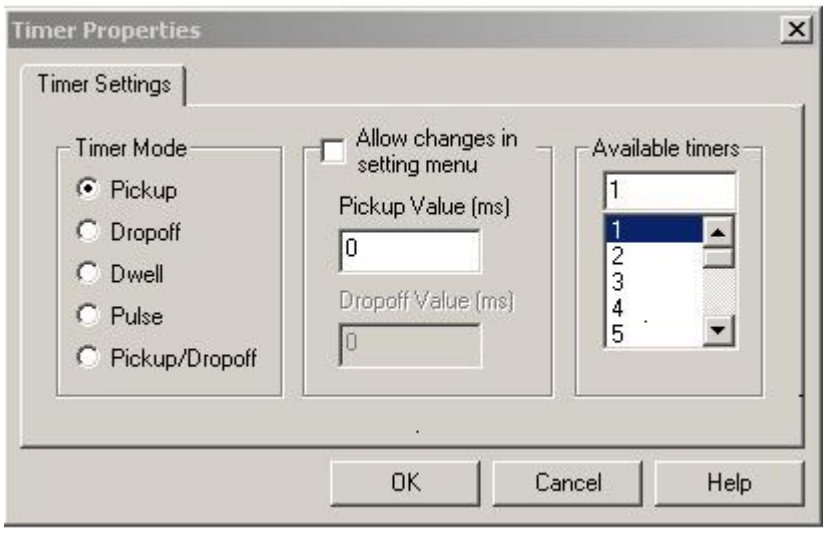
S0083ENa

1. Select the contact name from the Contact Name list (only shown when inserting a new symbol).
2. Choose the conditioner type required in the **Mode** tick list.
3. Set the **Pick-up** Time (in milliseconds), if required.
4. Set the **Drop-off** Time (in milliseconds), if required.

1.6.14 Timer properties



Each timer can be selected for pick up, drop off, dwell, pulse or pick-up/drop-off operation.



1. Choose the operation mode from the **Timer Mode** tick list.
2. Select the **Allow changes in the setting menu** check box if you want to change the timer settings in the setting file via **System Config** – **Timer 1-16** cells. Otherwise timer settings can be set in the PSL.
3. Set the Drop-off Time (in milliseconds), if required.

1.6.15 Gate properties

 or  or 

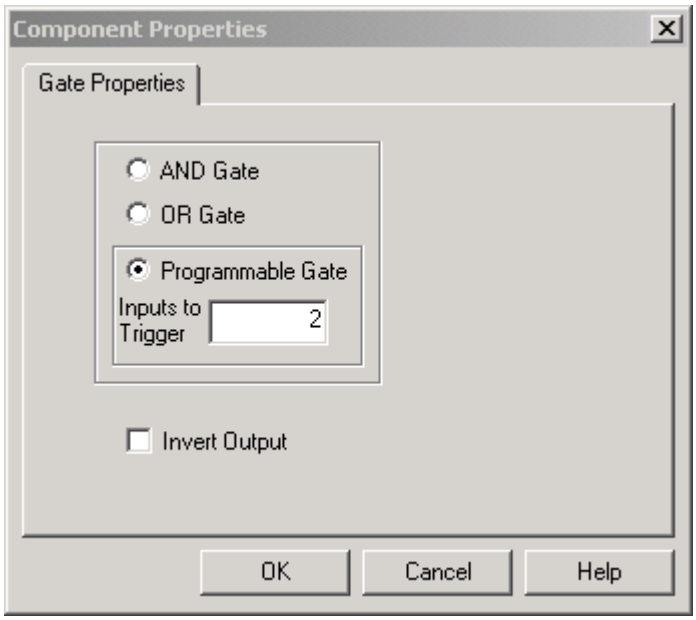
A Gate may be an **AND**, **OR**, or **Programmable Gate**.

An **AND** gate  requires that all inputs are TRUE for the output to be TRUE.

An **OR** gate  requires that one or more input is TRUE for the output to be TRUE.

PL

A **Programmable Gate** requires that the number of inputs that are TRUE is equal to or greater than its 'Inputs to Trigger' setting for the output to be TRUE.

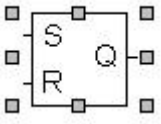


1. Select the Gate type **AND**, **OR**, or **Programmable**.
2. Set the number of inputs to trigger when a Programmable Gate is selected.
3. Select if the output of the gate should be inverted using the Invert Output check box. An inverted output is indicated with a "bubble" on the gate output.

PL

1.6.16 SR programmable gate properties

Each PSL S-R gate has a Set (S) and Reset (R) input and an output (Q).



A Programmable SR gate can be selected to operate with the following three latch properties:

Set	Reset	Q0 (Previous Output State)	Q1 Set Dominant	Q1 Reset Dominant	Q1 No Dominance
0	0	0	0	0	0
0	0	1	1	1	1
0	1	1	0	0	0
0	1	0	0	0	0
1	1	0	1	0	0
1	1	1	1	0	1
1	0	1	1	1	1
1	0	0	1	1	1

Q0 is the previous output state of the latch before the inputs change. Q1 is the output of the latch after the inputs change.

The Set dominant latch ignores the Reset if the Set is on.

The Reset Dominant latch ignores the Set if the Reset is on.

When both Set and Reset are on, the output of the non-dominant latch depends on its previous output Q0. Therefore if Set and Reset are energised simultaneously, the output state does not change.

Note: Use a set or reset dominant latch. Do not use a non-dominant latch unless this type of operation is required.

1.6.17 SR latch properties

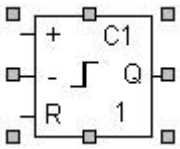
In the Component Properties dialog, you can select S-R latches as **Standard (no input dominant), Set input dominant** or **Reset input dominant**.

If you want the output to be inverted, check the **Invert Output** check box. An inverted output appears as a "bubble" on the gate output.

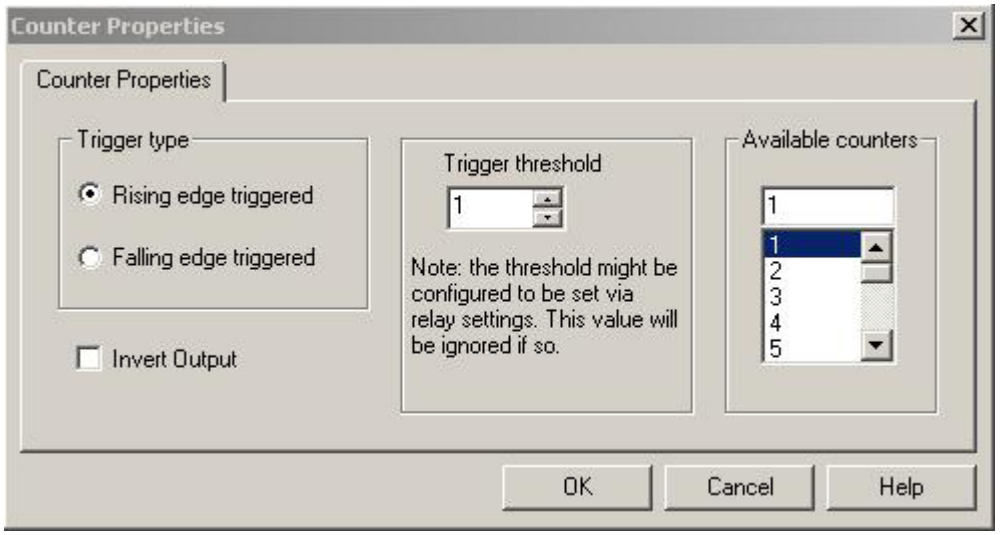


1.6.18 Counter properties

Each PSL counter has an increment (+), a decrement (-) and Reset (R) input and a count output (Q) which goes high when the count threshold value is exceeded.



In the Counter Properties dialog, you can select the **Trigger type** as **Rising Edge** or **Falling Edge**. The counter threshold can be set in the **Trigger threshold** box and the counter number can be set in the Available counter box.



1. Choose the trigger operation mode, **Rising Edge** or **Falling Edge** from the **Trigger Type**.
2. Set the counter threshold value (1-65535) in the **Trigger threshold**.

   Note: The counter threshold can be set in the menu settings, System Config - Counters **1-16** settings if the **CounterSourcePSL** setting = 0000000000000000 for all 16 counters.

   If the **CounterSourcePSL** setting = 1111111111111111, all 16 counters can be set via the counter properties in the PSL.
3. Select the counter number (1-16) from the **Available counters**.

PL

1.7 Description of logic nodes

DDB no.	English text	Source	Description
0	Output R1 (Output Label Setting)	Relay conditioner	Output Relay 1 is on (P342-6/8)
31	Output R32 (Output Label Setting)	Relay conditioner	Output Relay 32 is on (P342-6/8)
32	Input L1 (Input Label Setting)	Opto Isolator Input	Opto Input 1 is on (P342-6/8)
63	Input L32 (Input Label Setting)	Opto Isolator Input	Opto Input 32 is on (P342-6/8)
64	Relay Cond 1	PSL	Input signal driving Relay 1 is on (P342-6/8)
95	Relay Cond 32	PSL	Input signal driving Relay 32 is on (P342-6/8)
96	LED1 Red	PSL	Programmable LED 1 Red is on (P343-6/8)
97	LED1 Grn.	PSL	Programmable LED 1 Green is on (P343-6/8)
110	LED8 Red	PSL	Programmable LED 8 Red is on (P343-6/8)
111	LED8 Grn.	PSL	Programmable LED 8 Green is on (P343-6/8)
112	FnKey LED1 Red	PSL	Programmable Function Key LED 1 Red is on (P343-6/8)
113	FnKey LED1 Grn.	PSL	Programmable Function Key LED 1 Green is on (P343-6/8)
130	FnKey LED10 Red	PSL	Programmable Function Key LED 10 Red is on (P343-6/8)
131	FnKey LED10 Grn.	PSL	Programmable Function Key LED 10 Green is on (P343/4/5/6/8)
132 to 159	Not Used		
160	LED1 Con R	PSL	Input signal driving LED 1 Red is on (P343-6/8)

DDB no.	English text	Source	Description
161	LED1 Con G	PSL	Input signal driving LED 1 Green is on. To make LED 1 Yellow DDB 160 and DDB 161 must on at the same time. (P343-6/8)
174	LED8 Con R	PSL	Input signal driving LED 8 Red is on (P343-6/8)
175	LED8 Con G	PSL	Input signal driving LED 8 Green is on. To make LED 8 Yellow DDB 174 and DDB 175 must be on at the same time (P343-6/8)
176	FnKey LED1 ConR	PSL	Input signal driving Function Key LED 1 Red is on. This LED is associated with Function Key 1 (P343-6/8)
177	FnKey LED1 ConG	PSL	Input signal driving Function Key LED 1 Green is on. This LED is associated with Function Key 1. To make function key 1 LED, yellow DDB 176 and DDB 177 must be on at the same time (P343-6/8)
194	FnKey LED10 ConR	PSL	Input signal driving Function Key LED 10 Red is on. This LED is associated with Function Key 10 (P343-6/8)
195	FnKey LED10 ConG	PSL	Input signal driving Function Key LED 10 Green is on. This LED is associated with Function Key 10. To make function key LED 10 yellow, DDB 194 and DDB 195 must be on at the same time (P343-6/8)
196 to 223	Not Used		
224	LED1	LED conditioner	Programmable LED 1 is on (P341/2)
231	LED8	LED conditioner	Programmable LED 8 is on (P341/2)
232	LED Cond IN 1	PSL	Input signal driving LED 1 is on (P341/2))
239	LED Cond IN 8	PSL	Input signal driving LED 8 is on (P341/2)
240 to 255	Not Used		
256	Function Key 1	User Control	Function Key 1 is on. In ‘Normal’ mode it is high on keypress and in ‘Toggle’ mode remains high/low on single keypress (P343/4/5/6/8)
265	Function Key 10	User Control	Function Key 10 is on. In ‘Normal’ mode it is high on keypress and in ‘Toggle’ mode remains high/low on single keypress (P343/4/5/6/8)
266 to 287	Not Used		
288	Timer out 1	Auxiliary Timer out	Output from Auxiliary Timer 1 is on (P342-6/8)
303	Timer out 16	Auxiliary Timer out	Output from Auxiliary Timer 16 is on (P342-6/8)
304 to 319	Not Used		
320	Timer in 1	PSL	Input to Auxiliary Timer 1 is on (P342-6/8)
335	Timer in 16	PSL	Input to Auxiliary Timer 16 is on (P342-6/8)
336 to 352	Not Used		
353	F out of Range	Frequency Tracking	Frequency out of range. Frequency tracking range is 5-70 Hz (P342-6/8)
354	SG-DDB Invalid	Group Selection	Setting Group Selection DDB inputs have detected an invalid (disabled) settings group (P342-6/8)
355	Prot'n Disabled	Commissioning Test	Protection Disabled - typically out of service due to test mode (P342-6/8)
356	VT Fail Alarm	VT Supervision	VTS Indication alarm - failed VT (fuse blow) detected by VT supervision (P342-8)
357	CT-1 Fail Alarm	CT Supervision	CTS Indication Alarm for IA/IB/IC (CT supervision alarm) (P342-6)
358	CB Fail Alarm	Breaker Fail	Circuit Breaker Fail Alarm (P342-6)

DDB no.	English text	Source	Description
359	I ^ Maint Alarm	CB Monitoring	Circuit Breaker cumulative broken current has exceeded the Maintenance Alarm setting (P342-6)
360	I ^ Lockout Alarm	CB Monitoring	Circuit Breaker cumulative broken current has exceeded the Maintenance Lockout setting (P342-6)
361	CB Ops Maint.	CB Monitoring	Number of Circuit Breaker trips has exceeded Maintenance Alarm setting (P342-6)
362	CB Ops Lockout	CB Monitoring	Number of Circuit Breaker trips has exceeded the Maintenance Lockout setting (P342-6)
363	CB Op Time Maint.	CB Monitoring	Circuit Breaker operating time has exceeded Maintenance Alarm setting (slow interruption time) (P342-6)
364	CB Op Time Lock	CB Monitoring	Circuit Breaker operating time has exceeded the Lockout Alarm setting (too slow interruption) (P342-6)
365	Fault Freq. Lock	CB Monitoring	Excessive Fault Frequency Lockout Alarm (too many trips in a set time) (P342-6)
366	CB Status Alarm	CB Status	Indication of a fault with the Circuit Breaker state monitoring - example defective auxiliary contacts (P343-6)
367	Man CB Trip Fail	CB Control	Circuit Breaker failed to trip (after a manual/operator trip command) (P343-8)
368	Man CB Cls. Fail	CB Control	Circuit Breaker failed to close (after a manual/operator close command) (P343-6)
369	Man CB Unhealthy	CB Control	Manual Circuit Breaker Unhealthy output signal indicating that the circuit breaker has not closed successfully after a manual close command. (A successful close requires the Circuit Breaker Healthy signal to appear within the "healthy window" time) (P343-6)
370	NPS Thermal Alarm	NPS Thermal	Negative phase sequence thermal alarm (P342-6)
371	Gen Thermal Alm	Thermal Alarm	Thermal Alarm (P342-6)
372	V/Hz Alarm	Overfluxing	Overflux Alarm (voltage/frequency) (P342-6)
373	Field Fail Alarm	Field Failure	Field failure alarm (P342-6)
374	RTD Thermal Alarm	RTD Protection	Operation of any RTD 1-10 Alarm (DDB 1031-1040) (P342-6)
375	RTD Open Cct	RTD Protection	RTD open circuit (the RTD Open Cct cell in Measurements 3 indicates which RTD is open circuit) (P342-6)
376	RTD Short Cct	RTD Protection	RTD short circuit circuit (the RTD Short Cct cell in Measurements 3 indicates which RTD is open circuit) (P342-6)
377	RTD Data Error	RTD Protection	RTD data inconsistency error (the RTD Data Error cell in Measurements 3 indicates which RTD has a data error) (P342-6)
378	RTD Board Fail	RTD Protection	Self checking has identified a failure of the RTD board (P342-6)
379	Freq Prot Alarm	PSL	F<1 Trip OR F<2 Trip OR F<3 Trip OR F>1 Trip (P343-6). The F>1 Trip OR F>2 Trip (P348) (These DDB signals are mapped to Freq Prot Alarm in default PSL) (P343-6)
380	Voltage Prot Alarm	PSL	V<1 Trip OR V>1 Trip (P342-6). The V>1 Peak Trip OR V>2 Peak Trip OR V>3 RMS Trip OR V>4 RMS Trip (P348). (These DDB signals are mapped to Voltage Prot Alarm in default PSL)

DDB no.	English text	Source	Description
381	CT-2 Fail Alarm	CT Supervision	CTS Indication Alarm for IA-2/IB-2/IC-2 (CT supervision alarm). (P343-6/8)
382	64S R<1 Alarm	64S 100% Stator Earth Fault	Low frequency injection 100% stator earth fault under resistance stage 1 alarm (P345)
383	64S Fail Alarm	64S 100% Stator Earth Fault	Low frequency injection 100% stator earth fault supervision alarm (P345). DDB 383 is connected to DDB 1076 '64S Fail' in default PSL to give supervision alarm.
384	CL Card I/P Fail	Current Loop Inputs	Current Loop Input (transducer input) failure (P343-6/8)
385	CL Card O/P Fail	Current Loop Outputs	Current Loop Output (transducer output) failure (P343-6/8)
386	CL Input 1 Alarm	Current Loop Inputs	Current Loop Input (transducer input) 1 alarm (P343-6/8)
387	CL Input 2 Alarm	Current Loop Inputs	Current Loop Input (transducer input) 2 alarm (P343-6/8)
388	CL Input 3 Alarm	Current Loop Inputs	Current Loop Input (transducer input) 3 alarm (P343-6/8)
389	CL Input 4 Alarm	Current Loop Inputs	Current Loop Input (transducer input) 4 alarm (P343-6/8)
390	CLI1 I< Fail Alm	Current Loop Inputs	Current Loop Input (transducer input) 1 undercurrent alarm (current is <4 mA for 4-20 mA input)
391	CLI2 I< Fail Alm	Current Loop Inputs	Current Loop Input (transducer input) 2 undercurrent alarm (current is <4 mA for 4-20 mA input) (P343-6/8)
392	CLI3 I< Fail Alm	Current Loop Inputs	Current Loop Input (transducer input) 3 undercurrent alarm (current is <4 mA for 4-20 mA input) (P343-6/8)
393	CLI4 I< Fail Alm	Current Loop Inputs	Current Loop Input (transducer input) 4 undercurrent alarm (current is <4 mA for 4-20 mA input) (P343-6/8)
394	64R R<1 Alarm	64R Rotor Earth Fault	1st Stage Rotor Earth Fault Under Resistance Alarm (P342-6)
395	64R CL I/P Fail	64R Rotor Earth Fault	Rotor Earth Fault Current Loop Input (transducer input) Failure (P342-6)
394	9-2LE Data Alarm	NCIT	Abnormal state of IEC 61850-9-2LE sample (P348)
395	9-2LE Cfg Alarm	NCIT	Error in IEC 61850-9-2LE configuration (P348)
396	CT Mismatch Alm	Ratio Correction	CT parameter mismatch alarm (P342-6)
397	Loss of Life Alarm	Thermal Overload	Loss of Life Alarm (P342-6)
398	FAA Alarm	Thermal Overload	Aging Acceleration Factor Alarm (P342-6)
399	Thru Fault Alm	TF Monitoring	Through Fault Alarm (P342-6)
400	Circuit Flt Alm	Circuitry Fail	Circuit Fail Alarm (P342-6)
401	XThermPretrp Alm	Thermal Overload	Transformer Thermal Top Oil Pre-trip Alarm (P342-6)
402	Diff CTS Alm	Diff CTS	Differential CT Fail Alarm
403	Man No Checksync	CB Control	Indicates that the check synchronization signal has failed to appear for a manual close (P343-6)
404	System Split Alm	Sys Check	System Split alarm – will be raised if the system is split (remains permanently out of synchronism) for the duration of the system split timer (P342-6)
405	Pslip Angle Alm	PSL	Pole Slipping Alarm from phase angle method logic (P342-6)

DDB no.	English text	Source	Description
406	Pslip Power Alm	PSL	Pole Slipping Alarm from power method logic (P342-6)
405	MR User Alarm 11	PSL	User Alarm 11 (manual-resetting) (P348)
406	MR User Alarm 10	PSL	User Alarm 10 (manual-resetting) (P348)
407	MR User Alarm 9	PSL	User Alarm 9 (manual-resetting) (P343-6/8)
411	MR User Alarm 5	PSL	User Alarm 5 (manual-resetting) (P343-6/8)
412	SR User Alarm 4	PSL	User Alarm 4 (self-resetting) (P343-6/8)
415	SR User Alarm 1	PSL	User Alarm 1 (self-resetting) (P343-6/8)
416	Battery Fail	Self monitoring	Front panel miniature battery failure - either battery removed from slot, or low voltage (P343-6/8)
417	Field Volts Fail	Self monitoring	48 V Field Voltage Failure (P343-6/8)
418	Rear Comms 2 Fail	InterMiCOM	2nd Rear Comms Port Failure (P343-6/8)
419	GOOSE IED Absent	UCA2	The IED is not subscribed to a publishing IED in the current scheme (P343-6/8)
420	NIC Not Fitted	UCA2	Ethernet board not fitted (P343-6/8)
421	NIC No Response	UCA2	Ethernet board not responding (P343-6/8)
422	NIC Fatal Error	UCA2	Ethernet board unrecoverable error (P343-6/8)
423	NIC Soft Reload	UCA2	Ethernet board software reload alarm (P343-6/8)
424	Bad TCP/IP Cfg	UCA2	Bad TCP/IP configuration alarm (P343-6/8)
425	Bad OSI Config	UCA2	Bad OSI configuration alarm (P343-6/8)
426	NIC Link Fail	UCA2	Ethernet link lost (P343-6/8)
427	NIC SW Mis-Match	UCA2	Ethernet board software not compatible with main CPU (P343-6/8)
428	IP Addr Conflict	UCA2	The IP address of the IED is already used by another IED (P343-6/8)
429 to 432	Not Used		
433	Backup Setting	Self monitoring	This is an alarm that is ON if any setting fails during the setting changing process. If this happens, the relay will use the last known good setting (P343-6/8)
434	Reserved	Self monitoring	Bad DNP Settings (P343-6/8)
435	Backup Usr Curve	Self monitoring	This is an alarm that is ON if any user curve fails during the user curve download process. If this happens, the relay will use the last known good user curve (P343-6/8)
436	SNTP Failure	UCA2	SNTP failure (P342-8)
437	NIC MemAllocFail	UCA2	MMS libraries memory allocation has failed (P342-8)
438 to 511	Not Used		
512	Gen Diff Block	PSL	Block Generator Differential trip (P343-6)
513	Xform Diff Block	PSL	Block Transformer Differential protection (P343-6)
514	Inhibit Diff CTS	PSL	Inhibit Differential Current Transformer Supervision (P343-6)
515 to 543	Not Used		
544	IN>1 Timer Blk	PSL	Block Earth Fault Stage 1 time delay (P342-6)
545	IN>2 Timer Blk	PSL	Block Earth Fault Stage 2 time delay (P342-6)
546, 547	Not Used		
548	ISEF>1 Timer Blk	PSL	Block SEF Stage 1 time delay (P342-6)
549 to 551	Not used	PSL	

DDB no.	English text	Source	Description
552	64S I>1 Inhibit	PSL	Inhibit 64S Overcurrent Protection (P345)
553	64S R<1 Inhibit	PSL	Inhibit 64S Under Impedance Stage 1 (P345)
554	64S R<2 Inhibit	PSL	Inhibit 64S Under Impedance Stage 2 (P345)
555	64S Filter On	PSL	Enable the 64S band pass filter permanently (P345)
556	64R R<1 Inhibit	PSL	Inhibit 64R Under Impedance Stage 1 (P342-6)
557	64R R<2 Inhibit	PSL	Inhibit 64R Under Impedance Stage 2 (P342-6)
558 to 567	Not Used		
568	I>1 Peak Inhibit	PSL	Inhibit Phase Overcurrent Stage 1 - Peak (P348)
569	I>2 Peak Inhibit	PSL	Inhibit Phase Overcurrent Stage 2 - Peak (P348)
570	I>3 Peak Inhibit	PSL	Inhibit Phase Overcurrent Stage 3 - Peak (P348)
571	I>4 Peak Inhibit	PSL	Inhibit Phase Overcurrent Stage 4 - Peak (P348)
572	I>5 RMS Inhibit	PSL	Inhibit Phase Overcurrent Stage 1 - RMS (P348)
573	I>6 RMS Inhibit	PSL	Inhibit Phase Overcurrent Stage 2 - RMS (P348)
574	I>7 RMS Inhibit	PSL	Inhibit Phase Overcurrent Stage 3 - RMS (P348)
575	I>8 RMS Inhibit	PSL	Inhibit Phase Overcurrent Stage 4 - RMS (P348)
576	I>1 Timer Block	PSL	Block Phase Overcurrent Stage 1 Time delayed trip (P342-6)
577	I>2 Timer Block	PSL	Block Phase Overcurrent Stage 2 Time delayed trip (P342-6)
578	I>3 Timer Block	PSL	Block Phase Overcurrent Stage 3 Time delayed trip (P342-6)
579	I>4 Timer Block	PSL	Block Phase Overcurrent Stage 4 Time delayed trip (P342-6)
580 to 581	Not Used		
582	I2> Inhibit	PSL	Inhibit all Negative Sequence Overcurrent stages (P342-6)
583	I2>1 Timer Block	PSL	Block Negative Sequence Overcurrent Stage 1 Time delayed trip (P342-6)
584	I2>2 Timer Block	PSL	Block Negative Sequence Overcurrent Stage 2 Time delayed trip (P342-6)
585	I2>3 Timer Block	PSL	Block Negative Sequence Overcurrent Stage 3 Time delayed trip (P342-6)
586	I2>4 Timer Block	PSL	Block Negative Sequence Overcurrent Stage 4 Time delayed trip (P342-6)
587	I2>1 Inhibit	PSL	Inhibit Negative Sequence Overcurrent Stage 1 (P348)
588	I2>2 Inhibit	PSL	Inhibit Negative Sequence Overcurrent Stage 2 (P348)
589	I2>3 Inhibit	PSL	Inhibit Negative Sequence Overcurrent Stage 3 (P348)
590	I2>4 Inhibit	PSL	Inhibits Negative Sequence Overcurrent Stage 4 (P348)
591	V<3 Timer Block	PSL	Block Phase Undervoltage Stage 3 time delay (P342-6)

DDB no.	English text	Source	Description
592	VN>1 Timer Blk	PSL	Block Residual Overvoltage Stage 1 time delay (P342-6)
593	VN>2 Timer Blk	PSL	Block Residual Overvoltage Stage 2 time delay (P342-6)
594	VN>3 Timer Block	PSL	Block Residual Overvoltage Stage 3 Timer (P342-6)
595	VN>4 Timer Block	PSL	Block Residual Overvoltage Stage 4 Timer (P342-6)
596	VN>5 Timer Block	PSL	Block Residual Overvoltage Stage 5 Time delayed trip (P344/5 only) (P342-6)
597	VN>6 Timer Block	PSL	Block Residual Overvoltage Stage 6 Time delayed trip (P344/5 only) (P342-6)
598	V>1 Timer Block	PSL	Block Phase Overvoltage Stage 1 time delay (P342-6)
599	V>2 Timer Block	PSL	Block Phase Overvoltage Stage 2 time delay (P342-6)
600	V2>1 Accelerate	PSL	Accelerate NPS Overvoltage Stage 1 Start (P342-6)
601	V<1 Timer Block	PSL	Block Phase Undervoltage Stage 1 time delay (P342-6)
602	V<2 Timer Block	PSL	Block Phase Undervoltage Stage 2 time delay (P342-6)
603	Not Used		
604	V>1 Peak Inhibit	PSL	Inhibit Peak Phase Overvoltage Stage 1 (P348)
605	V>2 Peak Inhibit	PSL	Inhibit Peak Phase Overvoltage Stage 2 (P348)
606	V>3 RMS Inhibit	PSL	Inhibit RMS Phase Overvoltage Stage 3 (P348)
607	V>4 RMS Inhibit	PSL	Inhibit RMS Phase Overvoltage Stage 4 (P348)
608	VDepOC Timer Blk	PSL	Block Voltage Dependent Overcurrent Time delayed trip (voltage controlled or voltage restrained overcurrent) (P342-6)
609	UnderZ Timer Blk	PSL	Block Underimpedance Time delayed trip (Stage 1 and 2) (P342-6)
610	VN>1 Inhibit	PSL	Inhibit Residual Overvoltage Stage 1 (P348)
611	VN>2 Inhibit	PSL	Inhibit Residual Overvoltage Stage 2 (P348)
612 to 619	Not Used		
620	F>1 Inhibit	PSL	Inhibit Overfrequency Stage 1 (P348)
621	F>2 Inhibit	PSL	Inhibit Overfrequency Stage 2 (P348)
622	F>3 Inhibit	PSL	Inhibit Overfrequency Stage 3 (P348)
623	F>4 Inhibit	PSL	Inhibit Overfrequency Stage 4 (P348)
624	Not Used		
625	V/Hz>1 Inhibit	PSL	Inhibit Volts per Hz Stage 1 (P342-6)
626	F<1 Timer Block	PSL	Block Underfrequency Stage 1 Timer (P342-6)
627	F<2 Timer Block	PSL	Block Underfrequency Stage 2 Timer (P342-6)
628	F<3 Timer Block	PSL	Block Underfrequency Stage 3 Timer (P342-6)
629	F<4 Timer Block	PSL	Block Underfrequency Stage 4 Timer (P342-6)
630	F>1 Timer Block	PSL	Block Overfrequency Stage 1 Timer (P342-6)
631	F>2 Timer Block	PSL	Block Overfrequency Stage 2 Timer (P342-6)
632	Turbine F Inh	PSL	Inhibit Turbine Abnormal Frequency Protection (P342-6)

DDB no.	English text	Source	Description
633	df/dt> Inhibit	PSL	Inhibit df/dt Protection (P342-6)
634	df/dt>1 Tmr Blk	PSL	Block df/dt Stage 1 Timer (P342-6)
635	df/dt>2 Tmr Blk	PSL	Block df/dt Stage 2 Timer (P342-6)
636	df/dt>3 Tmr Blk	PSL	Block df/dt Stage 3 Timer (P342-6)
637	df/dt>4 Tmr Blk	PSL	Block df/dt Stage 4 Timer (P342-6)
638 to 639	Not used		
640	Reset I2 Thermal	PSL	Reset NPS Thermal State (P342-6)
641	Reset GenThermal	PSL	Reset Thermal Overload State (P342-6)
642 to 648	Not used		
649	Reset XThermal	PSL	Reset Transformer Thermal Overload State (P342-6)
650	Forced Air Cool	PSL	If DDB 650 = 1 then cooling mode is Forced Air Cooling, if DDB 651 = 1 then cooling mode is Forced Oil Cooling, if DDB 650 and 651 = 1 then cooling mode is Forced Air Oil Cooling, if DDB 650 and 651 = 0 then cooling mode is Natural Cooling (P342-6)
651	Forced Oil Cool	PSL	As above (P342-6)
652	TFR De-energized	PSL	Transformer de-energized status (P342-6)
653	Field Fail1 Inh	PSL	Inhibit Field Failure Stage 1 (P342-6)
654	Field Fail2 Inh	PSL	Inhibit Field Failure Stage 2 (P342-6)
655	FFail Alarm Inh	PSL	Inhibit Field Failure Alarm (P342-6)
656	CL1 Input 1 Blk	PSL	Block Current Loop Input (transducer input) 1 (P342-6/8)
657	CL1 Input 2 Blk	PSL	Block Current Loop Input (transducer input) 2 (P342-6/8)
658	CL1 Input 3 Blk	PSL	Block Current Loop Input (transducer input) 3 (P342-6/8)
659	CL1 Input 4 Blk	PSL	Block Current Loop Input (transducer input) 4 (P342-6/8)
660	SPower1 Inhibit	PSL	Inhibit Sensitive Power Stage 1 (P342-6)
661	SPower2 Inhibit	PSL	Inhibit Sensitive Power Stage 2 (P342-6)
662	SPower3 Inhibit	PSL	Inhibit Sensitive Power Stage 3 (P342-6)
663	SPower4 Inhibit	PSL	Inhibit Sensitive Power Stage 4 (P342-6)
664	V<1 Inhibit	PSL	Inhibit Undervoltage Stage 1 (P342-6)
665	V<2 Inhibit	PSL	Inhibit Undervoltage Stage 2 (P342-6)
666	V<3 Inhibit	PSL	Inhibit Undervoltage Stage 3 (P342-6)
667	Power1 Inhibit	PSL	Inhibit Power Stage 2 (P342-6)
668	Power2 Inhibit	PSL	Inhibit Power Stage 3 (P342-6)
669	Power3 Inhibit	PSL	Inhibit Power Stage 4 (P342-6)
670	Power4 Inhibit	PSL	Inhibit Power Stage 2 (P342-6)
671	Machine Start	PSL	This DDB is used to switch on the low pass filter 2 after machine start-up to enable accurate measurement of the rotor frequency when the machine is running (P348)
672	Fault REC TRIG	PSL	Trigger for Fault Recorder (P342-6/8)
673	Not used		
674	Any Trip	PSL	Any Trip – All trip signals that are required to operate the Trip LED, initiate the breaker fail protection and initiate the CB monitoring counters are mapped to this signal in the PSL (P342-6/8)

DDB no.	English text	Source	Description
675	SG Select x1	PSL	Setting Group Selector X1 (low bit) - selects SG2 if only DDB 624 signal is on. SG1 is active if both DDB 624 & DDB 625 = 0 SG4 is active if both DDB 624 & DDB 625 = 1 (P342-6/8)
676	SG Select 1x	PSL	Setting Group Selector 1X (high bit) - selects SG3 if only DDB 625 is active. SG1 is active if both DDB 624 & DDB 625 = 0 SG4 is active if both DDB 624 & DDB 625 = 1 (P342-6/8)
677	Test Mode	PSL	Commissioning Tests - automatically places relay in Test Mode which takes the relay out of service and allows secondary injection testing of the relay. For IEC 60870-5-103 protocol spontaneous events and cyclic measured data transmitted whilst the relay is in test mode will have a COT of 'test mode' (P342-6/8)
678	Init Trip CB	PSL	Initiate tripping of circuit breaker from a manual command (P342-6)
679	Init Close CB	PSL	Initiate closing of circuit breaker from a manual command (P342-6)
680	Ext. Trip 3ph	PSL	External Trip 3 phase - allows external protection to initiate breaker fail and circuit breaker condition monitoring counters (P342-6)
681	CB Aux 3ph(52-A)	PSL	52-A (CB closed) CB Auxiliary Input (3 phase) (P342-6)
682	CB Aux 3ph(52-B)	PSL	52-B (CB open) CB Auxiliary Input (3 phase) (P342-6)
683	CB Healthy	PSL	Circuit Breaker Healthy (input to manual close that the CB has enough energy to allow closing) (P342-6)
684	MCB/VTS	PSL	VT supervision input - signal from external Miniature Circuit Breaker showing MCB tripped (P342-6)
685	Monitor Blocked	PSL	For IEC-870-5-103 protocol only, used for "Monitor Blocking" (relay is quiet - issues no messages via SCADA port) (P342-6/8)
686	Command Blocked	PSL	For IEC-870-5-103 protocol only, used for "Command Blocking" (relay ignores SCADA commands) (P342-6/8)
687	Time Synch	PSL	Time Synchronism by Opto Input pulse (P342-6/8)
688	Reset Close Dly.	PSL	Reset Manual Circuit Breaker Close Time Delay (P342-6)
689	Reset Relays/LED	PSL	Reset Latched Relays & LEDs (manual reset of any latched trip contacts and LEDs) (P342-6/8)
690	Reset Lockout	PSL	Reset CB monitoring lockouts (P342-6)
691	Reset All Values	PSL	Reset Circuit Breaker Condition Monitoring Values (P342-6)
692	RP1 Read Only	PSL	Rear Port 1 Remote Read only (P342-6/8)
693	RP2 Read Only	PSL	Rear Port 2 Remote Read only (P342-6/8)
694	NIC Read Only	PSL	Ethernet Rear Port Remote Read only (P342-6/8)
695	103 MonitorBlock	PSL	IEC 60870-5-103 Monitor Block (P342-6/8)
696	103 CommandBlock	PSL	IEC 60870-5-103 Command Block (P342-6/8)

DDB no.	English text	Source	Description
697 to 727	Not used		
728	Monitor Bit 1	Commissioning Test	Monitor Port bit 1 Status
735	Monitor Bit 8	Commissioning Test	Monitor Port bit 8 Status
736	Gen Diff Trip	Gen Differential	Generator Differential Trip (P343-6)
737	Gen Diff Trip A	Gen Differential	Generator Differential Trip A (P343-6)
738	Gen Diff Trip B	Gen Differential	Generator Differential Trip B (P343-6)
739	Gen Diff Trip C	Gen Differential	Generator Differential Trip C (P343-6)
740	Xform Dif Trp	Xformer Differential	Transformer Differential Trip 3ph (P343-6)
741	Xform Dif Trp A	Xformer Differential	Transformer Differential Trip A (P343-6)
742	Xform Dif Trp B	Xformer Differential	Transformer Differential Trip B (P343-6)
743	Xform Dif Trp C	Xformer Differential	Transformer Differential Trip C (P343-6)
744	Xform Bias Trp A	Xformer Differential	Transformer Differential Low Set Trip A (P343-6)
745	Xform Bias Trp B	Xformer Differential	Transformer Differential Low Set Trip B (P343-6)
746	Xform Bias Trp C	Xformer Differential	Transformer Differential Low Set Trip C (P343-6)
747	Xform HS1 Trp A	Xformer Differential	Transformer Differential High Set 1 Trip A (P343-6)
748	Xform HS1 Trp B	Xformer Differential	Transformer Differential High Set 1 Trip B (P343-6)
749	Xform HS1 Trp C	Xformer Differential	Transformer Differential High Set 1 Trip C (P343-6)
750	Xform HS2 Trp A	Xformer Differential	Transformer Differential High Set 2 Trip A (P343-6)
751	Xform HS2 Trp B	Xformer Differential	Transformer Differential High Set 2 Trip B (P343-6)
752	Xform HS2 Trp C	Xformer Differential	Transformer Differential High Set 2 Trip C (P343-6)
753	PSlip Angle Trip	Pole Slip Internal Angle	Pole Slip Angle Trip
754	PSlip Power Trip	Pole Slip Power	Pole Slip Power Trip
755	FFail1 Cnt Trip	Field Failure Counter	Field Failure Stage 1 Counter Trip
756	FFail2 Cnt Trip	Field Failure Counter	Field Failure Stage 2 Counter Trip
757	PSlip Angle In	Pole Slip Internal Angle	Pole Slip Angle Input
758	PSlip Power In	Pole Slip Power	Pole Slip Power Input
759	FFail1 Cnt In	Field Failure Counter	Field Failure Stage 1 Counter Input
760	FFail2 Cnt In	Field Failure Counter	Field Failure Stage 2 Counter Input
761	PSlip Ang Alm In	Pole Slip Internal Angle	Pole Slip Angle Alarm Input
762	PSlip PowAlm In	Pole Slip Power	Pole Slip Power Alarm Input
763 to 767	Not Used		
768	IN>1 Trip	Earth Fault	1st Stage Earth Fault Trip (P342-6)
769	IN>2 Trip	Earth Fault	2nd Stage Earth Fault Trip (P342-6)
770 to 771	Not used		
772	IREF> Trip	Restricted Earth Fault	Restricted Earth Fault Trip (P342-6)
773	ISEF>1 Trip	Sensitive Earth Fault	1st Stage Sensitive Earth Fault Trip (P342-6)
774 to 776	Not Used		
777	100%StEF3H Trip	100% Stator Earth Fault	100% Stator Earth Fault Trip (3rd harmonic) (P343/4/5)
778	64S I>1 Trip	64S 100% Stator Earth Fault	1st Stage 100% Stator Earth Fault Overcurrent Trip (Low frequency injection) (P345)

DDB no.	English text	Source	Description
779	64S R<2 Trip	64S 100% Stator Earth Fault	2nd Stage 100% Stator Earth Fault Under Resistance Trip (Low frequency injection) (P345)
780	64R R<2 Trip	64R Rotor Earth Fault	2nd Stage Rotor Earth Fault Under Resistance Trip (P342-6)
784	I>1 Peak Trip	Phase Overcurrent	1st Stage Overcurrent Trip 3ph - Peak (P348)
785	I>1 Peak Trip A	Phase Overcurrent	1st Stage Overcurrent Trip A - Peak (P348)
786	I>1 Peak Trip B	Phase Overcurrent	1st Stage Overcurrent Trip B - Peak (P348)
787	I>1 Peak Trip C	Phase Overcurrent	1st Stage Overcurrent Trip C - Peak (P348)
788	I>2 Peak Trip	Phase Overcurrent	2nd Stage Overcurrent Trip 3ph - Peak (P348)
789	I>2 Peak Trip A	Phase Overcurrent	2nd Stage Overcurrent Trip A - Peak (P348)
790	I>2 Peak Trip B	Phase Overcurrent	2nd Stage Overcurrent Trip B - Peak (P348)
791	I>2 Peak Trip C	Phase Overcurrent	2nd Stage Overcurrent Trip C - Peak (P348)
792	I>3 Peak Trip	Phase Overcurrent	3rd Stage Overcurrent Trip 3ph - Peak (P348)
793	I>3 Peak Trip A	Phase Overcurrent	3rd Stage Overcurrent Trip A - Peak (P348)
794	I>3 Peak Trip B	Phase Overcurrent	3rd Stage Overcurrent Trip B - Peak (P348)
795	I>3 Peak Trip C	Phase Overcurrent	3rd Stage Overcurrent Trip C - Peak (P348)
796	I>4 Peak Trip	Phase Overcurrent	4th Stage Overcurrent Trip 3ph - Peak (P348)
797	I>4 Peak Trip A	Phase Overcurrent	4th Stage Overcurrent Trip A - Peak (P348)
798	I>4 Peak Trip B	Phase Overcurrent	4th Stage Overcurrent Trip B - Peak (P348)
799	I>4 Peak Trip C	Phase Overcurrent	4th Stage Overcurrent Trip C - Peak (P348)
800	I>5 RMS Trip	Phase Overcurrent	5th Stage Overcurrent Trip 3ph - RMS (P348)
801	I>5 RMS Trip A	Phase Overcurrent	5th Stage Overcurrent Trip A - RMS (P348)
802	I>5 RMS Trip B	Phase Overcurrent	5th Stage Overcurrent Trip B - RMS (P348)
803	I>5 RMS Trip C	Phase Overcurrent	5th Stage Overcurrent Trip C - RMS (P348)
804	I>6 RMS Trip	Phase Overcurrent	6th Stage Overcurrent Trip 3ph - RMS (P348)
805	I>6 RMS Trip A	Phase Overcurrent	6th Stage Overcurrent Trip A - RMS (P348)
806	I>6 RMS Trip B	Phase Overcurrent	6th Stage Overcurrent Trip B - RMS (P348)
807	I>6 RMS Trip C	Phase Overcurrent	6th Stage Overcurrent Trip C - RMS (P348)
808	I>7 RMS Trip	Phase Overcurrent	7th Stage Overcurrent Trip 3ph - RMS (P348)
809	I>7 RMS Trip A	Phase Overcurrent	7th Stage Overcurrent Trip A - RMS (P348)
810	I>7 RMS Trip B	Phase Overcurrent	7th Stage Overcurrent Trip B - RMS (P348)
811	I>7 RMS Trip C	Phase Overcurrent	7th Stage Overcurrent Trip C - RMS (P348)
812	I>8 RMS Trip	Phase Overcurrent	8th Stage Overcurrent Trip 3ph - RMS (P348)
813	I>8 RMS Trip A	Phase Overcurrent	8th Stage Overcurrent Trip A - RMS (P348)
814	I>8 RMS Trip B	Phase Overcurrent	8th Stage Overcurrent Trip B - RMS (P348)
815	I>8 RMS Trip C	Phase Overcurrent	8th Stage Overcurrent Trip C - RMS (P348)
816 to 823	Not Used		
824	I2>1 Trip	NPS Overcurrent	1st Stage Negative Phase Sequence Overcurrent Trip (P342-6/8)
825	I2>2 Trip	NPS Overcurrent	1st Stage Negative Phase Sequence Overcurrent Trip (P342-6/8)
826	I2>3 Trip	NPS Overcurrent	1st Stage Negative Phase Sequence Overcurrent Trip (P342-6/8)
827	I2>4 Trip	NPS Overcurrent	1st Stage Negative Phase Sequence Overcurrent Trip (P342-6/8)
828	Bfail1 Trip 3ph	Breaker Failure	1st Stage Breaker Fail Trip (P342-6)
829	Bfail2 Trip 3ph	Breaker Failure	2nd Stage Breaker Fail Trip (P342-6)
830 to 831	Not Used		

DDB no.	English text	Source	Description
832	VN>1 Trip	Residual O/V NVD	1st Stage Residual Overvoltage Trip (Derived O/V) (P342-6/8)
833	VN>2 Trip	Residual O/V NVD	2nd Stage Residual Overvoltage Trip (Derived O/V) (P342-6/8)
834	VN>3 Trip	Residual O/V NVD	1st Stage Residual Overvoltage Trip (VN1 Measured O/V) (P342-6)
835	VN>4 Trip	Residual O/V NVD	2nd Stage Residual Overvoltage Trip (VN1 Measured O/V) (P342-6)
836	VN>5 Trip	Residual O/V NVD	1st Stage Residual Overvoltage Trip (VN2 Measured O/V) (P344/5)
837	VN>6 Trip	Residual O/V NVD	2nd Stage Residual Overvoltage Trip (VN2 Measured O/V) (P344/5)
838	V>1 Peak Trip	Phase Overvoltage	1st Stage Phase Overvoltage Trip 3ph - Peak (P348)
839	V>1PeakTrip A/AB	Phase Overvoltage	1st Stage Phase Overvoltage Trip A/AB - Peak (P348)
840	V>1PeakTrip B/BC	Phase Overvoltage	1st Stage Phase Overvoltage Trip B/BC - Peak (P348)
841	V>1PeakTrip C/CA	Phase Overvoltage	1st Stage Phase Overvoltage Trip C/CA - Peak (P348)
842	V>2 Peak Trip	Phase Overvoltage	2nd Stage Phase Overvoltage Trip 3ph - Peak (P348)
843	V>2PeakTrip A/AB	Phase Overvoltage	2nd Stage Phase Overvoltage Trip A/AB - Peak (P348)
844	V>2PeakTrip B/BC	Phase Overvoltage	2nd Stage Phase Overvoltage Trip B/BC - Peak (P348)
845	V>2PeakTrip C/CA	Phase Overvoltage	2nd Stage Phase Overvoltage Trip C/CA - Peak (P348)
838	V>1 Trip	Phase Overvoltage	1st Stage Phase Overvoltage Trip 3ph (P342-6)
839	V>1 Trip A/AB	Phase Overvoltage	1st Stage Phase Overvoltage Trip A/AB (P342-6)
840	V>1 Trip B/BC	Phase Overvoltage	1st Stage Phase Overvoltage Trip B/BC (P342-6)
841	V>1 Trip C/CA	Phase Overvoltage	1st Stage Phase Overvoltage Trip C/CA (P342-6)
842	V>2 Trip	Phase Overvoltage	2nd Stage Phase Overvoltage Trip 3ph (P342-6)
843	V>2 Trip A/AB	Phase Overvoltage	2nd Stage Phase Overvoltage Trip A/AB (P342-6)
844	V>2 Trip B/BC	Phase Overvoltage	2nd Stage Phase Overvoltage Trip B/BC (P342-6)
845	V>2 Trip C/CA	Phase Overvoltage	2nd Stage Phase Overvoltage Trip C/CA (P342-6)
846	V2>1 Trip	NPS Overvoltage	Negative Phase Sequence Overvoltage Trip (P342-6)
847	V<1 Trip	Phase Undervoltage	1st Stage Phase Undervoltage Trip 3ph (P342-6)
848	V<1 Trip A/AB	Phase Undervoltage	1st Stage Phase Undervoltage Trip A/AB (P342-6)
849	V<1 Trip B/BC	Phase Undervoltage	1st Stage Phase Undervoltage Trip B/BC (P342-6)
850	V<1 Trip C/CA	Phase Undervoltage	1st Stage Phase Undervoltage Trip C/CA (P342-6)
851	V<2 Trip	Phase Undervoltage	2nd Stage Phase Undervoltage Trip 3ph (P342-6)

DDB no.	English text	Source	Description
852	V<2 Trip A/AB	Phase Undervoltage	2nd Stage Phase Undervoltage Trip A/AB (P342-6)
853	V<2 Trip B/BC	Phase Undervoltage	2nd Stage Phase Undervoltage Trip B/BC (P342-6)
854	V<2 Trip C/CA	Phase Undervoltage	2nd Stage Phase Undervoltage Trip C/CA (P342-6)
855	V>3 RMS Trip	Phase Overvoltage	3rd Stage Phase Overvoltage Trip 3ph - RMS (P348)
856	V>3RMS Trip A/AB	Phase Overvoltage	3rd Stage Phase Overvoltage Trip A/AB - RMS (P348)
857	V>3RMS Trip B/BC	Phase Overvoltage	3rd Stage Phase Overvoltage Trip B/BC - RMS (P348)
858	V>3RMS Trip C/CA	Phase Overvoltage	3rd Stage Phase Overvoltage Trip C/CA - RMS (P348)
859	V>4 RMS Trip	Phase Overvoltage	4th Stage Phase Overvoltage Trip 3ph - RMS (P348)
860	V>4RMS Trip A/AB	Phase Overvoltage	4th Stage Phase Overvoltage Trip A/AB - RMS (P348)
861	V>4RMS Trip B/BC	Phase Overvoltage	4th Stage Phase Overvoltage Trip B/BC - RMS (P348)
862	V>4RMS Trip C/CA	Phase Overvoltage	4th Stage Phase Overvoltage Trip C/CA - RMS (P348)
863	Not Used		
864	Field Fail1 Trip	Field Failure	Field Failure Stage 1 Trip (P342-6)
865	Field Fail2 Trip	Field Failure	Field Failure Stage 2 Trip (P342-6)
866	PSlipz Z1 Trip	Pole Slipping	Pole Slipping Zone 1 Trip (P343/4/5)
867	PSlipz Z2 Trip	Pole Slipping	Pole Slipping Zone 2 Trip (P343/4/5)
868	V Dep OC Trip	System Backup	Voltage Dependent Overcurrent Trip (P342-6)
869	V Dep OC Trip A	System Backup	Voltage Dependent Overcurrent Trip A (P342-6)
870	V Dep OC Trip B	System Backup	Voltage Dependent Overcurrent Trip B (P342-6)
871	V Dep OC Trip C	System Backup	Voltage Dependent Overcurrent Trip C (P342-6)
872	Z<1 Trip	System Backup	1st Stage Underimpedance Trip (P342-6)
873	Z<1 Trip A	System Backup	1st Stage Underimpedance Trip A (P342-6)
874	Z<1 Trip B	System Backup	1st Stage Underimpedance Trip B (P342-6)
875	Z<1 Trip C	System Backup	1st Stage Underimpedance Trip C (P342-6)
876	Z<2 Trip	System Backup	2nd Stage Underimpedance Trip (P342-6)
877	Z<2 Trip A	System Backup	2nd Stage Underimpedance Trip A (P342-6)
878	Z<2 Trip B	System Backup	2nd Stage Underimpedance Trip B (P342-6)
879	Z<2 Trip C	System Backup	2nd Stage Underimpedance Trip C (P342-6)
880	DeadMachine Trip	Dead Machine	Dead Machine Protection Trip (P343/4/5)
881	S2>1 Trip	NPS Overpower	Negative Phase Sequence VA Trip (S2 = V2 x I2) (P342-6)
882	Power1 Trip	Power	1st Stage Power Trip (P342-6)
883	Power2 Trip	Power	2nd Stage Power Trip (P342-6)
884	SPower1 Trip	Sensitive Power	1st Stage Sensitive Power Trip (P342-6)
885	SPower2 Trip	Sensitive Power	2nd Stage Sensitive Power Trip (P342-6)
886	Power3 Trip	Power	3rd Stage Power Trip (P342-6)
887	Power4 Trip	Power	4th Stage Power Trip (P342-6)

DDB no.	English text	Source	Description
888	SPower3 Trip	Sensitive Power	3rd Stage Sensitive Power Trip (P342-6)
889	SPower4 Trip	Sensitive Power	4th Stage Sensitive Power Trip (P342-6)
886 to 907	Not Used		
908	V<3 Trip	Phase Undervoltage	3rd Stage Phase Undervoltage Trip 3ph (P342-6)
909	V<3 Trip A/AB	Phase Undervoltage	3rd Stage Phase Undervoltage Trip A/AB (P342-6)
910	V<3 Trip B/BC	Phase Undervoltage	3rd Stage Phase Undervoltage Trip B/BC (P342-6)
911	V<3 Trip C/CA	Phase Undervoltage	3rd Stage Phase Undervoltage Trip C/CA (P342-6)
912	V/Hz>1 Trip	Overfluxing	1st Stage Overflux (voltage/frequency) Trip (P342-6)
913	V/Hz>2 Trip	Overfluxing	2nd Stage Overflux (voltage/frequency) Trip (P342-6)
914	V/Hz>3 Trip	Overfluxing	3rd Stage Overflux (voltage/frequency) Trip (P342-6)
915	V/Hz>4 Trip	Overfluxing	4th Stage Overflux (voltage/frequency) Trip (P342-6)
916	F<1 Trip	Underfrequency	1st Stage Underfrequency Trip (P342-6)
917	F<2 Trip	Underfrequency	2nd Stage Underfrequency Trip (P342-6)
918	F<3 Trip	Underfrequency	3rd Underfrequency Trip (P342-6)
919	F<4 Trip	Underfrequency	4th Stage Underfrequency Trip (P342-6)
920	F>1 Trip	Overfrequency	1st Stage Overfrequency Trip (P342-6/8)
921	F>2 Trip	Overfrequency	2nd Stage Overfrequency Trip (P342-6/8)
922	Freq Band1 Trip	Turbine F Prot	1st Frequency Band Trip - Turbine Frequency Protection (P342-6)
923	Freq Band2 Trip	Turbine F Prot	2nd Frequency Band Trip - Turbine Frequency Protection (P342-6)
924	Freq Band3 Trip	Turbine F Prot	3rd Frequency Band Trip - Turbine Frequency Protection (P342-6)
925	Freq Band4 Trip	Turbine F Prot	4th Frequency Band Trip - Turbine Frequency Protection (P342-6)
926	Freq Band5 Trip	Turbine F Prot	5th Frequency Band Trip - Turbine Frequency Protection (P342-6)
927	Freq Band6 Trip	Turbine F Prot	6th Frequency Band Trip - Turbine Frequency Protection (P342-6)
928	df/dt>1 Trip	df/dt	1st Stage Rate of Change of Frequency Trip (P342-6)
929	df/dt>2 Trip	df/dt	2nd Stage Rate of Change of Frequency Trip (P342-6)
930	df/dt>3 Trip	df/dt	3rd Stage Rate of Change of Frequency Trip (P342-6)
931	df/dt>4 Trip	df/dt	4th Stage Rate of Change of Frequency Trip (P342-6)
932 to 935	Not used		
936	df/dt>1 Under F	df/dt	Rate of Change of Frequency Stage 1 Underfrequency (P342-6)
937	df/dt>1 Over F	df/dt	Rate of Change of Frequency Stage 1 Overfrequency (P342-6)
938 to 943	Not Used		
944	NPS Thermal Trip	NPS Thermal	Negative Phase Sequence Thermal Trip (P342-6)

DDB no.	English text	Source	Description
945	Gen Thermal Trip	Thermal Overload	Thermal Overload Trip (P342-6)
946	Hot Spot>1 Trip	Xformer Thermal Overload	1st Stage Hot Spot Temperature Trip (P342-6)
947	Hot Spot>2 Trip	Xformer Thermal Overload	2nd Stage Hot Spot Temperature Trip (P342-6)
948	Hot Spot>3 Trip	Xformer Thermal Overload	3rd Stage Hot Spot Temperature Trip (P342-6)
949	Top Oil>1 Trip	Xformer Thermal Overload	1st Stage Top Oil Temperature Trip (P342-6)
950	Top Oil>2 Trip	Xformer Thermal Overload	2nd Stage Top Oil Temperature Trip (P342-6)
951	Top Oil>3 Trip	Xformer Thermal Overload	3rd Stage Top Oil Temperature Trip (P342-6)
952 to 975	Not used		
976	RTD 1 Trip	RTD Protection	RTD 1 Trip (P342-6)
985	RTD 10 Trip	RTD Protection	RTD 10 Trip (P342-6)
986	Any RTD Trip	RTD Protection	Any RTD Trip 1-10 (P342-6)
987	CL Input 1 Trip	Current Loop Inputs	Current Loop Input (transducer input) 1 Trip (P342-6/8)
988	CL Input 2 Trip	Current Loop Inputs	Current Loop Input (transducer input) 2 Trip (P342-6/8)
989	CL Input 3 Trip	Current Loop Inputs	Current Loop Input (transducer input) 3 Trip (P342-6/8)
990	CL Input 4 Trip	Current Loop Inputs	Current Loop Input (transducer input) 4 Trip (P342-6/8)
991	Not used		
992	Any Start	All protection	Any Start (P342-6/8)
993	Xform Bias StrtA	Xformer Differential	Transformer Differential Start A (P343-6)
994	Xform Bias StrtB	Xformer Differential	Transformer Differential Start B (P343-6)
995	Xform Bias StrtC	Xformer Differential	Transformer Differential Start C (P343-6)
996 to 1007	Not used		
1008	IN>1 Start	Earth Fault	1st Stage Earth Fault Start (P342-6)
1009	IN>2 Start	Earth Fault	2nd Stage Earth Fault Start (P342-6)
1010 to 1011	Not used		
1012	ISEF>1 Start	Sensitive Earth Fault	1st Stage Sensitive Earth Fault Start (P342-6)
1013 to 1015	Not Used		
1016	100%StEF3H Start	100% Stator Earth Fault	100% Stator Earth Fault Start (3rd harmonic) (P343/4/5)
1017	64S I<1 Start	64S 100% Stator Earth Fault	100% Stator Earth Fault Undercurrent Start (Low frequency injection) - used by supervision element (P345)
1018	64S V< Start	64S 100% Stator Earth Fault	100% Stator Earth Fault Undervoltage Start (Low frequency injection) - used by supervision element (P345)
1019	64S I>1 Start	64S 100% Stator Earth Fault	1st Stage 100% Stator Earth Fault Overcurrent Start (Low frequency injection) (P345)
1020	64S Start R<1 Alm	64S 100% Stator Earth Fault	1st Stage 100% Stator Earth Fault Under Resistance Alarm Start (Low frequency injection) (P345)
1021	64S R<2 Start	64S 100% Stator Earth Fault	2nd Stage 100% Stator Earth Fault Under Resistance Trip Start (Low frequency injection) (P345)
1022	64R Start R<1Alm	64R Rotor Earth Fault	1st Stage Rotor Earth Fault Under Resistance Alarm Start
1023	64R R<2 Start	64R Rotor Earth Fault	2nd Stage Rotor Earth Fault Under Resistance Trip Start

DDB no.	English text	Source	Description
1024	I>1 Peak Start	Phase Overcurrent	1st Stage Overcurrent Start 3ph - Peak (P348)
1025	I>1 Peak Start A	Phase Overcurrent	1st Stage Overcurrent Start A - Peak (P348)
1026	I>1 Peak Start B	Phase Overcurrent	1st Stage Overcurrent Start B - Peak (P348)
1027	I>1 Peak Start C	Phase Overcurrent	1st Stage Overcurrent Start C - Peak (P348)
1028	I>2 Peak Start	Phase Overcurrent	2nd Stage Overcurrent Start 3ph - Peak (P348)
1029	I>2 Peak Start A	Phase Overcurrent	2nd Stage Overcurrent Start A - Peak (P348)
1030	I>2 Peak Start B	Phase Overcurrent	2nd Stage Overcurrent Start B - Peak (P348)
1031	I>2 Peak Start C	Phase Overcurrent	2nd Stage Overcurrent Start C - Peak (P348)
1032	I>3 Peak Start	Phase Overcurrent	3rd Stage Overcurrent Start 3ph - Peak (P348)
1033	I>3 Peak Start A	Phase Overcurrent	3rd Stage Overcurrent Start A - Peak (P348)
1034	I>3 Peak Start B	Phase Overcurrent	3rd Stage Overcurrent Start B - Peak (P348)
1035	I>3 Peak Start C	Phase Overcurrent	3rd Stage Overcurrent Start C - Peak (P348)
1036	I>4 Peak Start	Phase Overcurrent	4th Stage Overcurrent Start 3ph - Peak (P348)
1037	I>4 Peak Start A	Phase Overcurrent	4th Stage Overcurrent Start A - Peak (P348)
1038	I>4 Peak Start B	Phase Overcurrent	4th Stage Overcurrent Start B - Peak (P348)
1039	I>4 Peak Start C	Phase Overcurrent	4th Stage Overcurrent Start C - Peak (P348)
1040	I>5 RMS Start	Phase Overcurrent	5th Stage Overcurrent Start 3ph - RMS (P348)
1041	I>5 RMS Start A	Phase Overcurrent	5th Stage Overcurrent Start A - RMS (P348)
1042	I>5 RMS Start B	Phase Overcurrent	5th Stage Overcurrent Start B - RMS (P348)
1043	I>5 RMS Start C	Phase Overcurrent	5th Stage Overcurrent Start C - RMS (P348)
1044	I>6 RMS Start	Phase Overcurrent	6th Stage Overcurrent Start 3ph - RMS (P348)
1045	I>6 RMS Start A	Phase Overcurrent	6th Stage Overcurrent Start A - RMS (P348)
1046	I>6 RMS Start B	Phase Overcurrent	6th Stage Overcurrent Start B - RMS (P348)
1047	I>6 RMS Start C	Phase Overcurrent	6th Stage Overcurrent Start C - RMS (P348)
1048	I>7 RMS Start	Phase Overcurrent	7th Stage Overcurrent Start 3ph - RMS (P348)
1049	I>7 RMS Start A	Phase Overcurrent	7th Stage Overcurrent Start A - RMS (P348)
1050	I>7 RMS Start B	Phase Overcurrent	7th Stage Overcurrent Start B - RMS (P348)
1051	I>7 RMS Start C	Phase Overcurrent	7th Stage Overcurrent Start C - RMS (P348)
1052	I>8 RMS Start	Phase Overcurrent	8th Stage Overcurrent Start 3ph - RMS (P348)
1053	I>8 RMS Start A	Phase Overcurrent	8th Stage Overcurrent Start A - RMS (P348)
1054	I>8 RMS Start B	Phase Overcurrent	8th Stage Overcurrent Start B - RMS (P348)
1055	I>8 RMS Start C	Phase Overcurrent	8th Stage Overcurrent Start C - RMS (P348)
1040	I>1 Start	Phase Overcurrent	1st Stage Overcurrent Start 3ph (P342-6)
1041	I>1 Start A	Phase Overcurrent	1st Stage Overcurrent Start A (P342-6)
1042	I>1 Start B	Phase Overcurrent	1st Stage Overcurrent Start B (P342-6)
1043	I>1 Start C	Phase Overcurrent	1st Stage Overcurrent Start C (P342-6)
1044	I>2 Start	Phase Overcurrent	2nd Stage Overcurrent Start 3ph (P342-6)
1045	I>2 Start A	Phase Overcurrent	2nd Stage Overcurrent Start A (P342-6)
1046	I>2 Start B	Phase Overcurrent	2nd Stage Overcurrent Start B (P342-6)
1047	I>2 Start C	Phase Overcurrent	2nd Stage Overcurrent Start C (P342-6)
1048	I>3 Start	Phase Overcurrent	3rd Stage Overcurrent Start 3ph (P342-6)
1049	I>3 Start A	Phase Overcurrent	3rd Stage Overcurrent Start A (P342-6)
1050	I>3 Start B	Phase Overcurrent	3rd Stage Overcurrent Start B (P342-6)
1051	I>3 Start C	Phase Overcurrent	3rd Stage Overcurrent Start C (P342-6)
1052	I>4 Start	Phase Overcurrent	4th Stage Overcurrent Start 3ph (P342-6)
1053	I>4 Start A	Phase Overcurrent	4th Stage Overcurrent Start A (P342-6)
1054	I>4 Start B	Phase Overcurrent	4th Stage Overcurrent Start B (P342-6)

DDB no.	English text	Source	Description
1055	I>4 Start C	Phase Overcurrent	4th Stage Overcurrent Start C (P342-6)
1056 to 1063	Not Used		
1064	I2>1 Start	NPS Overcurrent	1st Stage Negative Phase Sequence Overcurrent Start (P342-6/8)
1065	I2>2 Start	NPS Overcurrent	1st Stage Negative Phase Sequence Overcurrent Start (P342-6/8)
1066	I2>3 Start	NPS Overcurrent	1st Stage Negative Phase Sequence Overcurrent Start (P342-6/8)
1067	I2>4 Start	NPS Overcurrent	1st Stage Negative Phase Sequence Overcurrent Start (P342-6/8)
1068	IA< Start	Undercurrent	A phase Undercurrent Start (used in CB Fail logic) (P342-6)
1069	IB< Start	Undercurrent	B phase Undercurrent Start (used in CB Fail logic) (P342-6)
1070	IC< Start	Undercurrent	C phase Undercurrent Start (used in CB Fail logic) (P342-6)
1071	ISEF< Start	Undercurrent	Sensitive Earth Fault Undercurrent Start (used in CB Fail logic) (P342-6)
1072	IN< Start	Undercurrent	Earth Fault Undercurrent Start (used in CB Fail logic) (P342-6)
1073, 1074	Not Used		
1075	TF OC Start	TF Monitoring	Through fault overcurrent start (P342-6)
1076	Not Used		
1077	TF Recorder trig	TF Monitoring	Through Fault Recorder Trigger. A through fault event is recorded if any of the phase currents is bigger than the TF I> Trigger setting (P342-6)
1078 to 1087	Not Used		
1088	VN>1 Start	Residual O/V NVD	1st Stage Residual Overvoltage Start (Derived O/V) (P342-6/8)
1089	VN>2 Start	Residual O/V NVD	2nd Stage Residual Overvoltage Start (Derived O/V) (P342-6/8)
1090	VN>3 Start	Residual O/V NVD	1st Stage Residual Overvoltage Start (VN1 Measured O/V) (P342-6)
1091	VN>4 Start	Residual O/V NVD	2nd Stage Residual Overvoltage Start (VN1 Measured O/V) (P342-6)
1092	VN>5 Start	Residual O/V NVD	1st Stage Residual Overvoltage Start (VN2 Measured O/V) (P344/5)
1093	VN>6 Start	Residual O/V NVD	2nd Stage Residual Overvoltage Start (VN2 Measured O/V) (P344/5)
1094	V>1 Peak Start	Phase Overvoltage	1st Stage Phase Overvoltage Start 3ph - Peak (P348)
1095	V>1 PeakStrt A/AB	Phase Overvoltage	1st Stage Phase Overvoltage Start A/AB - Peak (P348)
1096	V>1PeakStrt B/BC	Phase Overvoltage	1st Stage Phase Overvoltage Start B/BC - Peak (P348)
1097	V>1PeakStrt C/CA	Phase Overvoltage	1st Stage Phase Overvoltage Start C/CA - Peak (P348)
1098	V>2 Peak Start	Phase Overvoltage	2nd Stage Phase Overvoltage Start 3ph - Peak (P348)
1099	V>2PeakStrt A/AB	Phase Overvoltage	2nd Stage Phase Overvoltage Start A/AB - Peak (P348)

DDB no.	English text	Source	Description
1100	V>2PeakStrt B/BC	Phase Overvoltage	2nd Stage Phase Overvoltage Start B/BC - Peak (P348)
1101	V>2PeakStrt C/CA	Phase Overvoltage	2nd Stage Phase Overvoltage Start C/CA - Peak (P348)
1094	V>1 Start	Phase Overvoltage	1st Stage Phase Overvoltage Start 3ph (P342-6)
1095	V>1 Start A/AB	Phase Overvoltage	1st Stage Phase Overvoltage Start A/AB (P342-6)
1096	V>1 Start B/BC	Phase Overvoltage	1st Stage Phase Overvoltage Start B/BC (P342-6)
1097	V>1 Start C/CA	Phase Overvoltage	1st Stage Phase Overvoltage Start C/CA (P342-6)
1098	V>2 Start	Phase Overvoltage	2nd Stage Phase Overvoltage Start 3ph (P342-6)
1099	V>2 Start A/AB	Phase Overvoltage	2nd Stage Phase Overvoltage Start A/AB (P342-6)
1100	V>2 Start B/BC	Phase Overvoltage	2nd Stage Phase Overvoltage Start B/BC (P342-6)
1101	V>2 Start C/CA	Phase Overvoltage	2nd Stage Phase Overvoltage Start C/CA (P342-6)
1102	V2>1 Start	NPS Overvoltage	Negative Phase Sequence Overvoltage Start (P342-6)
1103	V<1 Start	Phase Undervoltage	1st Stage Phase Undervoltage Start 3ph (P342-6)
1104	V<1 Start A/AB	Phase Undervoltage	1st Stage Phase Undervoltage Start A/AB (P342-6)
1105	V<1 Start B/BC	Phase Undervoltage	1st Stage Phase Undervoltage Start B/BC (P342-6)
1106	V<1 Start C/CA	Phase Undervoltage	1st Stage Phase Undervoltage Start C/CA (P342-6)
1107	V<2 Start	Phase Undervoltage	2nd Stage Phase Undervoltage Start 3ph (P342-6)
1108	V<2 Start A/AB	Phase Undervoltage	2nd Stage Phase Undervoltage Start A/AB (P342-6)
1109	V<2 Start B/BC	Phase Undervoltage	2nd Stage Phase Undervoltage Start B/BC (P342-6)
1110	V<2 Start C/CA	Phase Undervoltage	2nd Stage Phase Undervoltage Start C/CA (P342-6)
1111	V>3 RMS Start	Phase Overvoltage	3rd Stage Phase Overvoltage Start 3ph -RMS (P348)
1112	V>3RMS Strt A/AB	Phase Overvoltage	3rd Stage Phase Overvoltage Start A/AB - RMS (P348)
1113	V>3RMS Strt B/BC	Phase Overvoltage	3rd Stage RMS Phase Overvoltage Start B/BC - RMS (P348)
1114	V>3RMS Strt C/CA	Phase Overvoltage	3rd Stage Phase Overvoltage Start C/CA - RMS (P348)
1115	V>4 RMS Start	Phase Overvoltage	4th Stage Phase Overvoltage Start 3ph - RMS (P348)
1116	V>4RMS Strt A/AB	Phase Overvoltage	4th Stage Phase Overvoltage Start A/AB - RMS (P348)
1117	V>4RMS Strt B/BC	Phase Overvoltage	4th Stage Phase Overvoltage Start B/BC - RMS (P348)
1118	V>4RMS Strt C/CA	Phase Overvoltage	4th Stage Phase Overvoltage Start C/CA - RMS (P348)
1119	FFail Line Start	Field Failure	Field Failure Directional Line Start (P342-6)

DDB no.	English text	Source	Description
1120	FFail1 Start	Field Failure	1st Stage Field Failure Start (P342-6)
1121	FFail2 Start	Field Failure	2nd Stage Field Failure Start (P342-6)
1122	PSlipz Z1 Start	Pole Slipping	Pole slipping detected in Zone1 (P343/4/5)
1123	PSlipz Z2 Start	Pole Slipping	Pole slipping detected in Zone2 (P343/4/5)
1124	PSlipz LensStart	Pole Slipping	Measured impedance is within the Lens (P343/4/5)
1125	PSlipz BlindStrt	Pole Slipping	Impedance lies left hand side of Blinder (P343/4/5)
1126	PSlipz ReactStrt	Pole Slipping	Impedance lies in Zone 1 distinguished by Reactance line (P343/4/5)
1127	V Dep OC Start	System Backup	Voltage Dependent Overcurrent Start (P342-6)
1128	V Dep OC Start A	System Backup	Voltage Dependent Overcurrent Start A (P342-6)
1129	V Dep OC Start B	System Backup	Voltage Dependent Overcurrent Start B (P342-6)
1130	V Dep OC Start C	System Backup	Voltage Dependent Overcurrent Start C (P342-6)
1131	Z<1 Start	System Backup	1st Stage Underimpedance Start (P342-6)
1132	Z<1 Start A	System Backup	1st Stage Underimpedance Start A (P342-6)
1133	Z<1 Start B	System Backup	1st Stage Underimpedance Start B (P342-6)
1134	Z<1 Start C	System Backup	1st Stage Underimpedance Start C (P342-6)
1135	Z<2 Start	System Backup	2nd Stage Underimpedance Start (P342-6)
1136	Z<2 Start A	System Backup	2nd Stage Underimpedance Start A (P342-6)
1137	Z<2 Start B	System Backup	2nd Stage Underimpedance Start B (P342-6)
1138	Z<2 Start C	System Backup	2nd Stage Underimpedance Start C (P342-6)
1139	S2>1 Start	Power	Negative Phase Sequence VA Start (S2 = V2 x I2) (P342-6)
1140	Power1 Start	Power	1st Stage Power Start (P342-6)
1141	Power2 Start	Power	2nd Stage Power Start (P342-6)
1142	SPower1 Start	Sensitive Power	1st Stage Sensitive Power Start (P342-6)
1143	SPower2 Start	Sensitive Power	2nd Stage Sensitive Power Start(P342-6)
1144	Power3 Start	Power	3rd Stage Power Start (P342-6)
1145	Power4 Start	Power	4th Stage Power Start (P342-6)
1146	SPower3 Start	Sensitive Power	3rd Stage Sensitive Power Start (P342-6)
1147	SPower4 Start	Sensitive Power	4th Stage Sensitive Power Start (P342-6)
1148 to 1163	Not Used		
1164	V<3 Start	Phase Undervoltage	3rd Stage Phase Undervoltage Start 3ph (P342-6)
1165	V<3 Start A/AB	Phase Undervoltage	3rd Stage Phase Undervoltage Start A/AB (P342-6)
1166	V<3 Start B/BC	Phase Undervoltage	3rd Stage Phase Undervoltage Start B/BC (P342-6)
1167	V<3 Start C/CA	Phase Undervoltage	3rd Stage Phase Undervoltage Start C/CA (P342-6)
1168	V/Hz>1 Start	Overfluxing	1st Stage Overflux (voltage/frequency) Start (P342-6)
1169	V/Hz>2 Start	Overfluxing	2nd Stage Overflux (voltage/frequency) Start (P342-6)
1170	V/Hz>3 Start	Overfluxing	3rd Stage Overflux (voltage/frequency) Start (P342-6)

DDB no.	English text	Source	Description
1171	V/Hz>4 Start	Overfluxing	4th Stage Overflux (voltage/frequency) Start (P342-6)
1172	F<1 Start	Underfrequency	1st Stage Underfrequency Start (P342-6)
1173	F<2 Start	Underfrequency	2nd Stage Underfrequency Start (P342-6)
1174	F<3 Start	Underfrequency	3rd Stage Underfrequency Start (P342-6)
1175	F<4 Start	Underfrequency	4th Stage Underfrequency Start (P342-6)
1176	F>1 Start	Overfrequency	1st Stage Overfrequency Start (P342-6)
1177	F>2 Start	Overfrequency	2nd Stage Overfrequency Start (P342-6)
1178	Freq Band1 Start	Turbine F Prot	1st Frequency Band Start - Turbine Frequency Protection (P342-6)
1179	Freq Band2 Start	Turbine F Prot	2nd Frequency Band Start - Turbine Frequency Protection (P342-6)
1180	Freq Band3 Start	Turbine F Prot	3rd Frequency Band Start - Turbine Frequency Protection (P342-6)
1181	Freq Band4 Start	Turbine F Prot	4th Frequency Band Start - Turbine Frequency Protection (P342-6)
1182	Freq Band5 Start	Turbine F Prot	5th Frequency Band Start - Turbine Frequency Protection (P342-6)
1183	Freq Band6 Start	Turbine F Prot	6th Frequency Band Start - Turbine Frequency Protection (P342-6)
1184	df/dt>1 Start	df/dt	1st Stage Rate of Change of Frequency Start (P342-6)
1185	df/dt>2 Start	df/dt	2nd Stage Rate of Change of Frequency Start (P342-6)
1186	df/dt>3 Start	df/dt	3rd Stage Rate of Change of Frequency Start (P342-6)
1187	df/dt>4 Start	df/dt	4th Stage Rate of Change of Frequency Start (P342-6)
1188 to 1197	Not Used		
1198	F>3 Start	Overfrequency	3rd Stage Overfrequency Start (P348)
1199	F>4 Start	Overfrequency	4th Stage Overfrequency Start (P348)
1200	Hot Spot>1 Start	Thermal overload	1st Stage Hot Spot Temperature Start (P342-6)
1201	Hot Spot>2 Start	Thermal overload	2nd Stage Hot Spot Temperature Start (P342-6)
1202	Hot Spot>3 Start	Thermal overload	3rd Stage Hot Spot Temperature Start (P342-6)
1203	Top Oil>1 start	Thermal overload	1st Stage Top Oil Temperature Start (P342-6)
1204	Top Oil>2 start	Thermal overload	2nd Stage Top Oil Temperature Start (P342-6)
1205	Top Oil>3 start	Thermal overload	3rd Stage Top Oil Temperature Start (P342-6)
1206 to 1231	Not Used		
1232	CLI1 Alarm Start	Current Loop Inputs	Current Loop Input (transducer input) 1 Alarm Start (P342-6/8)
1233	CLI2 Alarm Start	Current Loop Inputs	Current Loop Input (transducer input) 2 Alarm Start (P342-6/8)
1234	CLI3 Alarm Start	Current Loop Inputs	Current Loop Input (transducer input) 3 Alarm Start (P342-6/8)
1235	CLI4 Alarm Start	Current Loop Inputs	Current Loop Input (transducer input) 4 Alarm Start (P342-6/8)
1236	CLI1 Trip Start	Current Loop Inputs	Current Loop Input (transducer input) 1 Trip Start (P342-6/8)

DDB no.	English text	Source	Description
1237	CLI2 Trip Start	Current Loop Inputs	Current Loop Input (transducer input) 2 Trip Start (P342-6/8)
1238	CLI3 Trip Start	Current Loop Inputs	Current Loop Input (transducer input) 3 Trip Start (P342-6/8)
1239	CLI4 Trip Start	Current Loop Inputs	Current Loop Input (transducer input) 4 Trip Start (P342-6/8)
1240 to 1247	Not Used		
1248	VTS Fast Block	VT Supervision	VT Supervision Fast Block - blocks elements which would otherwise mal-operate immediately after a fuse failure event occurs (P342-6/8)
1249	VTS Slow Block	VT Supervision	VT Supervision Slow Block - blocks elements which would otherwise mal-operate some time after a fuse failure event occurs (P342-6/8)
1252	VT Fail A	VT Supervision	VT Supervision detects failure of A phase and blocks neutral voltage protection which would otherwise mal-operate after a fuse failure event occurs (P348)
1253	VT Fail B	VT Supervision	VT Supervision detects failure of B phase and blocks neutral voltage protection which would otherwise mal-operate after a fuse failure event occurs (P348)
1254	VT Fail C	VT Supervision	VT Supervision detects failure of C phase and blocks neutral voltage protection which would otherwise mal-operate after a fuse failure event occurs (P348)
1263	CTS-1 Block	CT Supervision	CT Supervision Block for IA/IB/IC (current transformer supervision). CTS-1 Block and CTS-2 Block DDBs can be used to block protection functions not automatically blocked such as Generator Differential (P342-6)
1264	CTS-2 Block	CT Supervision	CT Supervision Block for IA-2/IB-2/IC-2 (current transformer supervision). CTS-1 Block and CTS-2 Block DDBs can be used to block protection functions not automatically blocked such as Generator Differential (P343-8)
1265	Diff CTS BLK	CT Supervision	Differential CT Supervision Block (P343-6)
1266	Diff CTS CT1	CT Supervision	Differential CT Supervision for IA/IB/IC (P343-6)
1267	Diff CTS CT2	CT Supervision	Differential CT Supervision for IA-2/IB-2/IC-2 (P343/4/5/6)
1268	CTS2 No Vn	CT Supervision	Stator CT Supervision, no neutral voltage detected (P348)
1269	CctFail Blk A	Xformer Diff	Circuitry Fault Alarm A (P343-6)
1270	CctFail Blk B	Xformer Diff	Circuitry Fault Alarm B (P343-6)
1271	CctFail Blk C	Xformer Diff	Circuitry Fault Alarm C (P343-6)
1272	2nd Har Blk A	Xformer Diff	2nd Harmonic blocked A. 2nd harmonic current is above Xform Ih(2)%> for phase A. (P343-6)
1273	2nd Har Blk B	Xformer Diff	2nd Harmonic blocked B. 2nd harmonic current is above Xform Ih(2)%> for phase B. (P343-6)
1274	2nd Har Blk C	Xformer Diff	2nd Harmonic blocked C. 2nd harmonic current is above Xform Ih(2)%> for phase C. (P343-6)
1275	5th Har Blk A	Xformer Diff	5th Harmonic blocked A. 5th harmonic current is above Xform Ih(5)%> for phase A. (P343-6)

DDB no.	English text	Source	Description
1276	5th Har Blk B	Xformer Diff	5th Harmonic blocked B. 5th harmonic current is above Xform Ih(5)%> for phase B. (P343-6)
1277	5th Har Blk C	Xformer Diff	5th Harmonic blocked C. 5th harmonic current is above Xform Ih(5)%> for phase C. (P343-6)
1278	Control Trip	CB Control	Control trip - operator trip instruction to the circuit breaker, via menu, or SCADA. (Does not operate for protection element trips) (P342-6)
1279	Control Close	CB Control	Control close command to the circuit breaker. Operates for a manual close command (menu, SCADA) (P342-6)
1280	Close in Prog	CB Control	Control close in progress - the relay has been given an instruction to close the circuit breaker, but the manual close timer delay has not yet finished timing out (P342-6)
1281	Lockout Alarm	CB Monitoring	Composite Lockout Alarm from CB Monitoring functions (I ^ Lockout Alarm OR CB Ops Lockout OR CB Op Time Lock OR Fault Freq Lock) (P342-6/8)
1282	CB Open 3 ph	CB Status	Three phase Circuit breaker Open Status (P342-6)
1283	CB Closed 3 ph	CB Status	Three phase Circuit breaker Closed Status (P342-6)
1284	All Poles Dead	Poledead	Pole dead logic detects 3 phase breaker open condition (P342-6)
1285	Any Pole Dead	Poledead	Pole dead logic detects at least one breaker pole open (P342-6)
1286	Pole Dead A	Poledead	Phase A Pole Dead (P342-6)
1287	Pole Dead B	Poledead	Phase B Pole Dead (P342-6)
1288	Pole Dead C	Poledead	Phase C Pole Dead (P342-6)
1289 to 1292	Not Used		
1293	Freq High	Frequency Tracking	Frequency measurement detects frequency above the allowed range. Stator frequency (P342-6), rotor frequency (P348)
1294	Freq Low	Frequency Tracking	Frequency measurement detects frequency below the allowed range. Stator frequency (P342-6), rotor frequency (P348)
1295	Freq Not found	Frequency Tracking	Frequency Not Found by the frequency measurement. Stator frequency (P342-6), rotor frequency (P348)
1297	64S F Band Block	64S 100% Stator earth Fault	64S 100% Stator Earth Fault - System frequency in blocking band (P345)
1298	64S Fail	64S 100% Stator earth Fault	64S 100% Stator Earth Fault - Injection failure (P345)
1304	RTD 1 Alarm	RTD Thermal	RTD 1 Alarm (P342-6)
1305	RTD 2 Alarm	RTD Thermal	RTD 2 Alarm (P342-6)
1306	RTD 3 Alarm	RTD Thermal	RTD 3 Alarm (P342-6)
1307	RTD 4 Alarm	RTD Thermal	RTD 4 Alarm (P342-6)
1308	RTD 5 Alarm	RTD Thermal	RTD 5 Alarm (P342-6)
1309	RTD 6 Alarm	RTD Thermal	RTD 6 Alarm (P342-6)
1310	RTD 7 Alarm	RTD Thermal	RTD 7 Alarm (P342-6)
1311	RTD 8 Alarm	RTD Thermal	RTD 8 Alarm (P342-6)

DDB no.	English text	Source	Description
1312	RTD 9 Alarm	RTD Thermal	RTD 9 Alarm (P342-6)
1313	RTD 10 Alarm	RTD Thermal	RTD 10 Alarm (P342-6)
1314	Blk Rmt. CB Ops	PSL	Blocks remote CB Trip/Close commands when asserted (P342-6)
1315	Freq2 High	Frequency Tracking	Frequency measurement detects Frequency 2 (stator) above the allowed range (P348)
1316	Freq2 Low	Frequency Tracking	Frequency measurement detects frequency 2 (stator) below the allowed range (P348)
1317	Freq2 Not Found	Frequency Tracking	Frequency 2 (stator) Not Found by the frequency measurement (P348)
1319 to 1327	Not Used		
1328	Live Gen	Voltage Monitors	Indicates live generator voltage condition is detected (P342-6)
1329	Dead Gen	Voltage Monitors	Indicates dead generator voltage condition is detected (P342-6)
1330	Live Bus	Voltage Monitors	Indicates live busbar voltage condition is detected (P342-6)
1331	Dead Bus	Voltage Monitors	Indicates dead busbar voltage condition is detected (P342-6)
1332	Check Sync 1 OK	Check Synchronization	Check synchronization stage 1 OK (P342-6)
1333	Check Sync 2 OK	Check Synchronization	Check synchronization stage 1 OK (P342-6)
1334	Not Used		
1335	SysChks Inactive	Check Synchronization	System checks inactive (output from the check synchronism, and other voltage checks) (P342-6)
1336	CS1 Enabled	Check Synchronization	Check sync. stage 1 OK (P342-6)
1337	CS2 Enabled	Check Synchronization	Check sync. stage 2 OK (P342-6)
1338	SysSplit Enabled	Check Synchronization	System Split function enabled (P342-6)
1339	CS1 Slipfreq>	Check Synchronization	Operates when 1st stage check sync. slip frequency is above the check sync. 1 slip frequency setting (P342-6)
1340	CS1 Slipfreq<	Check Synchronization	Operates when 1st stage check sync. slip frequency is below the check sync. 1 slip frequency setting (P342-6)
1341	CS2 Slipfreq>	Check Synchronization	Operates when 2nd stage check sync. slip frequency is above the check sync. 2 slip frequency setting (P342-6)
1342	CS2 Slipfreq<	Check Synchronization	Operates when 2nd stage check sync. slip frequency is below the check sync. 2 slip frequency setting (P342-6)
1343	CS Vgen<	Check Synchronization	Indicates the generator voltage is less than the check sync. undervoltage setting
1344	CS Vbus<	Check Synchronization	Indicates the busbar voltage is less than the check sync. undervoltage setting (P342-6)
1345	CS Vgen>	Check Synchronization	Indicates the generator voltage is greater than the check sync. overvoltage setting (P342-6)
1346	CS Vbus>	Check Synchronization	Indicates the busbar voltage is greater than the check sync. overvoltage setting (P342-6)
1347	CS Freq Low	Check Synchronization	Indicates the generator frequency is less than the Gen Under Freq setting (P342-6)
1348	CS Freq High	Check Synchronization	Indicates the generator frequency is greater than the Gen Over Freq setting (P342-6)

DDB no.	English text	Source	Description
1349	CS Vgen>Vbus	Check Synchronization	Indicates that the generator voltage is greater than bus voltage + check sync. differential voltage setting (P342-6)
1350	CS Vgen<Vbus	Check Synchronization	Indicates the busbar voltage is greater than line voltage + check sync. differential voltage setting (P342-6)
1351	CS1 Fgen>Fbus	Check Synchronization	Indicates the generator frequency is greater than the busbar frequency + check sync. 1 slip frequency setting where check sync. 1 slip control is set to frequency (P342-6)
1352	CS1 Fgen<Fbus	Check Synchronization	Indicates the busbar frequency is greater than generator frequency + check sync. 1 slip frequency setting where check sync. 1 slip control is set to frequency (P342-6)
1353	CS1 Ang Not OK +	Check Synchronization	Indicates the generator angle leads the bus angle and falls in range + CS1 phase angle (deg.) to 180° (P342-6)
1354	CS1 Ang Not OK -	Check Synchronization	Indicates if the line angle lags the busbar angle and falls in range - CS1 phase angle (deg.) to -180° (P342-6)
1355	CS2 Fgen>Fbus	Check Synchronization	Indicates the generator frequency is greater than the busbar frequency + check sync. 2 slip frequency setting where check sync. 1 slip control is set to frequency (P342-6)
1356	CS2 Fgen<Fbus	Check Synchronization	Indicates the busbar frequency is greater than generator frequency + check sync. 2 slip frequency setting where check sync. 1 slip control is set to frequency (P342-6)
1357	CS2 Ang Not OK +	Check Synchronization	Indicates the generator angle leads the bus angle and falls in range + CS2 phase angle (deg.) to 180° (P342-6)
1358	CS2 Ang Not OK -	Check Synchronization	Indicates if the line angle lags the busbar angle and falls in range – CS2 phase angle (deg.) to -180° (P342-6)
1359	CS Ang Rot ACW	Check Synchronization	The direction of rotation of generator angle, using busbar as a reference, is anti-clockwise (ACW) (P342-6)
1360	CS Ang Rot CW	Check Synchronization	The direction of rotation of generator angle, using busbar as a reference, is clockwise (CW) (P342-6)
1361	CS Guard Enabled	Check Synchronization	Check Synch Guard is on. Check synch is blocked (P342-6)
1362	Man Check Synch	PSL	Input to the circuit breaker control logic to indicate manual check synchronization conditions are satisfied (P342-6)
1363	CS Guard Enable	PSL	Check Synch Guard Enable input (CS Block input) (P342-6)
1364 to 1375	Not Used		
1376	Control Input 1	Control Input Command	Control Input 1 - for SCADA and menu commands into PSL (P342-6/8)
1407	Control Input 32	Control Input Command	Control Input 32 - for SCADA and menu commands into PSL (P342-6/8)
1408	Virtual Input 1	GOOSE Input Command	Virtual Input 1 - allows binary signals that are mapped to virtual inputs to interface into PSL (P342-6/8)
1471	Virtual Input 64	GOOSE Input Command	Virtual Input 64 - allows binary signals that are mapped to virtual inputs to interface into PSL (P342-6/8)

DDB no.	English text	Source	Description
1472 to 1503	Not Used		
1504	Quality VIP 1	GOOSE	GOOSE Virtual input 1 Quality bit (P342-6/8)
1567	Quality VIP 64	GOOSE	GOOSE Virtual input 64 Quality bit (P342-6/8)
1568 to 1599	Not Used		
1600	PubPres VIP 1	GOOSE	GOOSE Virtual input 1 publisher bit (P342-6/8)
1663	PubPres VIP 64	GOOSE	GOOSE Virtual input 64 publisher bit (P342-6/8)
1664 to 1695	Not Used		
1696	Virtual Output 01	GOOSE	Virtual Output 1 - output allows user to control a binary signal which can be mapped via SCADA protocol output to other devices (P342-6/8)
1759	Virtual Output 64	GOOSE	Virtual Output 64 - output allows user to control a binary signal which can be mapped via SCADA protocol output to other devices (P342-6/8)
1760 to 1791	Not Used		
1792	PSL Int 1	PSL	PSL Internal Node (P342-6/8)
2047	PSL Int 256	PSL	PSL Internal Node (P342-6/8)

Table 1: Description of available Logic Nodes

1.8 Factory default programmable scheme logic

The following section details the default settings of the PSL. .

The P342/3/4/5/6/8 model options are as follows:

Model	Opto Inputs	Relay Outputs
P342xxxxxxxxxP	8-24	7-24
P343xxxxxxxxxM	16-32	14-32
P344xxxxxxxxxM	16-32	16-32
P345xxxxxxxxxM	16-32	16-32
P346xxxxxxxxxM	16-32	16-32
P348xxxxxxxxxM	16-32	16-32

Table 2: Default settings

1.9 Logic input mapping

The default mappings for each of the opto-isolated inputs are as shown in the following table:

Opto-Input number	P342 relay text	Function
1	Input L1	L1 Setting Group selection
2	Input L2	L2 Setting Group selection
3	Input L3	L3 Block IN>2 Timer
4	Input L4	L4 Block I>2 Timer
5	Input L5	L5 Reset Relays and LEDs
6	Input L6	L6 Ext Prot Trip
7	Input L7	L7 52a (CB Status)
8	Input L8	L8 52b (CB Status)

Opto-Input number	P342 relay text	Function
9	Input L9	L9 Not Used
10	Input L10	L10 Not Used
11	Input L11	L11 Not Used
12	Input L12	L12 Not Used
13	Input L13	L13 Not Used
14	Input L14	L14 Not Used
15	Input L15	L15 Not Used
16	Input L16	L16 Not Used
17	Input L17	L17 Not Used
18	Input L18	L18 Not Used
19	Input L19	L19 Not Used
20	Input L20	L20 Not Used
21	Input L21	L21 Not Used
22	Input L22	L22 Not Used
23	Input L23	L23 Not Used
24	Input L24	L24 Not Used

Table 3: P342 opto inputs default mappings

Opto-Input number	P343/4/5/6 relay text	Function
1	Input L1	L1 Setting Group selection
2	Input L2	L2 Setting Group selection
3	Input L3	L3 Block IN>2 Timer
4	Input L4	L4 Block I>2 Timer
5	Input L5	L5 Reset Relays and LEDs
6	Input L6	L6 Ext Prot Trip
7	Input L7	L7 52a (CB Status)
8	Input L8	L8 52b (CB Status)
9	Input L9	L9 Not Used
10	Input L10	L10 Not Used
11	Input L11	L11 Not Used
12	Input L12	L12 Not Used
13	Input L13	L13 Not Used
14	Input L14	L14 Not Used
15	Input L15	L15 Not Used
16	Input L16	L16 Not Used
17	Input L17	L17 Not Used
18	Input L18	L18 Not Used
19	Input L19	L19 Not Used
20	Input L20	L20 Not Used
21	Input L21	L21 Not Used
22	Input L22	L22 Not Used
23	Input L23	L23 Not Used
24	Input L24	L24 Not Used
25	Input L25	L25 Not Used
26	Input L26	L26 Not Used

Opto-Input number	P343/4/5/6 relay text	Function
27	Input L27	L27 Not Used
28	Input L28	L28 Not Used
29	Input L29	L29 Not Used
30	Input L30	L30 Not Used
31	Input L31	L31 Not Used
32	Input L32	L32 Not Used

Table 4: P343/4/5/6 opto inputs default mappings

Opto-Input number	P348 relay text	Function
1	Input L1	L1 Setting Group Selection
2	Input L2	L2 Setting Group Selection
3	Input L3	L3 Overcurrent Inhibit
4	Input L4	L4 Overvoltage Inhibit
5	Input L5	L5 Reset Relays and LEDs
6	Input L6	L6 NPS Overcurrent Inhibit
7	Input L7	L7 Neutral Voltage Inhibit
8	Input L8	L8 Machine Start and Overfrequency Inhibit
9	Input L9	L9 CTS-2 No Neutral Voltage
10	Input L10	L10 Not Used
11	Input L11	L11 Not Used
12	Input L12	L12 Not Used
13	Input L13	L13 Not Used
14	Input L14	L14 Not Used
15	Input L15	L15 Not Used
16	Input L16	L16 Not Used
17	Input L17	L17 Not Used
18	Input L18	L18 Not Used
19	Input L19	L19 Not Used
20	Input L20	L20 Not Used
21	Input L21	L21 Not Used
22	Input L22	L22 Not Used
23	Input L23	L23 Not Used
24	Input L24	L24 Not Used
25	Input L25	L25 Not Used
26	Input L26	L26 Not Used
27	Input L27	L27 Not Used
28	Input L28	L28 Not Used
29	Input L29	L29 Not Used
30	Input L30	L30 Not Used
31	Input L31	L31 Not Used
32	Input L32	L32 Not Used

Table 5: P348 opto inputs default mappings

1.10 Relay output contact mapping

The default mappings for each of the relay output contacts are as shown in the following table:

Relay contact number	P342 relay text	P342 relay conditioner	Function
1	Output R1	Dwell 100 ms	R1 Trip CB
2	Output R2	Dwell 100 ms	R2 Trip Prime Mover
3	Output R3	Dwell 100 ms	R3 Any Protection Trip
4	Output R4	Delayed Drop-off timer 500 ms	R4 General Alarm
5	Output R5	Dwell 100 ms	R5 CB Fail
6	Output R6	Straight-through	R6 Earth Fault Protection Trip
7	Output R7	Straight-through	R7 Voltage or Frequency Protection Trip
8	Output R8	Straight-through	R8 Not Used
9	Output R9	Straight-through	R9 Not Used
10	Output R10	Straight-through	R10 Not Used
11	Output R11	Straight-through	R11 Not Used
12	Output R12	Straight-through	R12 Not Used
13	Output R13	Straight-through	R13 Not Used
14	Output R14	Straight-through	R14 Not Used
15	Output R15	Straight-through	R15 Not Used
16	Output R16	Straight-through	R16 Not Used
17	Output R17	Straight-through	R17 Not Used
18	Output R18	Straight-through	R18 Not Used
19	Output R19	Straight-through	R19 Not Used
20	Output R20	Straight-through	R20 Not Used
21	Output R21	Straight-through	R21 Not Used
22	Output R22	Straight-through	R22 Not Used
23	Output R23	Straight-through	R23 Not Used
24	Output R24	Straight-through	R24 Not Used

Table 6: P342 relay output contacts default mappings

Relay contact number	P343/4/5/6 relay text	P343/4/5/6 relay conditioner	Function
1	Output R1	Dwell 100 ms	R1 Trip CB
2	Output R2	Dwell 100 ms	R2 Trip Prime Mover
3	Output R3	Dwell 100 ms	R3 Any Protection Trip
4	Output R4	Delayed Drop-off timer 500 ms	R4 General Alarm
5	Output R5	Dwell 100 ms	R5 CB Fail
6	Output R6	Straight-through	R6 Earth Fault Protection Trip
7	Output R7	Straight-through	R7 Voltage Protection Trip
8	Output R8	Straight-through	R8 Frequency Protection trip
9	Output R9	Straight-through	R9 Differential Protection Trip
10	Output R10	Straight-through	R10 System Back-up Protection Trip
11	Output R11	Straight-through	R11 NPS Protection Trip
12	Output R12	Straight-through	R12 Field Failure Protection Trip
13	Output R13	Straight-through	R13 Power Protection Trip
14	Output R14	Straight-through	R14 V/Hz Protection Trip

Relay contact number	P343/4/5/6 relay text	P343/4/5/6 relay conditioner	Function
15	Output R15	Straight-through	R15 Not Used
16	Output R16	Straight-through	R16 Not Used
17	Output R17	Straight-through	R17 Not Used
18	Output R18	Straight-through	R18 Not Used
19	Output R19	Straight-through	R19 Not Used
20	Output R20	Straight-through	R20 Not Used
21	Output R21	Straight-through	R21 Not Used
22	Output R22	Straight-through	R22 Not Used
23	Output R23	Straight-through	R23 Not Used
24	Output R24	Straight-through	R24 Not Used
25	Output R25	Straight-through	R25 Not Used
26	Output R26	Straight-through	R26 Not Used
27	Output R27	Straight-through	R27 Not Used
28	Output R28	Straight-through	R28 Not Used
29	Output R29	Straight-through	R29 Not Used
30	Output R30	Straight-through	R30 Not Used
31	Output R31	Straight-through	R31 Not Used
32	Output R32	Straight-through	R32 Not Used

Table 7: P343/4/5/6 relay output contacts default mappings

Relay contact number	P348 relay text	P348 relay conditioner	Function
1	Output R1	Straight-through	R1 Overcurrent Trip
2	Output R2	Straight-through	R2 Overvoltage Trip
3	Output R3	Dwell 100 ms	R3 Any Protection Trip
4	Output R4	Delayed Drop-off timer 500 ms	R4 General Alarm
5	Output R5	Straight-through	R5 NPS Overcurrent Trip
6	Output R6	Straight-through	R6 Neutral Voltage Trip
7	Output R7	Straight-through	R7 Overfrequency Trip
8	Output R8	Straight-through	R8 Current Loop Input Trip
9	Output R9	Delayed Drop-off timer 500 ms	R9 IEC 61850-9-2 Alarm
10	Output R10	Straight-through	R10 Not Used
11	Output R11	Straight-through	R11 Not Used
12	Output R12	Straight-through	R12 Not Used
13	Output R13	Straight-through	R13 Not Used
14	Output R14	Straight-through	R14 Not Used
15	Output R15	Straight-through	R15 Not Used
16	Output R16	Straight-through	R16 Not Used
17	Output R17	Straight-through	R17 Not Used
18	Output R18	Straight-through	R18 Not Used
19	Output R19	Straight-through	R19 Not Used
20	Output R20	Straight-through	R20 Not Used
21	Output R21	Straight-through	R21 Not Used
22	Output R22	Straight-through	R22 Not Used
23	Output R23	Straight-through	R23 Not Used

Relay contact number	P348 relay text	P348 relay conditioner	Function
24	Output R24	Straight-through	R24 Not Used
25	Output R25	Straight-through	R25 Not Used
26	Output R26	Straight-through	R26 Not Used
27	Output R27	Straight-through	R27 Not Used
28	Output R28	Straight-through	R28 Not Used
29	Output R29	Straight-through	R29 Not Used
30	Output R30	Straight-through	R30 Not Used
31	Output R31	Straight-through	R31 Not Used
32	Output R32	Straight-through	R32 Not Used

Table 8: P348 relay output contacts default mappings

Note: A fault record can be generated by connecting one or a number of contacts to the "Fault Record Trigger" in PSL. It is recommended that the triggering contact be 'self reset' and not a latching. If a latching contact were chosen the fault record would not be generated until the contact had fully reset.

1.11 Programmable LED output mapping

The default mappings for each of the programmable LEDs are as shown in the following table for the P342 which have red LEDs:

LED number	LED Input connection/text	Latched	P342 LED function indication
1	LED 1 Red	Yes	Earth Fault Protection Trip
2	LED 2 Red	Yes	Overcurrent Protection Trip
3	LED 3 Red	Yes	Field Failure Protection Trip
4	LED 4 Red	Yes	NPS Protection Trip
5	LED 5 Red	Yes	Voltage Protection Trip
6	LED 6 Red	Yes	Frequency Protection Trip
7	LED 7 Red	Yes	Power ProtectionTrip
8	LED 8 Red	No	Any Start

Table 9: P342 programmable LED default mappings

The default mappings for each of the programmable LEDs are as shown in the following tables for the P343/4/5/6/8 which have tri-color LEDS (red/yellow/green):

LED number	LED Input connection/text	Latched	P343/4/5/6 LED function indication
1	LED 1 Red	Yes	Earth Fault Protection Trip
2	LED 2 Red	Yes	Overcurrent Protection Trip
3	LED 3 Red	Yes	Field Failure Protection Trip
4	LED 4 Red	Yes	NPS Protection Trip
5	LED 5 Red	Yes	Voltage Protection Trip
6	LED 6 Red	Yes	Frequency Protection Trip
7	LED 7 Red	Yes	Power Protection Trip
8	LED 8 Red	No	Any Start
9	FnKey LED1	No	Not Used
10	FnKey LED2	No	Not Used
11	FnKey LED3	No	Not Used
12	FnKey LED4 Red (Fnct Key is Toggled mode)	No	Inhibit Turbine Abnormal Frequency Protection

LED number	LED Input connection/text	Latched	P343/4/5/6 LED function indication
13	FnKey LED5 Red (Fnct Key is Toggled mode)	No	Enable Setting Group 2
14	FnKey LED6	No	Not Used
15	FnKey LED7 Yellow (Fnct Key is Normal mode)	No	Reset NPS Thermal Measurement to 0
16	FnKey LED8 Yellow (Fnct Key is Normal mode)	No	Reset Thermal Overload Measurement to 0
17	FnKey LED9 Yellow (Fnct Key is Normal mode)	No	Reset Relays and LEDs
18	FnKey LED10 Yellow (Fnct Key is Normal mode)	No	Trigger Disturbance Recorder

Table 10: P343/4/5/6 programmable LED default mappings

LED number	LED Input connection/text	Latched	P348 LED function indication
1	LED 1 Red	No	Overcurrent Trip
2	LED 2 Red	No	Overvoltage Trip
3	LED 3 Red	No	NPS Overcurrent Trip
4	LED 4 Red	No	Neutral Voltage Trip
5	LED 5 Red	No	Overfrequency Trip
6	LED 6 Red	No	Current Loop Input Trip
7	LED 7 Red	No	Machine Start and Overfrequency Inhibit
8	LED 8 Red	No	Any Start
9	FnKey LED1	No	Function Key 1
10	FnKey LED2	No	Function Key 2
11	FnKey LED3	No	Function Key 3
12	FnKey LED4 Red (Fnct Key is Toggled mode)	No	Function Key 4
13	FnKey LED5 Red (Fnct Key is Toggled mode)	No	Setting Group 2 Enabled
14	FnKey LED6	No	Function Key 6
15	FnKey LED7 Yellow (Fnct Key is Normal mode)	No	Function Key 7
16	FnKey LED8 Yellow (Fnct Key is Normal mode)	No	Function Key 8
17	FnKey LED9 Yellow (Fnct Key is Normal mode)	No	Reset Relays and LEDs
18	FnKey LED10 Yellow (Fnct Key is Normal mode)	No	Trigger Disturbance Recorder

Table 11: P348 programmable LED default mappings

1.12 Fault recorder start mapping

The default mapping for the signal which initiates a fault record is as shown in the following table:

Initiating Signal	Fault Trigger
Relay 3 (DDB 002)	Initiate fault recording from main protection trip

1.13 PSL DATA column

The P34x relay contains a PSL DATA column that can be used to track PSL modifications. A total of 12 cells are contained in the PSL DATA column, 3 for each setting group. The function for each cell is shown below:

Grp. PSL Ref.	When downloading a PSL to the relay, the user will be prompted to enter which group the PSL is for and a reference identifier. The first 32 characters of the reference ID will be displayed in this cell The ⟨ and ⟩ keys can be used to scroll through 32 characters as only 16 can be displayed at any one time.
18 Nov 2002 08:59:32.047	This cell displays the date and time when the PSL was down loaded to the relay.
Grp. 1 PSL ID - 2062813232	This is a unique number for the PSL that has been entered. Any change in the PSL will result in a different number being displayed.

Note: The above cells are repeated for each setting group.

2 P342 PROGRAMMABLE SCHEME LOGIC

2.1 Input Mappings

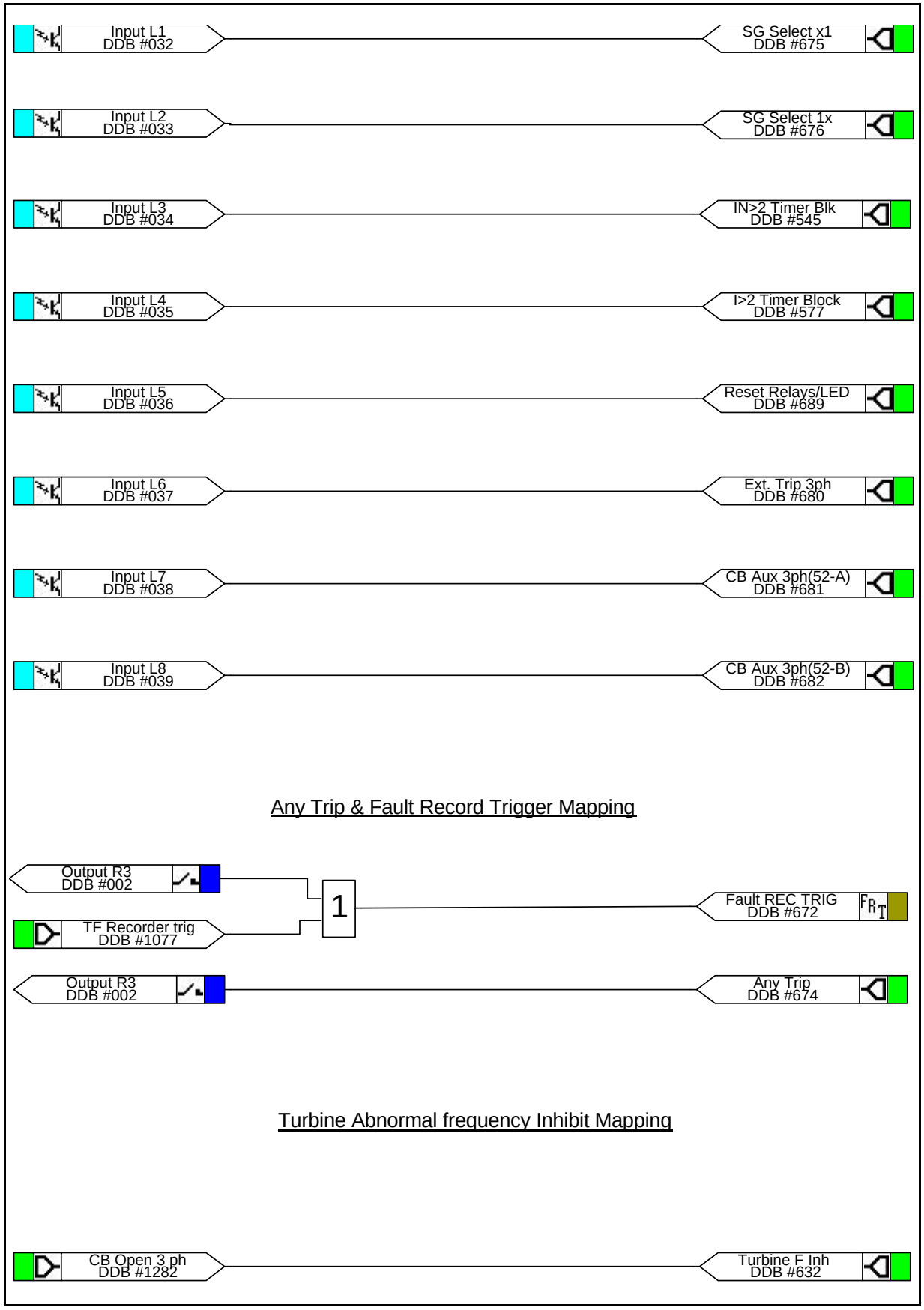


Figure 1: Opto input mappings

2.2 Output Mappings

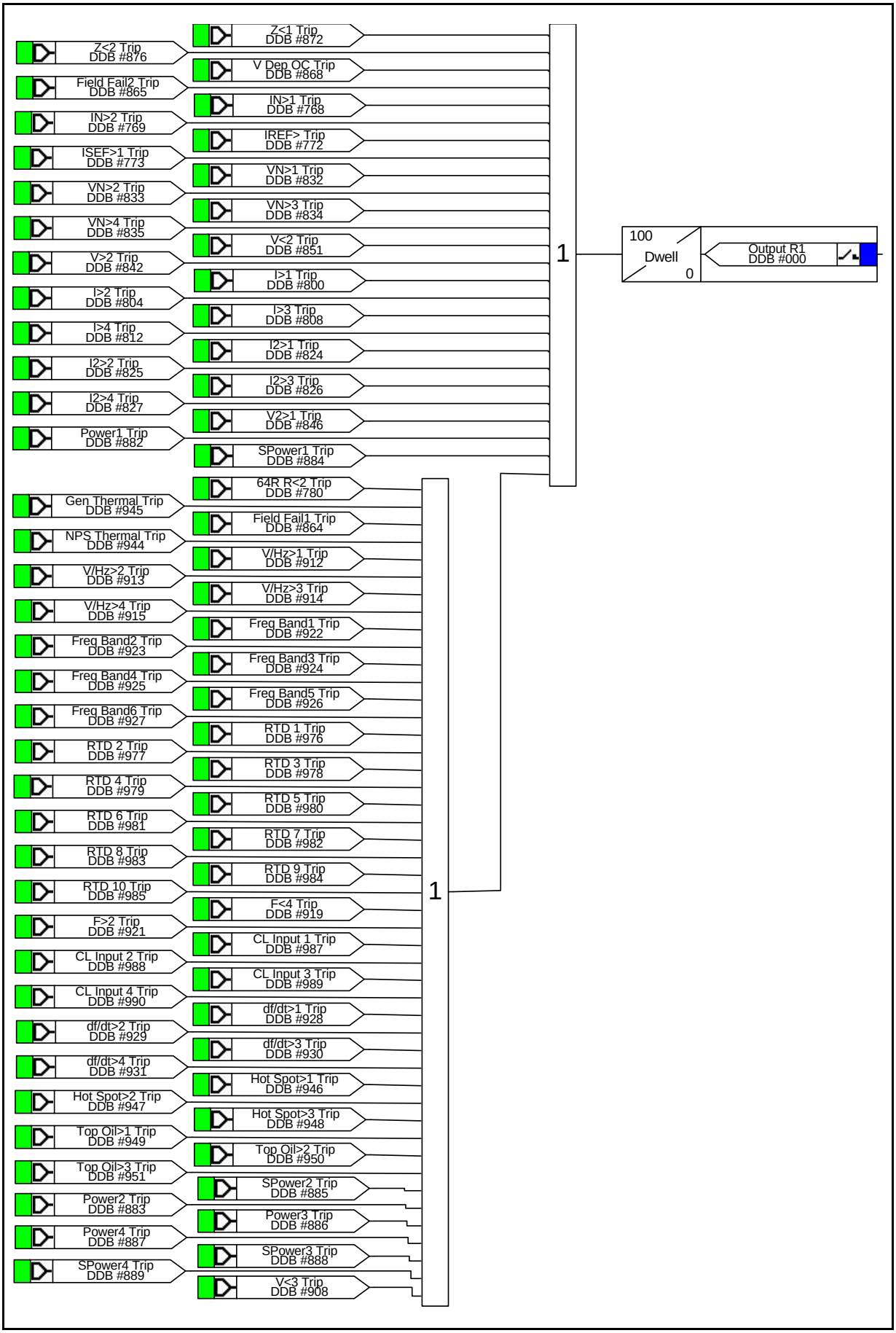


Figure 2: Output relay R1 (Trip CB) mappings

PL

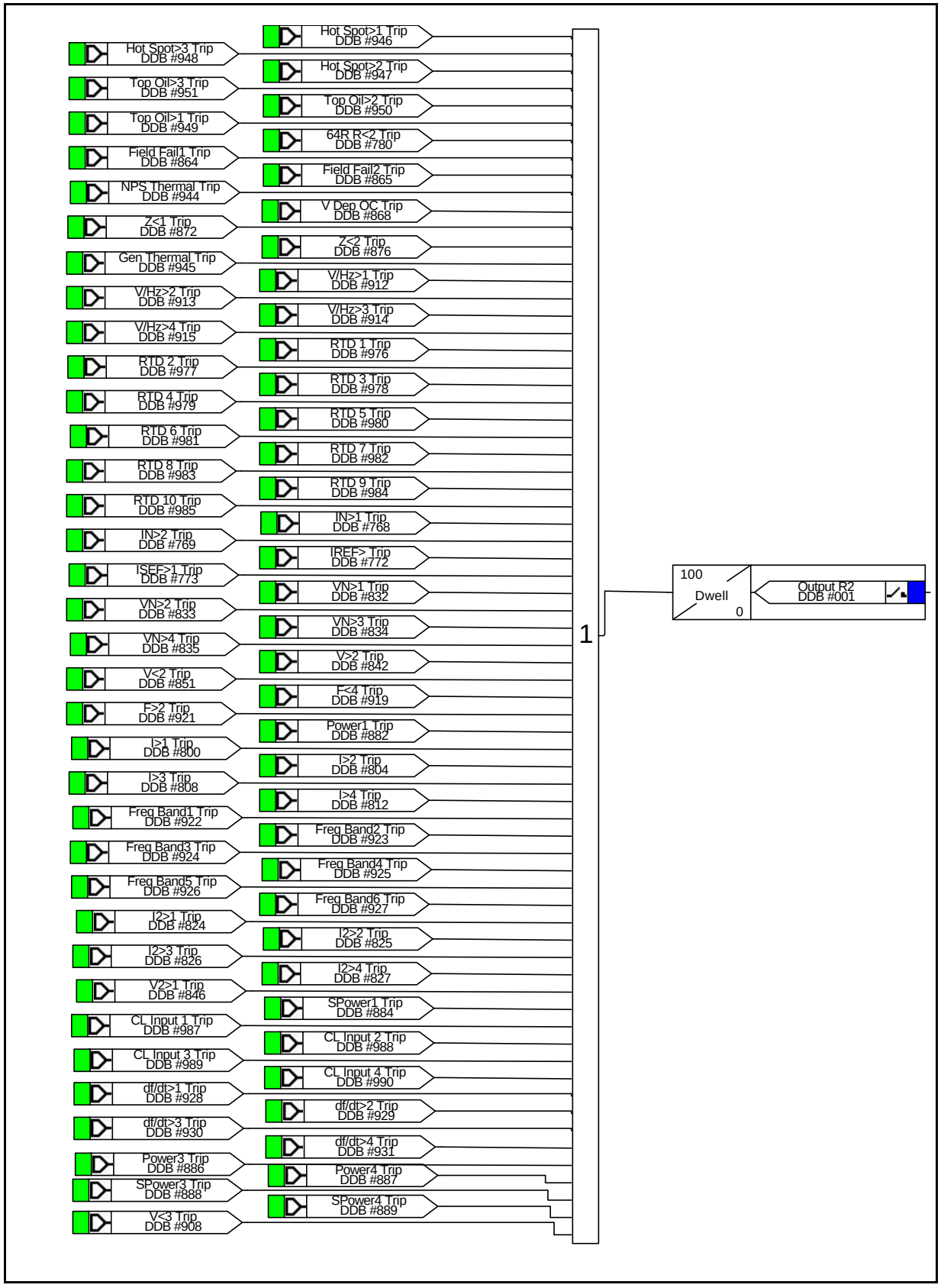


Figure 3: Output relay R2 (Trip Prime Mover) mappings

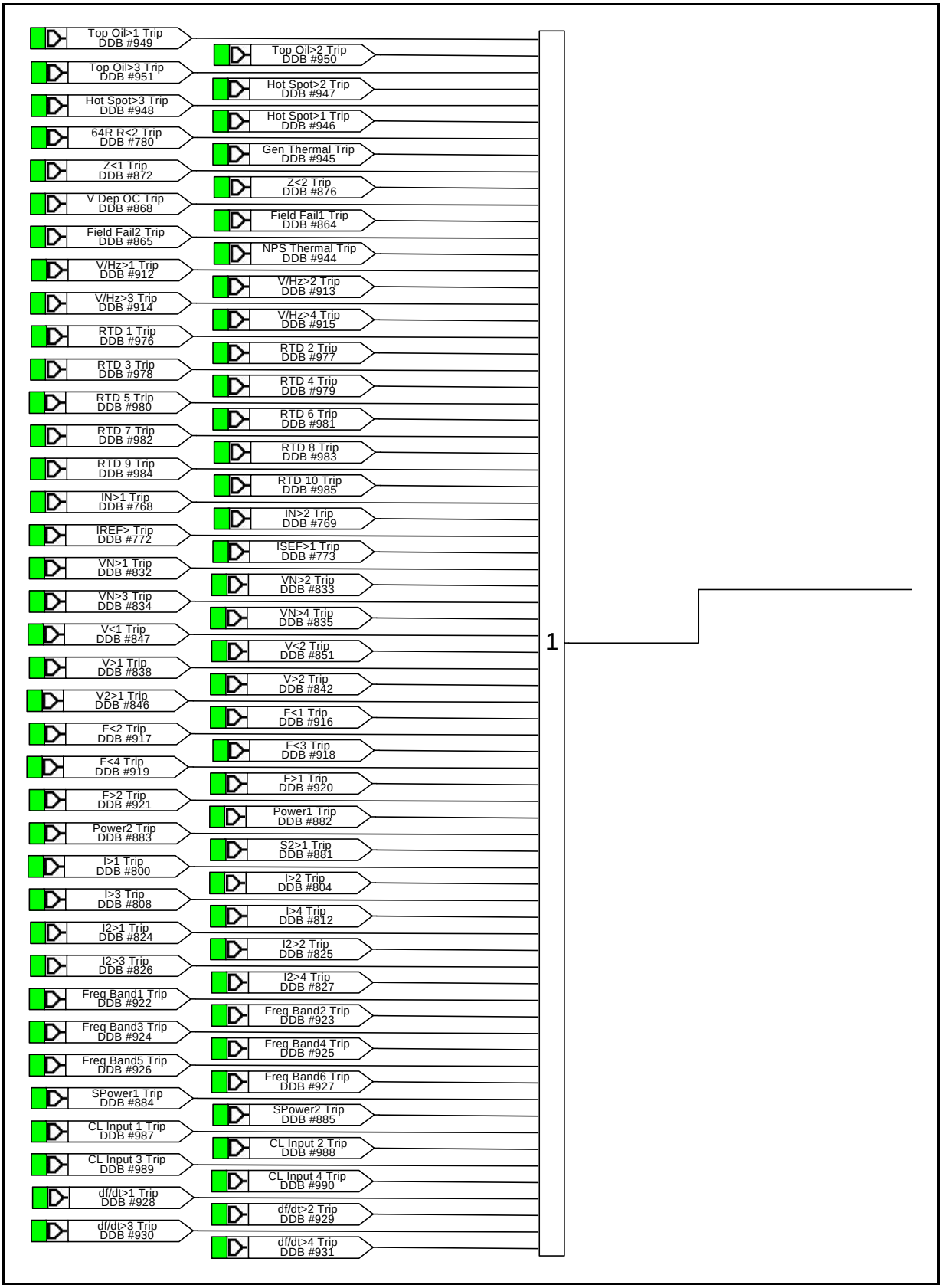


Figure 4: Output relay R3 (Any Trip) mappings

PL

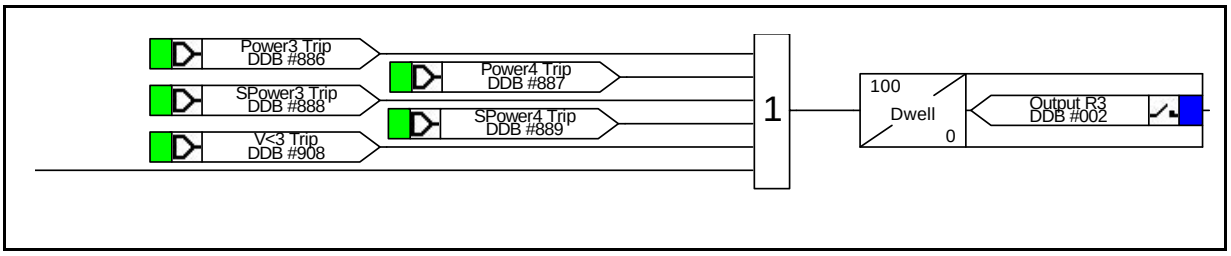


Figure 5: Output relay R3 (Any Trip) mappings

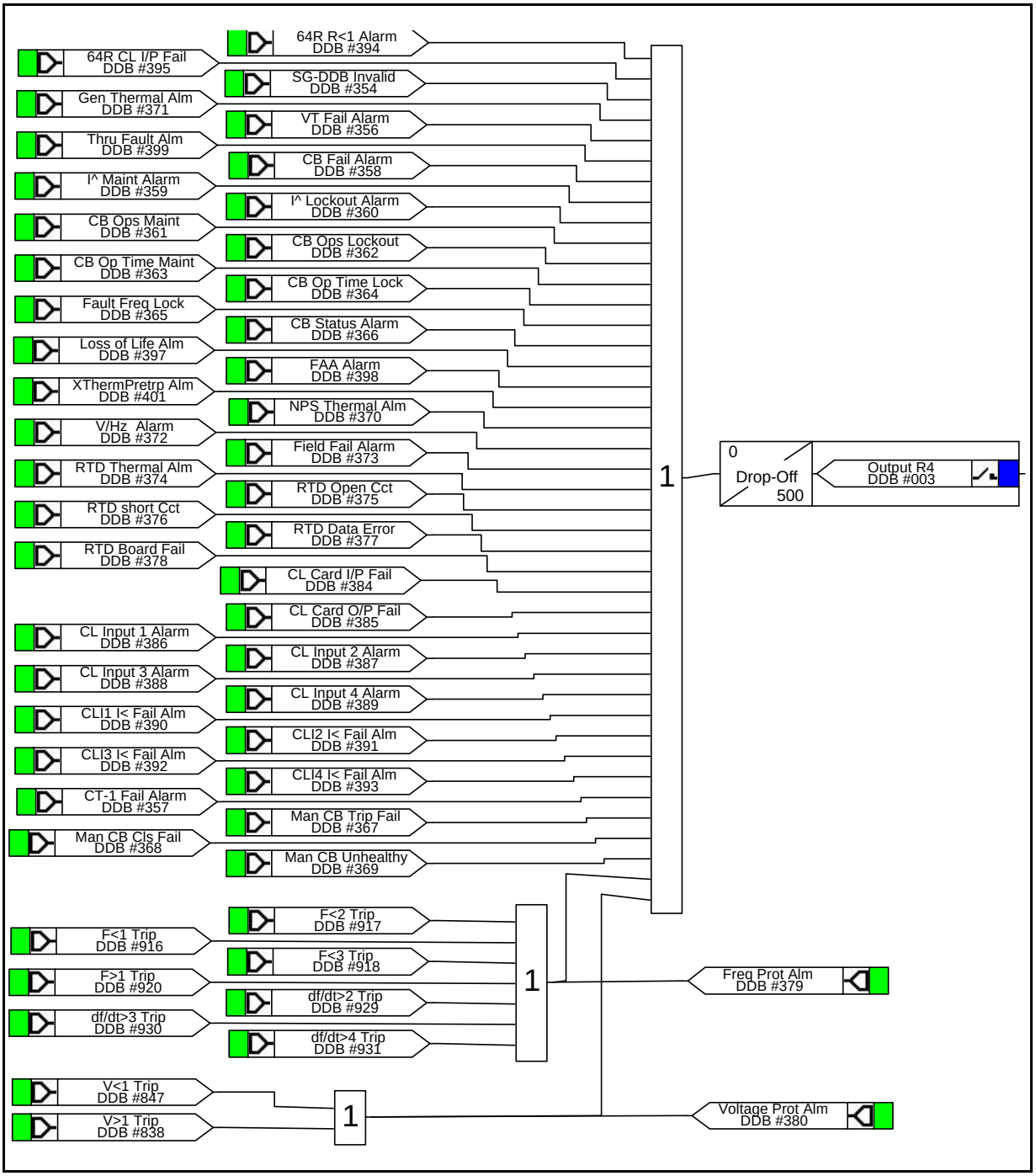


Figure 6: Output relay R4 (General Alarm) mappings

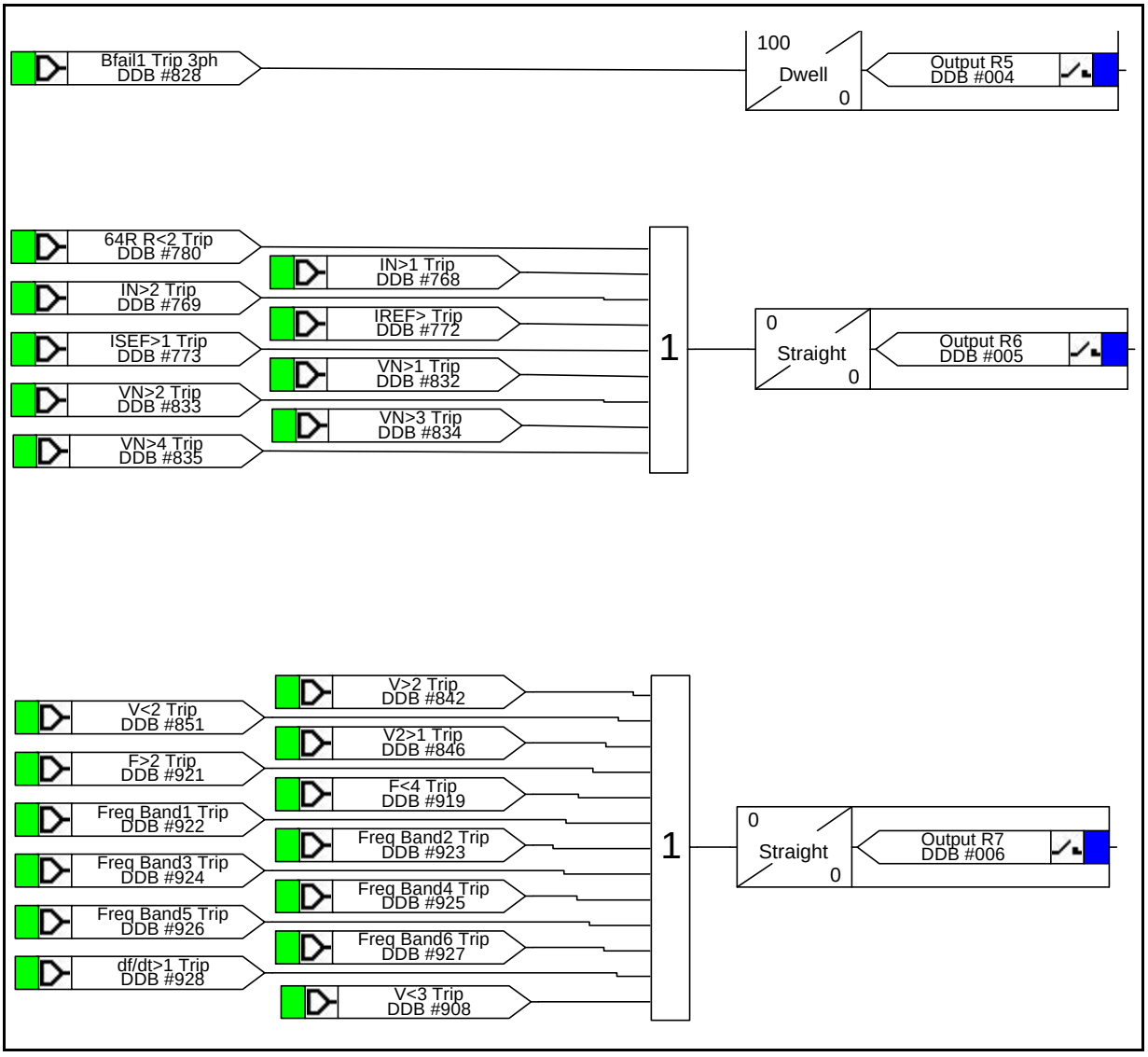


Figure 7: Output relay mappings

2.3 Check Synch Mapping

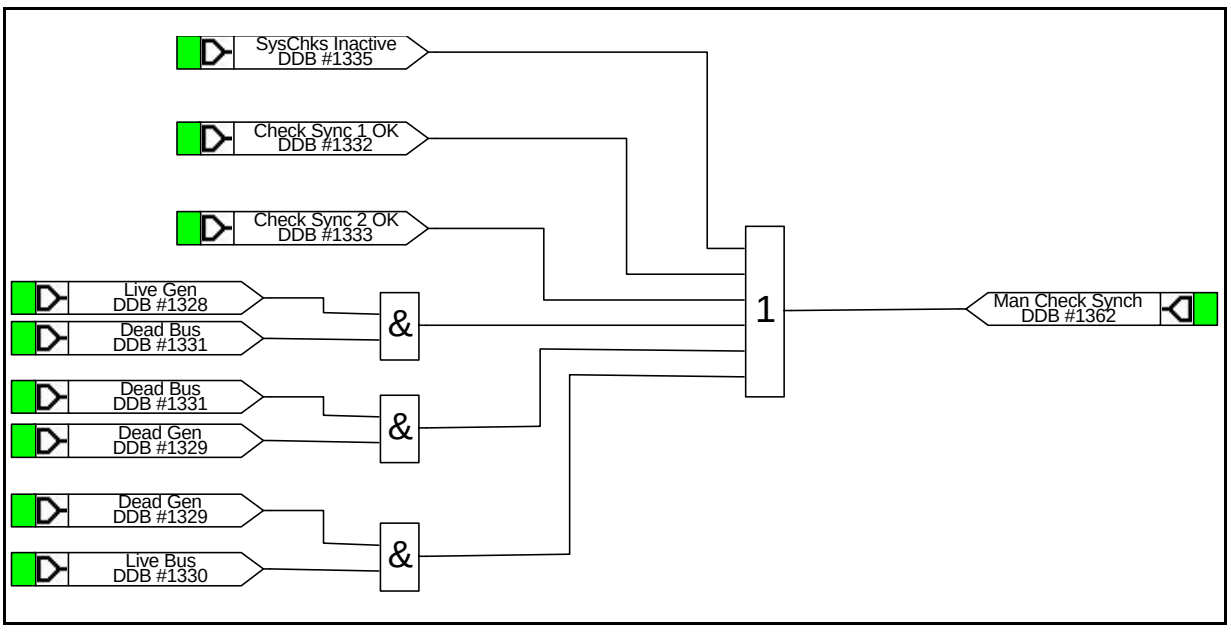


Figure 8: Check synch & voltage monitor mapping

PL

2.4 LED Mappings

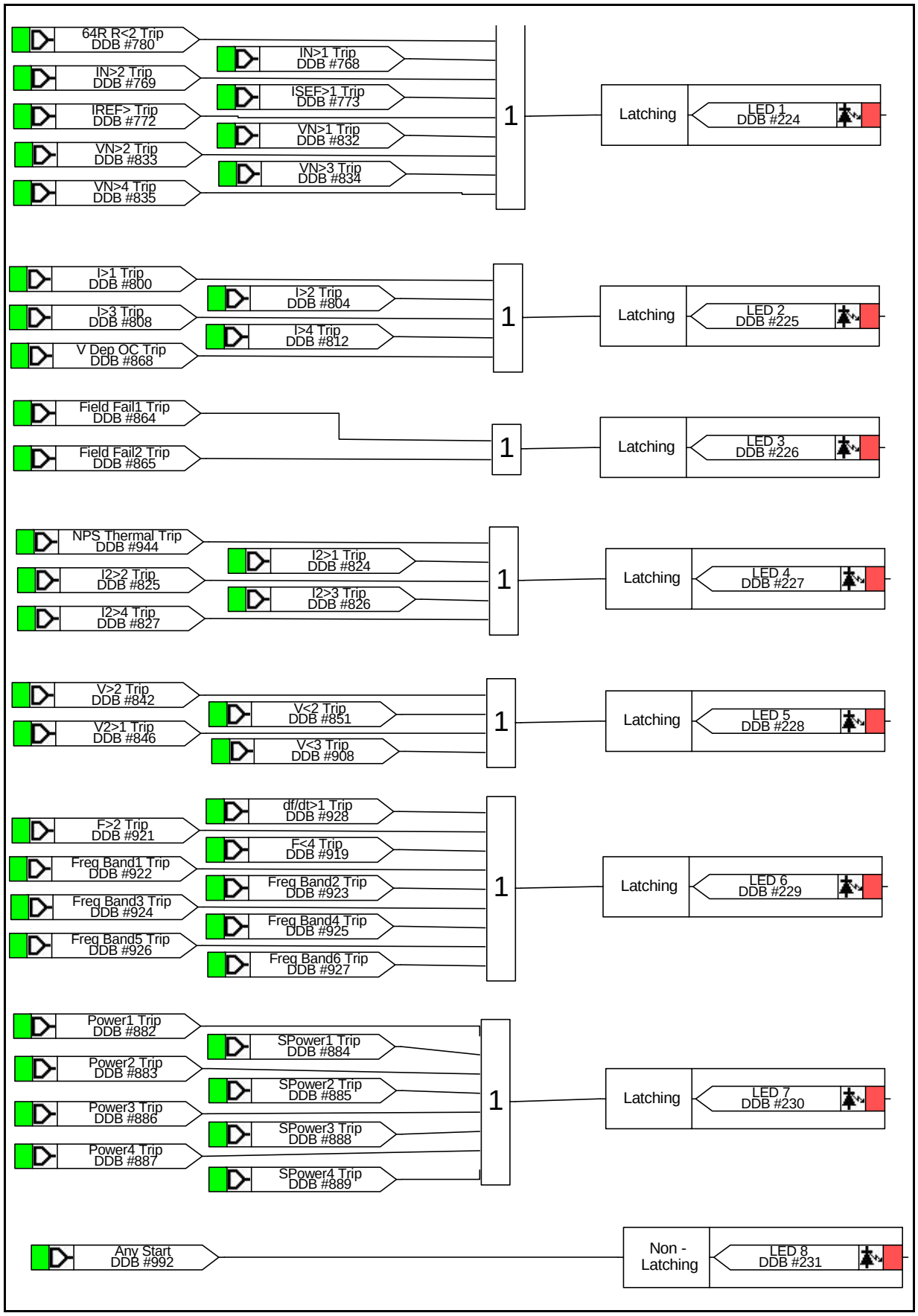


Figure 9: LED output mappings

3 P343 PROGRAMMABLE SCHEME LOGIC

3.1 Input Mappings

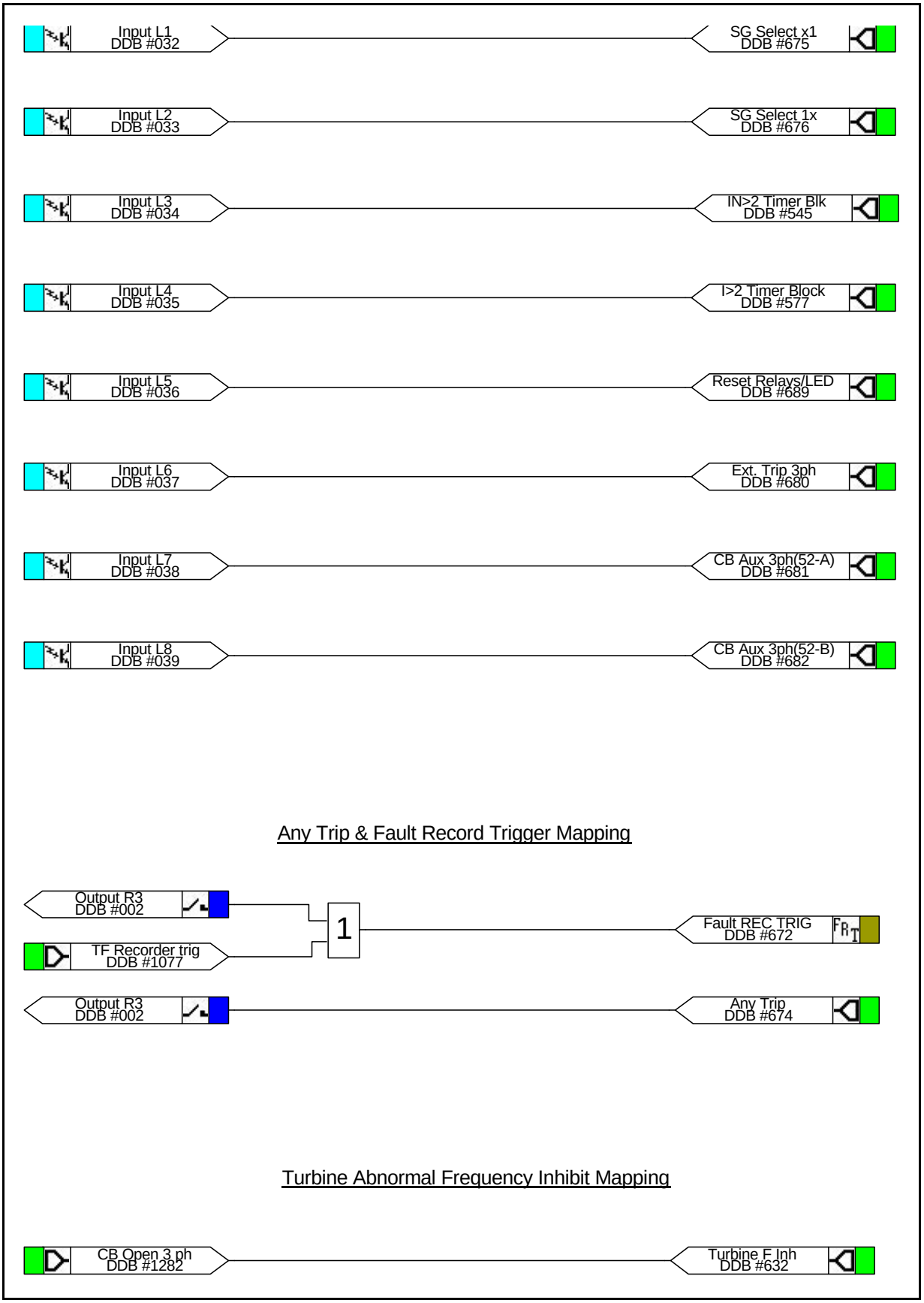


Figure 10: Opto input mappings

PL

PL

3.2 Output Mappings

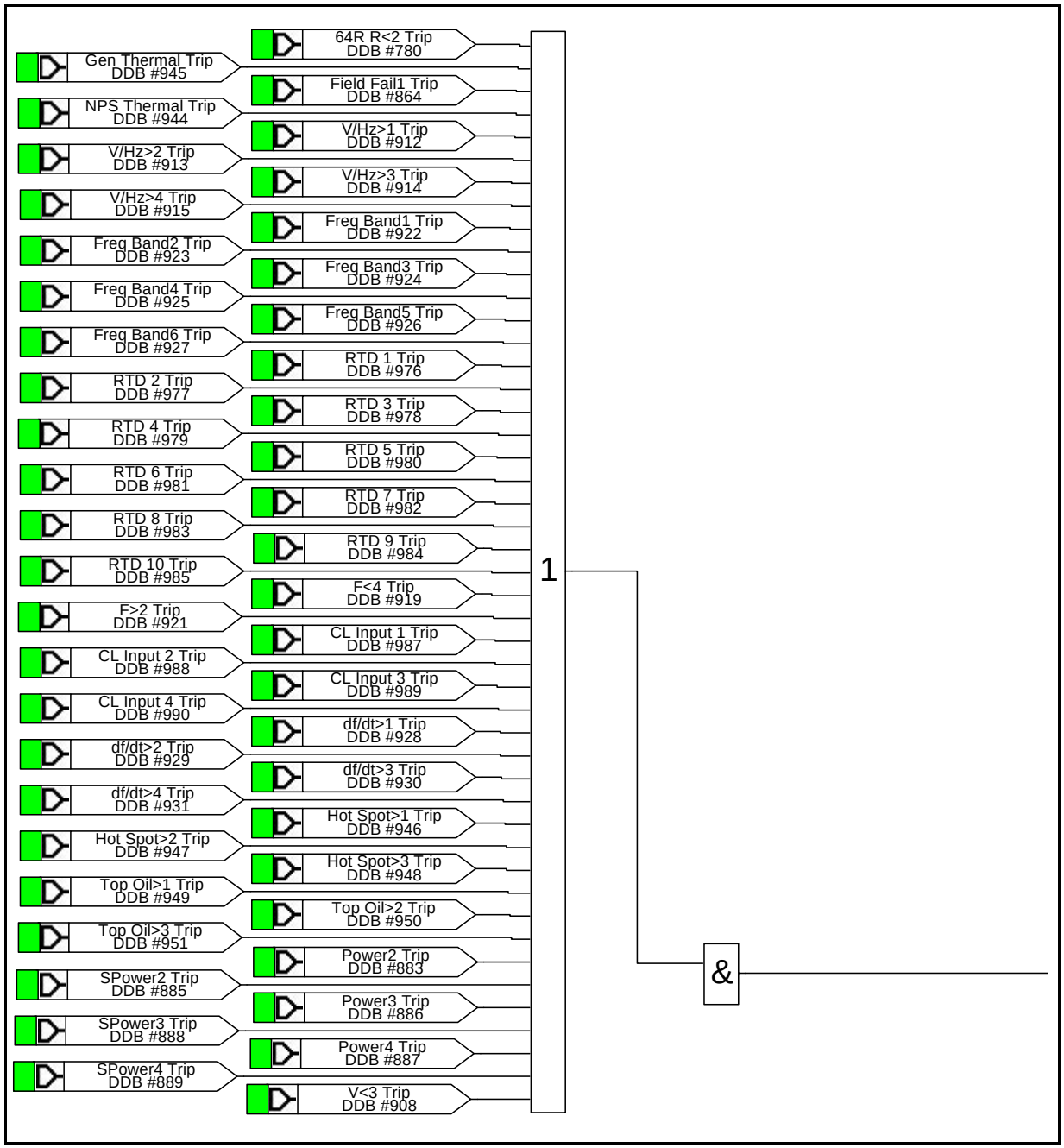


Figure 11: Output relay R1 (Trip CB) mappings

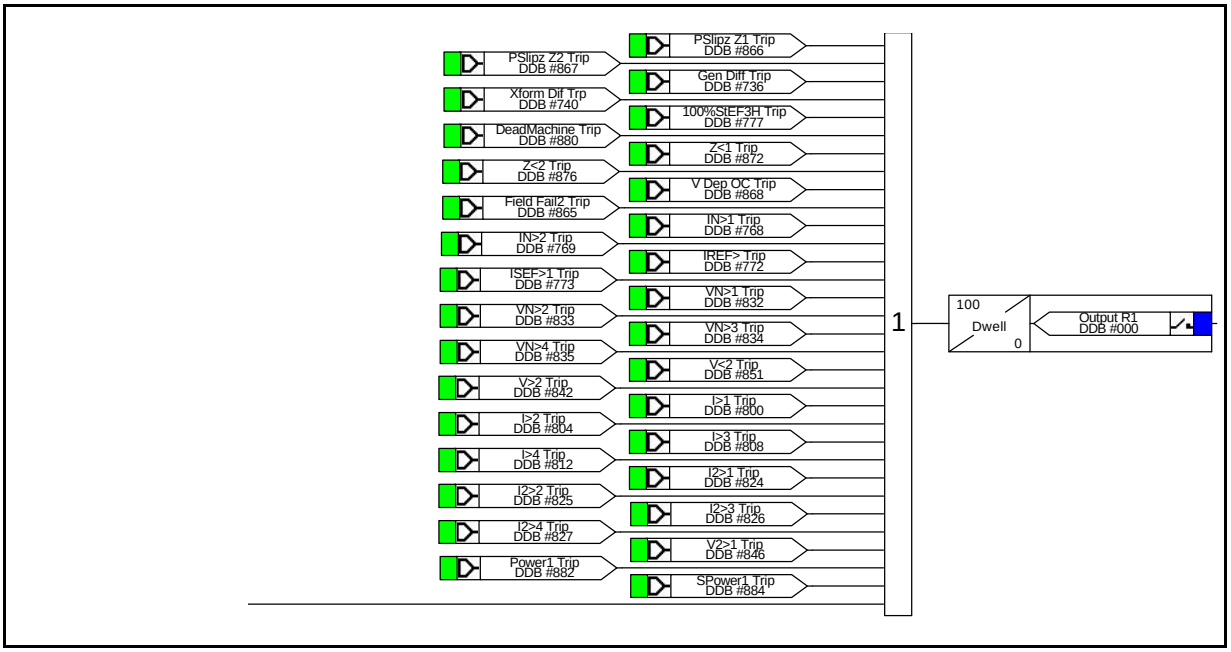


Figure 12: Output relay R1 (Trip CB) mappings

PL

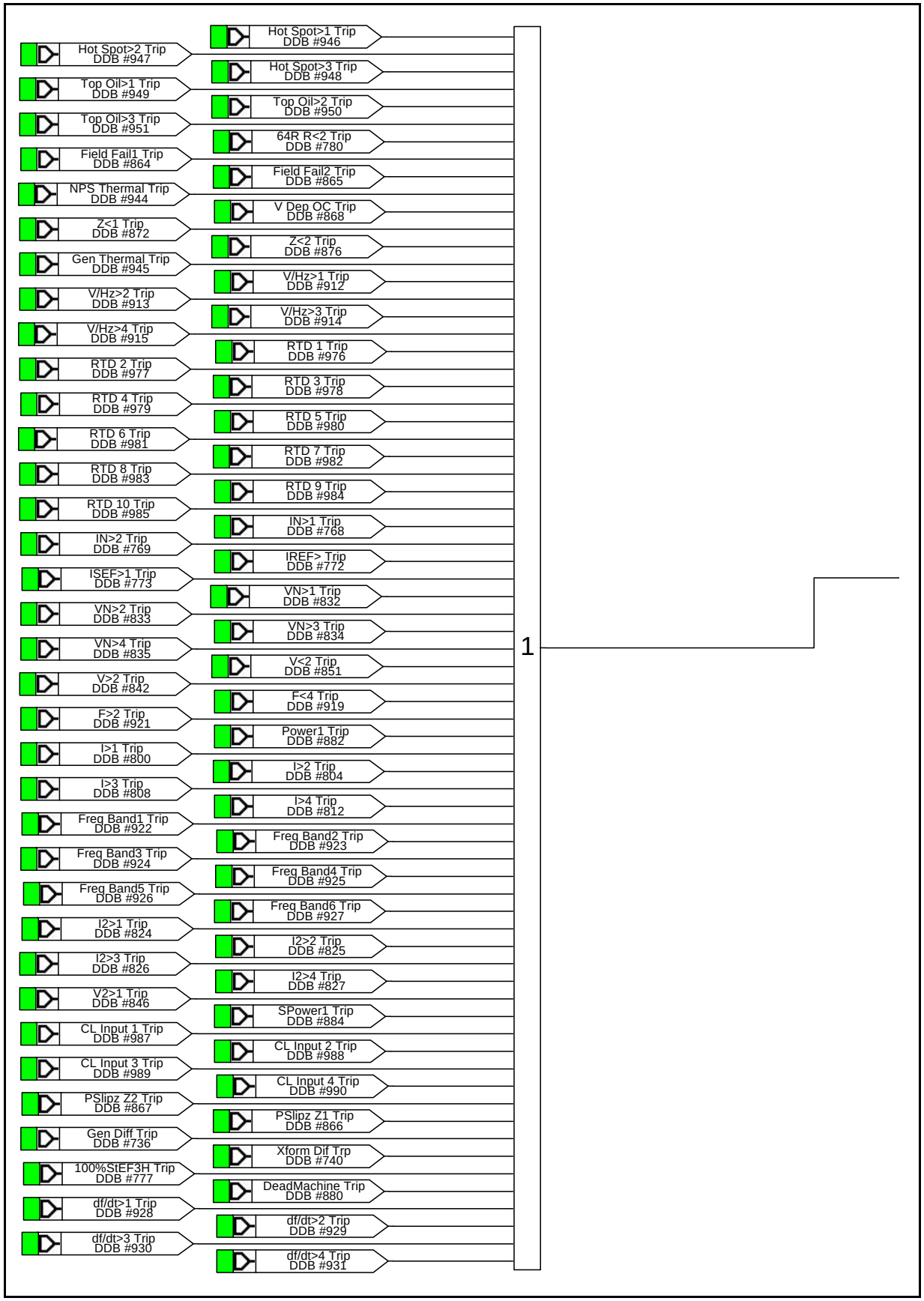


Figure 13: Output relay R2 (Trip Prime Mover) mappings

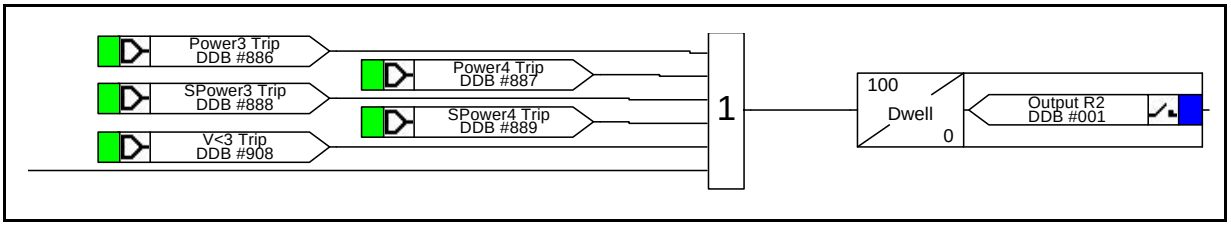


Figure 14: Output relay R2 (Trip Prime Mover) mappings

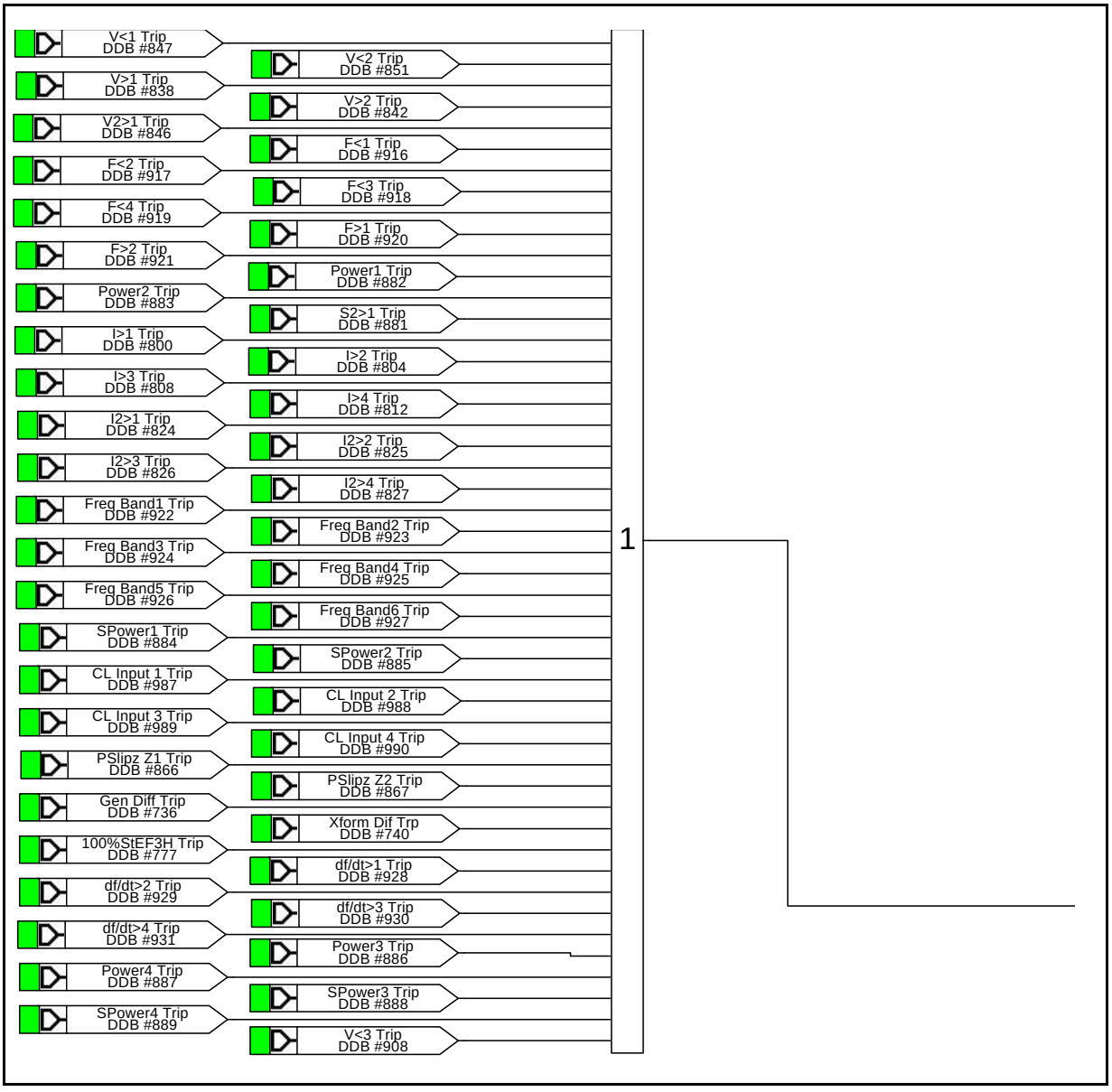


Figure 15: Output relay R3 (Any Trip) mappings

PL

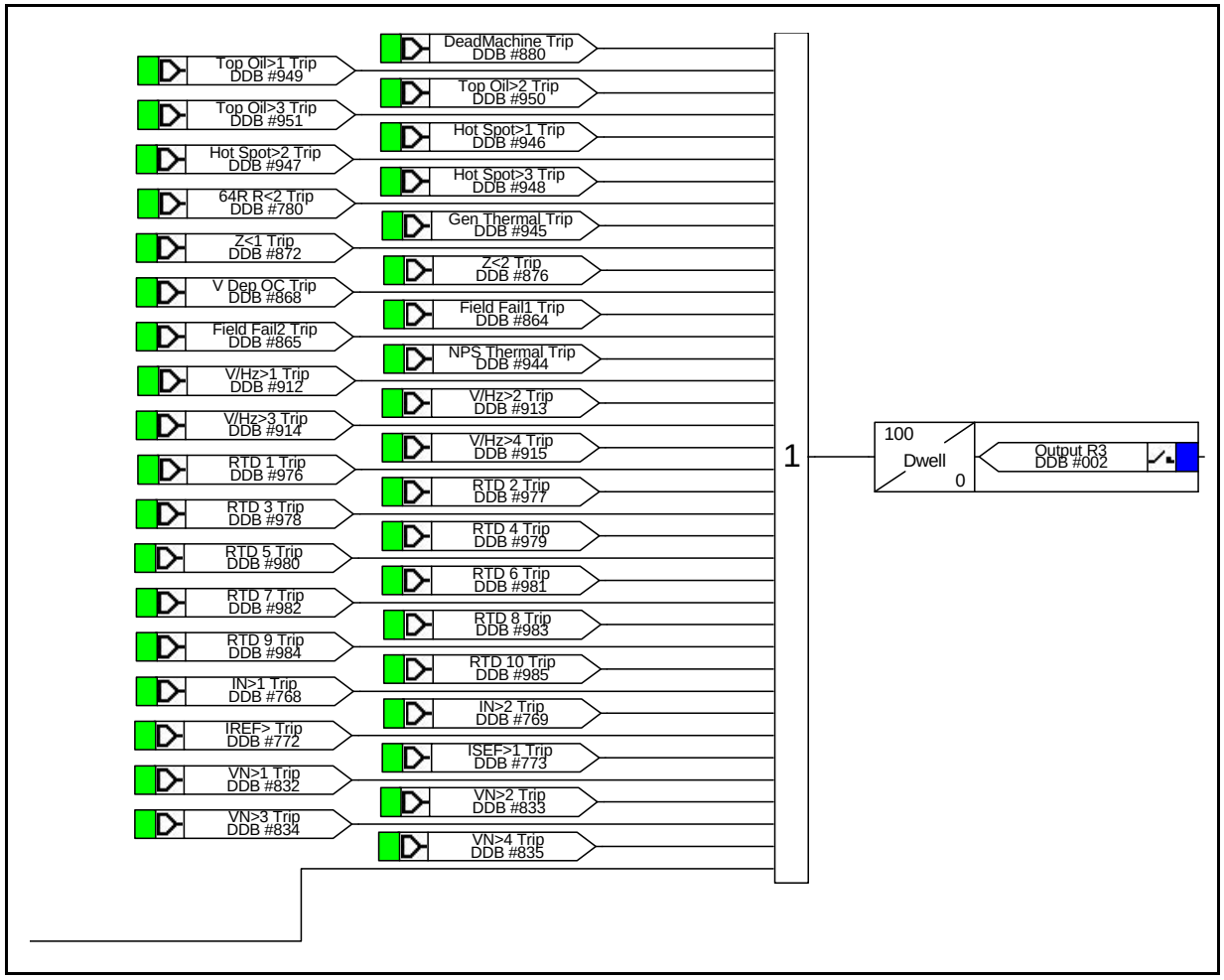


Figure 16: Output relay R3 (Any Trip) mappings

PL

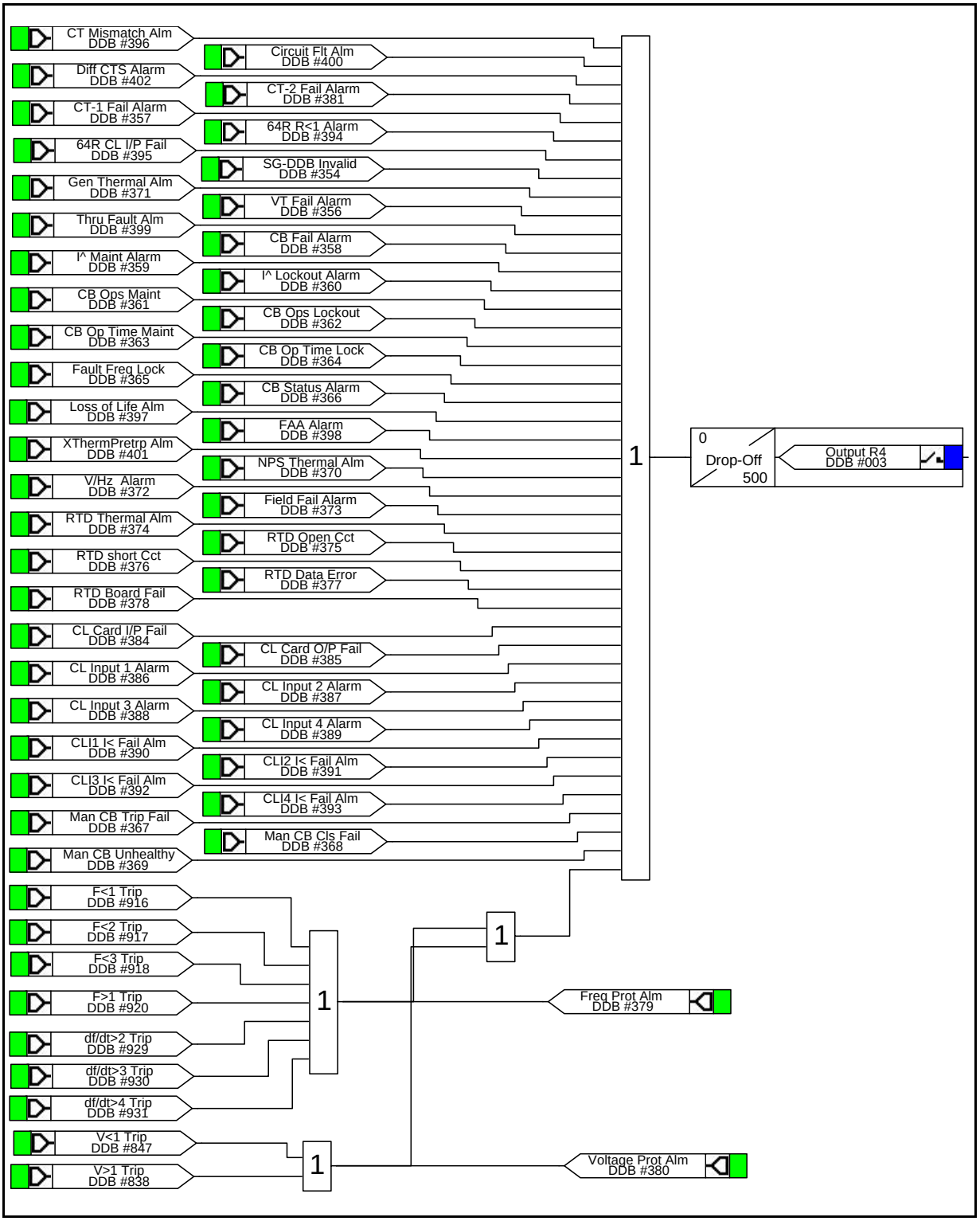


Figure 17: Output relay R4 (General Alarm) mappings

PL

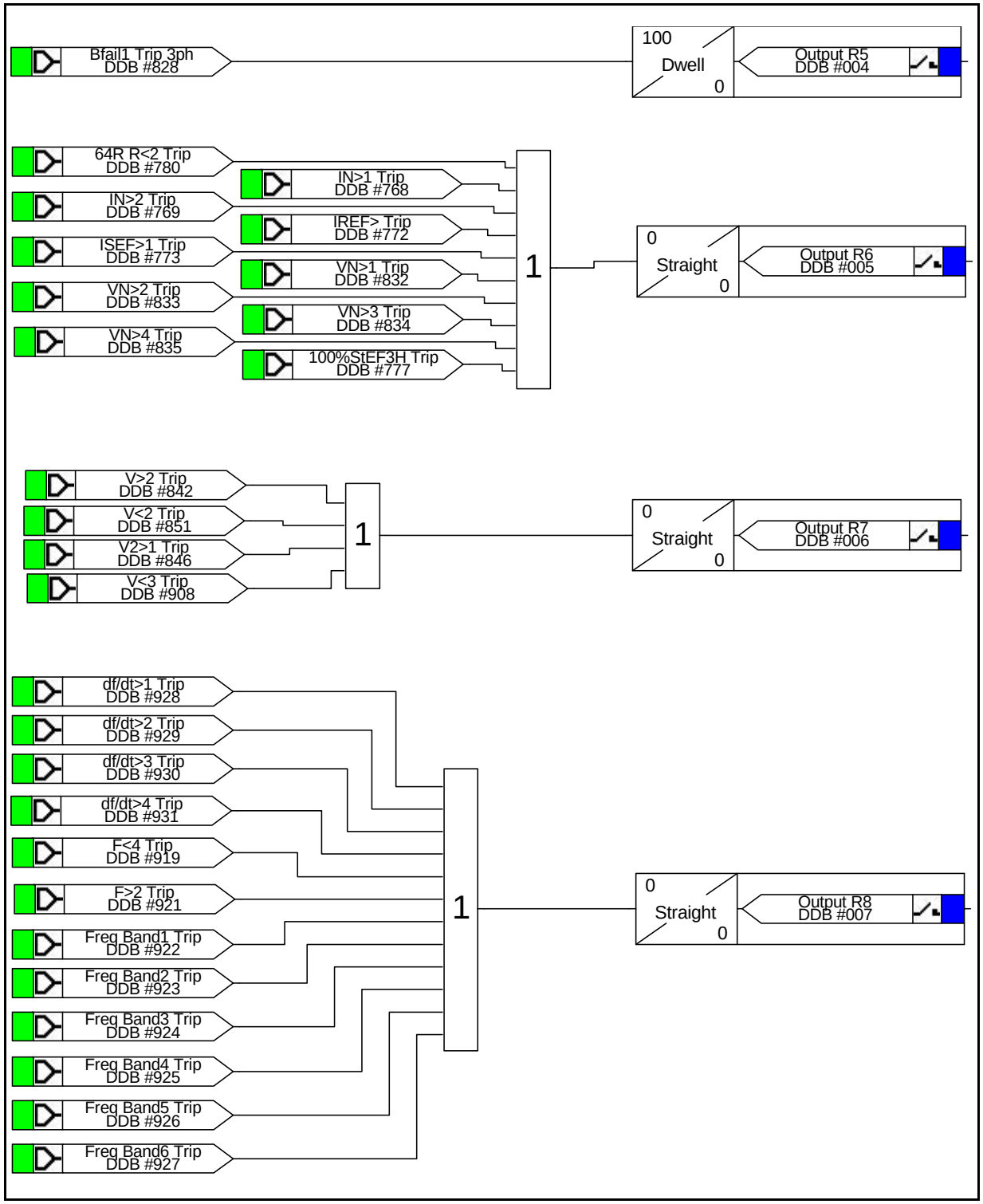


Figure 18: Output relay mappings

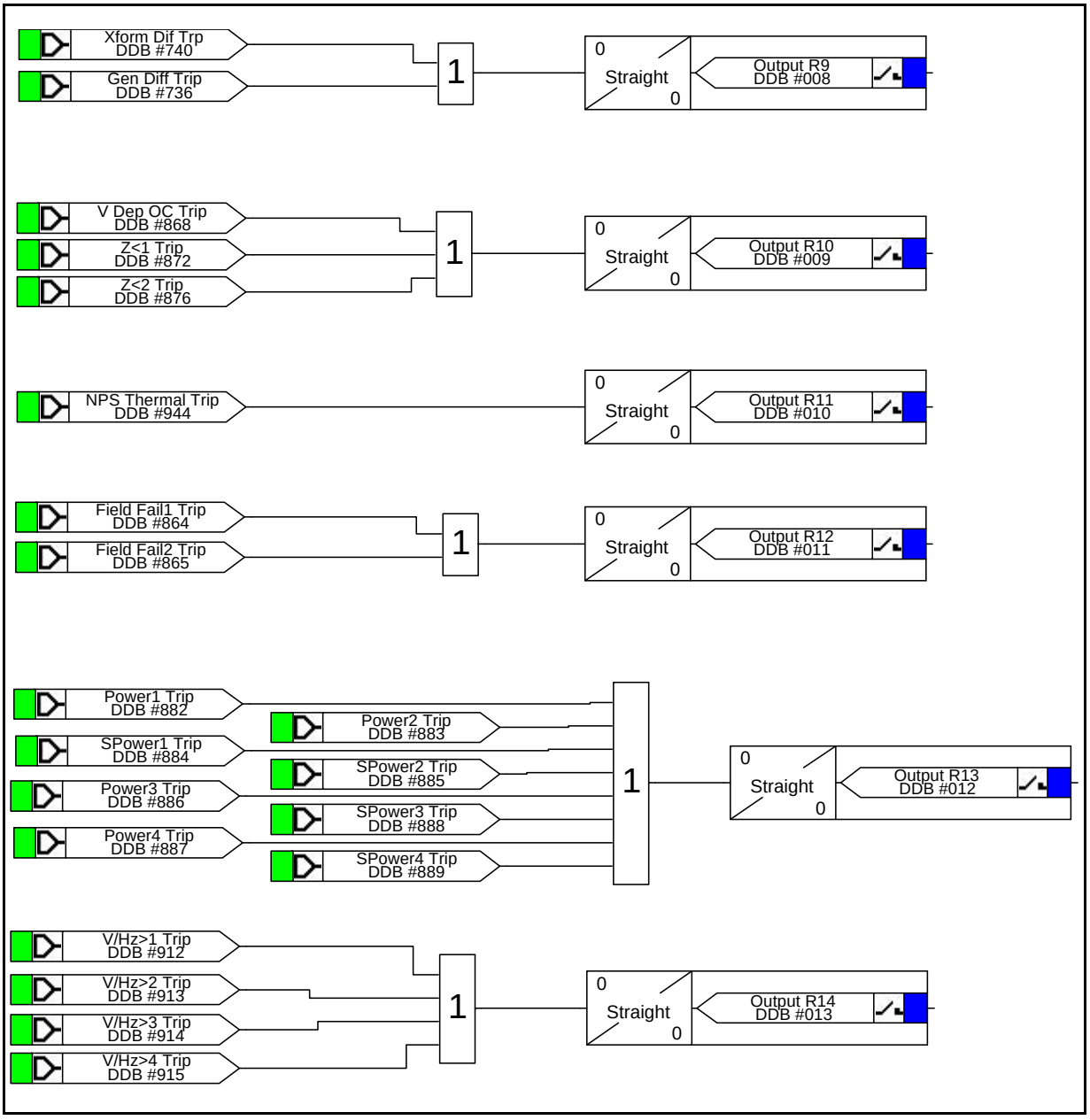


Figure 19: Output relay mappings

PL

PL

3.3 LED Mapping

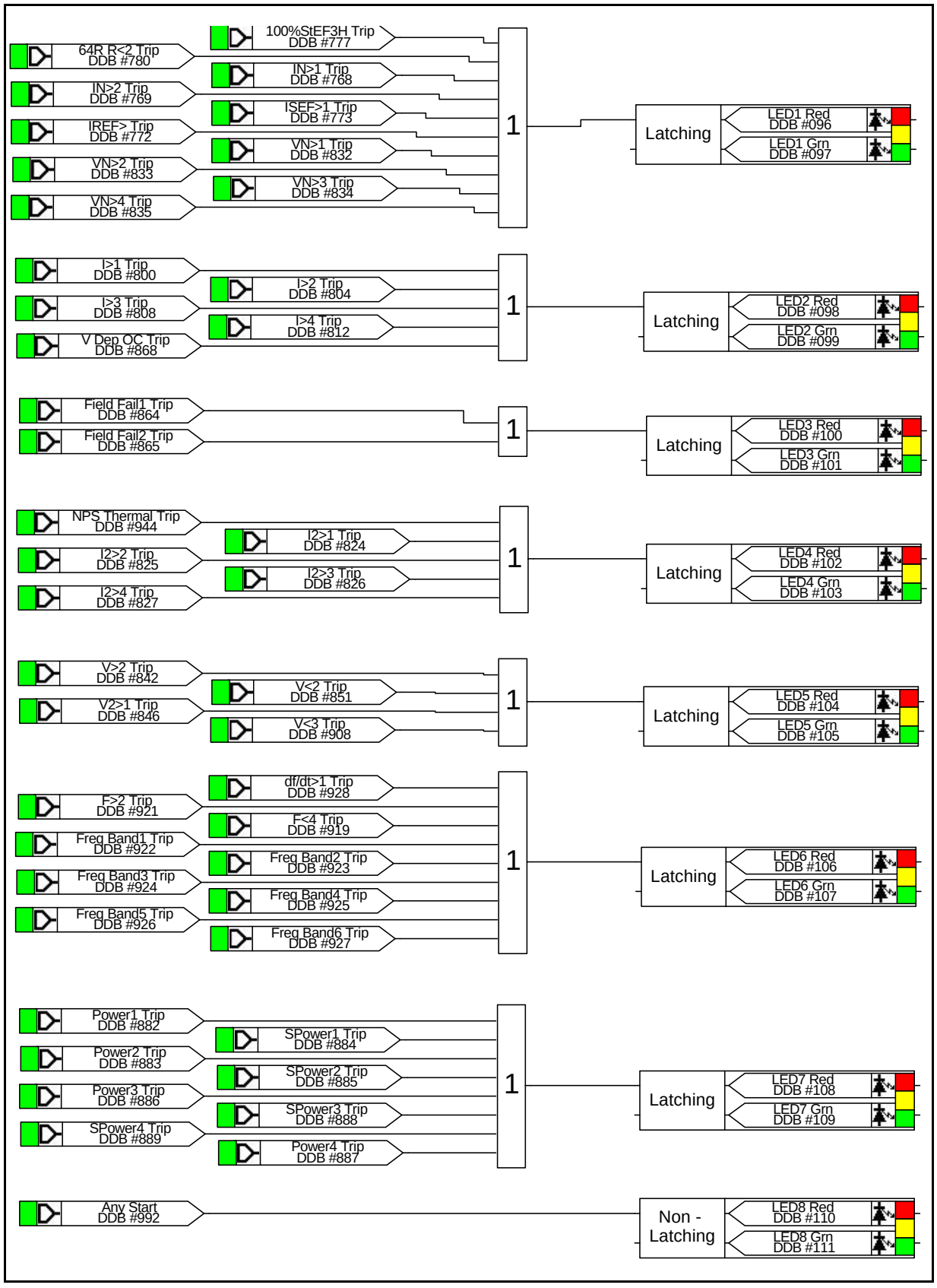


Figure 20: LED output mapping

3.4 Function and LED Mapping

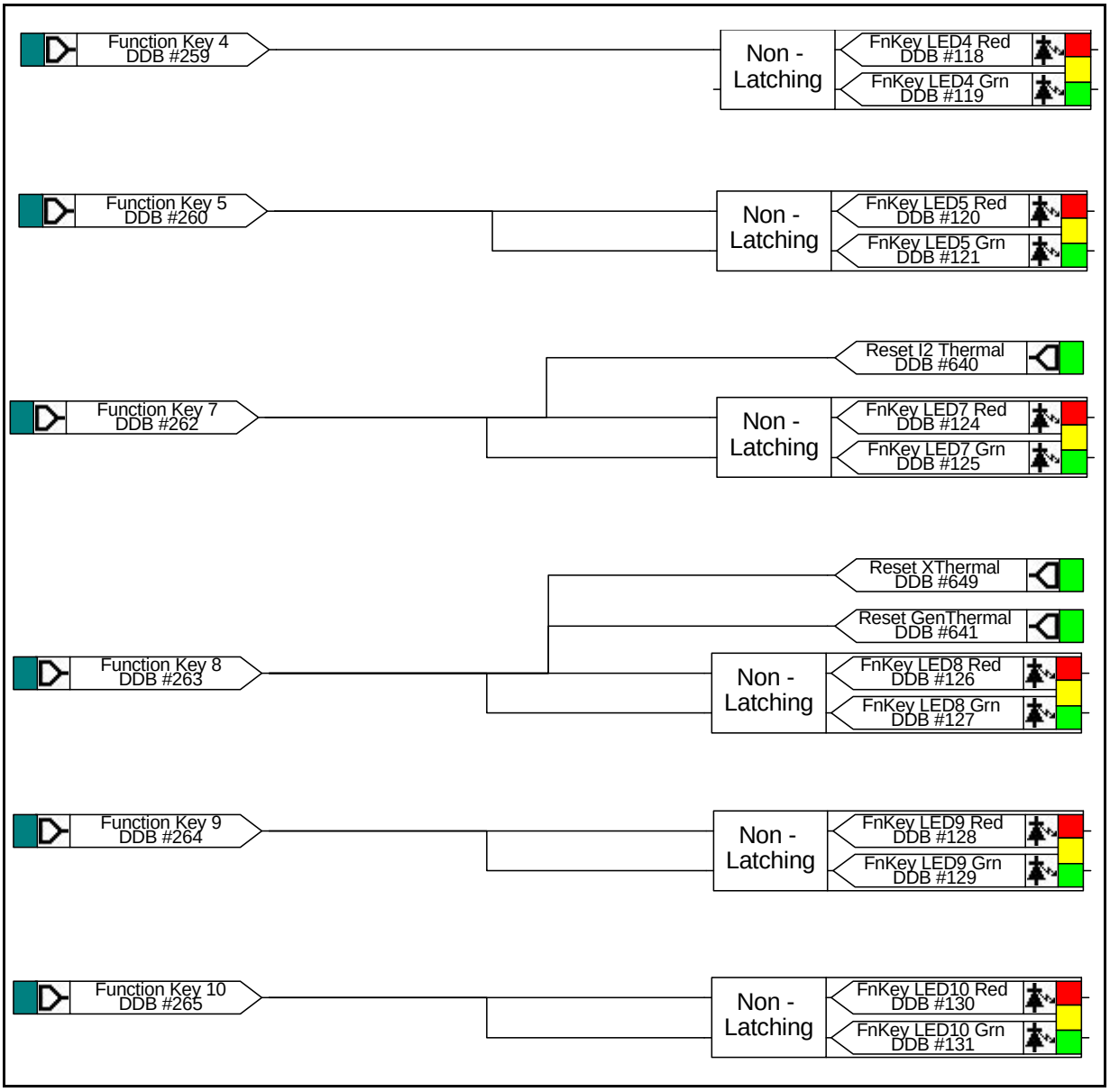


Figure 21: Function key and LED mapping

PL

3.5 Check Synch Mapping

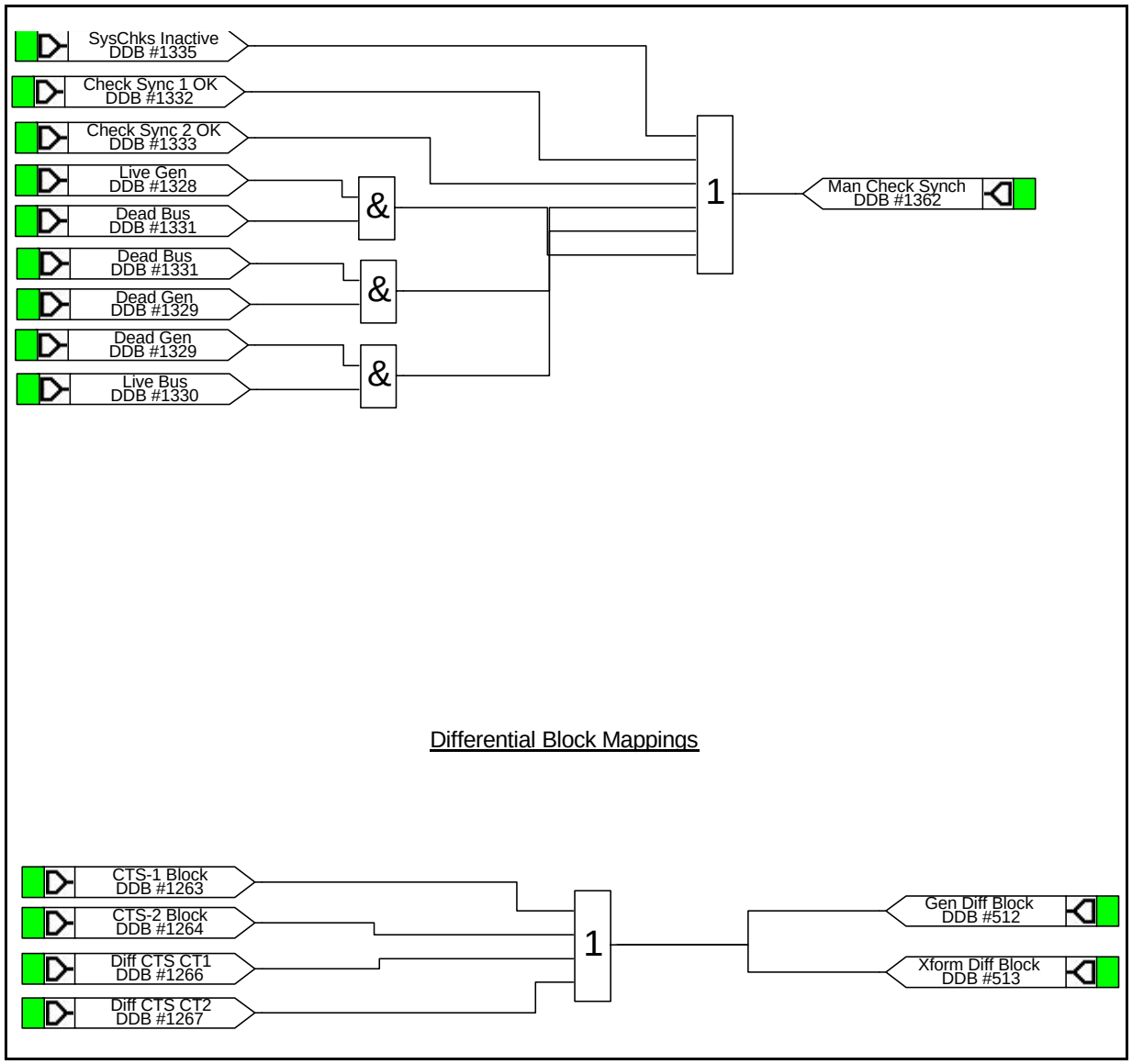


Figure 22: Check synch & voltage monitor mapping

PL

4 P344 PROGRAMMABLE SCHEME LOGIC

4.1 Input Mappings

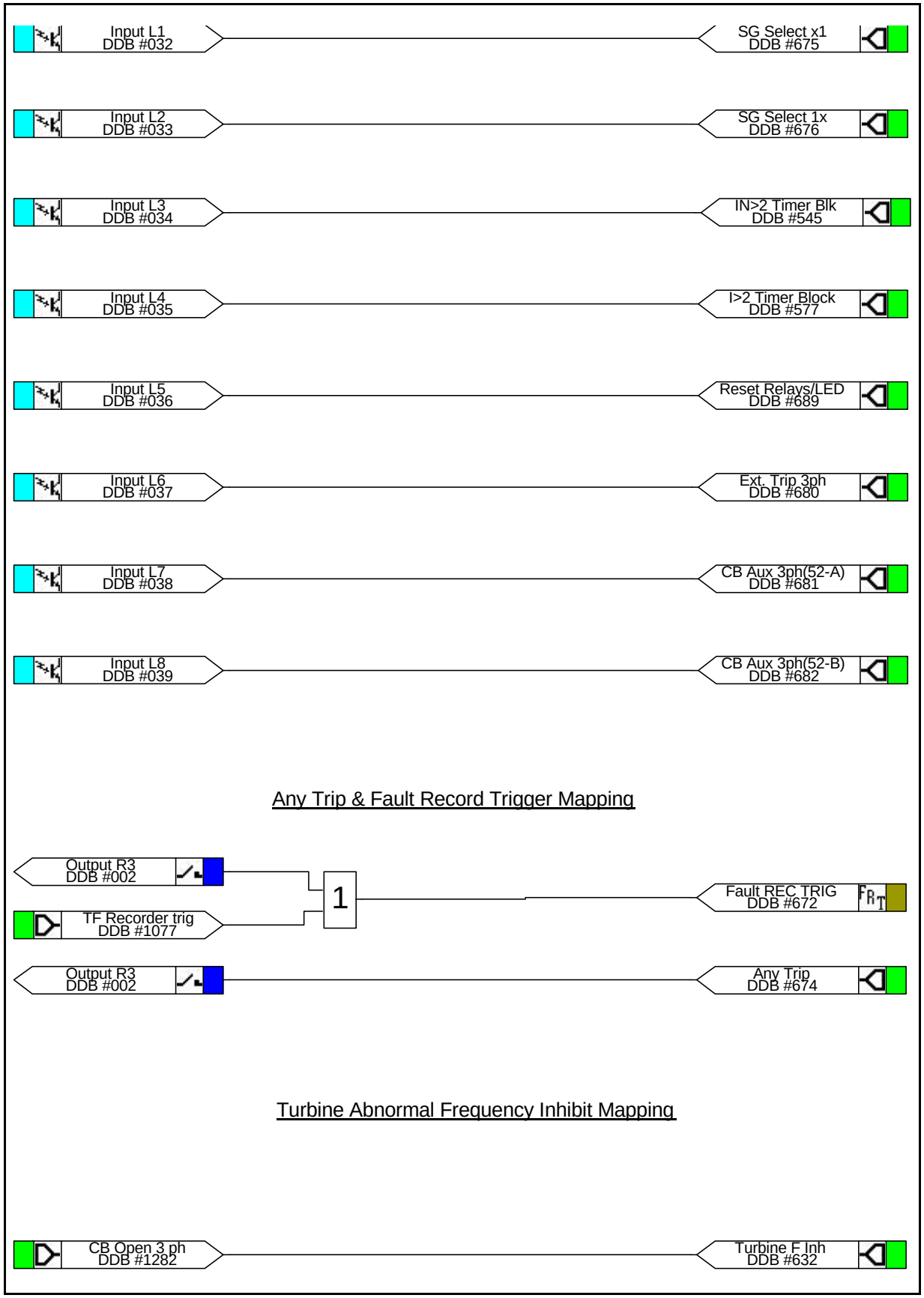


Figure 23: Opto input mappings

PL

4.2 Output Mappings

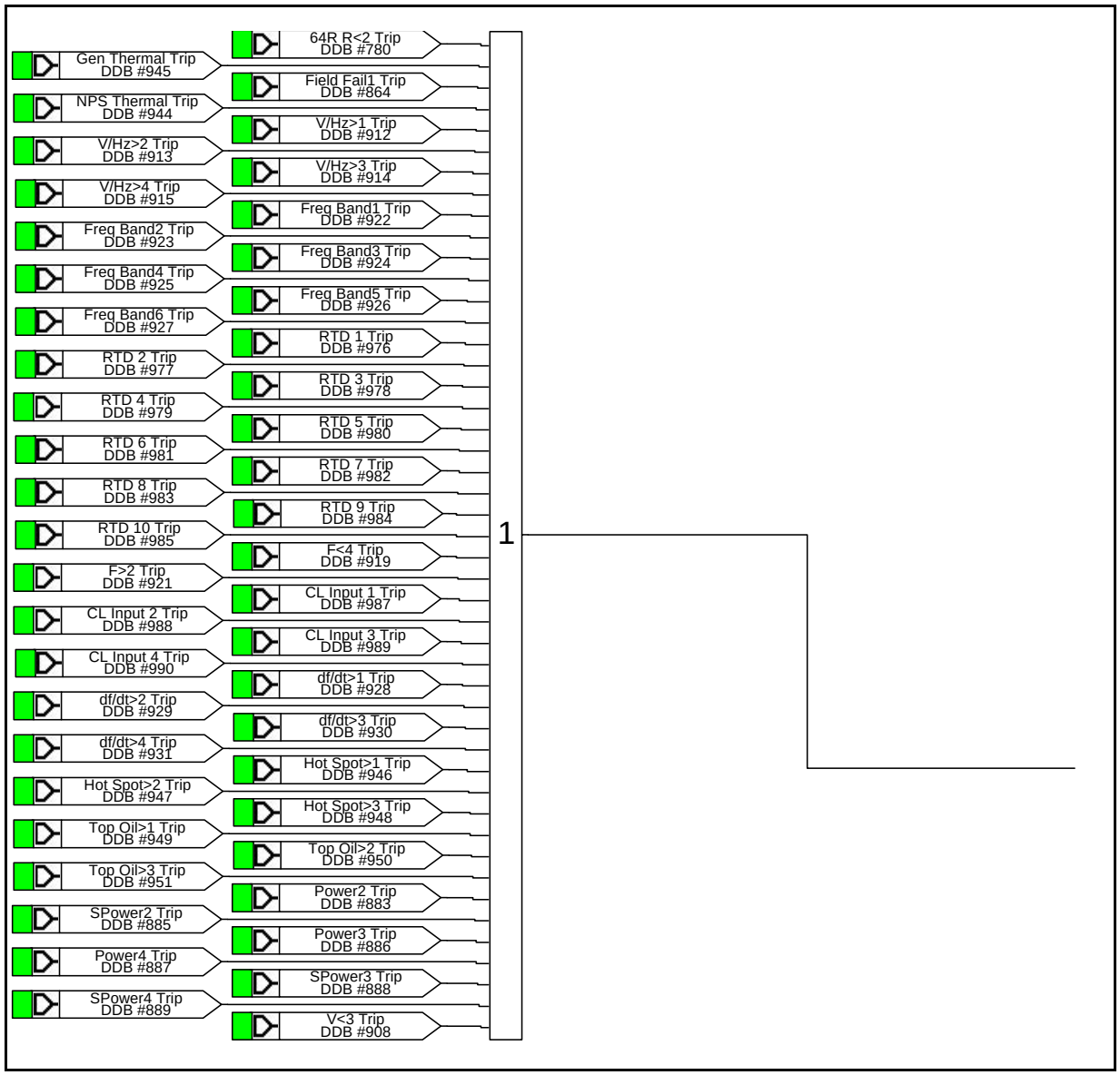


Figure 24: Output relay R1 (Trip CB) mappings

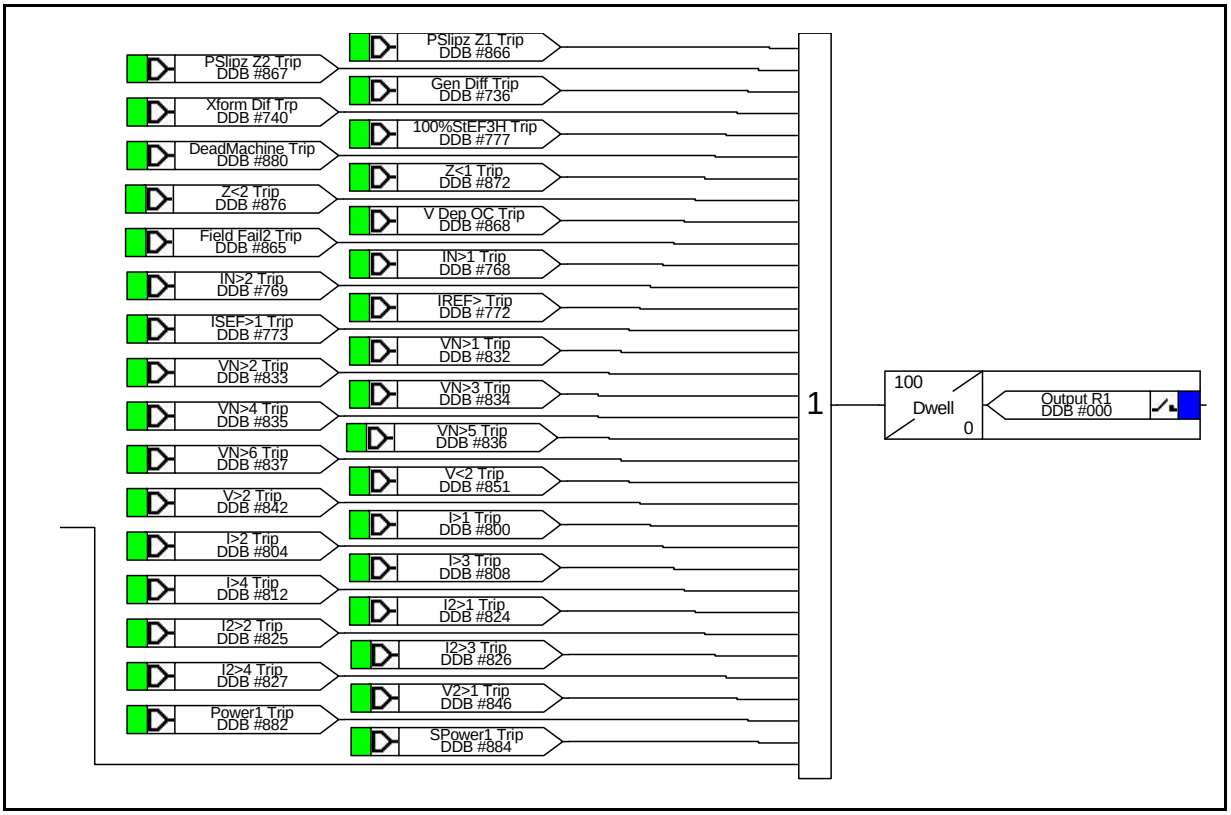


Figure 25: Output relay R1 (Trip CB) mappings

PL

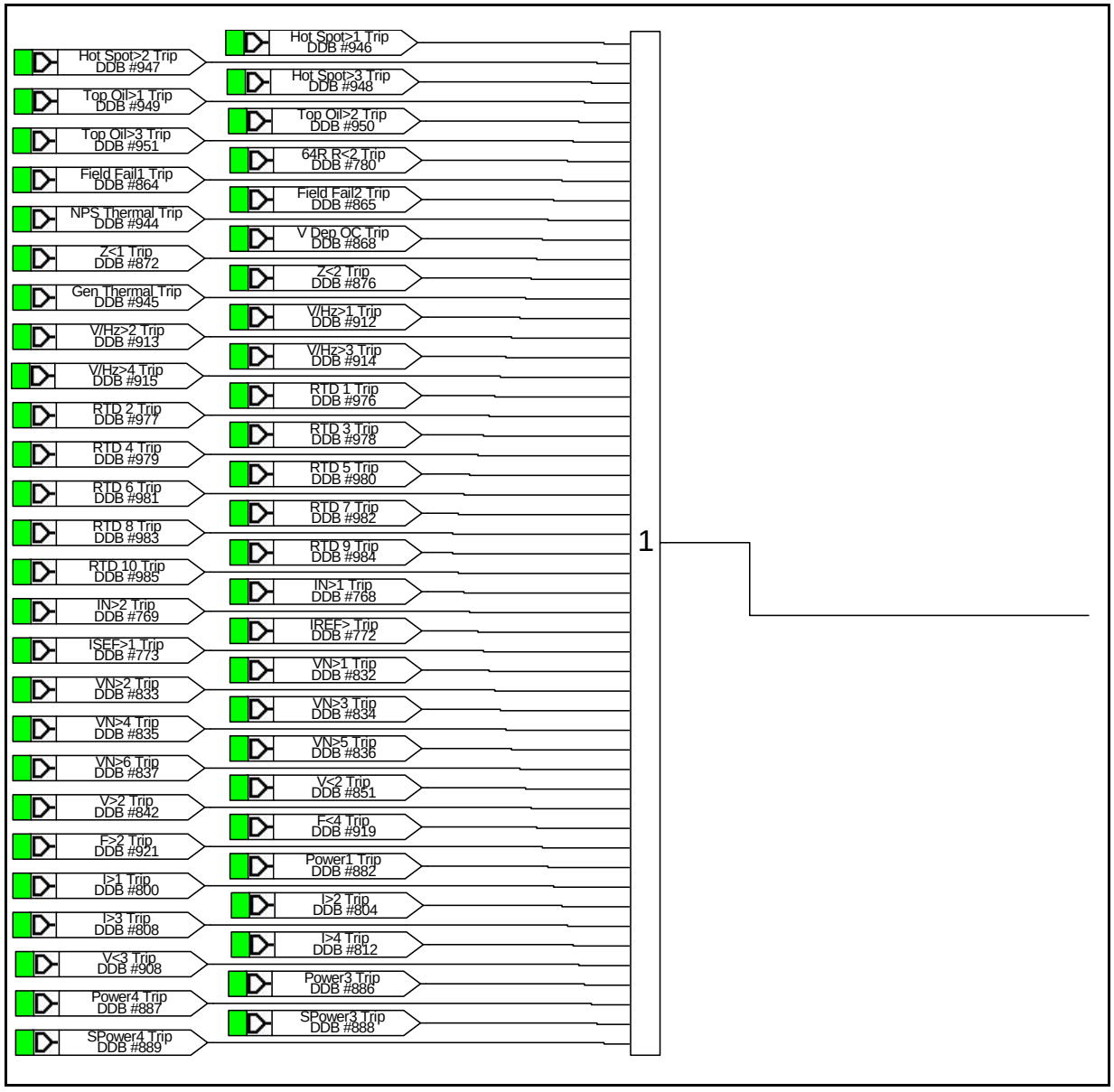


Figure 26: Output relay R2 (Trip Prime Mover) mappings

PL

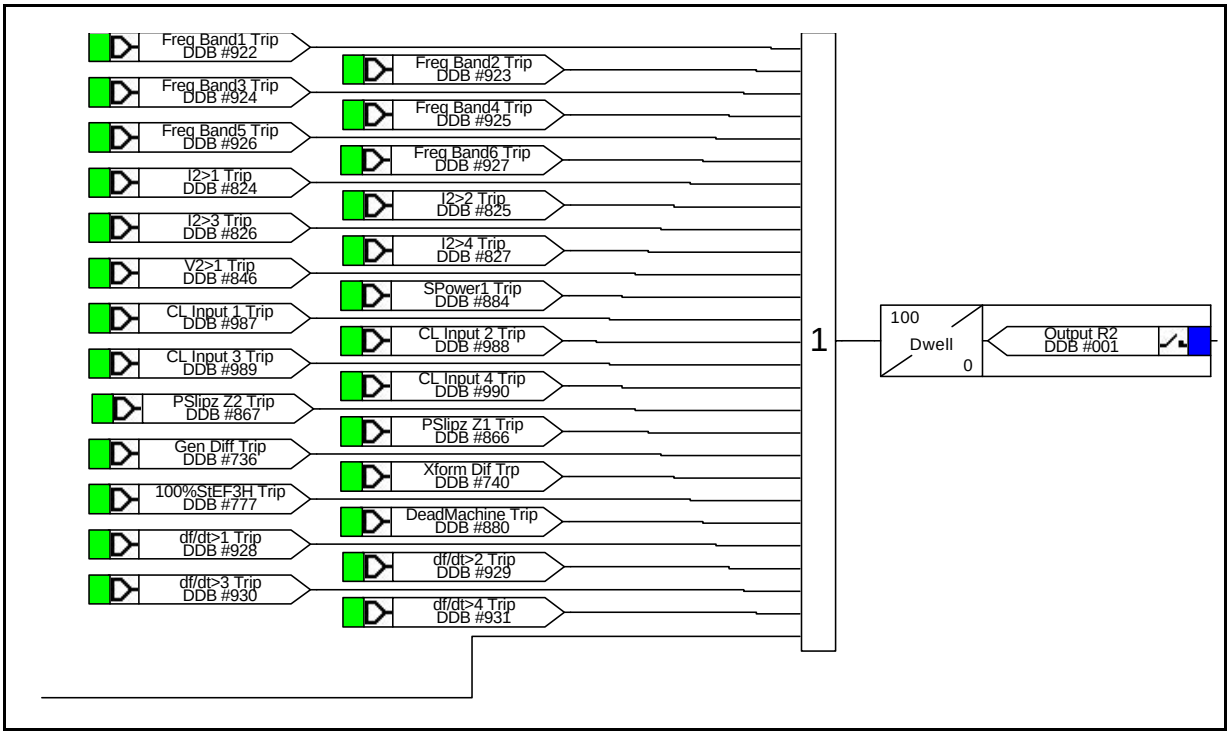


Figure 27: Output relay R2 (Trip Prime Mover) mappings

PL

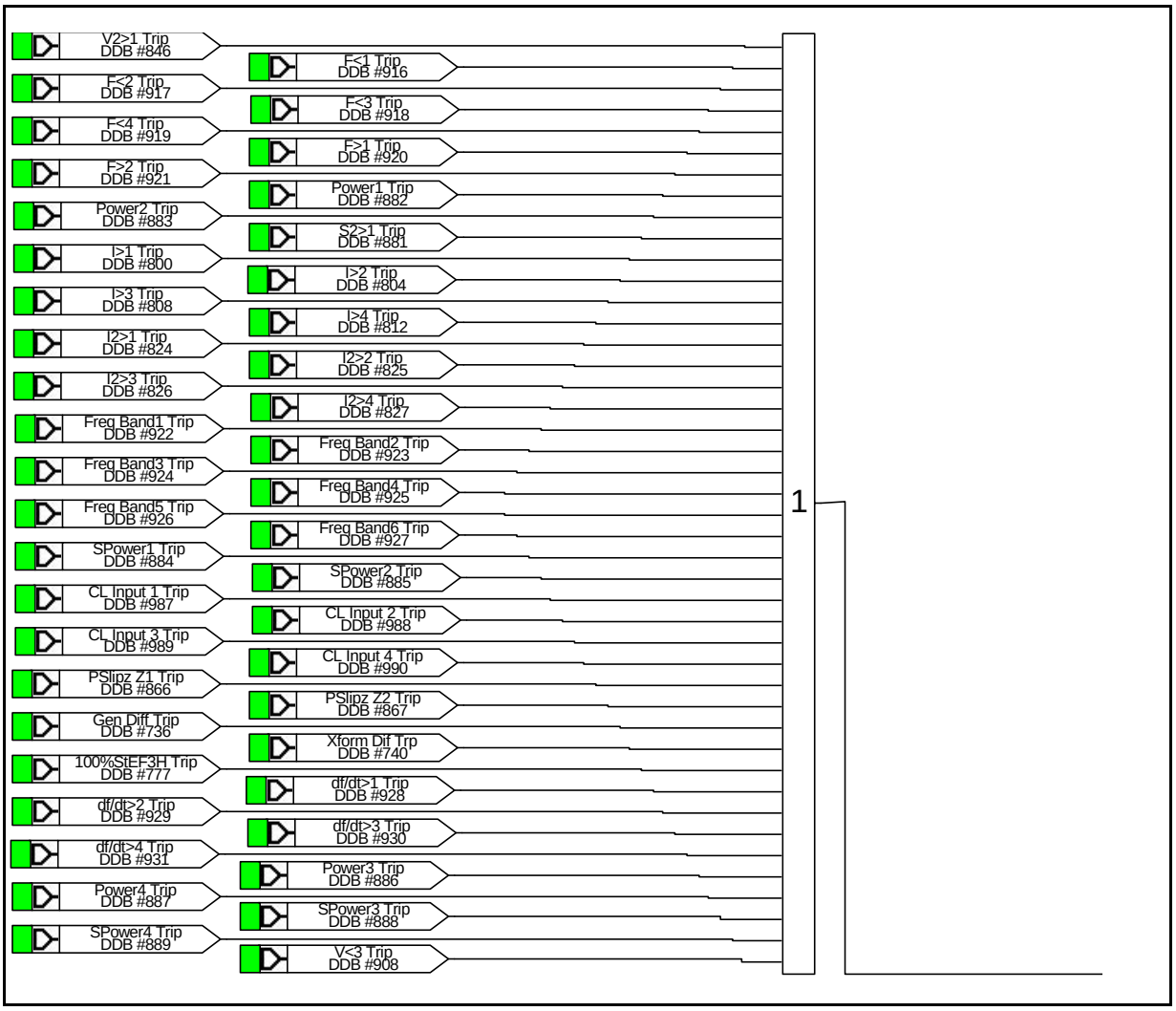


Figure 28: Output relay R3 (Any Trip) mappings

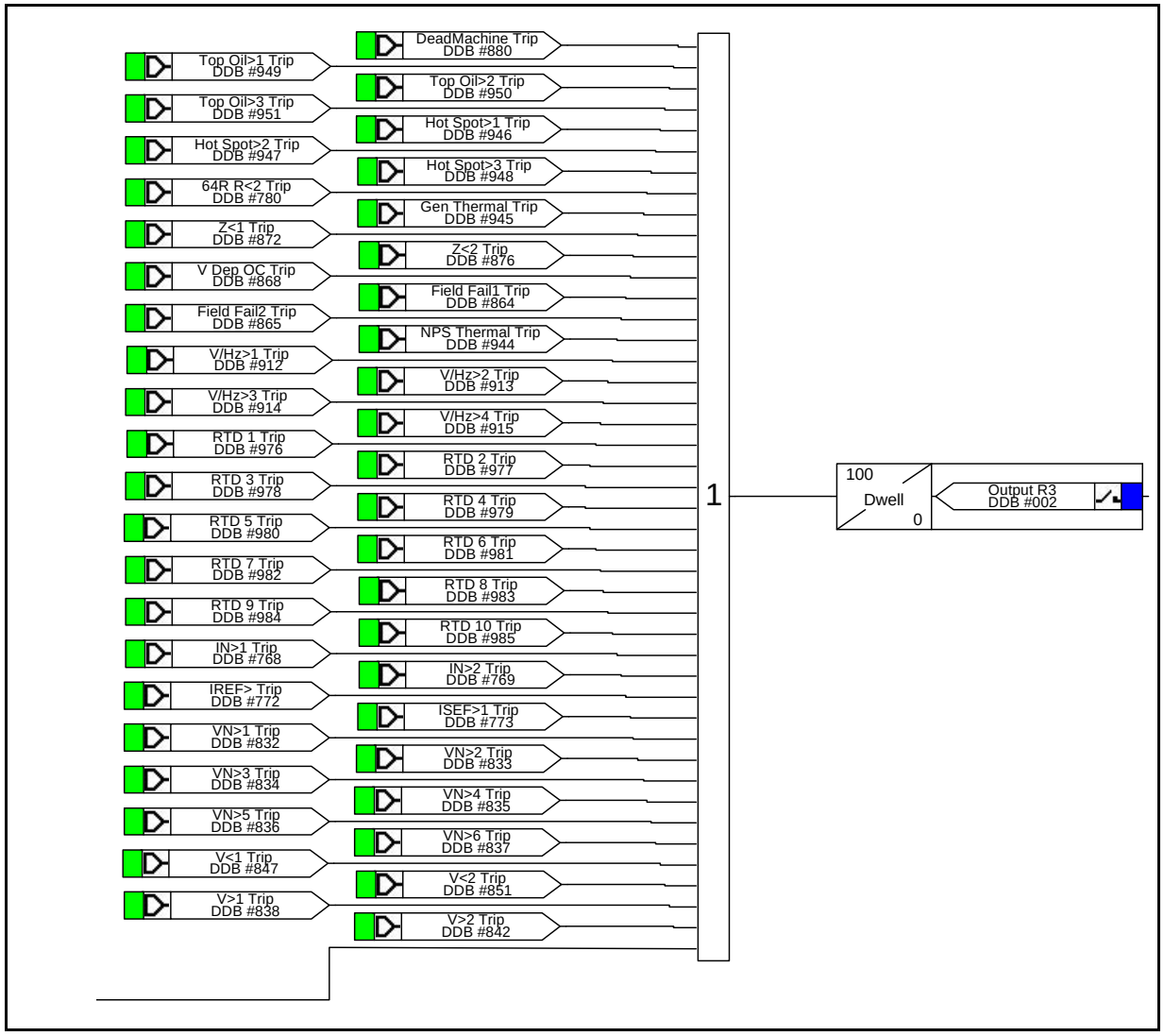


Figure 29: Output relay R3 (Any Trip) mappings

PL

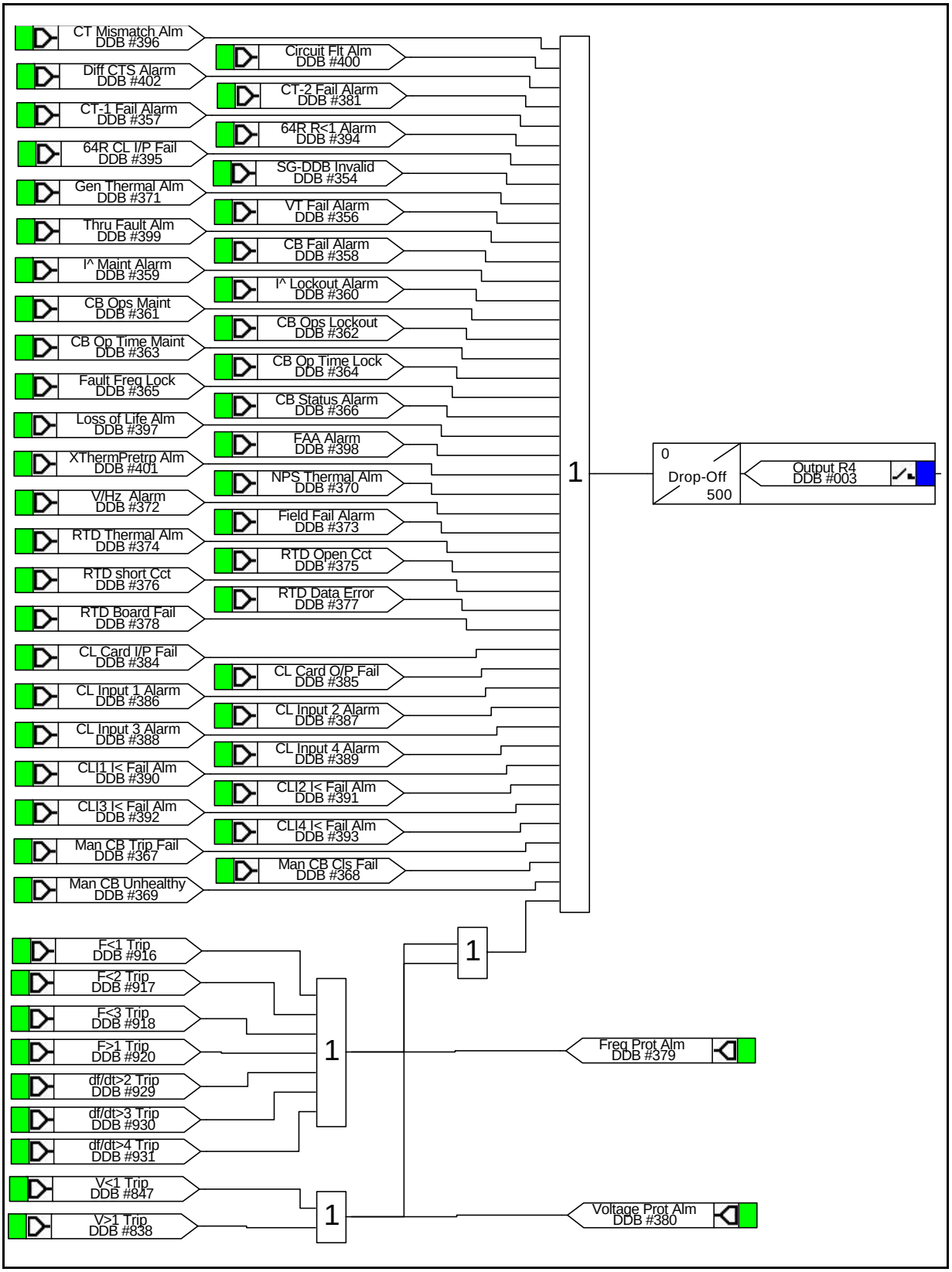


Figure 30: Output relay R4 (General Alarm) mappings

PL

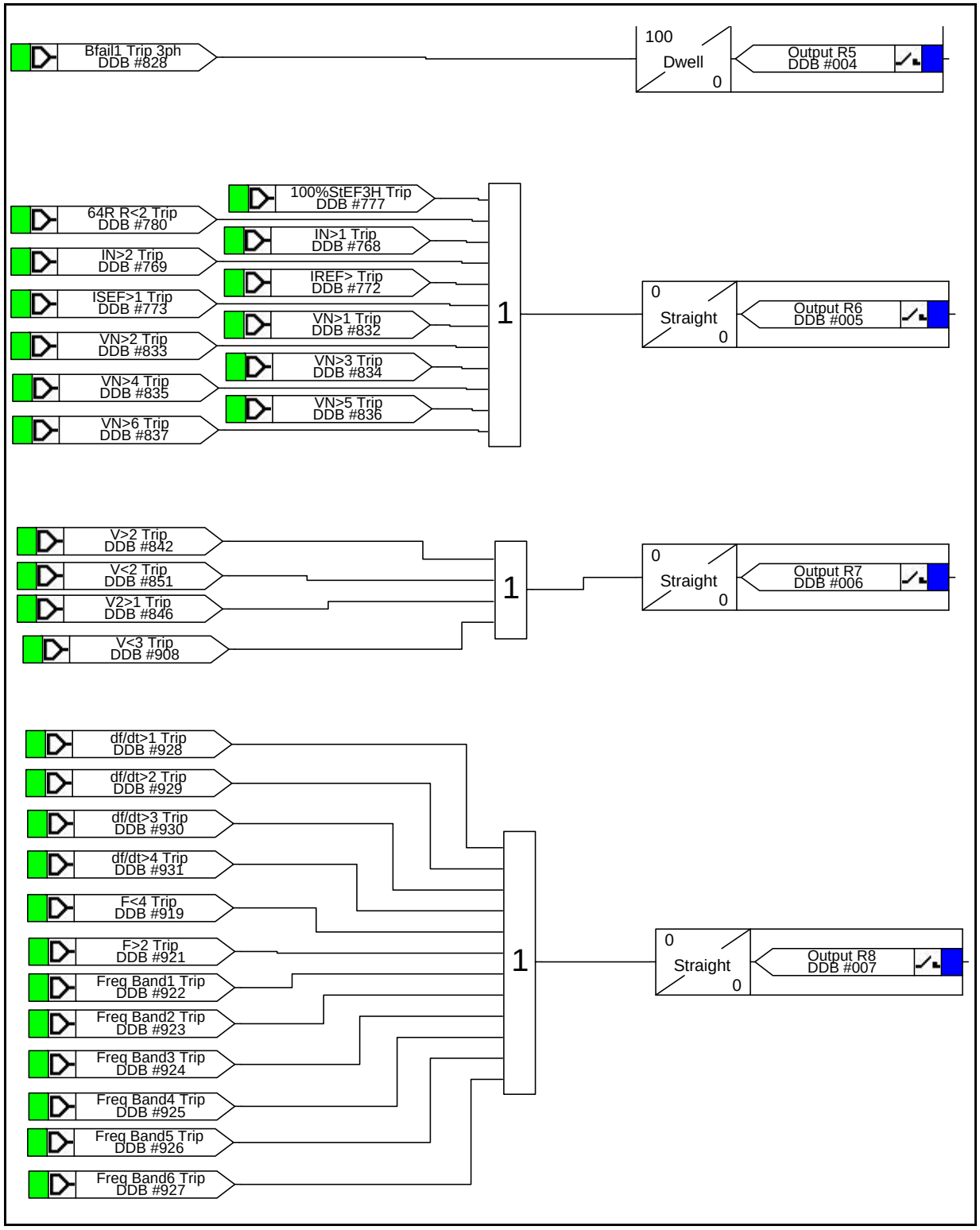


Figure 31: Output relay mappings

PL

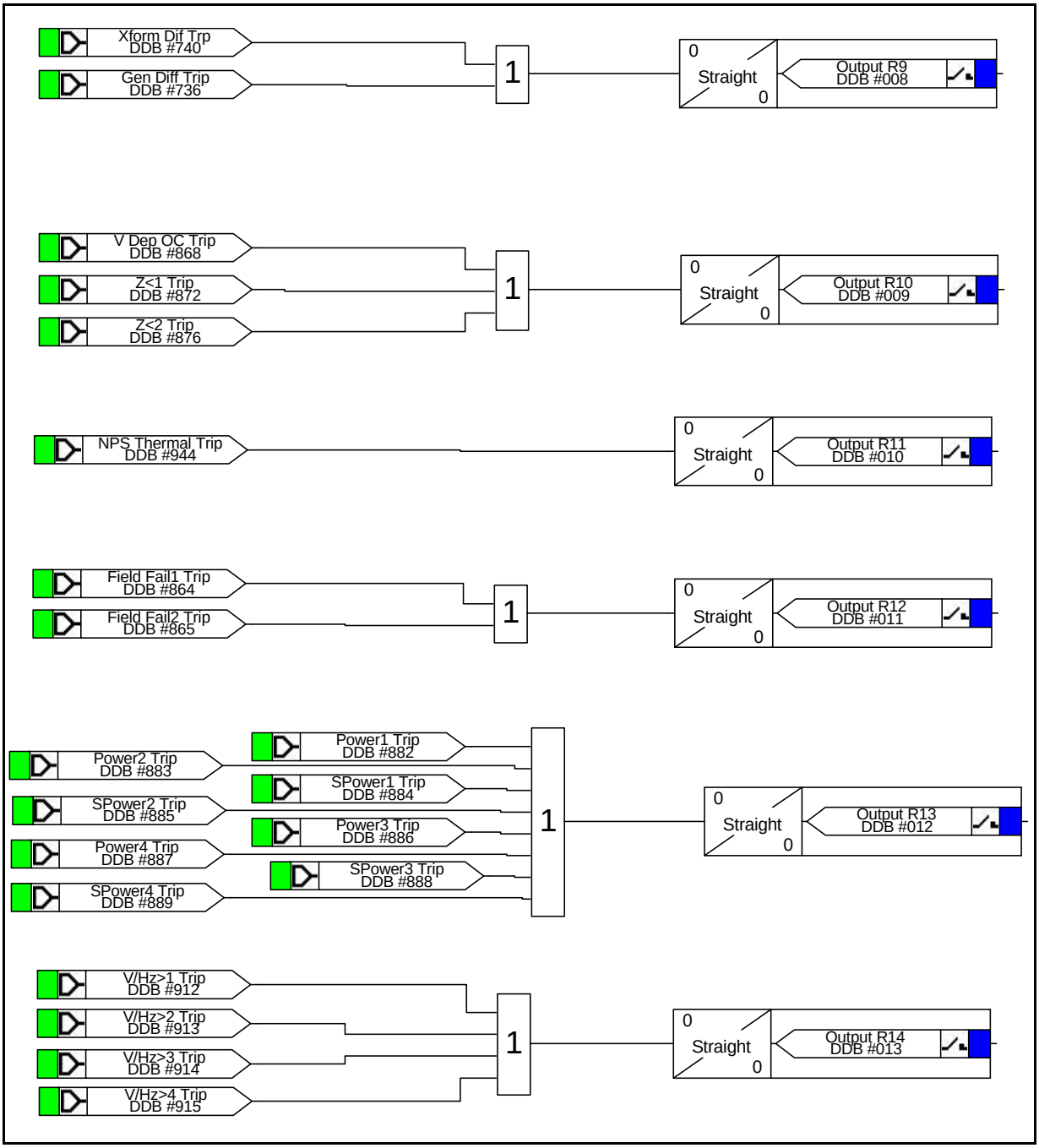


Figure 32: Output relay mappings

PL

4.3 Function and LED Mapping

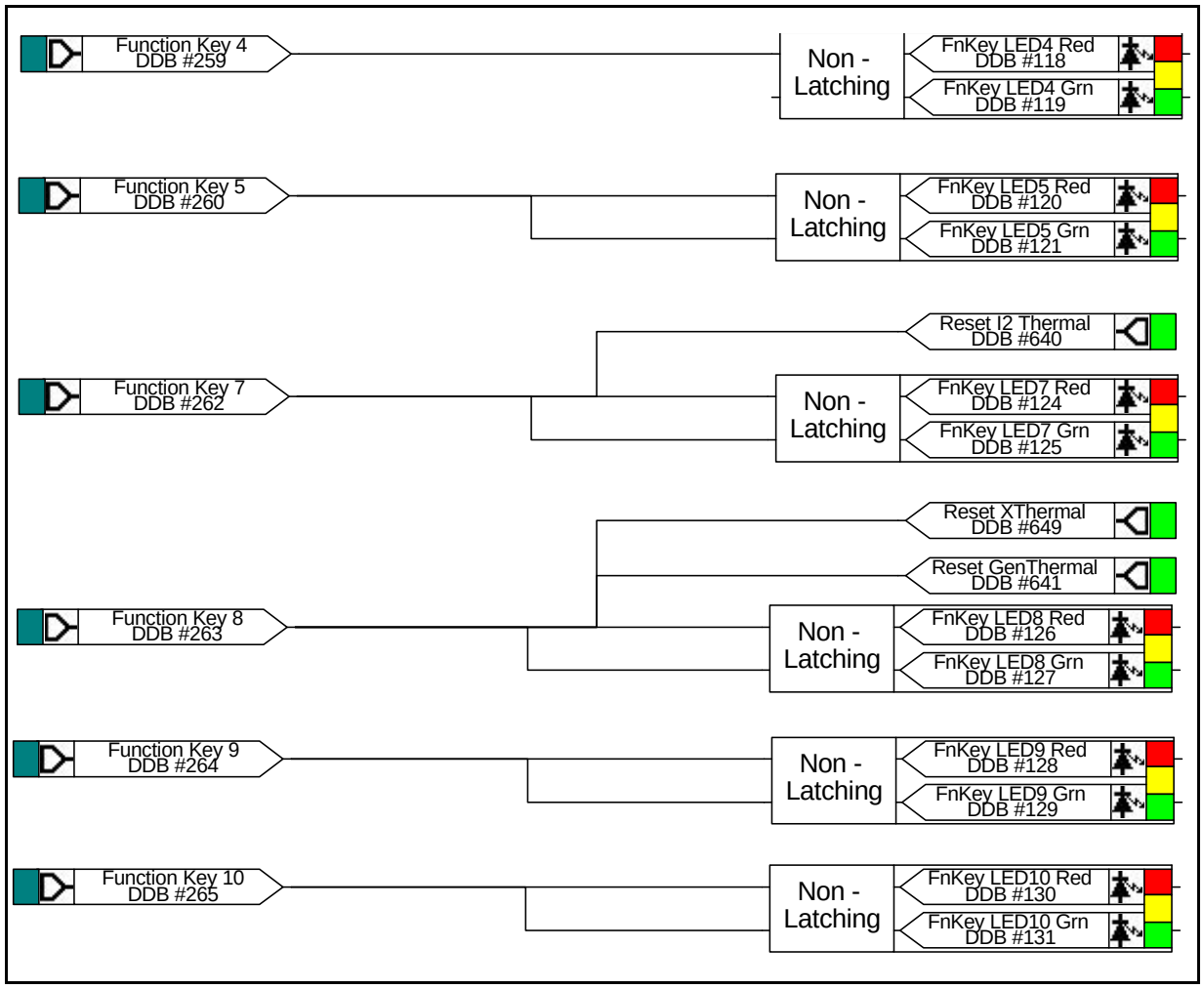


Figure 33: Function key and function LED mapping

PL

4.4 LED Mapping

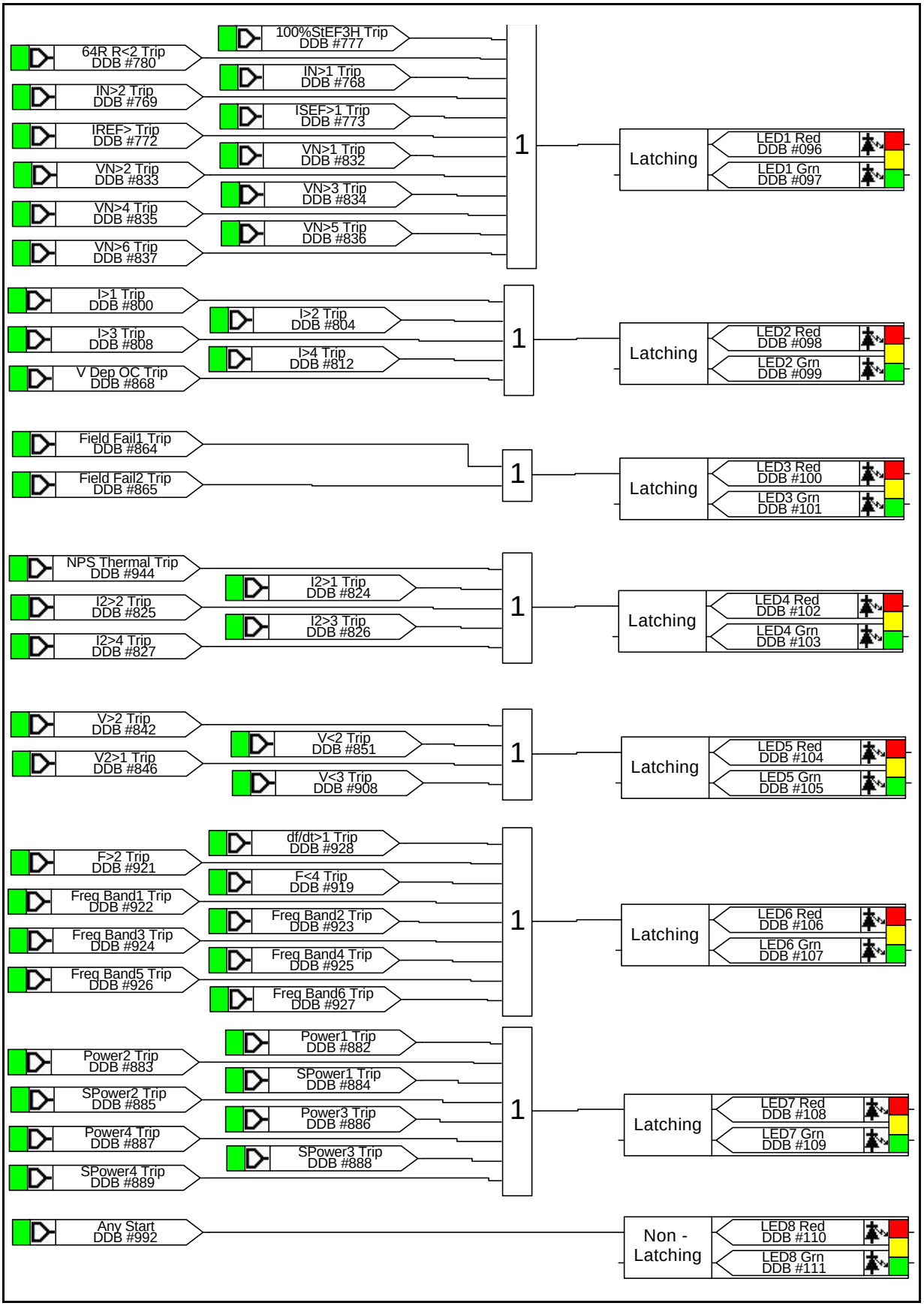


Figure 34: LED output mapping

4.5 Check Synch Mapping

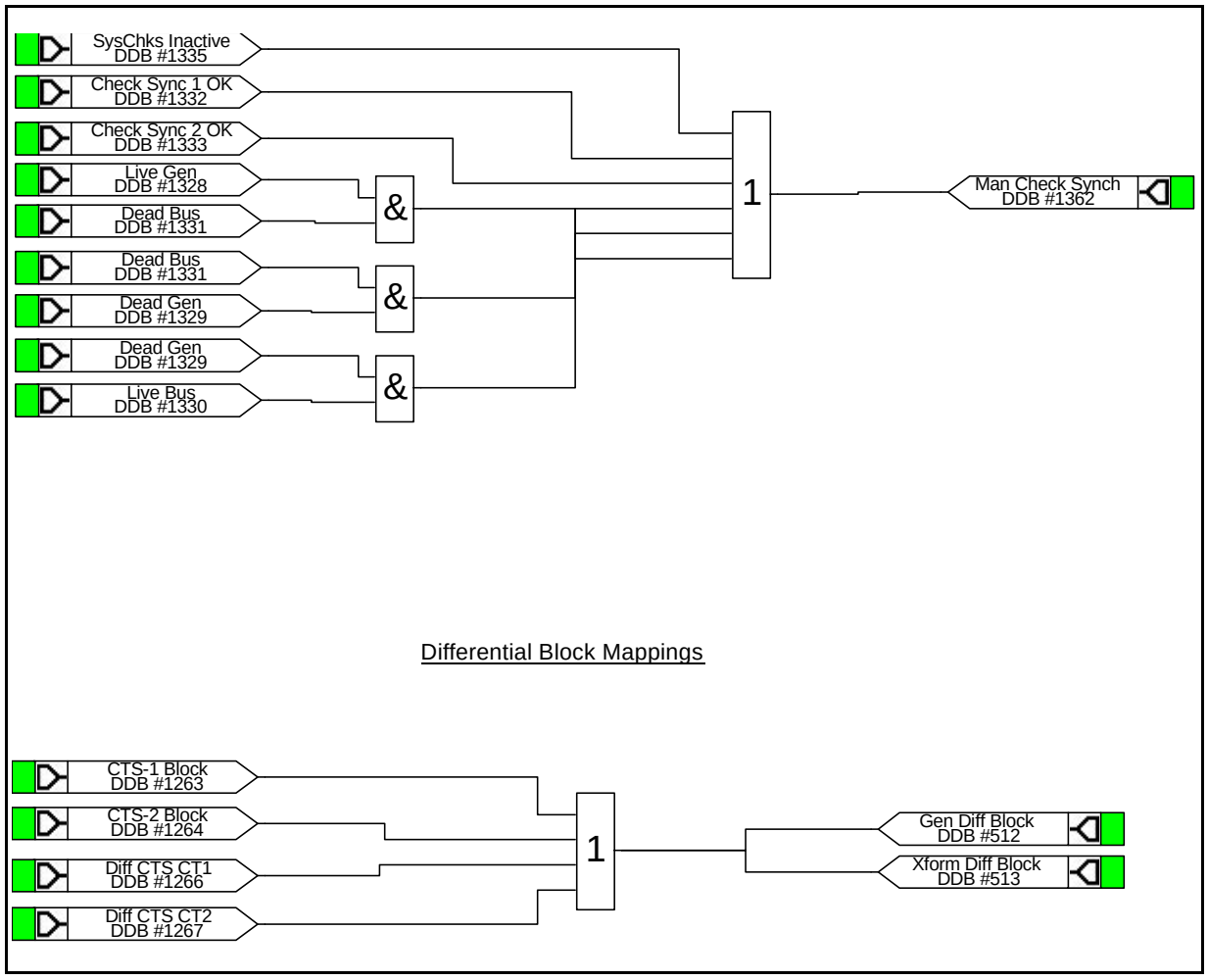


Figure 35: Check synch & voltage monitor mapping

PL

5 P345 PROGRAMMABLE SCHEME LOGIC

5.1 Input Mappings

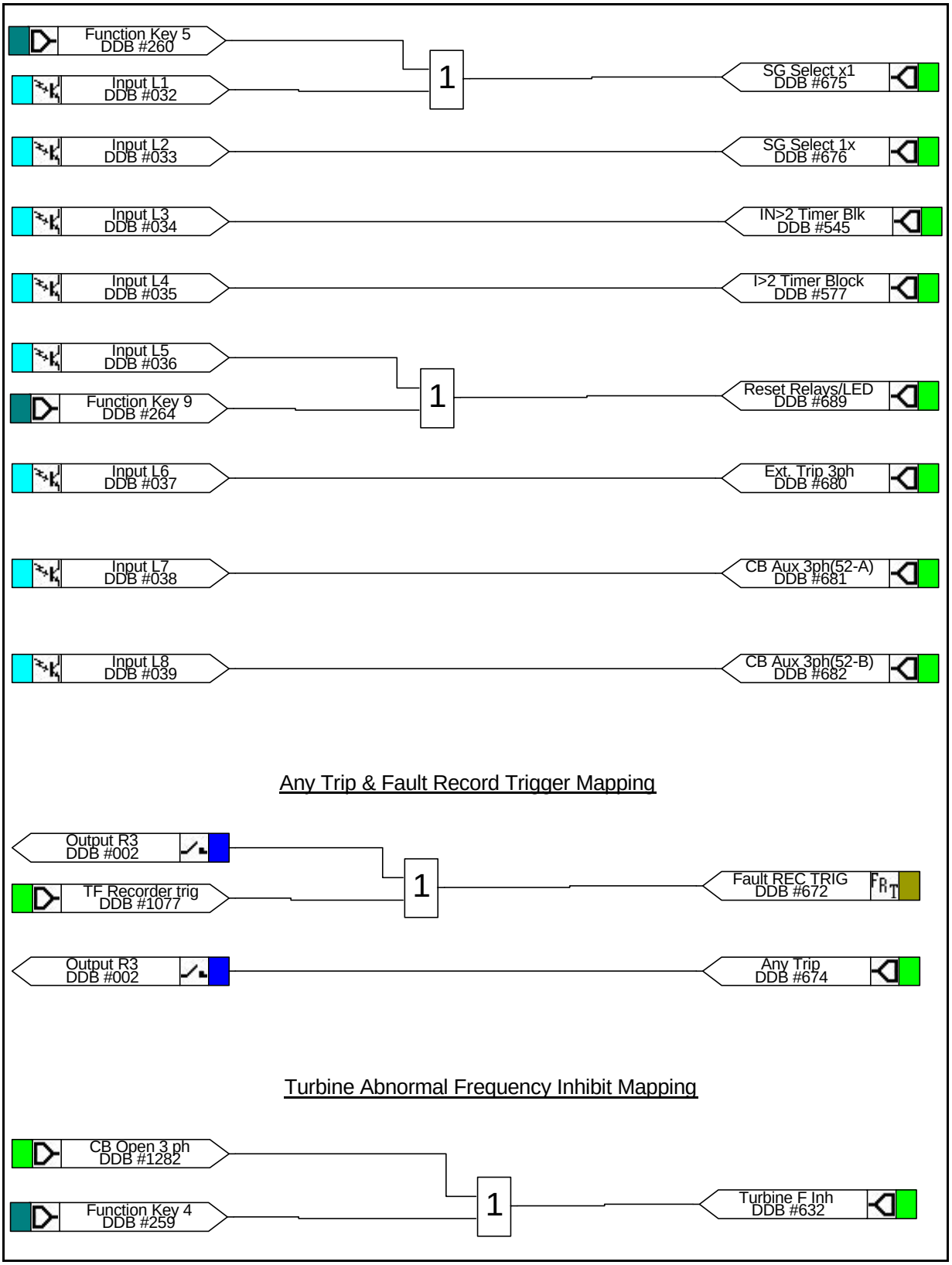


Figure 36: Opto input mappings

PL

5.2 Output Mappings

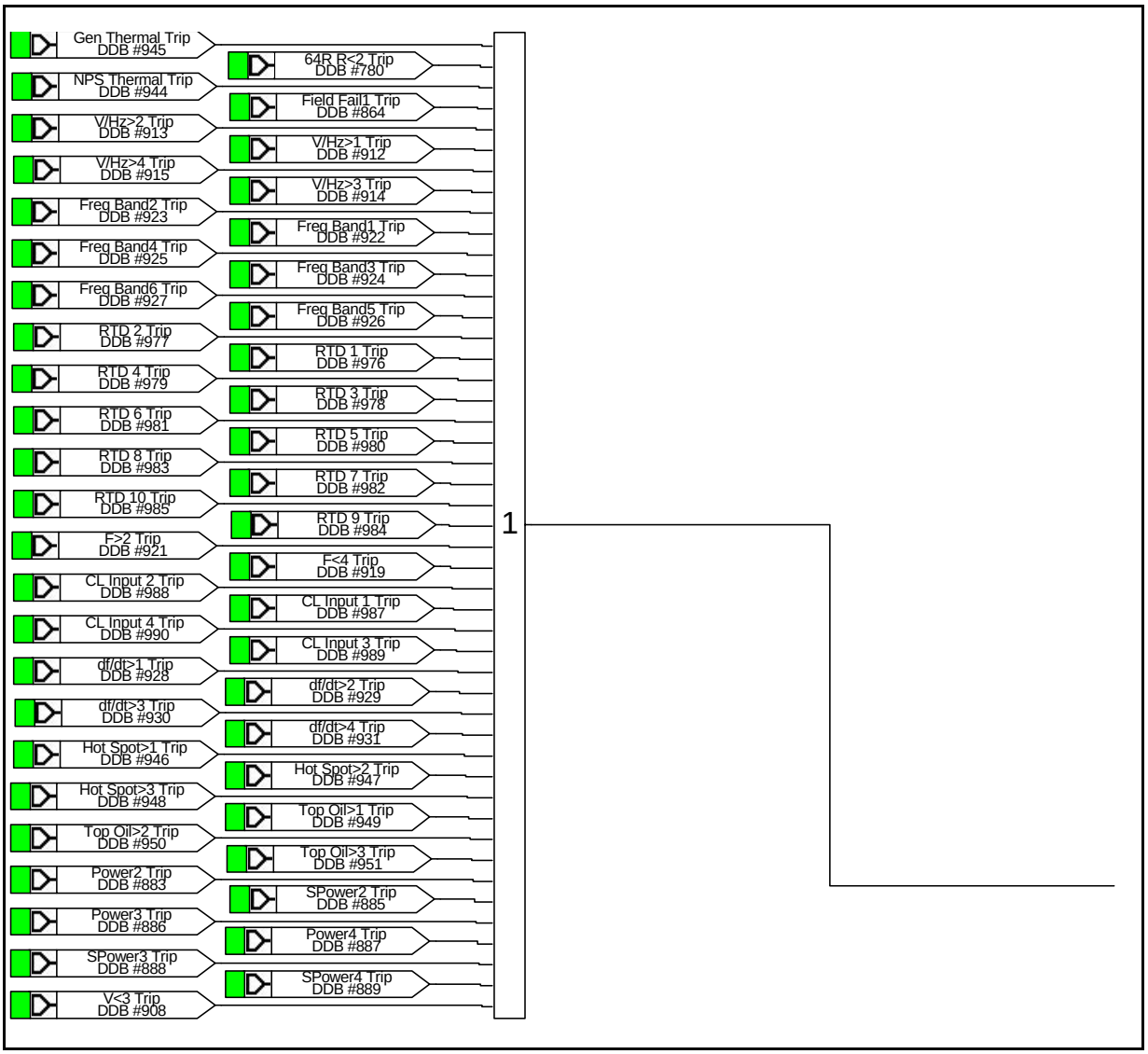


Figure 37: Output relay R1 (Trip CB) mappings

PL

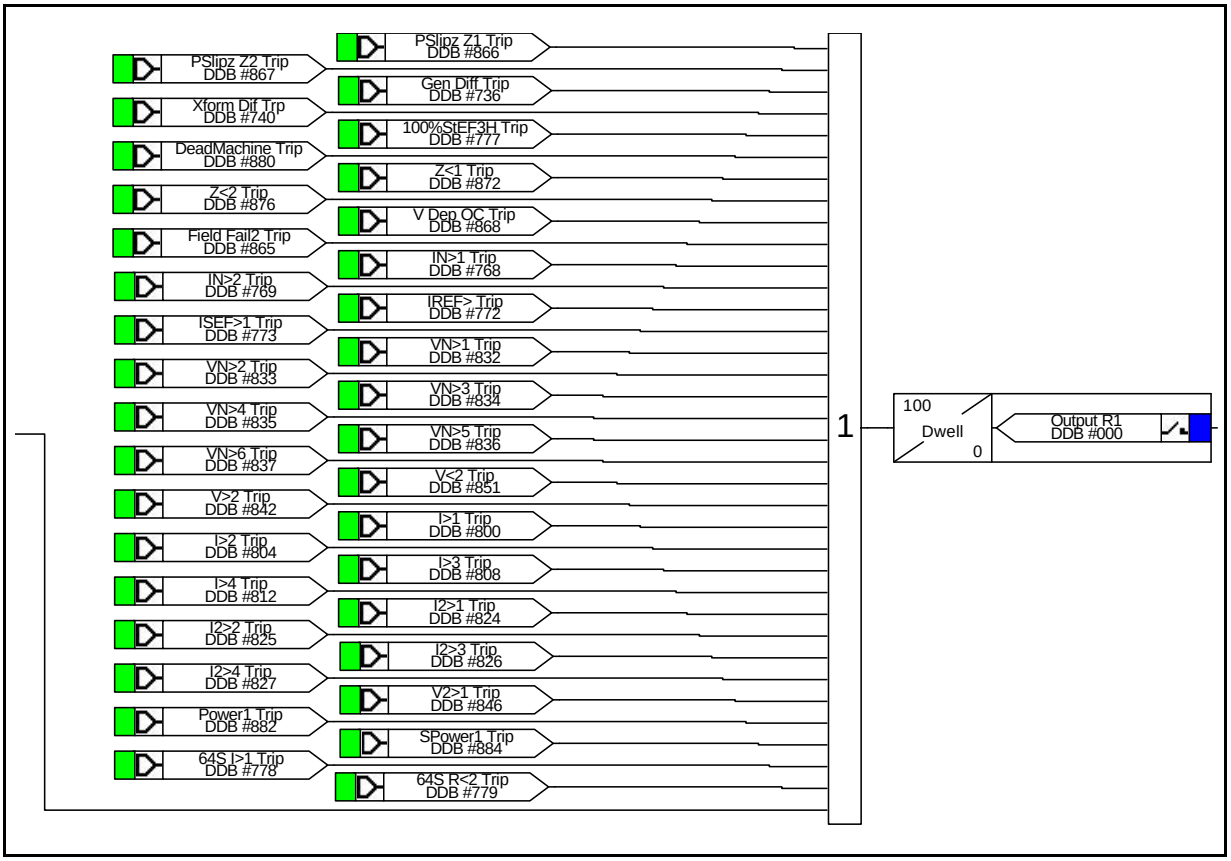


Figure 38: Output relay R1 (Trip CB) mappings

PL

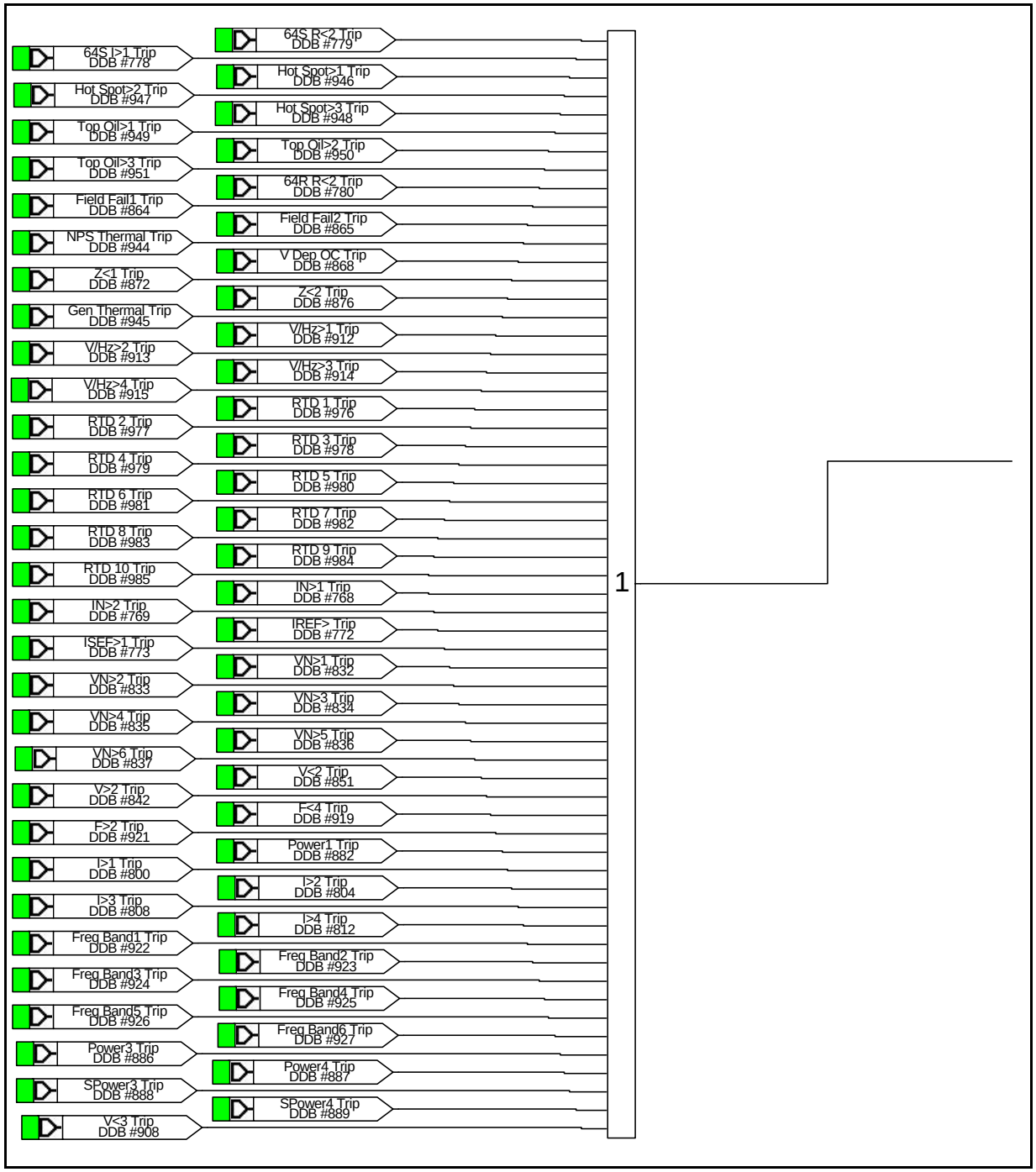


Figure 39: Output relay R2 (Trip Prime Mover) mappings

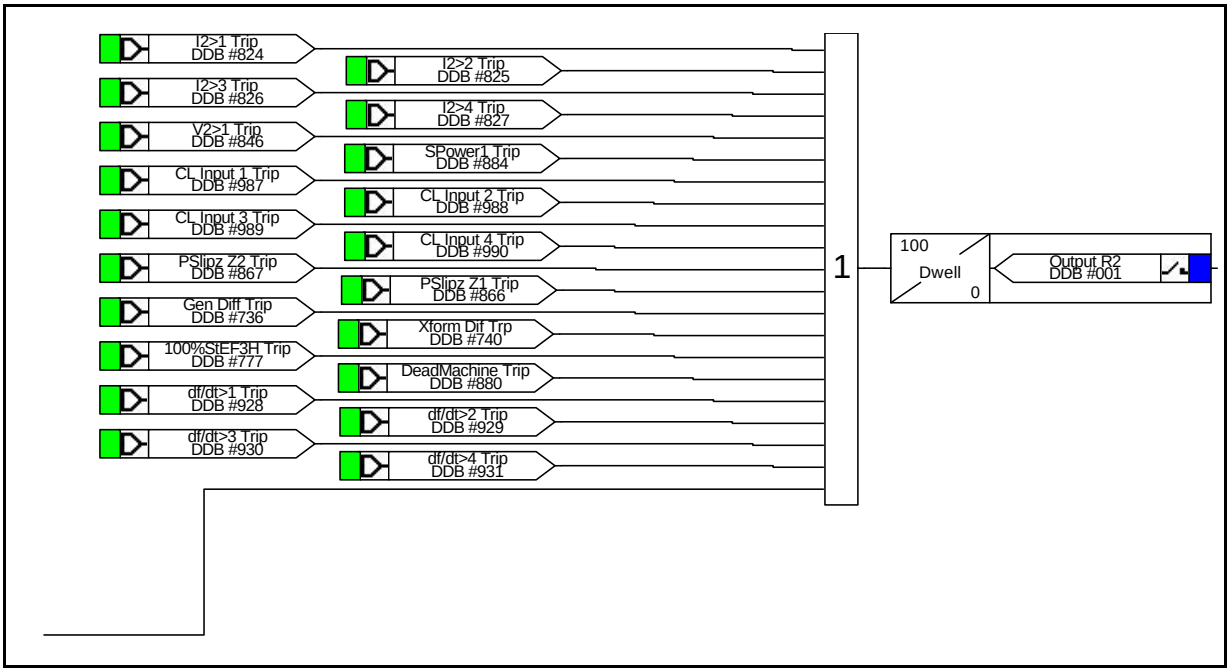


Figure 40: Output relay R2 (Trip Prime Mover) mappings

PL

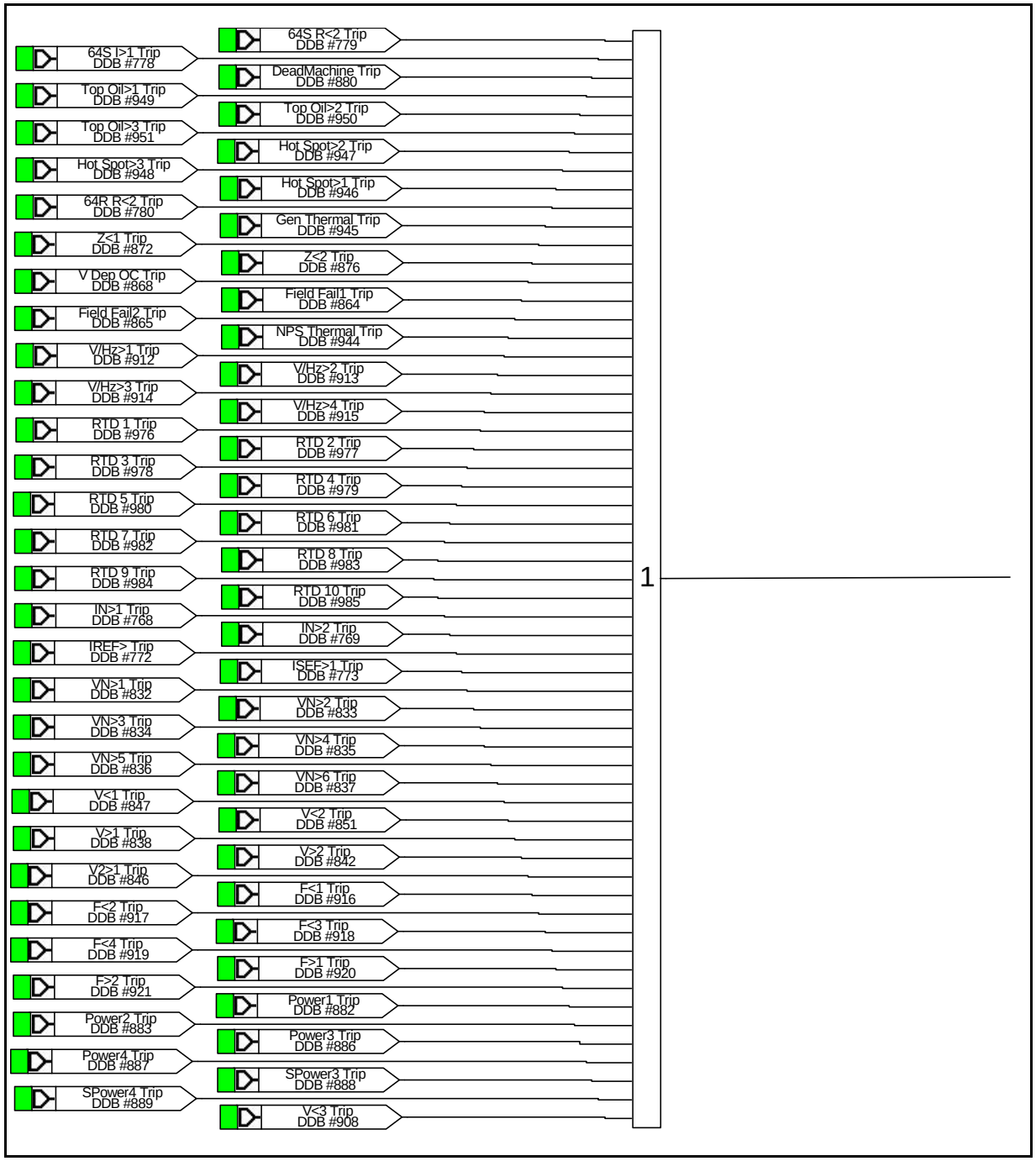


Figure 41: Output relay R3 (Any Trip) mappings

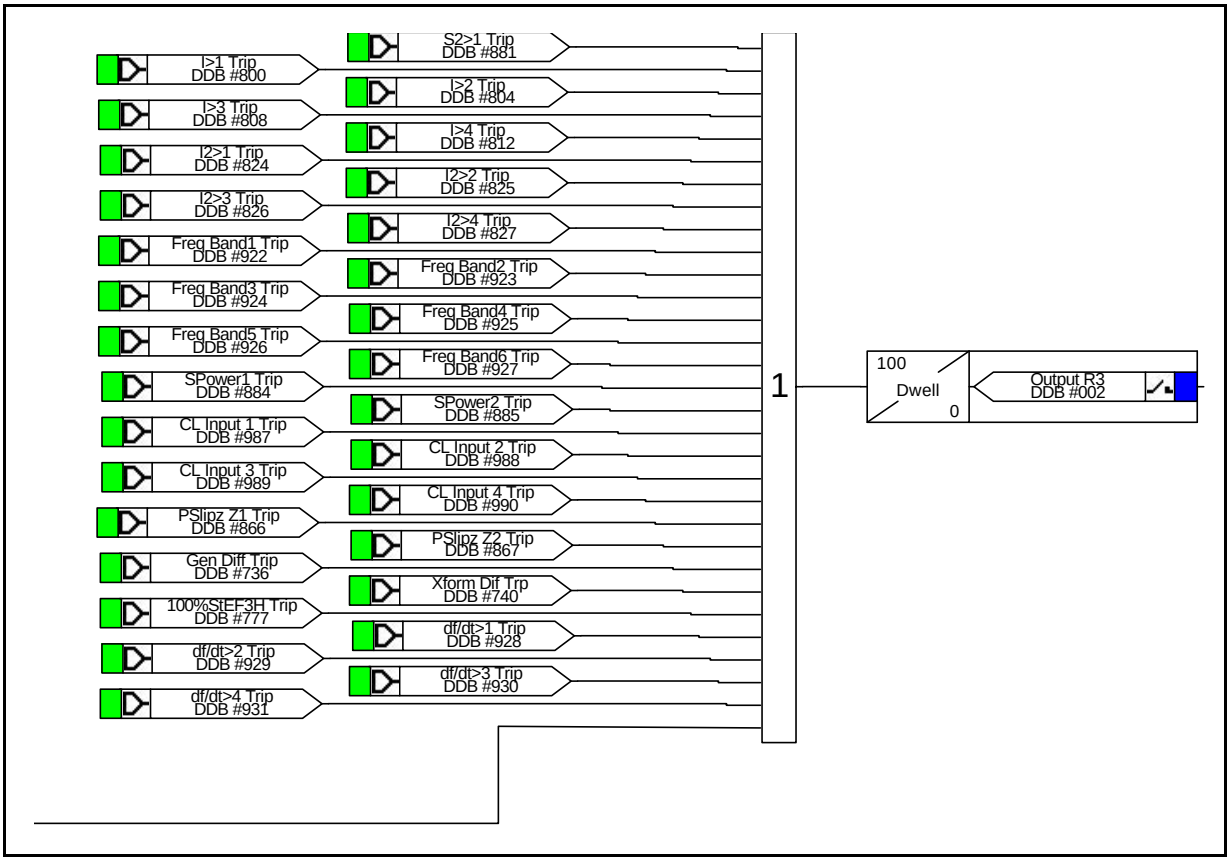


Figure 42: Output relay R3 (Any Trip) mappings

PL

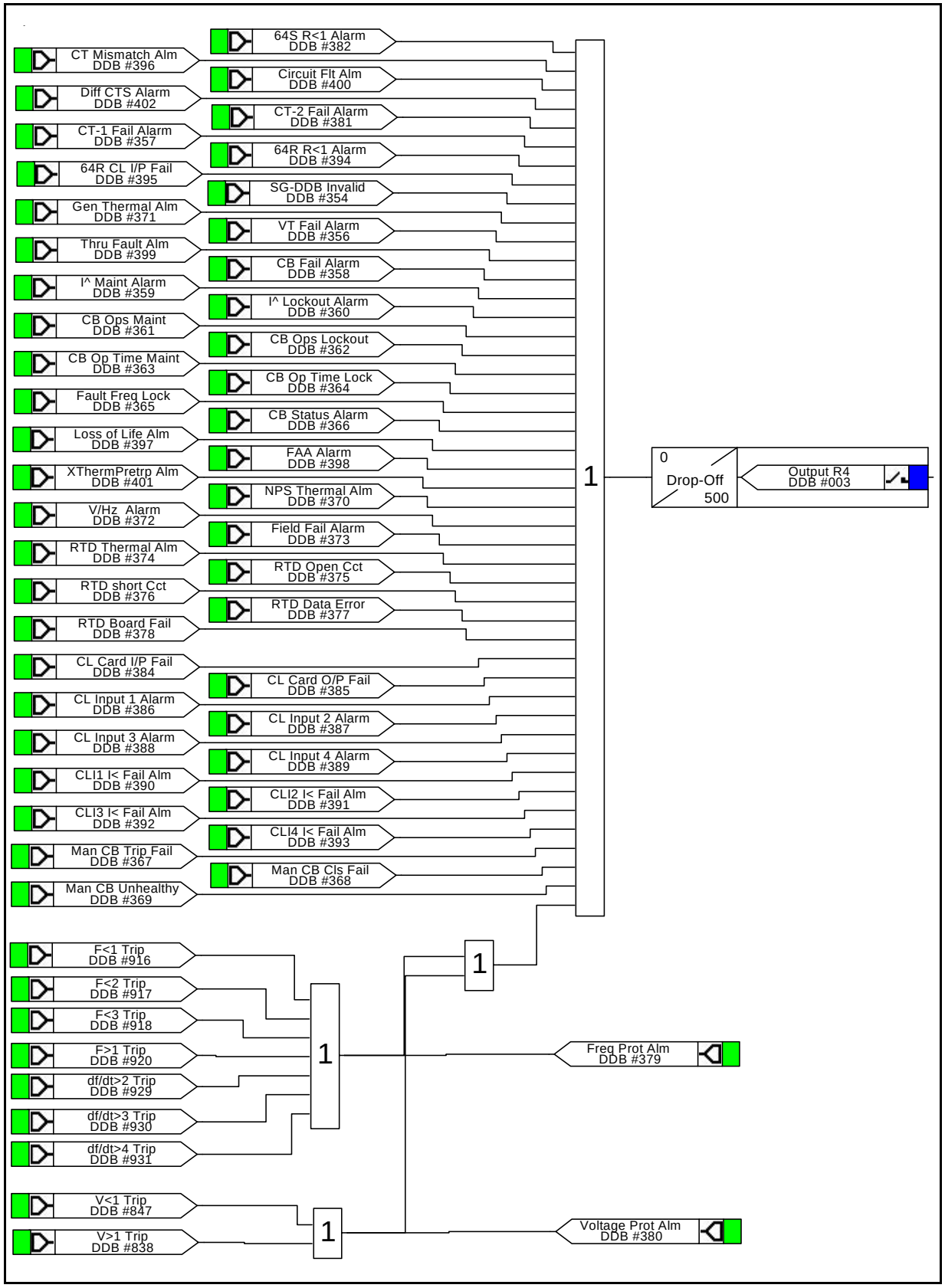


Figure 43: Output relay R4 (General Alarm) mappings

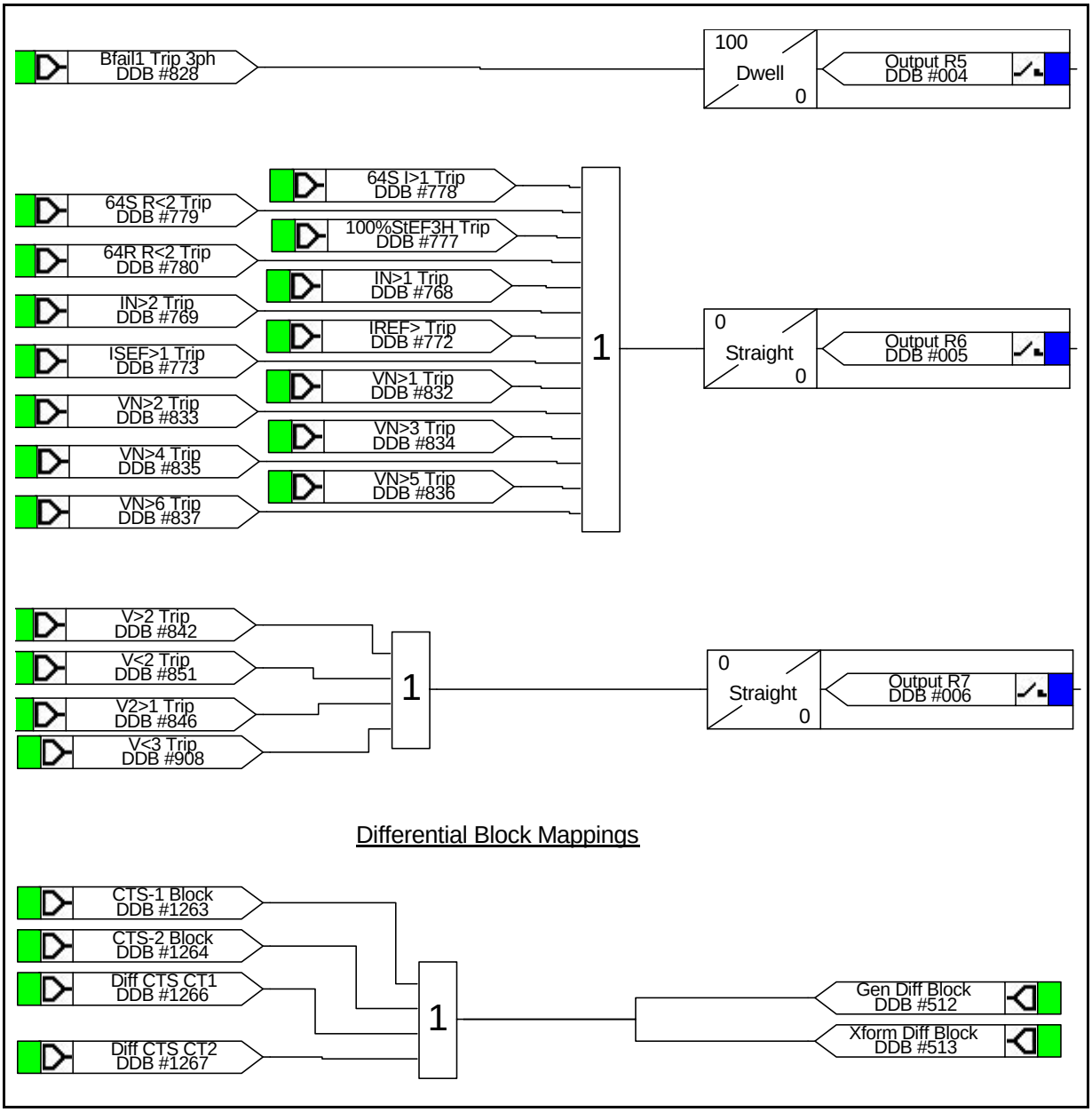


Figure 44: Output relay mappings

PL

PL

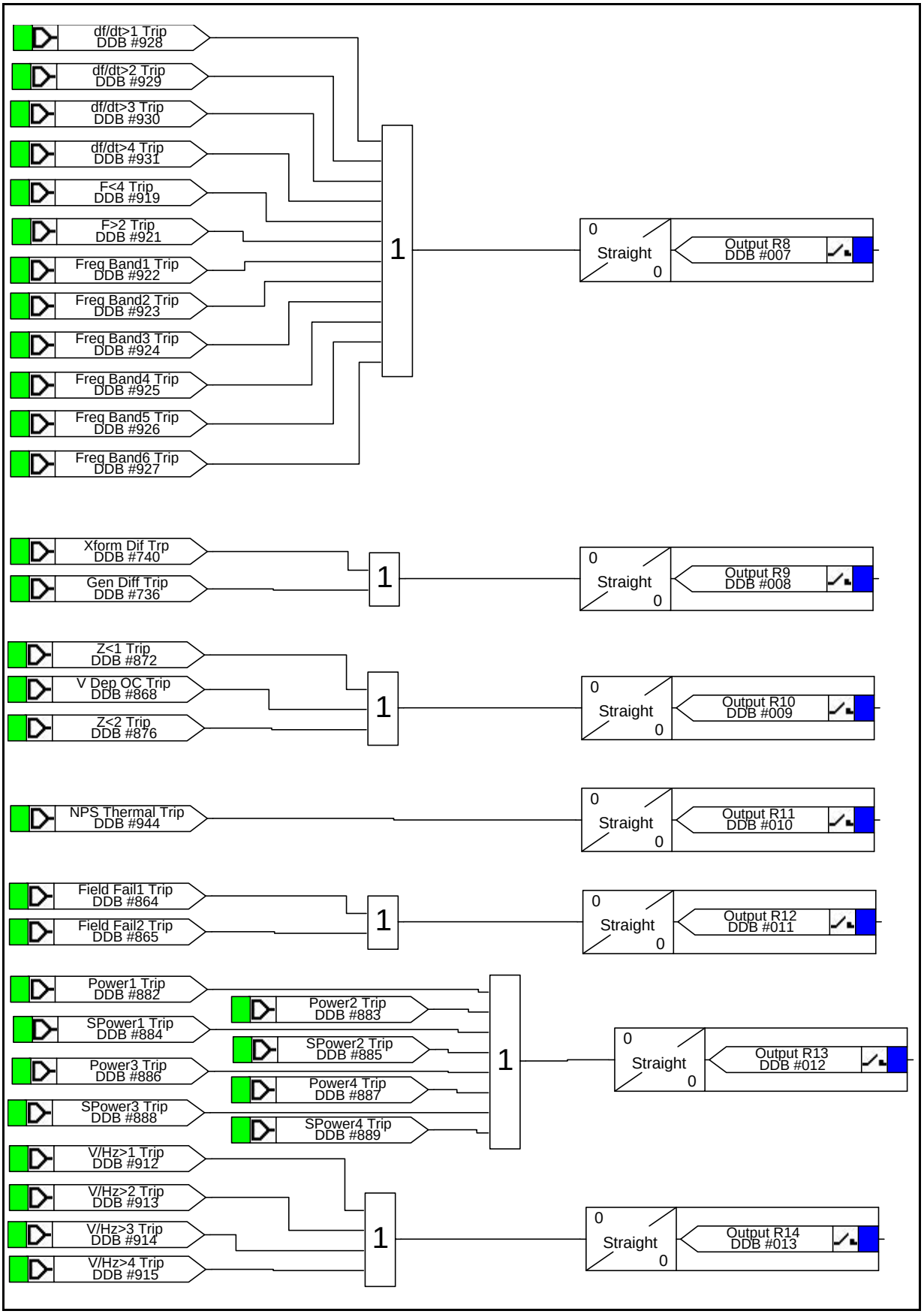


Figure 45: Output relay mappings

5.3 Function and LED Mapping

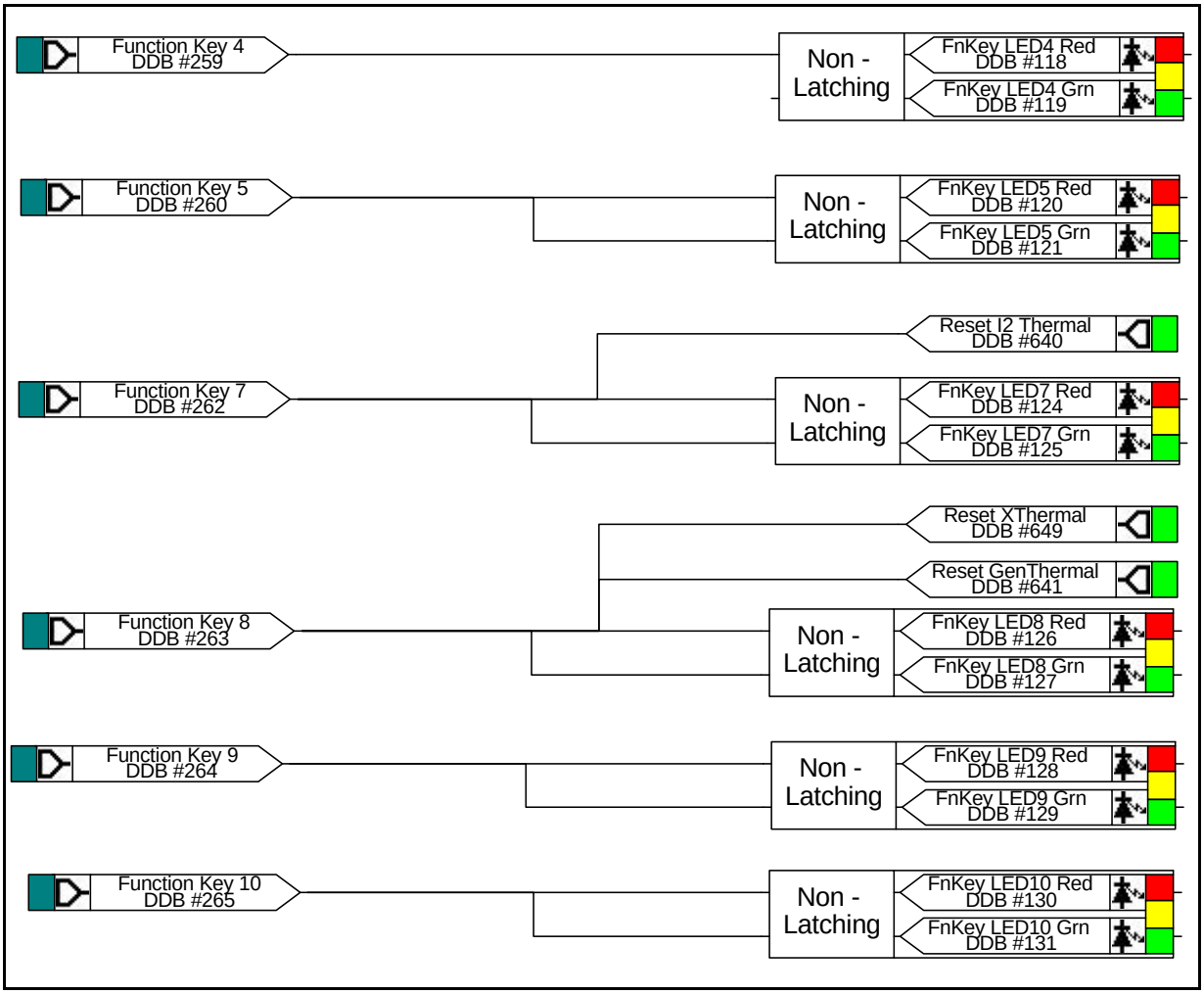


Figure 46: Function key and function LED mapping

PL

5.4 LED Mapping

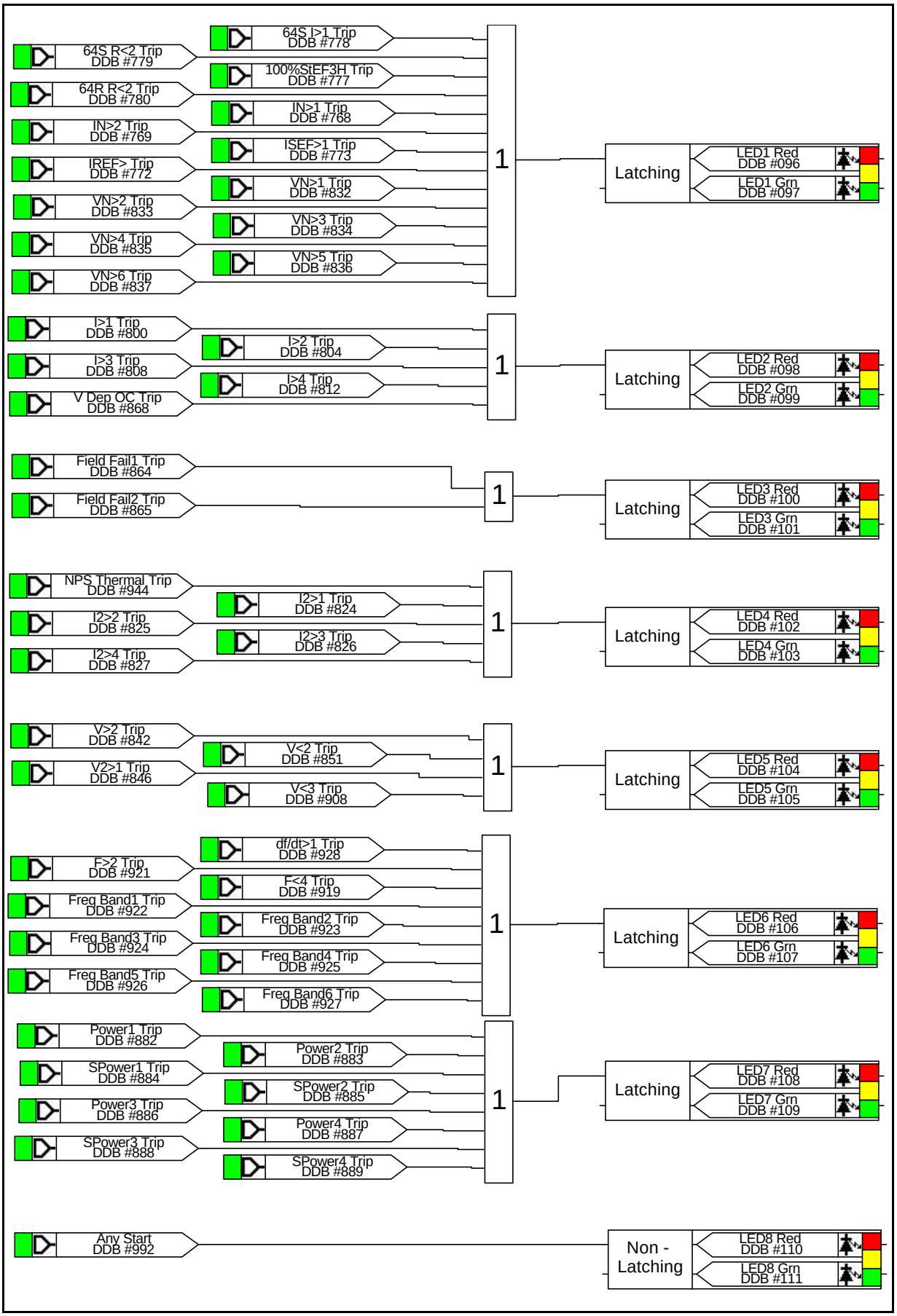


Figure 47: LED output mapping

5.5 Check Synch Mapping

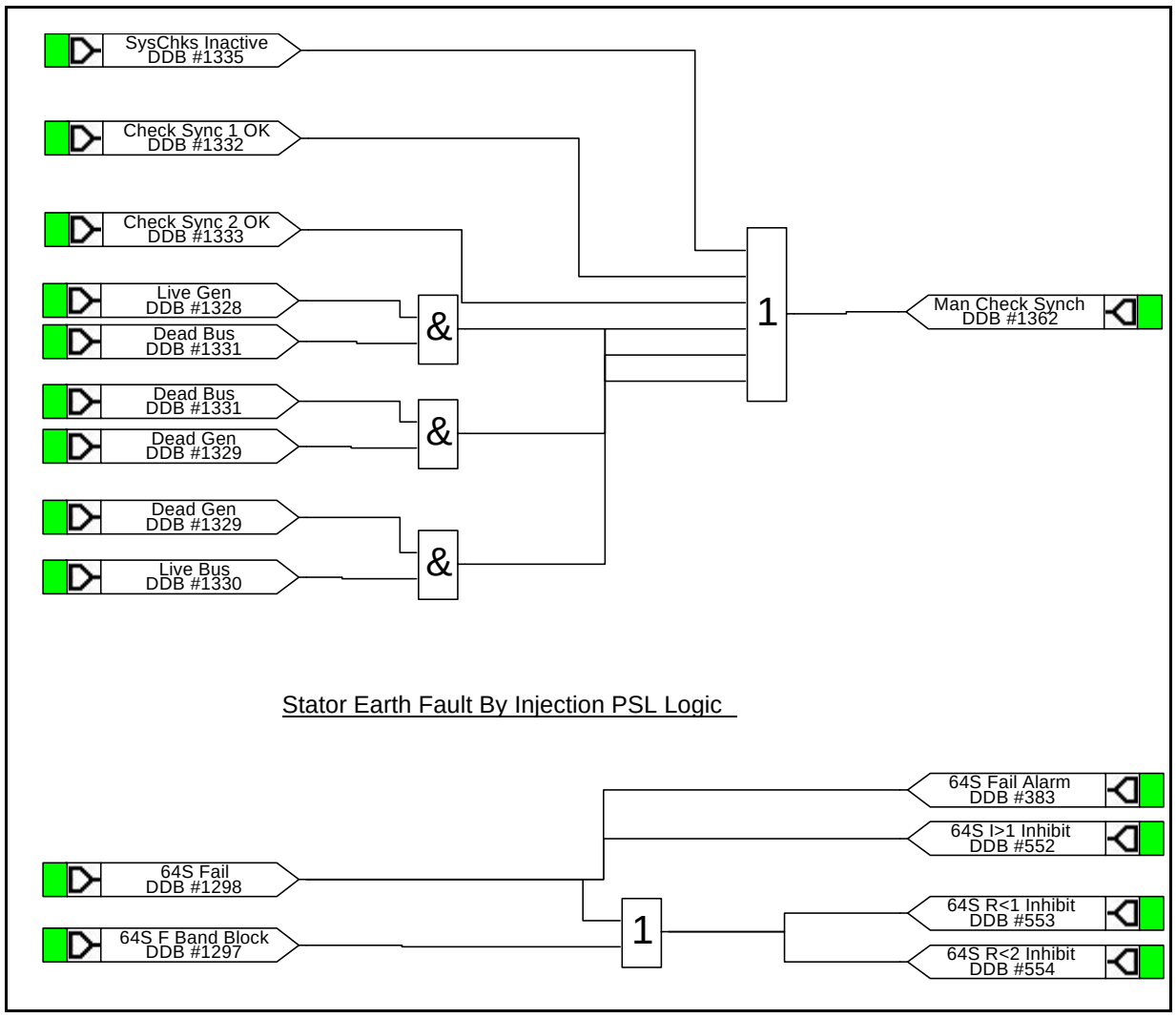


Figure 48: Check synch and VOL monitor mapping

PL

6 P346 PROGRAMMABLE SCHEME LOGIC

6.1 Input Mappings

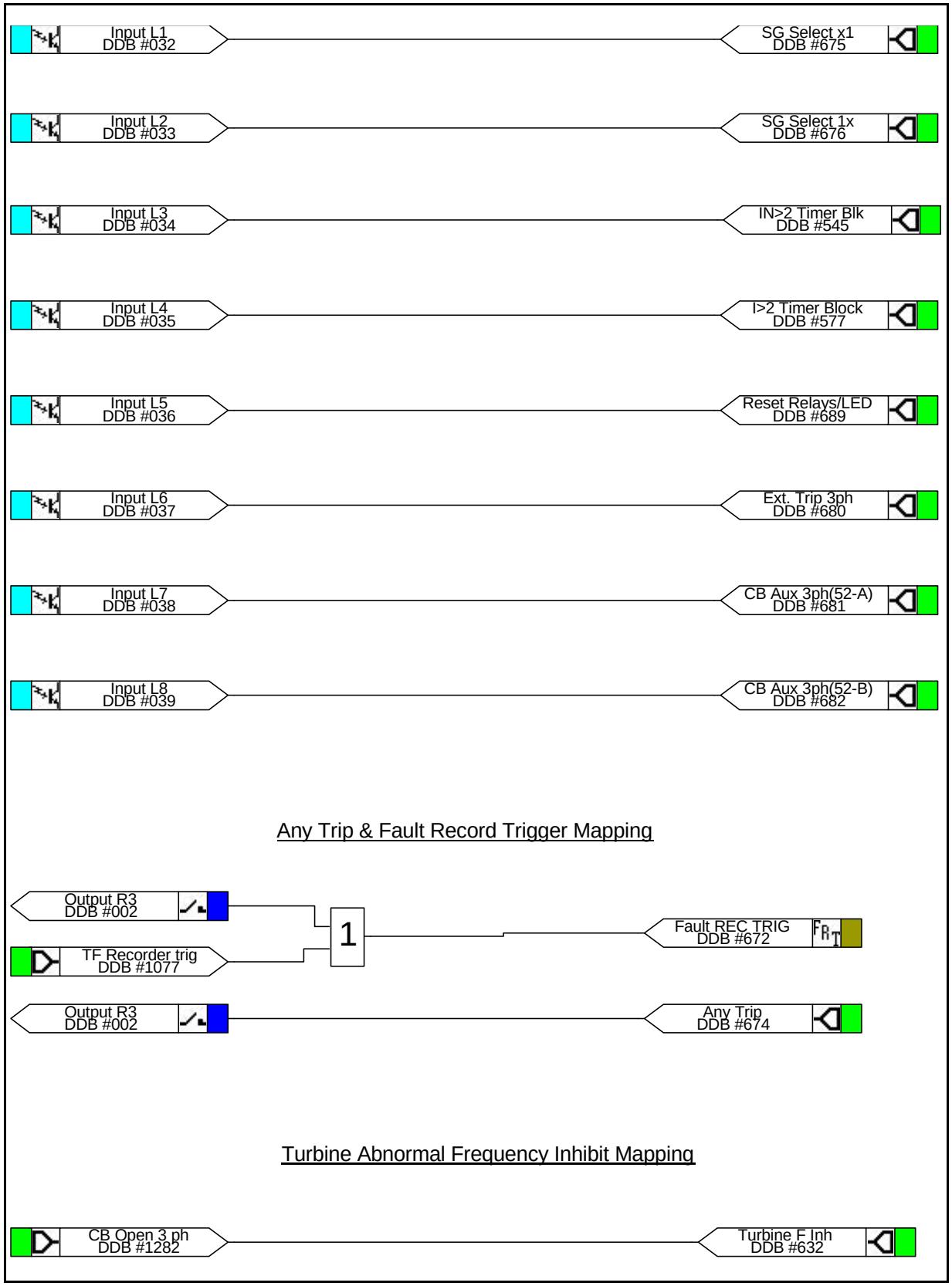


Figure 49: Opto input mapping

6.2 Output Mappings

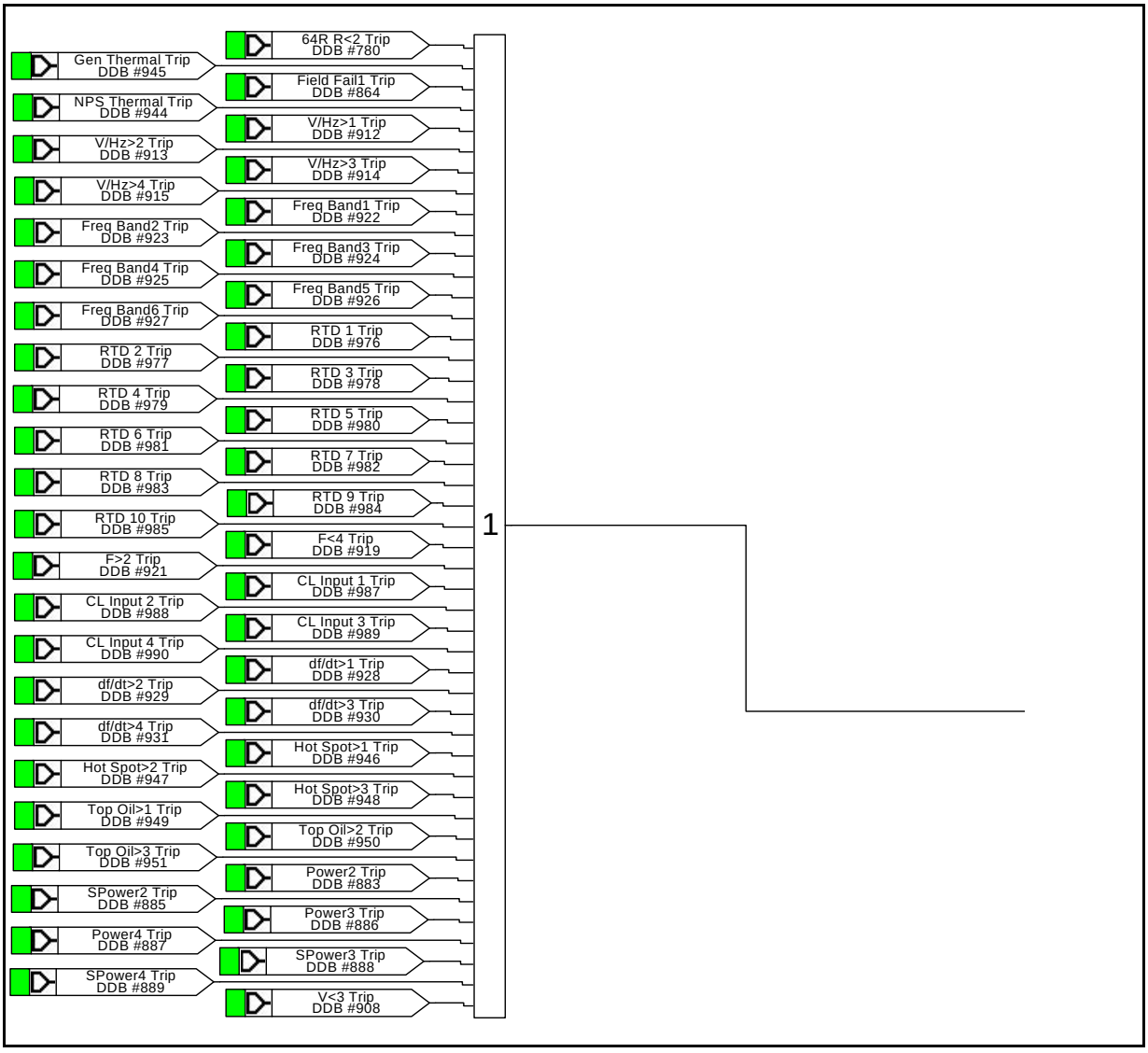


Figure 50: Output relay R1 (Trip CB) mappings

PL

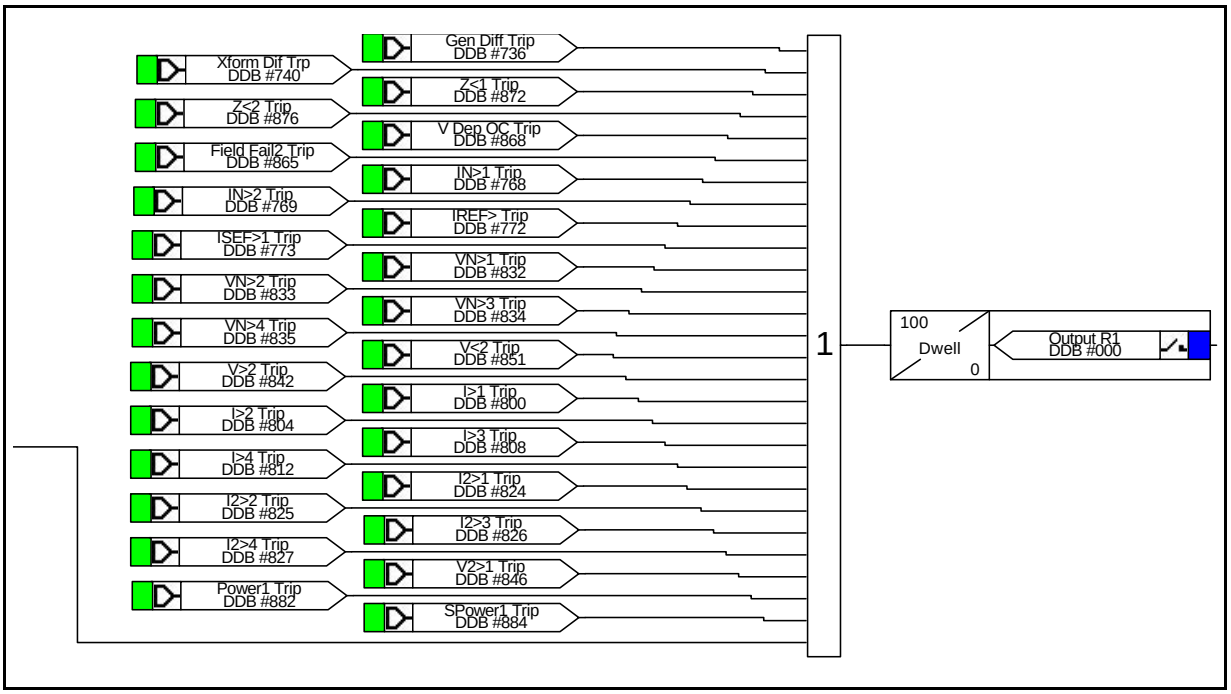


Figure 51: Output relay R1 (Trip CB) mappings

PL

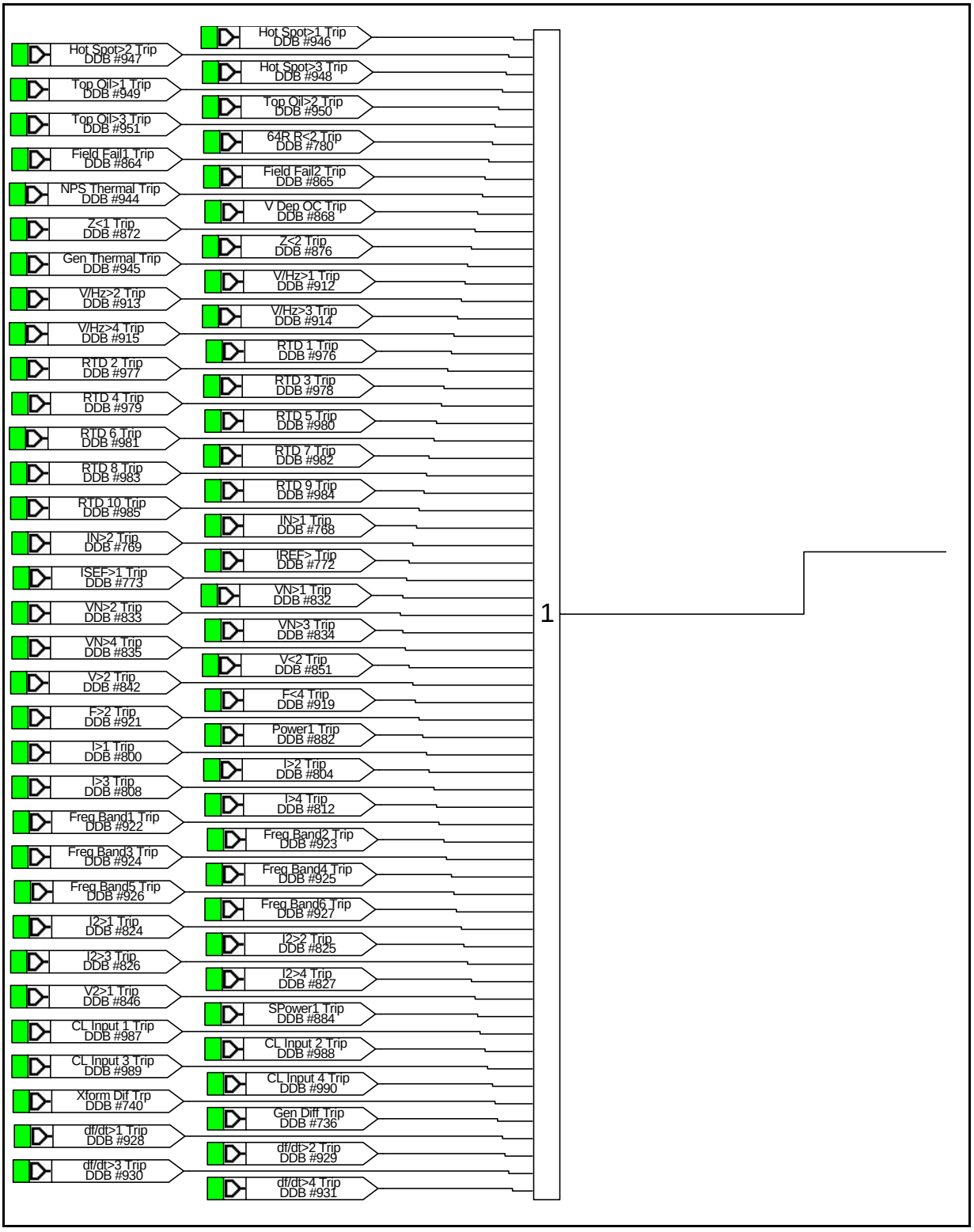


Figure 52: Output relay R2 (Trip Prime Mover) mappings

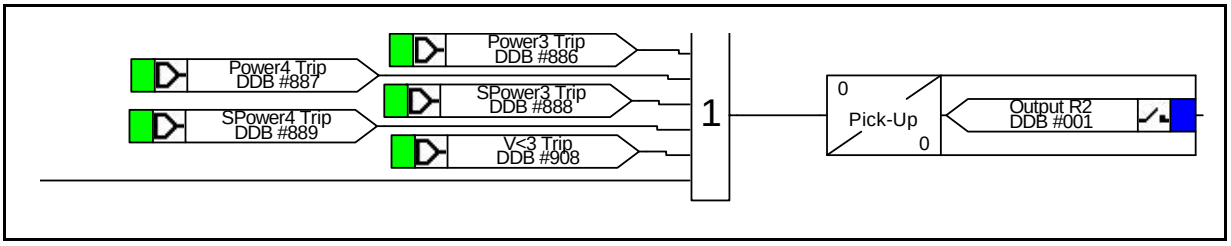


Figure 53: Output relay R2 (Trip Prime Mover) mappings

PL

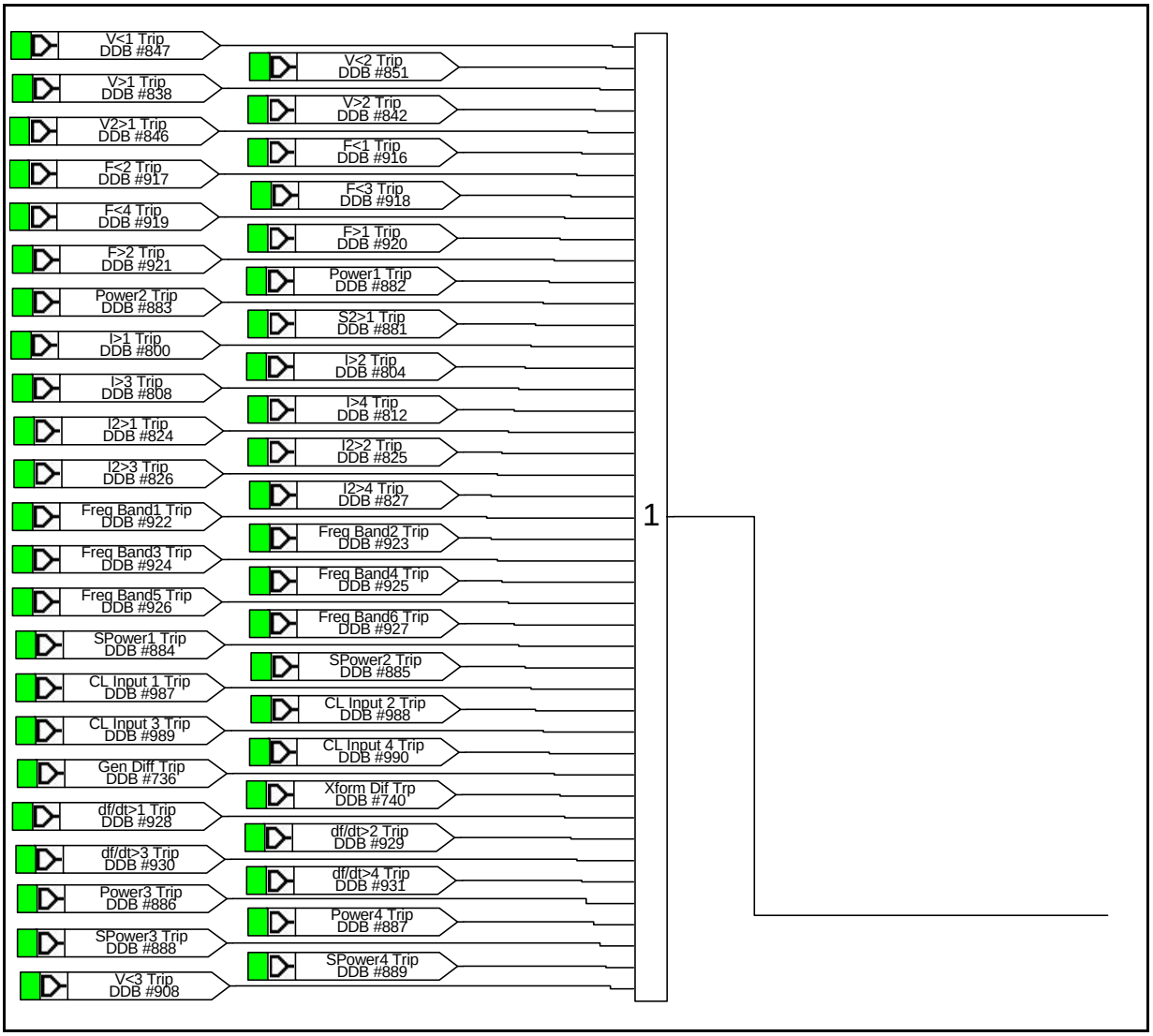


Figure 54: Output relay R3 (Any Trip) mappings

PL

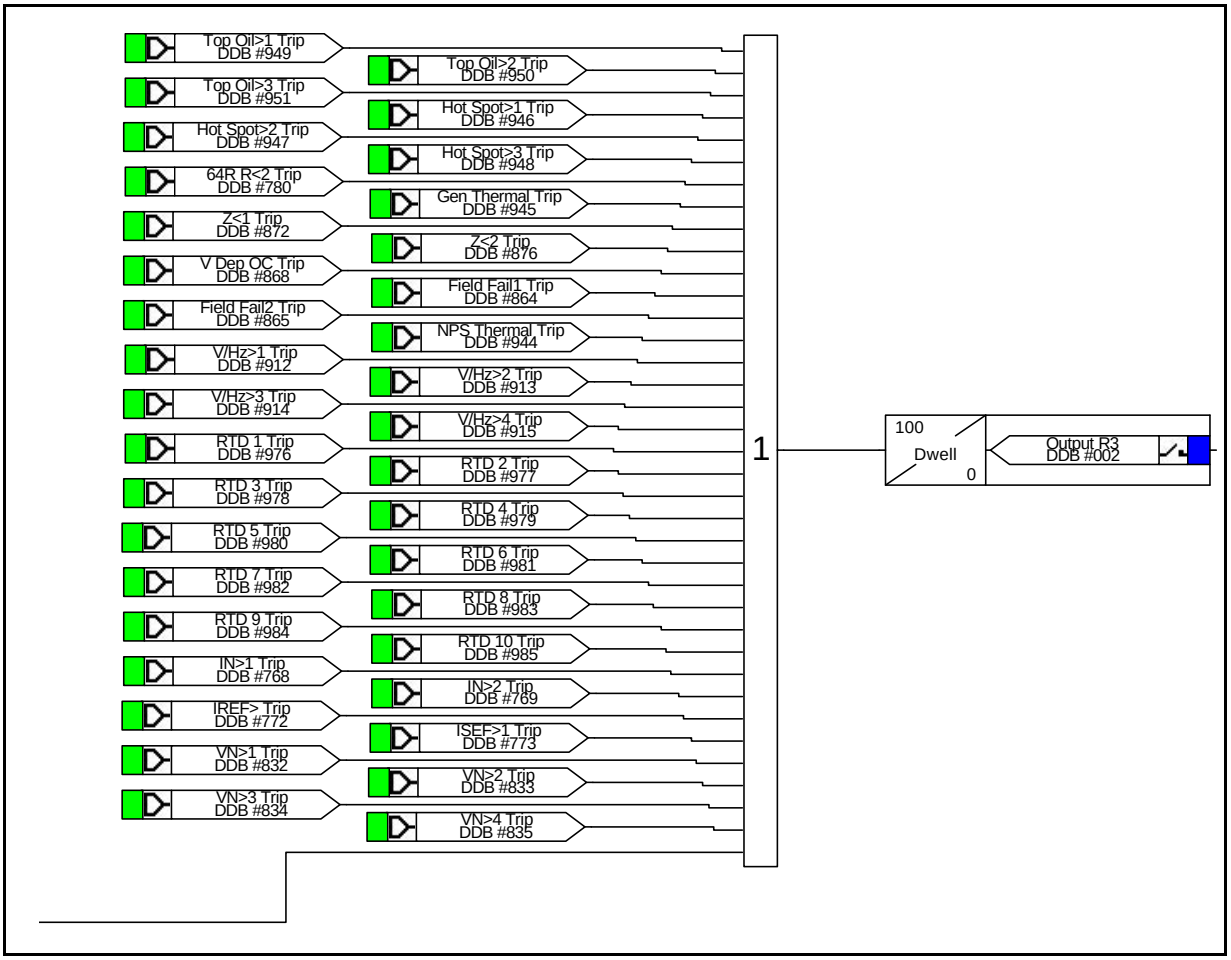


Figure 55: Output relay R3 (Any Trip) mappings

PL

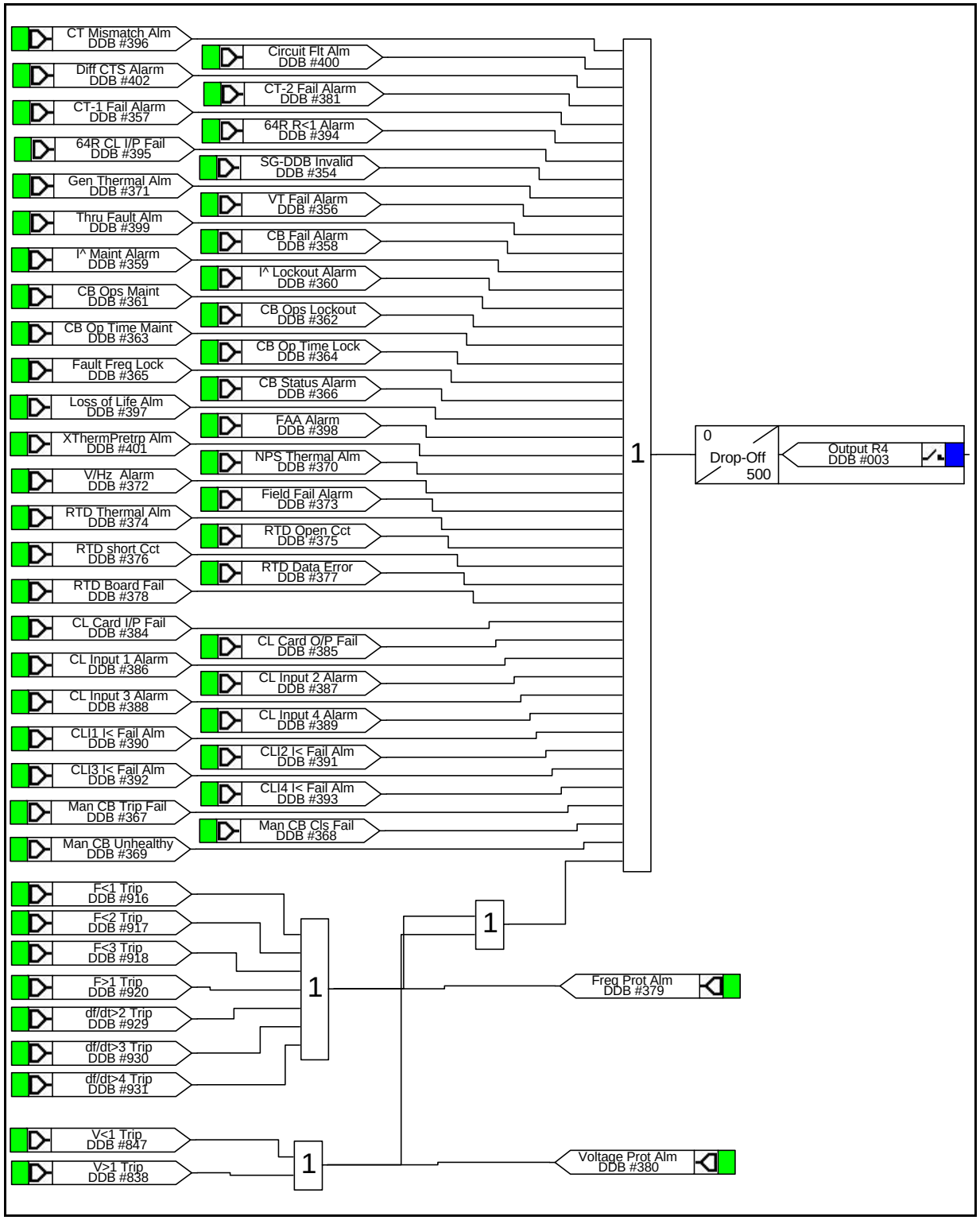


Figure 56: Output relay R4 (General Alarm) mappings

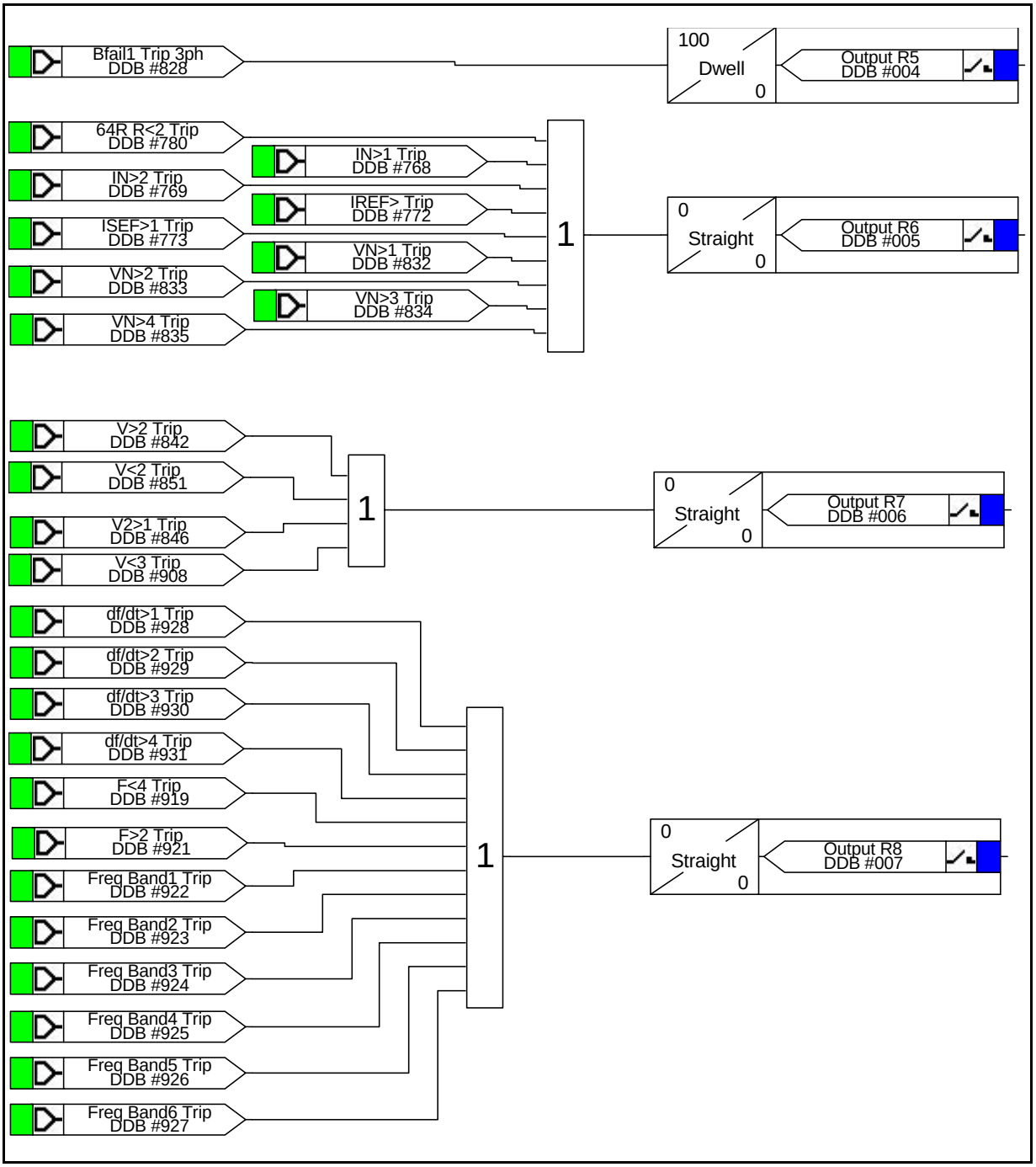


Figure 57: Output relay mappings

PL

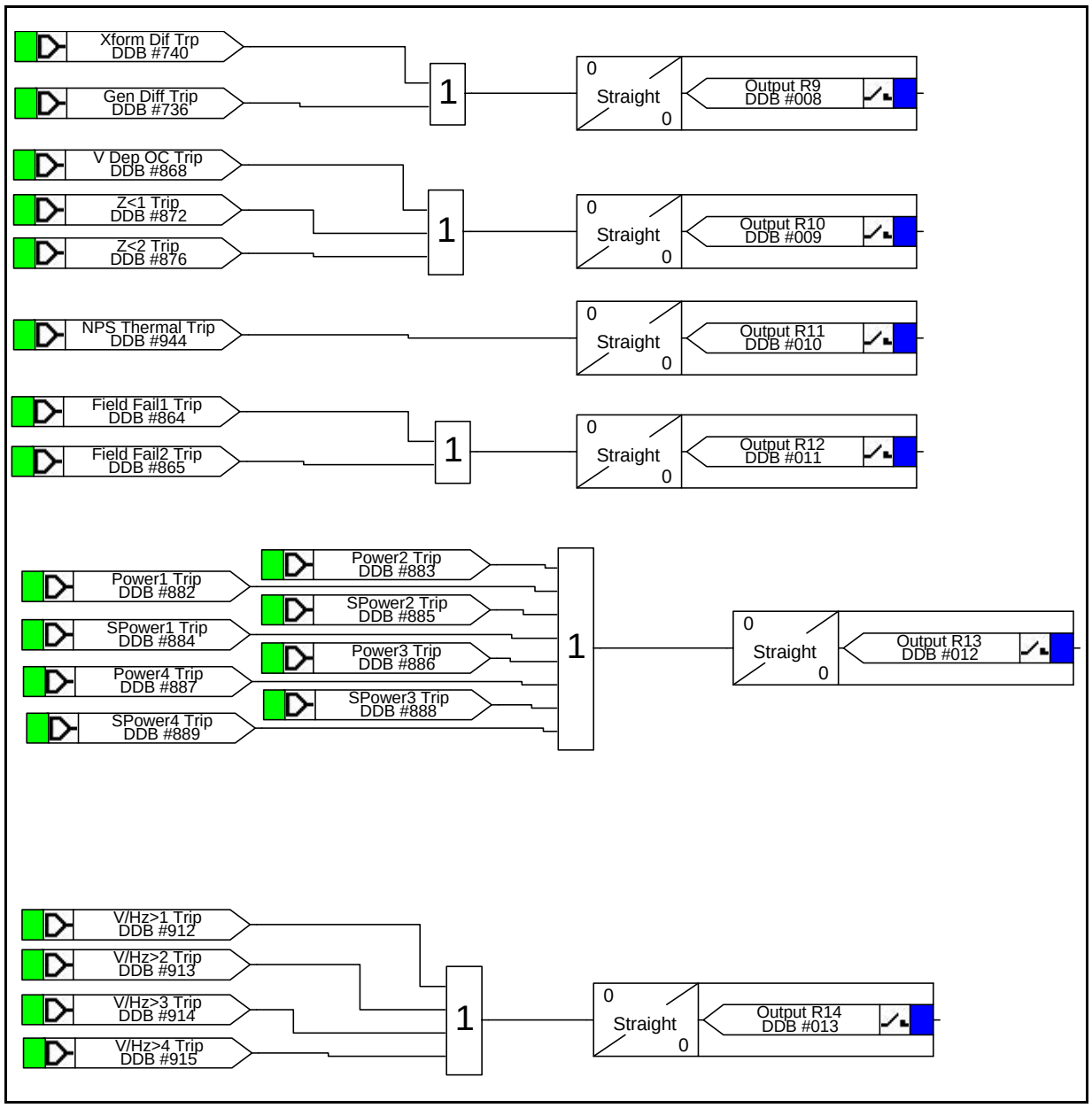


Figure 58: Output relay mappings

PL

6.3 LED Mapping

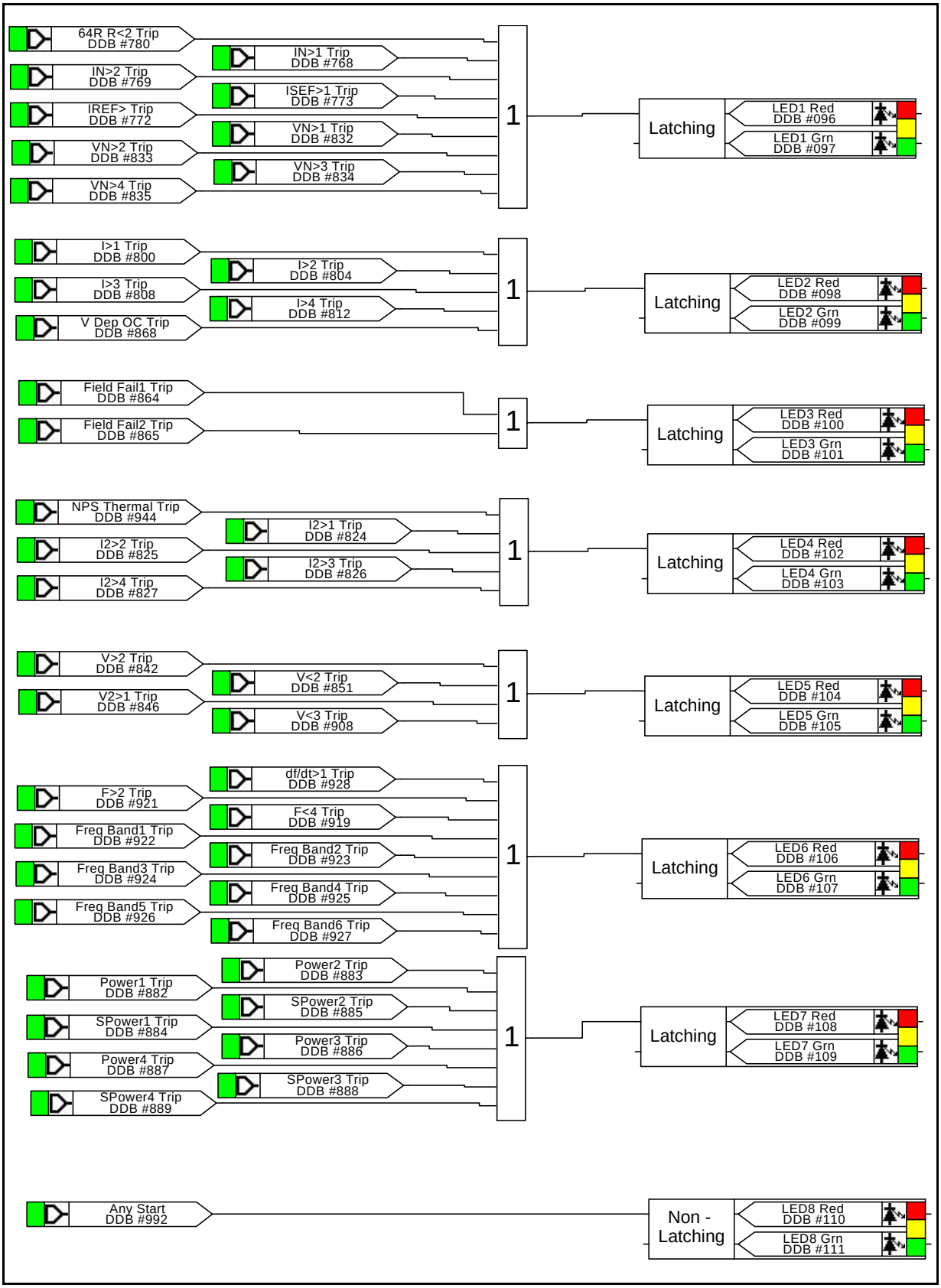


Figure 59: LED output mappings

PL

6.4 Function and LED Mapping

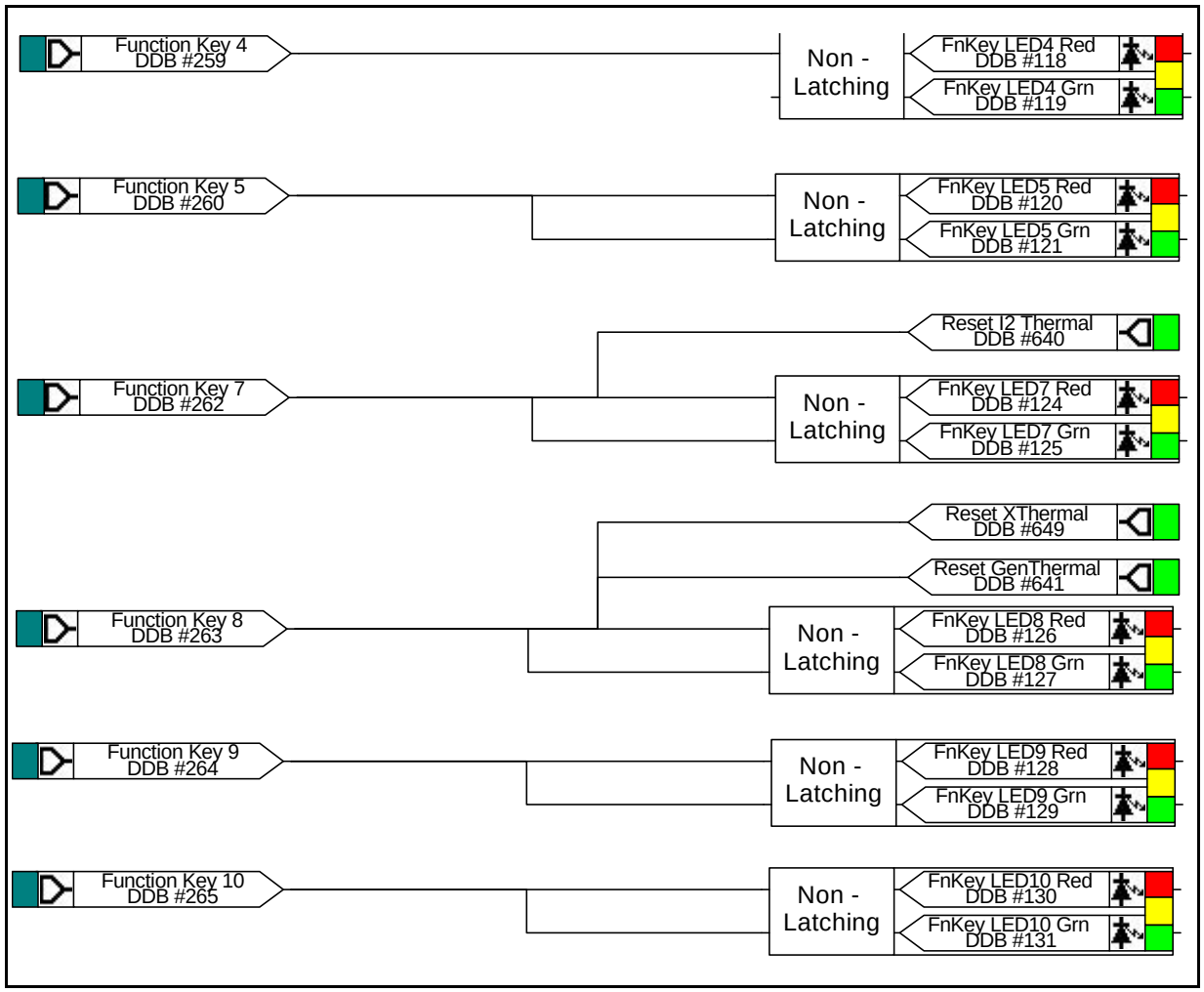


Figure 60: Function key and function LED mapping

PL

6.5 Check Synch Mapping

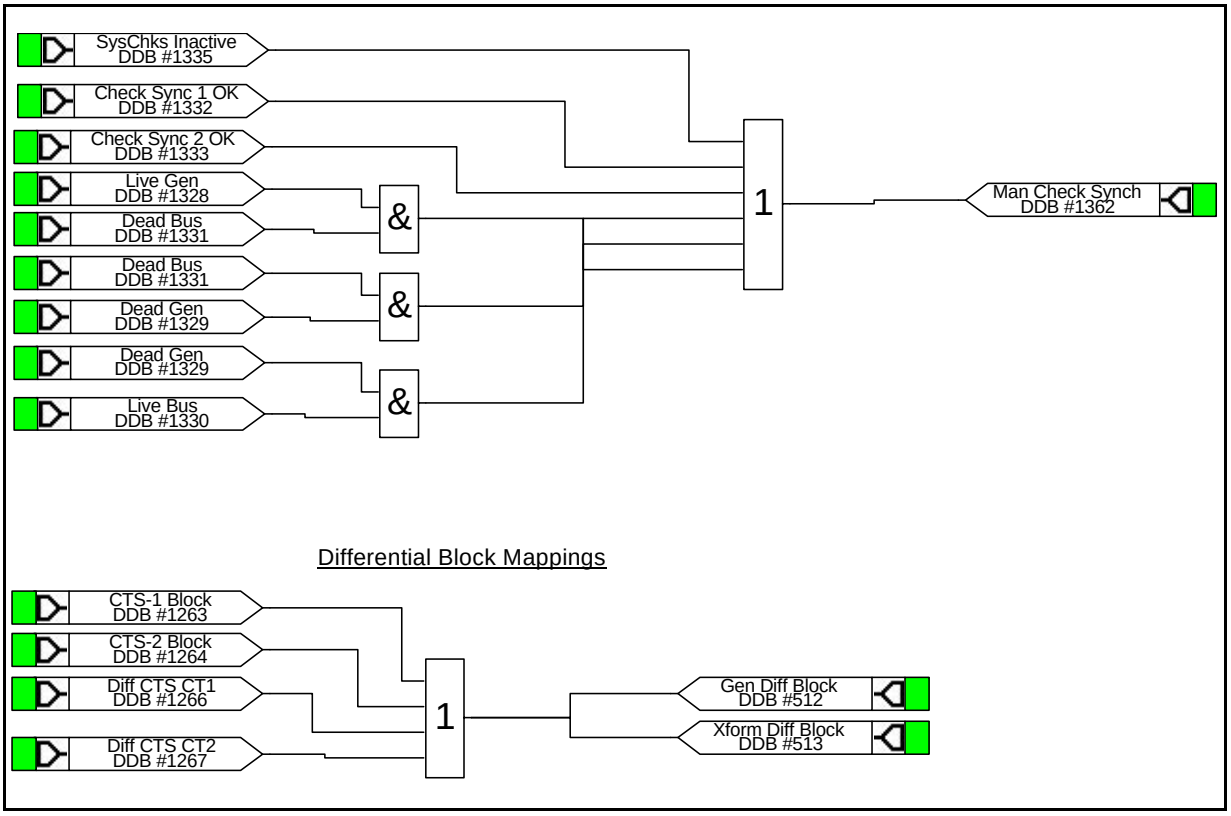


Figure 61: Check synch and voltage monitor mapping

PL

7 P348 PROGRAMMABLE SCHEME LOGIC

7.1 Input Mappings

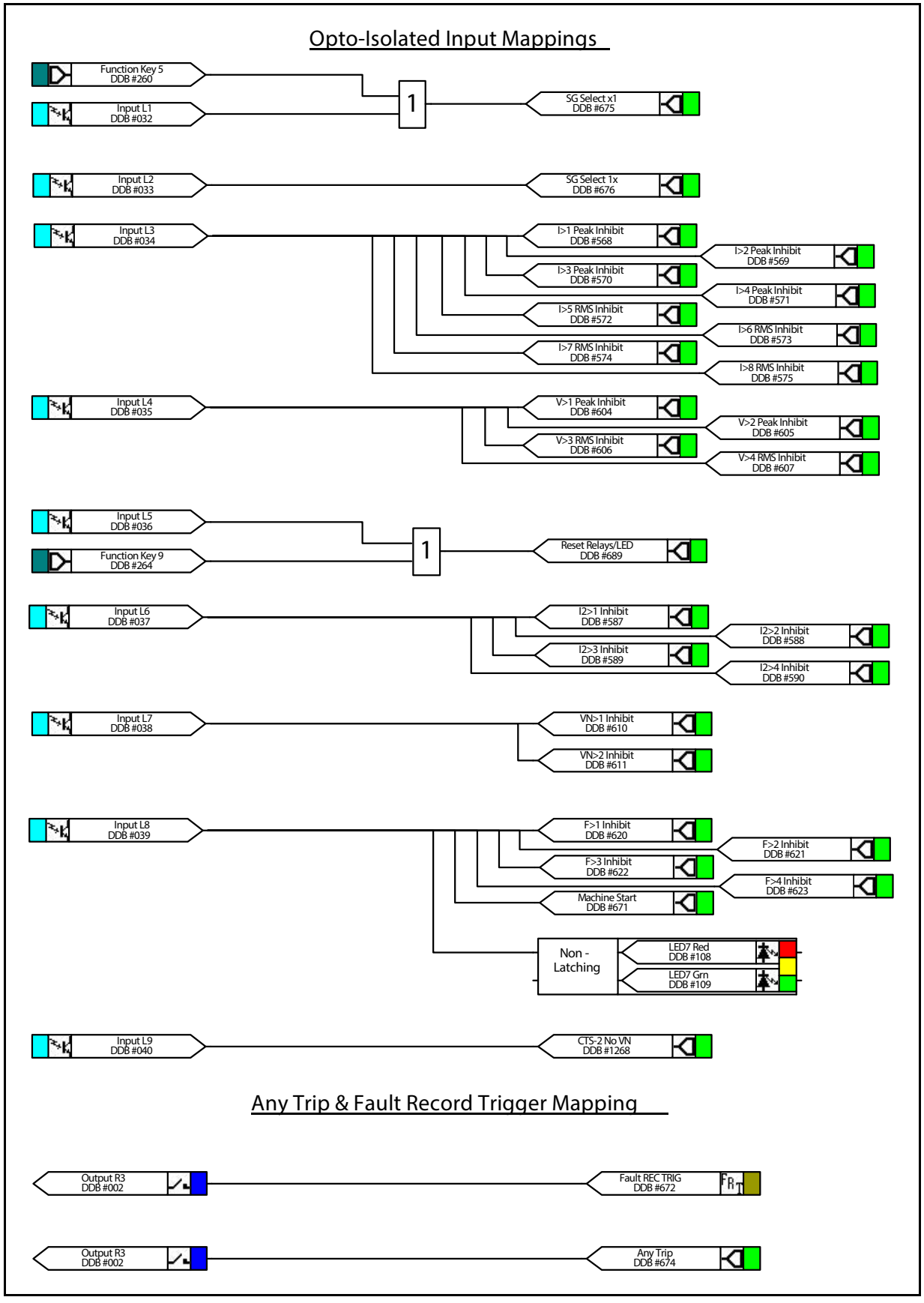


Figure 62: Opto input mappings

7.2 Output Mappings

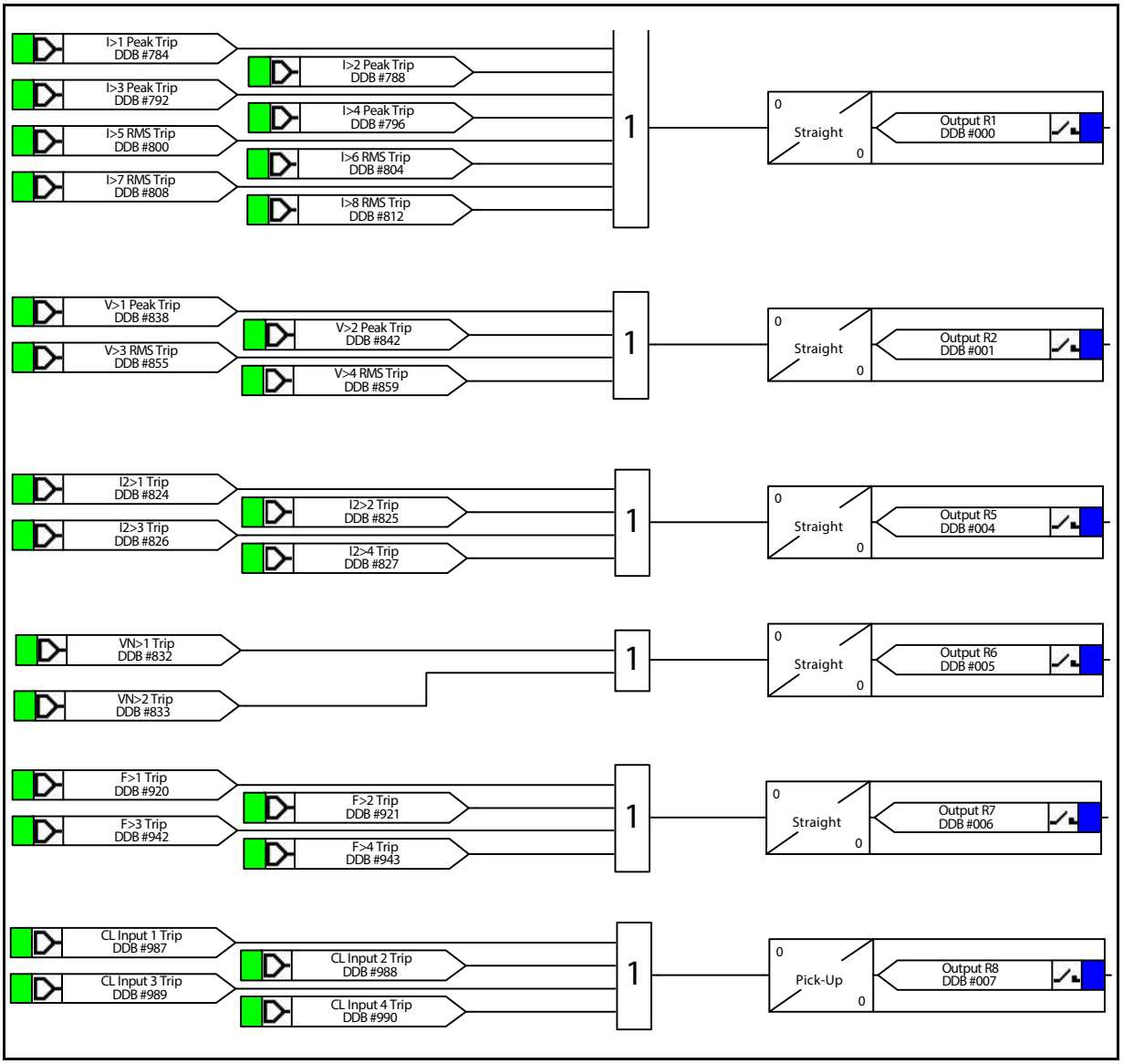


Figure 63: Output relay mappings

PL

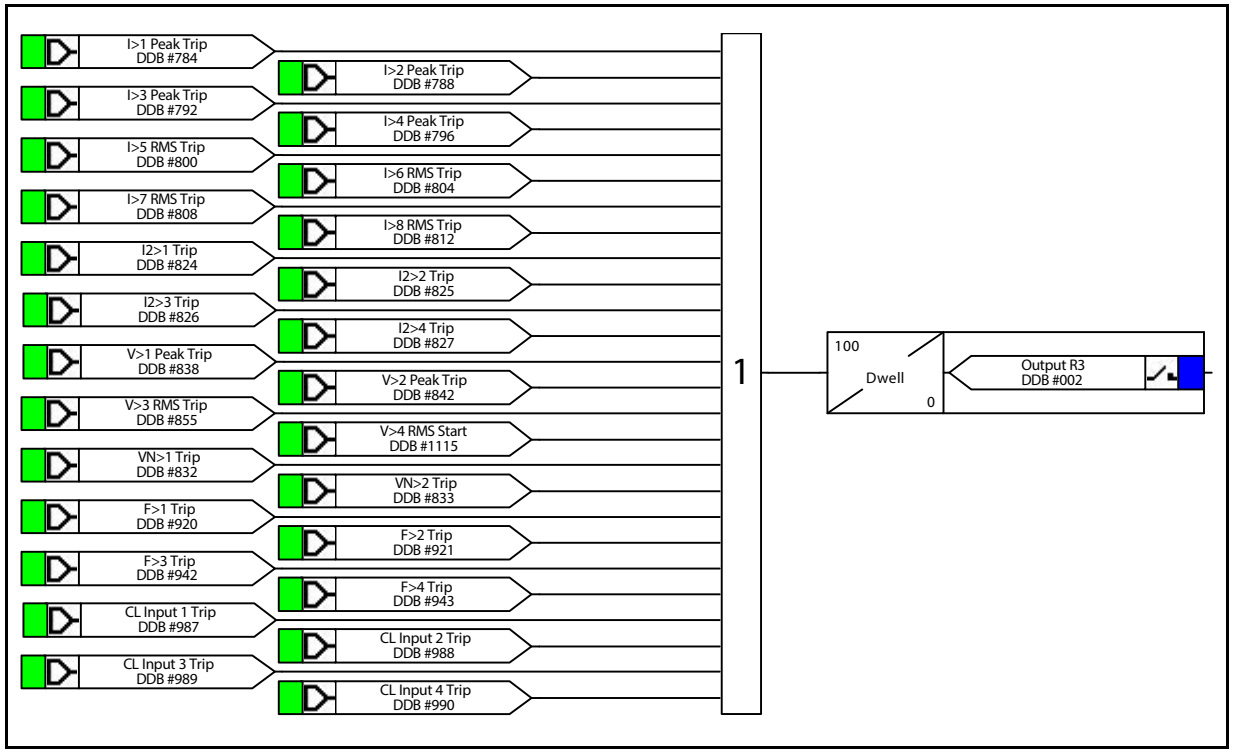


Figure 64: Output relay R3 (Any Trip) mappings

PL

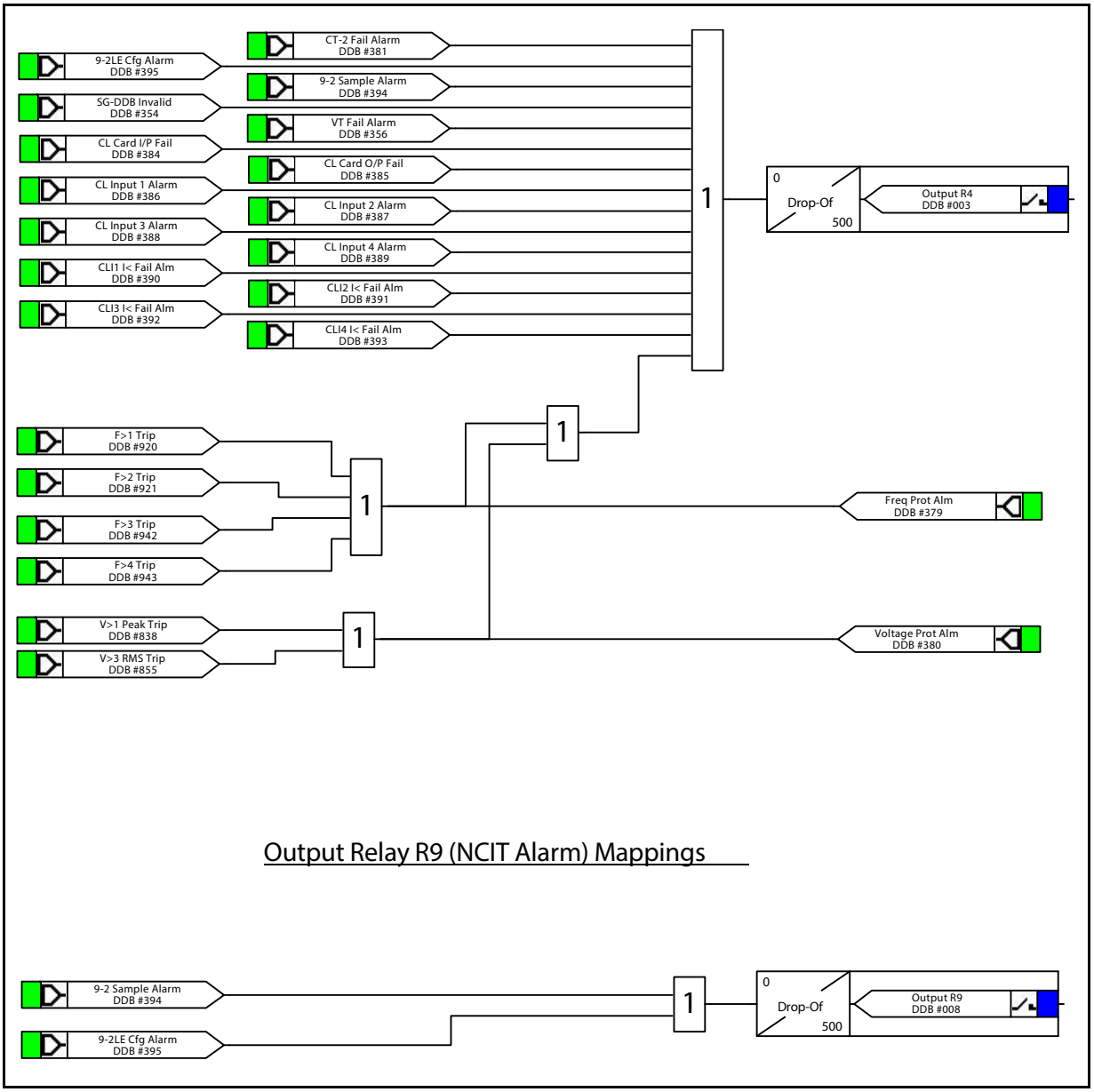


Figure 65: Output relay R4 (General Alarm) mappings

PL

PL

7.3 LED Mapping

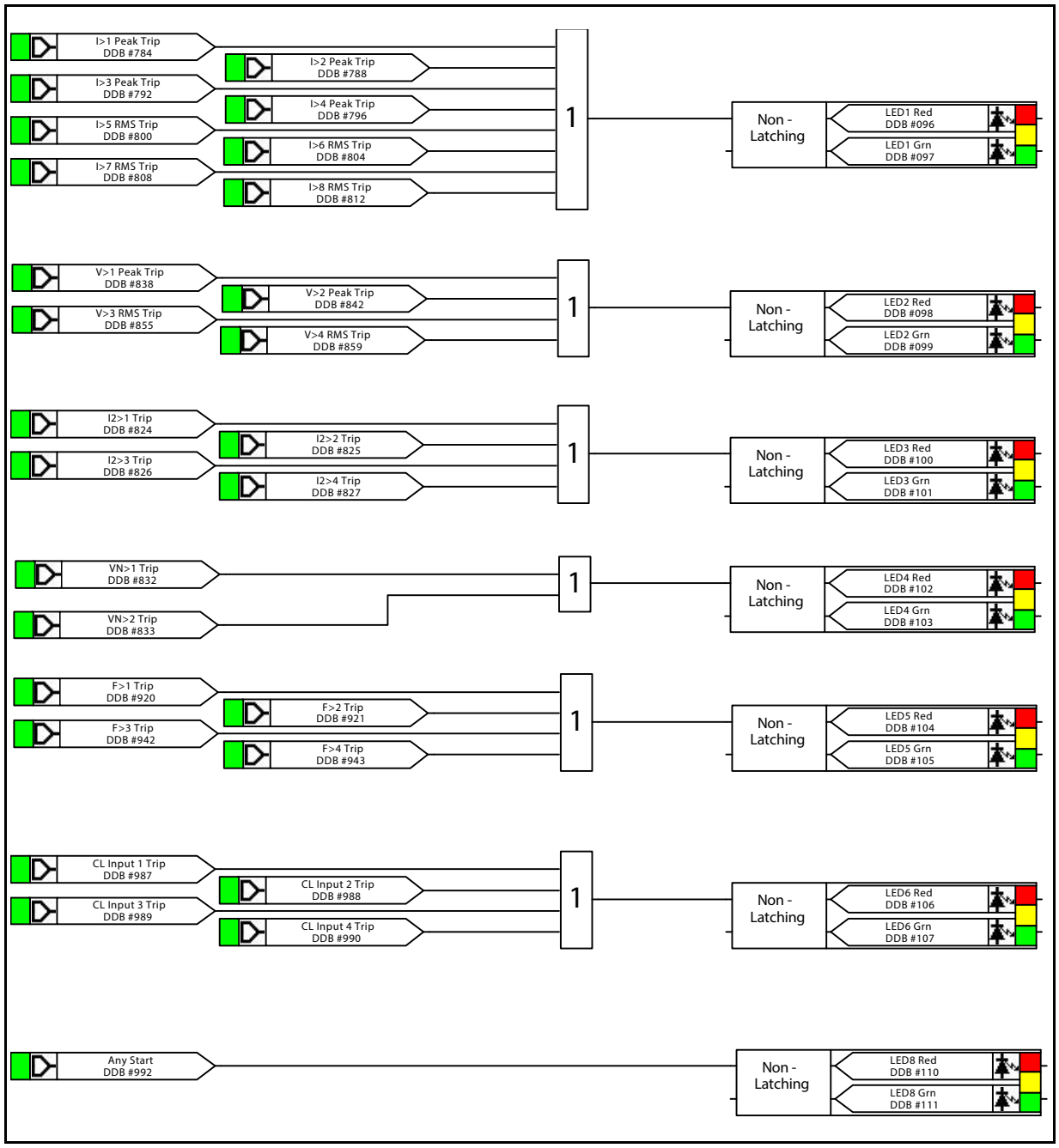


Figure 66: LED output mapping

7.4 Function and LED Mapping

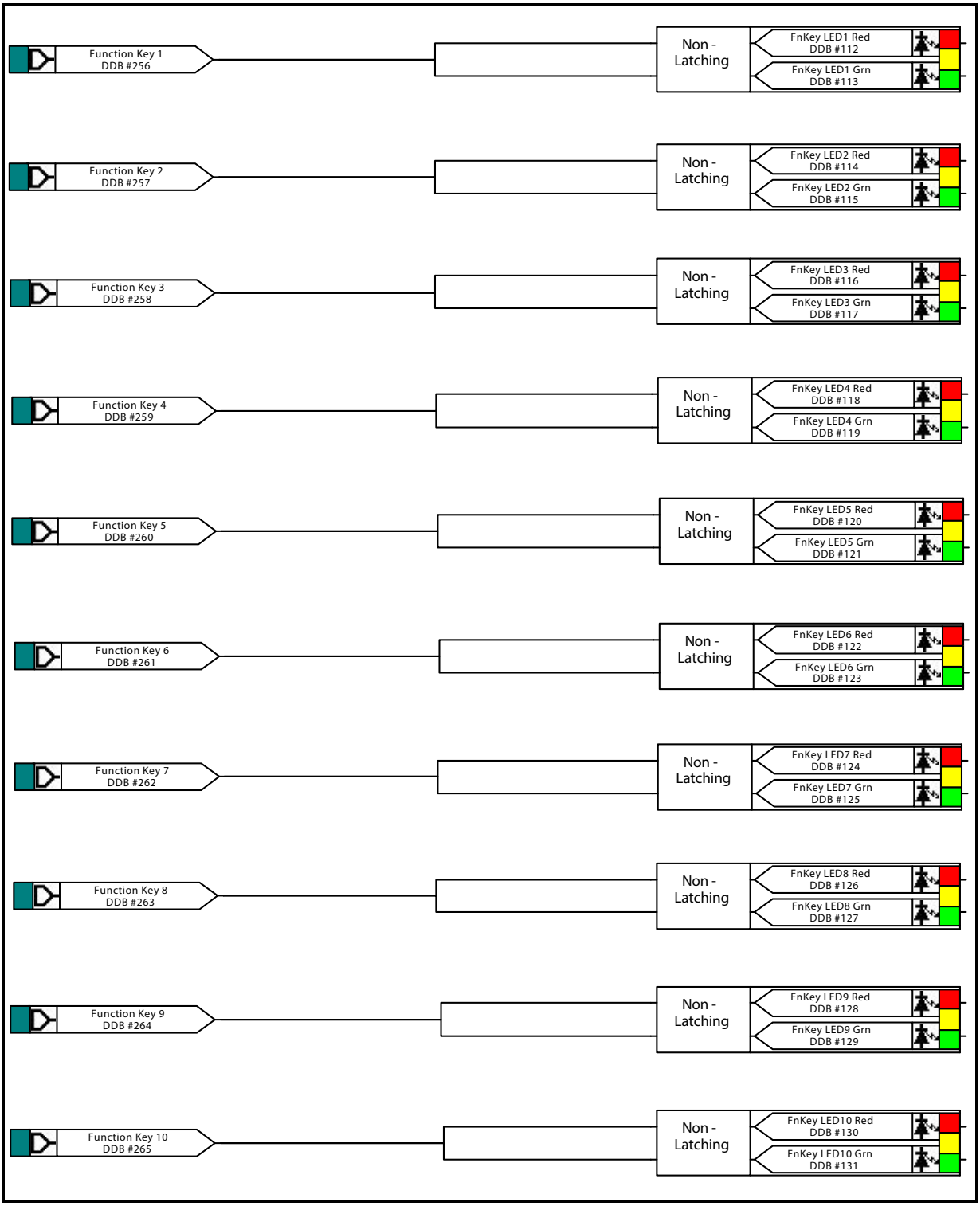


Figure 67: Function key and function LED mapping

PL

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MEASUREMENTS AND RECORDING

Hardware Suffix:	**P (P342) M (P343/4/6/8)** **M (P345/8)** **A (P391)**
Software Version:	**38 (P342/3/4/6)** **37 (P348)**

MR

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1 MEASUREMENTS AND RECORDING

1.1 Introduction

The P34x is equipped with integral measurements, event, fault and disturbance recording facilities suitable for analysis of complex system disturbances.

The relay is flexible enough to allow for the programming of these facilities to specific user application requirements and are discussed below.

1.2 Event & fault records

The relay records and time tags up to 512 events and stores them in non-volatile (battery backed up) memory. This enables the system operator to establish the sequence of events that occurred within the relay following a particular power system condition, switching sequence etc. When the available space is exhausted, the oldest event is automatically overwritten by the new one.

The real time clock within the relay provides the time tag to each event, to a resolution of 1 ms.

The event records are available for viewing either via the frontplate LCD or remotely, via the communications ports (courier and MODBUS versions only).

Local viewing on the LCD is achieved in the menu column entitled "VIEW RECORDS". This column allows viewing of event, fault and maintenance records and is shown in Table 1.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VIEW RECORDS				
Select Event	0	0	511	
Setting range from 0 to 511. This selects the required event record from the possible 512 that may be stored. A value of 0 corresponds to the latest event and so on.				
Menu Cell Ref	(From record)	Latched alarm active, Latched alarm inactive, Self reset alarm active, Self reset alarm inactive, Relay contact event, Opto-isolated input event, Protection event, General event, Fault record event, Maintenance record event		
Indicates the type of event.				
Time and Date	Data			
Time & Date Stamp for the event given by the internal Real Time Clock.				
Event text	Data.			
Up to 32 Character description of the Event. See event sheet in the Relay Menu Database document, *P34x/EN/MD.*				
Event Value	Data.			
32 bit binary string indicating ON or OFF (1 or 0) status of relay contact or opto input or alarm or protection event depending on event type. Unsigned integer is used for maintenance records. See event sheet in the Relay Menu Database document, *P34x/EN/MD*.				
Select Fault	0	0	19	1
Setting range from 0 to 19. This selects the required fault record from the possible 5 that may be stored. A value of 0 corresponds to the latest fault and so on.				
Faulted Phase	00000000			
Displays the faulted phase as a binary string, bits 0 – 8 = Start A/B/C/N Trip A/B/C/N.				
Start elements 1	00000000000000000000000000000000			
32 bit binary string gives status of first 32 start signals. See Data Type G84 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Start elements 2	00000000000000000000000000000000			
32 bit binary string gives status of second 32 start signals. See Data Type G107 in the Relay Menu Database document, *P34x/EN/MD* for details.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Start elements 3	00000000000000000000000000000000			
32 bit binary string gives status of third 32 start signals. See Data Type G129 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Start elements 4	00000000000000000000000000000000			
32 bit binary string gives status of third 32 start signals. See Data Type G131 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Trip elements 1	00000000000000000000000000000000			
32 bit binary string gives status of first 32 trip signals. See Data Type G85 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Trip elements 2	00000000000000000000000000000000			
32 bit binary string gives status of second 32 trip signals. See Data Type G86 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Trip elements 3	00000000000000000000000000000000			
32 bit binary string gives status of third 32 trip signals. See Data Type G130 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Trip elements 4	00000000000000000000000000000000			
32 bit binary string gives status of third 32 trip signals. See Data Type G132 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Fault Alarms	0000001000000000			
32 bit binary string gives status of fault alarm signals. See Data Type G87 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Fault Alarms2	0000001000000000			
32 bit binary string gives status of fault alarm signals. See Data Type G89 in the Relay Menu Database document, *P34x/EN/MD* for details.				
Fault Time	Data.			
Fault time and date.				
Active Group	Data.			
Active setting group 1-4.				
System Frequency	Data			
System frequency.				
System Frequency2	Data			
System frequency 2. (P348 only). In the P348 System Frequency 2 is measured from IA-2/IB-2/IC-2 current inputs (normally connected to the stator) and the System frequency is measured from IA-1/IB-1/IC-1 (normally connected to the rotor). In other P34x models the System Frequency is measured from VA/VB/VC or IA-1/IB-1/IC-1 (normally connected to the stator).				
Fault Duration				
Fault duration. Time from the start or trip until the undercurrent elements indicate the CB is open.				
CB Operate Time	Data.			
CB operating time. Time from protection trip to undercurrent elements indicating the CB is open.				
Relay Trip Time	Data.			
Relay trip time. Time from protection start to protection trip.				

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
The following cells provide measurement information of the fault: (P341-6) System Frequency, IA/IA-1, IB/IB-1, IC/IC-1, VAB, VBC, VCA, VAN, VBN, VCN, IA-2, IB-2, IC-2, IA Differential, IB Differential, IC Differential, IA Diff PU, IB Diff PU, IC Diff PU, IA Diff 2H, IB Diff 2H, IC Diff 2H, IA Diff 5H, IB Diff 5H, IC Diff 5H, VN/VN1 Measured, VN2 Measured, VN Derived, IN Measured, I Sensitive1, I Sensitive2, IREF Diff, IREF Bias, I2, V2, 3 Phase Watts, 3 Phase VARs, 3Ph Power Factor, Sen Watts, Sen VArs, Sen Power Factor, RTD 1-10, CLIO Input 1-4, df/dt, 64S V Magnitude, 64S I Magnitude, 64S Rprimary, 64R CL Input, 64R R Fault, IA Peak Mag, IB Peak Mag, IC Peak Mag, I^2t Phase A, I^2t Phase B, I^2t Phase C. P348 only System frequency, System Frequency 2, IA-1 RMS, IB-1 RMS, IC-1 RMS, VA-1 RMS, VB-1 RMS, VC-1 RMS, IA-2 RMS, IB-2 RMS, IC-2 RMS, VA-1 Peak, VB-1 Peak, VC-1 Peak, VN-1 Derived Peak, VA-2 RMS, VB-2 RMS, VC-2 RMS, VN-1 Derived RMS, I2 CT2 Peak, I2 CT2 RMS, CLIO Input 1-4, IA-1 Peak, IB-1 Peak, IC-1 Peak, IA-2 Peak, IB-2 Peak, IC-2 Peak.				
Select Maint	0	0	9	1
Setting range from 0 to 9. This selects the required maintenance report from the possible 10 that may be stored. A value of 0 corresponds to the latest report and so on.				
Maint Text	Data.			
Up to 32 Character description of the occurrence.				
Maint Type	Data.			
Maintenance record fault type. This will be a number defining the fault type.				
Maint Data	0	0	4	1
Error code associated with the failure found by the self monitoring. The Maint Type and Data cells are numbers representative of the occurrence. They form a specific error code which should be quoted in any related correspondence to Report Data.				
Evt Iface Source	Data.			
Interface on which the event was logged.				
Evt Access Level	Data.			
Any security event that indicates that it came from an interface action, such as disabling a port, will also record the access level of the interface that initiated the event. This will be recorded in the 'Event State' field of the event.				
Evt Extra Info	Data.			
Each event will have a unique event id. The event id is a 32 bit unsigned integer that is incremented for each new event record and is stored in the record in battery-backed memory (BBRAM). The current event id must be non-volatile so as to preserve it during power cycles, thus it too will be stored in BBRAM. The event id will wrap back to zero when it reaches its maximum (4,294,967,295). The event id will be used by PC based utilities when organising extracted logs from IED's.				
Reset Indication	No	No, Yes		N/A
Resets latched LEDs and latched relay contacts provided the relevant protection element has reset.				

Table 1: Local viewing of records

For extraction from a remote source via communications, refer to the SCADA Communications section (*P34x/EN SC*), where the procedure is fully explained.

Note: A full list of all the event types and the meaning of their values is given in the Relay Menu Database document, *P34x/EN MD*.

1.2.1 Types of event

An event may be a change of state of a control input or output relay, an alarm condition, setting change etc. The following sections show the various items that constitute an event:

1.2.1.1 Change of state of opto-isolated inputs

If one or more of the opto (logic) inputs has changed state since the last time that the protection algorithm ran, the new status is logged as an event. When this event is selected to be viewed on the LCD, three applicable cells will become visible as shown:

Time & date of event
"LOGIC INPUTS"
"Event Value 0101010101010101"

The Event Value is an 8, 12, 16, 24 or 32-bit word showing the status of the opto inputs, where the least significant bit (extreme right) corresponds to opto input 1 etc. The same information is present if the event is extracted and viewed via PC.

1.2.1.2 Change of state of one or more output relay contacts

If one or more of the output relay contacts have changed state since the last time that the protection algorithm ran, then the new status is logged as an event. When this event is selected to be viewed on the LCD, three applicable cells will become visible as shown below:

Time & date of event
"OUTPUT CONTACTS"
"Event Value 010101010101010101010"

The Event Value is a 7, 11, 14, 15, 16, 22, 24 or 32 bit word showing the status of the output contacts, where the least significant bit (extreme right) corresponds to output contact 1 etc. The same information is present if the event is extracted and viewed via PC.

1.2.1.3 Relay alarm conditions

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Any alarm conditions generated by the relays will also be logged as individual events. Table 2 shows examples of some of the alarm conditions and how they appear in the event list:

Alarm condition	Resulting event	
	Event text	Event value
Alarm Status 1 (Alarms 1 - 32) (32 bits)		
Setting Group Via Opto Invalid	Setting Grp Invalid ON/OFF	Bit position 2 in 32 bit field
Protection Disabled	Prot'n Disabled ON/OFF	Bit position 3 in 32 bit field
Frequency Out of Range	Freq out of Range ON/OFF	Bit position 13 in 32 bit field
VTS Alarm	VT Fail Alarm ON/OFF	Bit position 4 in 32 bit field
CB Trip Fail Protection	CB Fail ON/OFF	Bit position 6 in 32 bit field
Alarm Status 2 (Alarms 1 - 32) (32 bits)		
SR User Alarm 1 - 4 (Self Reset)	SR User Alarm 1 - 4 ON/OFF	Bit position 17 - 31 in 32 bit field
MR User Alarm 5 - 16 (Manual Reset)	MR User Alarm 5 - 16 ON/OFF	Bit position 16 - 27 in 32 bit field
Alarm Status 3 (Alarms 1 - 32) (32 bits)		
Battery Fail	Battery Fail ON/OFF	Bit position 0 in 32 bit field
Field Voltage Fail	Field V Fail ON/OFF	Bit position 1 in 32 bit field

Table 2: Alarm conditions

Table 2 shows the abbreviated description that is given to the various alarm conditions and also a corresponding value between 0 and 31. This value is appended to each alarm event in a similar way as for the input and output events previously described. It is used by the event extraction software, such as S1 Agile, to identify the alarm and is therefore invisible if the event is viewed on the LCD. Either ON or OFF is shown after the description to signify whether the particular condition has become operated or has reset.

The User Alarms can be operated from an opto input or a control input using the PSL. They can thus be useful to give an alarm led and message on the LCD display and an alarm indication via the communications of an external condition, for example trip circuit supervision alarm, rotor earth fault alarm. The menu text editor in S1 Agile can be used to edit the user alarm text to give a more meaningful description on the LCD display.

1.2.1.4 Protection element starts and trips

Any operation of protection elements, (either a start or a trip condition) will be logged as an event record, consisting of a text string indicating the operated element and an event value. Again, this value is intended for use by the event extraction software, such as S1 Agile, rather than for the user, and is therefore invisible when the event is viewed on the LCD.

1.2.1.5 General events

A number of events come under the heading of 'General Events' - an example is shown below:

Nature of event	Displayed text in event record	Displayed value
Level 1 password modified, either from user interface, front or rear port.	PW1 modified UI, F, R or R2	0 UI=6, F=11, R=16, R2=38

Table 3: General events

A complete list of the 'General Events' is given in the Relay Menu Database document, *P34x/EN MD*.

1.2.1.6 Fault records

Each time a fault record is generated, an event is also created. The event simply states that a fault record was generated, with a corresponding time stamp.

The viewing of the actual fault record is carried out in the "Select Fault'" cell further down the "VIEW RECORDS" column, which is selectable from up to 5 records. These records consist of fault flags, fault location, fault measurements etc. Also, the time stamp given in the fault record itself will be more accurate than the corresponding stamp given in the event record as the event is logged some time after the actual fault record is generated.

The fault record is triggered from the 'Fault REC. TRIG.' signal assigned in the default programmable scheme logic to relay 3, protection trip. The fault measurements in the fault record are given at the time of the protection start. Also, the fault recorder does not stop recording until any start (DDB 992) or the any trip signals (DDB 674) resets in order to record all the protection flags during the fault.

It is recommended that the triggering contact (relay 3 for example) be 'self reset' and not latching. If a latching contact were chosen the fault record would not be generated until the contact had fully reset.

1.2.1.7 Maintenance reports

Internal failures detected by the self-monitoring circuitry, such as watchdog failure, field voltage failure etc. are logged into a maintenance report. The maintenance report holds up to 10 such 'events' and is accessed from the "Select Report" cell at the bottom of the "VIEW RECORDS" column.

Each entry consists of a self explanatory text string and a 'Type' and 'Data' cell, which are explained in the menu extract at the beginning of this section and in further detail in the Relay Menu Database document *P34x/EN MD*.

Each time a Maintenance Report is generated, an event is also created. The event simply states that a report was generated, with a corresponding time stamp.

1.2.1.8 Setting changes

Changes to any setting within the relay are logged as an event. Two examples are shown in Table 4.

Type of setting change	Displayed text in event record	Displayed value
Control/Support Setting	C & S Changed	22
Group # Change	Group # Changed	#

Table 4: Setting changes

Where # = 1 to 4

Note: Control/Support settings are communications, measurement, CT/VT ratio settings etc, which are not duplicated within the four setting groups. When any of these settings are changed, the event record is created simultaneously. However, changes to protection or disturbance recorder settings will only generate an event once the settings have been confirmed at the 'setting trap'.

1.2.2 Resetting of event/fault records

To delete either the event, fault or maintenance reports, use the "RECORD CONTROL" column.

1.2.3 Viewing event records via S1 Agile support software

When the event records are extracted and viewed on a PC they look slightly different than when viewed on the LCD. The following shows an example of how various events appear when displayed using S1 Agile:

Monday 08 January 2001 18:45:28.633 GMT V<1 Trip A/AB ON

ALSTOM: MiCOM P343

Model Number: P343314B2M0360J

Address: 001 Column: 0F Row: 26

Event Type: Setting event

Event Value: 00000001000000000000000000000000

- Monday 08 January 2001 18:45:28.634 GMT Output Contacts

ALSTOM: MiCOM P343

Model Number: P343314B2M0360J

Address: 001 Column: 00 Row: 21

Event Type: Device output changed state

Event Value: 00000000001100

OFF 0 R1 Trip CB

OFF 1 R2 Trip PrimeMov

ON 2 R3 Any Trip

ON 3 R4 General Alarm

OFF 4 R5 CB Fail

OFF 5 R6 E/F Trip

OFF 6 R7 Volt Trip

OFF 7 R8 Freq Trip

OFF 8 R9 Diff Trip

OFF 9 R10 SysBack Trip

OFF 10 R11 NPS Trip

OFF 11 R12 FFail Trip

OFF 12 R13 Power Trip

OFF 13 R14 V/Hz Trip

- Monday 08 January 2001 18:45:28.633 GMT Voltage Prot Alm ON

ALSTOM: MiCOM P343

Model Number: P343314B2AM0360J

Address: 001 Column: 00 Row: 22

Event Type: Alarm event

Event Value: 00001000000000000000000000000000

OFF 0 Freq out of range

OFF 1 System Split Alm

OFF 2 SG-opto Invalid

OFF 3 Prot'n Disabled

OFF 4 VT Fail Alarm

OFF 5 CTS-1 Fail Alarm

OFF 6 CB Fail

OFF 7 I^ Maint Alarm

OFF 8 I^ Lockout Alarm

OFF 9 CB OPs Maint

OFF 10 CB OPs Lockout

OFF 11 CB Op Time Maint

OFF 12 CB Op Time Lock

OFF 13 Fault Freq Lock

OFF 14 CB Status Alarm

OFF 15 CB Trip Fail

OFF 16 CB Close Fail

OFF 17 Man CB Unhealthy

OFF 18 NPS Alarm

OFF 19 Thermal Alarm

OFF 20 V/Hz Alarm

OFF 21 Field Fail Alarm

OFF 22 RTD Thermal Alm

OFF 23 RTD Open Cct

OFF 24 RTD short Cct

OFF 25 RTD Data Error

OFF 26 RTD Board Fail

OFF 27 Freq Prot Alm

ON 28 Voltage Prot Alm

OFF 29 CTS-2 Fail Alarm

OFF 30 64S R<1 Alarm

OFF 31 User Alarm 3

OFF 31 64S Fail Alarm

The first line gives the description and time stamp for the event, whilst the additional information that is displayed below may be collapsed via the +/– symbol.

For further information regarding events and their specific meaning, refer to the Relay Menu Database document, *P34x/EN MD*. This is a standalone document not included in this manual.

1.2.4 Event filtering

It is possible to disable the reporting of events from all interfaces that supports setting changes. The settings that control the various types of events are in the record control column. The effect of setting each to disabled is as follows:

Menu text	Default setting	Available settings
RECORD CONTROL		
Clear Events	No	No or Yes
Selecting **Yes** will cause the existing event log to be cleared and an event will be generated indicating that the events have been erased.		
Clear Faults	No	No or Yes
Selecting **Yes** will cause the existing fault records to be erased from the relay.		
Clear Maint.	No	No or Yes
Selecting **Yes** will cause the existing maintenance records to be erased from the relay.		
Alarm Event	Enabled	Enabled or Disabled
Disabling this setting means that no event will be generated for all alarms.		
Relay O/P Event	Enabled	Enabled or Disabled
Disabling this setting means that no event will be generated for any change in relay output contact state.		
Opto Input Event	Enabled	Enabled or Disabled
Disabling this setting means that no event will be generated for any change in logic input state.		
General Event	Enabled	Enabled or Disabled
Disabling this setting means that no General Events will be generated. See event record sheet in the Relay Menu Database document, *P34x/EN MD* for list of general events.		
Fault Rec Event	Enabled	Enabled or Disabled
Disabling this setting means that no event will be generated for any fault that produces a fault record.		
Maint. Rec Event	Enabled	Enabled or Disabled
Disabling this setting means that no event will be generated for any maintenance records.		
Protection Event	Enabled	Enabled or Disabled
Disabling this setting means that no event will be generated for any operation of the protection elements.		
Clear Dist Recs	No	No or Yes
Command to clear disturbance record memory.		
DDB 31 - 0	11111111111111111111111111111111	
32 bit setting to enable or disable the event recording for DDBs 0-31. For each bit 1 = event recording Enabled, 0 = event recording Disabled.		

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Menu text	Default setting	Available settings
DDB 2047 - 2016	11111111111111111111111111111111	
32 bit setting to enable or disable the event recording for DDBs 2047 - 2016. For each bit 1 = event recording Enabled, 0 = event recording Disabled. There are similar cells showing 32 bit binary strings for all DDBs from 0 – 2047. The first and last 32 bit binary strings only are shown here.		

Table 5: Record control settings

Note: Some occurrences will result in more than one type of event, e.g. a battery failure will produce an alarm event and a maintenance record event.

If the Protection Event setting is Enabled a further set of settings is revealed which allows the event generation by individual DDB signals to be enabled or disabled.

For further information regarding events and their specific meaning, refer to the Relay Menu Database document *P34x/EN MD*.

1.3 Disturbance recorder

The integral disturbance recorder has an area of memory specifically set aside for record storage. The number of records that may be stored by the relay is dependent upon the selected recording duration. The relay can typically store a minimum of 50 records, each of 1.5 seconds duration (8 analogue channels and 32 digital channels). VDEW relays, however, have the same total record length but the VDEW protocol dictates that only 8 records can be extracted via the rear port. Disturbance records continue to be recorded until the available memory is exhausted, at which time the oldest record(s) are overwritten to make space for the newest one.

The recorder stores actual samples that are taken at a rate of 24 samples per cycle.

Each disturbance record consists of a maximum of 9/12/13/15/15 analog data channels for P342/3/4/5/8 and thirty-two digital data channels. The relevant CT and VT ratios for the analog channels are also extracted to enable scaling to primary quantities.

Note: If a CT ratio is set less than unity, the relay will choose a scaling factor of zero for the appropriate channel.

The "DISTURBANCE RECORDER" menu column is shown in Table 6.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DISTURB RECORDER				
Duration	1.5 s	0.1 s	10.5 s	0.01 s
Overall recording time setting.				
Trigger Position	33.3%	0%	100%	0.1%
Trigger point setting as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.				
Trigger Mode	Single	Single, Extended		
If set to single mode, if a further trigger occurs whilst a recording is taking place, the recorder will ignore the trigger. However, if this has been set to **Extended**, the post trigger timer will be reset to zero, thereby extending the recording time.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Analog. Channel 1	VA (P342-6), VA-1 (P348)	P341-6: Unused, VA, VB, VC, VN1, IA-1, IB-1, IC-1, IN, I Sensitive1, IA-2, IB-2, IC-2, VN2, I Sensitive2, V64S, I64S, Frequency, 64R CL Input Raw (unfiltered), 64R R Fault Raw (unfiltered), 64R R Fault (filtered), C/S voltage, 3 Phase Watts, 3 Phase VArs, 1Ph Sen Watts, 1Ph Sen VArs, 3Ph Sen Watts, 3Ph Sen VArs. P348 only: Unused, VA-1, VB-1, VC-1, VN-1 Derived, VAB-1, VBC-1, VCA-1, VA-2, VB-2, VC-2, IA-1, IB-1, IC-1, IA-2, IB-2, IC-2, I2 CT2, VA-1 RMS, VB-1 RMS, VC-1 RMS, VN-1 Derived RMS, VAB-1 RMS, VBC-1 RMS, VCA-1 RMS, IA-1 RMS, IB-1 RMS, IC-1 RMS, IA-2 RMS, IB-2 RMS, IC-2 RMS, I2 CTS RMS, IN-2 Derived RMS, Frequency, Frequency 2.		
Selects any available analog input to be assigned to this channel.				
Analog. Channel 2	VB (P342-6), VB-1 (P348)	As above.		
Analog. Channel 3	VC (P342-6), VC-1 (P348)	As above.		
Analog. Channel 4	VN1 (P342-6), VN-1 Derived (P348)	As above.		
Analog. Channel 5	IA-1 (P342-8)	As above.		
Analog. Channel 6	IB-1 (P342-8)	As above.		
Analog. Channel 7	IC-1 (P342-8)	As above.		
Analog. Channel 8	I Sensitive (P342-6), IA-2 (P348)	As above.		
Analog. Channel 9	IN (P342-6), IB-2 (P348)	As above.		
Analog. Channel 10	IA-2 (P343-6), IC-2 (P348)	As above.		
Analog. Channel 11	IB-2 (P343-6), Frequency (P348)	As above.		
Analog. Channel 12	IC-2 (P343-6), Frequency 2 (P348)	As above.		
Analog. Channel 13	VN2 (P344/5), Unused (P348)	As above.		
Analog. Channel 14	V64S (P345), Unused (P348)	As above.		
Analog. Channel 15	I64S (P345), Unused (P348)	As above.		
Analog. Channel 16	Unused	As above.		
Analog. Channel 17	Unused	As above.		
Analog. Channel 18	Unused	As above.		
Analog. Channel 19	Unused	As above.		
Analog. Channel 20	Unused	As above.		
Digital Inputs 1 to 32	Relays 1 to 12 and Opto's 1 to 12	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals		
The digital channels may be mapped to any of the opto isolated inputs or output contacts, in addition to a number of internal relay digital signals, such as protection starts, LEDs etc.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
Inputs 1 to 32 Trigger	No Trigger except Dedicated Trip Relay O/P's which are set to Trigger L/H	No Trigger, Trigger L/H, Trigger H/L		
Any of the digital channels may be selected to trigger the disturbance recorder on either a low to high (L/H) or a high to low (H/L) transition.				

Table 6: Disturbance recorder settings

The pre and post fault recording times are set by a combination of the "Duration" and "Trigger Position" cells. "Duration" sets the overall recording time and the "Trigger Position" sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1s post fault recording times.

If a further trigger occurs whilst a recording is taking place, the recorder will ignore the trigger if the **Trigger Mode** has been set to **Single**. However, if this has been set to **Extended**, the post trigger timer will be reset to zero, thereby extending the recording time.

The menu shows each of the analog channels is selectable from the available analog inputs to the relay. The digital channels may be mapped to any of the opto isolated inputs or output contacts, in addition to a number of internal relay digital signals, such as protection starts, LEDs etc. The complete list of these signals may be found by viewing the available settings in the relay menu or via a setting file in S1 Agile. Any of the digital channels may be selected to trigger the disturbance recorder on either a low to high or a high to low transition, via the "Input Trigger" cell. The default trigger settings are that any dedicated trip output contacts (e.g. relay 3) will trigger the recorder.

It is not possible to view the disturbance records locally via the LCD; they must be extracted using suitable software such as S1 Agile. This process is fully explained in the SCADA Communications chapter, *P34x/EN SC*.

1.4 Measurements

The relay produces a variety of both directly measured and calculated power system quantities. These measurement values are updated on a per second basis and can be viewed in the "Measurements" columns (up to three) of the relay or via S1 Agile Measurement viewer. The P34x relay is able to measure and display the following quantities as summarized.

- Phase Voltages and Currents
- Phase to Phase Voltage and Currents
- Sequence Voltages and Currents
- Slip Frequency
- Power and Energy Quantities
- Rms. Voltages and Currents
- Peak, Fixed and Rolling Demand Values

There are also measured values from the protection functions, which are also displayed under the measurement columns of the menu; these are described in the section on the relevant protection function.

1.4.1 Measured voltages and currents

The P341-6 relays produce both phase to ground and phase to phase voltage and current values. They are produced directly from the DFT (Discrete Fourier Transform) used by the relay protection functions and present both magnitude and phase angle measurement.

The P348 produces peak and RMS rotor/stator current values and peak and RMS rotor voltage values.

1.4.2 Sequence voltages and currents

Sequence quantities are produced by the P341-6 relays from the measured Fourier values; these are displayed as magnitude and phase angle values.

The P348 calculates peak sequence stator current values and RMS sequence stator current values using the sum of the samples squared over a cycle of sampled data.

1.4.3 Slip frequency

The P341-6 relays produce a slip frequency measurement by measuring the rate of change of phase angle, between the bus and line voltages, over a one-cycle period. The slip frequency measurement assumes the bus voltage to be the reference phasor.

1.4.4 Power and energy quantities

Using the measured voltages and currents the P341-6 relays calculate the apparent, real and reactive power quantities. These are produced on a phase by phase basis together with three-phase values based on the sum of the three individual phase values. The signing of the real and reactive power measurements can be controlled using the measurement mode setting. The four options are defined in the table below:

Measurement mode	Parameter	Signing
0 (Default)	Export Power	+
	Import Power	–
	Lagging Vars	+
	Leading VArs	–
1	Export Power (Watts)	–
	Import Power (Watts)	+
	Lagging VArs (Import VArs)	+
	Leading Vars (Export Vars)	–
2	Export Power (Watts)	+
	Import Power (Watts)	–
	Lagging VArs (Import VArs)	–
	Leading Vars (Export Vars)	+
3	Export Power (Watts)	–
	Import Power (Watts)	+
	Lagging VArs (Import VArs)	–
	Leading Vars (Export Vars)	+

Table 7: Power modes

In addition to the measured power quantities the relay calculates the power factor on a phase by phase basis in addition to a three-phase power factor.

These power values are also used to increment the total real and reactive energy measurements. Separate energy measurements are maintained for the total exported and imported energy. The energy measurements are incremented up to maximum values of 1000 GWhr or 1000 GVARhr at which point they will reset to zero, it is also possible to reset these values using the menu or remote interfaces using the reset demand cell.

For the energy measurements exporting Watts/VArs gives forward Whr/VArhr and importing Watts/VArs gives reverse Whr/VArhr.

1.4.5 RMS voltages and currents

RMS phase voltage and current values are calculated by the relay using the sum of the samples squared over a cycle of sampled data.

1.4.6 Demand values

The P341-6 relays produce fixed, rolling and peak demand values, using the reset demand menu cell it is possible to reset these quantities via the user interface or the remote communications.

Fixed demand values

The fixed demand value is the average value of a quantity over the specified interval; values are produced for each phase current and for three phase real and reactive power. The fixed demand values displayed by the relay are those for the previous interval, the values are updated at the end of the fixed demand period.

Rolling demand values

The rolling demand values are similar to the fixed demand values, the difference being that a sliding window is used. The rolling demand window consists of a number of smaller sub-periods. The resolution of the sliding window is the sub-period length, with the displayed values being updated at the end of each of the sub-periods.

Peak demand values

Peak demand values are produced for each phase current and the real and reactive power quantities. These display the maximum value of the measured quantity since the last reset of the demand values.

1.4.7 Settings

The following settings under the heading measurement set-up can be used to configure the relay measurement function.

Menu text	Default settings	Available settings
MEASURE'T SETUP		
Default Display	Description	Description/Plant Reference/ Frequency/Access Level/3Ph + N Current/3Ph Voltage/Power/Date and Time
This setting can be used to select the default display from a range of options, note that it is also possible to view the other default displays whilst at the default level using the ⟨ and ⟩ keys. However once the 15 minute timeout elapses the default display will revert to that selected by this setting. P341-8.		
Local Values	Primary	Primary/Secondary
This setting controls whether measured values via the front panel user interface and the front courier port are displayed as primary or secondary quantities. P341-8.		
Remote Values	Primary	Primary/Secondary
This setting controls whether measured values via the rear communication port are displayed as primary or secondary quantities. P341-8.		
Measurement Ref.	VA	VA/VB/VC/IA/IB/IC
Using this setting the phase reference for all angular measurements by the relay can be selected. P341-6.		
Measurement Mode	0	0 to 3 step 1
This setting is used to control the signing of the real and reactive power quantities; the signing convention used is defined section 1.4.4. P341-6.		
Fix Dem Period	30 minutes	1 to 99 minutes step 1 minute
This setting defines the length of the fixed demand window. P341-6.		
Roll Sub Period	30 minutes	1 to 99 minutes step 1 minute
The rolling demand uses a sliding/rolling window. The rolling demand window consists of a number of smaller sub periods (Num Sub Periods). The resolution of the rolling window is the sub period length (Roll Sub Period) with the displayed values being updated at the end of each sub period. P341-6.		
Num Sub Periods	1	1 to 15 step 1
This setting is used to set the number of rolling demand sub periods. P341-6.		

Menu text	Default settings	Available settings
MEASURE'T SETUP		
Remote 2 Values	Primary	Primary/Secondary
This setting controls whether measured values via the 2nd rear communication port are displayed as primary or secondary quantities. P341-8.		

Table 8: Measurement setup settings

1.4.8 Measurement display quantities

There are four "Measurement" columns available in the relay for viewing of measurement quantities. These can also be viewed with S1 Agile as shown below:

1.4.8.1 Measurements 1

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 1				
IA / IA-1 Magnitude	Data. IA. P342/ IA-1. P343-6			
IA / IA-1 Phase Angle	Data. IA. P342/ IA-1. P343-6			
IB / IB-1 Magnitude	Data. IA. P342/ IA-1. P343-6			
IC / IB-1 Phase Angle	Data. IA. P342/ IA-1. P343-6			
IC / IC-1 Magnitude	Data. IA. P342/ IA-1. P343-6			
IC / IC-1 Phase Angle	Data. IA. P342/ IA-1. P343-6			
IN Measured Mag	Data. P342-6			
IN Measured Angle	Data. P342-6			
IN / IN-1 Derived Mag	Data. IN = IA+IB+IC. P342/ IN-1 = IA-1+IB-1+IC-1. P343-6			
IN Derived Angle	Data. P342-6			
I Sen1 Magnitude	Data. P342-6			
I Sen1 Angle	Data. P342-6			
I1 Magnitude	Data. Positive sequence current. P342-6			
I2 magnitude	Data. Negative sequence current. P342-6			
I0 Magnitude	Data. Zero sequence current. P342-6			
IA RMS	Data. P342-6			
IB RMS	Data. P342-6			
IC RMS	Data. P342-6			
IA-1 RMS	Data. P348			
IB-1 RMS	Data. P348			
IC-1 RMS	Data. P348			
IN-2 Derived Mag	Data. IN-2 = IA-2+IB-2+IC-2. P343-6			
VAB Magnitude	Data. P342-6			
VAB Phase Angle	Data. P342-6			
VBC Magnitude	Data. P342-6			
VBC Phase Angle	Data. P342-6			
VCA Magnitude	Data. P342-6			
VCA Phase Angle	Data. P342-6			
VAN Magnitude	Data. P342-6			
VAN Phase Angle	Data. P342-6			
VBN Magnitude	Data. P342-6			
VBN Phase Angle	Data. P342-6			
VCN Magnitude	Data. P342-6			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VCN Phase Angle	Data. P342-6			
VN/VN1 Measured Mag	Data. VN.P342/VNI. P342-6			
VN/VN1 Measured Ang	Data. VN.P342/VNI. P342-6			
VN Derived Mag	Data. VN = VA+VB+VC. P342-6			
V1 Magnitude	Data. Positive sequence voltage. P342-6			
V2 Magnitude	Data. Negative sequence voltage. P342-6			
V0 Magnitude	Data. Zero sequence voltage. P342-6			
VAN RMS	Data. P342-6			
VBN RMS	Data. P342-6			
VCN RMS	Data. P342-6			
I Sen2 Magnitude	Data. P345			
I Sen2 Angle	Data. P345			
Frequency	Data. Stator frequency P342-6, rotor frequency P348			
Frequency2	Data. Stator frequency P348			
I1 Magnitude	Data. Positive sequence current. P342-6			
I1 Phase Angle	P342-6			
I2 Magnitude	Data. Negative sequence current. P342-6			
I2 Phase Angle	Data. P342-6			
I0 Magnitude	Data. Zero sequence current. P342-6			
I0 Phase Angle	Data. P342-6			
V1 Magnitude	Data. Positive sequence voltage. P342-6			
V1 Phase Angle	Data. P342-6			
V2 Magnitude	Data. Negative sequence voltage. P342-6			
V2 Phase Angle	Data. P342-6			
V0 Magnitude	Data. Zero sequence voltage. P342-6			
V0 Phase Angle	Data. P342-6			
VN2 Measured Mag	Data. P344/5. P342-6			
VN2 Measured Ang	Data. P344/5. P342-6			
C/S Voltage Mag	Data. P342-6			
C/S Voltage Ang	Data. P342-6			
CS Gen-Bus Mag	Data. P342-6			
CS Gen-Bus Angle	Data. P342-6			
Slip Frequency	Data. P342-6			
CS Frequency	Data. P342-6			
IA-2 RMS	Data. P348			
IB-2 RMS	Data. P348			
IC-2 RMS	Data. P348			
I2 CT2 RMS	Data. P348			
IA-1 Peak	Data. P348			
IB-1 Peak	Data. P348			
IC-1 Peak	Data. P348			
IA-2 Peak	Data. P348			
IB-2 Peak	Data. P348			
IC-2 Peak	Data. P348			
I2 CT2 Peak	Data. P348			
VA-1 RMS	Data. P348			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VB-1 RMS	Data. P348			
VC-1 RMS	Data. P348			
VN-1 Derived RMS	Data. P348			
VA-1 Peak	Data. P348			
VB-1 Peak	Data. P348			
VC-1 Peak	Data. P348			
VN-1 DerivedPeak	Data. P348			
VAB-1 RMS	Data. P348			
VBC-1 RMS	Data. P348			
VCA-1 RMS	Data. P348			
VAB-1 Peak	Data. P348			
VBC-1 Peak	Data. P348			
VCA-1 Peak	Data. P348			
VA-2 RMS	Data. P348			
VB-2 RMS	Data. P348			
VC-2 RMS	Data. P348			
IN-2 Derived RMS	Data. P348			

Table 9: Measurements 1

1.4.8.2 Measurements 2

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Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 2				
A Phase Watts	Data. P342-6			
B Phase Watts	Data. P342-6			
C Phase Watts	Data. P342-6			
A Phase VARs	Data. P342-6			
B Phase VARs	Data. P342-6			
C Phase VARs	Data. P342-6			
A Phase VA	Data. P342-6			
B Phase VA	Data. P342-6			
C Phase VA	Data. P342-6			
3 Phase Watts	Data. P342-6			
3 Phase VARs	Data. P342-6			
3 Phase VA	Data. P342-6			
NPS Power S2	Data. Negative sequence power, S2 =V2xI2. P342-6			
3Ph Power Factor	Data. P342-6			
APh Power Factor	Data. P342-6			
BPh Power Factor	Data. P342-6			
CPh Power Factor	Data. P342-6			
3Ph WHours Fwd	Data. P342-6			
3Ph WHours Rev	Data. P342-6			
3Ph VArHours Fwd	Data. P342-6			
3Ph VArHours Rev	Data. P342-6			
3Ph W Fix Demand	Data. P342-6			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
3Ph VAr Fix Demand	Data. P342-6			
IA Fixed Demand	Data. P342-6			
IB Fixed Demand	Data. P342-6			
IC Fixed Demand	Data. P342-6			
3Ph W Roll Demand	Data. P342-6			
3Ph VAr Roll Demand	Data. P342-6			
IA Roll Demand	Data. P342-6			
IB Roll Demand	Data. P342-6			
IC Roll Demand	Data. P342-6			
3Ph W Peak Demand	Data. P342-6			
3Ph VAr Peak Demand	Data. P342-6			
IA Peak Demand	Data. P342-6			
IB Peak Demand	Data. P342-6			
IC Peak Demand	Data. P342-6			
Reset Demand	No	No, Yes		N/A
Reset demand measurements command. Can be used to reset the fixed, rolling and peak demand value measurements to 0. P342-6				
NPS Power S2 CT2	Data. Negative sequence power, S2 =V2xI2. P342-6			

Table 10: Measurements 2

1.4.8.3 Measurements 3

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 3				
IA-2 Magnitude	Data. P343-6			
IA-2 Phase Angle	Data. P343-6			
IB-2 Magnitude	Data. P343-6			
IB-1 Phase Angle	Data. P343-6			
IC-2 Magnitude	Data. P343-6			
IC-2 Phase Angle	Data. P343-6			
IA Differential	Data. P343-6. Generator Diff phase A differential current.			
IB Differential	Data. P343-6. Generator Diff phase B differential current.			
IC Differential	Data. P343-6. Generator Diff phase C differential current.			
IA Bias	Data. P343-6. Generator Diff phase A bias current.			
IB Bias	Data. P343-6. Generator Diff phase A bias current.			
IC Bias	Data. P343-6. Generator Diff phase A bias current.			
IREF Diff	Data. Restricted earth fault differential current. P342-6			
IREF Bias	Data. Restricted earth fault bias current. P342-6			
VN 3rd harmonic	Data. 3rd harmonic neutral voltage used by 100% stator earth fault. P343-6.			
NPS Thermal	Data. Negative phase sequence thermal state. P342-6			
Reset NPS Thermal	No	No, Yes		N/A
Reset negative phase sequence thermal state command. Resets NPS Thermal state to 0. P342-6				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
RTD 1	Data. P342-6			
RTD 2-10	Data. P342-6			
RTD Open Cct	00000000			
This menu cell displays the status of the eight RTDs as a binary string, 0 = No Open Circuit, 1 = Open Circuit. The Open Cct alarms are latched. P342-6				
RTD Short Cct	00000000			
This menu cell displays the status of the eight RTDs as a binary string, 0 = No Short Circuit, 1 = Short Circuit. The Short Cct alarms are latched. P342-6				
RTD Data Error	00000000			
This menu cell displays the status of the eight RTDs as a binary string, 0 = No Data Error, 1 = Data Error. The Data Error alarms are latched. P342-6				
Reset RTD Flags	No	No, Yes		N/A
Reset RTD alarms command. Resets latched RTD Open Cct, Short Cct, Data Error alarms. P342-6				
Sen Watts	Data			
Sen VArs	Data			
Sen Power Factor	Data			
Thermal Overload	Data. Thermal state. P342-6			
Reset Thermal O/L	No	No, Yes		N/A
Reset thermal overload command. Resets thermal state to 0. P342-6				
CLIO Input 1	Data. Current loop (transducer) input 1. P342-8			
CLIO Input 2	Data. Current loop (transducer) input 2. P342-8			
CLIO Input 3	Data. Current loop (transducer) input 3. P342-8			
CLIO Input 4	Data. Current loop (transducer) input 4. P342-8			
F Band1 Time(s)	Data. Turbine abnormal frequency accumulated time in frequency band 1. P342-6			
Reset Freq Band1	No	No, Yes		N/A
Reset frequency band 1 command. Resets accumulated time of frequency band 1 to 0 s. P342-6				
F Band2-6 Time(s)	Data. Turbine abnormal frequency, accumulated time in frequency band 2-6. P342-6			
Reset Freq Band2-6	No	No, Yes		N/A
Reset frequency band 2-6 command. Resets accumulated time of frequency band 2-6 to 0 s. P342-6				
Reset Freq Bands	No	No, Yes		N/A
Reset frequency bands command. Resets accumulated time of all frequency bands (1-6) to 0 s. P342-6				
df/dt	Data. P342-6			
Volts/Hz	Data. P342-6			
64S V Magnitude	Data. 100% stator earth fault 20 Hz voltage. P345.			
64S I Magnitude	Data. 100% stator earth fault 20 Hz current. P345.			
64S I Angle	Data. 100% stator earth fault 20 Hz current angle with respect to the voltage. P345.			
64S R secondary	Data. 100% stator earth fault secondary resistance. P345.			
64S R primary	Data. 100% stator earth fault primary resistance. P345.			
64R CL Input	Data. Rotor earth fault current loop input current (0-20 mA). P342-6			
64R R Fault	Data. Rotor earth fault primary resistance from current loop input connected to P391. P342-6			
IA Diff PU	Data. Transformer Diff phase A per unit differential current. P343-6			
IB Diff PU	Data. Transformer Diff phase B per unit differential current. P343-6			
IC Diff PU	Data. Transformer Diff phase C per unit differential current. P343-6			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
IA Bias PU	Data. Transformer Diff phase A per unit bias current. P343-6			
IB Bias PU	Data. Transformer Diff phase A per unit bias current. P343-6			
IC Bias PU	Data. Transformer Diff phase A per unit bias current. P343-6			
IA Diff 2H	Data. Transformer Diff phase A 2nd harmonic current. P343-6			
IB Diff 2H	Data. Transformer Diff phase B 2nd harmonic current. P343-6			
IC Diff 2H	Data. Transformer Diff phase C 2nd harmonic current. P343-6			
IA Diff 5H	Data. Transformer Diff phase A 5th harmonic current. P343-6			
IB Diff 5H	Data. Transformer Diff phase B 5th harmonic current. P343-6			
IC Diff 5H	Data. Transformer Diff phase C 5th harmonic current. P343-6			
CT2 I1 Mag	Data. P343-6			
CT2 I1 Angle	Data. P343-6			
CT2 I2 Mag	Data. P343-6			
CT2 I2 Angle	Data. P343-6			
CT2 I0 Mag	Data. P343-6			
CT2 I0 Angle	Data. P343-6			
CT1 I2/I1	Data. P343-6			
CT2 I2/I1	Data. P343-6			
ZA Mag	Data. A Phase impedance			

Table 11: Measurements 3

1.4.8.4 Measurements 4

MR

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 3				
Hot Spot T	Data. Hot spot temperature. P342-6			
Top Oil T	Data. Top oil temperature. P342-6			
Reset Thermal	No	No, Yes		N/A
Reset thermal overload command. Resets thermal state to 0. P342-6				
Ambient T	Data. Ambient temperature. P342-6			
TOL Pretrip left	Data. Top oil (TOL) time left to trip. P342-6			
LOL status	Data. Accumulated loss of life (LOL) measurement in hours. P342-6			
Reset LOL	No	No, Yes		N/A
Reset loss of life LOL command. Resets LOL to 0. P342-6				
Rate of LOL	Data. Rate of loss of life (LOL) in %. P342-6			
LOL Ageing Fact	Data. Ageing acceleration factor (FAA). P342-6			
Lres at Design T	Data. Residual life at reference hottest spot temperature. P342-6			
FAA,m	Data. Mean ageing acceleration factor (FAA,m). P342-6			
Lres at FAA,m	Data. Residual life in hours at FAA,m (Lres(FAA,m)). P342-6			
Counter 1	Data. Counter 1 value			
Counter 2-16	Data. Counter 2-16 value			
Reset Counter1	No	No, Yes		N/A
Reset Counter2-16	No	No, Yes		N/A

Table 12: Measurements 4

MR

FIRMWARE DESIGN

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Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 RELAY SYSTEM OVERVIEW

1.1 Hardware overview

The relay hardware is made up of several modules from a standard range. Some modules are essential while others are optional depending on the user's requirements.

All modules are connected by a parallel data and address bus which allows the processor board to send and receive information to and from the other modules as required.

The different modules that can be present in the relay are as follows:

1.1.1 Processor board

The processor board performs all calculations for the relay and controls the operation of all other modules in the relay. The processor board also contains and controls the user interfaces (LCD, LEDs, keypad and communication interfaces).

1.1.2 Input module

The input module converts the information contained in the analog and digital input signals into a format suitable for processing by the processor board. The standard input module consists of two boards; a transformer board to provide electrical isolation and a main input board which provides analog to digital conversion and the isolated digital inputs.

1.1.3 Power supply module

The power supply module provides a power supply to all of the other modules in the relay, at three different voltage levels. It also provides the EIA(RS)485 electrical connection for the rear communication port. The second board of the power supply module contains the relays that provide the output contacts.

1.1.4 RTD board

This optional board can be used to process the signals from up to 10 resistance temperature detectors (RTDs) to measure the winding and ambient temperatures.

1.1.5 IRIG-B modulated or unmodulated board (optional)

This board, which is optional, can be used where an IRIG-B signal is available to provide an accurate time reference for the relay. There is also an option on this board to specify a fiber optic or Ethernet rear communication port.

All modules are connected by a parallel data and address bus that allows the processor board to send and receive information to and from the other modules as required. There is also a separate serial data bus for conveying sample data from the input module to the processor. Figure 1 shows the modules of the relay and the flow of information between them.

1.1.6 Second rear comms. board

The optional second rear port is designed typically for dial-up modem access by protection engineers and operators, when the main port is reserved for SCADA traffic. Communication is through one of three physical links; K-Bus, EIA(RS)485 or EIA(RS)232. The port supports full local or remote protection and control access by S1 Agile software. The second rear port is also available with an on board IRIG-B input.

1.1.7 Ethernet board

This is a mandatory board for IEC 61850 station bus and DNP 3.0 over Ethernet enabled relays. It provides network connectivity through either copper or fiber media at rates of 10 Mb/s (copper only) or 100 Mb/s or a 100 Mb/s fiber redundant Ethernet port. There is also an option on this board to specify IRIG-B port (modulated or un-modulated). This single/redundant port Ethernet board, the IRIG-B board mentioned in section 1.1.5 and second rear comms board mentioned in section 1.1.6 are mutually exclusive as they all utilize slot A within the relay case.

The P348 includes an IEC 61850-9-2 LE process bus Ethernet board to receive sampled values of current and voltage, see section 0.

All modules are connected by a parallel data and address bus which allows the processor board to send and receive information to and from the other modules as required.

There is also a separate serial data bus for conveying sample data from the input module to the processor. Figure 1 shows the modules of the relay and the flow of information between them.

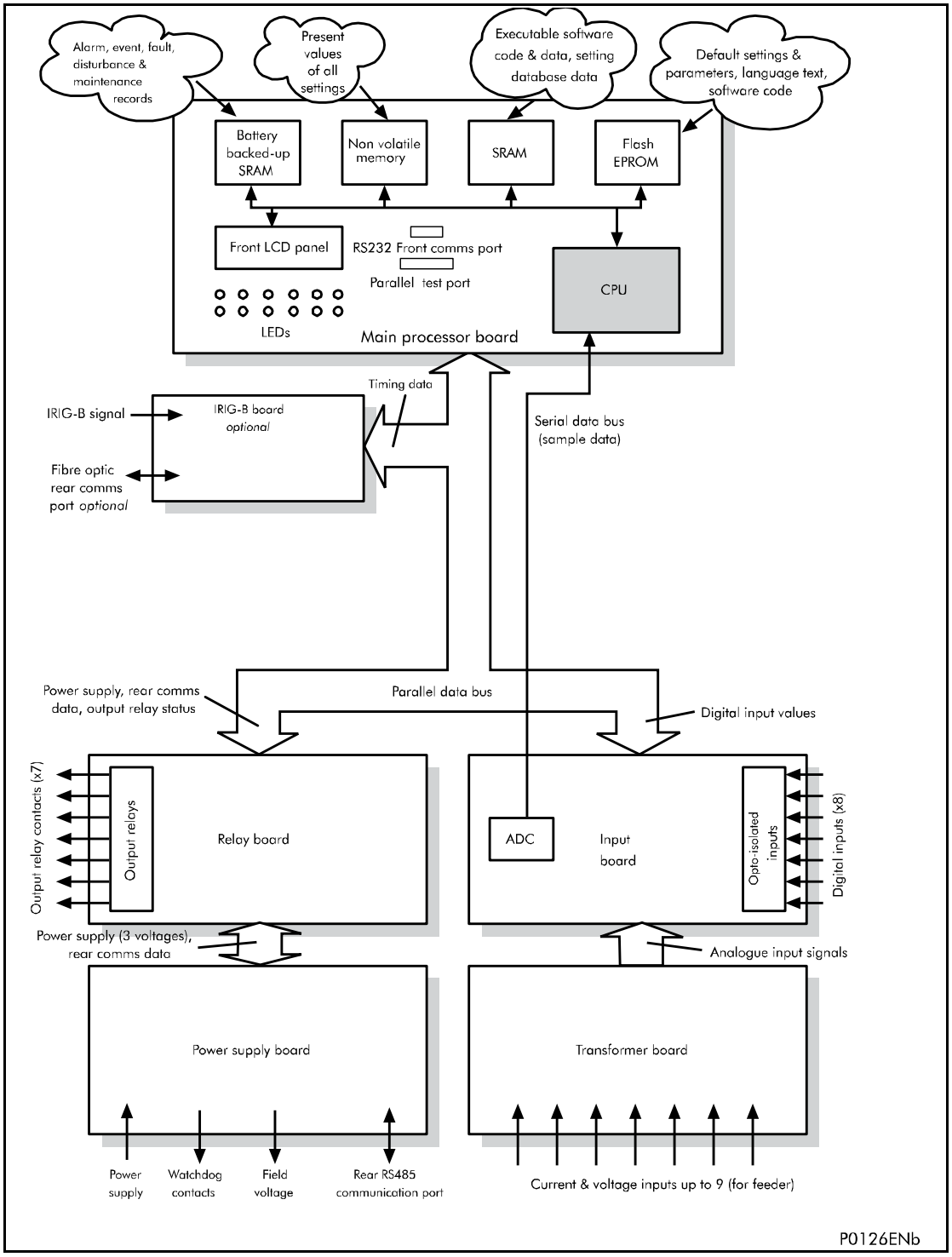


Figure 1: Relay modules and information flow

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1.1.8 P391 rotor earth fault injection, coupling and measurment unit

The P391 rotor earth fault protection device injects a DC voltage into the rotor circuit; the polarity of the voltage is reversed at low frequencies and the frequency is selectable by the user through a jumper link inside the device, 0.25 Hz, 0.5 Hz, 1 Hz. The voltage source is coupled to the excitation circuit via high resistance resistors. It is connected to the earthing brush of the rotor via a low resistance measuring shunt. The P391 includes a watchdog contact to indicate any fault in the device. It also includes a 0-20 mA current loop output of the resistance measurement which is connected to the P34x 0-20 mA current loop input to provide rotor earth fault alarm and trip stages.

1.2 Software overview

The software for the relay can be split into four elements; the real-time operating system, the system services software, the platform software and the protection and control software. These four elements are not distinguishable to the user, and are all processed by the same processor board. The distinction between the four parts of the software is explained in the following sections.

1.2.1 Real-time operating system

The real time operating system provides a framework for the different parts of the relay's software to operate in. The software is split into tasks. The real-time operating system schedules the processing of these tasks so that they are carried out at the correct time and in the correct priority. The operating system also exchanges of information between tasks in the form of messages.

1.2.2 System services software

The system services software provides the low-level control of the relay hardware. For example, the system services software controls the boot of the relay's software from the non-volatile flash EPROM memory at power-on, and provides driver software for the user interface through the LCD and keypad, and through the serial communication ports. The system services software provides an interface layer between the control of the relay's hardware and the rest of the relay software.

1.2.3 Platform software

The platform software deals with the management of the relay settings, the user interfaces and logging of event, alarm, fault and maintenance records. All of the relay settings are stored in a database in the relay. This database is directly compatible with Courier communications. For all other interfaces (such as the front panel keypad and LCD interface, MODBUS, IEC 60870-5-103, IEC 61850 and DNP3.0) the platform software converts the information from the database into the format required. The platform software notifies the protection & control software of all settings changes and logs data as specified by the protection & control software.

1.2.4 Protection & control software

The protection and control software performs the calculations for all of the protection algorithms of the relay. This includes digital signal processing such as Fourier filtering and ancillary tasks such as the disturbance recorder. The protection & control software interfaces with the platform software for settings changes and logging of records, and with the system services software for acquisition of sample data and access to output relays and digital opto-isolated inputs.

1.2.5 Disturbance recorder

The analog values and logic signals are routed from the protection and control software to the disturbance recorder software. The platform software interfaces to the disturbance recorder to allow extraction of the stored records.

2 HARDWARE MODULES

The relay is based on a modular hardware design where each module performs a separate function. This section describes the functional operation of the various hardware modules.

2.1 Processor board

The main processor board is based around a floating point, 32-bit Digital Signal Processor (DSP). It performs all calculations and controls the operation of all other modules in the IED, including the data communication and user interfaces. This board is the only board that does not fit into one of the slots. It resides in the front panel and is connected to the rest of the system via an internal ribbon cable.

The LCD and LEDs are mounted on the processor board along with the front panel communication ports. All serial communication is handled using a Field Programmable Gate Array (FPGA).

The memory provided on the main processor board is split into two categories, volatile and non-volatile: the volatile memory is fast access SRAM which is used for the storage and execution of the processor software, and data storage as required during the processor's calculations. The non-volatile memory is sub-divided into two groups:

- Flash memory for non-volatile storage of software code, text and configuration data including the present setting values
- Battery-backed SRAM for the storage of disturbance, event, fault and maintenance record data

2.2 Internal communication buses

The relay has two internal buses for the communication of data between different modules. The main bus is a parallel link that is part of a 64-way ribbon cable. The ribbon cable carries the data and address bus signals in addition to control signals and all power supply lines. Operation of the bus is driven by the main processor board that operates as a master while all other modules within the relay are slaves.

The second bus is a serial link that is used exclusively for communicating the digital sample values from the input module to the main processor board. The DSP processor has a built-in serial port that is used to read the sample data from the serial bus. The serial bus is also carried on the 64-way ribbon cable.

2.3 Input module

The input module provides the interface between the relay processor board(s) and the analog and digital signals coming into the relay. The input module of P342 consists of two PCBs; the main input board and the transformer board. This relay provides four voltage inputs and five current inputs. The P343/4/5/6 input module contains an additional transformer board, providing a total of 4/5/7 voltage inputs and 8 or 10 current inputs. The P344 input module is the same as the P343/6 except it includes an additional voltage input, so providing five voltage inputs and eight current inputs. The P345 input module is the same as the P344 except it includes an additional 20 Hz current and 20 Hz voltage input for 100% stator earth fault protection, a dedicated voltage input for check synchronising and an additional sensitive current input for wattmetric sensitive power protection. The P348 uses sampled values of current and voltage from an IEC 61850-9-2 LE Ethernet port, see section 0 for more information.

2.3.1 Transformer board

The transformer board holds up to four voltage transformers (VTs) and up to five current transformers (CTs). The auxiliary transformer board adds up to five more CTs and two more VTs. The current inputs accept either 1A or 5A nominal current (menu and wiring options) and the voltage inputs can be specified for either 110 V or 440 V nominal voltage (order option). The transformers are used both to step-down the currents and voltages to levels appropriate to the relay's electronic circuitry and to provide effective isolation between the relay and the power system. The connection arrangements of both the current and voltage

transformer secondaries provide differential input signals to the main input board to reduce noise.

2.3.2 Input board

The main input board is shown as a block diagram in Figure 2. It provides the circuitry for the digital input signals and the analog-to-digital conversion for the analog signals. It takes the differential analog signals from the CTs and VTs on the transformer board(s), converts these to digital samples and transmits the samples to the main processor board through the serial data bus. On the input board the analog signals are passed through an anti-alias filter before being multiplexed into a single analog to digital converter chip. The A-D converter provides 16-bit resolution and a serial data stream output. The digital input signals are opto isolated on this board to prevent excessive voltages on these inputs causing damage to the relay's internal circuitry.

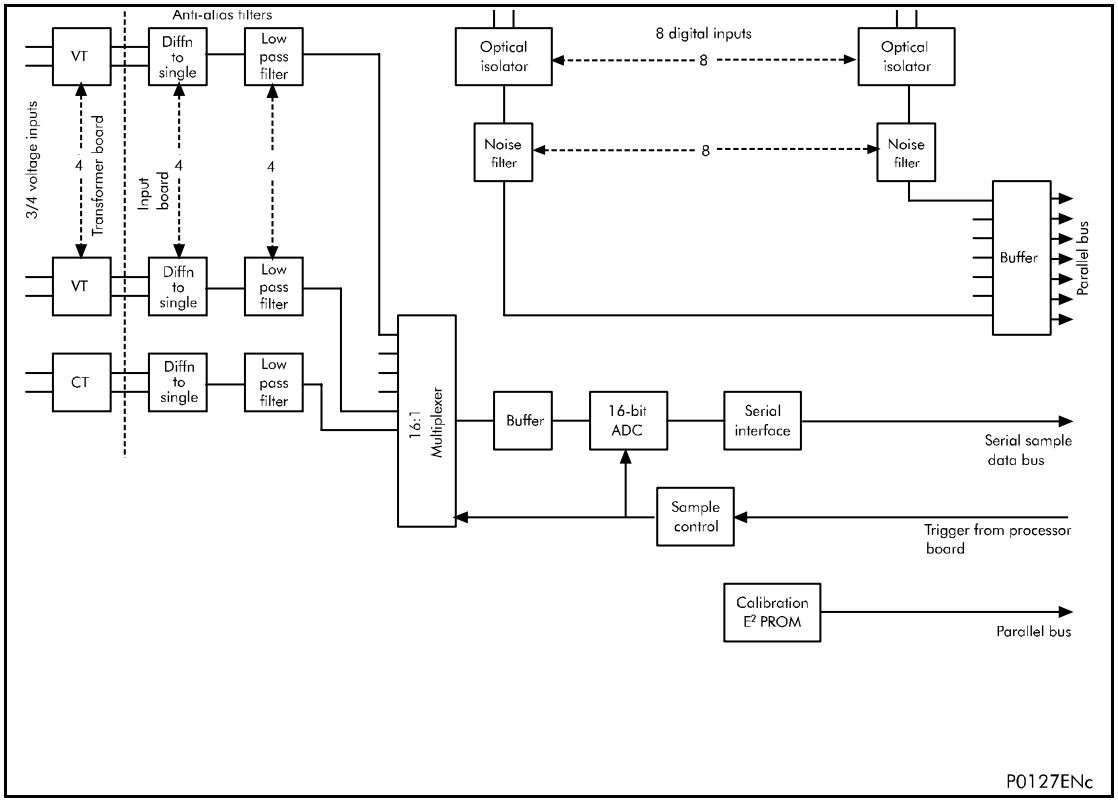


Figure 2: Main input board

The signal multiplexing allows 20 analog channels to be sampled with up to 10 current inputs and 7 voltage inputs to be accommodated. The 3 spare channels are used to sample 3 different reference voltages for the purpose of continually checking the operation of the multiplexer and the accuracy of the A-D converter. The sample rate is maintained at 24 samples per cycle of the power waveform by a logic control circuit that is driven by the frequency tracking function on the main processor board. The calibration non-volatile memory holds the calibration coefficients that are used by the processor board to correct for any amplitude or phase error introduced by the transformers and analog circuitry.

The other function of the input board is to read the signals present on the digital inputs and present this to the parallel data bus for processing. The input board holds 8 optical isolators for the connection of up to eight digital input signals. The opto-isolators are used with the digital signals for the same reason as the transformers with the analog signals; to isolate the relay's electronics from the power system environment. The input board provides some hardware filtering of the digital signals to remove unwanted noise before buffering the signals for reading on the parallel data bus. Depending on the relay model, more than 8 digital input signals can be accepted by the relay. This is achieved by the use of an additional opto-board that contains the same provision for 8 isolated digital inputs as the main input board, but does not contain any of the circuits for analog signals which are provided on the main input board.

2.3.3 Universal opto isolated logic inputs

The P34x series relays have universal opto isolated logic inputs that can be programmed for the nominal battery voltage of the circuit of which they are a part. This allows different voltages for different circuits such as signaling and tripping. From software version 30 onwards they can also be programmed as Standard 60% - 80% or 50% - 70% to satisfy different operating constraints.

Threshold levels are as follows:

Nominal battery voltage (Vdc)	Standard 60% - 80%		50% - 70%	
	No operation (logic 0) Vdc	Operation (logic 1) Vdc	No operation (logic 0) Vdc	Operation (logic 1) Vdc
24/27	<16.2	>19.2	<12.0	>16.8
30/34	<20.4	>24.0	<15.0	>21.0
48/54	<32.4	>38.4	<24.0	>33.6
110/125	<75.0	>88.0	<55.0	>77.0
220/250	<150.0	>176.0	<110	>154

Table 1: Threshold levels

This lower value eliminates fleeting pick-ups that may occur during a battery earth fault, when stray capacitance may present up to 50% of battery voltage across an input.

Each input also has selectable filtering which can be utilized. This allows use of a pre-set filter of ½ cycle which renders the input immune to induced noise on the wiring: although this method is secure it can be slow, particularly for intertripping. This can be improved by switching off the ½ cycle filter in which case one of the following methods to reduce ac noise should be considered. The first method is to use double pole switching on the input, the second is to use screened twisted cable on the input circuit.

New opto input boards have been designed and implemented in the P34xxxxxxxxxxM/P relays to satisfy the most modern and stringent surge withstand requirements. The new opto-input boards:

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- Provide immunity to spurious pickup for battery earth fault conditions, without the need of parallel resistors or time delays
- Provide immunity to wiring pickup (induced switching voltages) equivalent to that of a high-burden trip relay
- Allows the connection of wiring beyond the panel where screening may be insufficient or even missing
- Allows connection where spacing between DC wiring and CT circuits or primary conductors is less than the traditional recommended separation distances
- Maximises "contact wetting" capability. This is the ability to break down oxidisation on external initiating contacts, which may not have operated for some time
- Ensures a clean switch on (minimises chatter)
- Provides active balancing of the applied voltage when two inputs are used in series for trip circuit supervision, providing a completely self-contained trip circuit supervision solution.
- Provides compliance with the latest IEC EMC surge standards, which are much harsher than previously. The new standards use capacitor coupled discharge (peak + decaying exponential) tests, compared with the old standards which used spark gap discharge (peak only) tests.
- Provides compliance with the very harsh UK ESI48-4EB2 tests for the first time, without using external resistors to sink the energy. The opto-inputs are as immune to capacitive discharge as a hinged armature trip relay

- Provides programmable opto-input thresholds, which in combination with the other features, eliminates the risk of mal-operation for any earth faults in the battery circuit

2.4 Power supply module (including output relays)

The power supply module contains two boards, one for the power supply unit itself and the other for the output relays. The power supply board also contains the input and output hardware for the rear communication port which provides an EIA(RS)485 communication interface.

A new power supply module is implemented in the P34xxxxxxxxxxM/P relays. In the new PSU modules the 48V field voltage used to drive opto inputs has been removed. For the older models, the field voltage occupies terminals F/J/M 7, 8, 9 and 10 (dependant on the model) of the power supply board. For the new models, it is important NOT to make any connections to these terminals.

2.4.1 Power supply board (including EIA(RS)485 communication interface)

One of three different configurations of the power supply board can be fitted to the relay. This will be specified at the time of order and depends on the nature of the supply voltage that will be connected to the relay. The three options are shown in Table 2.

Nominal dc range	Nominal ac range
24/48 V	DC only
48/110 V	30/100 Vrms
110/250 V	100/240 Vrms

Table 2: Power supply options

The output from all versions of the power supply module are used to provide isolated power supply rails to all of the other modules within the relay. Three voltage levels are used in the relay: 5.1 V for all of the digital circuits, ±16 V for the analog electronics such as on the input board, and 22 V for driving the output relay coils and the RTD board if fitted. All power supply voltages including the 0 V earth line are distributed around the relay through the 64-way ribbon cable.

The two other functions provided by the power supply board are the EIA(RS)485 communications interface and the watchdog contacts for the relay. The EIA(RS)485 interface is used with the relay's rear communication port to provide communication using one of either Courier, MODBUS, or IEC60870-5-103 or DNP3.0 protocols. The EIA(RS)485 hardware supports half-duplex communication and provides optical isolation of the serial data being transmitted and received. All internal communication of data from the power supply board is conducted through the output relay board that is connected to the parallel bus.

The watchdog facility provides two output relay contacts, one normally open and one normally. These are driven by the main processor board and indicate that the relay is in a healthy state.

The power supply board incorporates inrush current limiting. This limits the peak inrush current, during energization, to approximately 10A.

2.4.2 Output relay board

There are 2 versions of the output relay board one with seven relays, three normally open contacts and four changeover contacts and one with eight relays, six normally open contacts and two changeover contacts.

For relay models with suffix A hardware, only the 7 output relay boards were available. For equivalent relay models in suffix B hardware or greater the base numbers of output contacts, using the 7 output relay boards, is being maintained for compatibility. The 8 output relay board is only used for new relay models or existing relay models available in new case sizes or to provide additional output contacts to existing models for suffix issue B or greater hardware.

Note: The model number suffix letter refers to the hardware version.

The relays are driven from the 22 V power supply line. The relays' state is written to or read from using the parallel data bus. Depending on the relay model, more than seven output contacts may be provided, through the use of up to three extra relay boards. Each additional relay board provides a further seven or eight output relays.

2.4.3 High break relay board

One 'high break' output relay board consisting of four normally open output contacts is available for the P342 and one or two boards is available for the P343/4/5/6 as an option.

This board contains a hybrid of MOSFET solid state devices (SSD) in parallel with high capacity relay output contacts. The MOSFET has a varistor across it to provide protection which is required when switching off inductive loads as the stored energy in the inductor causes a reverse high voltage which could damage the MOSFET.

When there is a control input command to operate an output contact the miniature relay is operated at the same time as the SSD. The miniature relay contact closes in nominally 3.5 mS and is used to carry the continuous load current; the SSD operates in <0.2 ms and is switched off after 7.5 mS. When the control input resets to open the contacts, the SSD is again turned on for 7.5 mS. The miniature relay resets in nominally 3.5 ms before the SSD and so the SSD is used to break the load. The SSD absorbs the energy when breaking inductive loads and so limits the resulting voltage surge. This contact arrangement is for switching dc circuits only. As the SSD comes on very fast (<0.2 ms) then these high break output contacts have the added advantage of being very fast operating.

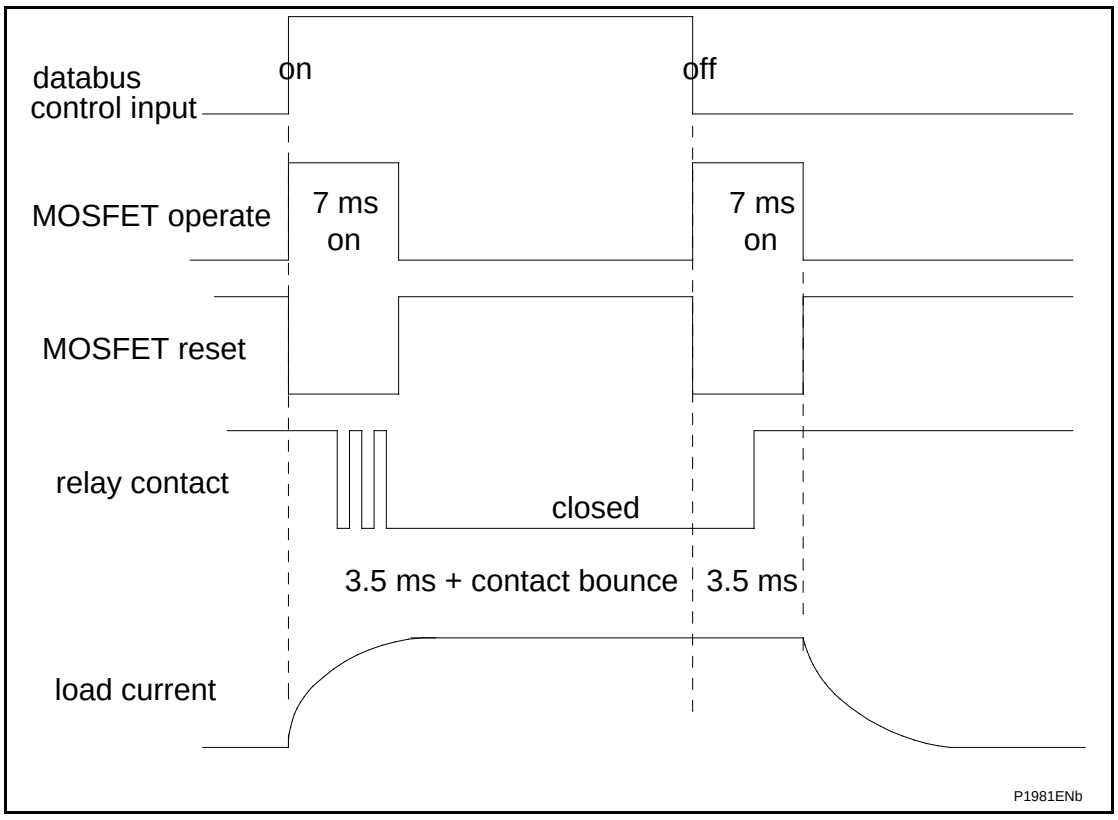


Figure 3: High break contact operation

2.4.3.1 High break contact applications

1. Efficient scheme engineering

In traditional hardwired scheme designs, high break capability could only be achieved using external electromechanical trip relays. External MVAJ tripping relays can be used or the new high break contacts inside MiCOM relays can be used - reducing panel space.

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2. Accessibility of CB auxiliary contacts

Common practice is to use circuit breaker 52a (CB Closed) auxiliary contacts to break the trip coil current on breaker opening, thus easing the duty on the protection contacts. In cases such as operation of disconnectors, or retrofitting, it may be that 52a contacts are either unavailable or unreliable. High break contacts can be used to break the trip coil current in these applications.

3. Breaker fail

The technique to use 52a contacts in trip circuits was described above. However, in the event of failure of the local circuit breaker (stuck breaker), or defective auxiliary contacts (stuck contacts), the 52a contact action is incorrect. The interrupting duty at the local breaker then falls on the relay output contacts which may not be rated to perform this duty. MiCOM high break contacts will avoid the risk of burnt relay contacts.

4. Initiation of teleprotection

The high break contacts also offer fast making. This can provide faster tripping: additionally, fast keying of teleprotection is a benefit. Fast keying bypasses the usual contact operation time, such that permissive, blocking and intertrip commands can be routed faster.

2.5 RTD board

The RTD (Resistance Temperature Detector) board is an order option. It is used to monitor the temperature readings from up to ten PT100 RTDs that are each connected using a 3-wire connection. The board is powered from the 22 V power rail that is used to drive the output relays. The RTD board includes two redundant channels that are connected to high stability resistors to provide reference readings. These are used to check the operation of the RTD board. The temperature data is read by the processor via the parallel data bus, and is used to provide thermal protection of the generator windings.

2.6 IRIG-B board modulated or unmodulated board (optional)

The IRIG-B board is an order option that can be fitted to provide an accurate timing reference for the relay. This can be used wherever an IRIG-B signal is available. The IRIG-B signal is connected to the board via a BNC connector on the back of the relay. The timing information is used to synchronize the relay's internal real-time clock to an accuracy of 1 ms. The internal clock is then used for the time tagging of the event, fault maintenance and disturbance records.

The IRIG-B board can also be specified with a fiber optic or Ethernet rear communication port.

2.7 Second rear communications board

For relays with Courier, MODBUS, IEC60870-5-103 or DNP3.0 protocol on the first rear communications port there is the hardware option of a second rear communications port, which will run the Courier language. This can be used over one of three physical links: twisted pair K-Bus (non-polarity sensitive), twisted pair EIA(RS)485 (connection polarity sensitive) or EIA(RS)232.

The second rear comms. Board, Ethernet and IRIG-B boards are mutually exclusive since they use the same hardware slot. For this reason two versions of second rear comms. and Ethernet boards are available; one with an IRIG-B input and one without. The physical layout of the second rear comms. board is shown in Figure 4.

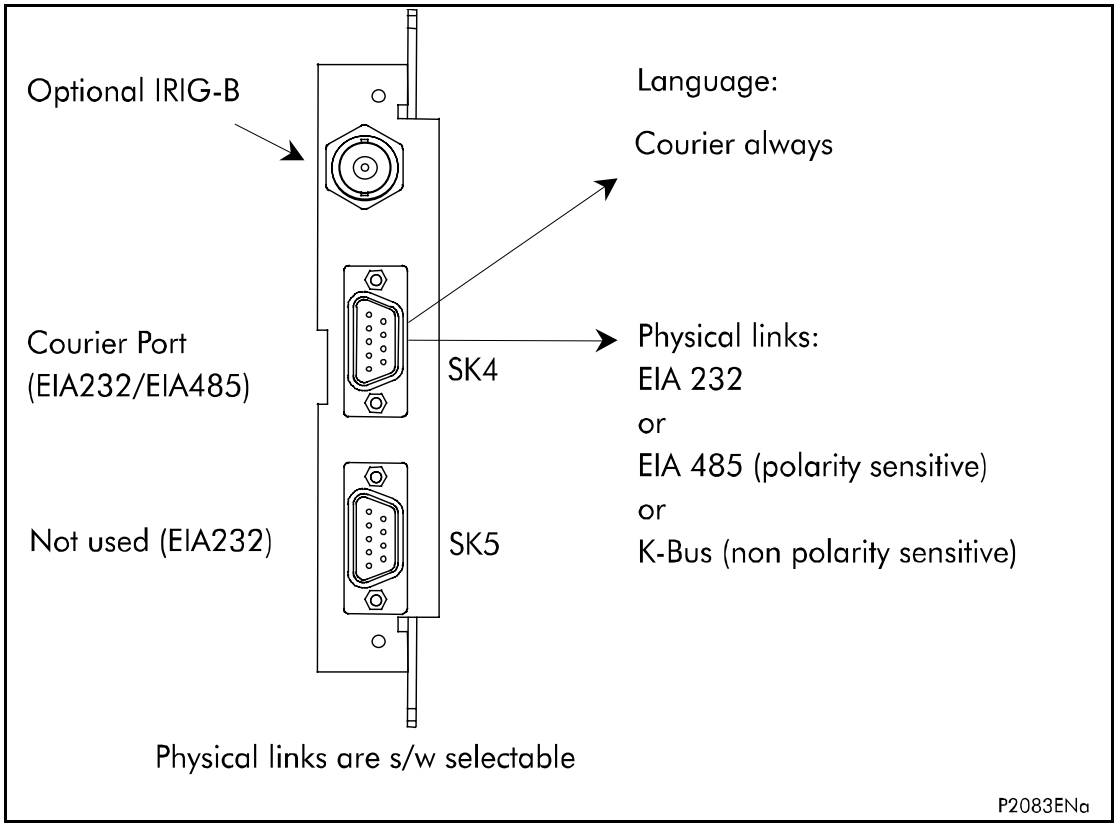


Figure 4: Second rear comms. port

2.8 IEC 61850-8-1 Ethernet board

For IEC 61850 station bus communications and DNP 3.0 over Ethernet two boards are available, the single Ethernet board (ZN0049) and the redundant Ethernet board (ZN0071). Both are required for communications but the dual redundant Ethernet board allows an alternative path to be always available, providing bumpless redundancy.

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The optional single Ethernet board (ZN0049) has three variants which support the IEC 61850 and DNP 3.0 implementation:

1. 100 Mbits/s Fiber Optic + 10/100 Mbits/s Copper
2. 100 Mbits/s Fiber Optic + 10/100 Mbits/s Copper + modulated IRIG-B
3. 100 Mbits/s Fiber Optic + 10/100 Mbits/s Copper + unmodulated IRIG-B

The single Ethernet port card is fitted into Slot A of the relay, which is the optional communications slot. Each Ethernet card has a unique MAC address used for Ethernet communications. This is printed on the rear of the card, alongside the Ethernet sockets.

The 100 Mbits/s Fiber Optic ports use ST® type connectors and are suitable for 1300 nm multi-mode fiber type.

The single Ethernet port board has copper ports using RJ45 type connectors. When using copper Ethernet, it is important to use Shielded Twisted Pair (STP) or Foil Twisted Pair (FTP) cables, to shield the IEC 61850 communications against electromagnetic interference. The RJ45 connector at each end of the cable must be shielded, and the cable shield must be connected to this RJ45 connector shield, so that the shield is grounded to the relay case. Both the cable and the RJ45 connector at each end of the cable must be Category 5 minimum, as specified by the IEC 61850 standard. It is recommended that each copper Ethernet cable is limited to a maximum length of three meters and confined within one bay/cubicle.

When using IEC 61850 and DNP 3.0 communications through the Ethernet card, the rear EIA(RS)485 and front EIA(RS)232 ports are also available for simultaneous use, both using the Courier protocol.

The physical layout of the single port Ethernet board is shown in Figure 5.

Industrial network failure can be disastrous. Redundancy provides increased security and reliability, but also devices can be added to or removed from the network without network downtime.

The following list shows General Electric's implementation of Ethernet redundancy, which has eight variants with embedded IEC 61850 and DNP 3.0 over Ethernet, plus SHP, RSTP, DHP and PRP redundancy protocols.

1. Self Healing Protocol (SHP) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST® connector) and modulated IRIG-B input.
2. Self Healing Protocol (SHP) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST® connector) and unmodulated IRIG-B input.

   Note: Both of these boards offer compatibility with C264-SWR202 and H35x multi-mode switches. Self healing Protocol is a General Electric proprietary solution providing extremely fast recovery time.

3. Rapid Spanning Tree Protocol (RSTP IEEE 802.1D 2004) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST® connector) and modulated IRIG-B input.
4. Rapid Spanning Tree Protocol (RSTP IEEE 802.1D 2004) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST® connector) and unmodulated IRIG-B input.

   Note: Both of these boards offer the RSTP protocol.

5. Dual Homing Protocol (DHP) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST® connector) and modulated IRIG-B input.
6. Dual Homing Protocol (DHP) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST® connector) and unmodulated IRIG-B input.

   Note: Both of these boards offer compatibility with C264-SWD202 and H36x multi-mode switches. Dual Homing Protocol is a General Electric proprietary solution providing bumpless redundancy to the IED.

7. Parallel Redundancy Protocol (PRP) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST® connector) and modulated IRIG-B input.
8. 8. Parallel Redundancy Protocol (PRP) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST® connector) and unmodulated IRIG-B input.

   Note: Both of these boards offer the PRP protocol (IEC 62439-3).

The redundant Ethernet board is fitted into Slot A of the IED, which is the optional communications slot. Each Ethernet board has two MAC addresses, one for the managed embedded switch and one for the IED. The MAC address of the IED is printed on the rear panel of the IED. See the Redundant Ethernet Board User Guide, *Px4x/EN REB* for more information on redundant Ethernet communications.

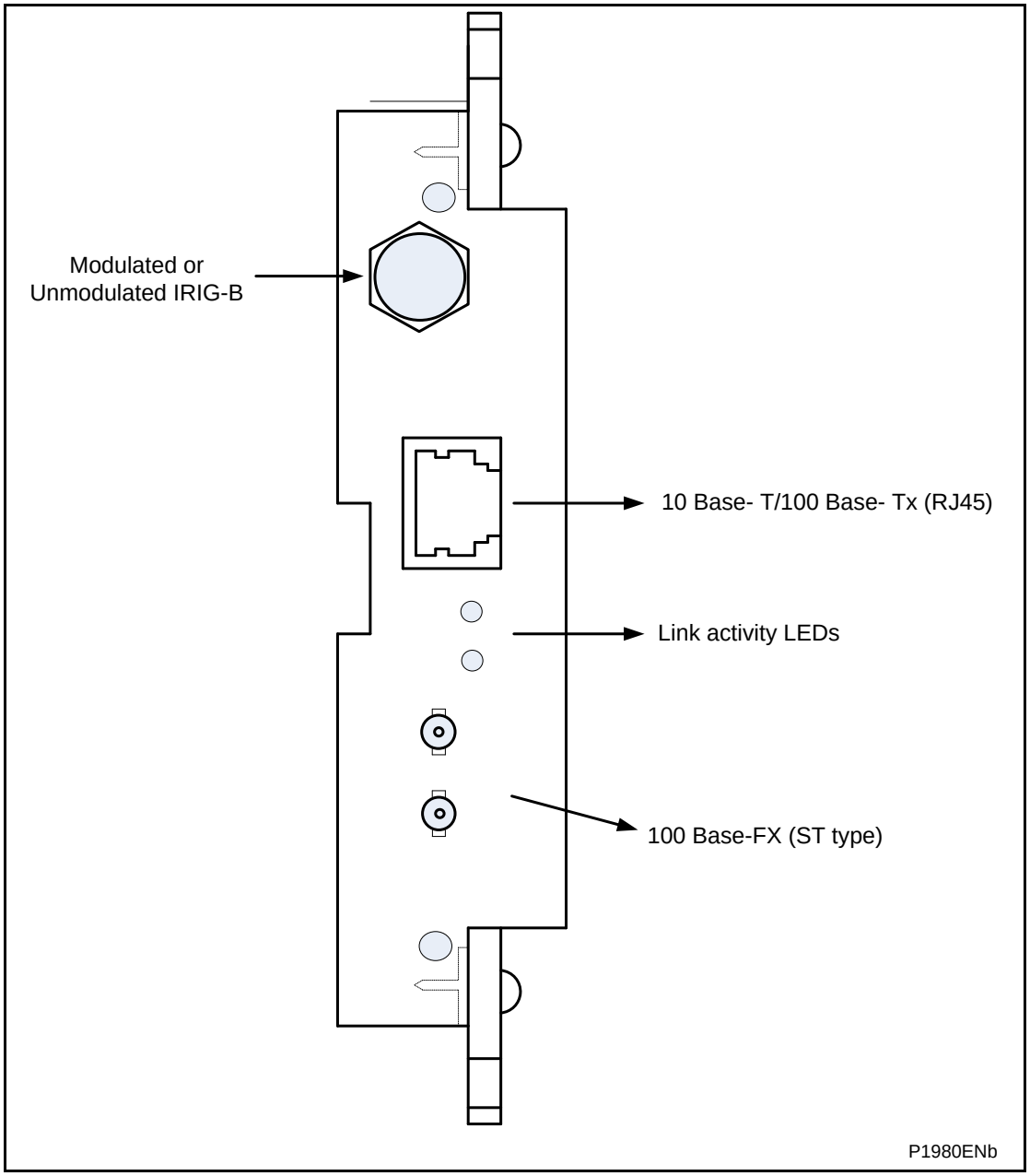


Figure 5: Single Ethernet board

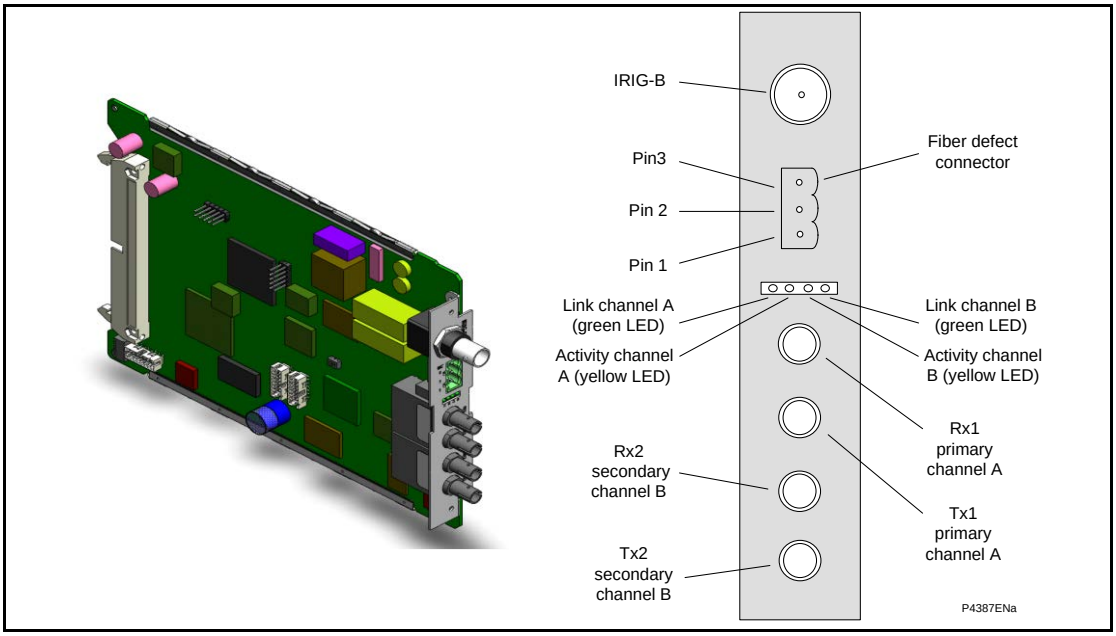


Figure 6: Redundant Ethernet board connectors

2.9 IEC 61850-9-2 LE Ethernet board (P348)

For IEC 61850-9-2 LE process bus communications a single Ethernet board (ZN0078) is available in the P348.

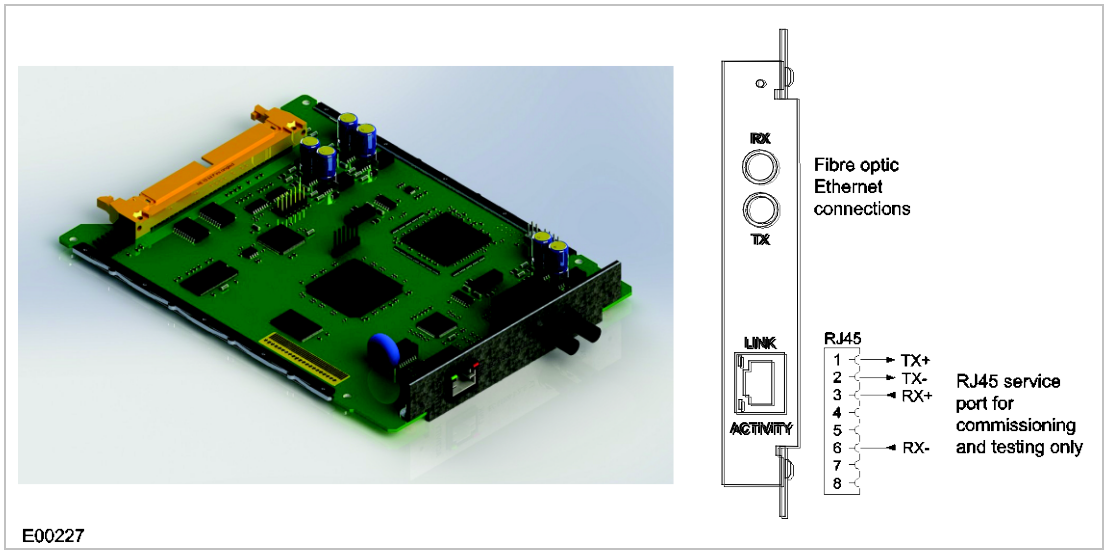


Figure 7: IEC 61850-9-2 LE Ethernet board connectors

Optical Fibre Connectors

Uses 1300 nm multi mode 100BaseFx with ST connectors.

RJ45 Connector

This is a service port for commissioning and testing only. Do not use this for permanent connections.

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LEDs

LED	Function	On	Off	Flashing
Green	Link	Link ok	Link broken	
Yellow	Activity			Traffic

Board Location

The board is located in the slot reserved for communication boards.

The following diagram shows the IEC 61850-9-2LE interface highlighted in grey.

See the IEC 61850-9-2 LE Technical Manual, *Px4x_9-2LE-TM*, for information regarding the IEC 61850-9-2 LE Ethernet communication port.

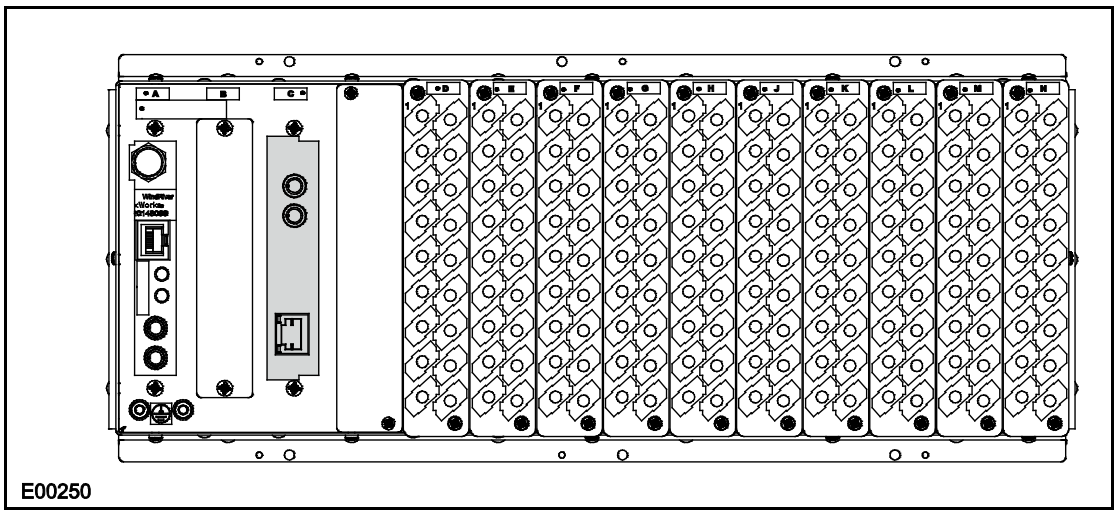


Figure 8: Rear view of IED showing IEC61850-9-2 LE interface

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2.10 Current loop input output board (CLIO)

The current loop input output (CLIO) board is an order option. The CLIO board is powered from the 22 V power rail that is used to drive the output relays.

Four analog (or current loop) inputs are provided for transducers with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA. The input current data is read by the processor through the parallel data bus, and is used to provide measurements from various transducers such as vibration monitors, tachometers and pressure transducers.

For each of the four current loop inputs there are two separate input circuits, 0 - 1 mA and 0 - 20 mA. The latter is also used for 0 - 10 mA and 4 - 20 mA transducer inputs. The anti-alias filters have a nominal cut-off frequency (3dB point) of 23 Hz to reduce power system interference from the incoming signals. Four analog current outputs are provided with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA which can alleviate the need for separate transducers. These may be used to feed standard moving coil ammeters for analog indication of certain measured quantities or into a SCADA using an existing analog RTU.

Each of the four current loop outputs provides one 0 - 1 mA output, one 0 - 20 mA output and one common return. Suitable software scaling of the value written to the board allows the 0 - 20 mA output to also provide 0 - 10 mA and 4 - 20 mA. Screened leads are recommended for use on the current loop output circuits.

The refresh interval for the outputs is nominally 50 ms. The exceptions are shown in section 2.27.3 of *P34x/EN AP*. Those exceptional measurements are updated once every second.

All external connections to the current loop I/O board are made via the same 15 way light duty I/O connector SL3.5/15/90F used on the RTD board. Two such connectors are used, one for the current loop outputs and one for the current loop inputs.

The I/O connectors accommodate wire sizes in the range 1/0.85 mm (0.57 mm2) to 1/1.38 mm (1.5 mm2) and their multiple conductor equivalents. The use of screened cable is recommended. The screen terminations should be connected to the case earth of the relay.

Basic Insulation (300 V) is provided between analog inputs/outputs and earth and between analog inputs and outputs. However, there is no insulation between one input and another or one output and another.

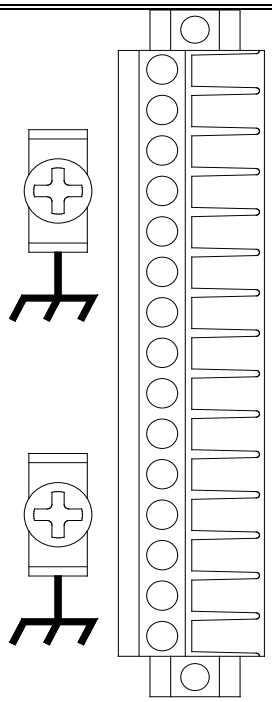
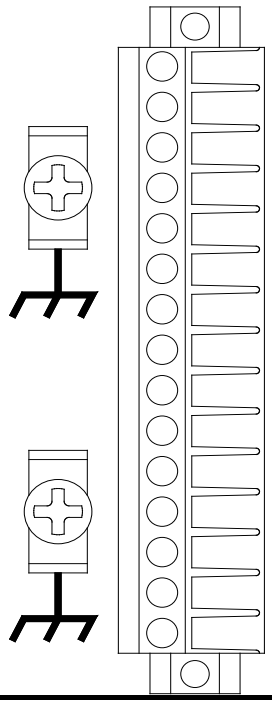
Connection	IO Blocks	Connection
Outputs		
Screen channel 1		0 - 10/0 - 20/4 - 20 mA channel 1 0 - 1 mA channel 1 Common return channel 1
Screen channel 2		0 - 10/0 - 20/4 - 20 mA channel 2 0 - 1 mA channel 2 Common return channel 2
Screen channel 3		0 - 10/0 - 20/4 - 20 mA channel 3 0 - 1 mA channel 3 Common return channel 3
Screen channel 4		0 - 10/0 - 20/4 - 20 mA channel 4 0 - 1 mA channel 4 Common return channel 4
Inputs		
Screen channel 1		0 - 10/0 - 20/4 - 20 mA channel 1 0 - 1 mA channel 1 Common channel 1
Screen channel 2		0 - 10/0 - 20/4 - 20 mA channel 2 0 - 1 mA channel 2 Common channel 2
Screen channel 3		0 - 10/0 - 20/4 - 20 mA channel 3 0 - 1 mA channel 3 Common channel 3
Screen channel 4		0 - 10/0 - 20/4 - 20 mA channel 4 0 - 1 mA channel 4 Common channel 4

Figure 9: Current loop input output board

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2.11 Mechanical layout

The relay case is pre-finished steel with a conductive covering of aluminum and zinc. This provides good earthing at all joints giving a low impedance path to earth that is essential for shielding from external noise. The boards and modules use a multi-point earthing strategy to improve the immunity to external noise and minimize the effect of circuit noise. Ground planes are used on boards to reduce impedance paths and spring clips are used to ground the module metalwork.

Heavy duty terminal blocks are used at the rear of the relay for the current and voltage signal connections. Medium duty terminal blocks are used for the digital logic input signals, the output relay contacts, the power supply and the rear communication port. A BNC connector is used for the optional IRIG-B signal. 9-pin and 25-pin female D-connectors are used at the front of the relay for data communication.

Inside the relay the PCBs plug into the connector blocks at the rear, and can be removed from the front of the relay only. The connector blocks to the relay's CT inputs are provided with internal shorting links inside the relay which will automatically short the current transformer circuits before they are broken when the board is removed.

The front panel consists of a membrane keypad with tactile dome keys, an LCD and 12 LEDs mounted on an aluminum backing plate.

2.12 P391 rotor earth fault measuring/coupling unit

The P391 is a stand alone unit that measures earth faults of generator field windings, see Figure 10 below.

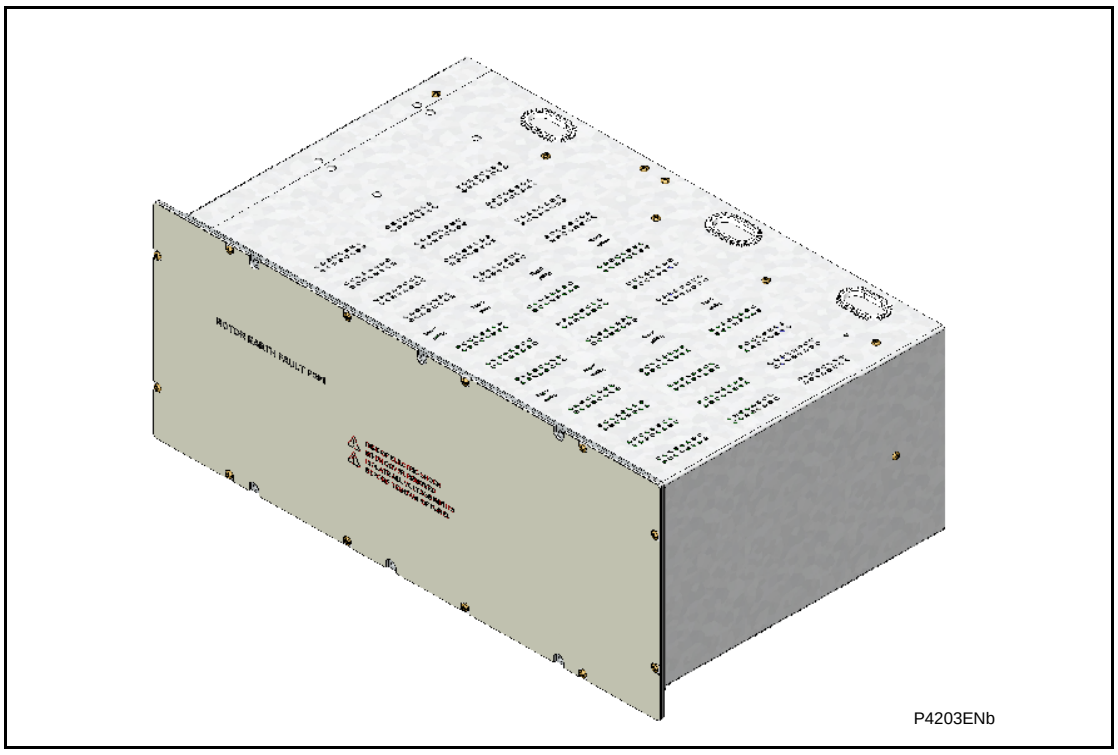


Figure 10: P391 rotor earth fault measuring/coupling unit

Inside the P391 are 3 printed circuit boards (PCB's), a description of these follow:

2.12.1 Injection resistor boards

There are two injection resistor boards within the P391. These couple the P391 to the high voltage of the generator field winding.

The main injection resistors are accessible via terminal numbers A8 & A16 and B8 & B16. This circuit provides 5.8 kV isolation to earth allowing the P391 to be connected to generator field voltages of up to 1200 V DC.

The PCB also offers a 500 Ω calibration resistor for use during commissioning of the P391. The calibration resistor is accessible via terminal numbers A3 & A5 or B3 & B5. This circuit provides 2 kV isolation to earth and the injection resistor circuit.

Warning: Under no circumstances should the calibration resistors be connected to the generator field winding with the field voltage live. The calibration resistors must only be used during calibration of the P391 to the P342/3/4/5/6 relay with the field voltage to the generator de-energized.

Warning: All voltage supplies must be isolated before the front cover or rear safety terminal cover is removed. This must be re-fitted before the supplies are restored

2.12.2 Power supply, control & measurement board

The board can be energized via terminal numbers C1 & C2. The power supply range is detailed in the table below:

Nominal range	Operative range
60 / 250 V dc	48 - 300 V dc
100 / 230 V (50-60 Hz)	85 – 253 V ac (45-65 Hz)

Table 3: P391 Power supply range

A power supply watchdog relay provides 1 changeover contact. These are accessible via terminal numbers C9, C10, and, C12 with the latter being the common contact.

Terminal C5 of the PCB provides the low frequency voltage output (±30 V DC Square wave output at 0.25 Hz, 0.5 Hz, or 1 Hz depending on injection frequency selected) that connects to the injection resistor boards and then to the generator field winding. The injection voltage frequency is selectable via an internal jumper on the PCB.

Terminal 6 provides the earth fault current return path from the generators earthing / grounding brush.

The returned fault current which represents the field winding fault resistance is fed through a measuring resistance, through a low pass filter, and conditioning circuit. The measured value is then converted to an output current in the range of 0-20 mA depending on the level of fault resistance to earth/ground in the generator field winding. This current output is available at terminals C17 & C18 of the board.

The output current circuit is classed as an Extra Low Voltage (ELV) circuit and is safe to touch under both normal operational use and single fault conditions.

The output current from terminals C17 & C18 is designed to be connected to the P342/3/4/5/6 relays 0-20 mA CLIO input circuit which converts the current input back to a resistance representing the generator field winding fault resistance. The P342/3/4/5/6 protection then uses this resistance value to execute its rotor earth fault protection application.

2.12.3 Mechanical layout – P391

The case materials of the relay are constructed from pre-finished steel that has a conductive covering of aluminum and zinc. This provides good earthing at all joints giving a low impedance path to earth that is essential for performance in the presence of external noise. The boards and modules use a multi-point earthing strategy to improve the immunity to external noise and minimize the effect of circuit noise. Ground planes are used on boards to reduce impedance paths and spring clips are used to ground the module metalwork.

Medium duty terminal blocks are used for all connections.

Inside the relay the PCBs plug into the connector blocks at the rear, and can be removed from the front of the relay only.

The front panel consists of a steel plate covered by an Alstom Grid branded membrane.

Ventilation holes are provided at the top and bottom of the case to allow cooling of the injection resistors. The case requires ventilation of the equivalent of 2U above and 1U below the case.

There are 3 mounting options available, these being, Rack, Panel or Wall which needs to be specified when ordering.

A rear terminal safety cover is also provided for all mounting options which must be fitted at all times.

3 RELAY SOFTWARE

The relay software was introduced in the overview of the relay at the start of this chapter. The software can be considered to be made up of four sections:

- The real-time operating system
- The system services software
- The platform software
- The protection & control software

This section describes in detail the latter two of these, the platform software and the protection & control software, which between them control the functional behavior of the relay. Figure 11 shows the structure of the relay software.

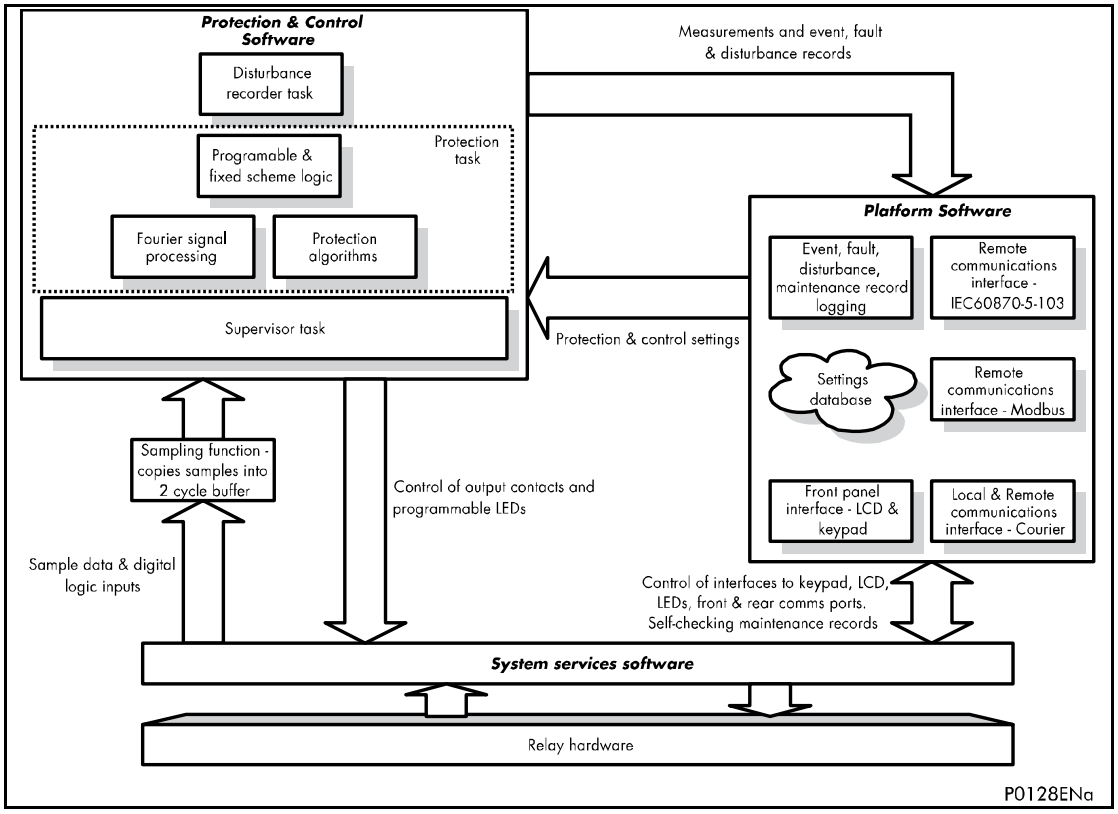


Figure 11: Relay software structure

3.1 Real-time operating system

The software is split into tasks; the real-time operating system is used to schedule the processing of the tasks to ensure that they are processed in the time available and in the desired order of priority. The operating system is also responsible in part for controlling the communication between the software tasks through the use of operating system messages.

3.2 System services software

Figure 11 shows the system services software provides the interface between the relay's hardware and the higher-level functionality of the platform software and the protection & control software. For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports, and controls the boot of the processor and downloading of the processor code into SRAM from non-volatile flash EPROM at power up.

3.3 Platform software

The platform software has three main functions:

- To control the logging of all records that are generated by the protection software, including alarms and event, fault, disturbance and maintenance records.
- To store and maintain a database of all of the relay's settings in non-volatile memory.
- To provide the internal interface between the settings database and each of the relay's user interfaces, i.e. the front panel interface and the front and rear communication ports, using whichever communication protocol has been specified (Courier, MODBUS, IEC 60870-5-103 and DNP3.0).

3.3.1 Record logging

The logging function is provided to store all alarms, events, faults and maintenance records. The records for all of these incidents are logged in battery backed-up SRAM in order to provide a non-volatile log of what has happened. The relay maintains four logs: one each for up to 32 alarms, 512 event records, 5 fault records and 10 maintenance records. The logs are maintained such that the oldest record is overwritten with the newest record. The logging function can be initiated from the protection software or the platform software.

The logging function can be initiated from the protection software or the platform software is responsible for logging of a maintenance record in the event of a relay failure. This includes errors that have been detected by the platform software itself or error that are detected by either the system services or the protection software functions. See section 4 Self testing & diagnostics later in this chapter.

3.3.2 Settings database

The settings database contains all of the settings and data for the relay, including the protection, disturbance recorder and control & support settings. The settings are maintained in non-volatile memory. The platform software's management of the settings database includes the responsibility of ensuring that only one user interface modifies the settings of the database at any one time. This feature is employed to avoid confusion between different parts of the software during a setting change. For changes to protection settings and disturbance recorder settings, the platform software operates a 'scratchpad' in SRAM memory. This allows a number of setting changes to be made in any order but applied to the protection elements, disturbance recorder and saved in the database in non-volatile memory, at the same time (see chapter *P34x/EN IT* on the user interface). If a setting change affects the protection & control task, the database advises it of the new values.

3.3.3 Database interface

The other function of the platform software is to implement the relay's internal interface between the database and each of the relay's user interfaces. The database of settings and measurements must be accessible from all of the relay's user interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each user interface.

3.4 Protection and control software

The protection and control software task is responsible for processing all of the protection elements and measurement functions of the relay. To achieve this it has to communicate with both the system services software and the platform software as well as organize its own operations. The protection software has the highest priority of any of the software tasks in the relay in order to provide the fastest possible protection response. The protection & control software has a supervisor task that controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

3.4.1 Overview - protection and control scheduling

After initialization at start-up, the protection & control task waits until there are enough samples to process. The sampling function is controlled by a 'sampling function' which is called by the system services software and takes each set of new samples from the input module and stores them in a two-cycle buffer. The protection & control software resumes execution when the number of unprocessed samples in the buffer reaches a certain number. For the P342/3/4/5/6 generator protection relays, the protection task is executed four times per cycle, i.e. after every 6 samples for the sample rate of 24 samples per power cycle used by the relay. However, the protection elements are split into groups so that different elements are processed each time, with every element being processed at least once per cycle. The protection and control software is suspended again when all of its processing on a set of samples is complete. This allows operations by other software tasks to take place.

See P34x/EN OP Operation chapter for information on P348 software protection and control scheduling.

3.4.2 Signal processing

The sampling function filters the digital input signals from the opto-isolators and tracks the frequency of the analog signals. The digital inputs are checked against their previous value over a period of half a cycle. Therefore, a change in the state of one of the inputs must be maintained over at least half a cycle before it is registered with the protection & control software.

The P342-6 frequency tracking of the analog input signals is achieved by a recursive Fourier algorithm which is applied to one of the input signals, and works by detecting a change in the measured signal's phase angle. The calculated value of the frequency is used to modify the sample rate being used by the input module so as to achieve a constant sample rate of 24 samples per cycle of the power waveform. The value of the frequency is also stored for use by the protection & control task.

When the P342-6 protection & control task is re-started by the sampling function, it calculates the Fourier components for the analog signals. The Fourier components are calculated using a one-cycle, 24-sample Discrete Fourier Transform (DFT). The DFT is always calculated using the last cycle of samples from the 2-cycle buffer, which is the most recent data is used. The DFT used in this way extracts the power frequency fundamental component from the signal and produces the magnitude and phase angle of the fundamental in rectangular component format. The DFT provides an accurate measurement of the fundamental frequency component, and effective filtering of harmonic frequencies and noise. This performance is achieved in conjunction with the relay input module which provides hardware anti-alias filtering to attenuate frequencies above the half sample rate, and frequency tracking to maintain a sample rate of 24 samples per cycle. The Fourier components of the input current and voltage signals are stored in memory so that they can be accessed by all of the protection elements' algorithms. The samples from the input module are also used in an unprocessed form by the disturbance recorder for waveform recording and to calculate true rms values of current, voltage and power for metering purposes.

See P34x/EN OP Operation chapter for information on P348 signal processing.

3.4.3 Frequency response

With the exception of the RMS measurements all other measurements and protection functions are based on the Fourier derived fundamental component in the P342-6. The fundamental component is extracted by using a 24 sample Discrete Fourier Transform (DFT). This gives good harmonic rejection for frequencies up to the 23rd harmonic. The 23rd is the first predominant harmonic that is not attenuated by the Fourier filter and this is known as an 'Alias'. However, the Alias is attenuated by approximately 85% by an additional, analog, 'anti-aliasing' filter (low pass filter). The combined affect of the anti-aliasing and Fourier filters is shown in Figure 12.

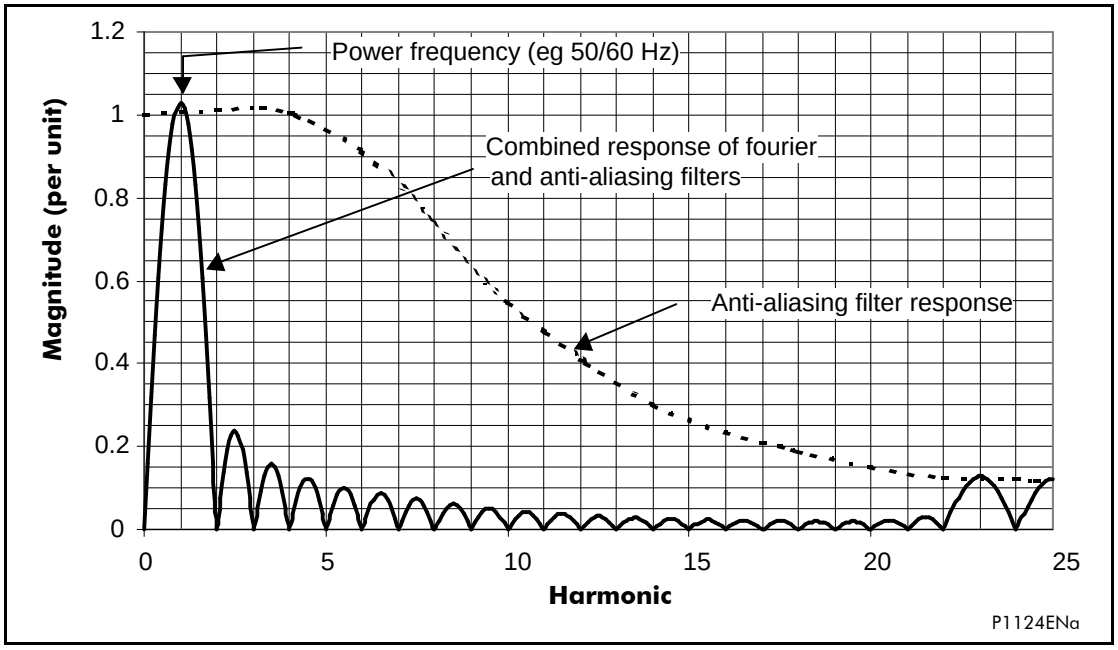


Figure 12: Frequency response

For power frequencies that are not equal to the selected rated frequency the harmonics are be attenuated to zero amplitude. For small deviations of ±1 Hz, this is not a problem but to allow for larger deviations, frequency tracking is used.

Frequency tracking in the P342-6 automatically adjusts the sampling rate of the analog to digital conversion to match the applied signal. In the absence of a suitable signal to amplitude track, the sample rate defaults to the selected rated frequency (Fn). If the signal is in the tracking range of 5 to 70 Hz, the relay will lock on to the signal and the measured frequency will coincide with the power frequency as shown in Figure 12. The resulting outputs for harmonics up to the 23rd will be zero. The relay will frequency track off any voltage or current in the order VA/VB/VC/IA/IB/IC down to 10% Vn for voltage and 5%In for current.

FD

See P34x/EN OP Operation chapter for information on P348 frequency response.

3.4.4 Programmable scheme logic

The purpose of the programmable scheme logic (PSL) is to allow the relay user to configure an individual protection scheme to suit their own particular application. This is done with programmable logic gates and delay timers.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements such as protection starts and trips, and the outputs of the fixed protection scheme logic. The fixed scheme logic provides the relay's standard protection schemes. The PSL itself consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, such as to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven: the logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection & control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

This system provides flexibility for the user to create their own scheme logic design. However, it also means that the PSL can be configured into a very complex system, and because of this setting of the PSL is implemented through the PC support package S1 Agile.

3.4.5 Function key interface (P343/4/5/6/8 only)

The ten function keys interface directly into the PSL as digital input signals and are processed based on the PSL's event driven execution. However, a change of state is only recognized when a key press is executed on average for longer than 200 ms. The time to register a change of state, depends on whether the function key press is executed at the start or the end of a protection task cycle, with the additional hardware and software scan time included. A function key press can provide a latched (toggled mode) or output on key press only (normal mode) depending on how it is programmed and can be configured to individual protection scheme requirements. The latched state signal for each function key is written to non-volatile memory and read from non-volatile memory during relay power up thus allowing the function key state to be reinstated after power-up should relay power be inadvertently lost.

3.4.5.1 PSL data

In the PSL editor in S1 Agile when a PSL file is downloaded to the relay the user can specify the group to download the file and a 32 character PSL reference description. This PSL reference is shown in the Grp. 1/2/3/4 PSL Ref. cell in the PSL DATA menu in the relay. The download date and time and file checksum for each groups PSL file is also shown in the PSL DATA menu in cells Date/Time and Grp. 1/2/3/4 PSL ID. The PSL data can be used to indicate if a PSL has been changed and therefore can be useful in providing information for version control of PSL files.

The default PSL Reference description is Default PSL followed by the model number, for example Default PSL P34x??????0yy0? where x refers to the model e.g. 1, 2, 3 and yy refers to the software version e.g. 05. This is the same for all protection setting groups (since the default PSL is the same for all groups). Since the LCD display (bottom line) only has space for 16 characters the display must be scrolled to see all 32 characters of the PSL Reference description.

The default date and time is the date and time when the defaults were loaded from flash into EEPROM.

Note: The PSL DATA column information is only supported by Courier and MODBUS, but not DNP3.0, IEC 61850 or IEC 60870-5-103.

3.4.6 Event, fault & maintenance recording

A change in any digital input signal or protection element output signal is used to indicate that an event has taken place. When this happens, the protection & control task sends a message to the supervisor task to indicate that an event is available to be processed and writes the event data to a fast buffer in SRAM that is controlled by the supervisor task. When the supervisor task receives either an event or fault record message, it instructs the platform software to create the appropriate log in battery backed-up SRAM. The operation of the record logging to battery backed-up SRAM is slower than the supervisor's buffer. This means that the protection software is not delayed waiting for the records to be logged by the platform software. However, in the rare case when a large number of records to be logged are created in a short period of time, it is possible that some will be lost, if the supervisor's buffer is full before the platform software is able to create a new log in battery backed-up SRAM. If this occurs then an event is logged to indicate this loss of information.

Maintenance records are created in a similar manner with the supervisor task instructing the platform software to log a record when it receives a maintenance record message. However, it is possible that a maintenance record may be triggered by a fatal error in the relay in which case it may not be possible to successfully store a maintenance record, depending on the nature of the problem. See section 4 on self supervision & diagnostics.

3.4.7 Disturbance recorder

The disturbance recorder operates as a separate task from the protection and control task. It can record the waveforms for up to 8 analog channels and the values of up to 32 digital signals. The recording time is user selectable up to a maximum of 10 seconds. The disturbance recorder is supplied with data by the protection and control task once per cycle. The disturbance recorder collates the data that it receives into the required length disturbance record. The disturbance records can be extracted by S1 Agile that can also store the data in COMTRADE format, thus allowing the use of other packages to view the recorded data.

4 SELF TESTING & DIAGNOSTICS

The relay includes several self-monitoring functions to check the operation of its hardware and software when it is in service. These are included so that if an error or fault occurs in the relay's hardware or software, the relay is able to detect and report the problem and attempt to resolve it by performing a reboot. The relay must therefore be out of service for a short period, during which the **Healthy** LED on the front of the relay is OFF and, the watchdog contact at the rear is ON. If the reboot fails to resolve the problem, the relay takes itself permanently out of service; the **Healthy** LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the relay stores a maintenance record in battery backed-up SRAM to allow the nature of the problem to be notified to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check that is performed when the relay is booted-up and secondly a continuous self-checking operation that checks the operation of the relay's critical functions whilst it is in service.

4.1 Start-up self-testing

The self-testing that is carried out when the relay is started takes a few seconds to complete, during which time the relay's protection is unavailable. This is signaled by the Healthy LED on the front of the relay that will illuminate when the relay has passed all of the tests and entered operation. If the testing detects a problem, the relay will remain out of service until it is manually restored to working order.

The operations that are performed at start-up are as follows:

4.1.1 System boot

The integrity of the flash EPROM memory is verified using a checksum before the program code and data stored in it is copied into SRAM to be used for execution by the processor. When the copy has been completed the data then held in SRAM is compared to that in the flash EPROM to ensure that the two are the same and that no errors have occurred in the transfer of data from flash EPROM to SRAM. The entry point of the software code in SRAM is then called which is the relay initialization code.

4.1.2 Initialization software

The initialization process includes the operations of initializing the processor registers and interrupts, starting the watchdog timers (used by the hardware to determine whether the software is still running), starting the real-time operating system and creating and starting the supervisor task. In the course of the initialization process the relay checks:

- The status of the battery
- The integrity of the battery backed-up SRAM that is used to store event, fault and disturbance records
- The operation of the LCD controller
- The watchdog operation

When the initialization software routine is compete, the supervisor task starts the platform software.

4.1.3 Platform software initialization & monitoring

In starting the platform software, the relay checks the integrity of the data held in non-volatile memory with a checksum, the operation of the real-time clock, and the IRIG-B, RTD and CLIO board if fitted. The final test that is made concerns the input and output of data; the presence and healthy condition of the input board is checked and the analog data acquisition system is checked through sampling the reference voltage.

At the successful conclusion of all of these tests the relay is entered into service and the protection started-up.

4.2 Continuous self-testing

When the relay is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software (see section on relay software earlier in this chapter) and the results reported to the platform software. The functions that are checked are as follows:

- The flash EPROM containing all program code and language text is verified by a checksum
- The code and constant data held in SRAM is checked against the corresponding data in flash EPROM to check for data corruption
- The SRAM containing all data other than the code and constant data is verified with a checksum
- The non-volatile memory containing setting values is verified by a checksum, whenever its data is accessed
- The battery status
- The integrity of the digital signal I/O data from the opto-isolated inputs and the relay contacts, is checked by the data acquisition function every time it is executed. The operation of the analog data acquisition system is continuously checked by the acquisition function every time it is executed, by means of sampling the reference voltage on a spare multiplexed channel
- The operation of the RTD board is checked by reading the temperature indicated by the reference resistors on the two spare RTD channels
- The operation of the IRIG-B board is checked, where it is fitted, by the software that reads the time and date from the board
- The correct operation of the CLIO board is checked, where it is fitted
- The operation of the Ethernet board is checked, where it is fitted, by the software on the main processor card. If the Ethernet board fails to respond an alarm is raised and the card is reset in an attempt to resolve the problem

In the unlikely event that one of the checks detects an error in the relay's subsystems, the platform software is notified and it will attempt to log a maintenance record in battery backed-up SRAM. If the problem is with the battery status, the RTD board, CLIO board or the IRIG-B board, the relay will continue in operation. However, for problems detected in any other area the relay will initiate a shutdown and re-boot. This will result in a period of up to 5 seconds when the protection is unavailable, but the complete restart of the relay including all initializations should clear most problems that could occur. An integral part of the start-up procedure is a thorough diagnostic self-check. If this detects the same problem that caused the relay to restart, the restart has not cleared the problem and the relay takes itself permanently out of service. This is indicated by the Healthy LED on the front of the relay, which goes OFF, and the watchdog contact that goes ON.

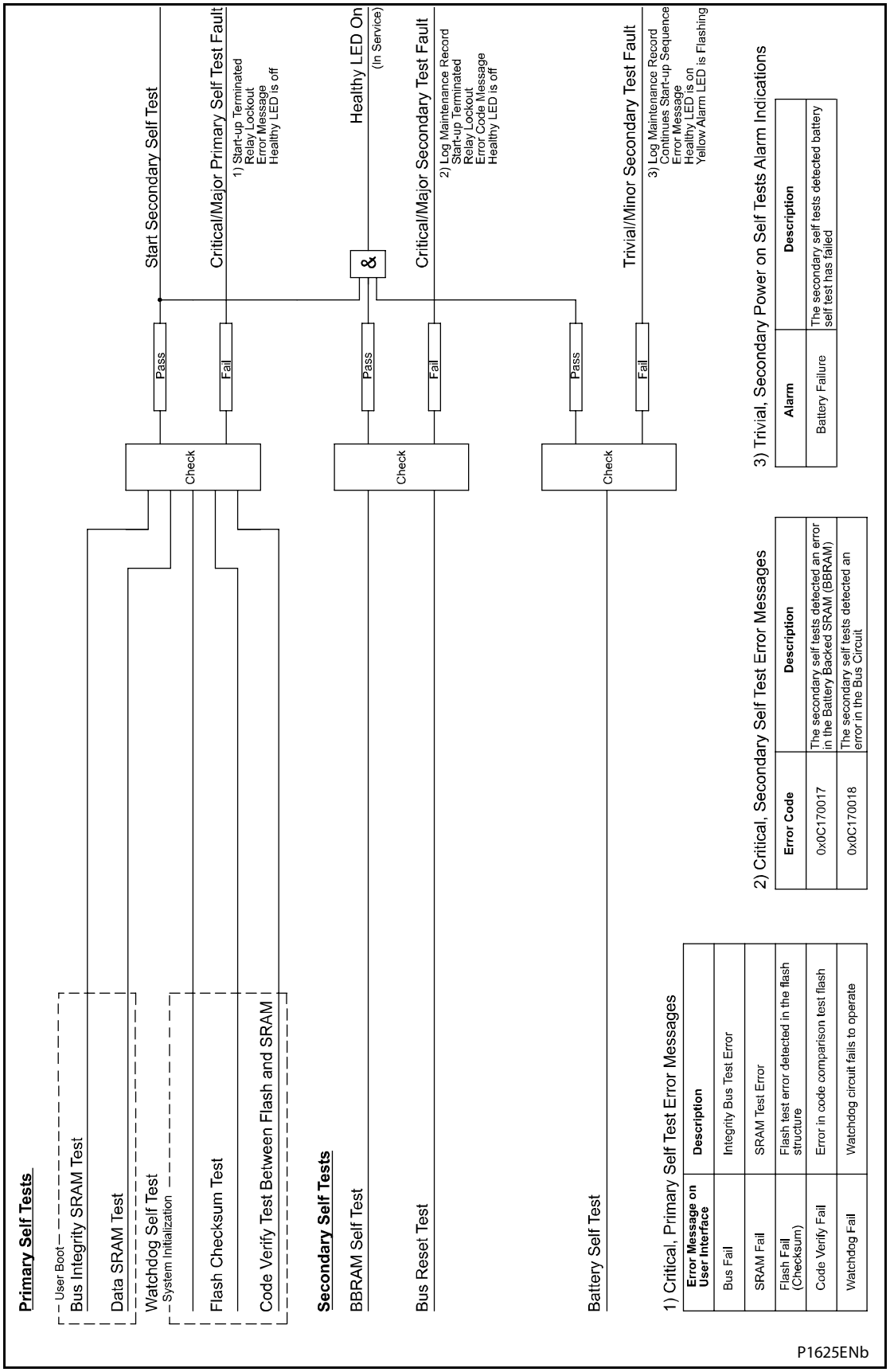


Figure 13: Start-up self-testing logic

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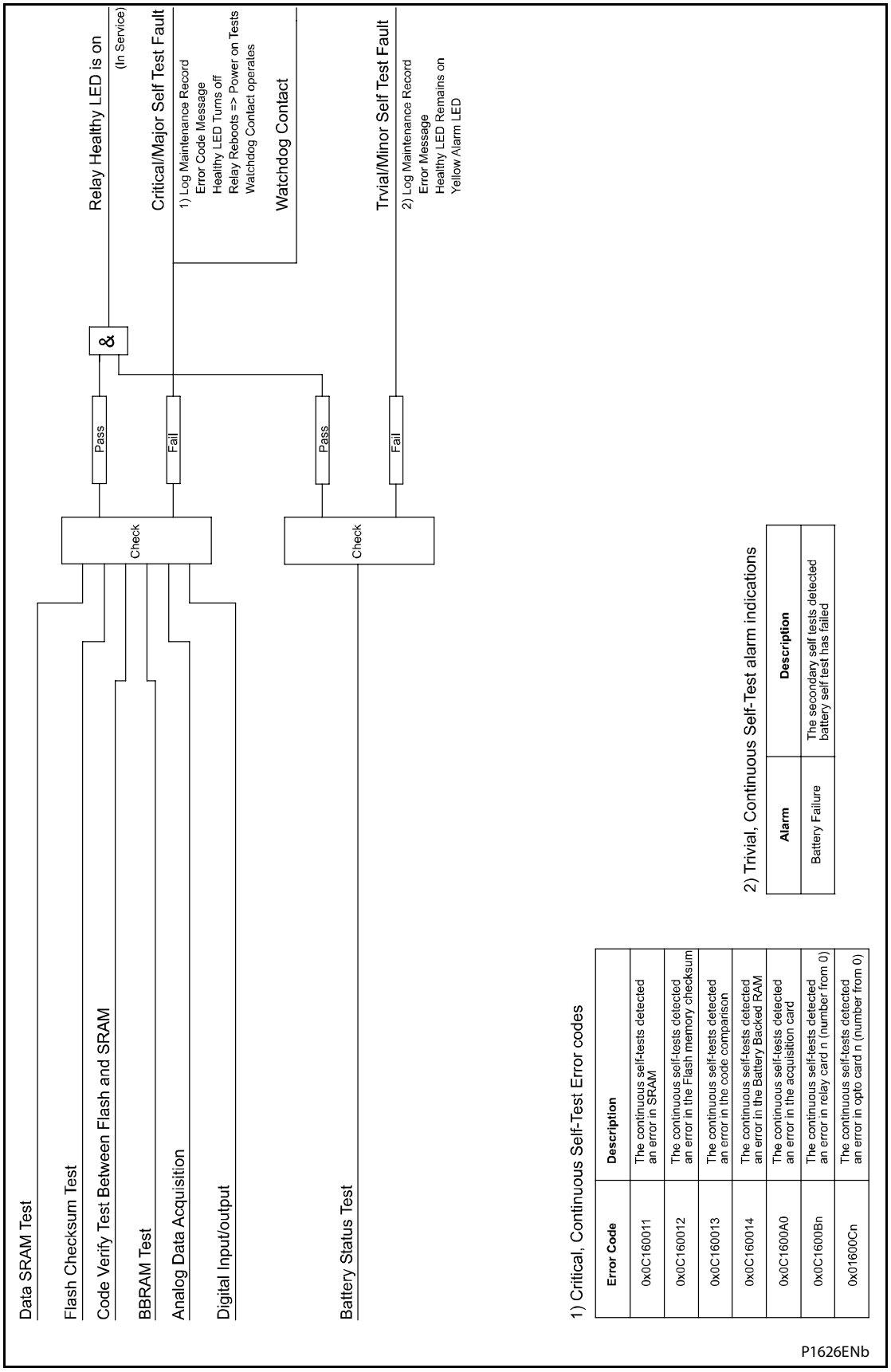


Figure 14: Continuous self-testing logic

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COMMISSIONING

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Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 INTRODUCTION

This Commissioning chapter covers both the P34x generator protection relay range and the P391 Generator Rotor Earth Fault Protection Unit

The P34x generator protection relays are fully numerical in their design, implementing all protection and non-protection functions in software. The relays employ a high degree of self-checking and, in the unlikely event of a failure, will give an alarm. As a result of this, the commissioning tests do not need to be as extensive as with non-numeric electronic or electro-mechanical relays.

To commission numeric relays, it is only necessary to verify that the hardware is functioning correctly and the application-specific software settings have been applied to the relay. It is considered unnecessary to test every function of the relay if the settings have been verified by one of the following methods:

- Extracting the settings applied to the relay using appropriate setting software (preferred method)

Using the operator interface

To confirm the product is operating correctly once the application-specific settings have been applied, a test should be performed on a single protection element.

Unless previously agreed to the contrary, the customer will be responsible for determining the application-specific settings to be applied to the relay and for testing of any scheme logic applied by external wiring and/or configuration of the relay's internal programmable scheme logic.

Blank commissioning test and setting records are provided at the end of this chapter for completion as required.

As the relay's menu language is user-selectable, it is acceptable for the Commissioning Engineer to change it to allow accurate testing as long as the menu is restored to the customer's preferred language on completion.

To simplify the specifying of menu cell locations in these Commissioning Instructions, they will be given in the form [courier reference: COLUMN HEADING, Cell Text]. For example, the cell for selecting the menu language (first cell under the column heading) is located in the System Data column (column 00) so it would be given as [0001: SYSTEM DATA, Language].



Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section/Safety Guide Pxxx-SG-4LM-2 or later issue and the ratings on the equipment's rating label.

2 SETTING FAMILIARIZATION

When first commissioning a P34x relay, allow sufficient time to become familiar with how to apply the settings.

The Relay Menu Database document and the Settings chapter (*P34x/EN MD*, *P34x/EN ST*) contain a detailed description of the menu structure of P34x relays.

With the secondary front cover in place, all keys except the ↵ key are accessible. All menu cells can be read. LEDs and alarms can be reset. However, no protection or configuration settings can be changed, or fault and event records cleared.

Removing the secondary front cover allows access to all keys so that settings can be changed, LEDs and alarms reset, and fault and event records cleared. However, to make changes to menu cells that have access levels higher than the default level, the appropriate password is needed.

Alternatively, if a portable PC with suitable setting software is available (such as S1 Agile), the menu can be viewed one page at a time to display a full column of data and text. This PC software also allows settings to be entered more easily, saved to a file on disk for future reference or printed to produce a setting record. Refer to the PC software user manual for details. If the software is being used for the first time, allow sufficient time to become familiar with its operation.

3 COMMISSIONING TEST MENU

To help minimize the time required to test MiCOM General Electric relays, the relay provides several test facilities under the **COMMISSION TESTS** menu heading. There are menu cells which allow the status of the opto-isolated inputs, output relay contacts, internal digital data bus (DDB) signals and user-programmable LEDs to be monitored. Also, there are cells to test the operation of the output contacts and user-programmable LEDs.

The following table shows the relay menu of commissioning tests, including the available setting ranges and factory defaults:

Menu text	Default setting	Settings
COMMISSION TESTS		
Opto I/P Status	–	–
Relay O/P Status	–	–
Test Port Status	–	–
LED Status	–	–
Monitor Bit 1	64 (LED 1)	0 to 2047 See *P34x/EN PL* for details of Digital Data Bus signals
Monitor Bit 3	66 (LED 3)	
Monitor Bit 4	67 (LED 4)	
Monitor Bit 5	68 (LED 5)	
Monitor Bit 6	69 (LED 6)	
Monitor Bit 7	70 (LED 7)	
Monitor Bit 8	71 (LED 8)	
Test Mode	Disabled	Disabled Test Mode Contacts Blocked
Test Pattern	All bits set to 0	0 = Not Operated 1 = Operated
Contact Test	No Operation	No Operation Apply Test Remove Test
Test LEDs	No Operation	No Operation Apply Test
Red LED Status	–	–
Green LED Status	–	–

Table 1: List of test facilities within COMMISSION TESTS menu

3.1 Opto I/P status

This menu cell displays the status of the relay's opto-isolated inputs as a binary string, a **1** indicating an energized opto-isolated input and a **0** a de-energized one. If the cursor is moved along the binary numbers the corresponding label text will be displayed for each logic input.

The menu cell can be used during commissioning or routine testing to monitor the status of the opto-isolated inputs whilst they are sequentially energized with a suitable dc voltage.

3.2 Relay O/P status

This menu cell displays the status of the digital data bus (DDB) signals that result in energization of the output relays as a binary string, a **1** indicating an operated state and **0** a non-operated state. If the cursor is moved along the binary numbers, the corresponding label text is displayed for each relay output.

The information displayed can be used during commissioning or routine testing to show the status of the output relays when the relay is 'in service'. Also, to fault find for output relay damage, compare the status of the output contact under investigation with its associated bit.

Note: When the **Test Mode** cell is set to **Enabled,** this cell continues to show which contacts would operate if the relay was in-service. It does not show the actual status of the output relays.

3.3 Test port status

This menu cell displays the status of the eight digital data bus (DDB) signals that have been allocated in the **Monitor Bit** cells. If the cursor is moved along the binary numbers the corresponding DDB signal text string will be displayed for each monitor bit.

By using this cell with suitable monitor bit settings, the state of the DDB signals can be displayed as various operating conditions or sequences are applied to the relay. Therefore the programmable scheme logic can be tested.

As an alternative to using this cell, the optional monitor/download port test box can be plugged into the monitor/download port located behind the bottom access cover. For details see section 3.11.

3.4 LED status

The **LED Status** cell is an 8-bit binary string that shows which of the user-programmable LEDs on the relay are ON when accessing the relay from a remote location. A **1** means that a particular LED is ON and a **0** means that is it off.

3.5 Monitor bits 1 to 8

The eight **Monitor Bit** cells allow the user to select the status of which digital data bus signals can be observed in the **Test Port Status** cell or using the monitor/download port.

Each **Monitor Bit** is set by entering the required digital data bus (DDB) signal number (0 - 2047) from the list of available DDB signals in *P34x/EN PL*. The pins of the monitor/download port used for monitor bits are shown in the table below. The signal ground is available on pins 18, 19, 22 and 25.

Monitor bit	1	2	3	4	5	6	7	8
Monitor/download port pin	11	12	15	13	20	21	23	24



The monitor/download port does not have electrical isolation against induced voltages on the communications channel. It should therefore only be used for local communications.

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3.6 Test mode

The Test Mode menu cell is used to allow secondary injection testing to be performed on the relay without operation of the trip contacts. The Test Mode is also used in the IEC60870-5-103 protocol, see section 5.8 of *P34x/EN SC.* It also enables a facility to directly test the output contacts by applying menu controlled test signals.

To select test mode the **Test Mode** menu cell should be set to **Test Mode**. This takes the relay out of service and blocks the maintenance counters. It also causes an alarm condition to be recorded and the yellow **Out of Service** LED **switches ON** and an alarm message **Prot'n. Disabled** is displayed.

To enable testing of output contacts, set the **Test Mode** cell to **Contacts Blocked**. This blocks the protection from operating the contacts. It also enables the test pattern and contact test functions, used to manually operate the output contacts. Once testing is complete, set the cell back to **Disabled** to restore the relay back to service.



When the Test Mode cell is set to Contacts Blocked the relay scheme logic does not drive the output relays and hence the protection will not trip the associated circuit breaker if a fault occurs.

3.7 Test pattern

The **Test Pattern** cell is used to select the output relay contacts that will be tested when the **Contact Test** cell is set to **Apply Test**. The cell has a binary string with one bit for each user-configurable output contact which can be set to **1** to operate the output under test conditions and **0** to not operate it.

3.8 Contact test

When the **Apply Test** command in this cell is issued, the contacts set to **1** for operation in the **Test Pattern** cell change state. After the test has been applied the command text on the LCD will change to **No Operation** and the contacts will remain in the Test State until reset issuing the **Remove Test** command. The command text on the LCD will again revert to **No Operation** after the **Remove Test** command has been issued.

Note: When the **Test Mode** cell is set to **Enabled** the **Relay O/P Status** cell does not show the current status of the output relays and hence can not be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.

3.9 Test LEDs

When the **Apply Test** command in this cell is issued the eight user-programmable LEDs (P342) or eighteen user-programmable LEDs (P343/4/5/6/8) are ON for approximately 2 seconds before they switch OFF and the command text on the LCD reverts to **No Operation**.

3.10 Red LED status and green LED status (P343/4/5/6/8)

The **Red LED Status** and **Green LED Status** cells are 18-bit binary strings that show which of the user-programmable LEDs on the relay are ON when accessing the relay from a remote location. **1** indicates a particular LED is ON and a **0** OFF. When the status of a particular LED in both cells is **1**, this means the LEDs is yellow.

3.11 Using a monitor/download port test box

A monitor/download port test box containing 8 LEDs and a switchable audible indicator is available from General Electric, or one of their regional sales offices. It is housed in a small plastic box with a 25-pin male D-connector that plugs directly into the relay's monitor/download port. There is also a 25-pin female D-connector which allows other connections to be made to the monitor/download port whilst the monitor/download port test box is in place.

Each LED corresponds to one of the monitor bit pins on the monitor/download port with **Monitor Bit 1** being on the left hand side when viewing from the front of the relay. The audible indicator can either be selected to sound if a voltage appears any of the eight monitor pins or remain silent so that indication of state is by LED alone.

4 EQUIPMENT REQUIRED FOR COMMISSIONING

4.1 Minimum equipment required

- Overcurrent test set with interval timer
- 110 V ac voltage supply (if stage 1 of the overcurrent function is set directional)
- Multimeter with suitable ac current range, and ac and dc voltage ranges of 0 - 440 V and 0 - 250 V respectively
- Continuity tester (if not included in multimeter)
- Phase angle meter
- Phase rotation meter

100 Ω precision wire wound or metal film resistor, 0.1% tolerance (0°C±2°C)

Note: Modern test equipment may contain many of the above features in one unit.

4.2 Optional equipment

- Multi-finger test plug type MMLB01 or P992 (if test block type MMLG or P991 installed).
- An electronic or brushless insulation tester with a dc output not exceeding 500 V (For insulation resistance testing when required).
- A portable PC, with appropriate software (This enables the rear communications port to be tested if this is to be used and will also save considerable time during commissioning).
- KITZ K-Bus to EIA(RS)232 protocol converter (if first rear EIA(RS)485 K-Bus port or second rear port configured for K-Bus is being tested and one is not already installed).
- EIA(RS)485 to EIA(RS)232 converter (if first rear EIA(RS)485 port or second rear port configured for EIA(RS)485 is being tested).

A printer (for printing a setting record from the portable PC).

4.3 Minimum equipment for IEC 61850-9-2 LE relays (P348)

This is a typical list of equipment required for testing the IEC 61850-9-2LE interface in the IED.

- IED test kit capable of generating IEC 61850-9-2LE Sampled Values or a conventional current and voltage source with a merging unit to generate the sampled values
- Ethernet switch(es)

Fibre optic cables

5 PRODUCT CHECKS

These product checks cover all aspects of the relay that need to be checked to ensure that it has not been physically damaged prior to commissioning, is functioning correctly and all input quantity measurements are within the stated tolerances.

If the application-specific settings have been applied to the relay prior to commissioning, it is advisable to make a copy of the settings so as to allow their restoration later.
If programmable scheme logic other than the default settings with which the relay is supplied have been applied the default settings should be restored prior to commissioning. This could be done by:

- Obtaining a setting file on a diskette from the customer. (This requires a portable PC with appropriate setting software for transferring the settings from the PC to the relay).
- Extracting the settings from the relay itself. (This again requires a portable PC with appropriate setting software).

Manually creating a setting record. This could be done using a copy of the setting record located at the end of this sub-document to record the settings as the relay's menu is sequentially stepped through via the front panel user interface.

If password protection is enabled, and the customer has changed password 2 that prevents unauthorized changes to some of the settings, either the revised password 2 should be provided, or the customer should restore the original password before testing is started.

Note: If the password has been lost, a recovery password can be obtained from General Electric by quoting the serial number of the relay. The recovery password is unique to that relay and will not work on any other relay.



Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section/Safety Guide Pxxx-SG-4LM-2 or later issue and the ratings on the equipment's rating label.

5.1 With the relay re-energized

The following group of tests should be carried out without the auxiliary supply being applied to the relay and with the trip circuit isolated.

The current and voltage transformer connections must be isolated from the relay for these checks. If a P991 or MMLG test block is provided, insert the test plug type P992 or MMLB01, which open-circuits all wiring routed through the test block.

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Before inserting the test plug, refer to the scheme diagram to ensure this will not cause damage or a safety hazard. For example, the test block may be associated with protection current transformer circuits. Before the test plug is inserted into the test block, make sure the sockets in the test plug which correspond to the current transformer secondary windings are linked.



DANGER: Never open circuit the secondary circuit of a current transformer since the high voltage produced may be lethal and could damage insulation.

If a test block is not provided, isolate the voltage transformer supply to the relay using the panel links or connecting blocks. Short-circuit and disconnect the line current transformers from the relay terminals. Where means of isolating the auxiliary supply and trip circuit (such as isolation links, fuses and MCB) are provided, these should be used. If this is not possible, the wiring to these circuits will have to be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

5.1.1 Visual inspection

Check the rating information under the top access cover on the front of the relay. Check that the relay being tested is correct for the protected line or circuit. Ensure that the circuit reference and system details are entered onto the setting record sheet. Double-check the CT secondary current rating, and be sure to record the actual CT tap which is in use.

Carefully examine the relay to see that no physical damage has occurred since installation.

Ensure that the case earthing connections, bottom left-hand corner at the rear of the relay case, are used to connect the relay to a local earth bar using an adequate conductor.

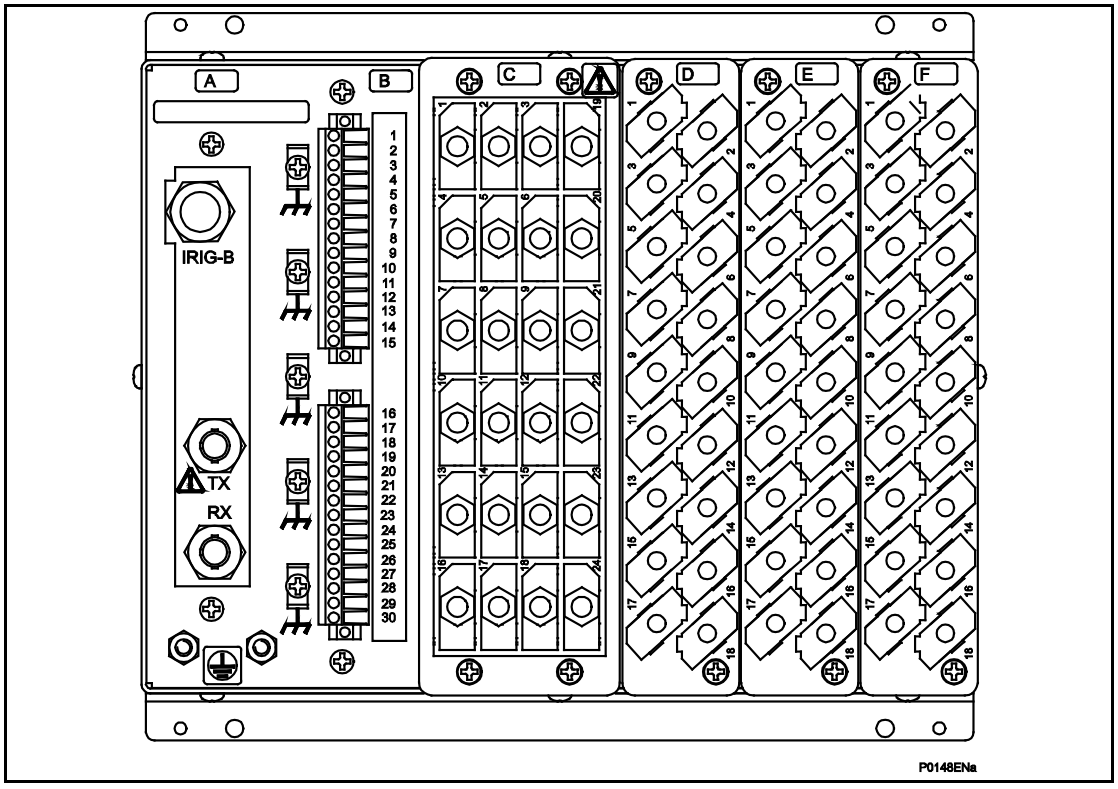


Figure 1: Rear terminal blocks on size 40TE case

5.1.2 Current transformer shorting contacts

If required, the current transformer shorting contacts can be checked to ensure that they close when the heavy duty terminal block (block reference C in figure 1) is disconnected from the current input PCB. For P342 relays block reference C (40TE case) and D (60TE case) are heavy duty terminal blocks. In the case of P343/4/5/6 relays they are located at block references C and E (60TE case) and D and F (80TE case). The P348 uses an IEC 61850-9-2 LE Ethernet port to obtain sampled values of current and voltage so this section is not applicable to the P348.

Current Input	Shorting contact between terminals			
	P342 (40TE), P343/6 (60TE)		P342 (60TE), P343/4/5/6 (80TE)	
	1A CT's	5A CT's	1A CT's	5A CT's
IA	C3 - C2	C1 - C2	D3 - D2	D1 - D2
IB	C6 - C5	C4 - C5	D6 - D5	D4 - D5
IC	C9 - C8	C7 - C8	D9 - D8	D7 - D8
IN	C12 - C11	C10 - C11	D12 - D11	D10 - D11
IN1 SENSITIVE	C15 - C14	C13 - C14	D15 - D14	D13 - D14
IN2 SENSITIVE (P345 only)			F15 - F14	F13 - F14

Current Input	Shorting contact between terminals			
IA(2) (P343/4/5/6 only)	E3 - E2	E1 - E2	F3 - F2	F1 - F2
IB(2) (P343/4/5/6 only)	E6 - E5	E4 - E5	F6 - F5	F4 - F5
IC(2) (P343/4/5/6 only)	E9 – E8	E7 – E8	F9 – F8	F7 – F8
I 100% STEF (P345 only)			F12 – F11	F10 – F11
C/S Voltage (P345 only)				F19-F20

Table 2: Current transformer shorting contact locations

Heavy duty terminal block are fastened to the rear panel using four crosshead screws. These are located top and bottom between the first and second, and third and fourth, columns of terminals (see figure 2).

Note: The use of a magnetic bladed screwdriver is recommended to minimize the risk of the screws being left in the terminal block or lost.

Pull the terminal block away from the rear of the case and check with a continuity tester that all the shorting switches being used are closed. Table 2 shows the terminals between which shorting contacts are fitted.

If external test blocks are connected to the relay, great care should be taken when using the associated test plugs such as MMLB and P992 since their use may make hazardous voltages accessible. *CT shorting links must be in place before the insertion or removal of MMLB test plugs, to avoid potentially lethal voltages.

***NOTE: When a P992 Test Plug is inserted into the P991 Test Block, the secondaries of the line CTs are automatically shorted, making them safe.**

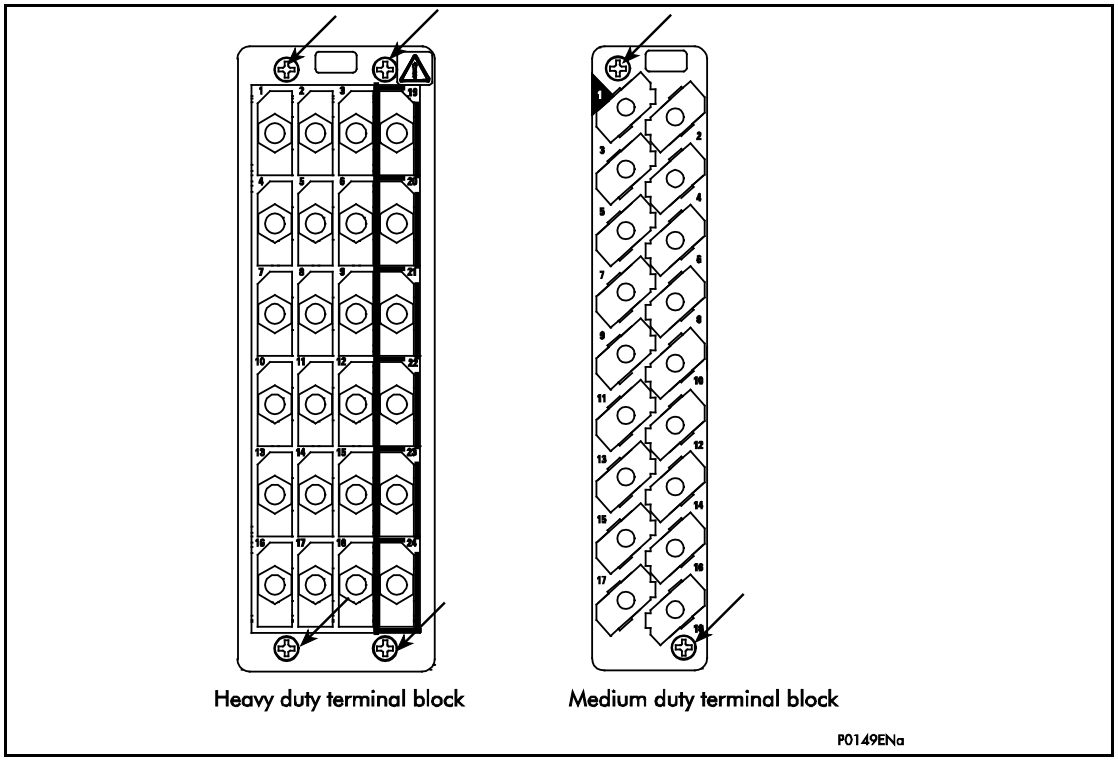


Figure 2: Location of securing screws for heavy duty terminal blocks

5.1.3 Insulation

Insulation resistance tests are only necessary during commissioning if it is required for them to be done and they haven't been performed during installation.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a dc voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The main groups of relay terminals are:

- Voltage transformer circuits (not applicable to P348)
- Current transformer circuits (not applicable to P348)
- Auxiliary voltage supply
- Field voltage output and opto-isolated control inputs
- Relay contacts
- First rear EIA(RS)485 communication port
- RTD inputs
- Current loop (analog) inputs and outputs (CLIO)

Case earth

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the unit.

5.1.4 External wiring

Check that the external wiring is correct to the relevant relay diagram or wiring diagram. The relay diagram number appears on the rating label under the top access cover on the front of the relay. The corresponding connection diagram will have been supplied with the General Electric order acknowledgement for the relay.

If a P991 or MMLG test block is provided, check the connections against the wiring diagram. It is recommended that the supply connections are to the live side of the test block (colored orange with the odd numbered terminals (1, 3, 5, 7 etc.)). The auxiliary supply is normally routed via terminals 13 (supply positive) and 15 (supply negative), with terminals 14 and 16 connected to the relay's positive and negative auxiliary supply terminals respectively. However, check the wiring against the schematic diagram for the installation to ensure compliance with the customer's normal practice.

5.1.5 Watchdog contacts

Using a continuity tester, check that the watchdog contacts are in the states given in Table 3 for a de-energized relay.

Terminals		Contact state	
		Relay de-energized	Relay energized
F11 - F12 J11 - J12 M11 - M12 P11 - P12	(P342 40TE) (P342/3 60TE) (P343/4/5/6 80TE) (P348 80TE)	Closed	Open
F13 - F14 J13 - J14 M13 - M14 P13 - P14	(P342 40TE) (P342/3/6 60TE) (P343/4/5/6 80TE) (P348 80TE)	Open	Closed

Table 3: Watchdog contact status

5.1.6 Auxiliary supply

The relay can be operated from either a dc only or an ac/dc auxiliary supply depending on the relay's nominal supply rating. The incoming voltage must be within the operating range specified in Table 4.

Without energizing the relay, measure the auxiliary supply to ensure it is within the operating range.

Nominal supply rating DC [AC rms]		DC operating range	AC operating range
24 - 48 V	[-]	19 – 65 V	-
48 - 110 V	[40 - 100 V]	37 - 150 V	32 - 110 V
110 - 240 V	[100 - 240 V]	87 - 300 V	80 - 265 V

Table 4: Operational range of auxiliary supply Vx

Note: The relay can withstand an ac ripple of up to 12% of the upper rated voltage on the dc auxiliary supply.

Do not energize the relay using the battery charger with the battery disconnected as this can irreparably damage the relay's power supply circuitry.

Energize the relay only if the auxiliary supply is within the operating range. If a test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the relay.

5.2 With the relay energized

The following group of tests verify that the relay hardware and software is functioning correctly and should be carried out with the auxiliary supply applied to the relay.

The current and voltage transformer connections must remain isolated from the relay for these checks. The trip circuit should also remain isolated to prevent accidental operation of the associated circuit breaker.

5.2.1 Watchdog contacts

Using a continuity tester, check the watchdog contacts are in the states given in Table 3 for an energized relay.

5.2.2 LCD front panel display

The liquid crystal display is designed to operate in a wide range of substation ambient temperatures. For this purpose, the Px40 relays have an **LCD Contrast** setting. This allows the user to adjust how light or dark the characters displayed will be. The contrast is factory pre-set to account for a standard room temperature, however it may be necessary to adjust the contrast to give the best in-service display. To change the contrast, cell [09FF: **LCD Contrast**] at the bottom of the **CONFIGURATION** column can be incremented (darker) or decremented (lighter), as required.

Care: **Before applying a contrast setting, ensure that it will not render the display too light or dark such that menu text becomes unreadable. Should such a mistake be made, it is possible to restore a visible display by downloading a S1 Studio setting file, with the LCD Contrast set within the typical range of 7 to 11.**

5.2.3 Date and time

Before setting the date and time, ensure that the factory-fitted battery isolation strip that prevents battery drain during transportation and storage has been removed. With the lower access cover open, the presence of the battery isolation strip can be checked by a red tab protruding from the positive side of the battery compartment. Lightly pressing the battery to prevent it falling out of the battery compartment, pull the red tab to remove the isolation strip.

The data and time should now be set to the correct values. The method of setting will depend on whether accuracy is being maintained via the optional inter-range instrumentation group standard B (IRIG-B) port on the rear of the relay.

5.2.3.1 With an IRIG-B signal

If a satellite time clock signal conforming to IRIG-B is provided and the relay has the optional IRIG-B port fitted, the satellite clock equipment should be energized.

To allow the relay's time and date to be maintained from an external IRIG-B source cell [0804: **DATE** and **TIME**, **IRIG-B Sync**] must be set to **Enabled**.

Ensure the relay is receiving the IRIG-B signal by checking that cell [0805: **DATE** and **TIME**, **IRIG-B Status**] reads **Active**.

Once the IRIG-B signal is active, adjust the time offset of the universal coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.

Check the time, date and month are correct in cell [0801: **DATE** and **TIME**, **Date/Time**]. The IRIG-B signal does not contain the current year so it will need to be set manually in this cell.

If the auxiliary supply fails, with a battery fitted in the compartment behind the bottom access cover, the time and date is maintained. Therefore, when the auxiliary supply is restored, the time and date will be correct and not need to be set again.

To test this, remove the IRIG-B signal, then remove the auxiliary supply from the relay. Leave the relay de-energized for approximately 30 seconds. On re-energization, the time in cell [0801: **DATE** and **TIME**, **Date/Time**] should be correct.

Reconnect the IRIG-B signal.

5.2.3.2 Without an IRIG-B signal

If the time and date is not being maintained by an IRIG-B signal, ensure that cell [0804: **DATE** and **TIME**, **IRIG-B Sync**.] is set to **Disabled**.

Set the date and time to the correct local time and date using cell [0801: **DATE** and **TIME**, **Date/Time**].

If the auxiliary supply fails, with a battery fitted in the compartment behind the bottom access cover, the time and date will be maintained. Therefore when the auxiliary supply is restored the time and date will be correct and not need to be set again.

To test this, remove the auxiliary supply from the relay for approximately 30 seconds. On re-energization, the time in cell [0801: **DATE** and **TIME**, **Date/Time**] should be correct.

5.2.4 Light emitting diodes (LED's)

On power up the green LED should switch on and stay on, indicating that the relay is healthy. The relay has non-volatile memory which stores the state (on or off) of the alarm, trip and, if configured to latch, user-programmable LED indicators when the relay was last energized from an auxiliary supply. Therefore these indicators may also switch on when the auxiliary supply is applied.

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If any of these LEDs are on, reset them before proceeding with further testing. If the LED successfully resets (the LED switches off), there is no testing required for that LED because it is known to be operational.

5.2.4.1 Testing the alarm and out of service LED's

The alarm and out of service LEDs can be tested using the **COMMISSIONING TESTS** menu column. Set cell [0F0D: **COMMISSIONING TESTS**, **Test Mode**] to **Contacts Blocked**. Check that the out of service LED is on continuously and the alarm LED flashes.

It is not necessary to return cell [0F0D: **COMMISSIONING TESTS**, **Test Mode**] to **Disabled** at this stage because the test mode will be required for later tests.

5.2.4.2 Testing the trip LED

The trip LED can be tested by initiating a manual circuit breaker trip from the relay. However, the trip LED will operate during the setting checks performed later. Therefore no further testing of the trip LED is required at this stage.

5.2.4.3 Testing the user-programmable LEDs

To test the user-programmable LEDs set cell [0F10: **COMMISSIONING TESTS**, **Test LED's**] to **Apply Test**. Check that all 8 (P342) or 18 (P343/4/5/6/8) programmable LEDs on the relay switch on.

5.2.5 Field voltage supply

The relay generates a field voltage of nominally 48 V that can be used to energize the opto-isolated inputs (alternatively the substation battery may be used).

Measure the field voltage across terminals 7 and 9 on the terminal block given in table 4. Check that the field voltage is within the range 40 V to 60 V when no load is connected and that the polarity is correct.

Note: The field voltage supply is only included in hardware version P34xxxxxxxxxxA-K.

Repeat for terminals 8 and 10.

Supply rail	Terminals		
	P342 (40TE)	P342/3/6 (60TE)	P343/4/5/6 (80TE)
+ve	F7 & F8	J7 & J8	M7 & M8
-ve	F9 & F10	J9 & J10	M9 & M10

Table 5: Field voltage terminals

5.2.6 Input opto-isolators

This test checks that all the opto-isolated inputs are functioning correctly. The P342 relay has 8 - 16 opto-isolated inputs in the 40TE case and 16 - 24 opto-isolated inputs in the 60TE case. The P343/6 relay has 16 - 24 opto-isolated inputs in the 60TE case and the P343/4/5/6 has 24 - 32 opto-isolated inputs in the 80TE case. The P348 has 16 - 32 opto-isolated inputs in the 80TE case.

Energize the opto-isolated inputs one at a time; see external connection diagrams in the Installation chapter (*P34x/EN IN*) for terminal numbers. Ensure that the correct opto input nominal voltage is set in the **Opto Config** menu. Ensure correct polarity and connect the field supply voltage to the appropriate terminals for the input being tested. Each opto input also has selectable filtering. This allows use of a pre-set filter of ½ cycle that renders the input immune to induced noise on the wiring.

Note: The opto-isolated inputs may be energized from an external dc auxiliary supply (for example the station battery) in some installations. Check that this is not the case before connecting the field voltage otherwise damage to the relay may result. If an external 24/27 V, 30/34 V, 48/54 V, 110/125 V, 220/250 V supply is being used it will be connected to the relay's optically isolated inputs directly. If an external supply is used it must be energized for this test, but only after confirming that it is suitably rated, with less than 12% ac ripple.

The status of each opto-isolated input can be viewed using either cell [0020: **SYSTEM DATA**, **Opto I/P Status**] or [0F01: **COMMISSIONING TESTS**, **Opto I/P Status**], a **1** indicating an energized input and a **0** indicating a de-energized input. When each opto-isolated input is energized, one of the characters on the bottom line of the display changes, to indicate the new state of the inputs.

5.2.7 Output relays

This test checks that all the output relays are functioning correctly. The P342 relay has 7 to 15 output relays in the 40TE case and 16 to 24 output relays in the 60TE case. The P343/6 relay has 14 to 22 output relays in the 60TE case and the P343/4/5/6 has 24 to 32 output relays in the 80TE case. The P348 relay has 16 to 32 output relays in the 80TE case.

Ensure that the cell [0F0D: **COMMISSIONING TESTS**, **Test Mode**] is set to **Contacts Blocked**.

The output relays should be energized one at a time. To select output relay 1 for testing, set cell [0F0E: **COMMISSIONING TESTS**, **Test Pattern**] 00000000000000000000000000000001.

Connect a continuity tester across the terminals corresponding to output relay 1 as shown in the external connection diagrams in the Installation chapter (*P34x/EN IN*).

To operate the output relay, set cell [0F0F: **COMMISSIONING TESTS**, **Contact Test**] to **Apply Test**. Operation is confirmed by the continuity tester operating for a normally open contact and ceasing to operate for a normally closed contact. Measure the resistance of the contacts in the closed state.

Reset the output relay by setting cell [0F0F: **COMMISSIONING TESTS**, **Contact Test**] to **Remove Test**.

Note: Ensure that the thermal ratings of anything connected to the output relays during the contact test procedure are not exceeded by the associated output relay being operated for too long. Keep the time between application and removal of contact test to a minimum.

Repeat the test for the rest of the relays.

Return the relay to service by setting cell [0F0D: **COMMISSIONING TESTS**, **Test Mode**] to **Disabled**.

5.2.8 RTD inputs

This test checks that all the RTD inputs are functioning correctly and is only performed on relays with the RTD board fitted that is P342/3/4/5/6 models.

A 100 Ω resistor, preferably with a tolerance of 0.1%, should be connected across each RTD in turn. The resistor needs to have a very small tolerance as RTDs complying to BS EN 60751: 1995 typically have a change of resistance of 0.39 Ω per °C, therefore the use of a precision wire wound or metal film resistor is recommended. It is essential to connect the RTD common return terminal to the appropriate RTD input otherwise the relay will report an RTD error as it will assume that the RTD wiring has been damaged. The connections required for testing each RTD input are given in table 5.

Check that the corresponding temperature displayed in the **MEASUREMENTS 3** column of the menu is 0°C ±2°C. This range takes into account the 0.1% resistor tolerance and relay accuracy of ±1°C. If a resistor of lower accuracy is used during testing the acceptable setting range will need to be increased.

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RTD	Terminal connections		Measurement cell (in 'Measurements 3' Column (04) of Menu)
	Resistor between	Wire between	
1	B1 and B2	B2 and B3	[0412: RTD 1 Label]
2	B4 and B5	B5 and B6	[0413: RTD 2 Label]
3	B7 and B8	B8 and B9	[0414: RTD 3 Label]
4	B10 and B11	B11 and B12	[0415: RTD 4 Label]
5	B13 and B14	B14 and B15	[0416: RTD 5 Label]
6	B16 and B17	B17 and B18	[0417: RTD 6 Label]
7	B19 and B20	B20 and B21	[0418: RTD 7 Label]
8	B22 and B23	B23 and B24	[0419: RTD 8 Label]
9	B25 and B26	B26 and B27	[041A: RTD 9 Label]
10	B28 and B29	B29 and B30	[041B: RTD 10 Label]

Table 6: RTD input terminals

5.2.9 Current loop inputs

This test checks that all the current loop (analog) inputs are functioning correctly and is only performed on relays with the CLIO (current loop input output) board fitted. The CLIO is an order option included in P342-8 models.

For details of the relay terminal connections see the connection diagrams in *P34x/EN IN*. For the current loop inputs the physical connection of the 0 - 1 mA input is different from that of the 0 - 10, 0 - 20 and 4 - 20 mA inputs, as shown in the connection diagrams.

An accurate dc current source can be used to apply various current levels to the current loop inputs. Another approach is to use the current loop output as a convenient and flexible dc current source to test the input protection functionality. Externally the current loop outputs can be fed into their corresponding current loop inputs. Then by applying a certain level of analog signal, such as V_A, to the relay the required dc output level can be obtained from the current loop output which is feeding the current loop input.

Enable the current loop input to be tested. Set the **CLIx Minimum** and **Maximum** settings and the **CLIx Input Type** for the application.

Apply a dc current to the relay current loop input at 50% of the CLI input maximum range, 0.5 mA (0 - 1 mA CLI), 5 mA (0 - 10 mA CLI) or 10 mA (0 - 20, 4 - 20 mA CLI).

Check the accuracy of the current loop input using the **MEASUREMENTS 3 - CLIO Input 1/2/3/4** column of the menu. The display should show (**CLIx Maximum** + **CLIx Minimum**)/2 ±1% full scale accuracy.

5.2.10 Current loop outputs

This test checks that all the current loop (analog) outputs are functioning correctly and is only performed on relays with the CLIO board fitted.

For details of the relay terminal connections, see the connection diagrams in *P34x/EN IN*.

Note: For the current loop outputs the physical connection of the 0 - 1 mA output is different from that of the 0 - 10, 0 - 20 and 4 - 20 mA outputs, as shown in the connection diagrams.

Enable the current loop output to be tested. Set the **CLOx Parameter**, **CLOx Minimum** and **Maximum** settings and the **CLOx Output Type** for the application. Apply the appropriate analog input parameter to the relay equals to (**CLOx Maximum** + **CLOx Minimum**)/2. The current loop output should be at 50% of its maximum rated output. Using a precision resistive current shunt and a high-resolution voltmeter, check that the current loop output is at 50% of its maximum rated output, 0.5 mA (0 - 1 mA CLO), 5 mA (0 - 10 mA CLO) or 10 mA (0 - 20, 4 - 20 mA CLO). The accuracy should be within ±0.5% of full scale + meter accuracy.

5.2.11 First rear communications port

This test should only be performed where the relay is to be accessed from a remote location and will vary depending on the communications standard being adopted.

It is not the intention of the test to verify the operation of the complete system from the relay to the remote location, just the relay's rear communications port and any protocol converter necessary.

5.2.11.1 Courier communications

If a K-Bus to EIA(RS)232 KITZ protocol converter is installed, connect a portable PC running the appropriate software (such as S1 Agile) to the incoming (remote from relay) side of the protocol converter.

If a KITZ protocol converter is not installed, it may not be possible to connect the PC to the relay installed. In this case a KITZ protocol converter and portable PC running appropriate software should be temporarily connected to the relay's first rear K-Bus port. The terminal numbers for the relay's first rear K-Bus port are given in table 6. However, as the installed protocol converter is not being used in the test, only the correct operation of the relay's

K-Bus port will be confirmed.

Connection		Terminal		
K-Bus	MODBUS, VDEW or DNP3.0	P342 (40TE)	P342/3/6 (60TE)	P343/4/5/6 (80TE)
Screen	Screen	F16	J16	M16
1	+ve	F17	J17	M17
2	-ve	F18	J18	M18

Table 7: EIA(RS)485 terminals

Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter (usually a KITZ but could be a SCADA RTU). The relay's Courier address in cell [0E02: **COMMUNICATIONS**, **RP1 Address**] must be set to a value between 1 and 254.

Check that communications can be established with this relay using the portable PC.

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: **COMMUNICATIONS**, **Physical Link**] to **Fiber Optic**. Ensure that the relay address and baud rate settings in the application software are set the same as those in cell [0E04 **COMMUNICATIONS**, **Baud Rate**] of the relay. Check that, using the Master Station, communications with the relay can be established.

5.2.11.2 MODBUS communications

Connect a portable PC running the appropriate MODBUS Master Station software to the relay's first rear EIA(RS)485 port via an EIA(RS)485 to EIA(RS)232 interface converter. The terminal numbers for the relay's EIA(RS)485 port are given in Table 7.

Ensure that the relay address, baud rate and parity settings in the application software are set the same as those in cells [0E02: **COMMUNICATIONS**, **RP1 Address**], [0E04: **COMMUNICATIONS**, **Baud Rate**] and [0E05: **COMMUNICATIONS**, **Parity**] of the relay.

Check that communications with this relay can be established.

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: **COMMUNICATIONS**, **Physical Link**] to **Fiber Optic**. Ensure that the relay address and baud rate settings in the application software are set the same as those in cell [0E04: **COMMUNICATIONS**, **Baud Rate**] of the relay. Check, using the Master Station, communications with the relay can be established.

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5.2.11.3 IEC60870-5-103 (VDEW) communications

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: **COMMUNICATIONS**, **Physical Link**] to **Fiber Optic** or **EIA(RS)485**.

IEC60870-5-103/VDEW communication systems are designed to have a local Master Station and this should be used to verify that the relay's rear fiber optic or EIA(RS)485 port, as appropriate, is working.

Ensure that the relay address and baud rate settings in the application software are set the same as those in cells [0E02: **COMMUNICATIONS**, **RP1 Address**] and [0E04: **COMMUNICATIONS**, **Baud Rate**] of the relay.

Check that, using the Master Station, communications with the relay can be established.

5.2.11.4 DNP3.0 communications (serial)

Connect a portable PC running the appropriate DNP3.0 Master Station Software to the relay's first rear EIA(RS)485 port via an EIA(RS)485 to EIA(RS)232 interface converter. The terminal numbers for the relay's EIA(RS)485 port are given in Table 7.

Ensure that the relay address, baud rate and parity settings in the application software are set the same as those in cells [0E02: **COMMUNICATIONS**, **RP1 Address**], [0E04: **COMMUNICATIONS**, **Baud Rate**] and [0E05: **COMMUNICATIONS**, **Parity**] of the relay.

Check that communications with this relay can be established.

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: **COMMUNICATIONS**, **Physical Link**] to **Fiber Optic**. Ensure that the relay address and baud rate settings in the application software are set the same as those in cell [0E04: **COMMUNICATIONS**, **Baud Rate**] of the relay. Check that, using the Master Station, communications with the relay can be established.

5.2.12 Ethernet communications port

This test should only be performed where the relay is to be accessed from a remote location using the optional Ethernet interface.

It is not the intention of the test to verify the operation of the complete system from the relay to the remote location, just the relay's Ethernet communications port.

5.2.12.1 IEC 61850 communications

The Ethernet communications interface for IEC 61850 can be tested either by using an IEC 61850 client application or MMS browser application or using S1 Agile.

Configuration of the relay IP parameters (**IP Address, SubNet Mask, Gateway Address**), Ethernet media and optional SNTP time synchronization parameters is performed by the IED Configurator tool. If these parameters are not available to import from an SCL file, they must be configured manually.

If the relay has one of the optional single Ethernet communications interfaces fitted, the port to be used should be selected using the IED Configurator tool [**Communications, Media**] to **Single Fibre** (for optical fibre) or **Single Copper or Redundant Fibre** (for single copper).

If the relay has one of the optional redundant Ethernet communications interfaces fitted, the port to be used should be selected using the IED Configurator tool [**Communications, Media**] to **Single Copper or Redundant Fibre**.

Send the IED Configurator parameters to the relay using the front port serial connection of the relay.

If using S1 Agile to test the Ethernet connection, it will also be necessary to set the relay's RP1 address in cell [0E02: **COMMUNICATIONS, RP1 Address**] to a value between 1 and 254.

Connect the portable PC running the appropriate IEC 61850 client application or MMS browser application or S1 Agile to the relay's Ethernet port. A standard "Fast Ethernet" copper cable with RJ45 connectors is used for the relay's single copper Ethernet port. 1300 nm multimode optical fibres with ST connectors are used for the relay's single or redundant fibre Ethernet ports. If using single copper or single fibre, it may be necessary to use an Ethernet switch to connect the relay to the portable PC. If using redundant fibre, it will be necessary to use an appropriate redundant Ethernet switch that matches the method of redundancy of the relay's Ethernet communications interface, for example PRP, to connect the relay to the portable PC.

If the assigned IP address is duplicated elsewhere on the same network, the remote communications will operate in an indeterminate way. However, the relay will check for a conflict on every IP configuration change and at power up. An alarm will be raised if an IP conflict is detected. The relay can be configured to accept data from networks other than the local network by using the **Gateway Address** setting.

Check that communications with this relay can be established. If using S1 Agile, select **Ethernet port** for the port selection, then enter the IP address and RP1 address to match the configuration, then verify the communications by extracting configuration or events files.

5.2.12.2 DNP 3.0 over Ethernet communications

The Ethernet communications interface for DNP 3.0 can be tested either by using a DNP 3.0 Ethernet client application or using S1 Agile.

Configuration of the relay IP parameters (**IP Address, Subnet Mask, Gateway**), Ethernet media and optional SNTP time synchronization parameters is performed by the DNP Settings File in S1 Agile. If these parameters are not available to import from an SCL file, they must be configured manually.

If the relay has one of the optional single Ethernet communications interfaces fitted, the port to be used should be selected using the IED Configurator tool [**Communications, Media**] to **Single Fibre** (for optical fibre) or **Single Copper or Redundant Fibre** (for single copper).

If the relay has one of the optional redundant Ethernet communications interfaces fitted, the port to be used should be selected using the IED Configurator tool [**Communications, Media**] to **Single Copper or Redundant Fibre**.

Send the DNP Settings File to the relay using the front port serial connection of the relay.

If using S1 Agile to test the Ethernet connection, it will also be necessary to set the relay's RP1 address in cell [0E02: **COMMUNICATIONS, RP1 Address**] to a value between 1 and 254.

Connect the portable PC running the appropriate DNP 3.0 Ethernet client application or S1 Agile to the relay's Ethernet port. A standard "Fast Ethernet" copper cable with RJ45 connectors is used for relay's single copper Ethernet port. 1300 nm multimode optical fibres with ST connectors are used for the relay's single or redundant fibre Ethernet ports. If using single copper or single fibre, it may be necessary to use an Ethernet switch to connect the relay to the portable PC. If using redundant fibre, it will be necessary to use an appropriate redundant Ethernet switch that matches the method of redundancy of the relay's Ethernet communications interface, for example PRP, to connect the relay to the portable PC.

If the assigned IP address is duplicated elsewhere on the same network, the remote communications will operate in an indeterminate way. However, the relay will check for a conflict on every IP configuration change and at power up. An alarm will be raised if an IP conflict is detected. The relay can be configured to accept data from networks other than the local network by using the **Gateway Address** setting.

Check that communications with this relay can be established. If using S1 Agile, select Ethernet port for the port selection, then enter the IP address and RP1 address to match the configuration, then verify the communications by extracting configuration or events files.

5.2.13 Second rear communications port

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This test should only be performed where the relay is to be accessed from a remote location and will vary depending on the communications standard being adopted.

It is not the intention of the test to verify the operation of the complete system from the relay to the remote location, just the relay's rear communications port and any protocol converter necessary.

5.2.13.1 K-Bus configuration

If a K-Bus to EIA(RS)232 KITZ protocol converter is installed, connect a portable PC running the appropriate software (such as S1 Agile or PAS&T) to the incoming (remote from relay) side of the protocol converter.

If a KITZ protocol converter is not installed, it may not be possible to connect the PC to the relay installed. In this case a KITZ protocol converter and portable PC running appropriate software should be temporarily connected to the relay's second rear communications port configured for K-Bus. The terminal numbers for the relay's K-Bus port are given in Table 8. However, as the installed protocol converter is not being used in the test, only the correct operation of the relay's K-Bus port will be confirmed.

Pin*	Connection
4	EIA(RS)485 - 1 (+ ve)
7	EIA(RS)485 - 2 (- ve)

Table 8: 2nd rear communications port K-Bus terminals

* - All other pins unconnected.

Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter (usually a KITZ but could be a SCADA RTU). The relay's Courier address in cell [0E90: **COMMUNICATIONS**, **RP2 Address**] must be set to a value between 1 and 254. The second rear communication's port configuration [0E88: **COMMUNICATIONS**, **RP2 Port Config**.] must be set to K-Bus.

Check that communications can be established with this relay using the portable PC.

5.2.13.2 EIA(RS)485 configuration

If an EIA(RS)485 to EIA(RS)232 converter is installed, connect a portable PC running the appropriate software (for example S1 Agile) to the EIA(RS)232 side of the converter and the second rear communications port of the relay to the EIA(RS)485 side of the converter.

The terminal numbers for the relay's EIA(RS)485 port are given in Table 8.

Ensure that the communications baud rate and parity settings in the application software are set the same as those in the relay. The relay's Courier address in cell [0E90: **COMMUNICATIONS**, **RP2 Address**] must be set to a value between 1 and 254. The second rear communication's port configuration [0E88: **COMMUNICATIONS**, **RP2 Port Config**] must be set to EIA(RS)485.

Check that communications can be established with this relay using the portable PC.

5.2.13.3 EIA(RS)232 configuration

Connect a portable PC running the appropriate software (for example S1 Agile) to the rear EIA(RS)232[1] port of the relay.

The second rear communications port connects via the 9-way female D-type connector (SK4). The connection is compliant to EIA(RS)574.

Pin	Connection
1	No Connection
2	RxD
3	TxD
4	DTR#
5	Ground
6	No Connection
7	RTS#
8	CTS#
9	No Connection

Table 9: Second rear communications port EIA(RS)232 terminals

- These pins are control lines for use with a modem.

Connections to the second rear port configured for EIA(RS)232 operation can be made using a screened multi-core communication cable up to 15 m long, or a total capacitance of 2500 pF. The cable should be terminated at the relay end with a 9-way, metal shelled, D-type male plug. The terminal numbers for the relay's EIA(RS)232 port are given in Table 9.

Ensure that the communications baud rate and parity settings in the application software are set the same as those in the relay. The relay's Courier address in cell [0E90: **COMMUNICATIONS**, **RP2 Address**] must be set to a value between 1 and 254. The second rear communication's port configuration [0E88: **COMMUNICATIONS RP2**, **Port Config**] must be set to EIA(RS)232.

Check that communications can be established with this relay using the portable PC.

[1] This port is actually compliant to EIA(RS)574; the 9-pin version of EIA(RS)232, see www.tiaonline.org.

5.2.14 IEC 61850-9-2 LE configuration (P348)

5.2.14.1 IEC 61850-9-2 LE configuration (P348) with one logical node

The settings for the IEC 61850-9-2LE interface are in the IED menu IEC 61850-9-2LE. See the Settings chapter.

1. If necessary, isolate or block any outgoing trips from the IED. If physical contacts from the IED are wired in the scheme, from the main IED menu select Test Mode.
2. Connect the IED's IEC 61850-9-2LE port to the Sampled Value source. If necessary this can be routed through an Ethernet switch.
3. In the IED menu setting IEC 61850-9-2LE > Physical Link, select Fibre Optic for receiving Sampled Values.
4. Check that the Logical Node name in the IED matches the name in the Sampled Value source (test kit or Merging Unit). Make any changes in the source Logical Node names. This prevents mismatches in Logical Node names when the IED is put into service when testing existing schemes.
5. Set the IED Synchro Alarm to No SYNC CLK so the IED accepts Sampled Value frames with or without synchronisation.
6. Generate Sampled Value frames with the current and voltage as required in the IED's Logical Node configuration for the tests required in the sections below, 5.2.15, 5.2.16, 6.3.7.
7. Change the Logical Node name configured in the test kit. Check the data cell SAV Absence displays '0' for the Logical Node configured in the IED. Check that all MEASUREMENTS displays for voltage or current are zero.
8. Depending on the scheme, use the Synchro Alarm setting to return the IED to service. Re-enable the IED trip outputs. If the RJ45 port was used for testing, change the setting IEC 61850-9-2LE > Physical Link to Fibre Optic.

5.2.14.2 IEC 61850-9-2 LE configuration (P348) with two or more logical nodes

The settings for the IEC 61850-9-2LE interface are in the IED menu IEC 61850-9-2LE.

1. If necessary, isolate or block any outgoing trips from the IED. If physical contacts from the IED are wired in the scheme, from the main IED menu select Test Mode.
2. Connect the IED's IEC 61850-9-2LE port to an Ethernet switch, which is connected to the Sampled Value sources. In the IED menu setting *IEC 61850-9-2LE* then ***Physical Link,*** select *Fibre Optic* for receiving Sampled Values.
3. Check that the Logical Node name in the IED matches the name in the Sampled Value source (test kit or Merging Unit). Make any changes in the source Logical Node names. This prevents mismatches in Logical Node names when the IED is put into service when testing existing schemes.
4. Set the IED ***Synchro Alarm*** to *Local 1PPS* so the IED accepts Sampled Value frames with local or global synchronisation.
5. Check that the Sampled Value source (test kit or Merging Unit) is GPS synchronised.
6. Check the receipt of Sampled Value frames one by one for each Logical Node configured in the IED.

Repeat the following steps for each Logical Node, configuring them one by one in the Sampled Value source(s).

1. Generate Sampled Value frames with the current and voltage as required in the IED's Logical Node configuration for the tests required in the sections below 5.2.15, 5.2.16, 6.3.7. You can check the receipt of Sampled Value frames for the configured Logical Node.

2. Change the Logical Node name configured in the test kit. Check the data cell ***SAV Absence*** displays '0' for the Logical Node configured in the IED. Check that all *MEASUREMENTS* displays for voltage or current are zero.

If the GPS signal is lost, repeat the following steps for each Logical Node.

1. Check the data cell ***9-2 Sample Alarm***.
2. Turn off the GPS to the Sampled Value source and turn it on again. Binary flags for respective Logical Node should indicate '1' for loss of GPS and return to '0' when the GPS is healthy.
3. Depending on the scheme, use the ***Synchro Alarm*** setting to return the IED to service. Re-enable the IED trip outputs. If the RJ45 port was used for testing, change the setting *IEC 61850-9-2LE* then ***Physical Link*** to *Fibre Optic*.

5.2.15 Current inputs

This test verifies that the accuracy of current measurement is within the acceptable tolerances.

All relays will leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required then this must be set in cell [0009: **SYSTEM DATA**, **Frequency**].

Apply current equal to the line current transformer secondary winding rating to each current transformer input of the corresponding rating in turn, checking its magnitude using a multimeter. Refer to Table 10 for the corresponding reading in the relay's **MEASUREMENTS 1** or **MEASUREMENTS 3** columns, as appropriate, and record the value displayed.

The P348 uses an IEC 61850-9-2 LE Ethernet port to obtain sampled values of current and voltage. For this relay apply IEC 61850-9-2 LE sampled values of current equal to the line current transformer secondary winding rating to each current input of the corresponding rating in turn, checking its magnitude using the test set. Refer to Table 12 for the corresponding reading in the relay's **MEASUREMENTS 1** column, as appropriate, and record the value displayed.

Menu cell	Apply current to			
	P342 (40TE) P343/6 (60TE)		P342 (60TE) P343/4/5/6 (80TE)	
	1A CT's	5A CT's	1A CT's	5A CT's
[0201: MEASUREMENTS 1, IA Magnitude]	C3 - C2	C1 - C2	D3 - D2	D1 - D2
[0203: MEASUREMENTS 1, IB Magnitude]	C6 - C5	C4 - C5	D6 - D5	D4 - D5
[0205: MEASUREMENTS 1, IC Magnitude]	C9 - C8	C7 - C8	D9 - D8	D7 - D8
[0207: MEASUREMENTS 1, IN Measured Mag]	C12 - C11	C10 - C11	D12 - D11	D10 - D11
[020B: MEASUREMENTS 1, ISEN1 Magnitude]	C15 - C14	C13 - C14	D15 - D14	D13 - D14
[022A: MEASUREMENTS 1, ISEN2 Magnitude] (P345 only)			F15 - F14	F13 - F14
[0401: MEASUREMENTS 3, IA-2 Magnitude] (P343/4/5/6 only)	E3 - E2	E1 - E2	F3 - F2	F1 - F2
[0403: MEASUREMENTS 3, IB-2 Magnitude] (P343/4/5/6 only)	E6 - E5	E4 - E5	F6 - F5	F4 - F5
[0405: MEASUREMENTS 3, IC-2 Magnitude] (P343/4/5/6 only)	E9 - E8	E7 - E8	F9 - F8	F7 - F8

Table 10: Current input terminals (P342-6)

The measured current values displayed on the relay LCD or a portable PC connected to the front communication port will either be in primary or secondary Amperes. If cell [0D02: **MEASURE'T SETUP**, **Local Values**] is set to **Primary**, the values displayed should be equal to the applied current multiplied by the corresponding current transformer ratio set in the **CT and VT RATIOS** menu column (see Table 11). If cell [0D02: **MEASURE'T SETUP, Local Values**] is set to **Secondary**, the value displayed should be equal to the applied current.

Note: If a PC connected to the relay via the rear communications port is being used to display the measured current, the process will be similar. However, the setting of cell [0D03: **MEASURE'T SETUP**, **Remote Values**] will determine whether the displayed values are in primary or secondary Amperes.

The measurement accuracy of the relay is ±1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

Menu cell	Corresponding CT ratio (in 'VT and CT RATIO column (0A) of menu)
[0201: MEASUREMENTS 1, IA-1 Magnitude] [0203: MEASUREMENTS 1, IB-1 Magnitude] [0205: MEASUREMENTS 1, IC-1 Magnitude]	[0A32: Phase CT1 Primary] [0A33: Phase CT1 Sec'y]
[0401: MEASUREMENTS 3, IA - 2 Magnitude] (P343/4/5/6 only) [0403: MEASUREMENTS 3, IB - 2 Magnitude] (P343/4/5/6 only) [0405: MEASUREMENTS 3, IC - 2 Magnitude] (P343/4/5/6 only)	[0A37: Phase CT2 Primary] [0A38: Phase CT2 Sec'y]
[0207: MEASUREMENTS 1, IN Measured Mag]	[0A09: E/F CT Primary] [0A0A: E/F CT Sec'y]
[020B: MEASUREMENTS 1, ISEN1 Magnitude] [022A: MEASUREMENTS 1, ISEN2 Magnitude] (P345 only)	[0A0B: SEF CT Primary] [0A0C: SEF CT Sec'y]

Table 11: CT ratio settings P342-6

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Menu cell	Corresponding CT ratio (in 'VT and CT RATIO column (0A) of menu)
[0210: MEASUREMENTS 1, IA-1 RMS] [0211: MEASUREMENTS 1, IB-1 RMS] [0212: MEASUREMENTS 1, IC-1 RMS] [0280: MEASUREMENTS 1, IA-2 RMS] [0281: MEASUREMENTS 1, IB-2 RMS] [0282: MEASUREMENTS 1, IC-2 RMS]	[0A07: Phase CT Primary] [0A08: Phase CT Sec'y]

Table 12: CT ratio settings P348

5.2.16 Voltage inputs

This test verifies the accuracy of voltage measurement is within the acceptable tolerances.

Apply rated voltage to each voltage transformer input in turn, checking its magnitude using a multimeter. Refer to Table 13 for the corresponding reading in the relay's MEASUREMENTS 1 column and record the value displayed.

The P348 uses an IEC 61850-9-2 LE Ethernet port to obtain sampled values of current and voltage. For this relay apply IEC 61850-9-2 LE sampled values of voltage equal to the line voltage transformer secondary winding rating to each voltage input of the corresponding rating in turn, checking its magnitude using the test set. Refer to Table 15 for the corresponding reading in the relay's MEASUREMENTS 1 column, as appropriate, and record the value displayed.

Menu cell	Voltage applied to	
	P342 (40TE), P343/6 (60TE)	P342 (60TE), P343/4/5/6 (80TE)
[021A: MEASUREMENTS 1, VAN Magnitude]	C19 - C22	D19 - D22
[021C: MEASUREMENTS 1, VBN Magnitude]	C20 - C22	D20 - D22
[021E: MEASUREMENTS 1, VCN Magnitude]	C21 - C22	D21 - D22
[0220: MEASUREMENTS 1, VN Measured Mag]	C23 - C24	D23 - D24
[0250: MEASUREMENTS 1, VN2 Measured Mag] (P344/5 only)		F23 - F24
[0270: MEASUREMENTS 1, C/S Voltage Mag] (P345 only)		F19 - F20

Table 13: Voltage input terminals

The measured voltage values displayed on the relay LCD or a portable PC connected to the front communication port will either be in primary or secondary volts. If cell [0D02: **MEASURE'T SETUP**, **Local Values**] is set to **Primary**, the values displayed should be equal to the applied voltage multiplied by the corresponding voltage transformer ratio set in the **VT and CT RATIOS** menu column (see Table 14). If cell [0D02: **MEASURE'T SETUP**, **Local Values**] is set to **Secondary**, the value displayed should be equal to the applied voltage.

Note: If a PC connected to the relay via the rear communications port is being used to display the measured voltage, the process will be similar. However, the setting of cell [0D03: **MEASURE'T SETUP**, **Remote Values**] will determine whether the displayed values are in primary or secondary volts.

The measurement accuracy of the relay is ±1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

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Menu cell	Corresponding VT ratio (in VT and CT RATIO column (0A) of menu)
[021A: MEASUREMENTS 1, VAN Magnitude] [021C: MEASUREMENTS 1, VBN Magnitude] [021E: MEASUREMENTS 1, VCN Magnitude]	[0A01: Main VT Primary] [0A02: Main VT Sec'y]
[0220: MEASUREMENTS 1, VN Measured Mag]	[0A05: VN VT Primary] [0A06: VN VT Sec'y]
[0250: MEASUREMENTS 1, VN2 Measured Mag] (P344/5 only)	[0A03: VN2 VT Primary] [0A04: VN2 VT Sec'y]
[0270: MEASUREMENTS 1, C/S Voltage Mag] (P345 only)	[0A16: C/S VT Prim'y] [0A17: C/S VT Sec'y]

Table 14: VT ratio settings P342-6

Menu cell	Corresponding VT ratio (in VT and CT RATIO column (0A) of menu)
[028B: MEASUREMENTS 1, VA-1 RMS] [028C: MEASUREMENTS 1, VB-1 RMS] [028D: MEASUREMENTS 1, VC-1 RMS] [028E: MEASUREMENTS 1, VN-1 Derived RMS]	[0A01: Main VT Primary] [0A02: Main VT Sec'y]

Table 15: VT ratio settings P348

6 SETTING CHECKS

The setting checks ensure that all of the application-specific relay settings (both the relay's function and programmable scheme logic settings) for the particular installation have been correctly applied to the relay.

If the application-specific settings are not available, ignore sections 6.1 and 6.2.

Note: The trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.

6.1 Apply application-specific settings

There are two methods of applying the settings:

- Transferring them from a pre-prepared setting file to the relay using a portable PC running the appropriate software (S1 Agile) via the relay's front EIA(RS)232 port, located under the bottom access cover, or the first rear communications port (Courier protocol with a KITZ protocol converter connected), or the second rear communications port. This method is preferred for transferring function settings as it is much faster and there is less margin for error. If programmable scheme logic other than the default settings with which the relay is supplied is to be used then this is the only way of changing the settings.
- If a setting file has been created for the particular application and provided on a diskette, this will further reduce the commissioning time and should always be the case where application-specific programmable scheme logic is to be applied to the relay.

Enter them manually via the relay's operator interface. This method is not suitable for changing the programmable scheme logic.



Note: It is essential that where the installation needs application-specific Programmable Scheme Logic that the appropriate .psl file is downloaded (sent) to the relay, for each and every setting group that will be used. If the user fails to download the required .psl file to any setting group that may be brought into service, then factory default PSL will still be resident. This may have severe operational and safety consequences.

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6.2 Check application-specific settings

Carefully check applied settings against the required application-specific settings to ensure they have been entered correctly. However, this is not considered essential if a customer-prepared setting file on diskette has been transferred to the relay using a portable PC.

There are two methods of checking the settings:

- Extract the settings from the relay using a portable PC running the appropriate software (S1 Agile) via the front EIA(RS)232 port, located under the bottom access cover, or the first rear communications port (Courier protocol with a KITZ protocol converter connected), or the second rear communications port. Compare the settings transferred from the relay with the original written application-specific setting record. (For cases where the customer has only provided a printed copy of the required settings but a portable PC is available).

Step through the settings using the relay's operator interface and compare them with the original application-specific setting record.

Unless previously agreed to the contrary, the application-specific programmable scheme logic will not be checked as part of the commissioning tests.

Due to the versatility and possible complexity of the programmable scheme logic, it is beyond the scope of these commissioning instructions to detail suitable test procedures. Therefore, when programmable scheme logic tests must be performed, written tests which will satisfactorily demonstrate the correct operation of the application-specific scheme logic

should be devised by the Engineer who created it. These should be provided to the Commissioning Engineer together with the diskette containing the programmable scheme logic setting file.

6.3 Demonstrate correct relay operation

Tests 5.2.13 and 5.2.14 have already demonstrated that the relay is within calibration, therefore the purpose of these tests is as follows:

- To confirm that the primary protection function of the P343/4/5/6 relay, the generator or generator-transformer differential protection or the primary protection of the P348, overcurrent protection can trip according to the correct application settings.
- To verify correct setting of the backup phase overcurrent protection (P342/3/4/5/6).

To verify correct assignment of the trip contacts, by monitoring the response to a selection of fault injections.

6.3.1 Generator differential protection (P343/4/5/6)

To avoid spurious operation of any other protection elements, all protection elements except the generator differential protection should be disabled for the duration of the differential element tests. This is done in the relay's **CONFIGURATION** column. Make a note of which elements need to be re-enabled after testing. The generator differential protection is selected by the **SYSTEM CONFIG – Winding Config – Generator** setting.

For testing the biased differential protection select the **Biased** setting in the **GEN DIFF**, **Gen Diff Func** menu and perform the tests described in section 6.3.1.2, 6.3.1.3 and 6.3.2. For testing the high impedance differential protection select the **High Impedance** setting in the **GEN DIFF**, **Gen Diff Func** menu and perform the tests described in section 6.3.2.

The P343/4/5/6 generator differential protection has three elements, one for each phase. The biased differential protection uses the maximum bias current in the three phases to bias the elements. The detailed bias characteristic is described in sub-document - Installation. The following instructions are for testing the bias characteristic of the B phase element. The bias current is applied to the A phase element.

6.3.1.1 Connect the test circuit

The following tests require a variable transformer and two resistors connected as shown in Figure 3. Alternatively an injection test set can be used to supply Ia and Ib currents.

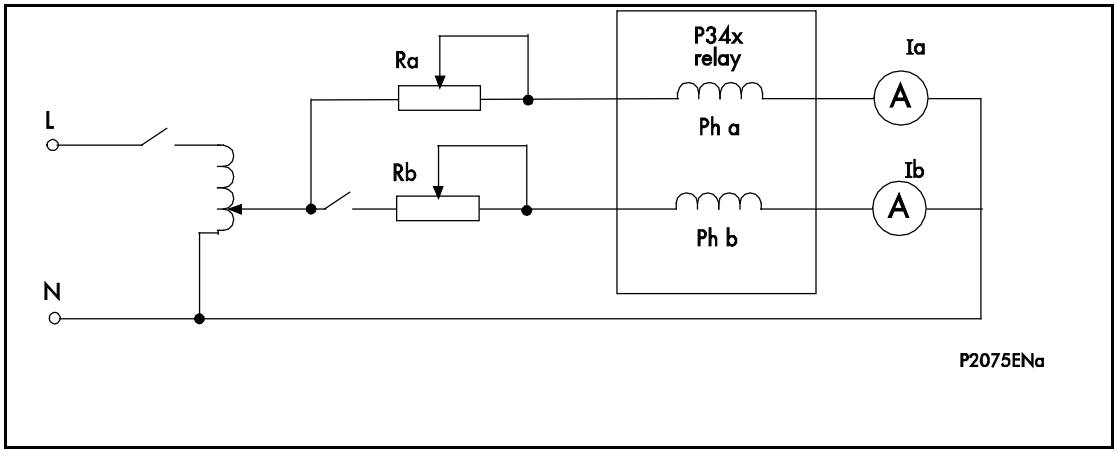


Figure 3: Connection for testing

For the biased differential protection a current is injected into the A phase IA-2 input, (E3 - E2 (1A, 60TE case), E1 - E2 (5A, 60TE case), F3 - F2 (1A, 80TE case), F1 - F2 (5A, 80TE case)), which is used as the bias current, IBias = (IA + IA-2)/2 = IA-2/2 as IA=0. Another current is injected into the B phase IB-2 input (E6 - E5 (1A, 60TE case), E4 - E5 (5A, 60TE case), F6 - F5 (1A, 80TE case), F4 - F5 (5A, 80TE case)) which is used as the differential current, Differential = IB-2 - IB = IB-2 as IB=0. Ia is always greater than Ib.

6.3.1.2 Biased differential protection lower slope

If three LEDs have been assigned to give phase segregated trip information, Gen Diff Trip A, Gen Diff Trip B and Gen Diff Trip C (DDB 737, 738, 739), these may be used to indicate correct per-phase operation. If not, monitor options will need to be used - see the next paragraph.

Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F05: **Monitor Bit 1**] to 737, [0F06: **Monitor Bit 2**] to 738 and [0F07: **Monitor Bit 3**] to 739. Cell [0F04: **Test Port Status**] will now appropriately set or reset the bits that now represent Phase A Trip (DDB 737), Phase B Trip (DDB 738) and Phase C Trip (DDB 739) with the rightmost bit representing Phase A Trip. From now on you should monitor the indication of [0F04: Test Port Status].

Adjust the variac and the resistor to inject 1 pu into IA-2 to give a bias current of 0.5 pu in the A-phase.

Note: 1pu = 1A into terminals E3 - E2 (60TE case), F3 - F2 (80TE case) for 1A applications; or 1 pu = 5A into terminals E1 - E2 (60TE case), F1-F2 (80TE case) for 5A applications).

The relay will trip and any contacts associated with the A-phase will operate, and bit 1 (rightmost) of [0F04: **Test Port Status**] will be set to 1. Some LEDs, including the yellow alarm LED, will come on, but ignore them for the moment.

Slowly increase the current in the B-phase IB-2 input E6 - E5 (1A, 60TE), E4 - E5 (5A, 60TE case), F6 - F5 (1A, 80TE case), F4 - F5 (5A, 80TE case) until phase B trips

(Bit 2 of [0F04: **Test Port Status**] is set to 1). Record the phase B current magnitude and check that it corresponds to the information below.

Switch OFF the ac supply and reset the alarms.

Bias current (IA-2/2)		Differential current (IB)	
Phase	**Magnitude**	**Phase**	**Magnitude**
A	0.5 pu	B	0.0 5 pu +/-10%

Table 16: Biased differential lower scope test currents

Assumption: Is1 = 0.05 pu, k1 = 0%, Is2 = 1.2 pu

For other differential settings the formula below can be used (enter k1 slope in pu form, for example percentage/100):

B phase operate current is (Is1 + IBias x k1) pu +/- 10%

6.3.1.3 Biased differential protection upper slope

Repeat the test in 6.2.1.2 with the A phase, IA-2, current set to be 3.4 pu (Ibias = 1.7 pu).

Slowly increase the current in the B phase until phase B trips (bit 2 of [0F04: **Test Port Status**] is set to 1). Record the phase B current magnitude and check that it corresponds to the information below.

Switch OFF the ac supply and reset the alarms.

Bias current (IA-2/2)		Differential current (IB)	
Phase	**Magnitude**	**Phase**	**Magnitude**
A	1.7 pu	B	0.8 pu +/-20%

Table 17: Biased differential upper scope test currents

Assumption: Is1 = 0.05 pu, k1 = 0%, Is2 = 1.2 pu, k2 =150%as above

For other differential settings the formula below can be used (enter k1 and k2 slopes in pu form, for example percentage/100):

Operate current is [(IBias x k2) + {(k1 – k2) x Is2 } + Is1] pu +/- 20%

Note: Particularly for 5A applications the duration of current injections should be short to avoid overheating of the variac or injection test set.

6.3.2 Generator differential operation and contact assignment

6.3.2.1 Phase A

Retaining the same test circuit as before, prepare for an instantaneous injection of 4 x Is1 pu current in the A phase, with no current in the B phase (B phase switch open). Connect a timer to start when the fault injection is applied, and to stop when the trip occurs.

Determine which output relay has been selected to operate when a Gen Diff Trip occurs by viewing the relay's programmable scheme logic. The programmable scheme logic can only be changed using the appropriate software. If this software is not available then the default output relay allocations will still be applicable. In the default PSL, relay 3 is the designated protection trip contact and DDB 736 Gen Diff Trip is assigned to this contact. If the generator differential trip is not mapped directly to an output relay in the programmable scheme logic, output relay 3 (H5-H6 in the 60TE case and L5-L6 in the 80TE case) should be used for the test as relay 3 initiates the trip led.

Ensure that the timer is reset.

Apply a current of 4 x the setting in cell [3002: **GROUP 1 GEN DIFF**, **Gen Diff Is1**] to the relay and note the time displayed when the timer stops.

After applying the test check the red trip led and yellow alarm led turns on when the relay operates. Check 'Alarms/Faults Present - Tripped Phase A, Gen Diff Trip' is on the display. Reset the alarms.

Three Pole Tripping	DDB 736:	Gen Diff Trip
Single Pole Tripping	DDB 737:	Gen Diff Trip A
	DDB 738:	Gen Diff Trip B
	DDB 739:	Gen Diff Trip C

Table 18: Generator differential protection DDBs

6.3.2.2 Phase B

Reconfigure the test equipment to inject fault current into the B phase. Repeat the test in 6.3.2.1, this time ensuring that the breaker trip contacts relative to B phase operation close correctly. Record the phase B trip time. Check the red trip led and yellow alarm led turns on when the relay operates. Check 'Alarms/Faults Present - Tripped Phase B, Gen Diff Trip' is on the display. Reset the alarms.

6.3.2.3 Phase C

Repeat 0 for the C phase.

The average of the recorded operating times for the three phases should be less than 30 ms. Switch OFF the ac supply and reset the alarms.

On completion of the tests any protection elements which were disabled for testing purposes must have their original settings restored in the **CONFIGURATION** column.

6.3.3 Backup phase overcurrent protection (P342/3/4/5/6)

The overcurrent protection function I>1 element should be tested.

To avoid spurious operation of any other protection elements all protection elements except the overcurrent protection should be disabled for the duration of the overcurrent element tests. This is done in the relay's **CONFIGURATION** column. Make a note of which elements need to be re-enabled after testing.

6.3.3.1 Connect the test circuit

Determine which output relay has been selected to operate when a I>1 trip occurs by viewing the relay's programmable scheme logic.

The programmable scheme logic can only be changed using the appropriate software. If this software has not been available then the default output relay allocations will still be applicable.

If the trip outputs are phase-segregated (that is a different output relay allocated for each phase), the relay assigned for tripping on 'A' phase faults should be used.

If stage 1 is not mapped directly to an output relay in the programmable scheme logic, output relay 3 (H5 - H6 in the 60TE case and L5 - L6 in the 80TE case) should be used for the test as relay 3 initiates the trip LED. In the default PSL relay 3 is the designated protection trip contact and DDB 800 I>1 Trip is assigned to this contact.

Three Pole Tripping	DDB 800:	I>1 Trip
Single Pole Tripping	DDB 801:	I>1 Trip A
	DDB 802:	I>1 Trip B
	DDB 803:	I>1 Trip C

Table 19: Overcurrent protection DDBs

The associated terminal numbers can be found from the external connection diagrams in the Installation chapter *P34x/EN IN*.

Connect the output relay so that its operation will trip the test set and stop the timer.



Connect the current output of the test set to the 'A' phase current transformer input of the relay (terminals C3 - C2 (1A, 60TE case), D3 - D2 (1A, 80TE case) C1 - C2 (5A, 60TE case), D1 - D2 (5A, 80TE case)).

Ensure that the timer will start when the current is applied to the relay.

6.3.3.2 Perform the test

Ensure that the timer is reset.

Apply a current of twice the setting in cell [3504: **GROUP 1 OVERCURRENT**, **I>1 Current Set**] to the relay and note the time displayed when the timer stops.

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Check the red trip led and yellow alarm led turns on when the relay operates. Check 'Alarms/Faults Present - Started Phase A, Tripped Phase A, Overcurrent Start I>1, Overcurrent Trip I>1' is on the display. Reset all alarms.

Note: The trip led is initiated from operation of relay 3, the protection trip contact in the default PSL.

6.3.3.3 Check the operating time

Check that the operating time recorded by the timer is within the range shown in table 13.

Note: Except for the definite time characteristic, the operating times given in table 13 are for a time multiplier or time dial setting of 1. Therefore to obtain the operating time at other time multiplier or time dial settings, the time given in table 12 must be multiplied by the setting of cell [3506: **GROUP 1 OVERCURRENT**, **I>1 TMS**] for IEC and UK characteristics or cell [3507: **GROUP 1 OVERCURRENT**, **Time Dial**] for IEEE and US characteristics.

In addition, for definite time and inverse characteristics there is an additional delay of up to 0.02 second and 0.08 second respectively that may need to be added to the relay's acceptable range of operating times.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

Characteristic	Operating time at twice current setting and time multiplier/time dial setting of 1.0	
	Nominal (seconds)	Range (seconds)
DT	[3505: **I>1 Time Delay**] setting	Setting ±5%
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	25.34 - 28
UK LT Inverse	120.00	114.00 - 126.00
IEEE M Inverse	3.8	3.61 - 3.99
IEEE V Inverse	7.03	6.68 - 7.38
IEEE E Inverse	9.52	9.04 - 10
US Inverse	2.16	2.05 - 2.27
US ST Inverse	12.12	11.51 - 12.73

Table 20: Characteristic operating times for I>1

On completion of the tests any protection elements that were disabled for testing purposes must have their original settings restored in the **CONFIGURATION** column.

6.3.4 Generator-transformer differential protection (P343/4/5/6)

To avoid spurious operation of any other protection elements, all protection elements except the transformer differential protection should be disabled for the duration of the differential element tests. This is done in the relay's **CONFIGURATION** column. The generator-transfomer differential protection is selected by the **SYSTEM CONFIG - Winding Config - Xformer** setting and is enabled by the setting **DIFFERENTIAL - Xformer Diff Func -** Enabled. Make a note of which elements need to be re-enabled after testing.

The P343/4/5/6 transformer differential protection has three elements, one for each phase. The biased differential protection uses the maximum bias current in the three phases to bias the elements. The detailed bias characteristic is described in the Operation chapter *P34x/EN OP*.

6.3.4.1 Low set element current sensitivity (Xform I_{s1})

If three LEDs have been assigned to give phase segregated trip information, Xform Dif Trp A, Xform Dif Trp B and Xform IDiff Trp C (DDB 741, 742, 743), these may be used to indicate correct per-phase operation. If not, monitor options need to be used (see the next paragraph).

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Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F07: **Monitor Bit 1**] to 741, [0F08: **Monitor Bit 2**] to 742 and [0F09: **Monitor Bit 3**] to 743. Cell [0F05: **Test Port Status**] will now appropriately set or reset the bits that now represent Phase A Trip (DDB 741), Phase B Trip (DDB 742) and Phase C Trip (DDB 743) with the rightmost bit representing Phase A Trip. From now on, monitor the indication of [0F05: **Test Port Status**].

Connect the equipment so that current can be injected into the A phase □A-2 HV input, (E3 - E2 (1A, 60TE case), E1 - E2 (5A, 60TE case), F3 - F2 (1A, 80TE case), F1 - F2 (5A, 80TE case)). Slowly increase the current from 0 Amps and note the pick-up value at which the A phase biased differential element operates. Reduce the current slowly and note the drop-off value at which it resets. Check that the pick-up and drop-off are within the range shown in Table 21:

In Table 21 below, $$I = \frac{I_{s1}}{amplitude \quad matching \quad factor}$$

Is1 is the low set setting which can be found in the cell **Xform Is1** under the **GROUP 1 DIFFERENTIAL PROTECTION** menu heading. The amplitude matching factor is used to compensate for a mismatch in currents due to the line side current transformer ratios. There is one amplitude matching factor for the HV side, which is in the cell **SYSTEM CONFIG - Match Factor HV** and one for the LV side found in the cell **SYSTEM CONFIG - Match Factor LV.** Use the appropriate amplitude matching factor to calculate the current to inject: this depends on whether it is being injected into the HV or LV current transformer inputs.

	Current level
Pick-up	0.90 x I to 1.1 x I
Drop-off	0.90 x pick-up to 1 x pick-up

Table 21: Low set element pick-up and drop-off

Repeat the above test for each of the remaining phases on the HV side, and for all three phases on the LV side. The connection terminals are shown in Table 10.

As the CT inputs to each phase have been verified by both the measurement checks and the low set differential trip checks, it is only necessary to check the operating time and the high set current sensitivity for each phase element on one side of the transformer.

6.3.4.2 Low set element operating time

Connect the relay so that current can be injected into the A phase IA-2 HV input, (E3 - E2 (1A, 60TE case), E1 - E2 (5A, 60TE case), F3 - F2 (1A, 80TE case), F1 - F2 (5A, 80TE case)). Connect a timer to start when the fault injection is applied, and to stop when the trip occurs.

Determine which output relay has been selected to operate when a Xform Dif Trp or Xform Bias Trp A/B/C occurs by viewing the relay's programmable scheme logic. The programmable scheme logic can only be changed using the appropriate software. If this software is not available then the default output relay allocations will still be applicable. In the default PSL, relay 3 is the designated protection trip contact and DDB 740 Xform Dif Trp is assigned to this contact. If the generator-transformer differential trip is not mapped directly to an output relay in the programmable scheme logic, output relay 3 (H5-H6 in the 60TE case and L5-L6 in the 80TE case) should be used for the test as relay 3 initiates the trip led.

Ensure that the timer is reset.

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Inject 4 x I into the HV side A phase. Check that the operating time for the relay is less than 33 ms. Repeat this test for both the remaining phases on the HV side. The current input terminals are shown in Table 10.

Three Pole Tripping	DDB 740:	Xform Dif Trp
Single Pole Tripping (Transformer Differential and Transformer Biased low set Differential protection)	DDB 741:	Xform Dif Trp A
	DDB 742:	Xform Dif Trp B
	DDB 743:	Xform Dif Trp C
	DDB 744:	Xform Bias Trp A
	DDB 745:	Xform Bias Trp B
	DDB 746:	Xform Bias Trp C

Table 22: High set element sensitivity

6.3.4.3 High set element current sensitivity (Xform Is-HS1)



The relay may be damaged by applying excessive current for long durations during testing, or in recurrent bursts without allowing time for the relay to cool down.

This test checks the instantaneous current sensitivity of the differential high set element. This test can only be performed if the test set can inject sufficient current into the relay to cause the element to trip at the calculated application setting.

The relay should be connected so that current can be injected into the A phase IA-2 HV input, (E3 - E2 (1A, 60TE case), E1 - E2 (5A, 60TE case), F3 - F2 (1A, 80TE case), F1 - F2 (5A, 80TE case)). Connect the output relay configured as Xform HS1 Trp A (DDB 747) to trip the test set and to stop a timer. Configure the test set so that when the current is applied to the relay, the timer starts.

It is important to trip the test set to avoid sustained application of excessive currents.

It is recommended that the low set differential is still enabled during this test. The timer should be started when the current is applied to the relay. As the setting is above the continuous current rating of the relay, DO NOT INCREASE THE CURRENT SLOWLY, since this may damage the relay before it can operate. Instead, set the current level then suddenly apply it. Two tests have to be performed for this particular protection function. These are shown in Table 23.

Is HS1 (Trip)	Is HS1 (No Trip)
1.1 x I	0.90 x I

Table 23: High set element sensitivity

The first test to be performed is at the higher current level, to check that the instantaneous element operates.

In Table 21, $$I = \frac{Is \quad HS1}{amplitude \quad matching \quad factor}$$

Is-HS1 is the high set setting which is in the cell **Xform Is HS1** under the **GROUP 1 DIFF PROTECTION** menu heading. The amplitude matching factor is used to compensate for a mismatch in currents due to the line side current transformer ratios. This is found in the cell **Match Factor HV** under the **GROUP 1 SYSTEM CONFIG** menu heading.

Inject 1.1 x I and ensure that the selected output relay operates.

For the second test it is important that the current is not applied for longer than one second.

Inject 0.9 x I for one second and ensure that the selected output relay does not operate. Repeat the above two tests for the two remaining elements of the HV side of the transformer. The current input terminals are shown in Table 10.

Three Pole Tripping	DDB 740:	Xform Dif Trp
Single Pole Tripping	DDB 747:	Xform HS1 Trp A
(Transformer Differential high set 1 protection)	DDB 748:	Xform HS1 Trp B
	DDB 749:	Xform HS1 Trp C

Table 24: Transformer differential protection DDBs

6.3.4.4 High set element operating time

This test can only be performed if the test set can inject sufficient current into the relay to cause the element to trip at the calculated application setting.

Connect the relay so that current can be injected into the A phase IA-2 HV input, (E3 - E2 (1A, 60TE case), E1 - E2 (5A, 60TE case), F3 - F2 (1A, 80TE case), F1 - F2 (5A, 80TE case)). Connect a timer to start when the fault injection is applied, and to stop when the trip occurs. Configure the test set so that when the current is applied to the relay, the timer starts.

Determine which output relay has been selected to operate when a Xform Dif Trp or Xform HS1 Trp A/B/C occurs by viewing the relay's programmable scheme logic. The programmable scheme logic can only be changed using the appropriate software. If this software is not available then the default output relay allocations will still be applicable. In the default PSL, relay 3 is the designated protection trip contact and DDB 740 Xform Dif Trp is assigned to this contact. If the generator-transformer differential trip is not mapped directly

to an output relay in the programmable scheme logic, output relay 3 (H5-H6 in the 60TE case and L5-L6 in the 80TE case) should be used for the test as relay 3 initiates the trip led.

Ensure that the timer is reset.

Inject 1.2 x I into the HV side A phase. Check that the operating time for the relay is less than 25 ms.

Repeat this test for both the remaining phases on the HV side. The current input terminals are shown in Table 10.

6.3.4.5 Differential through stability by primary injection

To check for through stability, it is preferable, especially for a new transformer installation to simulate a through-fed external fault, by a real primary fault simulation. This is achieved by placing a three-phase bolted short circuit on the downstream side of the LV CTs, and energizing the HV winding from a three-phase medium voltage supply. Typically, the HV winding is energized only from a voltage rated in the range 400 to 440 V, to limit the through fault current. In such a through fault situation, the relay should not trip.

Note: The procedure for primary testing is not covered here, as it must respect utility safety rules, permits to work, and sanctions for testing.

6.3.4.6 CT secondary wiring differential through stability test by secondary injection

Secondary injection can be used to verify settings. For a two-winding transformer, a fault current flowing out of the LV side is simulated, with a balancing set of currents on one or two phases flowing into the HV side. If all settings and CT orientations are correct, no trip should occur, and minimal differential current is measured by the relay.



During these tests, disable all the current operated protection functions except the transformer differential protection. Make a note of all the functions that must be enabled after the testing is completed.

6.3.4.6.1 Yy transformers and autotransformer

This test simulates current flowing through the transformer to an external fault.

Consider a two-winding Yy0 transformer application, and that IA-2 (E3 - E2 (1A, 60TE case), E1 - E2 (5A, 60TE case), F3 - F2 (1A, 80TE case), F1 - F2 (5A, 80TE case)) is assigned to the HV winding and IA (C3 - C2 (1A, 60TE case), C1 - C2 (5A, 60TE case), D3 - D2 (1A, 80TE case), D1 - D2 (5A, 80TE case)) is assigned to the LV winding. A fault current is injected, flowing out of phase A at the LV terminals. The same zero sequence filtering setting is applied for the HV and LV windings; therefore, if the current simulated is 1 pu out of IA at the LV connections, the input current to balance IA at the HV connections is also 1 pu.

Connect the test equipment as shown in Figure 4 for a Yy0 transformer connection:

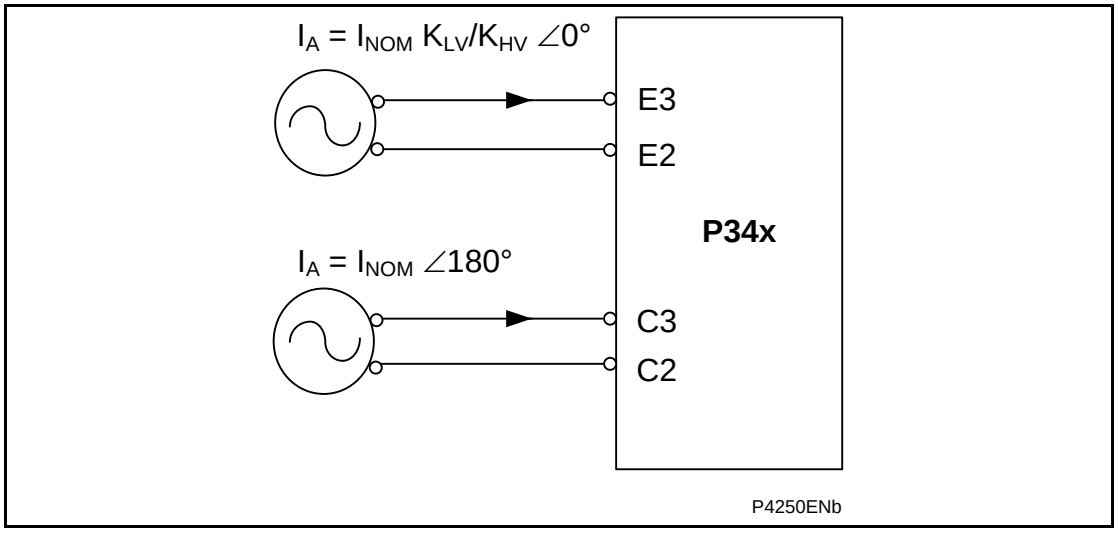


Figure 4: Test equipment connection for a Yy0 transformer(1A and 60TE)

A single phase current equal to the CT secondary rating (1 A or 5 A) is simulated to flow OUT on phase A, LV CT connections. On an automatic test set, use INOM ∠180º.

To balance, a current is applied to one phase input of the HV CT connections. The magnitude should be a current equal to (K_{LV} / K_{HV}) x I_{NOM}, and at a phase angle as shown below:

	LV CT injected phase	LV current	HV CT injected phase	HV current
Yy0, Autotrans former	A	INOM ∠180º	A	I_{NOM} . K_{LV} / K_{HV} ∠0º
Yy2	A	INOM ∠180º	C	I_{NOM} . K_{LV} / K_{HV} ∠180º
Yy4	A	INOM ∠180º	B	I_{NOM} . K_{LV} / K_{H}V ∠0º
Yy6	A	INOM ∠180º	A	I_{NOM} . K_{LV} / K_{HV} ∠180º
Yy8	A	INOM ∠180º	C	I_{NOM} . K_{LV} / K_{HV} ∠0º
Yy10	A	INOM ∠180º	B	I_{NOM} . K_{LV} / K_{HV} ∠180º

Table 25: Injected current for Yy ends

The amplitude matching factors K_{HV} and K_{LV} can be found in **Match Factor HV** and **Match Factor LV** respectively under the **GROUP 1 SYSTEM CONFIG** menu heading.

Apply the fault currents for approximately one second. If the HV CT connections and LV CT connections are in the correct orientation no trip should occur. It is important to read the displayed differential currents **IA Differential**, **IB Differential** and **IC Differential** under the **MEASUREMENT 3** menu heading to check that these measurements are low. These measurements must show less than 0.1 pu (10%), to prove that a balance is achieved.

The reason that the differential currents must be read is that in certain applications the Idiff> trip threshold may be set higher than I_{nom}, so that even an incorrect CT connection would not cause a trip.

It is not necessary to repeat the injection for other phases, because their orientation has already been checked in section 5.2.15, Current inputs.

Figure 5 shows the transformer connections for the configurations shown in Table 2.

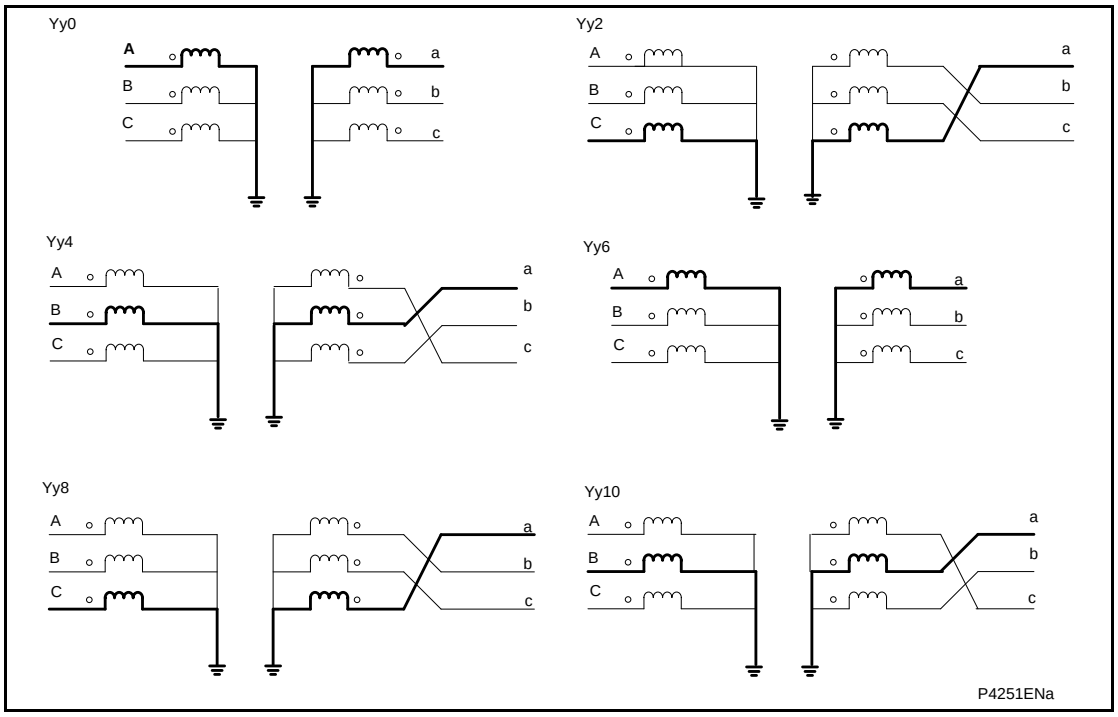


Figure 5: Yy transformer connections

6.3.4.6.2 Dy and Yd applications

This test simulates current flowing through the transformer to an external fault.

A fault current flowing out of the A phase on whichever winding is the star (wye) end is injected. For a Dy configuration it is the LV side, for a Yd configuration it is the HV side. The star winding phase A shares the same power transformer limb as two phases on the opposite side, so that a two-phase current loop needs to be injected to achieve a balance.

For ease of injection, a single phase current equal to the CT secondary rating (1 A or 5 A) is simulated to flow OUT on phase A of the wye end. On an automatic test set, use INOM ∠180º. To balance, a current is applied to two phase CT inputs (delta side). Table 26 shows the currents to be injected. The magnitude should be a current equal to [K_{wye} / (√3.K_{delta})] x I_{NOM}, and at the phase angles as shown below:

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	Star end injected phase	Current (Star)	Delta side injected loop	Current
Dy1 or Yd11	A	INOM ∠180º	A-C	IA = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠0º IC = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠180º
Dy3 or Yd9	A	INOM ∠180º	C-B	IC = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠0º IB = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠180º
Dy5 or Yd7	A	INOM ∠180º	A-B	IA = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠0º IB = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠180º
Dy7 or Yd5	A	INOM ∠180º	A-C	IA = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠0o IC = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠180º
Dy9 or Yd3	A	INOM ∠180º	B-C	IB = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠0º IC = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠180º
Dy11 or Yd1	A	INOM ∠180º	A-B	IA = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠0º IB = I_{NOM} . K_{WYE} / √3K_{DELTA} ∠180º

Table 26: Injected current for delta-star ends

For a Yd1 configuration, connect the test equipment as shown in Figure 6.

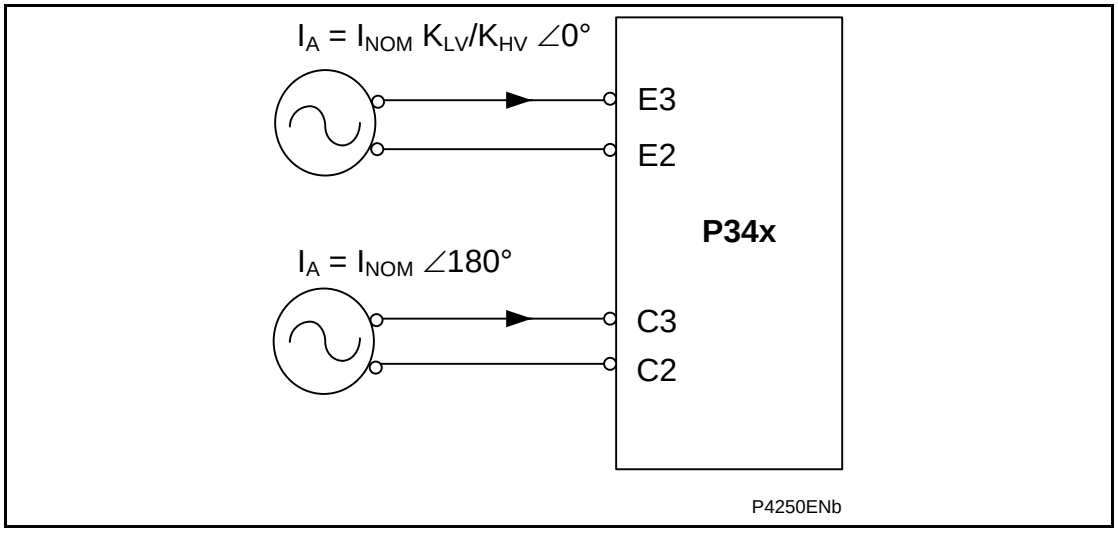


Figure 6: Test equipment connection for a Yd1 transformer(1A and 60TE) - is this the right diagram as same as fig 5

The amplitude matching factors K_{wye} and K_{delta} can be found in **Match Factor HV** and **Match Factor LV** under the **GROUP 1 SYSTEM CONFIG** menu heading

The delta side loop current may be applied as two separate current outputs from a test set, or one current looped out through the first phase specified, and returning back through the latter phase input.

Apply the fault currents for approximately one second. If the HV CT connections and LV CT connections are in the correct orientation no trip should occur. It is important to read the displayed differential currents **IA Differential**, **IB Differential and IC Differential** under the **MEASUREMENT 3** menu heading to check that these measurements are low. These measurements must show less than 0.1 p.u. (10%), to prove that a balance is achieved.

It is not necessary to repeat the injection for other phases, because their orientation has already been checked in section 5.2.15, Current inputs.

Figure 7 shows a Yd9 transformer with the current distribution for an AN external fault on the Y side of the transformer. During the test shown in Figure 6, the following current distribution occurs in the P34x.

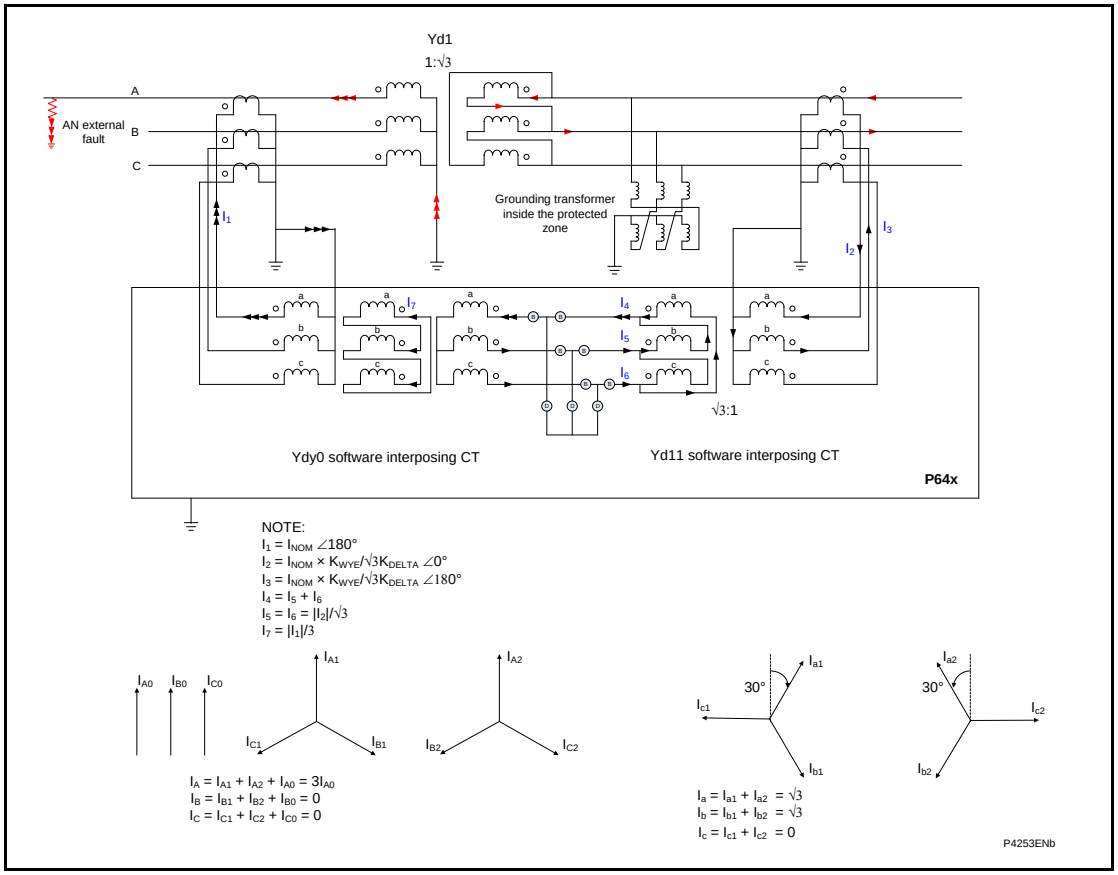


Figure 7: Yd9 configuration AN external fault current distribution

Figure 8 shows the transformer connections for the configurations shown in Table 26.

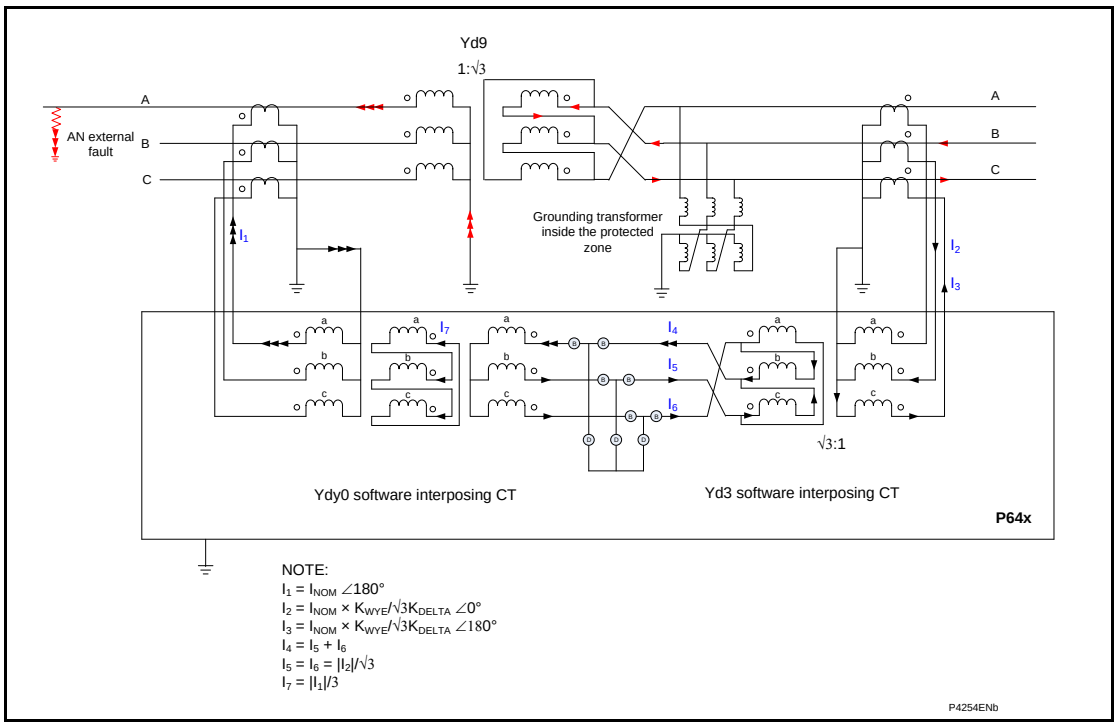


Figure 8: Yd transformer connections

CM

6.3.4.6.3 Dd applications

This test simulates current flowing through the transformer to an external fault.

In many such applications, there may be in-zone earthing transformers, so it is easier to simulate an external phase-phase fault, to avoid simulating a zero sequence current. If the HV CT connection is assigned to the HV end and LV CT connection to the LV end, and the current simulated is 1 pu out of LV CT connection, the input current to balance at HV CT connection is easy to determine. In the simplest application of a Dd0 transformer, an A-B fault is simulated flowing out of the LV side, fed by an A-B loop input on the HV side.

For ease of injection, a loop current equal to the CT secondary rating (1 A or 5 A) is simulated to flow OUT on phase A, LV CT connection, and looping back through phase B, LV CT connection. On an automatic test set, use I_{NOM} ∠180º. Because four-phase CT inputs to the relay are energized at once, it is necessary that the test set output current for this LV side is set as a single phase but looping through two phase CT inputs.

To balance, a loop current is applied at HV CT (the HV winding). The magnitude should be a current equal to (K_{LV}/K_{HV}) x I_{NOM}, and at a phase angle as shown below. The test set is configured to generate only one single phase output for this winding, looped through two phase CT inputs. Therefore in total, the output requirements can be satisfied by a test set typically having only up to three current outputs.

	LV CT injected phase	LV current terminal 5 CT	HV CT injected phase	HV current terminal 1 CT
Dd0	A-B	I_{NOM} ∠180º	A-B	I_{NOM} . K_{LV} / K_{HV} ∠0º
Dd2	A-B	I_{NOM} ∠180º	C-B	I_{NOM} . K_{LV} / K_{HV} ∠0º
Dd4	A-B	I_{NOM} ∠180º	C-A	I_{NOM} . K_{LV} / K_{HV} ∠0º
Dd6	A-B	I_{NOM} ∠180º	B-A	I_{NOM} . K_{LV} / K_{HV} ∠0º
Dd8	A-B	I_{NOM} ∠180º	B-C	I_{NOM} . K_{LV} / K_{HV} ∠0º
Dd10	A-B	I_{NOM} ∠180º	A-C	I_{NOM} . K_{LV} / K_{HV} ∠0º

Table 27: Current injected for Dd ends

The amplitude matching factors K_{HV} and K_{LV} can be found in **Match Factor HV** and **Match Factor LV** respectively under the **GROUP 1 SYSTEM CONFIG** menu heading.

For the Dd0 configuration, connect the test equipment as shown in Figure 9.

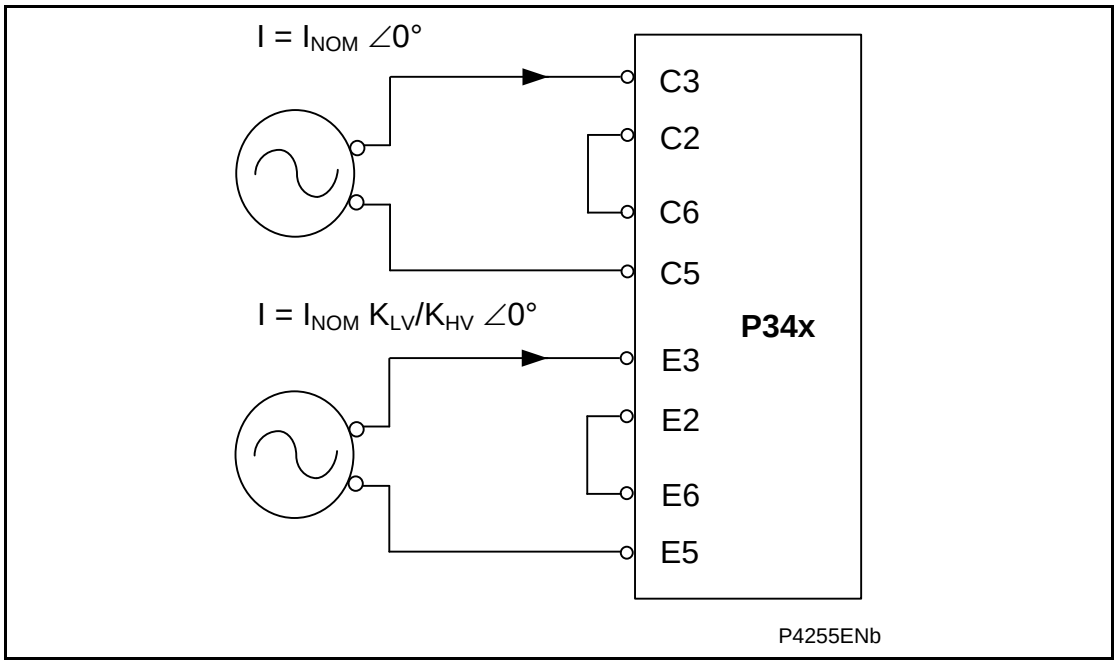


Figure 9: Test equipment connection for a Dd0 transformer(1A and 60TE)

Apply the fault currents for approximately one second. If the HV CT connection and the LV CT connections are in the correct orientation no trip should occur. It is important to read the displayed differential currents **IA Differential**, **IB Differential** and **IC Differential** under the **MEASUREMENT 3** menu heading to check that these measurements are low. These measurements must show less than 0.1 p.u. (10%), to prove that a balance is achieved.

It is not necessary to repeat the injection for other phases, because their orientation has already been checked in section 5.2.15, Current inputs.

Figure 10 shows the transformer connections for the configurations shown in Table 5.

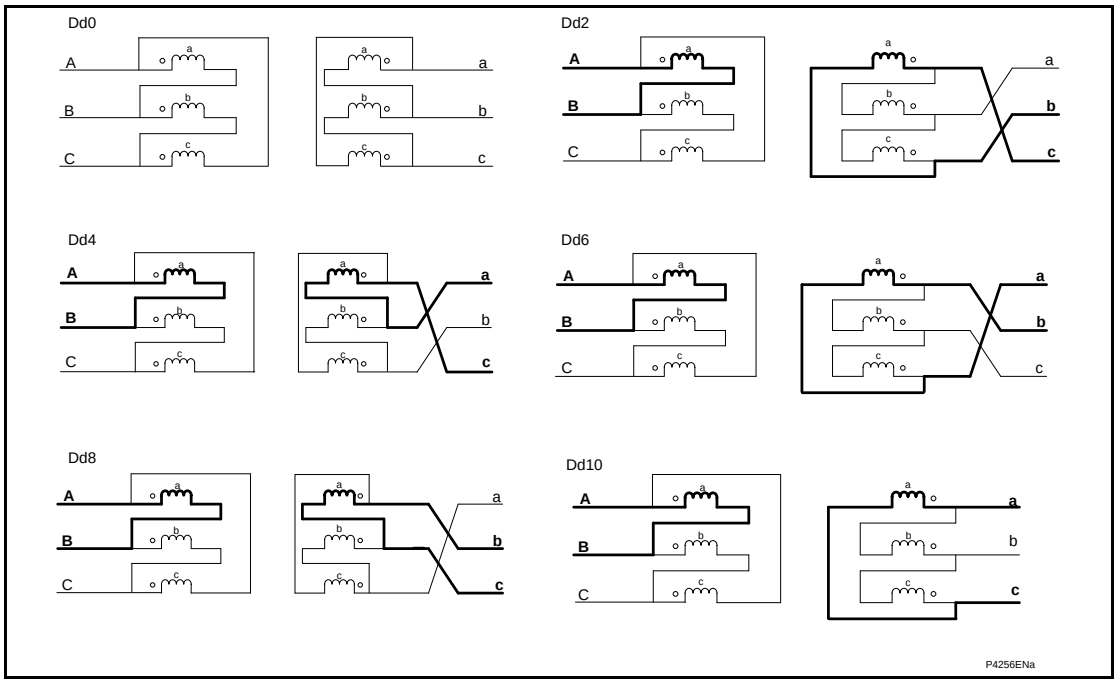


Figure 10: Dd transformer connections

6.3.4.7 Low set element bias characteristic

This test checks the low set element bias characteristic. The relay has a three slope bias characteristic, therefore this test is performed at three points on the bias curve, one at 0% slope, at 30% slope, and at 80% slope, corresponding with bias currents of 0.4 p.u., 0.8 p.u., and 1.5 p.u. respectively.

If three LEDs have been assigned to give phase segregated trip information, Xform Dif Trp A, Xform Dif Trp B and Xform IDiff Trp C (DDB 741, 742, 743), these may be used to indicate correct per-phase operation. If not, monitor options need to be used (see the next paragraph).

Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F07: **Monitor Bit 1**] to 741, [0F08: **Monitor Bit 2**] to 742 and [0F09: **Monitor Bit 3**] to 743. Cell [0F05: **Test Port Status**] will now appropriately set or reset the bits that now represent Phase A Trip (DDB 741), Phase B Trip (DDB 742) and Phase C Trip (DDB 743) with the rightmost bit representing Phase A Trip. From now on, monitor the indication of [0F05: **Test Port Status**].

It is important in this case that the injected currents are 180º out of phase. Connect the relay to the test equipment as shown in Figure 11.

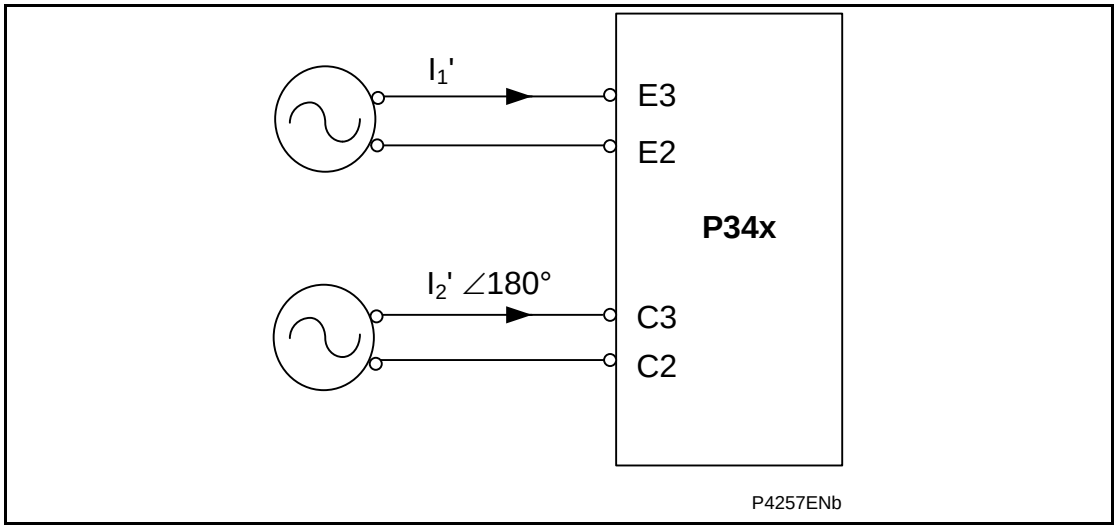


Figure 11: Low set element bias characteristic test equipment connection (1A and 60TE)

In total, six tests should be performed, one to cause the relay to trip and one not to cause the relay to trip, for the three sections of the bias curve. From Table 28, select the appropriate current values for each test, depending on the setting and rating of the relay. Using the equations below, calculate the current values to apply to the relay, (I1' and I2'). In all cases the current should be applied for no longer than one second, and should be within ±5% of the calculated values.

K_{CT1} is the HV CT amplitude matching factor and K_{CT2} is the LV CT amplitude matching factor which are found in the cell **Match Factor HV** and **Match Factor LV** under the **GROUP 1 SYSTEM CONFIG** menu heading.

$$I_1' = \frac{I_1}{K_{CT1}} \qquad I_2' = \frac{I_2}{K_{CT2}}$$

In (amps)	Is1 (pu)	0%				K1 = 30%				K2 = 80%			
		Trip		No trip		Trip		No trip		Trip		No trip	
		I1	I2	I1	I2	I1	I2	I1	I2	I1	I2	I1	I2
1	0.2	0.51	0.29	0.49	0.31	0.94	0.67	0.91	0.69	1.89	1.12	1.82	1.19
5	0.2	2.55	1.45	2.45	1.55	4.7	3.35	4.55	3.45	9.45	5.6	9.1	5.95

Table 28: Low set element bias characteristic test

6.3.4.8 Second-harmonic blocking

This test checks that the second harmonic blocking is functioning, and it requires a current source capable of generating second-harmonic current. Once enabled, it blocks the low set differential element if the percentage of second harmonic over fundamental component per phase basis exceeds the setting Ih(2)%>.

To run the test, proceed as follows:

Connect two current test sources to one phase of any current bias input. Figure 12 shows the current sources connected to A phase of current bias input 1:

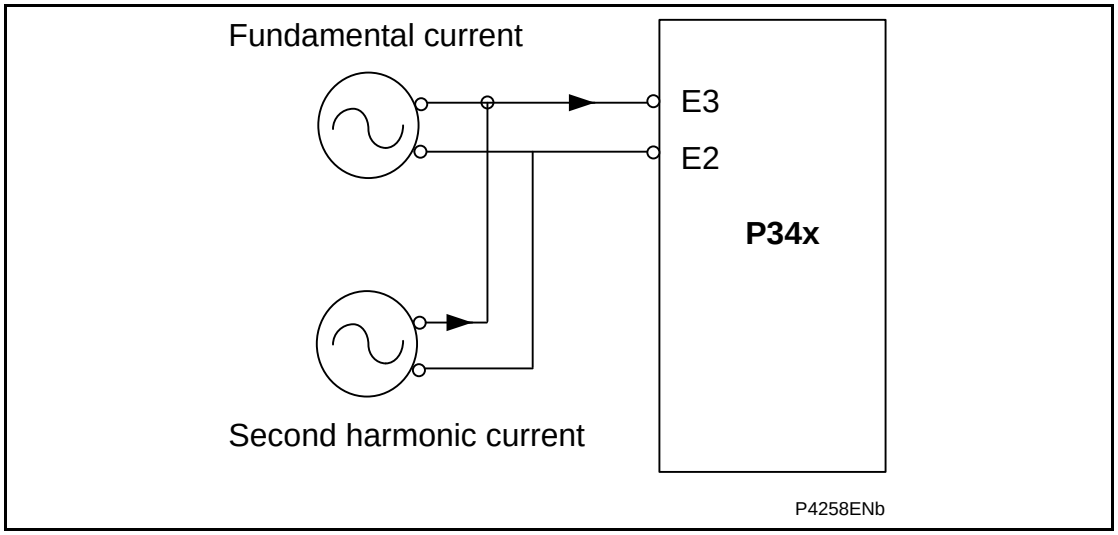


Figure 12: Second harmonic test(1A and 60TE)

Inject 4 x I of fundamental current, where:

$$I = \frac{I_{s1}}{K_{CT1}}$$

Is1 is the low set setting, KCT1 is the HV CT amplitude matching factor which is used to compensate for a mismatch in currents due to the line side current transformer ratios. This is found in the cell **Match Factor HV** under the **GROUP 1 SYSTEM CONFIG** menu heading.

Ensure that Xform Bias Trp A [DDB 744] asserts.

Apply and ramp second-harmonic current to dropout the low set differential element.

Turn on the second current source for second-harmonic current (120 Hz if Frequency = 60 and 100 Hz if Frequency = 50). Starting at zero current, slowly increase the magnitude of this second current source until Xform Bias Trp A [DDB 744] resets.

Note: The value of the applied current from the second test source. The current from the second-harmonic source is shown by:

$$\text{Second harmonic current} = \frac{Ih(2)\%}{100} \times \text{fundamental current} \pm 10\%$$

6.3.4.9 Fifth-harmonic blocking

This test checks that the fifth-harmonic blocking is functioning, and it requires a current source capable of generating fifth-harmonic current. Once enabled, it blocks the low set differential element if the percentage of fifth harmonic over fundamental component per phase basis exceeds the setting Ih(5)%>.

Connect two current test sources to one phase of any current bias input. Figure 13 shows the current sources connected to current bias input 1.

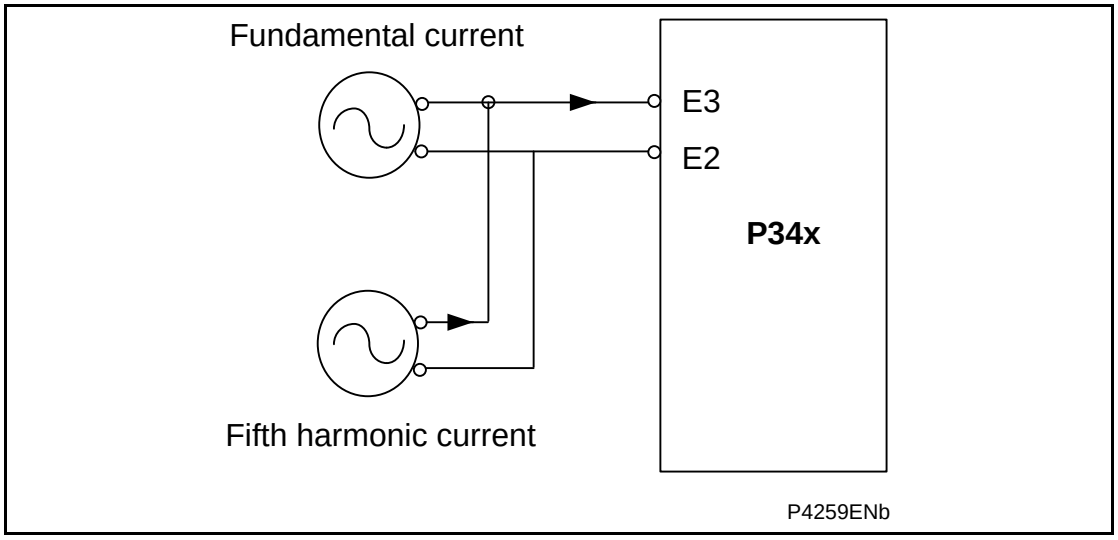


Figure 13: Fifth-harmonic (1A and 60TE)

Inject 4 x I of fundamental current, where:

$$I = \frac{I_{s1}}{K_{CT1}}$$

Is1 is the low set setting. K_{CT1} is the HV CT amplitude matching factor which is used to compensate for a mismatch in currents due to the line side current transformer ratios. This is found in the cell **Match Factor HV** under the **GROUP 1 SYSTEM CONFIG** menu heading. Ensure that Xform Bias Trp A [DDB 744] asserts.

Apply and ramp fifth-harmonic current to dropout the low-set differential element. Turn on the second current source for fifth-harmonic current (300 Hz if Frequency = 60, 250 Hz if Frequency = 50). Starting at zero current, slowly increase the magnitude of this second current source until Xform Bias Trp A [DDB 744] resets. Note the value of the applied current from the second test source. The current from the fifth-harmonic source is given by:

$$\text{Fifth harmonic current} = \frac{Ih(5)\%}{100} \times \text{fundamental current}$$

6.3.5 Generator 100% stator earth fault protection via low frequency injection (P345)

The 100% stator earth fault protection function via low frequency injection (64S) should be tested in the P345. The 100% stator earth fault protection via low frequency injection includes an overcurrent trip (64S I>1) an under resistance trip (64S R<2) and an under resistance alarm (64S R<1) element. It is only necessary to test the elements being used.

To avoid spurious operation of any other protection elements all protection elements except the 100% stator earth fault protection should be disabled for the duration of the 100% stator earth fault tests. This is done in the relay's **CONFIGURATION** column. Make a note of which elements need to be re-enabled after testing.

6.3.5.1 Connect the test circuit

Determine which output relay has been selected to operate when a 64S I>1 Trip (DDB 778) and 64S R<2 Trip (DDB 779) and 64S R<1 Alarm Trip (DDB 382) occurs by viewing the relay's programmable scheme logic.

The programmable scheme logic can only be changed using the appropriate software. If this software is not available then the default output relay allocations will still be applicable.

If the 64S protection signals are not independently mapped directly to an output relay in the programmable scheme logic, output relay 3 and 4 (L5 - L6 and L7 – L8 in the P345) could be used in the default PSL to check the operation of the protection functions. In the default PSL relay 3 is the designated protection trip contact and 64S I>1 Trip (DDB 778) and 64S R<2

Trip (DDB 779) are assigned to this contact. In the default PSL relay 4 is the designated general alarm contact and 64S R<1 Alarm Trip (DDB 382) is assigned to this contact.

Note: In the default PSL relay 3 is set to operate the Any Trip signal (DDB 674) which initiates the trip LED.

The associated terminal numbers can be found from the external connection diagrams in chapter *P34x/EN IN*.

Connect the output relay so that its operation will trip the test set and stop the timer.



Connect a 20 Hz current output of the test set to the 'I 100% STEF' current transformer input of the relay (terminals F12 – F11 (1A), F10 – F11 (5A)). Note, for the 5A inputs the 64S I Magnitude measurement in the Measurements 3 menu will show 5 times lower current than being injected.

Connect a 20 Hz voltage output of the test set to the 'V 100% STEF' voltage transformer input of the relay (terminals F21 – F22).

To simulate a generator standstill condition there should be no signal injected into the 3 phase voltage and current inputs.

Ensure that the timer will start when the current and voltage is applied to the relay.

6.3.5.2 Check the pick-up settings

Ensure that the following settings [**GROUP 1 100% STATOR EF**, **64S R Factor** = 1, **64S Series R** = 0, **64S Parallel G** = 0, **64S Angle Comp** = 0, **64S R<1 Alarm** = **Disabled**, **64S R<2 Trip** = **Disabled**, **64S Supervision** = **Disabled**, **VN 3rd Harmonic** = **Disabled**.]

If three LEDs have been assigned to give the 64S alarm and trip information, 64S I>1 Trip (DDB 778), 64S R<2 Trip (DDB 779) and 64S R<1 Alarm Trip (DDB 382), these may be used to indicate correct operation. If not, monitor options will need to be used - see the next paragraph.

Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F05: **Monitor Bit 1**] to 756, [0F06: **Monitor Bit 2**] to 757 and [0F07: **Monitor Bit 3**] to 382. Cell [0F04: Test Port Status] will now appropriately set or reset the bits that now represent 64S I>1 Trip (DDB 778), 64S R<2 Trip (DDB 779) and 64S R<1 Alarm Trip (DDB 382), with the rightmost bit representing 64S I>1 Trip. From now on you should monitor the indication of [0F04: **Test Port Status**].

Slowly increase the 20 Hz current to the I 100% STEF input F12 – F11 (1A), F10 – F11 (5A) until the 64S I> 1 element trips.

(Bit 3 of [0F04: **Test Port Status**] is set to 1). Record the 20Hz current magnitude and check that it corresponds to the 64S I>1 Trip Set ±5%.

Note: The 5A inputs the **64S I Magnitude** measurement in the **Measurements 3** menu will show 5 times lower current than being injected.

Switch OFF the test and reset the alarms.

Set **64S R<2 Trip** = **Enabled** and **64S R<1 Alarm** = **Disabled** and **64S Overcurrent** = **Disabled**.

Set the 20 Hz voltage to the V 100% STEF input, F21 – F22, to 20 V angle 0.

Slowly increase the 20 Hz current, angle 0, to the I 100% STEF input, F12 – F11 (1A), F10 – F11 (5A) until the 64S R<2 element trips.

(Bit 2 of [0F04: **Test Port Status**] is set to 1). Record the 20 Hz current and voltage magnitude and check that the resistance (R = V/I) corresponds to the 64S R<2 Trip Set ±5%.

Switch OFF the test and reset the alarms.

Set **64S R<1 Alarm** = **Enabled** and **64S R<2 Trip** = **Disabled** and **64S Overcurrent** = **Disabled**.

Set the 20 Hz voltage to the V 100% STEF input, F21 – F22, to 20 V angle 0.

Slowly increase the 20 Hz current, angle 0, to the I 100% STEF input, F12 – F11 (1A), F10 – F11 (5A) until the 64S R<1 element trips.

(Bit 3 of [0F04: **Test Port Status**] is set to 1). Record the 20 Hz current and voltage magnitude and check that the resistance (R = V/I) corresponds to the 64S R<1 Alm Set ±5%.

Switch OFF the test and reset the alarms.

6.3.5.3 Perform the timing tests

Ensure that the timer is reset.

Set 64S R<2 Trip = **Disabled** and **64S R<1 Alarm** = **Disabled** and **64S Overcurrent** = **Enabled**.

Apply a 20 Hz current of twice the setting in cell [3C44: GROUP 1 **100% STATOR EF**, **64S I>1 Trip Set]** to the relay and note the time displayed when the timer stops.

Check the red trip led and yellow alarm led turns on when the relay operates. Check 'Alarms/Faults Present - Started Phase N, Tripped Phase N, 100% 64S Start I>1, 100% 64S Trip I>1' is on the display. Reset all alarms. In the default PSL relay 3 is set to operate the Any Trip signal (DDB 674) which initiates the trip LED.

Check that the operating time recorded by the timer is within the range, 64S I>1 Trip Dly setting ±2% or 1.2 s whichever is greater with the P345 bandpass filter enabled and ±2% or 0.22 s whichever is greater with the P345 bandpass filter disabled. The P345 bandpass filter is automatically enabled when the system frequency is <45 Hz or it can be permanently enabled using DDB 555, 64S Filter On.

Allowance must also be made for the accuracy of the test equipment being used.

Ensure that the timer is reset.

Set **64S R<2 Trip** = **Enabled** and **64S R<1 Alarm** = **Disabled** and **64S Overcurrent** = **Disabled**.

Apply a 20 Hz voltage of 20 V, angle 0 and a 20 Hz current, angle 0 to give half the setting in cell [3C2C: GROUP 1 **100% STATOR EF**, **64S R<2 Trip Set**] to the relay and note the time displayed when the timer stops.

Check the red trip led and yellow alarm led turns on when the relay operates. Check 'Alarms/Faults Present - Started Phase N, Tripped Phase N, 100% 64S Start R<2, 100% 64S Trip R<2' is on the display. Reset all alarms.

Note: In the default PSL relay 3 is set to operate the Any Trip signal (DDB 674) which initiates the trip LED.

Check that the operating time recorded by the timer is within the range, **64S R<2 Trip Dly** setting ±2% or 1.2 s whichever is greater with the P345 bandpass filter enabled and ±2% or 0.22 s whichever is greater with the P345 bandpass filter disabled. The P345 bandpass filter is automatically enabled when the system frequency is <45 Hz or it can be permanently enabled using DDB 555, 64S Filter On.

Allowance must also be made for the accuracy of the test equipment being used.

Ensure that the timer is reset.

Set **64S R<2 Trip** = **Disabled** and **64S R<1 Alarm** = **Enabled** and **64S Overcurrent** = **Disabled**.

Apply a 20 Hz voltage of 20 V, angle 0 and a 20 Hz current, angle 0 to give half the setting in cell [3C20: GROUP 1 **100% STATOR EF**, **64S R<1 Alm Set**] to the relay and note the time displayed when the timer stops.

Check the yellow alarm led turns on when the relay operates. Check 'Alarms/Faults Present -100% 64S Alarm R<1' is on the display. Reset all alarms.

Check that the operating time recorded by the timer is within the range, **64S R<1 Alm Dly** setting ±2% or 1.2 s whichever is greater with the P345 bandpass filter enabled and ±2% or 0.22 s whichever is greater with the P345 bandpass filter disabled. The P345 bandpass filter is automatically enabled when the system frequency is <45 Hz or it can be permanently enabled using DDB 555, 64S Filter On.

Allowance must also be made for the accuracy of the test equipment being used.

Ensure that the timer is reset.

6.3.5.4 Perform the 100% stator earth fault supervision test

Set the **64S Supervision** = **Enabled**, Set **64S R<2 Trip** = **Enabled and 64S R<1 Alarm** = **Enabled** and **64S Overcurrent** = **Enabled**.

In the default PSL the 64S Fail (DDB 1298) supervision signal is connected to the 64S Fail Alarm (DDB 383) signal. The 64S Fail signal is an output from the 64S supervision element and the 64S Fail Alarm signal triggers the alarm led and alarm message. For applications where the 20 Hz generator is powered by the VT it may be desirable not to alarm every time the generator is off line so the supervision element and alarm have separate DDBs. The 64S Fail signal is also connected to the 64S I>1 Inhibit, 64S R<1 Inhibit and 64S R<2 Inhibit in the default PSL.

If an LED has been assigned to give the 64S Fail Alarm or 64S Fail information, 64S Fail Alarm (DDB 383), this may be used to indicate correct operation. If not, monitor options will need to be used - see the next paragraph.

Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F08: **Monitor Bit 4**] to 383 and cell [0F09: **Monitor Bit 5**] to 1076. Cell [0F04: **Test Port Status**] will now appropriately set or reset the bit that now represent 64S Fail Alarm (DDB 383) and 64S Fail (DDB 1298). From now on you should monitor the indication of [0F04: **Test Port Status**].

Apply a 20 Hz current and 20 Hz voltage above the settings in cell [3C50/54: GROUP 1 **100% STATOR EF**, **64S V <1 Set**, **64S V<1 Set**] but below the **64SI>1 Trip**, **64S R<2 Trip** and **64S R<1 Alarm** settings.

Set the voltage to half the **64S V<1 Set** and the current to half the **64S I< Set** and check the 64S Fail Alarm and 64S Fail operates and that there is no operation of the **64SI>1 Trip**, **64S R<2 Trip** and **64S R<1 Alarm** elements. (Bit 4 and 5 of [0F04: **Test Port Status**] is set to 1 and bits 1, 2, 3 = 0)

Check the yellow alarm led turns on when the relay operates. Check 'Alarms/Faults Present – 64S Fail Alarm' is on the display. Reset all alarms.

Check that the operating time recorded by the timer is within the range, **64S Superv'n Dly** setting ±2% or 1.2s whichever is greater with the P345 bandpass filter enabled and ±2% or 0.22 s whichever is greater with the P345 bandpass filter disabled. The P345 bandpass filter is automatically enabled when the system frequency is <45 Hz or it can be permanently enabled using DDB 555, 64S Filter On.

Allowance must also be made for the accuracy of the test equipment being used.

On completion of the tests any protection elements that were disabled for testing purposes must have their original settings restored in the **CONFIGURATION** column.

6.3.5.5 64S calibration procedure

The 100% stator earth fault protection can be calibrated with the machine at standstill, because the measuring principle for the earth resistance calculation is independent of whether the machine is at standstill, rotating or excited. A prerequisite is, however, that the 20 Hz generator must be supplied with a DC voltage or an external ac voltage source depending on the application, (see the connection diagrams in *P34x/EN/IN*).

Ensure that the cell [0F0D: **COMMISSIONING TESTS**, **Test Mode**] is set to **Contacts Blocked**. This blocks the operation of the Trip Contacts. Check the Out of Service LED is on and the alarm message 'Prot'n Disabled' is given.

The following measurements are available in the Measurements 3 column. All measurements are based on the 20 Hz components extracted from the voltage and current signals. A magnitude threshold level of 0.05 V and 0.1mA for the voltage and current is implemented, below which the associated measurements display zero. The 64S R is the compensated resistance in both primary and secondary quantities. The resistance measurement displays a significantly large number to indicate an invalid measurement if either the voltage or the current magnitude is below the threshold. The 64S Voltage signal is used as the phase reference for the 64S current signal.

MEASUREMENTS 3
64S V Magnitude
64S I Magnitude
64S I Angle
64S R secondary
64S R primary

The purpose of the 64S calibration procedure is to establish the correct settings for the angle compensation (**64S Angle Comp**), the Series Resistance (**64S Series R**) and the parallel conductance (**64S Parallel G**). They are required so that the relay can calculate more accurately the value of the fault resistance Rf based on the equivalent circuit as shown below.

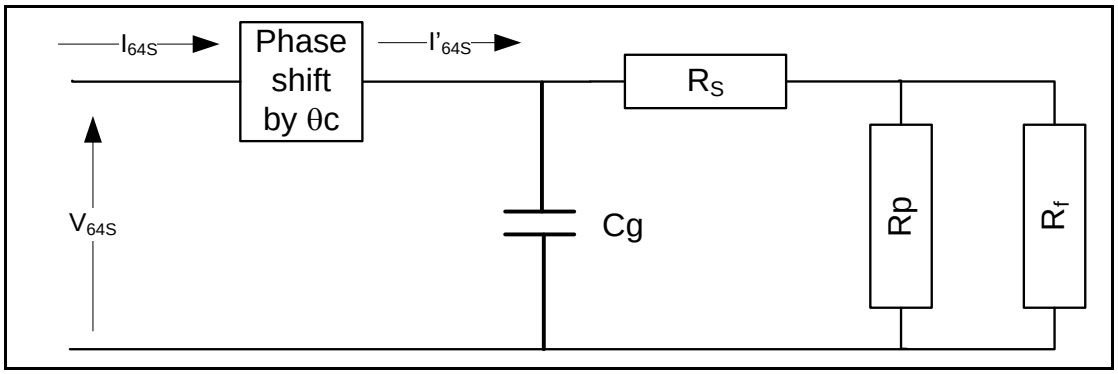


Figure 14: Calibration model for the 64S

To obtain the correct results, it is essential that the **64S R Factor** should have already been established and has been entered into the relay. The **64S Angle Comp, 64S Series R** and **64S Parallel G** settings should all be set to 0 initially.

As the calibration procedure requires fault resistance to be applied to the star point of the generator which is on the primary circuit, it is better to proceed with the calibration based on primary settings and measurements. Therefore in the Configuration column, the **Setting Values** should be set to **Primary**. For the **64S R** measurement, the primary value should also be used.

Caution: Dangerous high voltages may be present at the generator terminals if the 20 Hz injection voltage is not removed when the generator is taken out of service.

If the 20 Hz injection voltage generator receives power from the generator terminal voltage, then the 20 Hz injection voltage generator will be automatically switched off whenever the generator terminal voltage is not present.

6.3.5.5.1 Angle compensation setting (**64S angle comp**)

The angle compensation setting is used to remove any phase error caused by the internal and external CTs associated with the 64S current measurement. To establish this setting, it is necessary to remove any parallel earthing point such as an additional earthing transformer which may contribute to the presence of the parallel resistance Rp in Figure 4.

Under no fault condition, the relay should only see the lumped capacitance Cg on the system. The I64S should be capacitive and should lead the voltage V64S by +90°. The **64S Angle Comp** setting should be adjusted so that the +90° is achieved. The measurement **64S I Angle** displays the angle of I'64S with respect to V64S and can be used to assist with this setting adjustment.

6.3.5.5.2 Series resistance setting (64S Series R)

After the angle compensation setting has been set, the series resistance RS can be established by applying a short circuit fault at the generator star point. With the **64S Series R** setting originally set to zero, the relay is now measuring the resistance due to the earthing transformer and its connecting cables.

In order to compensate for this extra resistance of the circuit, the value read from the **64S R Primary** measurement should be entered into the **64S Series R** setting. After the setting has been entered, the **64S R Primary** measurement should now read zero.

6.3.5.5.3 Calibration at the 64S alarm and trip settings

The above calibration procedures are performed under no fault and short-circuit fault conditions. To provide a better match of the relays **64S R Primary** measurement to the applied fault resistance across the whole range of fault resistance it may be necessary to re-adjust the **64S Angle Comp** setting and **64 Series R** setting at the **64S R<1 Alm Set** and **64S R<2Trip Set** points.

Apply a fault resistance equal to the **64S R<2 Trip** setting and adjust the **64S Angle Comp** and the **64S Series R** settings for a closer match to the relays measured resistance **64S R Primary** if required. Repeat the process with a fault resistance equal to the **64S R<1 Alarm** setting.

In general it is recommended that the **64S Series R** setting should only be used to provide minor adjustments of a few ohms and is more appropriate for trip or alarm threshold of less than a few hundred ohms. To provide a closer match of the relays **64S R Primary** measurement to the applied fault resistance at higher settings it is more effective to adjust the **64S Angle Comp** setting.

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Since the resistance measured by the relay is effectively equal to $\frac{V_{64S}}{I_{64S} * \cos(\theta_{I'64S-V64S})}$, if the measured resistance is less than expected, the **64S Angle Comp** setting should be adjusted such that the current vector will be rotated in the anti-clockwise direction. If the **64S Angle Comp** (θc) was originally set as a negative value (that is, the current vector was rotated clockwise by $|\theta c|°$), it should be set less negative so that the $I64S*\cos(\theta_{I'64S-V64S})$ denominator decreases in value. The reverse logic should be applied if the measured resistance is more than expected.

Finally apply various fault resistances, re-check the short-circuit condition and the no fault condition to ensure that the results are satisfactory. This whole process may need to be re-iterated to ensure the most desirable match.

6.3.5.5.4 Parallel conductance (64S Parallel G)

After the above settings have been finalized, re-connect any parallel earthing point of the system, then apply a no fault condition to the generator. The **64S R Primary** measured by the relay will be the parallel resistance Rp. It's reciprocal should then be applied to the **64S Parallel G** setting.

6.3.5.5.5 Checking with other resistance values

After the above calibration procedure, apply different fault resistance to the star point of the generator so as to obtain a complete set of measurements from the relay.

6.3.5.5.6 Testing the 100% stator earth fault protection on the generator

Insert on the primary side a resistance which corresponds to about 90 % of the resistance for the alarm stage, **64S R<1 Alm Set** and check that the **64S R<1 Alarm** is operated after the delay time **64S R<1 Alm Dly** (default setting 1.00s). Further reduce the earth resistance to 90 % of the trip stage pickup value **64S R<2 Trip Set** and check that the **64S R<2 Trip** is operated after the delay time, **64S R<2 Trip Dly** (default setting 1.00 sec). Also, if used check that the **64S I>1 Trip** is operated after the delay time, **64S I>1 Trip Dly** (default setting 1.00 sec). Reset all alarms.

Remove the test resistor.

If the 100% stator earth fault protection is blocked with the DDBs 64S I>1 Inhibit (552) or 64S R<1 Inhibit (553) or 64S R<2 Inhibit (554) using an opto-isolated input, the functioning of the input should be checked.

Switch off the voltage supply for the 20 Hz generator, or energize the block binary input. Check the yellow alarm led turns on and check 'Alarms/Faults Present - 64S Fail Alarm' is on the display (assuming the 64S Fail Alarm (DDB 383) is connected to the 64S Fail signal (DDB 1298) in the PSL). Switch on the 20 Hz generator or remove the block and reset all alarms.

If this alarm indication already occurs with the 20 Hz generator in operation, the monitoring threshold, **64S V<1 Set**, should be reduced. This can be the case if the loading resistance is very small (< 1 Ω).

Note: If the external band pass filter accessory is to be checked as well, short-circuit the earthing or neutral transformer on the secondary side with the machine at standing still, and switch the 20 Hz generator on. Multiply the operational measured value **64S I Magnitude** with the CT ratio of the miniature CT (such as 400 A/ 5A). The flowing current must be greater than 3 A. If the current is significantly less, the resonance frequency of the bandpass has changed. It can be better matched by adding or removing capacitors. Finally, remove the shorting link and check the galvanic isolation with the measured value **64S V Magnitude**.

6.3.5.6 Start-up tests

Ensure that the cell [0F0D: **COMMISSIONING TESTS**, **Test Mode**] is set to **Contacts Blocked**. This blocks the operation of the Trip Contacts. Check the Out of Service LED is on and the alarm message 'Prot'n Disabled' is given.

The 20 Hz generator and bandpass filter accessories of the protection device must be operational.

Start up the generator and excite it to maximum generator voltage.

Check the protection does not pick up.

Check that the resistance values, **64S R< primary/secondary**, in the **Measurements 3** menu are well in excess of the trip and alarm settings, **64S R<1 Alm Set/64S R<2 Trip Set** and the current value, **64S I Magnitude**, is at least half the overcurrent setting, **64S I>1 Trip Set**.

Shut down generator.

If the 100% stator earth fault protection operates during the generator start up there may be some zero sequence voltage being produced by the machine, depending on the type of starting, which could be superimposed on the 20 Hz voltage causing incorrect measurements. The P345 100% stator earth fault protection includes a low pass filter and a bandpass filter which will filter signal frequencies 0-15 Hz and >25 Hz. DDB 1297 **64S F Band Block** operates between 15-25 Hz and can be used in the Programmable Scheme Logic to block the 100% stator earth fault protection via the inhibit signals, DDBs 552 - 64S I> Inhibit, DDB 553 - 64S R<1 Inhibit, DDB 554 - 64S R<2 Inhibit.

Ensure that the cell [0F0D: **COMMISSIONING TESTS**, **Test Mode**] is set to **Disabled**. Check the Out of Service LED is off and the alarm message 'Prot'n Disabled' is reset.

On completion of the tests any protection elements that were disabled for testing purposes must have their original settings restored in the **CONFIGURATION** column.

6.3.6 P391 generator rotor earth fault protection




The user shall be familiar with all safety statements listed in this chapter and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.



Before connecting the P391 to compatible equipment, all applicable safety statements and warnings for the relevant equipment shall be considered, to minimize the likelihood of any safety hazards.



Isolate all voltage inputs, including the high voltage DC rotor winding supply before removing the P391 from its mounting, removing its front panel or transparent terminal cover.



The internal circuitry of the P391 is not protected against electrostatic discharges (ESD) when the front panel is removed. ESD precautions and a clean working environment should be maintained when setting the internal frequency jumper PL3.

See section 2 of the Installation Chapter, *P34x/EN IN*, 'Handling of Electronic Equipment' for information on electrostatic discharge precautions.



Under no circumstances should the high voltage DC rotor winding supply be connected directly to the P391 500 Ω internal calibration resistors (terminals A3, A5, B3 or B5).



Before connecting temporary test equipment or test circuits, all applicable ratings, safety statements and warnings for the relevant equipment shall be considered, to minimize the likelihood of any safety hazards.



Isolate all voltage inputs, including the high voltage DC rotor winding supply from all equipment before connecting or disconnecting test equipment or test circuits.

Ensure that test circuits will not cause an electric shock, burns, fire or explosion hazard during setup or testing.



Before energizing the P391 voltage inputs, ensure the unit is suitably mounted and mechanically secure and its front panel and transparent terminal cover are fitted.

The P391 front panel and transparent terminal cover shall remain in place at all times during operation of the unit.



Wiring between the DC rotor winding and the P391 shall be suitably rated to withstand at least twice the rotor winding supply voltage to earth. This is to ensure that the wiring insulation can withstand the inductive Electro Motive Force (EMF) voltage which will be experienced on disconnection or de-energization of the DC rotor winding supply.



Under no circumstances should the high voltage DC rotor winding supply be connected via MMLG or P990 test blocks. Both MMLG and P990 test blocks are not rated for continuous working voltages greater than 300 Vrms. These test blocks are not designed to withstand the inductive EMF voltages which will be experienced on disconnection or de-energization of the DC rotor winding supply.

The P391 provides generator Rotor Earth Fault (REF) protection using an integral coupling, injection and measurement circuit to monitor the rotor field winding for the presence of earth faults.

The P391 injects a square wave signal into the rotor field winding circuit and measures any change to the waveform characteristic caused by a change in resistance between the rotor winding circuit and earth (a rotor earth fault).

Continuous measurements are passed to the P342/3/4/5/6 protection relay for processing via a Current Loop Input/Output (CLIO) signaling circuit with an output range of 0-20 mA. The P391 CLIO output signal can be connected to any of the four CLIO inputs provided by the P342/3/4/5/6 range. Note: rotor earth fault protection is only available if the protection relay includes the CLIO hardware option.

The square wave frequency can be adjusted to 0.25 Hz, 0.5 Hz, or 1.0 Hz, selectable by a jumper link on the P391 unit. Note: The **Injection Freq** setting in the P342/3/4/5/6 **ROTOR EF** menu must also be adjusted to match the injection frequency setting of the P391.

All P342/3/4/5/6 protection elements except rotor earth fault protection should be disabled during rotor earth fault tests, to avoid spurious operation. These can be disabled in the P342/3/4/5/6 **CONFIGURATION** column. It is advisable to note any elements temporarily disabled so they can be re-enabled after testing.

6.3.6.1 Injection frequency selection




The user shall be familiar with all safety statements listed in section 6.3.6 of this commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

The P391 injects a square-wave voltage at a fixed injection frequency (Fg) into the generator field winding. A jumper link on the P391 unit (see section 11 in *P34x/EN IN*) is used to select the frequency 0.25 Hz or 0.5 Hz or 1 Hz. To change the injection frequency the P391 should be de-energized first before the front panel is removed to reveal the jumper link. The default factory position is 0.25 Hz. Note, the **Injection Freq** setting in the **ROTOR EF** menu in the P34x must be set to match the injection frequency link setting in the P391.

The injection frequency can be selected after measuring the rotor field winding capacitance to earth. Table 29 below provides recommendations for the injection frequency based on the capacitance measurement. If the operating time is important to the application, follow the guideline below to select the frequency for the injection signal. Otherwise, leave the module at its default jumper setting of 0.25 Hz.

The rotor capacitance can be measured with a capacitance meter by connecting the meter across the field winding to earth. The P391 should be disconnected from the rotor field winding. Measurement should be taken from the P391 cable ends shorted together (cables connected to A16-B16) and earth (cable connected to C6) to include the capacitance of any cables between the rotor field winding and the P391. The machine should be off line and the field excitation should be off during the capacitance measurement. The field breaker should be closed for the capacitance measurement.

Alternatively, apply a known resistance to the slip rings and earth as described in section 6.3.6.7 ‘Testing the rotor earth fault protection on the generator at standstill’. Then with the highest injection frequency set in the P391 and P345, 1 Hz, measure the insulation resistance. The measured resistance value **64R Fault** in the P34x **Measurements 3** menu indicates the rotor earth resistance. Then select the next highest injection frequency of 0.5 Hz and measure the insulation resistance. If the measured insulation resistances are the same, choose 1 Hz as the injection frequency. Otherwise select the lowest injection frequency of 0.25 Hz and measure the insulation resistance. If the measured insulation resistances at 0.5 Hz and 0.25 Hz are the same, choose 0.5 Hz as the injection frequency. Otherwise choose 0.25 Hz as the injection frequency.

Note: If there is no insulation deterioration, there is no leakage path via the field winding to earth and the insulation resistance value is extremely high. The relay provides capped values if the fault resistance measurement is beyond the supported range: 50 ohms to 1M ohms.

Field-to-Earth Capacitance (Cfg)	Jumper position	Injection signal frequency (Fg)	Time between each insulation resistance calculation	Calculation accuracy
Cfg <2.1 µF	Bottom	1 Hz	0.5 s	Within Specification
2.1 µF≤ Cfg ≤5 µF	Middle	0.5 Hz	1 s	Within Specification
5 µF≤ Cfg ≤10 µF	Top	0.25 Hz	2 s	Within Specification
Cfg >10 µF	Top	0.25 Hz	2 s	Not Within Specification

Table 29: Injection frequency for different field to earth capacitance values

Forced Rfault value	Forced or capped value	Value meaning
9.999 MΩ	Capped	Infinity value (divide by zero prevented).
9.998 MΩ	Forced	CLIO input data invalid
9.997 MΩ	Forced	Rotor EF protection disabled.
9.996 MΩ	Capped	R fault above upper limit (1 MΩ)
0 Ω	Capped	R fault below lower limit (50 Ω).

Table 30: Forced/capped resistance values

6.3.6.2 Calibration




The user shall be familiar with all safety statements listed in section 6.3.6 of this commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

Disconnect the rotor field winding and brush earth connection from the P391.

Connect the P342/3/4/5/6 and P391 to the 500 Ω calibration resistance (P391 terminals A3-A5 or B3-B5) as shown in Figure 5.

Check the measured resistance value **64R Fault** in the **Measurements 3** menu in the P34x relay. If the resistance measurement is not equal to 500 Ω use the **R Compensation** setting in the **ROTOR EF** menu to compensate the measurement until it is as close as possible to 500 Ω. The **R Compensation** value should be chosen so that the average value is nearest 500 Ω if the measurement is fluctuating between 2 values.

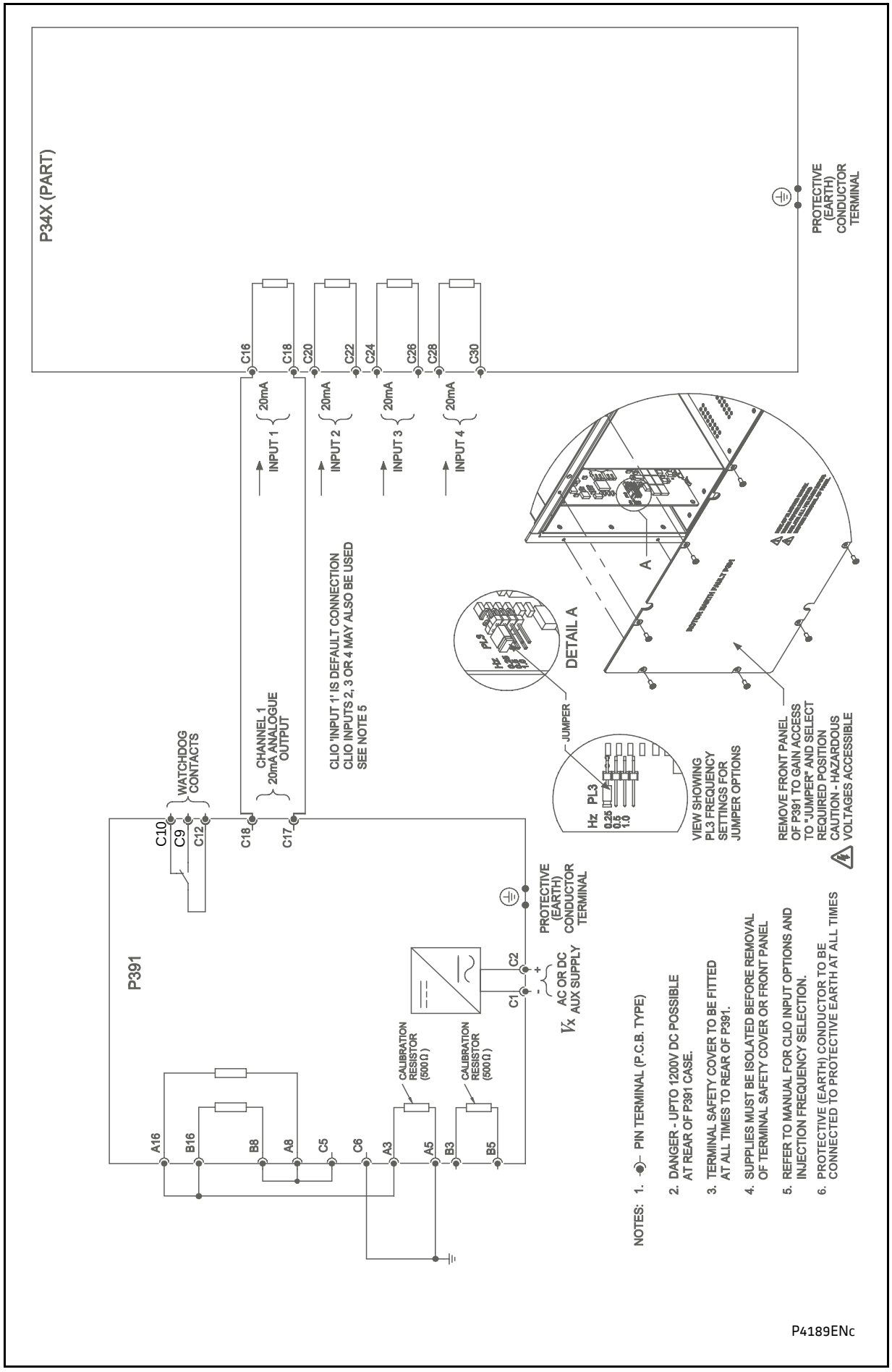


Figure 15: Calibration circuit for the 64R rotor earth fault protection

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6.3.6.3 Connect the test circuit




The user shall be familiar with all safety statements listed in section 6.3.6 of this commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

Determine which output relay has been selected to operate when a 64R R<2 Trip (DDB 780) and 64R R<1 Alarm (DDB 394) occurs by viewing the relay's programmable scheme logic.

The programmable scheme logic can only be changed using the appropriate software. If this software is not available then the default output relay allocations will still be applicable.

If the 64R protection signals are not independently mapped directly to an output relay in the programmable scheme logic, output relay 3 and 4 could be used in the default PSL to check the operation of the protection functions. In the default PSL relay 3 is the designated protection trip contact and 64R R<2 Trip (DDB 780) is assigned to this contact. In the default PSL relay 4 is the designated general alarm contact and 64R R<1 Alarm (DDB 394) is assigned to this contact. Note, in the default PSL relay 3 is set to operate the Any Trip signal (DDB 674) which initiates the trip LED.

The associated terminal numbers can be found from the external connection diagrams in chapter *P34x/EN IN*.

Connect the output relays so that its operation will trip the test set and stop the timer.

Connect the P342/3/4/5/6 and P391 to a resistance decade box or discrete resistance to represent to fault resistance and a capacitor to represent the field winding capacitance as shown in Figure 6.

To simulate a generator standstill condition no signal should be injected into the 3 phase voltage and current inputs.

Ensure that the timer will start when the current and voltage is applied to the relay.

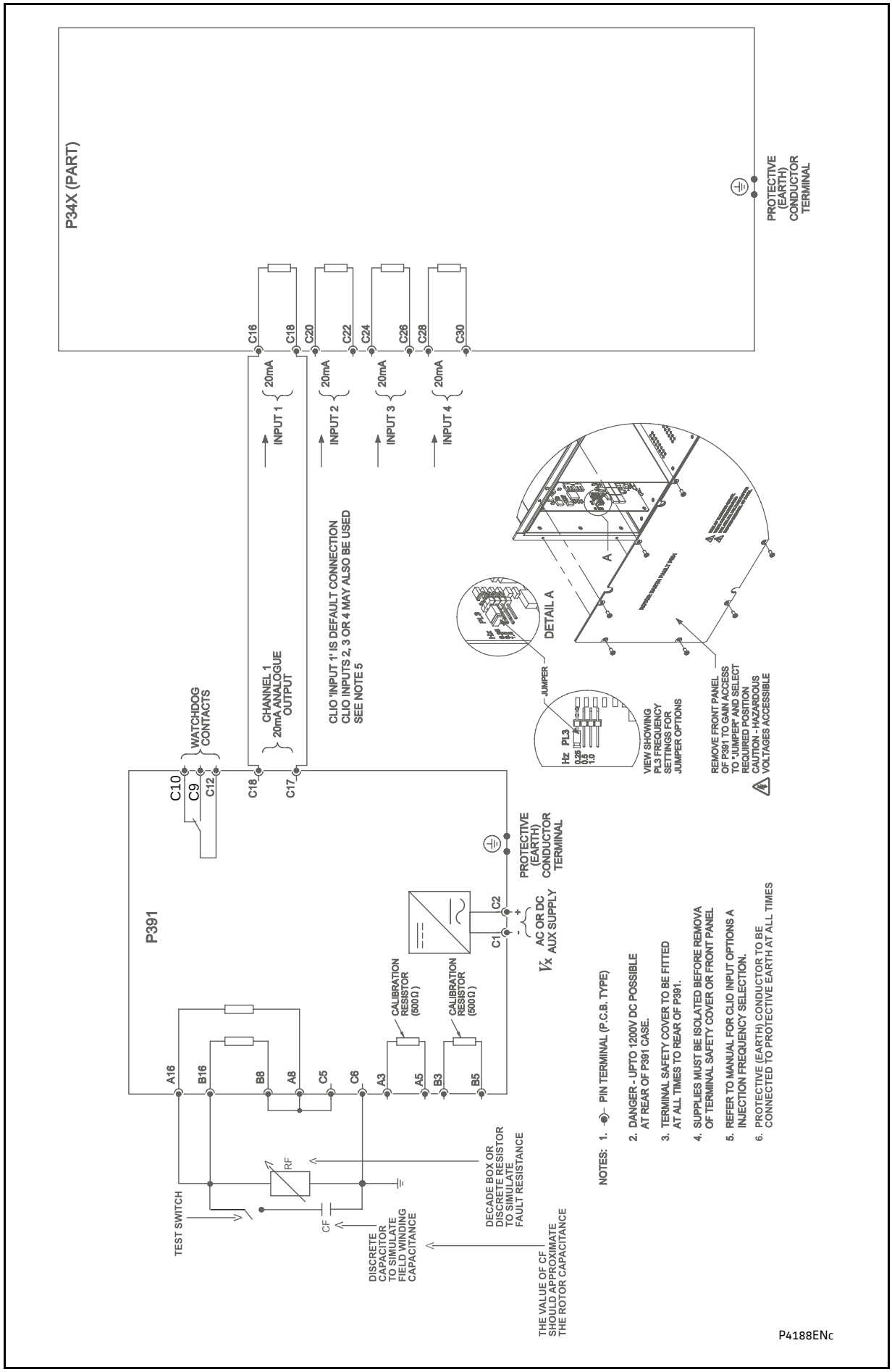


Figure 16: Test circuit for the 64R rotor earth fault protection

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6.3.6.4 Check the pick-up settings



The user shall be familiar with all safety statements listed in section 6.3.6 of this commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

Ensure that the following settings [**GROUP 1 ROTOR EF**, **Injection Freq, CL I/P Select**, **R Compensation** are set to the application values]

If two LEDs have been assigned to give the 64R alarm and trip start information, 64R R<2 Start (DDB 1023) and 64R Start R<1 Alm (DDB 1022), these may be used to indicate correct operation or alternatively the time delayed alarm and trip signals 64R R<2 Trip (DDB 780) and 64S R<1 Alarm Trip (DDB 394) can be used. If not, monitor options will need to be used - see the next paragraph.

Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F05: **Monitor Bit 1**] to 1023, [0F06: **Monitor Bit 2**] to 1022. Cell [0F04: **Test Port Status**] will now appropriately set or reset the bits that now represent 64R R<2 Start (DDB 1023) and 64R Start R<1 Alm (DDB 1022). From now on you should monitor the indication of [0F04: Test Port Status].

Set 64S R<2 Trip = **Enabled** and **64R R<1 Alarm** = **Disabled.**

Set the fault resistance to 10% above the trip setting and slowly reduce the resistance until the 64R R<2 start element operates (Bit 1 of [0F04: **Test Port Status**] is set to 1). Check that the resistance corresponds to the **64R R<2 Trip Set**, ±10% (1 k to 10 kΩ), ±5% (10 k to 80 kΩ). Note, the time the relay takes to update the resistance measurements will depend on the injection frequency, see table 15.

Switch OFF the test and reset the alarms.

Set **64S R<1 Alarm** = **Enabled** and **64R R<2 Trip** = **Disabled**.

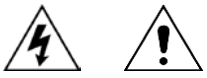
Set the fault resistance to 10% above the alarm setting and slowly reduce the resistance until the 64R R<1 start element operates (Bit 2 of [0F04: **Test Port Status**] is set to 1). Check that the resistance corresponds to the **64R R<1 Alm Set**, ±10% (1 k to 10 kΩ), ±5% (10 k to 80 kΩ).

Switch OFF the test and reset the alarms.

Note: The measured rotor resistance value **64R Fault** is shown in the **Measurements 3** menu.

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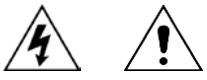
6.3.6.5 Checking with other resistance values



The user shall be familiar with all safety statements listed in section 6.3.6 of this commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

If required, after the above test procedure, apply different fault resistances so as to obtain a complete set of measurements from the relay. Use the **64R Fault** values in the **Measurements 3** menu to check the rotor earth resistance accuracy.

6.3.6.6 Perform the timing tests



The user shall be familiar with all safety statements listed in section 6.3.6 of this commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

Ensure that the timer is reset.

Set 64S R<2 Trip = **Enabled and 64S R<1 Alarm** = **Disabled**.

Apply a resistance of half the setting in cell [3918: **GROUP 1 ROTOR EF, 64R R<2 Trip Set**] to the relay and note the time displayed when the timer stops.

Check the red trip LED and yellow alarm LED turns on when the relay operates. Check 'Alarms/Faults Present - 64R Start R<2, 64R Trip R<2' is on the display. Reset all alarms.

Note: In the default PSL relay 3 is set to operate the Any Trip signal (DDB 674) which initiates the trip LED.

Check that the operating time recorded by the timer is within the range, 64S R<2 Trip Dly setting ±2% or 2.5/fs whichever is greater, fs = injection frequency.

Allowance must also be made for the accuracy of the test equipment being used.

Ensure that the timer is reset.

Set **64R R<2 Trip** = **Disabled** and **64R R<1 Alarm** = **Enabled**.

Apply a resistance to give half the setting in cell [390C: **GROUP 1 ROTOR EF**, **64R R<1 Alm Set**] to the relay and note the time displayed when the timer stops.

Check the yellow alarm LED turns on when the relay operates. Check 'Alarms/Faults Present – 64R Alarm R<1' is on the display. Reset all alarms.

Check that the operating time recorded by the timer is within the range, **64R R<1 Alm Dly** setting ±2% or 2.5/fs whichever is greater.

Allowance must also be made for the accuracy of the test equipment being used.

Ensure that the timer is reset.

6.3.6.7 Testing the rotor earth fault protection on the generator at standstill




The user shall be familiar with all safety statements listed in section 6.3.6 of this commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

The rotor earth fault protection can be checked with the machine at standstill. For this the P345 and P391 coupling unit must be connected to the rotor circuit as shown in the Installation Chapter, *P34x/EN IN*.

In the **Commission Tests** menu set the **Test Mode** setting to **Test Mode** which takes the relay out of service and blocks the maintenance counters. It also causes an alarm condition to be recorded and the yellow 'Out of Service' LED to illuminate and an alarm message 'Prot'n. Disabled' is given. The Test Mode menu cell is used to allow secondary injection testing to be performed on the relay without operation of the trip contacts.

First set the injection frequency setting as described in section 6.3.6.1.

Check the measured rotor to ground resistance value in fault free condition. The measured rotor resistance value should be very large, for example 9.996 MΩ. The measured rotor resistance value **64R Fault** is shown in the **Measurements 3** menu.

After this fault resistors equal to the **64R R<1 Alm Set** and the **64R R< Trip Set** settings are installed, and the resistance measurements **64R Fault** are checked against the resistor values. In machines with rotating rectifier excitation, the resistor is placed between the measurement slip rings. In machines with excitation via slip rings the resistor is placed between one slip ring and earth.

Finally, the alarm and the trip stages are checked. A test resistance is applied equal to 90 % of the set value and operation of the alarm and trip stage is checked. On machines with slipring excitation, the test is performed for both sliprings.

To check operation of the alarm and trip stages go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F05: **Monitor Bit 1**] to 780, [0F06: **Monitor Bit 2**] to 394. Cell [0F04: **Test Port Status**] will now appropriately set or reset the bits that now represent 64R R<2 Trip (DDB 780) and 64R R<1 Alm (DDB 394).

Remove the earth fault resistor and check the resistance measurement is similar to the value measured previously for a fault free condition.

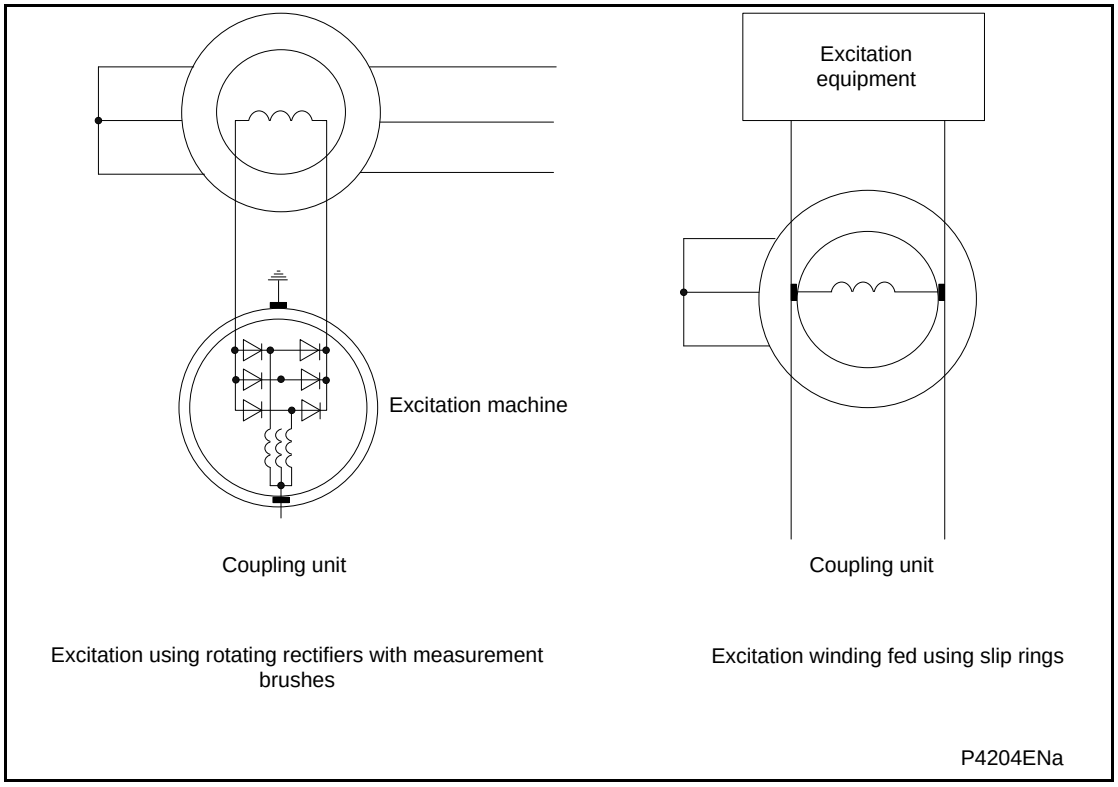


Figure 17: Types of excitation

6.3.6.8 Testing the rotor earth fault protection on the generator when running

The user shall be familiar with all safety statements listed in section 6.3.6 of this commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

To eliminate interference which might originate from a running machine, in particular from the excitation system, it is recommended to perform an additional check with the machine running.

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If the rotor circuit is not isolated from earth, insertion of the test resistor to earth can result in a double earth fault. Non observance of the following procedures could result in fatal injury or equipment damage. Ensure that the rotor circuit is completely isolated from earth, to avoid the test earthing resistor from causing a double earth fault.

Start up the generator and excite to the rated voltage. If applicable place measurement brushes into operation. In fault free condition the measured rotor resistance value should be very large, for example 9.996 MΩ. The measured rotor resistance value **64R Fault** is shown in the **Measurements 3** menu. Shut down generator.

In machines with rotating rectifier excitation, the resistor is placed between the measurement slip rings. In machines with excitation via slip rings the resistor is placed between one slip ring and earth.

Set the resistor to approximately 90% of the trip resistance **64R R<2 Trip Set**. Start up the generator and excite to the rated voltage. Check the measured resistance value **64R Fault** in the **Measurements 3** menu and check the 64R R<2 Trip (DDB 780) has operated. Shut down generator. For generators with excitation via slip rings, the test is repeated for the other slip ring.

Set the resistor to 90% of the alarm resistance **64R R<2 Alm Set**. Start up the generator and excite to the rated voltage. Check the measured resistance value **64R Fault** in the **Measurements 3** menu and check the 64R R<2 Alm (DDB394) has operated. Shut down generator. For generators with excitation via slip rings, the test is repeated for the other slip ring.

Remove the earth fault resistor. Start up the generator and excite to the rated voltage and check the resistance measurement is similar to the value measured previously for a fault free condition. Shut down generator.

To check operation of the alarm and trip stages go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F05: **Monitor Bit 1**] to 780, [0F06: **Monitor Bit 2**] to 394. Cell [0F04: **Test Port Status**] will now appropriately set or reset the bits that now represent 64R R<2 Trip (DDB 780) and 64R R<1 Alm (DDB 394).

In the **Commission Tests** Menu set the **Test Mode** setting to **Disabled** which puts the relay back into service. Check yellow 'Out of Service' and 'Alarm' LED and alarm message 'Prot'n. Disabled' are reset.

6.3.7 Peak and RMS overcurrent protection (P348)

The Peak and RMS overcurrent protection function I >1 Peak and I >5 RMS element should be tested.

To avoid spurious operation of any other protection elements all protection elements except the overcurrent protection should be disabled for the duration of the overcurrent element tests. This is done in the relay's **CONFIGURATION** column. Make a note of which elements need to be re-enabled after testing.

To set up IEC 61850-9-2 LE configuration with one or more logical nodes see sections 5.2.14 and 5.2.14.2.

6.3.7.1 Connect the test circuit

Determine which output relay has been selected to operate when a I >1 Peak Trip and I >1 RMS Trip occurs by viewing the relay's programmable scheme logic.

The programmable scheme logic can only be changed using the appropriate software. If this software has not been available then the default output relay allocations will still be applicable.

If the trip outputs are phase-segregated (that is a different output relay allocated for each phase), the relay assigned for tripping on 'A' phase faults should be used.

If I >1 and I >5 is not mapped directly to an output relay in the programmable scheme logic, output relay 3 (N5 - N6 in the 80TE case) should be used for the test as relay 3 initiates the trip LED. In the default PSL relay 3 is the designated protection trip contact and DDB 784 I >1 Peak Trip and DDB 800 I >5 RMS Trip are assigned to this contact.

Three Pole Tripping	DDB 784: I >1 Peak Trip DDB 800: I >1 RMS Trip
Single Pole Tripping	DDB 785: I >1 Peak Trip A DDB 786: I >1 Peak Trip B DDB 787: I >1 Peak Trip C DDB 801: I >1 RMS Trip A DDB 802: I >1 RMS Trip B DDB 803: I >1 RMS Trip C

Table 31: Overcurrent protection DDBs

The associated terminal numbers can be found from the external connection diagrams in the Installation chapter *P34x/EN IN*.

Connect the output relay so that its operation will trip the test set and stop the timer.

Connect the IEC 61850-9-2 LE port of the test set to the IEC 61850-9-2 LE port of the relay.

Ensure that the timer will start when the current is applied to the relay.

6.3.7.2 Peak overcurrent pick-up test

If an LED has been assigned to give the I>1 Peak Trip (DDB 784), this may be used to indicate correct operation. If not, monitor options can to be used - see the next paragraph.

Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F05: **Monitor Bit 1**] to 784. Cell [0F04: Test Port Status] will now appropriately set or reset the bits that now represent I>1 Peak Trip (DDB 784) with the rightmost bit representing I>1 Peak Trip. From now on you should monitor the indication of [0F04: **Test Port Status**].

Slowly increase the A phase dc current to the appropriate current inputs (**IA-1 I, B-1, IC-1** or **IA-2, IB-2, IC-2**) as set by the **I>1 CT Source** until the I>1 Peak element trips.

(Bit 1 of [0F04: **Test Port Status**] is set to 1). Record the dc current magnitude and check that it corresponds to the □>1 Current Set ±5%.

Switch OFF the test and reset the alarms.

6.3.7.3 Peak overcurrent timing test

Ensure that the timer is reset.

Apply A phase dc current to the appropriate current inputs (**IA-1, IB-1, IC-1** or **IA-2, IB-2, IC-2**) as set by the **I >1 CT Source** of twice the setting in cell [3527: **GROUP 1 OVERCURRENT, I >1 Current Set**] to the relay and note the time displayed when the timer stops.

Check the red trip led and yellow alarm led turns on when the relay operates. Check 'Alarms/Faults Present – 'Started Phase A, Tripped Phase A, Overcurrent Start I>1 Peak, Overcurrent Trip I>1 Peak' is on the display. Reset all alarms.

Note: The trip led is initiated from operation of relay 3, the protection trip contact in the default PSL.

Check that the operating time recorded by the timer is within the range, I>1 Time Delay setting ±2% or 50ms whichever is greater.

Allowance must also be made for the accuracy of the test equipment being used.

Ensure that the timer is reset.

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6.3.7.4 RMS overcurrent pick-up test

If an LED has been assigned to give the I>5 RMS Trip (DDB 800), this may be used to indicate correct operation. If not, monitor options can to be used - see the next paragraph.

Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F05: **Monitor Bit 1**] to 800. Cell [0F04: Test Port Status] will now appropriately set or reset the bits that now represent I>5 RMS Trip (DDB 800) with the rightmost bit representing I>5 RMS Trip. From now on you should monitor the indication of [0F04: **Test Port Status**].

Slowly increase the A phase ac current to the appropriate current inputs (**IA-1, IB-1, IC-1** or **IA-2, IB-2, IC-2**) as set by the **I>1 CT Source** until the I>5 RMS element trips.

(Bit 1 of [0F04: **Test Port Status**] is set to 1). Record the dc current magnitude and check that it corresponds to the I >5 Current Set ±5%.

Switch OFF the test and reset the alarms.

6.3.7.5 RMS overcurrent timing test

Ensure that the timer is reset.

Apply A phase ac current (50 or 60Hz) to the appropriate current inputs (**IA-1, IB-1, IC-1** or **IA-2, IB-2, IC-2**) as set by the **I>5 CT Source** of twice the setting in cell [35A4: **GROUP 1 OVERCURRENT**, I**>5 Current Set**] to the relay and note the time displayed when the timer stops.

Check the red trip led and yellow alarm led turns on when the relay operates. Check 'Alarms/Faults Present – 'Started Phase A, Tripped Phase A, Overcurrent Start I>5 RMS, Overcurrent Trip I>5 RMS' is on the display. Reset all alarms.

Note: The trip led is initiated from operation of relay 3, the protection trip contact in the default PSL.

Check that the operating time recorded by the timer is within the range shown in Table 20.

Note: Except for the definite time characteristic, the operating times given in Table 20 are for a time multiplier or time dial setting of 1. Therefore to obtain the operating time at other time multiplier or time dial settings, the time given in Table 20 must be multiplied by the setting of cell [35A6: **GROUP 1 OVERCURRENT**, **I>5 TMS**] for IEC and UK characteristics or cell [35A7: **GROUP 1 OVERCURRENT**, I>5 **Time Dial**] for IEEE and US characteristics.

In addition, for definite time and inverse characteristics there is an additional delay of up to 0.02 second and 0.08 second respectively that may need to be added to the relay's acceptable range of operating times.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

Characteristic	Operating time at twice current setting and time multiplier/time dial setting of 1.0	
	Nominal (seconds)	Range (seconds)
DT	[35A5: **I>5 Time Delay**] setting	Setting ±5% or 50ms whichever is greater
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	25.34 - 28
UK LT Inverse	120.00	114.00 - 126.00
IEEE M Inverse	3.8	3.61 - 3.99
IEEE V Inverse	7.03	6.68 - 7.38
IEEE E Inverse	9.52	9.04 - 10
US Inverse	2.16	2.05 - 2.27
US ST Inverse	12.12	11.51 - 12.73

Table 32: Characteristic operating times for I>5

On completion of the tests any protection elements that were disabled for testing purposes must have their original settings restored in the **CONFIGURATION** column.

7 ON-LOAD CHECKS

The following on-load measuring checks ensure the external wiring to the current and voltage inputs is correct but can only be carried out if there are no restrictions preventing the energization of the plant being protected.



Remove all test leads, temporary shorting leads, etc. and replace any external wiring that has been removed to allow testing.

If it has been necessary to disconnect any of the external wiring from the relay in order to perform any of the foregoing tests, it should be ensured that all connections are replaced in accordance with the relevant external connection or scheme diagram.

7.1 Voltage connections



Using a multimeter measure the voltage transformer secondary voltages to ensure they are correctly rated. Check that the system phase rotation is correct using a phase rotation meter.

Compare the values of the secondary phase voltages with the relays measured values, which can be found in the **MEASUREMENTS 1** menu column.

If cell [0D02: **MEASURE'T SETUP**, **Local Values**] is set to **Secondary**, the values displayed on the relay LCD or a portable PC connected to the front EIA(RS)232 communication port should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If cell [0D02: **MEASURE'T SETUP**, **Local Values**] is set to **Primary**, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the **CT & VT RATIOS** menu column (see Table 33 and **Error! Reference source not found.**). Again the values should be within 1% of the expected value, plus an additional allowance for the accuracy of the test equipment being used.

Voltage	Cell in MEASUREMENTS 1 Column (02)	Corresponding VT ratio (in VT and CT RATIO column (0A) of menu)
V_{AB}	[0214: VAB Magnitude]	[0A01: Main VT Primary] [0A02: Main VT Sec'y]
V_{BC}	[0216: VBC Magnitude]	
V_{CA}	[0218: VCA Magnitude]	
V_{AN}	[021A: VAN Magnitude]	
V_{BN}	[021C: VBN Magnitude]	
V_{CN}	[021E: VCN Magnitude]	
V_N	[0220: VN Measured Mag]	[0A05: VN VT Primary] [0A06: VN VT Sec'y]
V_{N2} (P344/5 only)	[0250: VN2 Measured Mag]	[0A03: VN2 VT Primary] [0A04: VN2 VT Sec'y]
C/S Voltage (P345 only)	[0270: MEASUREMENTS 1, C/S Voltage Mag] (P345 only)	[0A16: C/S VT Prim'y] [0A17: C/S VT Sec'y]

Table 33: Measured voltages and VT ratio settings P342-6

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Voltage	Cell in MEASUREMENTS 1 Column (02)	Corresponding VT ratio (in VT and CT RATIO column (0A) of menu)
$V_{AB-1\ RMS}$	[0293: MEASUREMENTS 1, VAB-1 RMS]	[0A01: Main VT Primary] [0A02: Main VT Sec'y]
$V_{BC-1\ RMS}$	[0294: MEASUREMENTS 1, VBC-1 RMS]	
$V_{CA-1\ RMS}$	[0295: MEASUREMENTS 1, VCA-1 RMS]	
$V_{N-1\ Derived\ RMS}$	[028E: MEASUREMENTS 1, VN-1 Derived RMS]	

Table 34: Measured voltages and VT ratio settings P348

7.2 Current connections

Measure the current transformer secondary values for each input using a multimeter connected in series with corresponding relay current input.

Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of power flow by contacting the system control center.

Ensure the current flowing in the neutral circuit of the current transformers is negligible.

Compare the values of the secondary phase currents and phase angle with the relay's measured values, which can be found in the **MEASUREMENTS 1** menu column.

Note: Under normal load conditions the earth fault function will measure little, if any, current. It is therefore necessary to simulate a phase to neutral fault. This can be achieved by temporarily disconnecting one or two of the line current transformer connections to the relay and shorting the terminals of these current transformer secondary windings.

Check that the IA/IB/IC Differential currents (P343-6) measured on the relay are less than 10% of the IA/IB/IC Bias currents, see the **Measurements 3** menu. Check that the I2 Magnitude negative phase sequence current measured by the relay is not greater than expected for the particular installation, see the **Measurements 1** menu. Check that the active and reactive power (P342-6) measured by the relay are correct, see the **Measurements 2** menu. The power measurement modes are described in the Measurements and Recording chapter, *P34x/EN MR*.

If cell [0D02: **MEASURE'T SETUP**, **Local Values**] is set to **Secondary**, the currents displayed on the relay LCD or a portable PC connected to the front EIA(RS)232 communication port should be equal to the applied secondary current. The values should be within 1% of the applied secondary currents. However, an additional allowance must be made for the accuracy of the test equipment being used.

If cell [0D02: **MEASURE'T SETUP**, **Local Values**] is set to **Primary,** the currents displayed should be equal to the applied secondary current multiplied by the corresponding current transformer ratio set in **CT & VT RATIOS** menu column (see Table 11 and Table 12). Again the values should be within 1% of the expected value, plus an additional allowance for the accuracy of the test equipment being used.

Note: If a P342/3/4/5/6 relay is applied with a single dedicated current transformer for the earth fault function, it may not be possible to check the relay's measured values as the neutral current will be almost zero.

8 FINAL CHECKS

The tests are now complete.



Remove all test or temporary shorting leads, etc. If it has been necessary to disconnect any of the external wiring from the relay in order to perform the wiring verification tests, it should be ensured that all connections are replaced in accordance with the relevant external connection or scheme diagram.

Ensure that the relay has been restored to service by checking that cell [0F0D: **COMMISSIONING TESTS**, **Test Mode**] is set to **Disabled**.

If the relay is in a new installation or the circuit breaker has just been maintained, the circuit breaker maintenance and current counters should be zero. These counters can be reset using cell [0606: **CB CONDITION**, **Reset All Values**]. If the required access level is not active, the relay will prompt for a password to be entered so that the setting change can be made.

If the menu language has been changed to allow accurate testing it should be restored to the customer's preferred language.

If an MMLG or P991 test block is installed, remove the MMLB01 or P992 test plug and replace the MMLG cover so that the protection is put into service.

Ensure that all event records, fault records, disturbance records, alarms and LEDs have been reset before leaving the relay.

If applicable, replace the secondary front cover on the relay.

9 COMMISSIONING TEST RECORD

Date:		Engineer:	
Station:		Circuit:	
		System Frequency:	Hz
VT Ratio:	/ V	CT Ratio (tap in use):	/ A

Front Plate Information

Generator protection relay	P34
Model number	
Serial number	
Rated current In	1A ☐ 5A ☐
Rated voltage Vn	
Auxiliary voltage Vx	

Test Equipment Used

This section should be completed to allow future identification of protective devices that have been commissioned using equipment that is later found to be defective or incompatible but may not be detected during the commissioning procedure.

Overcurrent test set	Model: Serial No:	
Phase angle meter	Model: Serial No:	
Phase rotation meter	Model: Serial No:	
Insulation tester	Model: Serial No:	
Setting software:	Type: Version:	

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Have all relevant safety instructions been followed? Yes ☐ No ☐

5. PRODUCT CHECKS

5.1 With the relay de-energized

5.1.1 Visual inspection

Relay damaged? Yes ☐ No ☐

Rating information correct for installation? Yes ☐ No ☐

Case earth installed? Yes ☐ No ☐

5.1.2 Current transformer shorting contacts close? Yes ☐ No ☐ Not checked ☐

5.1.3 Insulation resistance >100 MΩ at 500 V dc Yes ☐ No ☐ Not tested ☐

5.1.4 External wiring

Wiring checked against diagram? Yes ☐ No ☐

Test block connections checked? Yes ☐ No ☐ N/A ☐

5.1.5	Watchdog contacts (auxiliary supply off)						
	Terminals 11 and 12	Contact closed?	Yes	☐	No	☐	
		Contact resistance		Ω	Not measured	☐	
	Terminals 13 and 14	Contact open?	Yes	☐	No	☐	
5.1.6	Measured auxiliary supply			V ac/dc			
5.2	With the relay energized						
5.2.1	Watchdog contacts (auxiliary supply on)						
	Terminals 11 and 12	Contact open?	Yes	☐	No	☐	
	Terminals 13 and 14	Contact closed?	Yes	☐	No	☐	
		Contact resistance		Ω	Not measured	☐	
5.2.2	LCD front panel display						
	LCD contrast setting used						
5.2.3	Date and time						
	Clock set to local time?		Yes	☐	No	☐	
	Time maintained when auxiliary supply removed?		Yes	☐	No	☐	
5.2.4	Light emitting diodes						
	Relay healthy (green) LED working?		Yes	☐	No	☐	
	Alarm (yellow) LED working?		Yes	☐	No	☐	
	Out of service (yellow) LED working?		Yes	☐	No	☐	
	Trip (red) LED working?		Yes	☐	No	☐	
	All 8 (P342/3/4), 18 (P345) programmable LEDs working?		Yes	☐	No	☐	
5.2.5	Field supply voltage						
	Value measured between terminals 7 and 9			V dc			
	Value measured between terminals 8 and 10			V dc			
5.2.6	Input opto-isolators						
	Opto input 1	working?	Yes	☐	No	☐	
	Opto input 2	working?	Yes	☐	No	☐	
	Opto input 3	working?	Yes	☐	No	☐	
	Opto input 4	working?	Yes	☐	No	☐	
	Opto input 5	working?	Yes	☐	No	☐	
	Opto input 6	working?	Yes	☐	No	☐	
	Opto input 7	working?	Yes	☐	No	☐	
	Opto input 8	working?	Yes	☐	No	☐	
	Opto input 9	working?	Yes	☐	No	☐	
			N/A	☐			
	Opto input 10	working?	Yes	☐	No	☐	
			N/A	☐			
	Opto input 11	working?	Yes	☐	No	☐	
			N/A	☐			
	Opto input 12	working?	Yes	☐	No	☐	
			N/A	☐			

	Opto input 13	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 14	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 15	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 16	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 17	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 18	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 19	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 20	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 21	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 22	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 23	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 24	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 25	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 26	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 27	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 28	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 29	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 30	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 31	working?	Yes ☐	No ☐		
			N/A ☐			
	Opto input 32	working?	Yes ☐	No ☐		
			N/A ☐			
5.2.7	Output relays					
	Relay 1	working?	Yes ☐	No ☐		
		Contact resistance		Ω	Not measured ☐	
	Relay 2	working?	Yes ☐	No ☐		
		Contact resistance		Ω	Not measured ☐	
	Relay 3	working?	Yes ☐	No ☐		
		Contact resistance		Ω	Not measured ☐	

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Relay 4	working?		Yes ☐	No ☐
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 5	working?		Yes ☐	No ☐
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 6	working?		Yes ☐	No ☐
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 7	working?		Yes ☐	No ☐
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 8	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 9	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance		Ω	Not measured ☐
Relay 10	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance		Ω	Not measured ☐
Relay 11	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 12	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 13	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 14	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 15	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 16	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance	(N/C)	Ω	Not measured ☐
		(N/O)	Ω	Not measured ☐
Relay 17	working?		Yes ☐	No ☐
			N/A ☐	
	Contact resistance		Ω	Not measured ☐

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Relay 18	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 19	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 20	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 21	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 22	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 23	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance	(N/C)	Ω	Not measured ☐		
		(N/O)	Ω	Not measured ☐		
Relay 24	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance	(N/C)	Ω	Not measured ☐		
		(N/O)	Ω	Not measured ☐		
Relay 25	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 26	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 27	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 28	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 29	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 30	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance		Ω	Not measured ☐		
Relay 31	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance	(N/C)	Ω	Not measured ☐		
		(N/O)	Ω	Not measured ☐		
Relay 32	working?		Yes ☐	No ☐		
			N/A ☐			
	Contact resistance	(N/C)	Ω	Not measured ☐		
		(N/O)	Ω	Not measured ☐		

5.2.8 RTD inputs

Resistor tolerance

RTD 1 reading	[0412: RTD 1 Label]	%
RTD 2 reading	[0413: RTD 2 Label]	°C
RTD 3 reading	[0414: RTD 3 Label]	°C
RTD 4 reading	[0415: RTD 4 Label]	°C
RTD 5 reading	[0416: RTD 5 Label]	°C
RTD 6 reading	[0417: RTD 6 Label]	°C
RTD 7 reading	[0418: RTD 7 Label]	°C
RTD 8 reading	[0419: RTD 8 Label]	°C
RTD 9 reading	[041A: RTD 9 Label]	°C
RTD 10 reading	[041B: RTD 10 Label]	°C

5.2.9 Current loop inputs

CLI input type

0 - 1 mA ☐
0 - 10 mA ☐
0 - 20 mA ☐
4 - 20 mA ☐

CLI1 reading at 50% CLI maximum range
[0425: CLI1 Input Label]
CLI2 reading at 50% CLI maximum range
[0426: CLI2 Input Label]
CLI3 reading at 50% CLI maximum range
[0427: CLI3 Input Label]
CLI4 reading at 50% CLI maximum range
[0428: CLI4 Input Label]

5.2.10 Current loop outputs

0 - 1 mA ☐
0 - 10 mA ☐
0 - 20 mA ☐
4 - 20 mA ☐

CLO output type mA
CLO1 output current at 50% of rated output mA
CLO2 output current at 50% of rated output mA
CLO3 output current at 50% of rated output mA
CLO4 output current at 50% of rated output mA

5.2.11 First rear communications port

Communication standard

K-Bus ☐ MODBUS ☐
IEC 60870-5-103 ☐
DNP3* ☐ IEC 61850 ☐

Communications established? Yes ☐ No ☐

Protocol converter tested? Yes ☐ No ☐ N/A ☐

5.2.12 Ethernet communications port

Communication standard

IEC 61850 ☐
DNP 3.0 ☐

Communications established? Yes ☐ No ☐

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	Protocol converter tested?	Yes ☐	No ☐		
		N/A ☐			
		K-Bus	☐		
5.2.13	Second rear communications port	EIA(RS)485	☐		
		EIA(RS)232	☐		
	Communication port configuration	Yes ☐	No ☐		
	Communications established?	Yes ☐	No ☐		
		N/A ☐			
	Protocol converter tested?				
5.2.14	IEC 61850-9-2 LE communications port				
	Communication port configuration	Yes ☐	No ☐		
	Communications established?	Yes ☐	No ☐		
5.2.15	Current inputs				
	Displayed current	Primary ☐	Secondary ☐		
	Phase CT ratio	$\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	N/A ☐		
	Earth fault CT ratio	$\left(\frac{\text{[E/F CT Primary]}}{\text{[E/F CT Sec'y]}}\right)$	N/A ☐		
	SEF CT ratio	$\left(\frac{\text{[SEF CT Primary]}}{\text{[SEF CT Sec'y]}}\right)$	N/A ☐		

Input CT	Applied Value		Displayed Value	
IA	A		A	
IB	A		A	
IC	A		A	
IN	A	N/A ☐	A	N/A ☐
IN Sensitive/ISEF	A		A	
IA (2)	A	N/A ☐	A	N/A ☐
IB (2)	A	N/A ☐	A	N/A ☐
IC (2)	A	N/A ☐	A	N/A ☐

5.2.16	Voltage inputs				
	Displayed voltage	Primary ☐	Secondary ☐		
	Main VT ratio	$\left(\frac{\text{[Main VT Primary]}}{\text{[Main VT Sec'y.]}}\right)$	N/A ☐		
	VN VT ratio	$\left(\frac{\text{[VN VT Primary]}}{\text{[VN VT Secondary]}}\right)$	N/A ☐		
	VN2 VT ratio	$\left(\frac{\text{[VN2 VT Primary]}}{\text{[VN2 VT Secondary]}}\right)$	N/A ☐		
	C/S VT ratio	$\left(\left[\frac{C/S\ VT\ prim'y}{C/S\ VT\ Sec'y}\right]\right)$	N/A ☐		

CM

	Input VT	Applied Value	Displayed value
	Va	V	V
	Vb	V	V
	Vc	V	V
	VN	V	V
	VN2 (P344/5 only)	V	V
	C/S Voltage (P345 only)	V	V

6.	SETTING CHECKS					
6.1	Application-specific function settings applied?	Yes	☐	No	☐	
	Application-specific programmable scheme logic settings applied?	Yes	☐	No	☐	
		N/A	☐			
6.2	Application-specific function settings verified?	Yes	☐	No	☐	
		N/A	☐			
	Application-specific programmable scheme logic tested?	Yes	☐	No	☐	
		N/A	☐			
6.3	Demonstrate correct relay operation					
6.3.1	Generator differential protection (P343/4/5/6)					
6.3.1.2	Generator Differential lower slope pickup	A				
6.3.1.3	Generator Differential upper slope pickup	A				
6.3.2.1	Generator Differential Phase A contact routing OK?	Yes	☐	No	☐	
	Generator Differential Phase A trip time	s				
6.3.2.2	Generator Differential Phase B contact routing OK?	Yes	☐	No	☐	
	Generator Differential Phase B trip time	s				
6.3.2.3	Generator Differential Phase C contact routing OK?	Yes	☐	No	☐	
	Generator Differential Phase C trip time	s				
	Average trip time, Phases A, B and C	s				
6.3.3	Back-up phase overcurrent protection (P342/3/4/5/6)					
6.3.3.3	Check the operating time					
	I>1 Trip timing tested?	Yes	☐	No	☐	
	Applied current	A				
	Expected operating time	s				
	Measured operating time	s				
6.3.4	Generator-Transformer differential protection (P343/4/5/6)					
6.3.4.1	Low set element current sensitivity (Is1)	HV IA	A			
		HV IB	A			
		HV IC	A			
		LV IA	A			
		LV IB	A			
		LV IC	A			
6.3.4.2	Low set element operating time	HV IA	s			
		HV IB	s			
		HV IC	s			

CM

6.3.4.3	High set element current sensitivity (Is HS1)	HV IA	A
		HV IB	A
		HV IC	A
6.3.4.4	High set element operating time	HV IA	s
		HV IB	s
		HV IC	s

6.3.4.5 Differential through stability by primary injection OK? Yes ☐ No ☐

6.3.4.6 CT secondary wiring differential through stability test by secondary injection OK? Yes ☐ No ☐

6.3.4.7 Low set element bias characteristic

In (amps)	Is1 (pu)	0%				K1 = 30%				K2 = 80%			
		Trip		No trip		Trip		No trip		Trip		No trip	
		I1	I2	I1	I2	I1	I2	I1	I2	I1	I2	I1	I2
1	0.2												
5	0.2												

6.3.4.8 Second-harmonic blocking A

6.3.4.9 Fifth-harmonic blocking A

6.3.5 Generator 100% stator earth fault protection via low frequency injection (P345)

6.3.5.2 Check pickup settings

64S I> Trip tested? Yes ☐ No ☐

64S I>1 Trip pickup A

64S R<2 Trip tested? Yes ☐ No ☐

64S R<2 Trip pickup Ω

64S R<1 Alarm tested? Yes ☐ No ☐

64S R<1 Alarm pickup Ω

6.3.5.3 Perform timing tests

64S I>1 Trip timing tested? Yes ☐ No ☐

Applied current A

Expected operating time s

Measured operating time s

64S R<2 Trip timing tested? Yes ☐ No ☐

Applied impedance Ω

Expected operating time s

Measured operating time s

64S R<1 Alarm timing tested? Yes ☐ No ☐

Applied impedance Ω

Expected operating time s

Measured operating time s

CM

6.3.5.4	Perform the 100% stator earth fault supervision test				
	64S Supervision tested?	Yes	☐	No	☐
	Applied voltage		V		
	Applied current		A		
	Expected operating time		s		
	Measured operating time		s		
6.3.5.5	Calibration Tests				
	Establish the 64S angle compensation, series resistance and parallel conductance settings				
	64S Angle Comp		°		
	64S Series R		Ω		
	Calibration at the 64S alarm and trip settings				
	Primary resistance check of 64S R<2 Trip tested?	Yes	☐	No	☐
	Applied primary resistance		Ω		
	64S R Primary measurement		Ω		
	64S Angle Comp		°		
	64S Series R		Ω		
	Primary resistance check of 64S R<1 Alarm tested?	Yes	☐	No	☐
	Applied primary resistance		Ω		
	64S R Primary measurement		Ω		
	64S Angle Comp		°		
	64S Series R		Ω		
	64S Parallel G		S		
	Check with other resistance values				
	Applied primary resistance		Ω		
	64S R Primary measurement		Ω		
	Applied primary resistance		Ω		
	64S R Primary measurement		Ω		
	Applied primary resistance		Ω		
	64S R Primary measurement		Ω		
	Applied primary resistance		Ω		
	64S R Primary measurement		Ω		
	Applied primary resistance		Ω		
	64S R Primary measurement		Ω		
6.3.5	Testing the 100% stator earth fault protection on the generator				
6.3.5.2	Check the pick-up settings				
	Primary resistance check of 64S R<1 Alarm tested?	Yes	☐	No	☐
	Applied primary resistance		Ω		
	64S R Primary measurement		Ω		
	Expected operating time		s		
	Measured operating time		s		
	Primary resistance check of 64S R<2 Trip tested?	Yes	☐	No	☐
	Applied primary resistance		Ω		
	64S R Primary measurement		Ω		
	Expected operating time		s		
	Measured operating time		s		

	Primary resistance check of 64S I>1 Trip tested?	Yes	☐	No	☐
	Applied primary resistance		Ω		
	64S I Magnitude measurement		A		
6.3.5.3	Perform the timing tests				
	Expected operating time		s		
	Measured operating time		s		
6.3.5.4	Perform the supervision test				
	Supervision function tested?	Yes	☐	No	☐
	Primary resistance measurements checked?	Yes	☐	No	☐
6.3.5.6	Start-up Tests				
	Start-up test performed?	Yes	☐	No	☐
	64S R Primary measurement		Ω		
6.3.6	Generator rotor earth fault protection				
6.3.6.1	Select injection frequency				
	Applied injection frequency		Hz		
6.3.6.2	Calibration				
	R Compensation		Ω		
6.3.6.4	Check pickup settings				
	64R R<2 Trip tested?	Yes	☐	No	☐
	64R R<2 Trip pickup		Ω		
	64R R<1 Alarm tested?	Yes	☐	No	☐
	64R R<1 Alarm pickup		Ω		
6.3.6.5	Check with other resistance values				
	Applied primary resistance		Ω		
	64R R Fault measurement		Ω		
	Applied primary resistance		Ω		
	64R R Fault measurement		Ω		
	Applied primary resistance		Ω		
	64R R Fault measurement		Ω		
	Applied primary resistance		Ω		
	64R R Fault measurement		Ω		
	Applied primary resistance		Ω		
	64R R Fault measurement		Ω		
6.3.6.6	Perform timing tests				
	64R R<2 Trip timing tested?	Yes	☐	No	☐
	Applied resistance		Ω		
	Expected operating time		s		
	Measured operating time		s		
	64R R<1 Alarm timing tested?	Yes	☐	No	☐
	Applied resistance		Ω		

CM

	Expected operating time		s		
	Measured operating time		s		
6.3.6.7	Testing the rotor earth fault protection on the generator at standstill				
	Resistance check with no fault?	Yes	☐	No	☐
	64R R Fault measurement		Ω		
	Resistance check of 64S R<1 Alarm tested?	Yes	☐	No	☐
	Applied resistance		Ω		
	64R R Fault measurement		Ω		
	Resistance check of 64S R<2 Trip tested?	Yes	☐	No	☐
	Applied resistance		Ω		
	64R R Fault measurement		Ω		
	Operation check of 64S R<1 Alarm tested?	Yes	☐	No	☐
	Operation check of 64S R<1 Alarm tested?	Yes	☐	No	☐
6.3.6.8	Testing the rotor earth fault protection on the generator running				
	Resistance check with no fault?	Yes	☐	No	☐
	64R R Fault measurement		Ω		
	Operation check of 64S R<2 Trip tested?	Yes	☐	No	☐
	Operation check of 64S R<1 Alarm tested?	Yes	☐	No	☐
	Resistance check with no fault?	Yes	☐	No	☐
	64R R Fault measurement		Ω		
6.3.7	Peak and RMS overcurrent protection (P348)				
6.3.7.1	Peak overcurrent pickup settings				
	I>1 Peak Trip tested?	Yes	☐	No	☐
	I>1 Peak Trip pickup		A		
6.3.7.2	Peak overcurrent timing test				
	I>1 Peak Trip timing tested?	Yes	☐	No	☐
	Applied current		A		
	Expected operating time		s		
	Measured operating time		s		
6.3.7.3	RMS overcurrent pickup settings				
	I>5 RMS Trip tested?	Yes	☐	No	☐
	I>5 RMS Trip pickup		A		
6.3.7.4	RMS overcurrent timing test				
	I>5 RMS Trip timing tested?	Yes	☐	No	☐
	Applied current		A		
	Expected operating time		s		
	Measured operating time		s		
7.	ON-LOAD CHECKS				
	Test wiring removed?	Yes	☐	No	☐
		N/A	☐		

CM

	Disturbed customer wiring re-checked?			Yes ☐ N/A ☐	No	☐
	On-load test performed?			Yes ☐	No	☐
7.1	VT wiring checked?			Yes ☐ N/A ☐	No	☐
	Phase rotation correct?			Yes ☐	No	☐
	Displayed voltage			Primary ☐	Secondary	☐
	Main VT ratio	$\left(\frac{\text{[Main VT Primary]}}{\text{[Main VT Sec'y.]}}\right)$		V	N/A	☐
	VN VT ratio	$\left(\frac{\text{[VN VT Primary]}}{\text{[VN VT Secondary]}}\right)$		V	N/A	☐
	VN2 VT ratio	$\left(\frac{\text{[VN2 VT Primary]}}{\text{[VN2 VT Secondary]}}\right)$		V	N/A	☐
	C/S VT ratio	$\left(\left[\frac{C/S\ VT\ \ prim'y}{C/S\ VT\ \ Sec'y}\right]\right)$		V	N/A	☐

Voltages	Applied Value	Displayed value
VAN/VAB	V	V
VBN/VBC	V	V
VCN/VCA	V	V
VN	V	V
VN2 (P344/5 only)	V	V
C/S (P344/5 only)	V	V

7.2	CT wiring checked?			Yes ☐ N/A ☐	No	☐
	CT polarities correct?			Yes ☐	No	☐
	Displayed current			Primary ☐	Secondary	☐
	Phase CT ratio	$\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$		A	N/A	☐
	Earth Fault CT ratio	$\left(\frac{\text{[E/F CT Primary]}}{\text{[E/F CT Sec'y]}}\right)$		A	N/A	☐
	SEF CT ratio	$\left(\frac{\text{[SEF CT Primary]}}{\text{[SEF CT Sec'y]}}\right)$		A	N/A	☐

Currents	Applied Value		Displayed value		
IA	A		A		
IB	A		A		
IC	A		A		
IN	A	N/A ☐	A	N/A	☐
IN Sensitive/ISEF	A		A		
IA (2)	A	N/A ☐	A	N/A	☐
IB (2)	A	N/A ☐	A	N/A	☐
IC (2)	A	N/A ☐	A	N/A	☐

CM

8. FINAL CHECKS

Test wiring removed?	Yes ☐	No ☐	N/A ☐	
Disturbed customer wiring re-checked?	Yes ☐	No ☐	N/A ☐	
Test mode disabled?	Yes ☐	No ☐		
Circuit breaker operations counter reset?	Yes ☐	No ☐	N/A ☐	
Current counters reset?	Yes ☐	No ☐	N/A ☐	
Event records reset?	Yes ☐	No ☐		
Fault records reset?	Yes ☐	No ☐		
Disturbance records reset?	Yes ☐	No ☐		
Alarms reset?	Yes ☐	No ☐		
LEDs reset?	Yes ☐	No ☐		
Secondary front cover replaced?	Yes ☐	No ☐	N/A ☐	

Commissioning Engineer

Date:

Customer Witness

Date:

MAINTENANCE

MT

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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FIGURES

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1 MAINTENANCE

1.1 Maintenance period

It is recommended that products supplied by General Electric receive periodic monitoring after installation. As with all products some deterioration with time is inevitable. In view of the critical nature of protective relays and their infrequent operation, it is desirable to confirm that they are operating correctly at regular intervals.

General Electric protective relays are designed for life in excess of 20 years.

The P34x generator relays are self-supervising and so require less maintenance than earlier designs of relay. Most problems will result in an alarm so that remedial action can be taken. However, some periodic tests should be done to ensure that the relay is functioning correctly and the external wiring is intact.

If the customer's organization has a Preventative Maintenance Policy, the recommended product checks should be included in the regular program. Maintenance periods depend on many factors, such as:

- The operating environment
- The accessibility of the site
- The amount of available manpower
- The importance of the installation in the power system
- The consequences of failure

1.2 Maintenance checks

Although some functionality checks can be performed from a remote location using the communications ability of the relays, these are predominantly restricted to checking that the relay is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. Therefore, it is recommended that maintenance checks are performed locally (that is at the substation itself).

Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety and technical data sections and the ratings on the equipment's rating label.



Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section/Safety Guide Pxxx-SG-4LM-2 or later issue and the ratings on the equipment's rating label.

If a P391 is used the user should additionally be familiar with the ratings and warning statements in the P391 technical manual sections.

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1.2.1 Alarms

Check the alarm status LED to identify if any alarm conditions exist. If the LED is ON, press the read key [⊙] repeatedly to step through the alarms. Clear the alarms to switch the LED OFF.

1.2.2 Opto-isolators

Check the relay responds when the opto-isolated inputs are energized. See section 5.2.6 of *P34x/EN CM*.

1.2.3 Output relays

Check the output relays operate. See section 5.2.7 of *P34x/EN CM*.

1.2.4 Measurement accuracy

If the power system is energized, compare the values measured by the relay with known system values to check they are in the approximate expected range. If they are, the relay is performing the analog/digital conversion and calculations are being performed correctly. See sections 7.1 and 7.2 of *P34x/EN CM*.

Alternatively, check the values measured by the relay against known values injected into the relay using the test block, if fitted, or injected directly into the relay terminals. See sections 5.2.13 and 5.2.14 of *P34x/EN CM*. These tests prove the calibration accuracy is being maintained.

1.3 P34x method of repair

If the relay develops a fault while in service, depending on the type of the fault, the watchdog contacts change state and an alarm condition is flagged. Due to the extensive use of surface-mount components faulty PCBs cannot be repaired and should be replaced. Therefore either the complete relay or just the faulty PCB, identified by the in-built diagnostic software, can be replaced. See the Troublshooting chapter *P34x/EN TS*.

The preferred method is to replace the complete relay. This ensures the internal circuitry is protected against electrostatic discharge and physical damage at all times and avoids incompatibility between replacement PCBs. However, it may be difficult to remove an installed relay due to limited access in the back of the cubicle and rigidity of the scheme wiring.

Replacing PCBs can reduce transport costs but requires clean, dry conditions on site and higher skills from the person performing the repair. However, if the repair is not performed by an approved service center, the warranty will be invalidated.



Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section/Safety Guide Pxxx-SG-4LM-2 or later issue and the ratings on the equipment's rating label. This should ensure that no damage is caused by incorrect handling of the electronic components.

1.3.1 Replacing the complete relay

The case and the rear terminal blocks are designed to ease removal of the complete relay, without disconnecting the scheme wiring.



Before working at the rear of the relay, isolate all voltage and current supplies to the relay.

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Note: The MiCOM range of relays have integral current transformer shorting switches which will close when the heavy duty terminal block is removed.

1. Disconnect the relay earth connection from the rear of the relay.

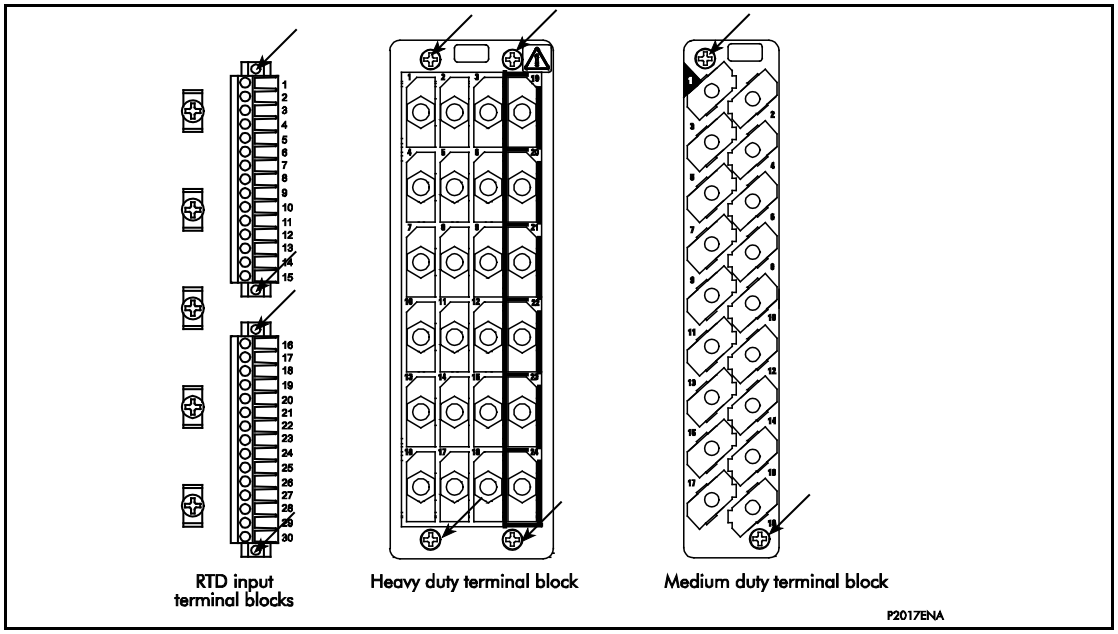


Figure 1: Location of securing screws for terminal blocks

There are three types of terminal block used on the relay, RTD/CLIO input, heavy duty and medium duty, which are fastened to the rear panel using screws (crosshead on the heavy and medium duty blocks, slotted on RTD/CLIO input blocks), as in Figure 1.

Note: The use of a magnetic bladed screwdriver is recommended to minimize the risk of the screws being left in the terminal block or lost.

2. Without exerting excessive force or damaging the scheme wiring, pull the terminal blocks away from their internal connectors.
3. Remove the screws used to fasten the relay to the panel, rack, etc. These are the screws with the larger diameter heads that are accessible with the access covers are fitted and open.

If the top and bottom access covers have been removed, do not remove the screws with the smaller diameter heads which are accessible. These screws hold the front panel on the relay.

4. Withdraw the relay from the panel, rack, etc. carefully because it will be heavy due to the internal transformers.
5. To reinstall the repaired or replacement relay follow steps 1 to 5 in reverse. Relocate each terminal block in the correct position. Replace the case earth, IRIG-B and fiber optic connections. To help identify each terminal block, they are labeled alphabetically with 'A' on the left hand side when viewed from the rear.

Once reinstallation is complete the relay should be recommissioned using the instructions in the Commissioning chapter *P34x/EN CM*.

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1.3.2 Replacing a PCB

Replacing printed circuit boards and other internal components of protective relays must be undertaken only by Service Centers approved by General Electric. Failure to obtain the authorization of General Electric After Sales Engineers prior to commencing work may invalidate the product warranty.

General Electric Support teams are available world-wide and it is strongly recommended that any repairs be entrusted to those trained personnel.

If the relay fails to operate correctly refer to the Troublshooting chapter *P34x/EN TS*, to help determine which PCB is faulty.

1. To replace any of the relay's PCBs it is necessary to first remove the front panel.

Before removing the front panel to replace a PCB the auxiliary supply must be removed. It is also strongly recommended that the voltage and current transformer connections and trip circuit are isolated.

2. Open the top and bottom access covers. With size 60TE/80TE cases the access covers have two hinge-assistance T-pieces which clear the front panel molding when the access covers are opened by more than 90°, therefore allowing their removal.
3. If fitted, remove the transparent secondary front cover. A description of how to do this is given in document 'Introduction'.
4. By applying outward pressure to the middle of the access covers, they can be bowed sufficiently so as to disengage the hinge lug allowing the access cover to be removed. The screws that fasten the front panel to the case are now accessible.
5. The size 40TE case has four crosshead screws fastening the front panel to the case, one in each corner, in recessed holes. The size 60TE/80TE case has an additional two screws, one midway along each of the top and bottom edges of the front plate. Undo and remove the screws.

Do not remove the screws with the larger diameter heads which are accessible when the access covers are fitted and open. These screws hold the relay in its mounting (panel or cubicle).

6. When the screws have been removed, the complete front panel can be pulled forward and separated from the metal case.

Caution should be observed at this stage because the front panel is connected to the rest of the relay circuitry by a 64-way ribbon cable.

Additionally, from here on, the internal circuitry of the relay is exposed and not protected against electrostatic discharges, dust ingress, etc. Therefore, ESD precautions and clean working conditions should be maintained at all times.

The ribbon cable is fastened to the front panel using an IDC connector; a socket on the cable itself and a plug with locking latches on the front panel. Gently push the two locking latches outwards which will eject the connector socket slightly. Remove the socket from the plug to disconnect the front panel.

The PCBs in the relay are now accessible. Figures 63 to 73 in the Installation chapter *P34x/EN IN* show the PCB locations for the generator relays in the size 40TE case (P342), size 60TE case (P342 and P343/6) and size 80TE case (P343/4/5/6) respectively.

Note: The numbers above the case outline identify the guide slot reference for each printed circuit board. Each printed circuit board has a label stating the corresponding guide slot number to ensure correct re-location after removal. To serve as a reminder of the slot numbering there is a label on the rear of the front panel metallic screen.

The 64-way ribbon cable to the front panel also provides the electrical connections between PCBs with the connections being via IDC connectors.

The slots inside the case to hold the PCBs securely in place each correspond to a rear terminal block. Looking from the front of the relay these terminal blocks are labeled from right to left.

Note: To ensure compatibility, always replace a faulty PCB with one of an identical part number. Table 1 lists the part numbers of each PCB type.

PCB		Part number	Design suffix
Main processor board		ZN0006 001	A/B/C
Main processor board	P341/2	ZN0026 001	J
Main processor board	P343/4/5/6 only	ZN0041 001	K
Power supply board	(24/48 V dc)	ZN0001 001	A/B
Main processor board	P342	ZN0070 102	P

PCB		Part number	Design suffix
Main processor board	P343/4/5/6/8	ZN0069 102	M
Power supply board	(24/48 V dc)	ZN0021 001	C/J/K
	(48/125 V dc)	ZN0021 002	C/J/K
	(110/250 V dc)	ZN0021 003	C/J/K
Power supply board	(24/48 V dc)	ZN0021 201	M/P
	(48/125 V dc)	ZN0021 202	M/P
	(110/250 V dc)	ZN0021 203	M/P
Relay board	7 Relay contacts	ZN0002 001	A
Relay board	7 Relay contacts	ZN0031 101	B/C/J/P
Relay board	8 Relay contacts	ZN0019 101	B/C/J/K/M/P
Relay board	4 high break contacts	ZN0042 001	J/K/M/P
Opto board	8 Opto inputs	ZN0005 002	A
Opto board	8 Opto inputs	ZN0017 002	B/C
Dual char. opto board	8 Opto inputs	ZN0017 212	J/K/M/P
Dual input/output board	4 Opto inputs + 4 relay contacts	ZN0028 002	B/C
Dual char. input/output board	4 Opto inputs + 4 relay contacts	ZN0028 211	J/P
IRIG-B board (comms. assy.)	(IRIG-B modulated input only)	ZN0007 001	A/B/C/J/K/M/P
	(Fiber optic port only)	ZN0007 002	A/B/C/J/K/M/P
	(IRIG-B input modulated with fiber optic port)	ZN0007 003	A/B/C/J/K/M/P
RTD board	10 RTDs	ZN0010 001	A/B/C/J
RTD board	10 RTDs	ZN0044 001	J/K/M/P
2nd rear comms. board	(2nd rear comms with IRIG-B modulated)	ZN0025 001	C/J/K/M/P
2nd rear comms. board	(2nd rear comms port only)	ZN0025 002	C/J/K/M/P
Ethernet board	(Ethernet port only)	ZN0049 001	J/K/M/P
	(Ethernet with IRIG-B modulated)	ZN0049 002	J/K/M/P
	(Ethernet with IRIG-B un-modulated)	ZN0049 003	J/K/M/P
	(IRIG-B un-modulated input only)	ZN0049 004	J/K/M/P
	Redundant Ethernet Self-Healing Ring, 2 multi-mode fiber ports + Modulated IRIG-B	ZN0071 001	J/K/M/P
	Redundant Ethernet Self-Healing Ring, 2 multi-mode fiber ports + Unmodulated IRIG-B	ZN0071 002	J/K/M/P
	Redundant Ethernet RSTP, 2 multi-mode fiber ports + Modulated	ZN0071 005	J/K/M/P
	Redundant Ethernet RSTP, 2 multi-mode fiber ports + Unmodulated IRIG-B	ZN0071 006	J/K/M/P
	Redundant Ethernet Dual-Homing Star, 2 multi-mode fiber ports + Modulated IRIG-B	ZN0071 007	J/K/M/P

PCB		Part number	Design suffix
	Redundant Ethernet Dual-Homing Star, 2 multi-mode fiber ports + Unmodulated IRIG-B	ZN0071 008	J/K/M/P
	Redundant Ethernet PRP, 2 multi-mode fibre ports + Modulated IRIG-B	ZN0071 009	J/K/M/P
	Redundant Ethernet PRP, 2 multi-mode fibre ports + Un-modulated IRIG-B	ZN0071 010	J/K/M/P
CLIO board	4 inputs + 4 outputs	ZN0018 001	C/J/K
Transformer board		ZN0004 001	A/B/C/J/K/M/P
Auxiliary transformer board		ZN0011 001	A/B/C/J/P
Auxiliary transformer board	P345 only	ZN0052 001	K/M
Input board	8 Opto inputs	ZN0005 001	A
Input board	8 Opto inputs	ZN0017 001	B/C
Dual char. input board	8 Opto inputs	ZN0017 212	J/K/M/P
Input module (transformer + auxiliary transformer + input board)	P341 Vn = 100/120 V	GN0010 004	A
	P341 Vn = 380/480 V	GN0010 008	A
	P342 Vn = 100/120 V	GN0010 009	A
	P342 Vn = 380/480 V	GN0010 010	A
	P343 Vn = 100/120 V	GN0012 002	A
	P343 Vn = 380/480 V	GN0012 003	A
	P341 Vn = 100/120 V	GN0010 024	B/C
	P341 Vn = 380/480 V	GN0010 028	B/C
	P342 Vn = 100/120 V	GN0010 029	B/C
	P342 Vn = 380/480 V	GN0010 030	B/C
	P343 Vn = 100/120 V	GN0012 009	B/C
	P343 Vn = 380/480 V	GN0012 010	B/C
	P341 Vn = 100/120 V	GN0010 078	J/P
	P341 Vn = 380/480 V	GN0010 079	J/P
	P341 (60TE) Vn = 100/120 V	GN0012 022	J/P
	P341 (60TE) Vn = 380/480 V	GN0012 023	J/P
	P342 Vn = 100/120 V	GN0010 080	J/P
	P342 Vn = 380/480 V	GN0010 081	J/P
	P343 Vn = 100/120 V	GN0012 024	K/M
	P343 Vn = 380/480 V	GN0012 025	K/M
	P344 Vn = 380/480 V	GN0012 026	K/M
	P344 Vn = 380/480 V	GN0012 027	K/M
	P345 Vn = 100/120 V	GN0407 001/2	K/M
	P345 Vn = 380/480 V	GN0407 003/4	K/M
IEC 61850-9-2 LE board	P348	ZN0078 001	M
Measurement board	P391	ZN0066 001	A
Coupling resistor board	P391	ZN0064 001	A

Table 1: PCB part numbers

1.3.2.1 Replacing the main processor board

The main processor board is in the front panel. The other PCBs are in the main case of the relay.

1. Place the front panel with the user interface face-down and remove the six screws from the metallic screen, as shown in Figure 2. Remove the metal plate.
2. Remove the two screws, either side of the rear of the battery compartment recess, that hold the main processor PCB in position.
3. The user interface keypad is connected to the main processor board via a flex-strip ribbon cable. Carefully disconnect the ribbon cable at the PCB-mounted connector as it could easily be damaged by excessive twisting.

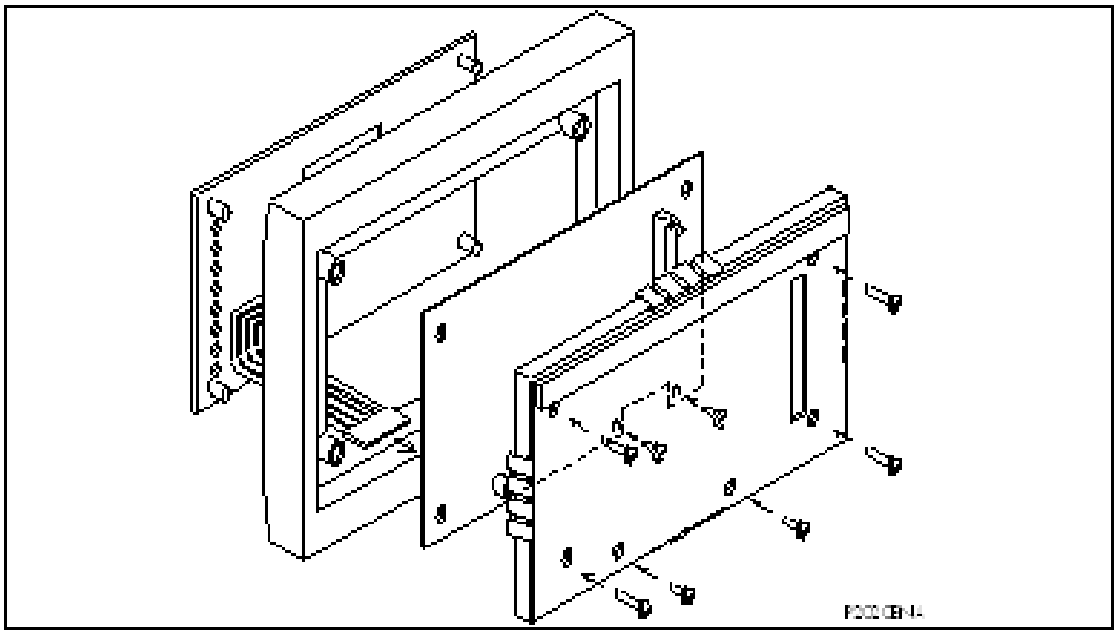


Figure 2: Front panel assembly

4. The front panel can then be re-assembled with a replacement PCB using the reverse procedure. Make sure the ribbon cable is reconnected to the main processor board and all eight screws are re-fitted.
5. Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on size 60TE cases, press at the location of the hinge-assistance T-pieces so that they click back into the front panel molding.

After replacement of the main processor board, all the settings required for the application will need to be re-entered. Therefore, it is useful if an electronic copy of the application-specific settings is available on disk. Although this is not essential, it can reduce the time taken to re-enter the settings and hence the time the protection is out of service.

6. Once the relay has been reassembled after repair, recommission it in accordance with the instructions in the Commissioning chapter, *P34x/EN CM*.

1.3.2.2 Replacement of the IRIG-B/2nd rear communications/ethernet board

Depending on the model number of the relay, the relay may have an IRIG-B board fitted with connections for IRIG-B signals, IEC60870-5-103 (VDEW) communications, both or not be present at all. The relay may also have the 2nd communications board fitted with or without IRIG-B in same position. The relay may also have the Ethernet/Redundant Ethernet communications board fitted with or without IRIG-B in same position.

1. To replace a faulty board, disconnect all IRIG-B and/or IEC60870-5-103 and/or communications connections at the rear of the relay.
2. The board is secured in the case by two screws accessible from the rear of the relay, one at the top and another at the bottom, as shown in Figure 3. Remove these screws carefully as they are not captive in the rear panel of the relay.

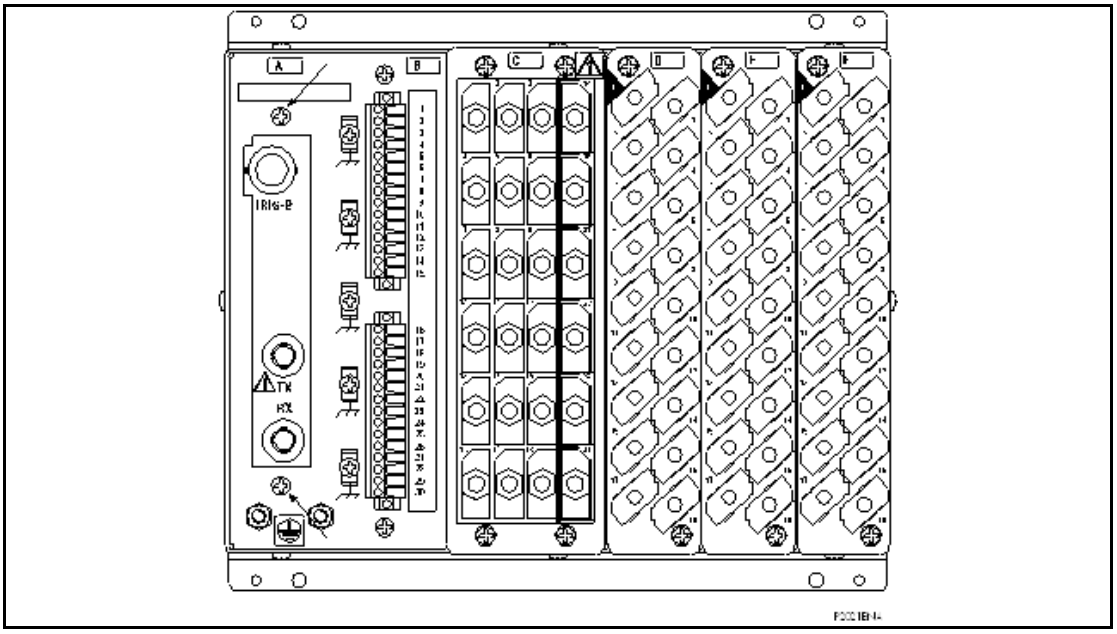


Figure 3: Location of securing screws for IRIG-B board

3. Gently pull the IRIG-B board or 2nd rear communications board or Ethernet board forward and out of the case.

To help identify that the correct board has been removed, Figure 4 illustrates the layout of the IRIG-B board with both IRIG-B and IEC 60870-5-103 options fitted (ZN0007 003). The other versions (ZN0007 001 and ZN0007 002) use the same PCB layout but have less components fitted. Figure 5 shows the 2nd communications board with IRIG-B.

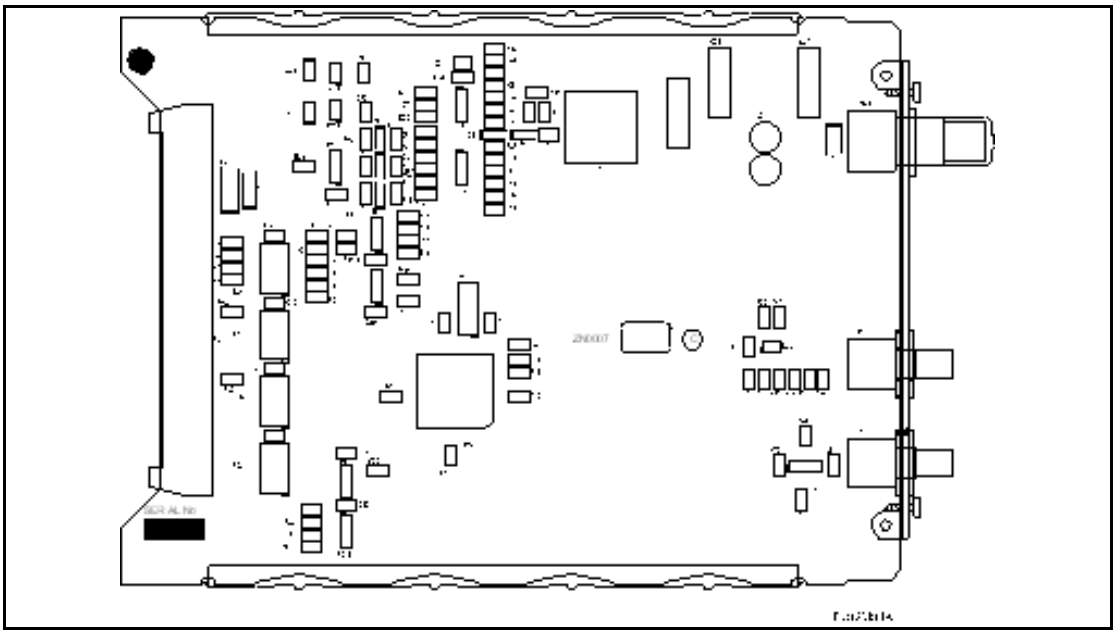


Figure 4: Typical IRIG-B board

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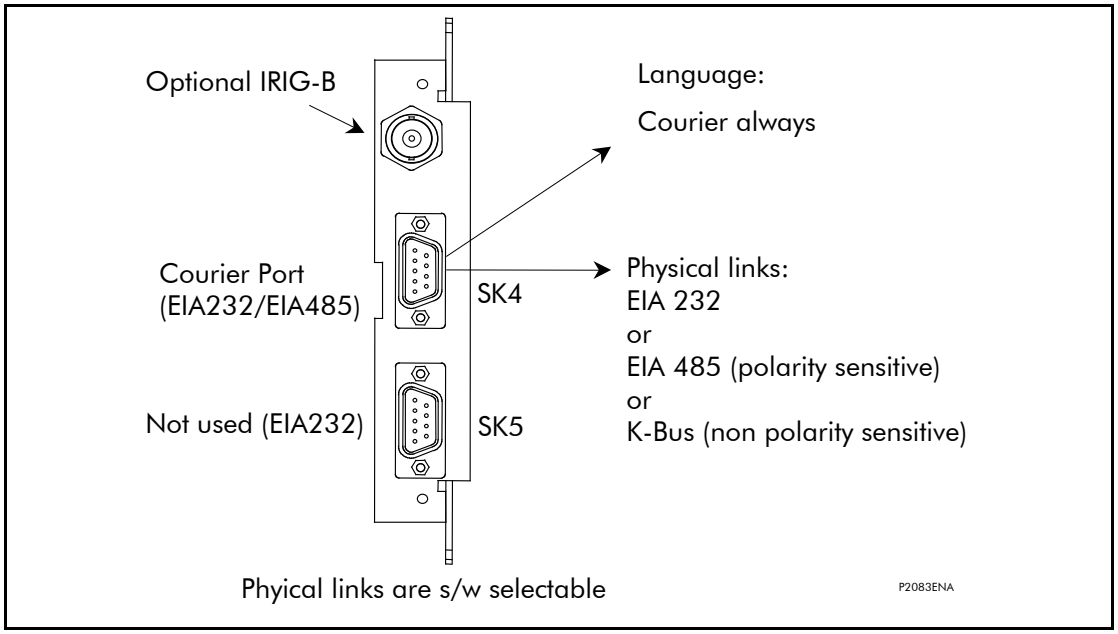


Figure 5: 2nd rear communications board with IRIG-B

4. Before fitting the replacement PCB check that the number on the round label adjacent to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect write the correct slot number on the label.
5. Fit the replacement PCB carefully into the appropriate slot. Make sure it is pushed fully back on to the rear terminal blocks and the securing screws are re-fitted.
6. Reconnect all IRIG-B and/or IEC 60870-5-103 and/or communications connections at the rear of the relay.
7. Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on size 60TE/80TE cases, press at the location of the hinge-assistance T-pieces so that they click back into the front panel molding.
8. Once the relay has been reassembled after repair, recommission it according to the instructions in the Commissioning chapter, *P34x/EN CM*.

1.3.2.3 Replacement of the input module

The input module comprises of two or three boards fastened together. In the P342 relays the input module consists of a transformer board and an input board. The P343/4/5/6 input module has three boards; input, transformer and auxiliary transformer.

1. The module is secured in the case by two screws on its right-hand side, accessible from the front of the relay, as shown in Figure 6. Remove these screws carefully as they are not captive in the front plate of the module.

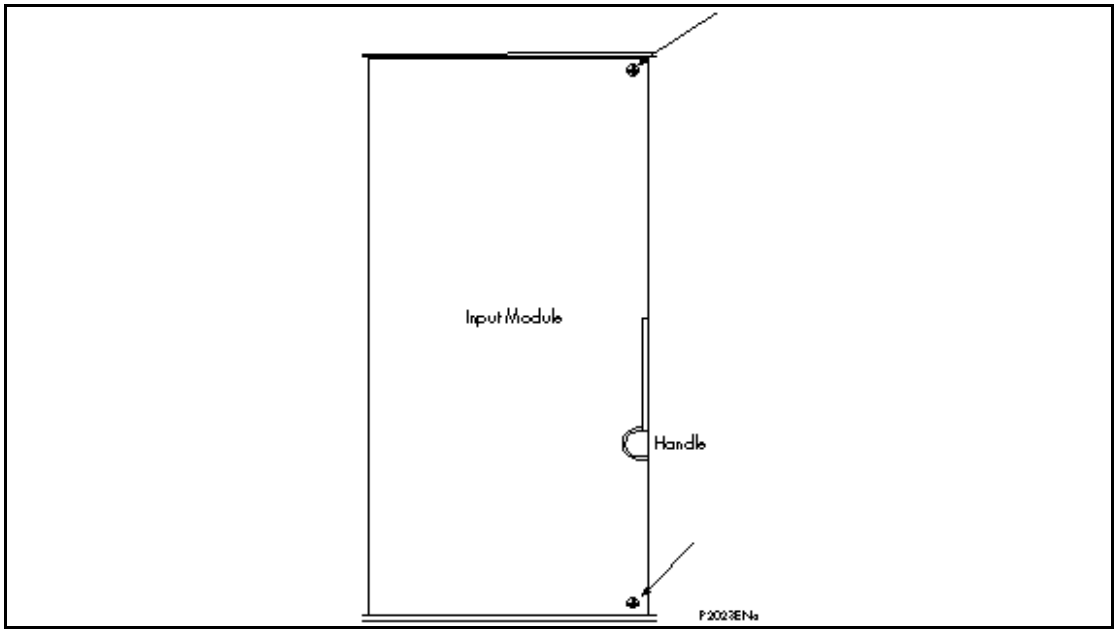


Figure 6: Location of securing screws for input module

2. On the right-hand side of the analog input module in P342 relays there is a small metal tab which brings out a handle. In the P343/4/5/6 relay there is an additional tab on the left hand side. Grasping the handle or handles firmly, pull the module forward, away from the rear terminal blocks. A reasonable amount of force will be required to achieve this due to the friction between the contacts of the terminal blocks; one medium duty and one heavy duty in P341 and P342 relays, one medium duty and two heavy duty in P343/4/5/6 relays.

   Note: Care should be taken when withdrawing the input module as it will suddenly come loose once the friction of the terminal blocks has been overcome. This is particularly important with unmounted relays as the metal case will need to be held firmly whilst the module is withdrawn.

3. Remove the module from the case, taking care as it is heavy because it contains all the relay's input voltage and current transformers.
4. Before fitting the replacement module check that the number on the round label adjacent to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect write the correct slot number on the label.
5. The replacement module can be slotted in using the reverse procedure, ensuring that it is pushed fully back on to the rear terminal blocks. To help confirm that the module has been inserted fully there is a V-shaped cut-out in the bottom plate of the case that should be fully visible. Re-fit the securing screws.

   Note: The transformer and input boards within the module are calibrated together with the calibration data being stored on the input board. Therefore it is recommended that the complete module is replaced to avoid on-site recalibration having to be performed.

6. Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on size 60TE/80TE cases, press at the location of the hinge-assistance T-pieces so that they click back into the front panel molding.
7. Once the relay has been reassembled after repair, it should be recommissioned in accordance with the instructions in the Commissioning chapter, *P34x/EN CM*.

In the P348 the analogue input module is replaced by an IEC 61850-9-2 LE Ethernet communications board providing current and voltage measurements from a merging unit. This board can be replaced in the same way as the other communications boards described in section 1.3.2.2. See Figure 7 for location of IEC 61850-9-2 LE Ethernet interface.

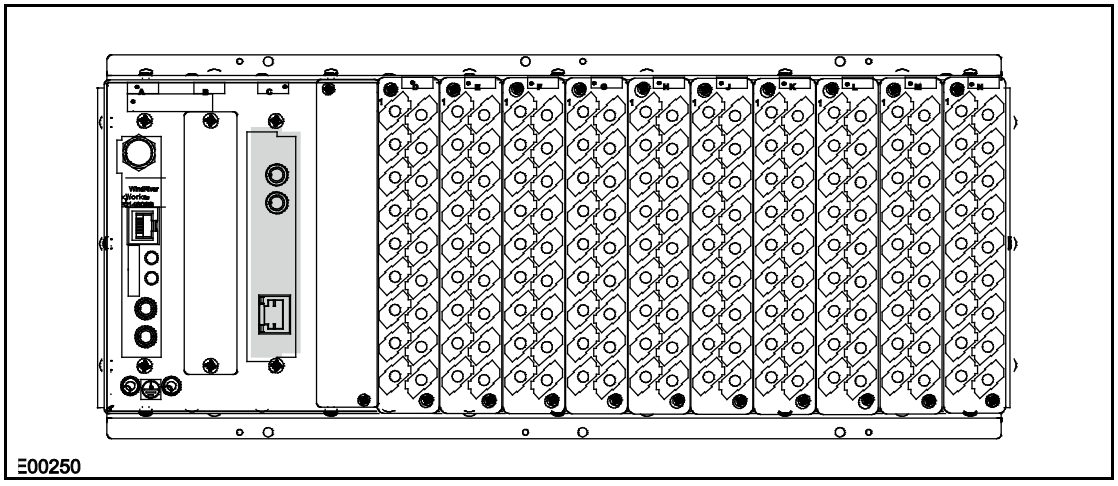


Figure 7: Rear view of IED showing IEC 61850-9-2 LE interface

1.3.2.4 Replacement of the power supply board

Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section/Safety Guide Pxxx-SG-4LM-2 or later issue and the ratings on the equipment's rating label.

The power supply board is fastened to a relay board to form the power supply module and is located on the extreme left-hand side of all generator relays.

1. Pull the power supply module forward, away from the rear terminal blocks and out of the case. A reasonable amount of force will be required to achieve this due to the friction between the contacts of the two medium duty terminal blocks.
2. The two boards are held together with push-fit nylon pillars and can be separated by pulling them apart.

Note: Take care when separating the boards to avoid damaging the inter-board connectors located near the lower edge of the PCBs towards the front of the power supply module.

The power supply board is the one with two large electrolytic capacitors on it that protrude through the other board that forms the power supply module. To help identify that the correct board has been removed, Figure 7 illustrates the layout of the power supply board for all voltage ratings.

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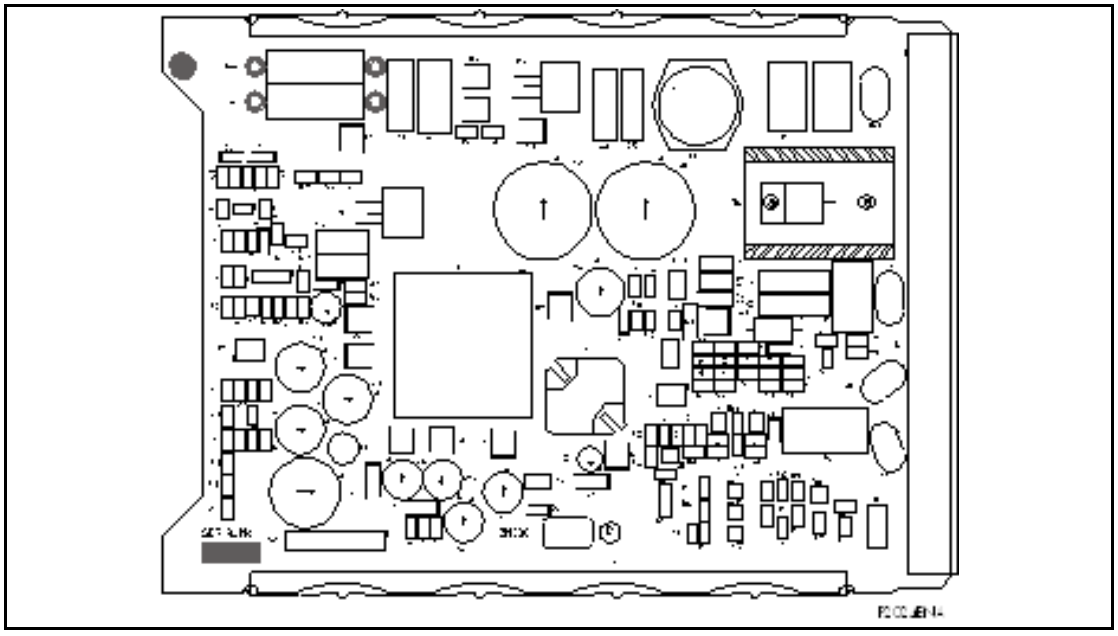


Figure 8: Typical power supply board

3. Before re-assembling the module with a replacement PCB check that the number on the round label adjacent to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect write the correct slot number on the label.
4. Re-assemble the module with a replacement PCB ensuring the inter-board connectors are firmly pushed together. Fit the four push-fit nylon pillars are securely located in their respective holes in each PCB.
5. Slot the power supply module back into the relay case, ensuring that it is pushed fully back on to the rear terminal blocks.
6. Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on size 60TE/80TE cases, press at the location of the hinge-assistance T-pieces so that they click back into the front panel molding.
7. Once the relay has been reassembled after repair, it should be re-commissioned in accordance with the instructions in the Commissioning chapter, *P34x/EN CM*.

1.3.2.5 Replacement of the relay board in the power supply module

1. Remove and replace the relay board in the power supply module as described in 1.3.2.4 above.

The relay board is the one with holes cut in it to allow the transformer and two large electrolytic capacitors of the power supply board to protrude through. To help identify the board see Figure 8.

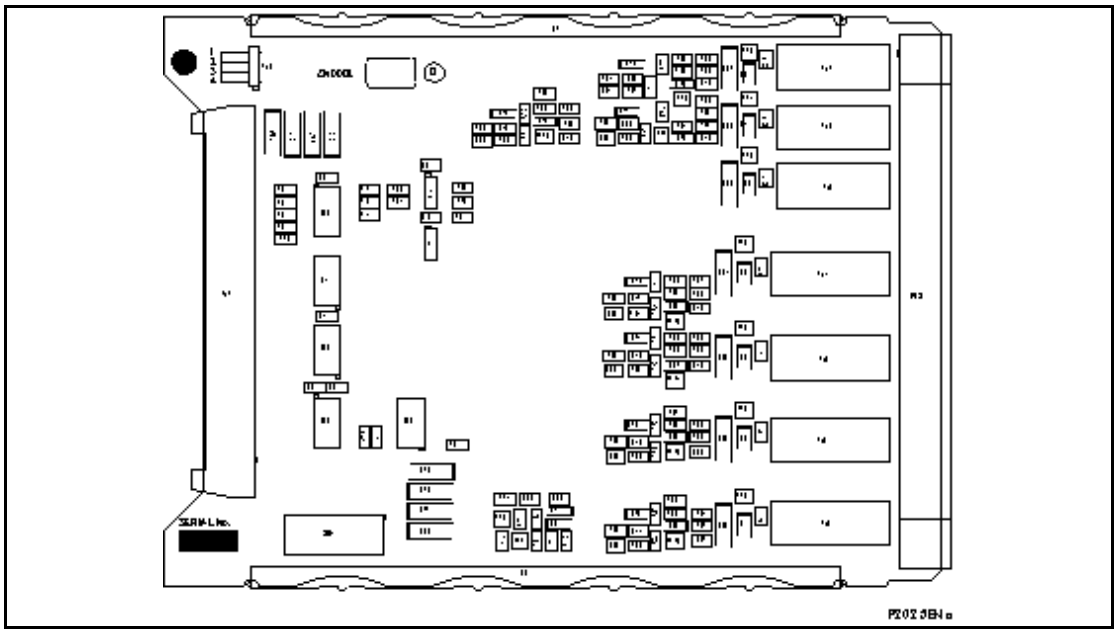


Figure 9: Typical relay board

2. Before re-assembling the module with a replacement relay board check that the number on the round label adjacent to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect write the correct slot number on the label.
3. Ensure the setting of the link (located above IDC connector) on the replacement relay board is the same as the one being replaced before replacing the module in the relay case.
4. Once the relay has been reassembled after repair, recommission it in accordance with the instructions in the Commissioning chapter, *P34x/EN CM*.

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1.3.2.6 Replacement of the opto and separate relay boards (P343/4/5/6/8 only)

The P343/4/5/6/8 generator relay has two additional boards to the P341 and P342. These boards provide extra output relays and optically-isolated inputs to those in the power supply and input modules respectively.

1. To remove either, gently pull the faulty PCB forward and out of the case.
2. If the relay board is being replaced, ensure the setting of the link (located above IDC connector) on the replacement relay board is the same as the one being replaced. To help you identify the correct board has been removed, Figure 8 and Figure 9 illustrate the layout of the relay and opto boards respectively.

If a new board is being added to increase the number of opto inputs or relay outputs check the terminal numbers (B1, B2 for example) of the new opto inputs or relay outputs on wiring connection diagram in the Installation Chapter, *P34x/EN IN*, for the rear slot position B/C/D etc. Then check the final assembly drawings for the correct jumper link position for that slot position so that the relay will correctly recognize the new PCB.

3. Before fitting the replacement PCB check that the number on the round label adjacent to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect write the correct slot number on the label.
4. Carefully slide the replacement board into the appropriate slot, ensuring that it is pushed fully back on to the rear terminal blocks.
5. Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on size 60TE/80TE cases, press at the location of the hinge-assistance T-pieces so that they click back into the front panel molding.

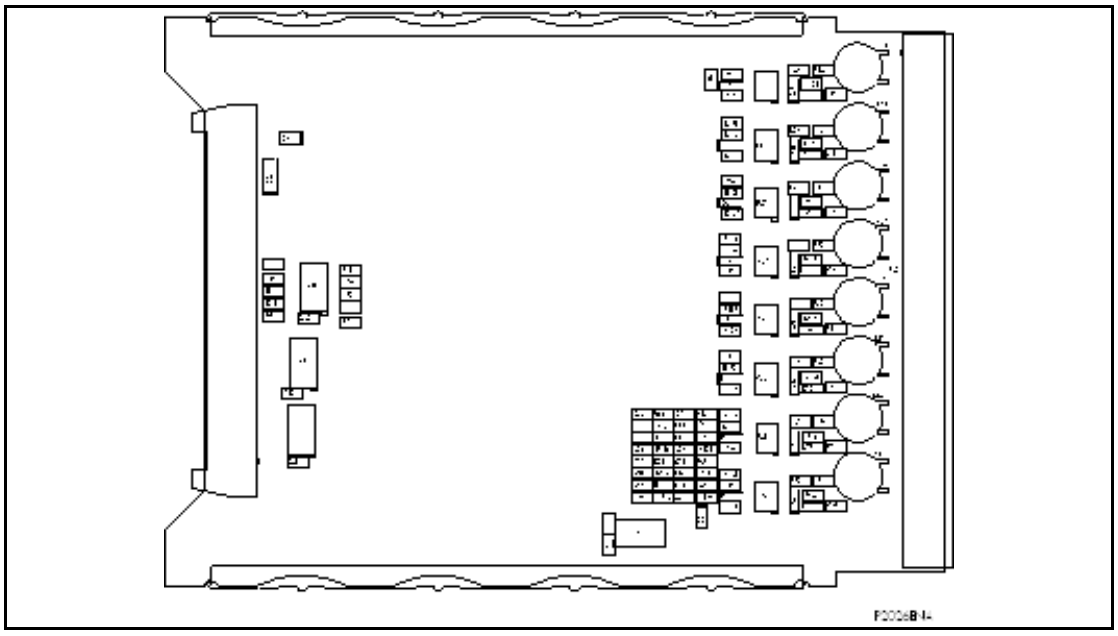


Figure 10: Typical opto board

6. Once the relay has been reassembled after repair, recommission it according to the instructions in the Commissioning chapter, *P34x/EN CM*.

1.3.2.7 Replacement of the RTD input board

All external connections to the RTD board are made using the 15 way light duty I/O connector SL3.5/15/90F. Two such connectors are used for the 10 RTDs.

1. To replace a faulty RTD input board, first remove the two 15-way terminal blocks, each is fastened to its other half by slotted screws above and below the row of terminals, as shown in Figure 10. Remove these screws carefully as they are not captive in the terminal blocks.

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2. Without damaging the RTD wiring, pull the terminal blocks away from their internal halves. It is not necessary to disconnect the RTD screen connections from the spade connectors on the metal rear panel of the relay.

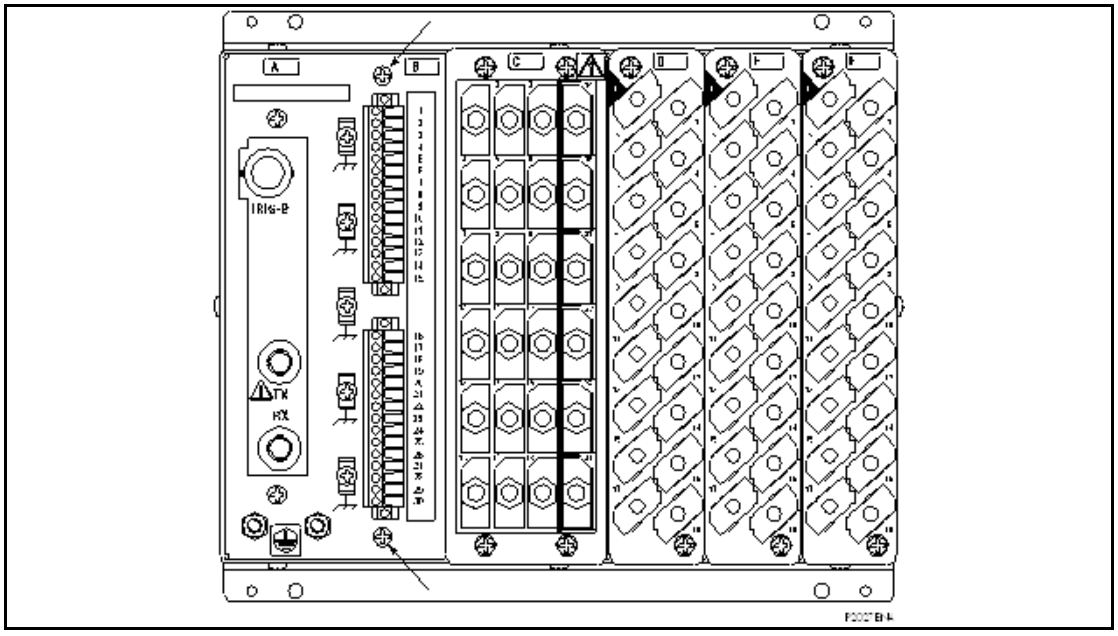


Figure 11: Location of securing screws for RTD/CLIO input board

3. The RTD input board is secured in the case by two screws accessible from the rear of the relay, one at the top and another at the bottom, as shown in Figure 10. Remove these screws carefully as they are not captive in the rear panel of the relay.

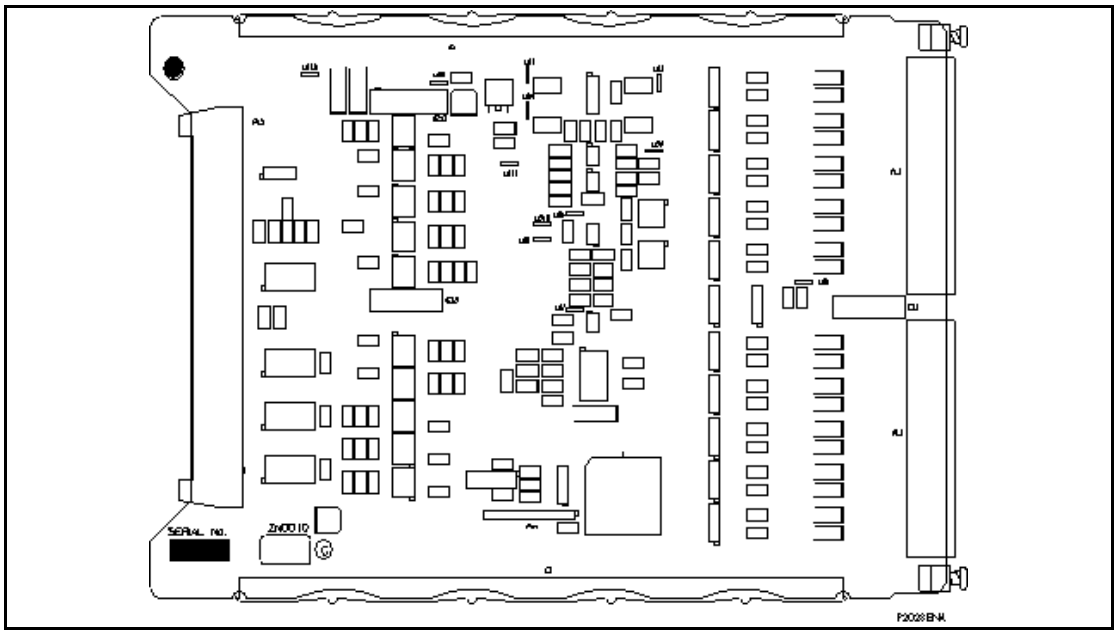


Figure 12: Typical RTD input board

4. Gently pull the faulty RTD input PCB forward and out of the case. To help identify that the correct board has been removed, Figure 10 illustrates the PCB layout.
5. The replacement PCB should be carefully slotted into the appropriate slot, ensuring that it is pushed fully back and the board securing screws are re-fitted.
6. Refit the RTD input terminal blocks, ensuring that they are in the correct location and that their fixing screws are replaced.
7. Once the relay has been reassembled after repair, recommission it according to the instructions in the Commissioning chapter, *P34x/EN CM*.

1.3.2.8 Replacement of the CLIO input board

All external connections to the current loop input output board are made using the same 15 way light duty I/O connector SL3.5/15/90F as used on the RTD board. Two such connectors are used, one for the current loop outputs and one for the current loop inputs.

1. To replace a faulty CLIO board, it is necessary to first remove the two 15-way terminal blocks, each is fastened to its other half by slotted screws above and below the row of terminals, as shown in Figure 11. Remove these screws carefully as they are not captive in the terminal blocks.

   Note: The CLIO board occupies the same slot B as the RTD board in the 60TE case but uses a separate slot C in the 80TE case.

2. Without damaging the CLIO wiring, pull the terminal blocks away from their internal halves. It is not necessary to disconnect the CLIO screen connections from the spade connectors on the metal rear panel of the relay.
3. The CLIO board is secured in the case by two screws accessible from the rear of the relay, one at the top and another at the bottom, as shown in Figure 11. Remove these screws carefully as they are not captive in the rear panel of the relay.
4. Gently pull the faulty CLIO PCB forward and out of the case.
5. The replacement PCB should be carefully slotted into the appropriate slot, ensuring that it is pushed fully back and the board securing screws are re-fitted.
6. Refit the CLIO terminal blocks, ensuring that they are in the correct location and that their fixing screws are replaced.
7. Once the relay has been reassembled after repair, recommission it according to the instructions in the Commissioning chapter, *P34x/EN CM*.

1.4 Re-calibration

Re-calibration is not required when a PCB is replaced unless it happens to be one of the boards in the input module, the replacement of either directly affect the calibration.

Although it is possible to carry out re-calibration on site, this requires test equipment with suitable accuracy and a special calibration program to run on a PC. It is therefore recommended that the work is carried out by the manufacturer, or entrusted to an approved service centre.

1.5 Changing the battery

Each relay has a battery to maintain status data and the correct time when the auxiliary supply voltage fails. The data maintained includes event, fault and disturbance records and the thermal state at the time of failure.

This battery will periodically need changing, although an alarm will be given as part of the relay's continuous self-monitoring in the event of a low battery condition.

If the battery-backed facilities are not required to be maintained during an interruption of the auxiliary supply, the steps below can be followed to remove the battery, but do not replace with a new battery.



Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section/Safety Guide Pxxx-SG-4LM-2 or later issue and the ratings on the equipment's rating label.

1.5.1 Instructions for replacing the battery

1. Open the bottom access cover on the front of the relay.
2. Gently extract the battery from its socket. If necessary, use a small insulated screwdriver to prize the battery free.
3. Ensure that the metal terminals in the battery socket are free from corrosion, grease and dust.



The replacement battery should be removed from its packaging and placed into the battery holder, taking care to ensure that the polarity markings on the battery agree with those adjacent to the socket.

Note: Only use a type ½AA Lithium battery with a nominal voltage of 3.6 V and safety approvals such as UL (Underwriters Laboratory), CSA (Canadian Standards Association) or VDE (Vereinigung Deutscher Elektrizitätswerke).

4. Ensure that the battery is securely held in its socket and that the battery terminals are making good contact with the metal terminals of the socket.
5. Close the bottom access cover.

1.5.2 Post modification tests

To ensure that the replacement battery will maintain the time and status data if the auxiliary supply fails, check cell [0806: **DATE and TIME**, Battery Status] reads **Healthy**.

If you need further confirmation that the replacement battery is installed correctly, perform the commissioning test described in section 5.2.3 of *P34x/EN CM*.

1.5.3 Battery disposal

Dispose the removed battery according to the disposal procedure for Lithium batteries in the country in which the relay is installed.

1.6 Cleaning

Before cleaning the relay ensure that all ac and dc supplies, current transformer and voltage transformer connections are isolated to prevent any chance of an electric shock while cleaning.



Before cleaning the relay ensure that all ac and dc supplies, current transformer and voltage transformer connections are isolated to prevent any chance of an electric shock whilst cleaning.

Only clean the equipment with a lint-free cloth dampened with clean water. Do not use detergents, solvents or abrasive cleaners as they may damage the relay's surface and leave a conductive residue.

1.7 P391 method of repair

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The user shall be familiar with all safety statements listed in section 6.3.5 of the commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

Should the P391 Generator Rotor Earth Fault Unit (REFU) develop a fault whilst in service it will be necessary to replace either the entire REFU or an internal Printed Circuit Board (PCB), dependant on working conditions of the installation environment.

The preferred method is to replace the complete REFU as it ensures that the internal circuitry is protected against electrostatic discharge and physical damage at all times. This also overcomes the possibility of fitting an incompatible replacement PCB. It may be necessary to replace a PCB where it is difficult to replace a complete REFU due to limited access or rigidity of the scheme wiring.

Replacing PCBs can reduce transport costs but requires clean, dry onsite conditions and requires a highly skilled repair engineer. The warranty will be invalidated if the repair is not performed by an General Electric approved service centre. Repairing faulty PCBs to component level shall not be attempted as the use of unapproved replacement components may compromise equipment safety or degrade performance. Attempting to repair a faulty PCB will void the warranty and may cause subsequent damage if incorrectly undertaken.

Under certain equipment fault conditions, the P391 watchdog contacts will change state and an alarm condition will be flagged.

1.7.1 Replacing a complete P391 REFU.




The user shall be familiar with all safety statements listed in section 6.3.5 of the commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.

1. Remove all connections to the P391 REFU.
2. Remove the screws used to fasten the REFU to the panel, rack or wall, paying special attention to support the unit as it becomes free from its mounting.
3. To reinstall the repaired or replacement REFU follow the above instructions in reverse, ensuring that each connection is made to the correct terminal and that the protective earth is replaced.
4. Once reinstallation is complete the REFU should be recommissioned using the P391 instructions in the Commissioning chapter, *P34x/EN CM*.

1.7.2 Replacing P391 internal PCBs




The user shall be familiar with all safety statements listed in section 6.3.5 of the commissioning manual and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.



The internal circuitry of the P391 is not protected against electrostatic discharges (ESD) when the front panel is removed. ESD precautions and a clean working environment should be maintained.

See section 2 of the Installation chapter, *P34x/EN IN*, 'Handling of Electronic Equipment' for information on electrostatic discharge precautions.

The P391 REFU comprises three internal PCBs; one PSU/Measurement PCB and two identical resistor coupling PCBs. Each PCB plugs directly into a socket mounted inside the metal case. (Each socket corresponds directly to a terminal block on the outside of the case). Polarizing guides on the PCB connector and metal guides inside the case ensure the PCB can be correctly connected in only one orientation.

Replacing printed circuit boards and other internal components of the REFU must be undertaken only by Service Centers approved by General Electric. Failure to obtain the authorization of General Electric After Sales Engineers prior to commencing work may invalidate the product warranty.

General Electric Support teams are available world-wide, and it is strongly recommended that any repairs be entrusted to those trained personnel.

1. To replace any of the REFU's PCBs it will be necessary to first remove the front panel. The P391 has twelve size 4 pan head self tapping screws fastening the front panel to the case. Undo and remove these screws.
2. When the screws have been removed, the complete front panel can be pulled forward and separated from the metal case.

The PCBs within the REFU are now accessible. The P391 final assembly drawings in the Installation chapter, *P34x/EN IN* illustrate the PCB locations for the P391.

Note: Each internal slot is labeled inside the casework with a reference number. This reference number will correspond to a label attached to the PCB inserted.

Note: To ensure compatibility, always replace a faulty PCB with one of an identical reference number. Table 2 lists PCB reference numbers.

PCB/Slot reference number	Description	Qty
ZN0066001	PSU and Measurement PCB	1
ZN0064001	72 kΩ Coupling Resistor PCB	2

Table 2: PCB reference lists

3. Gently pull on the PCB to be replaced taking care not to damage any components with excess pressure or rough handling.
4. The replacement PCB should be carefully slid into the appropriate slot, ensuring that it is mates securely into the rear socket.
5. Refit the front panel using the reverse procedure to that given in section 1.7.1.
6. Once the REFU has been reassembled after repair, it should be re-commissioned in accordance with the instructions in Commissioning chapter, *P34x/EN CM*.

1.7.3 Cleaning



Isolate all voltage inputs, including the high voltage DC rotor winding supply before cleaning the P391 REFU

The equipment may be cleaned using a lint-free cloth dampened with clean water. The use of detergents, solvents or abrasive cleaners is not recommended as they may damage the REFU's surface and leave a conductive residue.

TROUBLESHOOTING

Hardware Suffix: **P (P342) M (P343/4/5/6/8)**
A (P391)

Software Version: **38 (P342/3/4/5/6)**
37 (P348)

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1 INTRODUCTION



Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety Section, the Technical Data chapter and the ratings on the equipment's rating label

The purpose of this chapter of the technical manual is to allow an error condition on the relay to be identified so that appropriate corrective action can be taken.

If the relay develops a fault, usually it is possible to identify which relay module needs attention. The Maintenance chapter (*P34x/EN MT*) advises on the recommended method of repair where faulty modules need replacing. It is not possible to perform an on-site repair to a faulted module.

If a faulty relay or module is being returned to the manufacturer or one of their approved service centers, include a completed copy of the Repair or Modification Return Authorization (RMA) Form.

2 INITIAL PROBLEM IDENTIFICATION

Use Table 1 below to find the description that best matches the problem experienced, then consult the section referenced to perform a more detailed analysis of the problem.

Symptom	Refer to
Relay fails to power up	Section 4
Relay powers up - but indicates error and halts during power-up sequence	Section 5
Relay Powers up but Out of Service LED is illuminated	Section 6
Error during normal operation	Section 7
Mal-operation of the relay during testing	Section 8

Table 1: Problem identification

3 POWER UP ERRORS

If the relay does not appear to power up, use the procedure in Table 2 to determine whether the fault is in the external wiring, auxiliary fuse, power supply module of the relay or the relay front panel.

Test	Check	Action
1	Measure auxiliary voltage on terminals 1 and 2. Verify the voltage level and polarity against rating the label on front. Terminal 1 is –dc, 2 is +dc	If the auxiliary voltage is present and correct, go to test 2. Otherwise check the wiring and fuses in the auxiliary supply.
2	Do LEDs/and LCD backlight illuminate on power-up, also check the N/O watchdog contact for closing.	If they illuminate or the contact closes and no error code is displayed then error is probably in the main processor board (front panel). If they do not illuminate and the contact does not close then proceed to test 3.

Table 2: Failure of relay to power up

4 ERROR MESSAGE/CODE ON POWER-UP

During the power-up sequence of the relay self-testing is performed as indicated by the messages displayed on the LCD. If an error is detected by the relay during these self-tests then an error message will be displayed and the power-up sequence will be halted. If the error occurs when the relay application software is executing then a maintenance record will be created and the relay will reboot.

Test	Check	Action
1	Is an error message or code permanently displayed during power up?	If the relay locks up and displays an error code permanently, go to test 2. If the relay prompts for user input, go to test 4. If the relay re-boots automatically, go to test 5.
2	Record displayed error, then remove and re-apply relay auxiliary supply.	Record whether the same error code is displayed when the relay is rebooted. If no error code is displayed then contact the local service center stating the error code and relay information. If the same code is displayed proceed to test 3.
3	Error code Identification The following text messages (in English) are displayed if a fundamental problem is detected preventing the system from booting: Bus Fail – address lines SRAM Fail – data lines FLASH Fail format error FLASH Fail checksum Code Verify Fail The following hex error codes relate to errors detected in specific relay modules:	These messages indicate that a problem has been detected on the relay's main processor board in the front panel.
	0c140005/0c0d0000	Input Module (inc. Opto-isolated inputs)
	0c140006/0c0e0000	Output Relay Cards
	The last 4 digits provide details on the actual error.	Other error codes relate to problems within the main processor board hardware or software. It will be necessary to contact General Electric with details of the problem for a full analysis.
4	The relay displays a message for corrupt settings and prompts for restoration of defaults to the affected settings.	The power up tests have detected corrupted relay settings. Restore the default settings to allow the power-up to complete, then re-apply the application-specific settings.
5	The relay resets when the power up is complete. A record is error code is displayed.	Error 0x0E080000, programmable scheme logic error due to excessive execution time. If relay powers up successfully, check programmable logic for feedback paths. Other error codes will relate to software errors on the main processor board, contact General Electric.

Table 3: Power-up self-test error

5 OUT OF SERVICE LED ILLUMINATED ON POWER UP

Test	Check	Action	
1	Using the relay menu confirm whether the Commission Test/Test Mode setting is Enabled. If it is not enabled, go to test 2.	If the setting is Enabled then disable the test mode and make sure the Out of Service LED is OFF.	
2	Select View Records, then view the last maintenance record from the menu.	Check for H/W Verify Fail this indicates a discrepancy between the relay model number and the hardware; examine the "Maint. Data", this indicates the causes of the failure using bit fields: Bit Meaning	
		0	The application type field in the model number does not match the software ID
		1	The application field in the model number does not match the software ID
		2	The variant 1 field in the model number does not match the software ID
		3	The variant 2 field in the model number does not match the software ID
		4	The protocol field in the model number does not match the software ID
		5	The language field in the model number does not match the software ID
		6	The VT type field in the model number is incorrect (110 V VTs fitted)
		7	The VT type field in the model number is incorrect (440 V VTs fitted)
		8	The VT type field in the model number is incorrect (no VTs fitted)

Table 4: Out of service LED illuminated

6 ERROR CODE DURING OPERATION

The relay performs continuous self-checking. If the relay detects an error it displays an error message, logs a maintenance record and after a 1.6 second delay the relay resets. A permanent problem (for example due to a hardware fault) is usually detected in the power up sequence, then the relay displays an error code and halts. If the problem was transient, the relay reboots correctly and continues operation. By examining the maintenance record logged, the nature of the detected fault can be determined.

There is also a case where a maintenance record will be logged due to a detected error where the relay will not reset. This is detection of a failure of the lithium battery, in this case the failure is indicated by an alarm message, however the relay will continue to operate.

To prevent the relay from issuing an alarm when there is a battery failure, select Date and Time then Battery Alarm then Disabled. The relay can then be used without a battery and no battery alarm message appears.

In the case of the RTD board failure, an alarm "RTD board fail" message is displayed, the RTD protection is disabled, but the operation of the rest of the relay functionality is unaffected.

7 MAL-OPERATION OF THE RELAY DURING TESTING

7.1 Failure of output contacts

An apparent failure of the relay output contacts can be caused by the relay configuration. Perform the following tests to identify the real cause of the failure. The relay self-tests verify that the coil of the contact has been energized. An error is displayed if there is a fault in the output relay board.

Test	Check	Action
1	Is the Out of Service LED illuminated?	If this LED is ON, the relay may be in test mode or the protection has been disabled due to a hardware verify error (see Table 4).
2	Examine the Contact status in the Commissioning section of the menu.	If the relevant bits of the contact status are operated then proceed to test 4, if not proceed to test 3.
3	Verify by examination of the fault record or by using the test port whether the protection element is operating correctly.	If the protection element does not operate verify whether the test is being correctly applied. If the protection element does operate then it will be necessary to check the programmable logic, to ensure that the mapping of the protection element to the contacts is correct.
4	Using the Commissioning/Test mode function apply a test pattern to the relevant relay output contacts and verify whether they operate (note the correct external connection diagram should be consulted). A continuity tester can be used at the rear of the relay for this purpose.	If the output relay does operate then the problem must be in the external wiring to the relay. If the output relay does not operate this could indicate a failure of the output relay contacts (note that the self-tests verify that the relay coil is being energized). Ensure that the closed resistance is not too high for the continuity tester to detect.

Table 5: Failure of output contacts

7.2 Failure of opto-isolated inputs

The opto-isolated inputs are mapped onto the relay internal signals using the programmable scheme logic. If an input does not appear to be recognized by the relay scheme logic, use the Commission Tests/Opto Status menu option to check whether the problem is in the opto-isolated input or the mapping of its signal to the scheme logic functions. If the opto-isolated input does appear to be read correctly, examine its mapping in the programmable logic.

If the relay does not correctly read the opto-isolated input state, test the applied signal. Verify the connections to the opto-isolated input using the correct wiring diagram and the nominal voltage settings in the Opto Config. menu. In the Opto Config. menu select the nominal battery voltage for all opto inputs by selecting one of the five standard ratings in the Global Nominal V settings. Select Custom to set each opto input individually to a nominal voltage. Using a voltmeter, verify that voltage greater than the minimum pick-up level is present on the terminals of the opto-islated input in the energized state (see chapter *P34x/EN TD* for opto pick-up levels). If the signal is correctly applied to the relay, the failure may be on the input card. Depending on which opto-isolated input has failed, the complete analog input module or a separate opto board may need to be replaced. The board in the analog input module cannot be individually replaced without recalibrating the relay.

7.3 Incorrect analog signals

The measurements can be configured in primary or secondary to assist. If the analog quantities measured by the relay do not seem correct, use the measurement function of the relay to determine the type of problem. Compare the measured values displayed by the relay with the actual magnitudes at the relay terminals. Check the correct terminals are used (in particular the dual rated CT inputs) and check the CT and VT ratios set on the relay are correct. Use the correct 120 degree displacement of the phase measurements to confirm the inputs are correctly connected.

7.4 PSL editor troubleshooting

A failure to open a connection could be due to one or more of the following:

- The relay address is not valid (note: this address is always 1 for the front port).
- Password in not valid
- Communication Set-up - COM port, Baud rate, or Framing - is not correct
- Transaction values are not suitable for the relay and/or the type of connection
- Modem configuration is not valid. Changes may be necessary when using a modem
- The connection cable is not wired correctly or broken. See S1 Studio connection configurations
- The option switches on any KITZ101/102 this is in use may be incorrectly set

7.4.1 Diagram reconstruction after recover from relay

Although a scheme can be extracted from a relay, the facility is provided to recover a scheme if the original file is unobtainable.

A recovered scheme is logically correct but much of the original graphical information is lost. Many signals will be drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B.

Any annotation added to the original diagram (titles, notes, etc.) are lost.

Sometimes a gate type may not be what was expected. For example, a 1-input AND gate in the original scheme will appear as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 will also appear as OR gates.

7.4.2 PSL version check

The PSL is saved with a version reference, time stamp and CRC check. This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

8 REPAIR AND MODIFICATION PROCEDURE

Please follow these 5 steps to return an Automation product to us:

1. Contact us at https://www.gegridsolutions.com/contact to get a copy of the Repair and Modification Authorization Form (RMA)
2. Fill in the RMA form

Fill in only the white part of the form.

Please ensure that all fields marked (M) are completed such as:

- Equipment model
- Model No. and Serial No.
- Description of failure or modification required (please be specific)
- Value for customs (in case the product requires export)
- Delivery and invoice addresses
- Contact details

3. Send the RMA form to your local contact
4. Receive from local service contact, the information required to ship the product

Your local service contact will provide you with all the information:

- Pricing details
- RMA number
- Repair center address

If required, an acceptance of the quote must be delivered before going to next stage.

5. Send the product to the repair center

- Address the shipment to the repair center specified by your local contact
- Ensure all items are protected by appropriate packaging: anti-static bag and foam protection
- Ensure a copy of the import invoice is attached with the unit being returned
- Ensure a copy of the RMA form is attached with the unit being returned
- E-mail or fax a copy of the import invoice and airway bill document to your local contact

SCADA COMMUNICATIONS

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 INTRODUCTION

This chapter describes the remote interfaces of the MiCOM relay in enough detail to allow integration in a substation communication network. As has been outlined in earlier chapters, the relay supports a choice of one of five protocols through the rear communication interface, selected using the model number when ordering. This is in addition to the front serial interface and second rear communications port, which supports the Courier protocol only.

The rear EIA(RS)485 interface is isolated and is suitable for permanent connection whichever protocol is selected. The advantage of this type of connection is that up to 32 relays can be 'daisy chained' together using a simple twisted pair electrical connection. The rear interface can also be Ethernet.

For each of the protocol options, the supported functions and commands are listed with the database definition. The operation of standard procedures such as extraction of event, fault and disturbance records, or setting changes is also be described.

The descriptions in this chapter do not aim to fully describe the protocol in detail. Refer to the relevant documentation protocol for this information. This chapter serves to describe the specific implementation of the protocol in the relay.

2 REAR PORT INFORMATION AND CONNECTION ADVICE – EIA(RS)485 PROTOCOLS

2.1 Rear communication port EIA(RS)485 interface

The rear EIA(RS)485 communication port is provided by a 3-terminal screw connector located on the back of the relay. See chapter P34x/EN IN for details of the connection terminals. The rear port provides K-Bus/EIA(RS)485 serial data communication and is intended for use with a permanently wired connection to a remote control center. Of the three connections, two are for the signal connection, and the other is for the earth shield of the cable. When the K-Bus option is selected for the rear port, the two signal connections are not polarity conscious, however for MODBUS, IEC 60870-5-103 and DNP3.0 care must be taken to observe the correct polarity.

The protocol provided by the relay is indicated in the relay menu in the **Communications** column. Using the keypad and LCD, firstly check that the **Comms. settings** cell in the **Configuration** column is set to **Visible**, then move to the 'Communications' column. The first cell down the column shows the communication protocol being used by the rear port.

2.2 EIA(RS)485 bus

The EIA(RS)485 two-wire connection provides a half-duplex fully isolated serial connection to the product. The connection is polarized and while the product's connection diagrams show the polarization of the connection terminals, there is no agreed definition of which terminal is which. If the master is unable to communicate with the product, and the communication parameters match, make sure the two-wire connection is reversed.

EIA(RS)485 provides the capability to connect multiple devices to the same two-wire bus. MODBUS is a master-slave protocol, so one device will be the master, and the remaining devices are slaves. It is not possible to connect two masters to the same bus, unless they negotiate bus access.

2.2.1 Bus termination

The EIA(RS)485 bus must have 120 Ω (Ohm) ½ Watt terminating resistors fitted at either end across the signal wires - see Figure 1. Some devices may be able to provide the bus terminating resistors by different connection or configuration arrangements, in which case separate external components are not needed. However, this product does not provide such a facility, so if it is located at the bus terminus an external termination resistor is needed.

2.2.2 Bus connections & topologies

The EIA(RS)485 standard requires that each device be directly connected to the physical cable that is the communications bus. Stubs and tees are expressly forbidden, as are star topologies. Loop bus topologies are not part of the EIA(RS)485 standard and are forbidden by it.

Two-core screened cable is recommended. The specification of the cable will be dependent on the application, although a multi-strand 0.5 mm^2 per core is normally adequate. Total cable length must not exceed 1000 m. The screen must be continuous and connected at one end, normally at the master connection point; it is important to avoid circulating currents, especially when the cable runs between buildings, for both safety and noise reasons.

This product does not provide a signal ground connection. If the bus cable has a signal ground connection, it must be ignored. However, the signal ground must have continuity for the benefit of other devices connected to the bus. For both safety and noise reasons, the signal ground must never be connected to the cable's screen or to the product's chassis.

2.2.3 Biasing

It may also be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to switch from receive mode to transmit mode. This may be because the master purposefully waits in receive mode, or even in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequentially not responding. Symptoms of this are poor response times (due to retries), increasing message error counters, erratic communications, and even a complete failure to communicate.

Biasing requires that the signal lines be weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean; otherwise noise will be injected.

Note: Some devices may (optionally) be able to provide the bus bias, in which case external components will not be required.

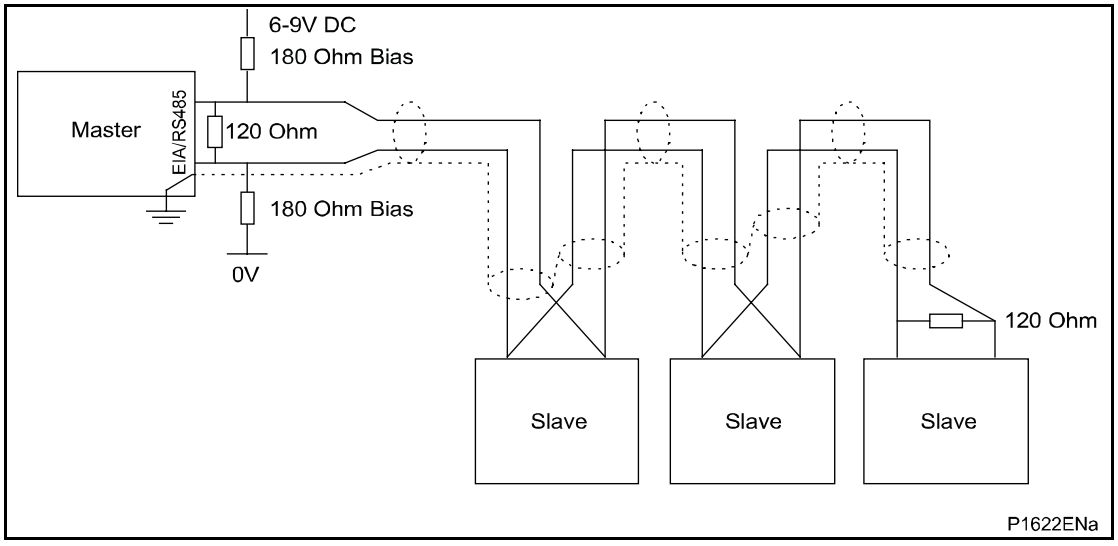


Figure 1: EIA(RS)485 bus connection arrangements

It is possible to use the product's field voltage output (48 V DC) to bias the bus using values of 2.2 kΩ (½W) as bias resistors instead of the 180 Ω resistors shown in the above diagram.

The following warnings apply:

- It is extremely important that the 120 Ω termination resistors are fitted. Failure to do so will result in an excessive bias voltage that may damage the devices connected to the bus.
- As the field voltage is much higher than that required, General Electric cannot assume responsibility for any damage that may occur to a device connected to the network as a result of incorrect application of this voltage.
- Ensure the field voltage is not being used for other purposes, such as powering logic inputs, because noise may be passed to the communication network.

2.2.4 Courier communication

Courier is the communication language developed by General Electric to allow remote interrogation of its range of protection relays. Courier uses a master and slave basis where the slave units contain information in the form of a database, and respond with information from the database when it is requested by a master unit.

The relay is a slave unit that is designed to be used with a Courier master unit such as S1 Agile, S10, PAS&T or a SCADA system. S1 Agile is a Windows compatible software package which is specifically designed for setting changes with the relay.

To use the rear port to communicate with a PC-based master station using Courier, a KITZ K-Bus to EIA(RS)232 protocol converter is required. This unit is available from General Electric. A typical connection arrangement is shown in Figure 2. For more detailed information on other possible connection arrangements refer to the manual for the Courier master station software and the manual for the KITZ protocol converter. Each spur of the K-Bus twisted pair wiring can be up to 1000 m in length and have up to 32 relays connected to it.

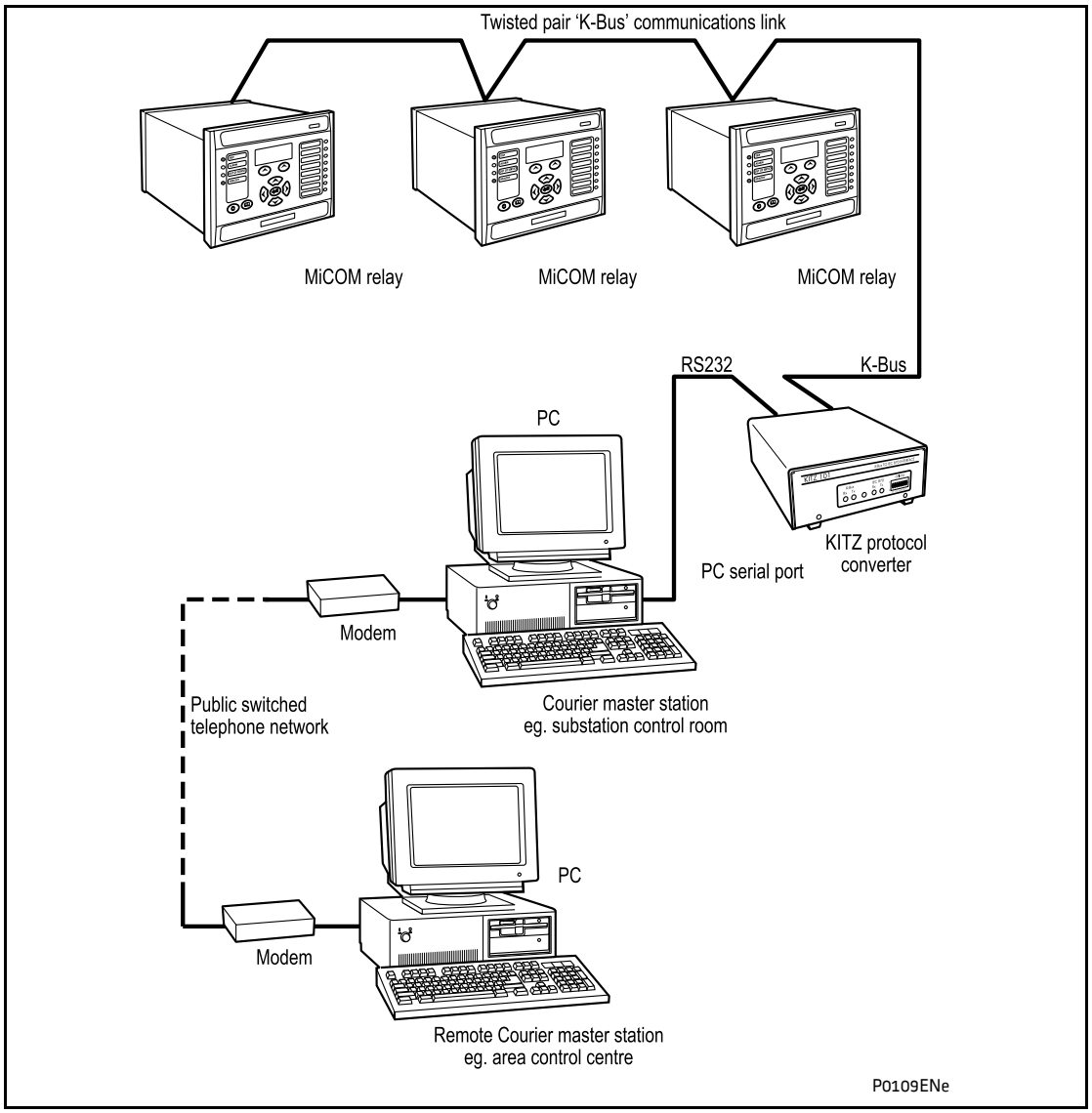


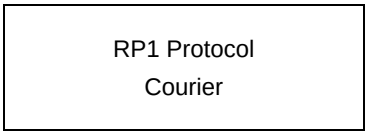
Figure 2: Remote communication connection arrangements

Once the physical connection is made to the relay, configure the relay's communication settings using the keypad and LCD user interface.

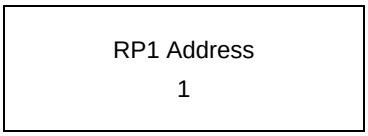
In the relay menu, select the **Configuration** column, then check the **Comms. settings** cell is set to **Visible**.

Select the **Communications** column. Only two settings apply to the rear port using Courier, the relay's address and the inactivity timer. Synchronous communication is used at a fixed baud rate of 64 kbits/s.

Move down the **Communications** column from the column heading to the first cell down which indicates the communication protocol:

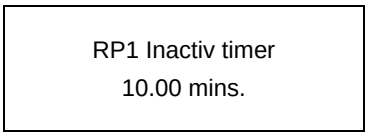


The next cell down the column controls the address of the relay:



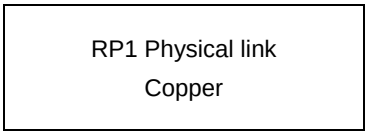
Since up to 32 relays can be connected to one K-Bus spur, as indicated in Figure 2, each relay must have a unique address so that messages from the master control station are accepted by one relay only. Courier uses an integer number between 0 and 254 for the relay address that is set with this cell. It is important that no two relays have the same Courier address. The Courier address is then used by the master station to communicate with the relay.

The next cell down controls the inactivity timer:



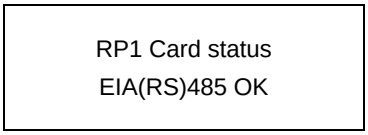
The inactivity timer controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

The next cell down the column controls the physical media used for the communication:

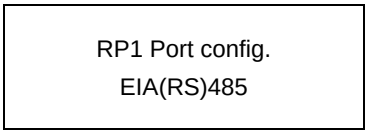


The default setting is to select the copper electrical EIA(RS)485 connection. If the optional fiber optic connectors are fitted to the relay, then this setting can be changed to 'Fiber optic'. This cell is also invisible if second rear comms. port is fitted as it is mutually exclusive with the fiber optic connectors.

As an alternative to running Courier over K-Bus, Courier over EIA(RS)485 may be selected. The next cell down indicates the status of the hardware, e.g.:

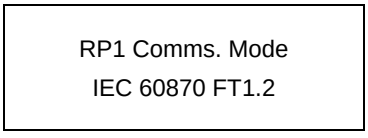


The next cell allows for selection of the port configuration:



The port can be configured for EIA(RS)485 or K-Bus.

In the case of EIA(RS)485 the next cell selects the communication mode:



The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.

In the case of EIA(RS)485 the next cell down controls the baud rate. For K-Bus the baud rate is fixed at 64kbit/second between the relay and the KITZ interface at the end of the relay spur.

RP1 Baud rate
19200

Courier communications is asynchronous. Three baud rates are supported by the relay, '9600 bits/s', '19200 bits/s' and '38400 bits/s',

If you modify protection and disturbance recorder settings using an on-line editor such as PAS&T, you must confirm them. To do this, from the Configuration column select the Save **changes** cell. Off-line editors such as S1 Agile do not need this action for the setting changes to take effect.

2.2.5 MODBUS communication

MODBUS is a master/slave communication protocol that can be used for network control. In a similar way to Courier, the master device initiates all actions and the slave devices, (the relays), respond to the master by supplying the requested data or by taking the requested action. MODBUS communication is achieved via a twisted pair connection to the rear port and can be used over a distance of 1000 m with up to 32 slave devices.

To use the rear port with MODBUS communication, the relay's communication settings must be configured. To do this use the keypad and LCD user interface. In the relay menu firstly check that the **Comms. settings** cell in the **Configuration** column is set to **Visible**, then move to the 'Communications' column. Four settings apply to the rear port using MODBUS that are described below. Move down the **Communications** column from the column heading to the first cell down that indicates the communication protocol:

RP1 Protocol
MODBUS

The next cell down controls the MODBUS address of the relay:

RP1 MODBUS address
23

Up to 32 relays can be connected to one MODBUS spur, and therefore it is necessary for each relay to have a unique address so that messages from the master control station are accepted by one relay only. MODBUS uses an integer number between 1 and 247 for the relay address. It is important that no two relays have the same MODBUS address. The MODBUS address is then used by the master station to communicate with the relay.

The next cell down controls the inactivity timer:

RP1 Inactiv timer
10.00 mins.

The inactivity timer controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

The next cell down the column controls the baud rate to be used:

RP1 Baud rate
9600 bits/s

MODBUS communication is asynchronous. Three baud rates are supported by the relay, '9600 bits/s', '19200 bits/s' and '38400 bits/s'. It is important that whatever baud rate is selected on the relay is the same as that set on the MODBUS master station.

The next cell down controls the parity format used in the data frames:

RP1 Parity
None

The parity can be set to be one of 'None', 'Odd' or 'Even'. It is important that whatever parity format is selected on the relay is the same as that set on the MODBUS master station.

The next cell down the column controls the physical media used for the communication:

RP1 Physical link
Copper

The default setting is to select the copper electrical EIA(RS)485 connection. If the optional fiber optic connectors are fitted to the relay, then this setting can be changed to 'Fiber optic'. This cell is also invisible if second rear comms. port is fitted as it is mutually exclusive with the fiber optic connectors.

The next cell down controls the format of the Date/Time (software 30 or later):

MODBUS
IEC time standard

The format can be selected to either 'Standard' (as per IEC 60870-5-4 'Binary Time 2a'), the default, or to 'Reverse' for compatibility with the product ranges. For further information see *P34x/EN SC* section 4.16

2.2.6 IEC 60870-5 CS 103 communication

The IEC specification IEC 60870-5-103: Telecontrol Equipment and Systems, Part 5: Transmission Protocols Section 103 defines the use of standards IEC 60870-5-1 to

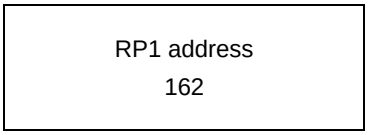
IEC 60870-5-5 to perform communication with protection equipment. The standard configuration for the IEC 60870-5-103 protocol is to use a twisted pair connection over distances up to 1000 m. As an option for IEC 60870-5-103, the rear port can be specified to use a fiber optic connection for direct connection to a master station. The relay operates as a slave in the system, responding to commands from a master station. The method of communication uses standardized messages which are based on the VDEW communication protocol.

To use the rear port with IEC 60870-5-103 communication, configure the relay's communication settings using the keypad and LCD user interface.

1. In the relay menu, select the **Configuration** column, then check that the **Comms. settings** cell in is set to **Visible**.
2. Select the **Communications** column. Four settings apply to the rear port using IEC 60870-5-103 that are described below.
3. Move down the **Communications** column from the column heading to the first cell that indicates the communication protocol:

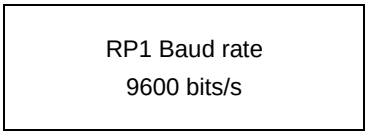
RP1 Protocol
IEC 60870-5-103

4. The next cell down controls the IEC 60870-5-103 address of the relay:



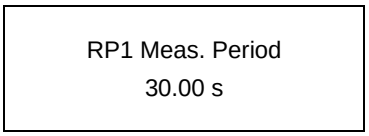
Up to 32 relays can be connected to one IEC 60870-5-103 spur, and therefore it is necessary for each relay to have a unique address so that messages from the master control station are accepted by one relay only. IEC 60870-5-103 uses an integer number between 0 and 254 for the relay address. It is important that no two relays have the same IEC 60870-5-103 address. The IEC 60870-5-103 address is then used by the master station to communicate with the relay.

5. The next cell down the column controls the baud rate to be used:



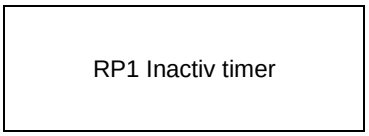
IEC 60870-5-103 communication is asynchronous. Two baud rates are supported by the relay, '9600 bits/s' and '19200 bits/s'. It is important that whatever baud rate is selected on the relay is the same as that set on the IEC 60870-5-103 master station.

6. The next cell down controls the period between IEC 60870-5-103 measurements:

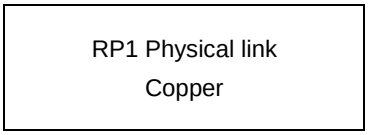


The IEC 60870-5-103 protocol allows the relay to supply measurements at regular intervals. The interval between measurements is controlled by this cell, and can be set between 1 and 60 seconds.

7. The following cell is not currently used but is available for future expansion:

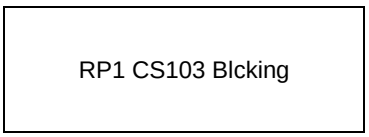


8. The next cell down the column controls the physical media used for the communication:



The default setting is to select the copper electrical EIA(RS)485 connection. If the optional fiber optic connectors are fitted to the relay, then this setting can be changed to 'Fiber optic'. This cell is also invisible if second rear comms. port is fitted as it is mutually exclusive with the fiber optic connectors.

9. The next cell down can be used for monitor or command blocking:



There are three settings associated with this cell; these are:

1. Disabled - No blocking selected.
2. Monitor Blocking - When the monitor blocking DDB Signal is active high, either by energizing an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the relay returns a “Termination of general interrogation” message to the master station.
3. Command Blocking - When the command blocking DDB signal is active high, either by energizing an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the relay returns a “negative acknowledgement of command” message to the master station.

2.2.7 DNP3.0 communication

The DNP3.0 protocol is defined and administered by the DNP User Group. Information about the user group, DNP3.0 in general and protocol specifications can be found on their website: www.dnp.org

The relay operates as a DNP3.0 slave and supports subset level 2 of the protocol plus some of the features from level 3. DNP3.0 communication is achieved using a twisted pair connection to the rear port and can be used over a distance of 1000 m with up to 32 slave devices.

1. To use the rear port with DNP3.0 communication, configure the relay’s communication settings using the keypad and LCD user interface.
2. In the relay menu, select the **Configuration** column, then check that the **Comms. setting** cell in is set to **Visible**.
3. Four settings apply to the rear port using IEC 60870-5-103 that are described below.
4. Move down the **Communications** column from the column heading to the first cell down. This shows the communications protocol.

RP1 Protocol
DNP3.0

5. The next cell controls the DNP3.0 address of the relay:

RP1 Address
232

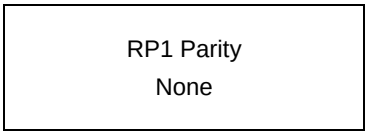
Upto 32 relays can be connected to one DNP3.0 spur, and therefore it is necessary for each relay to have a unique address so that messages from the master control station are accepted by only one relay. DNP3.0 uses a decimal number between 1 and 65519 for the relay address. It is important that no two relays have the same DNP3.0 address. The DNP3.0 address is then used by the master station to communicate with the relay.

6. The next cell down the column controls the baud rate to be used:

RP1 Baud rate
9600 bits/s

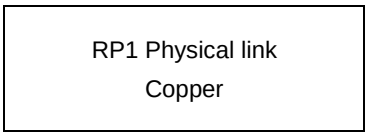
DNP3.0 communication is asynchronous. Six baud rates are supported by the relay ‘1200 bits/s’, ‘2400 bits/s’, ‘4800 bits/s’, ’9600 bits/s’, ‘19200 bits/s’ and ‘38400 bits/s’. It is important that whatever baud rate is selected on the relay is the same as that set on the DNP3.0 master station.

7. The next cell down the column controls the parity format used in the data frames:



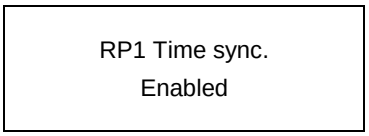
The parity can be set to be one of 'None', 'Odd' or 'Even'. It is important that whatever parity format is selected on the relay is the same as that set on the DNP3.0 master station.

8. The next cell down the column controls the physical media used for the communication:



The default setting is to select the copper electrical EIA(RS)485 connection. If the optional fiber optic connectors are fitted to the relay, then this setting can be changed to 'Fiber optic'. This cell is also invisible if second rear comms. port is fitted as it is mutually exclusive with the fiber optic connectors.

9. The next cell down the column sets the time synchronization request from the master by the relay:

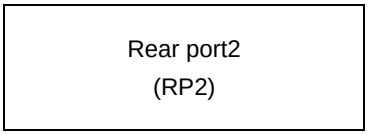


The time sync. can be set to either enabled or disabled. If enabled it allows the DNP3.0 master to synchronize the time.

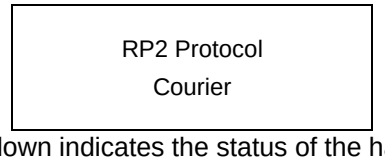
2.3 Second rear communication port

For relays with Courier, MODBUS, IEC 60870-5-103 or DNP3.0 protocol on the first rear communications port there is the hardware option of a second rear communications port, which will run the Courier language. This can be used over one of three physical links: twisted pair K-Bus (non-polarity sensitive), twisted pair EIA(RS)485 (connection polarity sensitive) or EIA(RS)232.

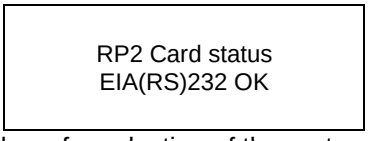
1. Move down the settings until the following sub heading is displayed



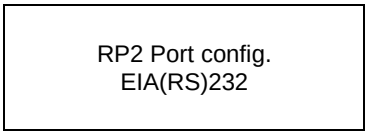
2. The next cell down indicates the language, which is fixed at Courier for RP2:



3. The next cell down indicates the status of the hardware, e.g.:



4. The next cell allows for selection of the port configuration:



The port can be configured for EIA(RS)232, EIA(RS)485 or K-Bus.

5. For EIA(RS)232 and EIA(RS)485, the next cell selects the communication mode. The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.

RP2 Comms. mode
IEC 60870 FT1.2

The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.

6. The next cell down controls the comms. port address:

RP2 Address
255

Since up to 32 relays can be connected to one K-Bus spur, as indicated in Figure 2, it is necessary for each relay to have a unique address so that messages from the master control station are accepted by one relay only. Courier uses an integer number between 0 and 254 for the relay address that is set with this cell. It is important that no two relays have the same Courier address. The Courier address is then used by the master station to communicate with the relay.

7. The next cell down controls the inactivity timer:

RP2 Inactivity timer
15 mins.

The inactivity timer controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

8. For EIA(RS)232 and EIA(RS)485 the next cell down controls the baud rate. For K-Bus the baud rate is fixed at 64 kbit/second between the relay and the KITZ interface at the end of the relay spur.

RP2 Baud rate
19200

Courier communications is asynchronous. Three baud rates are supported by the relay, '9600 bits/s', '19200 bits/s' and '38400 bits/s'.

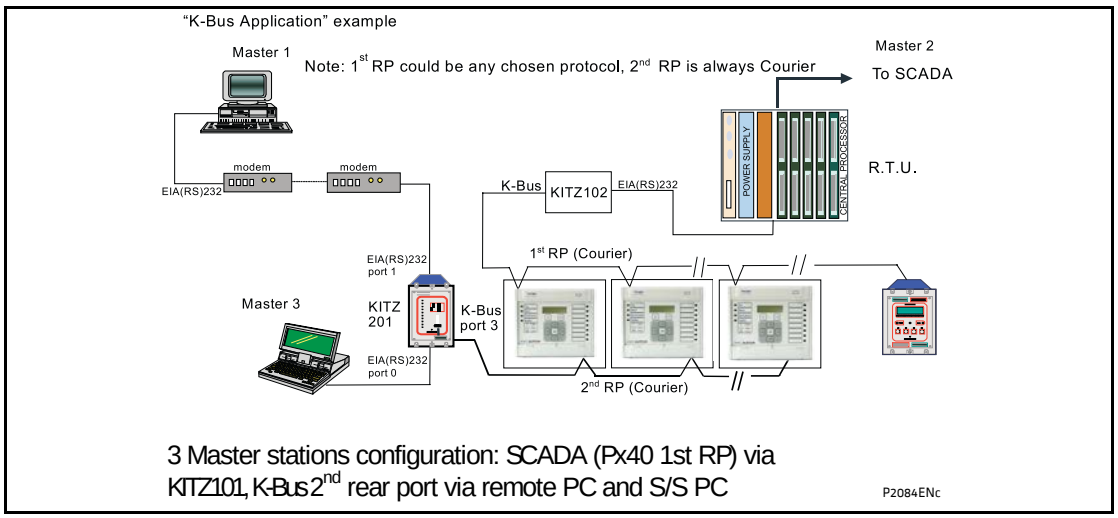


Figure 3: Second rear port K-Bus application

SC

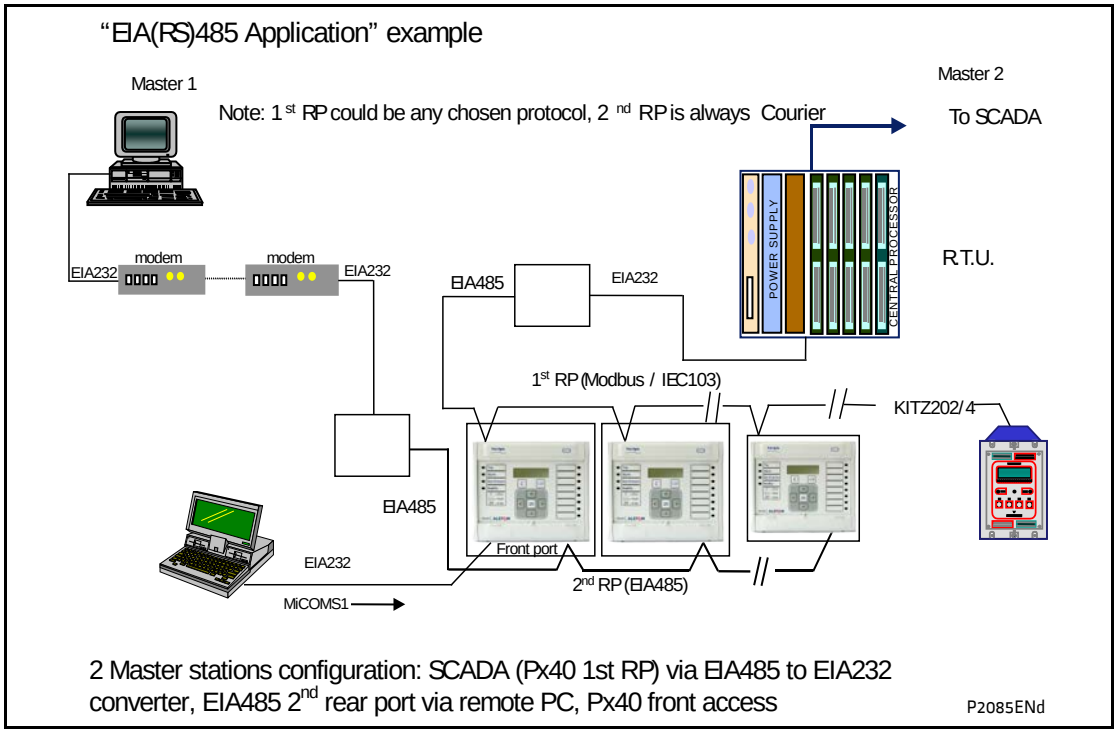


Figure 4: Second rear port EIA(RS)485 example

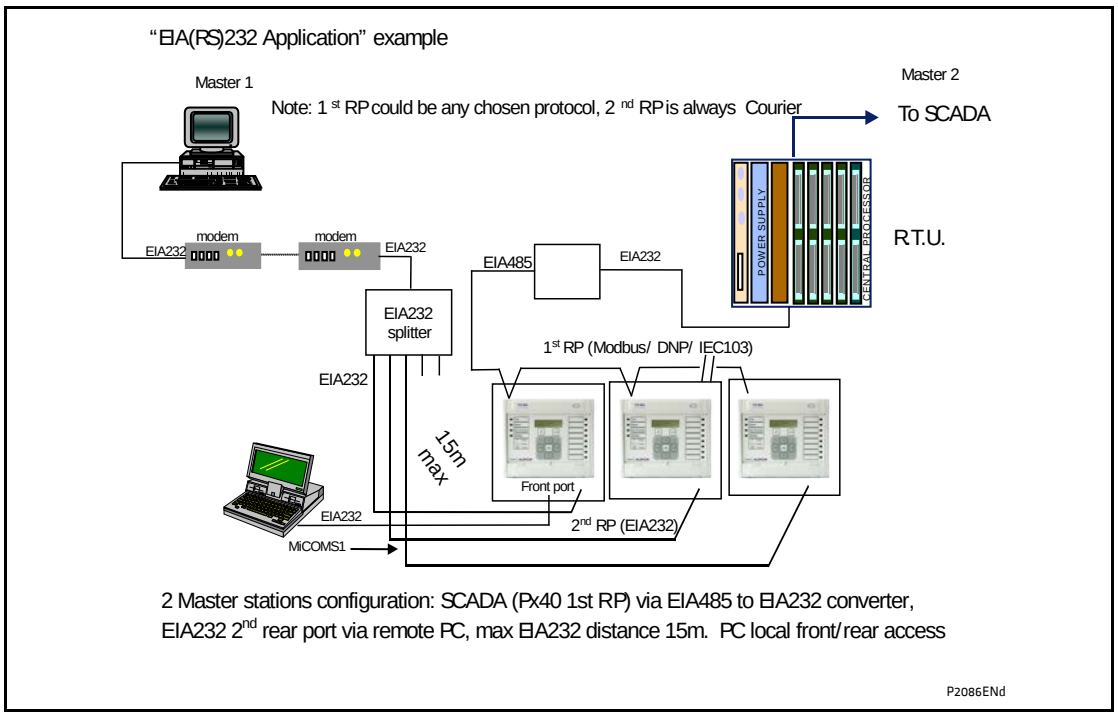


Figure 5: Second rear port EIA(RS)232 example

SC

3 COURIER INTERFACE

3.1 Courier protocol

Courier is a General Electric communication protocol. The concept of the protocol is that a standard set of commands is used to access a database of settings and data within the relay. This allows a generic master to be able to communicate with different slave devices. The application specific aspects are contained within the database itself rather than the commands used to interrogate it, so the master station does not need to be pre-configured.

The same protocol can be used via two physical links K-Bus or EIA(RS)232.

K-Bus is based on EIA(RS)485 voltage levels with HDLC FM0 encoded synchronous signaling and its own frame format. The K-Bus twisted pair connection is unpolarized, whereas the EIA(RS)485 and EIA(RS)232 interfaces are polarized.

The EIA(RS)232 interface uses the IEC 60870-5 FT1.2 frame format.

The relay supports an IEC 60870-5 FT1.2 connection on the front-port. This is intended for temporary local connection and is not suitable for permanent connection. This interface uses a fixed baud rate, 11-bit frame, and a fixed device address.

The rear interface is used to provide a permanent connection for K-Bus and allows multi-drop connection. It should be noted that although K-Bus is based on EIA(RS)485 voltage levels it is a synchronous HDLC protocol using FM0 encoding. It is not possible to use a standard EIA(RS)232 to EIA(RS)485 converter to convert IEC 60870-5 FT1.2 frames to K-Bus. Also, it is not possible to connect K-Bus to an EIA(RS)485 computer port. A protocol converter, such as the KITZ101, should be employed for this purpose.

For a detailed description of the Courier protocol, command-set and link description, see the following documentation:

R6509	K-Bus Interface Guide
R6510	IEC 60870 Interface Guide
R6511	Courier Protocol
R6512	Courier User Guide

3.2 Front courier port

The front EIA(RS)232[1] 9 pin port supports the Courier protocol for one to one communication. It is designed for use during installation and commissioning/maintenance and is not suitable for permanent connection. Since this interface will not be used to link the relay to a substation communication system, some of the features of Courier are not implemented. These are as follows:

Automatic extraction of Event Records:

Courier Status byte does not support the Event flag.

Send Event/Accept Event commands are not implemented.

Automatic extraction of Disturbance records:

Courier Status byte does not support the Disturbance flag.

Busy Response Layer:

Courier Status byte does not support the Busy flag, the only response to a request will be the final data.

[1] This port is actually compliant to EIA(RS)574; the 9-pin version of EIA(RS)232, see www.tiaonline.org.

Fixed Address:

The address of the front Courier port is always 1; the Change Device address command is not supported.

Fixed Baud Rate:

19200 bps.

Note: Although automatic extraction of event and disturbance records is not supported it is possible to manually access this data through the front port.

3.3 Supported command set

The following Courier commands are supported by the relay:

Protocol Layer

- Reset Remote Link
- Poll Status
- Poll Buffer*

Low Level Commands

- Send Event*
- Accept Event*
- Send Block
- Store Block Identifier
- Store Block Footer

Menu Browsing

- Get Column Headings
- Get Column Text
- Get Column Values
- Get Strings
- Get Text
- Get Value
- Get Column Setting Limits

Setting Changes

- Enter Setting Mode
- Preload Setting
- Abort Setting
- Execute Setting
- Reset Menu Cell
- Set Value

Control Commands

- Select Setting Group
- Change Device Address*

Set Real Time

Note: Commands indicated with an * are not supported via the front Courier port.

3.4 Relay courier database

The Courier database is two-dimensional. Each cell in the database is referenced by a row and column address. Both the column and the row can take a range from 0 to 255. Addresses in the database are specified as hexadecimal values, for example, 0A02 is column 0A (10 decimal) row 02. Associated settings or data are part of the same column. Row zero of the column has a text string to identify the contents of the column and to act as a column heading.

The Relay Menu Database document *P34x/EN MD* contains the complete database definition for the relay. For each cell location the following information is stated:

- Cell Text
- Cell Datatype
- Cell value
- Whether the cell is settable, if so
- Minimum value
- Maximum value
- Step size
- Password Level required to allow setting changes
- String information (for Indexed String or Binary flag cells)

3.5 Setting changes

(See R6512, Courier User Guide - Chapter 9)

Courier provides two mechanisms for making setting changes, both of these are supported by the relay. Either method can be used for editing any of the settings within the relay database.

3.5.1 Method 1

This uses a combination of three commands to perform a settings change:

Enter Setting Mode	-	Checks that the cell is settable and returns the limits.
Pre-load Setting	-	Places a new value to the cell, this value is echoed to ensure that setting corruption has not taken place, the validity of the setting is not checked by this action.
Execute Setting	-	Confirms the setting change, if the change is valid then a positive response is returned, if the setting change fails then an error response is returned.
Abort Setting	-	This command can be used to abandon the setting change.

This is the most secure method. It is ideally suited to on-line editors as the setting limits are taken from the relay before the setting change is made. However, this method can be slow if many settings are being changed as three commands are required for each change.

3.5.2 Method 2

The Set Value command can be used to directly change a setting, the response to this command will be either a positive confirm or an error code to indicate the nature of a failure. This command can be used to implement a setting more rapidly then the previous method, however the limits are not extracted from the relay. This method is most suitable for off-line setting editors such as S1 Agile, or for the issuing of pre-configured (SCADA) control commands.

3.5.3 Relay settings

There are three categories of settings within the relay database:

- Control and support
- Disturbance recorder
- Protection settings group

Setting changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to either the Disturbance recorder settings or the Protection Settings Groups are stored in a 'scratchpad' memory and are not immediately implemented by the relay.

To action setting changes stored in the scratchpad the Save Changes cell in the Configuration column must be written to. This allows the changes to either be confirmed and stored in non-volatile memory, or the setting changes to be aborted.

3.5.4 Setting transfer mode

If it is necessary to transfer all of the relay settings to or from the relay a cell within the Communication System Data column can be used. This cell (location BF03) when set to 1 makes all of the relay settings visible. Any setting changes made, with the relay set in this mode, are stored in scratchpad memory (including control and support settings). When the value of BF03 is set back to 0 any setting changes are verified and stored in non-volatile memory.

3.6 Event extraction

Events can be extracted either automatically (rear port only) or manually (either Courier port). For automatic extraction all events are extracted in sequential order using the standard Courier event mechanism, this includes fault/maintenance data if appropriate. The manual approach allows the user to select events, faults, or maintenance data at random from the stored records.

3.6.1 Automatic event extraction

(See Chapter 7 Courier User Guide, publication R6512).

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported through the rear Courier port.

When new event information is created the Event bit is set in the Status byte, this indicates to the Master device that event information is available. The oldest, unextracted event can be extracted from the relay using the Send Event command. The relay will respond with the event data, which is either a Courier Type 0 or Type 3 event. The Type 3 event is used for fault records and maintenance records.

Once an event has been extracted from the relay, the Accept Event can be used to confirm that the event has been successfully extracted. If all events have been extracted then the event bit is reset, if there are more events still to be extracted the next event can be accessed using the Send Event command as before.

3.6.2 Event types

Events will be created by the relay under the following circumstances:

- Change of state of output contact
- Change of state of opto input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out

- Fault record (Type 3 Courier Event)
- Maintenance record (Type 3 Courier Event)

3.6.3 Event format

The Send Event command results in the following fields being returned by the relay:

- Cell reference
- Time stamp
- Cell text
- Cell value

The Relay Menu Database document, *P34x/EN MD*, contains a table of the events created by the relay and indicates how the contents of the above fields are interpreted. Fault records and Maintenance records will return a Courier Type 3 event, which contains the above fields together with two additional fields:

- Event extraction column
- Event number

These events contain additional information that is extracted from the relay using the referenced extraction column. Row 01 of the extraction column contains a setting that allows the fault/maintenance record to be selected. This setting should be set to the event number value returned within the record; the extended data can be extracted from the relay by uploading the text and data from the column.

3.6.4 Manual event record extraction

Column 01 of the database can be used for manual viewing of event, fault, and maintenance records. The contents of this column will depend on the nature of the record selected. It is possible to select events by event number and to directly select a fault record or maintenance record by number.

Event Record selection (Row 01)

This cell can be set to a value between 0 to 249 to select which of the 250 stored events is selected, 0 will select the most recent record; 249 the oldest stored record. For simple event records, (Type 0) cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3) then the remainder of the column will contain the additional information.

Fault Record Selection (Row 05)

This cell can be used to directly select a fault record using a value between 0 and 4 to select one of up to five stored fault records. (0 will be the most recent fault and 4 will be the oldest). The column will then contain the details of the fault record selected.

Maintenance Record Selection (Row F0)

This cell can be used to select a maintenance record using a value between 0 and 4 and operates in a similar way to the fault record selection.

It should be noted that if this column is used to extract event information from the relay the number associated with a particular record will change when a new event or fault occurs.

3.7 Disturbance record extraction

The stored disturbance records within the relay are accessible in a compressed format through the Courier interface. The records are extracted using column B4.

Note: Cells required for extraction of uncompressed disturbance records are not supported.

Select Record Number (Row 01)

This cell can be used to select the record to be extracted. Record 0 is the oldest unextracted record, already extracted older records will be assigned positive values, and negative values will be used for more recent records. To help automatic extraction through the rear port the Disturbance bit of the Status byte is set by the relay whenever there are unextracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from cell 02. The disturbance record itself can be extracted using the block transfer mechanism from cell B00B. It should be noted that the file extracted from the relay is in a compressed format. Use S1 Agile to de-compress this file and save the disturbance record in the COMTRADE format.

As has been stated, the rear Courier port can be used to automatically extract disturbance records as they occur. This operates using the standard Courier mechanism, see Chapter 8 of the Courier User Guide. The front Courier port does not support automatic extraction although disturbance record data can be extracted manually from this port.

3.8 Programmable scheme logic settings

The programmable scheme logic (PSL) settings can be uploaded from and downloaded to the relay using the block transfer mechanism defined in Chapter 12 of the Courier User Guide.

The following cells are used to perform the extraction:

- B204 Domain/: Used to select either PSL settings (Upload or download) or PSL configuration data (Upload only)
- B208 Sub-Domain: Used to select the Protection Setting Group to be uploaded/downloaded.
- B20C Version: Used on a download to check the compatibility of the file to be downloaded with the relay.
- B21C Transfer Mode: Used to set-up the transfer process.
- B120 Data Transfer Cell: Used to perform upload or download.

The programmable scheme-logic settings can be uploaded and downloaded to and from the relay using this mechanism. If it is necessary to edit the settings S1 Agile must be used as the data format is compressed. S1 Agile also performs checks on the validity of the settings before they are downloaded to the relay.

4 MODBUS INTERFACE

The MODBUS interface is a master/slave protocol and it is defined by MODBUS.org:

See www.modbus.org

MODBUS Serial Protocol Reference Guide: PI-MBUS-300 Rev. E

4.1 Serial interface

The MODBUS interface uses the first rear EIA(RS)485 (RS485) two-wire port "RP1". The port is designated "EIA(RS)485/K-Bus Port" on the external connection diagrams.

The interface uses the MODBUS "RTU" mode of communication, rather than the "ASCII" mode since it provides for more efficient use of the communication bandwidth and is in wide spread use. This mode of communication is defined by the MODBUS standard, noted above.

4.1.1 Character framing

The character framing is 1 start bit, 8 bit data, either 1 parity bit and 1 stop bit, or two stop bits. This gives 11 bits per character.

4.1.2 Maximum MODBUS query and response frame size

The maximum query and response frame size is limited to 260 bytes in total. (This includes the frame header and CRC footer, as defined by the MODBUS protocol.).

4.1.3 User configurable communications parameters

The following parameters can be configured for this port using the product's front panel user interface (in the communications sub-menu):

- Baud rate: 9600, 19200, 38400bps
- Device address: 1 - 247
- Parity: Odd, even, none.
- Inactivity time: [2] 1 - 30 minutes

Note: The MODBUS interface communication parameters are not part of the product's setting file and cannot be configured with the S1 Agile setting support tool.

4.2 Supported MODBUS query functions

The MODBUS protocol provides numerous query functions, of which the product supports the subset in Table 1. The product will respond with exception code 01 if any other query function is received by it.

Query function code	MODBUS query name	Application
01	Read Coil Status	Read status of output contacts (0x addresses)
02	Read Input Status	Read status of opto-isolated status inputs (1x addresses)
03	Read Holding Registers	Read setting values (4x addresses)
04	Read Input Registers	Read measurement values (3x addresses)
06	Preset Single Register	Write single setting value (4x addresses)

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2 The inactivity timer is started (or restarted) whenever the active password level is reduced upon the entry of a valid password, or a change is made to the setting scratchpad. When the timer expires, the password level is restored to its default level and any pending (uncommitted) setting changes on the scratch pad are discarded. The inactivity timer is disabled when the password level is at its default value and there are no settings pending on the scratchpad. See section 4.13.

Query function code	MODBUS query name	Application
07	Read Exception Status	Read relay status, same value as register 3x1
08	Diagnostics	Application defined by the MODBUS protocol specification
11	Fetch Communication Event Counter	
12	Fetch Communication Event Log	
16	Preset Multiple Registers	Write multiple setting values (4x addresses)

Table 1: MODBUS query functions supported by the product

4.3 MODBUS response code interpretation

Code	MODBUS response name	Product interpretation
01	Illegal Function Code	The function code transmitted is not supported.
02	Illegal Data Address	The start data address in the request is not an allowable value. If any of the addresses in the range cannot be accessed due to password protection then all changes within the request are discarded and this error response will be returned. **Note:** If the start address is correct but the range includes non-implemented addresses this response is not produced.
03	Illegal Value	A value referenced in the data field transmitted by the master is not within range. Other values transmitted within the same packet will be executed if inside range.
04	Slave Device Failure	An exception arose during the processing of the received query that is not covered by any of the other exception codes in this table.
05	Acknowledge	Not used.
06	Slave Device Busy	The write command cannot be implemented due to the product's internal database being locked by another interface. This response is also produced if the product is busy executing a previous request.

Table 2: MODBUS response code interpretation

4.4 Maximum query and response parameters

Table 3 shows the maximum amount of data that the product can process for each of the supported query functions (see section 4.2) and the maximum amount of data that can be sent in a corresponding response frame. The principal constraint is the maximum query and response frame size, as noted in section 4.1.2. Maximum MODBUS query and response frame size.

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Query function code	MODBUS query name	Maximum query data request size	Maximum response data size
01	Read Coil Status	32 coils	32 coils
02	Read Input Status	32 inputs	32 inputs
03	Read Holding Registers	127 registers	127 registers
04	Read Input Registers	127 registers	127 registers
06	Preset Single Register	1 register	1 register
07	Read Exception Status	-	8 coils
08	Diagnostics	-	-

Query function code	MODBUS query name	Maximum query data request size	Maximum response data size
11	Fetch Communication Event Counter	-	-
12	Fetch Communication Event Log	-	70 bytes
16	Preset Multiple Registers	127 registers	127 registers

Table 3: Maximum query and response parameters for supported queries

4.5 Register mapping

4.5.1 Conventions

4.5.1.1 Memory pages

The MODBUS specification associates a specific register address space to each query that has a data address field. The address spaces are often called memory pages, because they are analogous to separate memory devices. In fact a simplistic view of the queries in MODBUS is that a specified location in a specified memory device is being read or written. However, it should be borne in mind that the product's implementation of such queries is not as a literal memory access but as a translation to an internal database query[3].

Each MODBUS memory page has a name and an ID. Table 4 provides a summary of the memory pages, their Ids, and their application in the product.

It is common shorthand practice to prefix a decimal register address with the page ID and, for the most part, this is the style used in this document.

Memory page ID	MODBUS memory page name	Product application
0x	Coil Status	Read and write access of the Output Relays.
1x	Input Status	Read only access of the Opto-Isolated Status Inputs.
3x	Input Registers	Read only data access, e.g. measurements and records.
4x	Holding Registers	Read and write data access, e.g. Product configurations settings and control commands.
6x	Extended Memory File	Not used/supported.

Table 4: MODBUS "memory" pages reference and application

4.5.1.2 MODBUS register identification

The MODBUS convention is to document register identifiers with ordinal values (first, second, third…) whereas the actual protocol uses memory-page based register addresses that begin with address zero. Therefore, the first register in a memory page is register address zero. The second register is register address 1 and so on. In general, one must be subtracted from a registers identifier to find its equivalent address.

Note: The page number notation is not part of the address.

3 One consequence of this is that the granularity of the register address space (in the 3x and 4x memory pages) is governed by the size of the data item being requested from the internal database. Since this is often more than the 16-bits of an individual register, not all register addresses are valid. See section 4.14 for more details.

Example:

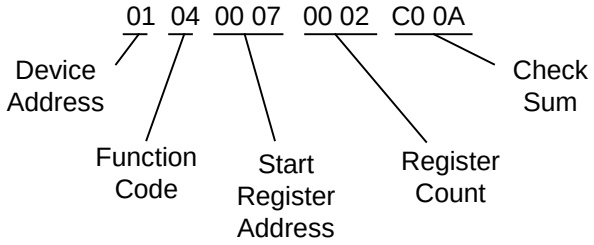
Task:

Obtain the status of the output contacts from the P343 device at address 1.

The output contact status is a 32-bit binary string held in input registers 3x8 and 3x9 (see section 4.8).

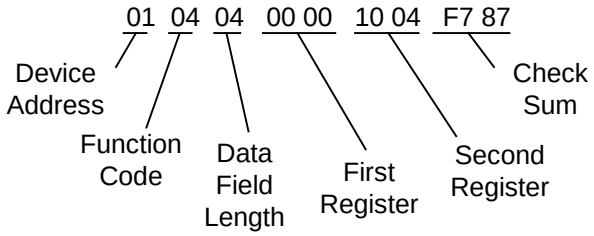
Select MODBUS function code 4 “Read input registers” and request two registers starting at input register address 7. NB the register address is one less than the required register ordinal.

The MODBUS query frame is: [4]



The frame is transmitted from left to right by the master device. Note that the start register address, register count and check sum are all 16-bit numbers that are transmitted in a high byte - low byte order.

The query may elicit the following response: 4



The frame was transmitted from left to right by the slave device. The response frame is valid because 8th bit of the function code field is not set. The data field length is 4 bytes since the query was a read of two 16-bit registers. The data field consists of two pairs of bytes in a high byte - low byte order with the first requested registers data coming first. Therefore, the request for the 32-bit output contact status starting at register 3x8 is 00001004h (1000000000100b), which indicates that outputs 3 and 13 are energized and the remaining outputs are de-energized.

4.6 Register map

For a complete map of the MODBUS addresses supported by the product, see the Relay Menu Database document, *P34x/EN MD*.

The register map tables in this document include an “Equivalent Courier Cell” column. The cell identifiers relate to the product’s internal Courier database and may be used in cross-reference with the Courier Protocol documentation and/or the product’s front panel user interface documentation.

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The “Data Format” column specifies the format of the data presented by the associated MODBUS register or registers. Section 4.14 describes the formats used.

The right-hand columns in the tables show whether the register is used in a particular product model; an asterisk indicates that the model implements the register.

4.7 Measurement values

The following table presents all of the product’s available measurements: analog values and counters. Their values are refreshed approximately every second.

[4] The following frame data is shown in hexadecimal 8-bit bytes.

Measurement name	Measurement unit	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P341	P342	P343	P344	P345	P346
IA Magnitude	Amps	0201	3x00200	3x00201	G24	2	*	*				
IA-1 Magnitude	Amps	0201	3x00200	3x00201	G24	2			*	*	*	*
IA Phase Angle	Degrees	0202	3x00202		G30	1	*	*				
IA-1 Phase Angle	Degrees	0202	3x00202		G30	1			*	*	*	*
IB Magnitude	Amps	0203	3x00203	3x00204	G24	2	*	*				
IB-1 Magnitude	Amps	0203	3x00203	3x00204	G24	2			*	*	*	*
IB Phase Angle	Degrees	0204	3x00205		G30	1	*	*				
IB-1 Phase Angle	Degrees	0204	3x00205		G30	1			*	*	*	*
IC Magnitude	Amps	0205	3x00206	3x00207	G24	2	*	*				
IC-1 Magnitude	Amps	0205	3x00206	3x00207	G24	2			*	*	*	*
IC Phase Angle	Degrees	0206	3x00208		G30	1	*	*				
IC-1 Phase Angle	Degrees	0206	3x00208		G30	1			*	*	*	*
IN Measured Mag	Amps	0207	3x00209	3x00210	G24	2		*	*	*	*	*
IN Measured Ang	Degrees	0208	3x00211		G30	1		*	*	*	*	*
IN Derived Mag	Amps	0209	3x00212	3x00213	G24	2	*	*				
IN-1 Derived Mag	Amps	0209	3x00212	3x00213	G24	2			*	*	*	*
IN Derived Angle	Degrees	020A	3x00214		G30	1	*					
Isen1 Magnitude	Amps	020B	3x00215	3x00216	G24	2	*	*	*	*	*	*
Isen1 Angle	Degrees	020C	3x00217		G30	1	*	*	*	*	*	*
I1 Magnitude	Amps	020D	3x00218	3x00219	G24	2	*	*	*	*	*	*
I2 Magnitude	Amps	020E	3x00220	3x00221	G24	2	*	*	*	*	*	*
I0 Magnitude	Amps	020F	3x00222	3x00223	G24	2	*	*	*	*	*	*
I1 Phase Angle	Degrees	0241	3x00266		G30	1	*	*	*	*	*	*
I2 Phase Angle	Degrees	0243	3x00267		G30	1	*	*	*	*	*	*
I0 Phase Angle	Degrees	0245	3x00268		G30	1	*	*	*	*	*	*
IA RMS	Amps	0210	3x00224	3x00225	G24	2	*	*	*	*	*	*
IB RMS	Amps	0211	3x00226	3x00227	G24	2	*	*	*	*	*	*
IC RMS	Amps	0212	3x00228	3x00229	G24	2	*	*	*	*	*	*
IN-2 Derived Mag	Amps	0213	3x00273	3x00274	G24	2			*	*	*	*
VAB Magnitude	Volts	0214	3x00230	3x00231	G24	2	*	*	*	*	*	*
VAB Phase Angle	Degrees	0215	3x00232		G30	1	*	*	*	*	*	*
VBC Magnitude	Volts	0216	3x00233	3x00234	G24	2	*	*	*	*	*	*
VBC Phase Angle	Degrees	0217	3x00235		G30	1	*	*	*	*	*	*
VCA Magnitude	Volts	0218	3x00236	3x00237	G24	2	*	*	*	*	*	*
VCA Phase Angle	Degrees	0219	3x00238		G30	1	*	*	*	*	*	*
VAN Magnitude	Volts	021A	3x00239	3x00240	G24	2	*	*	*	*	*	*
VAN Phase Angle	Degrees	021B	3x00241		G30	1	*	*	*	*	*	*

Measurement name	Measurement unit	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P341	P342	P343	P344	P345	P346
VBN Magnitude	Volts	021C	3x00242	3x00243	G24	2	*	*	*	*	*	*
VBN Phase Angle	Degrees	021D	3x00244		G30	1	*	*	*	*	*	*
VCN Magnitude	Volts	021E	3x00245	3x00246	G24	2	*	*	*	*	*	*
VCN Phase Angle	Degrees	021F	3x00247		G30	1	*	*	*	*	*	*
VN Measured Mag	Volts	0220	3x00248	3x00249	G24	2	*	*	*			*
VN1 Measured Mag	Volts	0220	3x00248	3x00249	G24	2				*	*	
VN Measured Ang	Degrees	0221	3x00250		G30	1	*	*	*			*
VN1 Measured Ang	Degrees	0221	3x00250		G30	1				*	*	
VN2 Measured Mag	Volts	0250	3x00275	3x00276	G24	2				*	*	
VN2 Measured Ang	Degrees	0251	3x00277		G30	1				*	*	
VN Derived Mag	Volts	0222	3x00251	3x00252	G24	2	*	*	*	*	*	*
VN Derived Ang	Degrees	0223	3x00272[5]		G30	1	*	*	*	*	*	*
VN Derived Ang	Degrees	0223	3x00272[6]		G30	1	*	*	*	*	*	*
C/S Voltage Mag	Volts	0270	3x00281	3x00282	G24	2	*	*	*	*	*	*
C/S Voltage Ang	Degrees	0271	3x00283		G30	1	*	*	*	*	*	*
Gen-Bus Volt	Volts	0272	3x00284	3x00285			*	*	*	*	*	*
Gen-Bus Angle	Degrees	0273	3x00286		G30	1	*	*	*	*	*	*
Slip Frequency	Hertz	0274	3x00287		G30	1	*	*	*	*	*	*
C/S Frequency	Hertz	0275	3x00288		G30	1	*	*	*	*	*	*
V1 Magnitude	Volts	0224	3x00253	3x00254	G24	2	*	*	*	*	*	*
V2 Magnitude	Volts	0225	3x00255	3x00256	G24	2	*	*	*	*	*	*
V0 Magnitude	Volts	0226	3x00257	3x00258	G24	2	*	*	*	*	*	*
V1 Phase Angle	Degrees	0247	3x00269		G30	1	*	*	*	*	*	*
V2 Phase Angle	Degrees	0249	3x00270		G30	1	*	*	*	*	*	*
V0 Phase Angle	Degrees	024B	3x00271		G30	1	*	*	*	*	*	*
VAN RMS	Volts	0227	3x00259	3x00260	G24	2	*	*	*	*	*	*
VBN RMS	Volts	0228	3x00261	3x00262	G24	2	*	*	*	*	*	*
VCN RMS	Volts	0229	3x00263	3x00264	G24	2	*	*	*	*	*	*

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5 Register 3x00272 was 3x00252 in P340 software revisions 01, 02, 03, 04, 05, 06, & 07. Register 3x00252 overlaps with the register pair beginning at 3x00251. As separate requests, these registers yielded the correct values. However, the overlap prevents a multi-register request that yields the required data. Moreover, the overlap could confuse certain master stations such that the value of assigned to the 3x00252 variable was the value yielded for the 3x00251 register-pair request. This is because it considers the slaves register map to be discrete 16 bit registers akin to a piece of memory and simply works to construct a copy of the slaves register memory.

6 Register 3x00272 was 3x00252 in P340 software revisions 01, 02, 03, 04, 05, 06, & 07. Register 3x00252 overlaps with the register pair beginning at 3x00251. As separate requests, these registers yielded the correct values. However, the overlap prevents a multi-register request that yields the required data. Moreover, the overlap could confuse certain master stations such that the value of assigned to the 3x00252 variable was the value yielded for the 3x00251 register-pair request. This is because it considers the slaves register map to be discrete 16 bit registers akin to a piece of memory and simply works to construct a copy of the slaves register memory.

Measurement name	Measurement unit	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P341	P342	P343	P344	P345	P346
Isen2 Magnitude	Amps	022A	3x00289	3x00290	G24	2					*	
Isen2 Angle	Degrees	022B	3x00291		G30	1					*	
Frequency	Hertz	022D	3x00265		G30	1	*	*	*	*	*	*
A Phase Watts	Watts	0301	3x00391	3x00392	G125	2	*	*	*	*	*	*
A Phase Watts	Watts	0301	3x00300	3x00302	G29	3	*	*	*	*	*	*
B Phase Watts	Watts	0302	3x00393	3x00394	G125	2	*	*	*	*	*	*
B Phase Watts	Watts	0302	3x00303	3x00305	G29	3	*	*	*	*	*	*
C Phase Watts	Watts	0303	3x00395	3x00396	G125	2	*	*	*	*	*	*
C Phase Watts	Watts	0303	3x00306	3x00308	G29	3	*	*	*	*	*	*
A Phase VArs	VAr	0304	3x00397	3x00398	G125	2	*	*	*	*	*	*
A Phase VArs	VAr	0304	3x00309	3x00311	G29	3	*	*	*	*	*	*
B Phase VArs	VAr	0305	3x00399	3x00400	G125	2	*	*	*	*	*	*
B Phase VArs	VAr	0305	3x00312	3x00314	G29	3	*	*	*	*	*	*
C Phase VArs	VAr	0306	3x00401	3x00402	G125	2	*	*	*	*	*	*
C Phase VArs	VAr	0306	3x00315	3x00317	G29	3	*	*	*	*	*	*
A Phase VA	VA	0307	3x00403	3x00404	G125	2	*	*	*	*	*	*
A Phase VA	VA	0307	3x00318	3x00320	G29	3	*	*	*	*	*	*
B Phase VA	VA	0308	3x00405	3x00406	G125	2	*	*	*	*	*	*
B Phase VA	VA	0308	3x00321	3x00323	G29	3	*	*	*	*	*	*
C Phase VA	VA	0309	3x00407	3x00408	G125	2	*	*	*	*	*	*
C Phase VA	VA	0309	3x00324	3x00326	G29	3	*	*	*	*	*	*
3 Phase Watts	Watts	030A	3x00409	3x00410	G125	2	*	*	*	*	*	*
3 Phase Watts	Watts	030A	3x00327	3x00329	G29	3	*	*	*	*	*	*
3 Phase VArs	VAr	030B	3x00411	3x00412	G125	2	*	*	*	*	*	*
3 Phase VArs	VAr	030B	3x00330	3x00332	G29	3	*	*	*	*	*	*
3 Phase VA	VA	030C	3x00413	3x00414	G125	2	*	*	*	*	*	*
3 Phase VA	VA	030C	3x00333	3x00335	G29	3	*	*	*	*	*	*
NPS Power S2	VA	030D	3x00336	3x00338	G29	3		*	*	*	*	*
NPS Power S2	VA	030D	3x00500	3x00501	G125	2		*	*	*	*	*
APh Sensitive Watts	Watts	0420	3x00476	3x00477	G125	2	*	*	*	*	*	*
APh Sensitive VArs	VAr	0421	3x00478	3x00479	G125	2	*	*	*	*	*	*
APh Sensitive Power Angle	Degrees	0422	3x00480		G30	1	*	*	*	*	*	*
3Ph Power Factor	-	030E	3x00339		G30	1	*	*	*	*	*	*
APh Power Factor	-	030F	3x00340		G30	1	*	*	*	*	*	*
BPh Power Factor	-	0310	3x00341		G30	1	*	*	*	*	*	*
CPh Power Factor	-	0311	3x00342		G30	1	*	*	*	*	*	*
3 Phase WHours Fwd	Wh	0312	3x00415	3x00416	G125	2	*	*	*	*	*	*
3 Phase WHours Fwd	Wh	0312	3x00343	3x00345	G29	3	*	*	*	*	*	*

Measurement name	Measurement unit	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P341	P342	P343	P344	P345	P346
3 Phase WHours Rev	Wh	0313	3x00417	3x00418	G125	2	*	*	*	*	*	*
3 Phase WHours Rev	Wh	0313	3x00346	3x00348	G29	3	*	*	*	*	*	*
3 Phase VArHours Fwd	VArh	0314	3x00419	3x00420	G125	2	*	*	*	*	*	*
3 Phase VArHours Fwd	VArh	0314	3x00349	3x00351	G29	3	*	*	*	*	*	*
3 Phase VArHours Rev	VArh	0315	3x00421	3x00422	G125	2	*	*	*	*	*	*
3 Phase VArHours Rev	VArh	0315	3x00352	3x00354	G29	3	*	*	*	*	*	*
3 Phase W Fix Demand	Watts	0316	3x00423	3x00424	G125	2	*	*	*	*	*	*
3 Phase W Fix Demand	Watts	0316	3x00355	3x00357	G29	3	*	*	*	*	*	*
3 Phase VArs Fix Demand	VAr	0317	3x00425	3x00426	G125	2	*	*	*	*	*	*
3 Phase VArs Fix Demand	VAr	0317	3x00358	3x00360	G29	3	*	*	*	*	*	*
IA Fixed Demand	Amps	0318	3x00361	3x00362	G24	2	*	*	*	*	*	*
IB Fixed Demand	Amps	0319	3x00363	3x00364	G24	2	*	*	*	*	*	*
IC Fixed Demand	Amps	031A	3x00365	3x00366	G24	2	*	*	*	*	*	*
3 Phase W Roll Demand	Watts	031B	3x00427	3x00428	G125	2	*	*	*	*	*	*
3 Phase W Roll Demand	Watts	031B	3x00367	3x00369	G29	3	*	*	*	*	*	*
3 Phase VArs Roll Demand	VAr	031C	3x00429	3x00430	G125	2	*	*	*	*	*	*
3 Phase VArs Roll Demand	VAr	031C	3x00370	3x00372	G29	3	*	*	*	*	*	*
IA Roll Demand	Amps	031D	3x00373	3x00374	G24	2	*	*	*	*	*	*
IB Roll Demand	Amps	031E	3x00375	3x00376	G24	2	*	*	*	*	*	*
IC Roll Demand	Amps	031F	3x00377	3x00378	G24	2	*	*	*	*	*	*
3 Phase W Peak Demand	Watts	0320	3x00431	3x00432	G125	2	*	*	*	*	*	*
3Ph W Peak Dem	Watts	0320	3x00379	3x00381	G29	3	*	*	*	*	*	*
3 Phase VArs Peak Demand	VAr	0321	3x00433	3x00434	G125	2	*	*	*	*	*	*
3 Phase VArs Peak Demand	VAr	0321	3x00382	3x00384	G29	3	*	*	*	*	*	*
IA Peak Demand	Amps	0322	3x00385	3x00386	G24	2	*	*	*	*	*	*
IB Peak Demand	Amps	0323	3x00387	3x00388	G24	2	*	*	*	*	*	*
IC Peak Demand	Amps	0324	3x00389	3x00390	G24	2	*	*	*	*	*	*
CT2 NPS Power S2	Watts	0326	3x00593	3x00595	G29	3			*	*	*	*

Measurement name	Measurement unit	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P341	P342	P343	P344	P345	P346
IA-2 Magnitude	Amps	0401	3x00435	3x00436	G24	2			*	*	*	*
IA-2 Phase Angle	Degrees	0402	3x00437		G30	1			*	*	*	*
IB-2 Magnitude	Amps	0403	3x00438	3x00439	G24	2			*	*	*	*
IB-2 Phase Angle	Degrees	0404	3x00440		G30	1			*	*	*	*
IC-2 Magnitude	Amps	0405	3x00441	3x00442	G24	2			*	*	*	*
IC-2 Phase Angle	Degrees	0406	3x00443		G30	1			*	*	*	*
IA Differential	Amps	0407	3x00444	3x00445	G24	2			*	*	*	*
IB Differential	Amps	0408	3x00446	3x00447	G24	2			*	*	*	*
IC Differential	Amps	0409	3x00448	3x00449	G24	2			*	*	*	*
IA Bias	Amps	040A	3x00450	3x00451	G24	2			*	*	*	*
IB Bias	Amps	040B	3x00452	3x00453	G24	2			*	*	*	*
IC Bias	Amps	040C	3x00454	3x00455	G24	2			*	*	*	*
IREF Diff	Amps	040D	3x00456	3x00457	G24	2		*	*	*	*	*
IREF Bias	Amps	040E	3x00458	3x00459	G24	2		*	*	*	*	*
VN 3rd Harmonic	Volts	040F	3x00460	3x00461	G24	2			*	*	*	
NPS Thermal	Percentage	0410	3x00462		G1	1		*	*	*	*	*
RTD 1	Celsius	0412	3x00463		G10	1		*	*	*	*	*
RTD 2	Celsius	0413	3x00464		G10	1		*	*	*	*	*
RTD 3	Celsius	0414	3x00465		G10	1		*	*	*	*	*
RTD 4	Celsius	0415	3x00466		G10	1		*	*	*	*	*
RTD 5	Celsius	0416	3x00467		G10	1		*	*	*	*	*
RTD 6	Celsius	0417	3x00468		G10	1		*	*	*	*	*
RTD 7	Celsius	0418	3x00469		G10	1		*	*	*	*	*
RTD 8	Celsius	0419	3x00470		G10	1		*	*	*	*	*
RTD 9	Celsius	041A	3x00471		G10	1		*	*	*	*	*
RTD 10	Celsius	041B	3x00472		G10	1		*	*	*	*	*
RTD Open Circuit	-	041C	3x00473		G108	1		*	*	*	*	*
RTD Short Circuit	-	041D	3x00474		G109	1		*	*	*	*	*
RTD Data Error	-	041E	3x00475		G110	1		*	*	*	*	*
Sen Watts	W	0420	3x00527	3x00529	G29	2		*	*	*	*	*
Sen Vars	VAr	0421	3x00530	3x00532	G29	2		*	*	*	*	*
Sen Power Factor		0422	3x00533		G30	1		*	*	*	*	*
Thermal Overload	Percentage	0423	3x00481		G1	1	*	*	*	*	*	*
CLIO Input 1	-	0425	3x00482	3x00483	G125	2	*	*	*	*	*	*
CLIO Input 2	-	0426	3x00484	3x00485	G125	2	*	*	*	*	*	*
CLIO Input 3	-	0427	3x00486	3x00487	G125	2	*	*	*	*	*	*
CLIO Input 4	-	0428	3x00488	3x00489	G125	2	*	*	*	*	*	*
CB Operations	-	0601	3x00600		G1	1	*	*	*	*	*	*
Total IA Broken	Amps	0602	3x00601	3x00602	G24	2	*	*	*	*	*	*
Total IB Broken	Amps	0603	3x00603	3x00604	G24	2	*	*	*	*	*	*
Total IC Broken	Amps	0604	3x00605	3x00606	G24	2	*	*	*	*	*	*

Measurement name	Measurement unit	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P341	P342	P343	P344	P345	P346
CB Operate Time	Seconds	0605	3x00607		G25	1	*	*	*	*	*	*
Freq Band 1 Time (s)	Seconds	0430	3x00502	3x00503	G27	2		*	*	*	*	*
Freq Band 2 Time (s)	Seconds	0434	3x00504	3x00505	G27	2		*	*	*	*	*
Freq Band 3 Time (s)	Seconds	0438	3x00506	3x00507	G27	2		*	*	*	*	*
Freq Band 4 Time (s)	Seconds	043C	3x00508	3x00509	G27	2		*	*	*	*	*
Freq Band 5 Time (s)	Seconds	0440	3x00510	3x00511	G27	2		*	*	*	*	*
Freq Band 6 Time (s)	Seconds	0444	3x00512	3x00513	G27	2		*	*	*	*	*
df/dt	Hertz/S	0448	3x00525	3x00526	G125	2	*	*	*	*	*	*
Volts Per Hertz	V/Hz	0450	3x00514	3x00515	G24	2		*	*	*	*	*
64S V Magnitude	Volts	0452	0x00516	0x00517	G24	2					*	
64S I Magnitude	Amps	0454	0x00518	0x00519	G24	2					*	
64S I Angle	Degrees	0455	0x00520		G30	1					*	
64S R secondary	Ohms	0457	0x00521	0x00522	G125	2					*	
64S R primary	Ohms	0458	0x00523	0x00524	G125	2					*	
64R CL Input	Amps	0471	0x00539	0x00540	G125	2		*	*	*	*	*
64R R Fault	Ohms	0472	0x00541	0x00552	G125	2		*	*	*	*	*
IA Diff PU	Amps	0491	3x11300	3x11301	G24	2			*	*	*	*
IB Diff PU	Amps	0492	3x11302	3x11303	G24	2			*	*	*	*
IC Diff PU	Amps	0493	3x11304	3x11305	G24	2			*	*	*	*
IA Bias PU	Amps	0494	3x11306	3x11307	G24	2			*	*	*	*
IB Bias PU	Amps	0495	3x11308	3x11309	G24	2			*	*	*	*
IC Bias PU	Amps	0496	3x11310	3x11311	G24	2			*	*	*	*
IA Diff 2H	Amps	0497	3x11312	3x11313	G24	2			*	*	*	*
IB Diff 2H	Amps	0498	3x11314	3x11315	G24	2			*	*	*	*
IC Diff 2H	Amps	0499	3x11316	3x11317	G24	2			*	*	*	*
IA Diff 5H	Amps	049A	3x11318	3x11319	G24	2			*	*	*	*
IB Diff 5H	Amps	049B	3x11320	3x11321	G24	2			*	*	*	*
IC Diff 5H	Amps	049C	3x11322	3x11323	G24	2			*	*	*	*
CT2 I1 Mag	Amps	049D	3x11324	3x11325	G24	2			*	*	*	*
CT2 I1 Angle	Degrees	049E	3x11351		G30	1			*	*	*	*
CT2 I2 Mag	Amps	049F	3x11326	3x11327	G24	2			*	*	*	*
CT2 I2 Angle	Degrees	04A0	3x11352		G30	1			*	*	*	*
CT2 I0 Mag	Amps	04A1	3x11328	3x11329	G24	2			*	*	*	*
CT2 I0 Angle	Degrees	04A2	3x11353		G30	1			*	*	*	*
CT1 I2/I1	-	04A3	3x11330	3x11331	G24	2			*	*	*	*
CT2 I2/I1	-	04A4	3x11332	3x11333	G24	2			*	*	*	*
ZA Mag	Ohms	04A5	3x11354	3x11355	G125	2		*	*	*	*	*
Hot Spot T	Celsius	0501	3x11334		G10	1		*	*	*	*	*
Top Oil T	Celsius	0502	3x11335		G10	1		*	*	*	*	*

Measurement name	Measurement unit	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P341	P342	P343	P344	P345	P346
Ambient T	Celsius	0504	4x00113		G10	1		*	*	*	*	*
TOL Pretrip left	Seconds	0505	3x11337	3x11338	G24	2		*	*	*	*	*
LOL status	-	0506	3x11339	3x11340	G24	2		*	*	*	*	*
Rate of LOL	-	0508	3x11341	3x11342	G24	2		*	*	*	*	*
LOL Ageing Fact	-	0509	3x11343	3x11344	G24	2		*	*	*	*	*
Lres at Design T	-	050A	3x11345	3x11346	G24	2		*	*	*	*	*
FAA,m	-	050B	3x11347	3x11348	G24	2		*	*	*	*	*
Lres at FAA,m	-	050C	3x11349	3x11350	G24	2		*	*	*	*	*
Counter 1		0560	3x00617		G1	1	*	*	*	*	*	*
Counter 2		0561	3x00618		G1	1	*	*	*	*	*	*
Counter 3		0562	3x00619		G1	1	*	*	*	*	*	*
Counter 4		0563	3x00620		G1	1	*	*	*	*	*	*
Counter 5		0564	3x00621		G1	1	*	*	*	*	*	*
Counter 6		0565	3x00622		G1	1	*	*	*	*	*	*
Counter 7		0566	3x00623		G1	1	*	*	*	*	*	*
Counter 8		0567	3x00624		G1	1	*	*	*	*	*	*
Counter 9		0568	3x00625		G1	1	*	*	*	*	*	*
Counter 10		0569	3x00626		G1	1	*	*	*	*	*	*
Counter 11		056A	3x00627		G1	1	*	*	*	*	*	*
Counter 12		056B	3x00628		G1	1	*	*	*	*	*	*
Counter 13		056C	3x00629		G1	1	*	*	*	*	*	*
Counter 14		056D	3x00630		G1	1	*	*	*	*	*	*
Counter 15		056E	3x00631		G1	1	*	*	*	*	*	*
Counter 16		056F	3x00632		G1	1	*	*	*	*	*	*

Table 5: Measurement data available in the P341-6 product range

4.8 Binary status information

Binary status information is available for the product's optically-isolated status inputs ("optos"), relay contact outputs, alarm flags, control inputs, internal digital data bus ("DDB"), and the front panel 25-pin test port. [7]

The product's internal digital data bus consists of 2047 binary-status flags. The allocation of the points in the DDB are largely product and version specific. See the Relay Menu Database document, *P34x/EN MD*, for a definition of the product's DDB.

The relay-contact status information is available from the 0x "Coil Status" MODBUS page and from the 3x "Input Register" MODBUS page. For legacy reasons the information is duplicated in the 3x page with explicit registers (8 & 9) and in the DDB status register area (11023 & 11024).

The current state of the optically isolated status inputs is available from the 1x "Input Status" MODBUS page and from the 3x "Input Register" MODBUS page. The principal 3x registers are part of the DDB status register area (11025 & 11026). For legacy reasons, a single register at 3x00007 provides the status of the first 16 inputs.

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[7] The test port allows the product to be configured to map up to eight of its digital data bus (DDB - see Relay Menu Database document, *P34x/EN MD*) signals to eight output pins. The usual application is to control test equipment. However, since the test port output status is available on the MODBUS interface, it could be used to efficiently collect up to eight DDB signals.

The 0x “Coil Status” and 1x “Input Status” pages allow individual or blocks of binary status flags to be read. The resultant data is left aligned and transmitted in a big-endian (high order to low order) format in the response frame. Relay contact 1 is mapped to coil 1, contact 2 to coil 2 and so on. Similarly, opto-input 1 is mapped to input 1, opto-input 2 to input 2 and so on.

The following table presents the available 3x and 4x binary status information.

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P341	P342	P343	P344	P345	P346
Product Status	-	3x00001		G26	1	*	*	*	*	*	*
Opto I/P Status	0030	3x11025	3x11026	G8	2	*	*	*	*	*	*
Relay O/P Status	0040	3x00008	3x00009	G9	2	*	*	*	*	*	*
Alarm Status 1	0050	3x00011	3x00012	G96	2	*	*	*	*	*	*
Alarm Status 2	0051	3x00013	3x00014	G128	2	*	*	*	*	*	*
Alarm Status 3	0052	3x00015	3x00016	G228	2	*	*	*	*	*	*
Ctrl I/P Status	1201	4x00950	4x00951	G202	2	*	*	*	*	*	*
Relay Test Port Status	0F03	3x11022		G1	1	*	*	*	*	*	*
DDB 31 - 0	0F20	3x11023	3x11024	G27	2	*	*	*	*	*	*
DDB 63 - 32	0F21	3x11025	3x11026	G27	2	*	*	*	*	*	*
DDB 95 - 64	0F22	3x11027	3x11028	G27	2	*	*	*	*	*	*
DDB 127 - 96	0F23	3x11029	3x11030	G27	2	*	*	*	*	*	*
DDB 159 - 128	0F24	3x11031	3x11032	G27	2	*	*	*	*	*	*
DDB 191 - 160	0F25	3x11033	3x11034	G27	2	*	*	*	*	*	*
DDB 223 - 192	0F26	3x11035	3x11036	G27	2	*	*	*	*	*	*
DDB 255 - 224	0F27	3x11037	3x11038	G27	2	*	*	*	*	*	*
DDB 287 - 256	0F28	3x11039	3x11040	G27	2	*	*	*	*	*	*
DDB 319 - 288	0F29	3x11041	3x11042	G27	2	*	*	*	*	*	*
DDB 351 - 320	0F2A	3x11043	3x11044	G27	2	*	*	*	*	*	*
DDB 383 - 352	0F2B	3x11045	3x11046	G27	2	*	*	*	*	*	*
DDB 415 - 384	0F2C	3x11047	3x11048	G27	2	*	*	*	*	*	*
DDB 447 - 416	0F2D	3x11049	3x11050	G27	2	*	*	*	*	*	*
DDB 479 - 448	0F2E	3x11051	3x11052	G27	2	*	*	*	*	*	*
DDB 511 - 480	0F2F	3x11053	3x11054	G27	2	*	*	*	*	*	*
DDB 543 - 512	0F30	3x11055	3x11056	G27	2	*	*	*	*	*	*
DDB 575 - 544	0F31	3x11057	3x11058	G27	2	*	*	*	*	*	*
DDB 607 - 576	0F32	3x11059	3x11060	G27	2	*	*	*	*	*	*
DDB 639 - 608	0F33	3x11061	3x11062	G27	2	*	*	*	*	*	*
DDB 671 - 640	0F34	3x11063	3x11064	G27	2	*	*	*	*	*	*
DDB 703 - 672	0F35	3x11065	3x11066	G27	2	*	*	*	*	*	*
DDB 735 - 704	0F36	3x11067	3x11068	G27	2	*	*	*	*	*	*
DDB 767 - 736	0F37	3x11069	3x11070	G27	2	*	*	*	*	*	*
DDB 799 - 768	0F38	3x11071	3x11072	G27	2	*	*	*	*	*	*
DDB 831 - 800	0F39	3x11073	3x11074	G27	2	*	*	*	*	*	*
DDB 863 - 832	0F3A	3x11075	3x11076	G27	2	*	*	*	*	*	*
DDB 895 - 864	0F3B	3x11077	3x11078	G27	2	*	*	*	*	*	*
DDB 927 - 896	0F3C	3x11079	3x11080	G27	2	*	*	*	*	*	*
DDB 959 - 928	0F3D	3x11081	3x11082	G27	2	*	*	*	*	*	*

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P341	P342	P343	P344	P345	P346
DDB 991 - 960	0F3E	3x11083	3x11084	G27	2	*	*	*	*	*	*
DDB 1023 - 992	0F3F	3x11085	3x11086	G27	2	*	*	*	*	*	*
DDB 1055-1024	0F40	3x11087	3x11088	G27	2	*	*	*	*	*	*
DDB 1087-1056	0F41	3x11089	3x11090	G27	2	*	*	*	*	*	*
DDB 1119-1088	0F42	3x11091	3x11092	G27	2	*	*	*	*	*	*
DDB 1151-1120	0F43	3x11093	3x11094	G27	2	*	*	*	*	*	*
DDB 1183-1152	0F44	3x11095	3x11096	G27	2	*	*	*	*	*	*
DDB 1215-1184	0F45	3x11097	3x11098	G27	2	*	*	*	*	*	*
DDB 1247-1216	0F46	3x11099	3x11100	G27	2	*	*	*	*	*	*
DDB 1279-1248	0F47	3x11101	3x11102	G27	2	*	*	*	*	*	*
DDB 1311-1280	0F48	3x11103	3x11104	G27	2	*	*	*	*	*	*
DDB 1343-1312	0F49	3x11105	3x11106	G27	2	*	*	*	*	*	*
DDB 1375-1344	0F4A	3x11107	3x11108	G27	2	*	*	*	*	*	*
DDB 1407-1376	0F4B	3x11109	3x11110	G27	2	*	*	*	*	*	*
DDB 1439-1408	0F4C	3x11111	3x11112	G27	2	*	*	*	*	*	*
DDB 1471-1440	0F4D	3x11113	3x11114	G27	2	*	*	*	*	*	*
DDB 1503-1472	0F4E	3x11115	3x11116	G27	2	*	*	*	*	*	*
DDB 1535-1504	0F4F	3x11117	3x11118	G27	2	*	*	*	*	*	*
DDB 1567-1536	0F50	3x11119	3x11120	G27	2	*	*	*	*	*	*
DDB 1599-1568	0F51	3x11121	3x11122	G27	2	*	*	*	*	*	*
DDB 1631-1600	0F52	3x11123	3x11124	G27	2	*	*	*	*	*	*
DDB 1663-1632	0F53	3x11125	3x11126	G27	2	*	*	*	*	*	*
DDB 1695-1664	0F54	3x11127	3x11128	G27	2	*	*	*	*	*	*
DDB 1727-1696	0F55	3x11129	3x11130	G27	2	*	*	*	*	*	*
DDB 1759-1728	0F56	3x11131	3x11132	G27	2	*	*	*	*	*	*
DDB 1791-1760	0F57	3x11133	3x11134	G27	2	*	*	*	*	*	*
DDB 1823-1792	0F58	3x11135	3x11136	G27	2	*	*	*	*	*	*
DDB 1855-1824	0F59	3x11137	3x11138	G27	2	*	*	*	*	*	*
DDB 1887-1856	0F5A	3x11139	3x11140	G27	2	*	*	*	*	*	*
DDB 1919-1888	0F5B	3x11141	3x11142	G27	2	*	*	*	*	*	*
DDB 1951-1920	0F5C	3x11143	3x11144	G27	2	*	*	*	*	*	*
DDB 1983-1952	0F5D	3x11145	3x11146	G27	2	*	*	*	*	*	*
DDB 2015-1984	0F5E	3x11147	3x11148	G27	2	*	*	*	*	*	*
DDB 2047-2016	0F5F	3x11149	3x11150	G27	2	*	*	*	*	*	*

Table 6: Binary status information available in the P340 product range

4.9 Measurement and binary status 3x register sets

The data available from the 3x input registers is arranged into register sets. A register set is a fixed collection of values in a contiguous block of register addresses. The advantage of this is that multiple values may be read with a single MODBUS query, function code 4 “Read Input Registers”, up to the maximum data limits of the query (see section 4.4).

The definition of a register-set is specified by the selection of a start and end address, which can span multiple contiguous values in the 3x Register, see the Relay Menu Database document, *P34x/EN MD*. The only rule being that a register set must not result in an attempt to read only part of a multi-register data type (see section 4.14). A register set can span unused register locations, in which case a value of zero is returned for each such register location.

Some examples of useful register sets are:

- 3x11203 to 3x11150 provide the DDB status
- 3x391 to 3x408 provide the per phase power measurements in floating point format
- 3x409 to 3x414 provide the three-phase power measurements in floating point format
- 3x10106 to 3x10115 provide the ten RTD measurement values (P342/3/4/5/6 only)

There are many other possibilities depending on your application and an appraisal of the 3x Register Map in the Relay Menu Database document, *P34x/EN MD*. The capabilities of the MODBUS master device, performance targets, and communications latencies may also influence the degree to which multiple values are read as register sets, as opposed to individually.

4.10 Controls

The following table presents MODBUS 4x “Holding Registers” that allow the external system to control aspects of the product’s behavior, configuration, records, or items of plant connected to the product such as circuit breakers.

The column “Command or setting” indicates whether the control is a self-resetting “Command” or a state based “Setting”.

“Command” controls will automatically return to their default value when the control action has been completed. For example, writing the “trip” value to the “CB Trip/Close” control will result in the controlled circuit breaker opening (if CB remote control is enabled, the CB has a valid state, and it was closed). The value of the “CB Trip/Close” register will automatically return to “no operation”. This may lead to problems with masters that attempt to verify write requests by reading back the written value.

“Setting” controls maintain the written value, assuming that it was accepted. For example the **Active Setting** register reports the current active group on reads. The Active Setting Group register also accepts writes with a valid setting group number to change the active group to the one specified. This assumes that the setting group selection by optically isolated status inputs has not been enabled and that the specified group is enabled.

Entries without a defined setting range, as per the “min.”, “max.” and “step” columns, are binary-string values whose pattern is defined by its stated data type.

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	Default value	Command or setting	Min	Max	Step	Password level	P341	P342	P343	P344	P345	P346
Active Setting Group	0903	4x00404		G90	1	1	Setting	0	3	1	1	*	*	*	*	*	*
CB Trip/Close	0010	4x00021		G55	1	No Operation	Command	0	2	1	1	*	*	*	*	*	*
Reset NPS Thermal	0411	4x00104		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset RTD Flags	041F	4x00105		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset Thermal O/L	0424	4x00106		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Demand	0325	4x00103		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Record Control	-	4x00401		G6	1	0	Setting					*	*	*	*	*	*
Test Mode	0F0D	4x00858		G119	1	Disabled	Setting	0	2	1	2	*	*	*	*	*	*
Test LEDs	0F10	4x00862		G94	1	No Operation	Command	0	1	1	2	*	*	*	*	*	*
Lockout Reset	0708	4x00206		G11	1	No	Command	0	1	1	2	*	*	*	*	*	*
Reset CB Data	0606	4x00150		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Ctrl I/P Status	1201	4x00950	4x00951	G202	2	0	Setting				2	*	*	*	*	*	*
Control Input 1	1202	4x00952		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 2	1203	4x00953		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 3	1204	4x00954		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 4	1205	4x00955		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 5	1206	4x00956		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 6	1207	4x00957		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 7	1208	4x00958		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 8	1209	4x00959		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 9	120A	4x00960		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 10	120B	4x00961		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 11	120C	4x00962		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 12	120D	4x00963		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 13	120E	4x00964		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 14	120F	4x00965		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 15	1210	4x00966		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 16	1211	4x00967		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 17	1212	4x00968		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 18	1213	4x00969		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 19	1214	4x00970		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	Default value	Command or setting	Min	Max	Step	Password level	P341	P342	P343	P344	P345	P346
Control Input 20	1215	4x00971		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 21	1216	4x00972		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 22	1217	4x00973		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 23	1218	4x00974		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 24	1219	4x00975		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 25	121A	4x00976		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 26	121B	4x00977		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 27	121C	4x00978		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 28	121D	4x00979		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 29	121E	4x00980		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 30	121F	4x00981		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 31	1220	4x00982		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Control Input 32	1221	4x00983		G203	1	No Operation	Command	0	2	1	2	*	*	*	*	*	*
Reset Freq Band 1	0432	4x00107		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset Freq Band 2	0436	4x00108		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset Freq Band 3	043A	4x00109		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset Freq Band 4	043E	4x00110		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset Freq Band 5	0442	4x00111		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset Freq Band 6	0446	4x00112		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset Thermal	0503	4x00113		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset LOL	0507	4x00114		G11	1	No	Command	0	1	1	1		*	*	*	*	*
Reset Counter1	0580	4x00117		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter2	0581	4x00118		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter3	0582	4x00119		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter4	0583	4x00120		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter5	0584	4x00121		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter6	0585	4x00122		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter7	0586	4x00123		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter8	0587	4x00124		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	Default value	Command or setting	Min	Max	Step	Password level	P341	P342	P343	P344	P345	P346
Reset Counter9	0588	4x00125		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter10	0589	4x00126		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter11	058A	4x00127		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter12	058B	4x00128		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter13	058C	4x00129		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter14	058D	4x00130		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter15	058E	4x00131		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*
Reset Counter16	058F	4x00132		G11	1	No	Command	0	1	1	1	*	*	*	*	*	*

Table 7: Control (commands) available in the P341-6 product range

4.11 Event extraction

The product can store up to 512 event records in battery backed-up memory. An event record consists of a time stamp, a record type, and a set of information fields. The record type and the information fields record the event that occurred at the time captured by the time stamp.

The product has several classes of event record:

- Alarm events
- Opto-isolated status input events
- Relay contact output events
- Protection/DDB operation events
- Fault data capture events
- General events

The Relay Menu Database document, *P34x/EN MD* specifies the available events. Note that the product provides an “event filtering” feature that may be used to prevent specific events from being logged. The event filter is configured in the “Record Control” section of the product’s menu database in the S1 Agile configuration tool.

The product supports two methods of event extraction providing either automatic or manual extraction of the stored event, fault, and maintenance records.

It is important to appreciate that the product stores event, fault, and maintenance records in three separate queues. As entries are added to the fault and maintenance queues a corresponding event is added to the event queue. Each queue is of different length and each queue may be individually cleared (see section 4.11.4). It is therefore possible to have a fault event or a maintenance event entry in the event queue with no corresponding entry in the associated queue because it has been overwritten or deleted.

The manual extraction procedure (section 4.11.1) allows each of these three queues to be read independently.

The automatic extraction procedure (section 4.11.2) reads records from the event queue. If the event record is either a fault or a maintenance record then the records extended data is read too, if it is available from their queues.

Note: Version 31 of the product introduced a new set of 3x registers for the presentation of the event and fault record data. These registers are used

throughout the text of the following sub-sections. For legacy compatibility, the original registers are still provided. These are described as previous MODBUS address in the Relay Menu Database document, *P34x/EN MD*. They should not be used for new installations. See section 4.11.5 for additional information.

4.11.1 Manual extraction procedure

There are three registers available to manually select stored records, there are also three read only registers allowing the number of stored records to be determined.

4x00100 - Select Event, 0 to 511[8]

4x00101 - Select Fault, 0 to 4

4x00102 - Select Maintenance Record, 0 to 4

For each of the above registers, a value of zero represents the most recent stored record. The following registers can be read to indicate the numbers of the various types of record stored.

The values in the following registers indicate the number of each type of record stored.

3x10000 - Number of stored event records

3x10001 - Number of stored fault records

3x10002 - Number of stored maintenance records

Each fault or maintenance record logged causes an event record to be created by the product. If this event record is selected the additional registers showing the fault or maintenance record details will also become populated.

4.11.2 Automatic extraction procedure

Automatic event-record extraction allows records to be extracted as they occur. Event records are extracted in sequential order, including any fault or maintenance data that may be associated with an event.

The MODBUS master can determine whether the product has any events stored that have not yet been extracted. This is done by reading the product's status register 3x00001 (G26 data type). If the event bit, of this register, is set then the product contains event records that have not yet been extracted.

To select the next event for sequential extraction, the master station writes a value of one to the record selection register 4x00400 (G18 data type). The event data together with any fault/maintenance data can be read from the registers specified in 4.11.3. Once the data has been read, the event record can be marked as having been read by writing a value of two to register 4x00400. Alternatively, since the G18 data type consists of bit fields, it is possible to both mark the current record as having been read and to automatically select the next unread record by writing a value of three to the register.

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When the last (most recent) record has been accepted the event flag in the status register (3x00001) will reset. If the last record was accepted, by writing a value of three to the record selection register (4x00400), then a dummy record will appear in the event-record registers, with an "Event Type" value of 255. Attempting to select another record, when none are available will result in a MODBUS exception code 3 - "Invalid value" (see section 4.3).

One possible event record extraction procedure is illustrated in Figure 6.

[8] This was 249 in P340 software revisions 01, 02, 03, 04, 05, 06, & 07, since they only stored 250 event records.

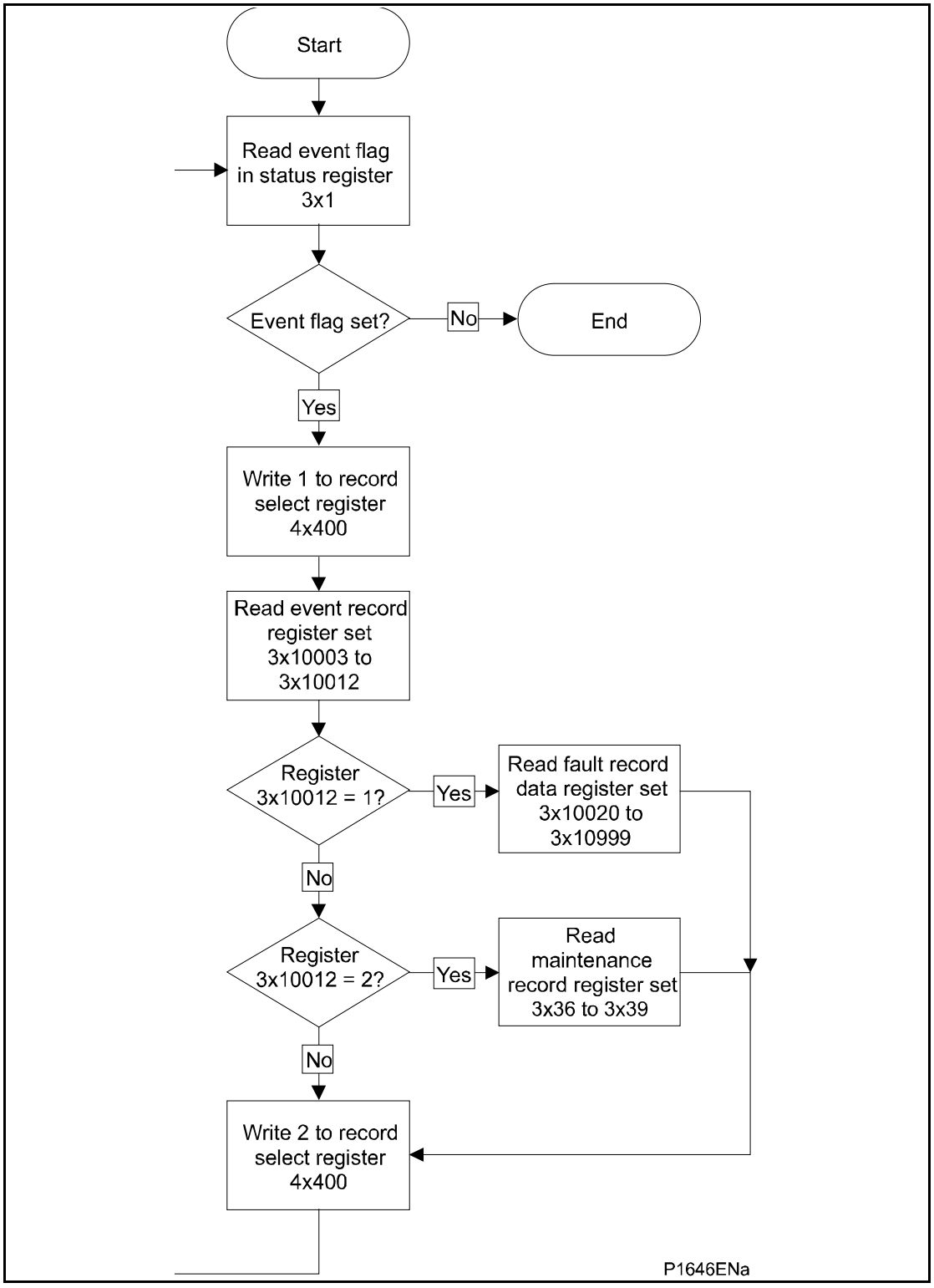


Figure 6: Automatic event extraction procedure

4.11.3 Record data

The location and format of the registers used to access the record data is the same whether they have been selected using manual or automatic extraction mechanisms detailed above.

Description	Register	Length (registers)	Comments
Time Stamp	3x10003	4	See G12 data type the Relay Menu Database document, *P34x/EN MD*.
Event Type	3x10007	1	Indicates the type of the event record. See G13 data type in the Relay Menu Database document, *P34x/EN MD* (additionally, a value of 255 indicates that the end of the event log has been reached).
Event Value	3x10008	2	Contains the associated status register value, as a string of binary flags, for relay-contact, opto-input, alarm, and protection events. Otherwise, it will have a value of zero. When a status value is supplied, the value represents the recorded value of the event types associated register pair, as indicated by the Event Origin value. [9]
Event Origin	3x10010	1	The Event Original value indicates the MODBUS Register pair where the change occurred. [10] Possible values are: 11 (3x00011): Alarm Status 1 event 13 (3x00013): Alarm Status 2 event 15 (3x00015: Alarm Status 3 event 23 (3x11023): Relay contact event (2 registers: DDB 0-31 status) 25 (3x11025): Status input event (2 registers: DDB 32-63 status) 27 to 85 (3x11027 – 3x11085): Protection events (Indicates the 32 bit DDB status word that was the origin of the event) For General events, Fault events, and Maintenance events a value of zero will be returned.
Event Index	3x10011	1	The Event Index value is used to distinguish between events with the same Event Type and Event Origin. The registers value depends on the type of the event: For protection events, the value is the ID of the DDB that caused the event. For alarm events, the value is the ID of the alarm that caused the event. In both cases, the value includes the direction of the state transition in the most significant bit. This direction bit is 1 for a 0-1 (low to high) change, and 0 for a 1-0 (high to low) change. For all other types of events, it will have a value of zero.

[9] The protection-event status information is the value of the DDB status word that contains the protection DDB that caused the event.

[10] Subtracting 3000 from the Event Origin value results in the MODBUS 3x memory-page register ID, subtracting one from this results in the MODBUS register address - see section 4.5.1.2. The resultant register address can be used in a function code 4 MODBUS query.

Description	Register	Length (registers)	Comments
Additional Data Present	3x10012	1	Indicates whether the record has additional data. 0: Indicates that there is no additional data. 1: Indicates that fault record data can be read from 3x10020 to 3x10999. [11] 2: Indicates that maintenance record data can be read from registers 3x36 to 3x39.

Table 8: Event record extraction registers

If a fault record or maintenance record is directly selected using the manual mechanism, then the data can be read from the fault or maintenance data register ranges specified above. The event record data in registers 3x10003 to 3x10012 will not be valid.

See the Relay Menu Database document, *P34x/EN MD* for the record values for each event.

The general procedure for decoding an event record is to use the value of the "Event Type" field combined with the value of the "Event Index" field to uniquely identify the event. The exceptions to this are event types 4, 5, 7, 8, & 9.

Event types 4 "Relay Contact Output Events" and 5 "Opto-Isolated Status Input Events" only provide the value of the input or output status register (as indicated by the Event Origin value) at the time the event occurred. If event transition information for each input or output is required then this must be deduced by comparing the event value with the previous event value (for identically typed events records).

Event type 7 "General Event" events are solely identified by their "Event Value".

Event types 8 "Fault Record" and 9 "Maintenance Record" require additional registers to be read when the associated additional data is available. [12] The Fault record registers in the range 3x10020 to 3x10999 (the exact number of registers depends on the individual product) are clearly documented in the 3x register-map in the Relay Menu Database document, *P34x/EN MD.* The two additional 32-bit maintenance record register-pairs consist of a maintenance record type (register pair 3x36/7) and a type-specific error code (register pair 3x38/9). Table 9 lists the different types of maintenance record available from the product.

Maintenance record	Front panel text	Record type 3x00036
Power on test errors (non-fatal)		
Watchdog 1 failure (fast)	Fast W'Dog Error	0
Battery fail	Battery Failure	1
Battery-backed RAM failure	BBRAM Failure	2
Field voltage failure	Field Volt Fail	3
Ribbon bus check failure	Bus Reset Error	4
Watchdog 2 failure (slow)	Slow W'Dog Error	5
Continuous self-test errors		
SRAM bus failure	SRAM Failure Bus	6
SRAM cell failure	SRAM Failure Blk.	7
Flash EPROM checksum failure	FLASH Failure	8
Program code verify failure	Code Verify Fail	9
Battery-backed RAM failure	BBRAM Failure	10
Battery fail	Battery Failure	11
Field Voltage failure	Field Volt Fail	12
EEPROM failure	EEPROM Failure	13

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[11] The exact number of fault record registers depends on the individual product - see Relay Menu Database, *P34x/EN MD.*

[12] At the beginning of section 4.11, it should not be assumed that the additional data will be available for fault and maintenance record events.

Maintenance record	Front panel text	Record type 3x00036
Fatal software exception	Software Failure	14
Incorrect hardware configuration	H/W Verify Fail	15
Software exception (typically non-fatal)	Non Standard	16
Analog module failure	Ana. Sample Fail	17
Ethernet card error	NIC Soft Error	18

Table 9: Maintenance record types

4.11.4 Event record deletion

It is possible to independently delete ("clear") the stored event, fault, and maintenance record queues. This is done by writing a value of 1, 2, or 3 to register 4x401 (G6 data type), respectively.

This register also provides an option to reset the product's front panel indications, which has the same effect as pressing the front panel "Clear" key when viewing alarm indications using the front panel user interface. This is accomplished by writing a value of 4 to register 4x401.

See also section 4.12.4 for details about deleting disturbance records.

4.11.5 Legacy event record support

Version 31 of the P34x product introduced a new set of 3x registers for the presentation of the event and fault record data. For legacy compatibility, the original registers are supported and are described in this section. They should not be used for new installations and they are correspondingly described as previous MODBUS address in the 3x-register table in the Relay Menu Database document, *P34x/EN MD*.

Table 10: provides a mapping between the obsolete event record 3x-registers and the registers used in the event record discussions in the prior sub-sections.

The obsolete fault record data between registers 3x113 and 3x199, and 3x490 and 3x499, now exists between registers 3x10020 and 3x10999. In comparison with the obsolete fault record data, the data between registers 3x10020 and 3x10999 is ordered (slightly) differently and it contains new data values. These new values (since version 31 of the product) are not available in the obsolete fault-record register sets.

The maintenance-record registers 3x36 to 3x39 remain unaffected by this evolution.

Description	Obsolete register	Length (registers)	Corresponds to register
Number of stored event records	3x00100	1	3x10000
Number of stored fault records	3x00101	1	3x10001
Number of stored maintenance records	3x00102	1	3x10002
Time Stamp	3x00103	4	3x10003
Event Type	3x00107	1	3x10007
Event Value	3x00108	2	3x10008
Event Origin	3x00110	1	3x10010
Event Index	3x00111	1	3x10011
Additional Data Present	3x00112	1	3x10012

Table 10: Correspondence of obsolete event record 3x registers with their counterparts

4.12 Disturbance record extraction

The product provides facilities for both manual and automatic extraction of disturbance records. The two methods differ only in the mechanism for selecting a disturbance record, the method for extracting the data and the format of the data are identical. Note that the record format and extraction procedures have changed for version “20” of the product software and are not compatible with prior versions.

Records extracted are presented in IEEE COMTRADE format. This involves extracting two files: an ASCII text configuration file, and a binary data file.

Each file is extracted by repeatedly reading a data-page until all of the file’s data has been transferred. The data-page is made up of 127 registers; providing a maximum of 254 bytes per register block request.

4.12.1 Interface registers

The following set of registers is presented to the master station to support the extraction of uncompressed disturbance records:

Register	Name	Description
3x00001	Status register	Provides the status of the product as bit flags: b0 - Out of service b1 - Minor self test failure b2 - Event b3 - Time synchronization b4 - Disturbance b5 - Fault b6 - Trip b7 - Alarm b8 to b15 - Unused A ‘1’ in bit “b4” indicates the presence of one or more disturbance records.
3x00800	Number of stored disturbances	Indicates the total number of disturbance records currently stored in the product, both extracted and unextracted.
3x00801	Unique identifier of the oldest disturbance record	Indicates the unique identifier value for the oldest disturbance record stored in the product. This is an integer value used in conjunction with the ‘Number of stored disturbances’ value to calculate a value for manually selecting records.
4x00250	Manual disturbance record selection register	This register is used to manually select disturbance records. The values written to this cell are an offset of the unique identifier value for the oldest record. The offset value, which ranges from 0 to the No of stored disturbances - 1, is added to the identifier of the oldest record to generate the identifier of the required record.
4x00400	Record selection command register	This register is used during the extraction process and has a number of commands. These are: b0 - Select next event b1 - Accept event b2 - Select next disturbance record b3 - Accept disturbance record b4 - Select next page of disturbance data b5 - Select data file
3x00930 to 3x00933	Record time stamp	These registers return the timestamp of the disturbance record.
3x00802	Number of registers in data page	This register informs the master station of the number of registers in the data page that are populated.
3x00803 to 3x00929	Data page registers	These 127 registers are used to transfer data from the product to the master station.

Register	Name	Description
3x00934	Disturbance record status register	The disturbance record status register is used during the extraction process to indicate to the master station when data is ready for extraction. See next table.
4x00251	Data file format selection	This is used to select the required data file format. This is reserved for future use.

Table 11: Disturbance record extraction registers

The Disturbance Record status register will report one of the following values:

State		Description
Idle		This will be the state reported when no record is selected; such as after power on or after a record has been marked as extracted.
Busy		The product is currently processing data.
Page ready		The data page has been populated and the master can now safely read the data.
Configuration complete		All of the configuration data has been read without error.
Record complete	4	All of the disturbance data has been extracted.
Disturbance overwritten	5	An error occurred during the extraction process where the disturbance being extracted was overwritten by a new record.
No unextracted disturbances	6	An attempt was made by the master station to automatically select the next oldest unextracted disturbance when all records have been extracted.
Not a valid disturbance	7	An attempt was made by the master station to manually select a record that did not exist in the product.
Command out of sequence	8	The master station issued a command to the product that was not expected during the extraction process.

Table 12: Disturbance record status register (3x934) values

4.12.2 Extraction procedure

The following procedure must be used to extract disturbance records from the product. The procedure is split into four sections:

9. Selection of a disturbance - either manually or automatically
10. Extraction of the configuration file
11. Extraction of the data file
12. Accepting the extracted record (automatic extraction only)

4.12.2.1 Manual extraction procedure

The procedure used to extract a disturbance manually is shown in the diagram below. The manual method of extraction does not allow for the acceptance of disturbance records.

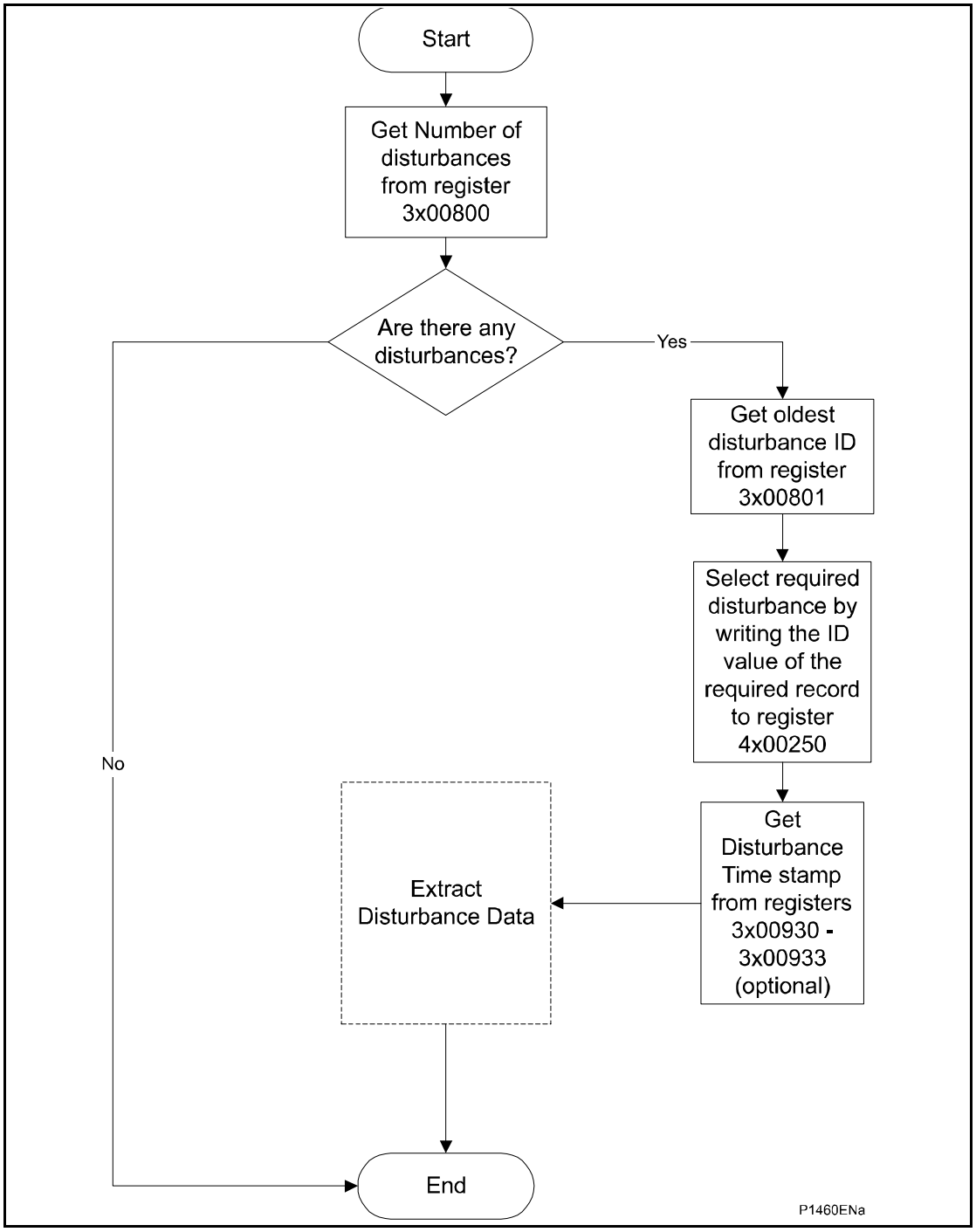


Figure 7: Manual selection of a disturbance record

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4.12.2.2 Automatic extraction procedure - option 1

There are two methods that can be used for automatically extracting disturbances. The procedure for the first method is shown below. This also shows the acceptance of the disturbance record once the extraction is complete.

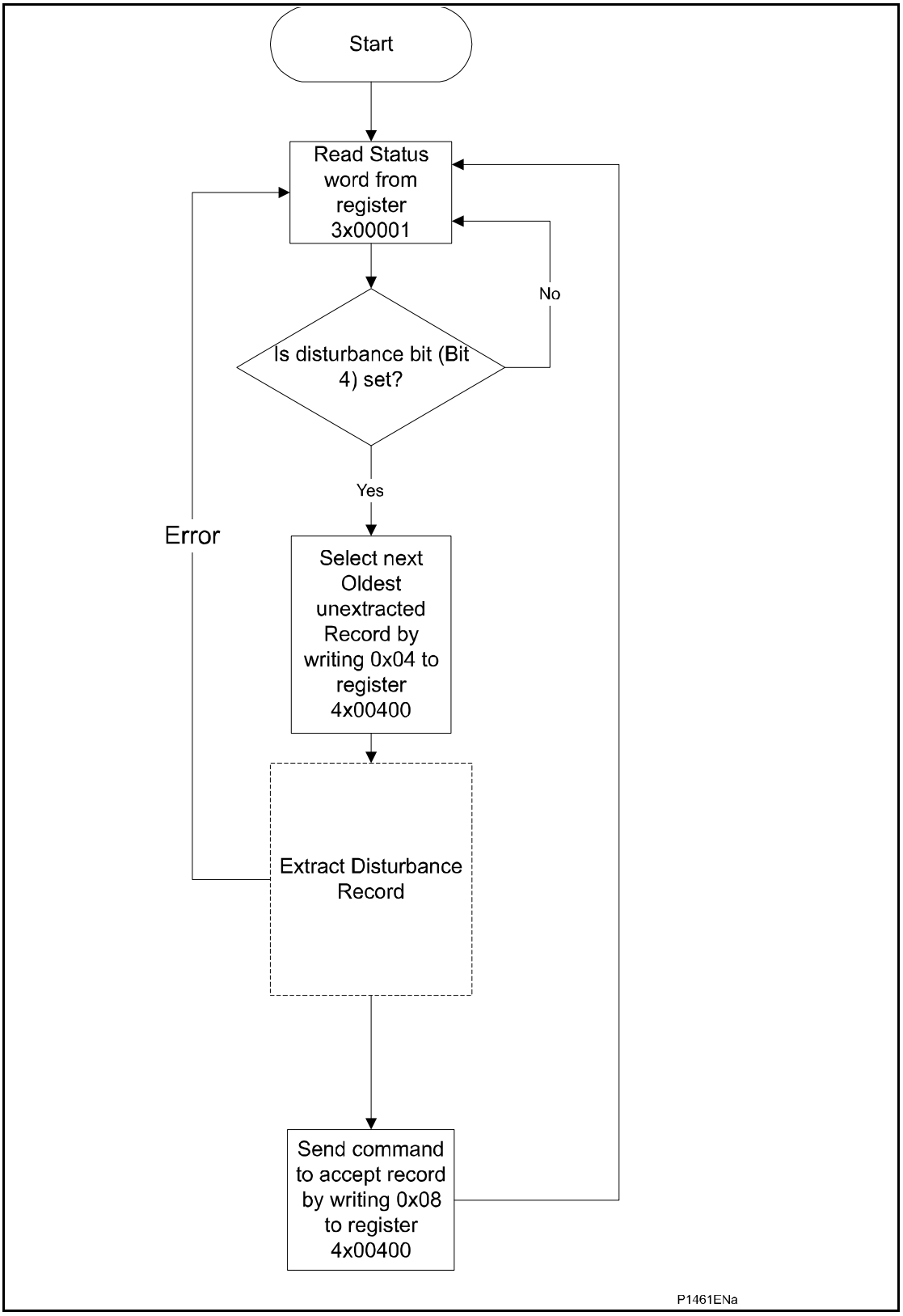


Figure 8: Automatic selection of a disturbance - option 1

4.12.2.3 Automatic extraction procedure - option 2

The second method that can be used for automatic extraction is shown in the diagram below. This also shows the acceptance of the disturbance record once the extraction is complete.

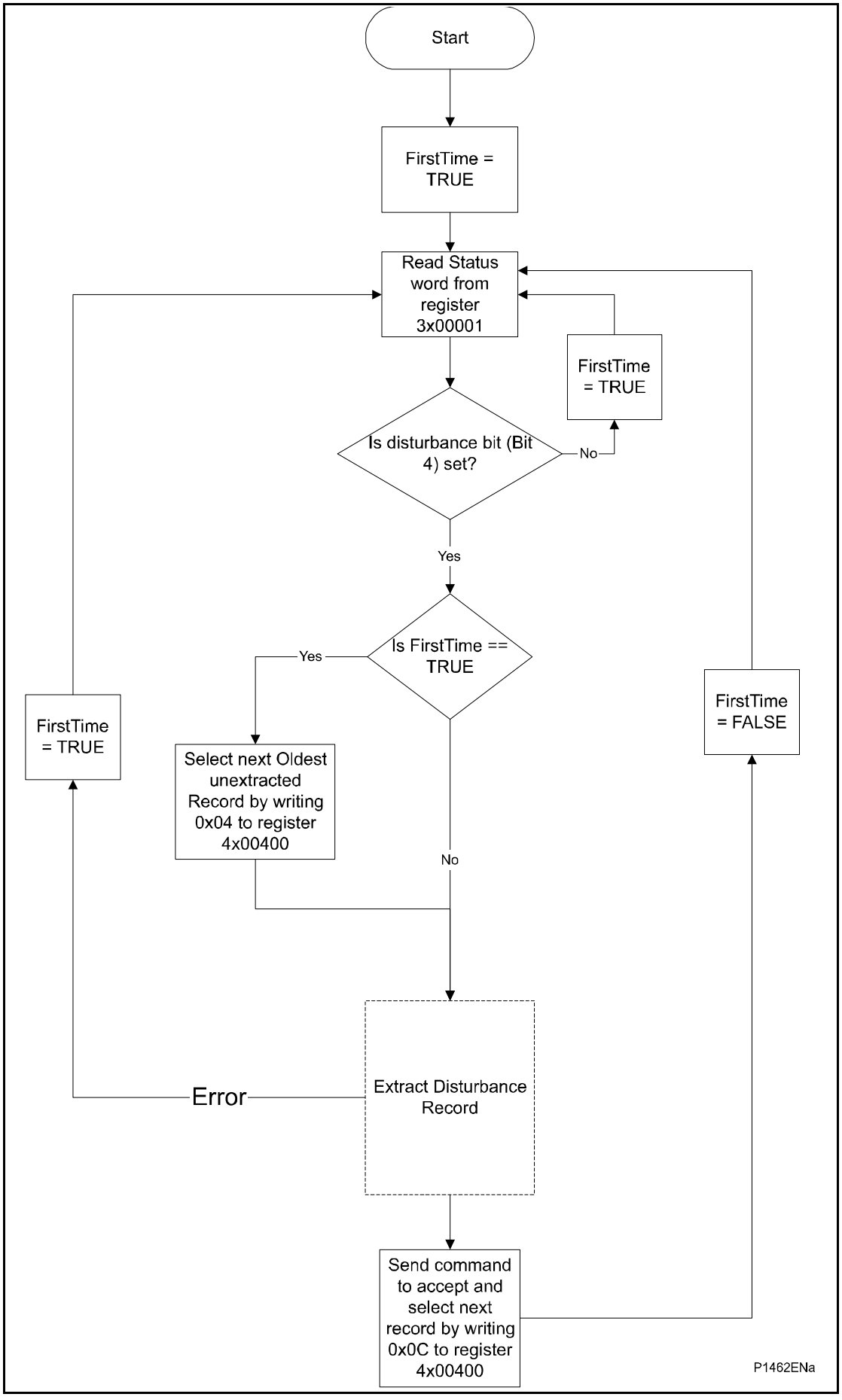


Figure 9: Automatic selection of a disturbance - option 2

4.12.2.4 Extracting the disturbance data

Extraction of a selected disturbance record is a two-stage process. This involves first reading the configuration file, then the data file. Figure 10 shows how the configuration file is extracted.

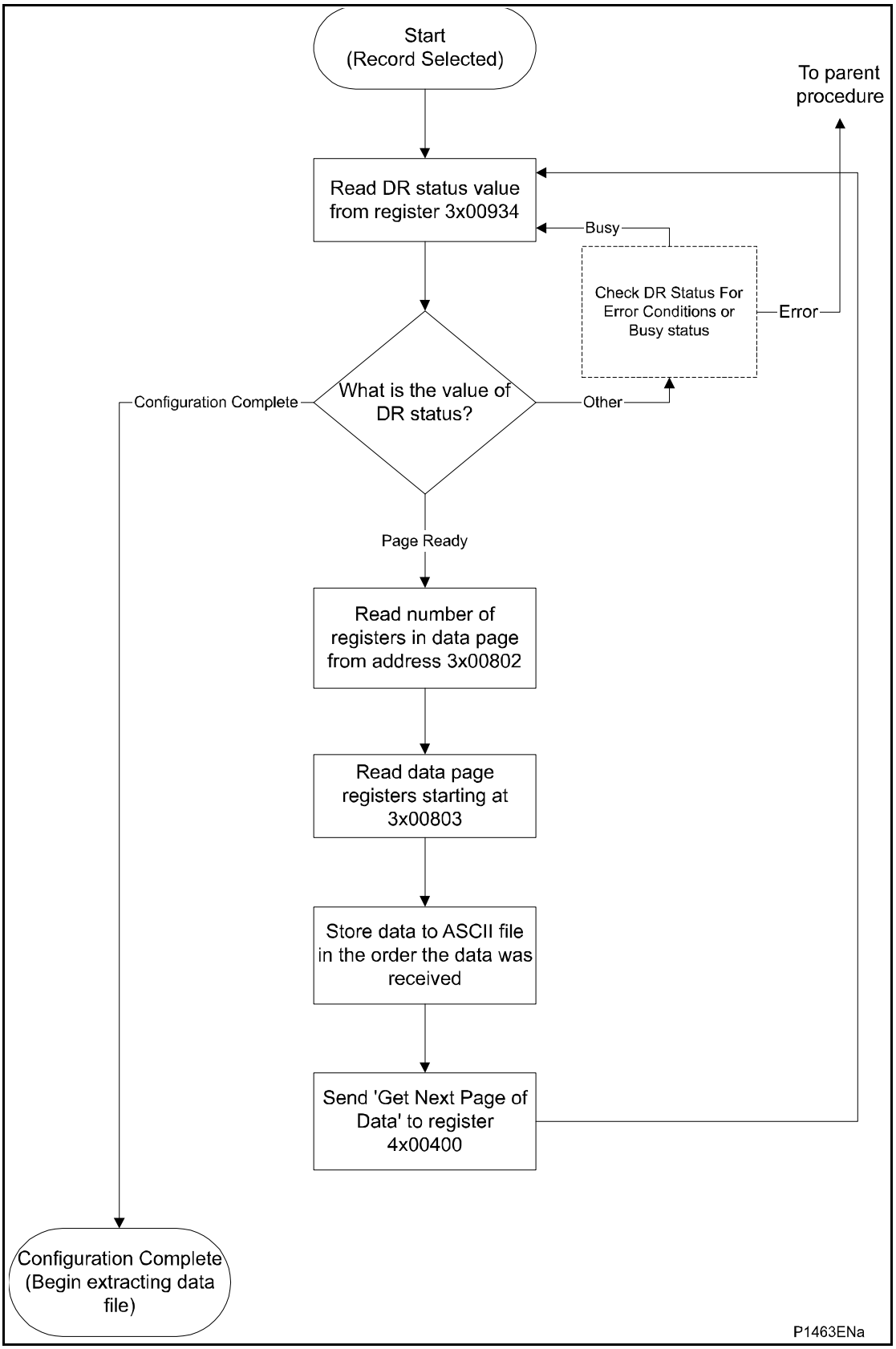


Figure 10: Extracting the COMTRADE configuration file

The following diagram shows how the data file is extracted:

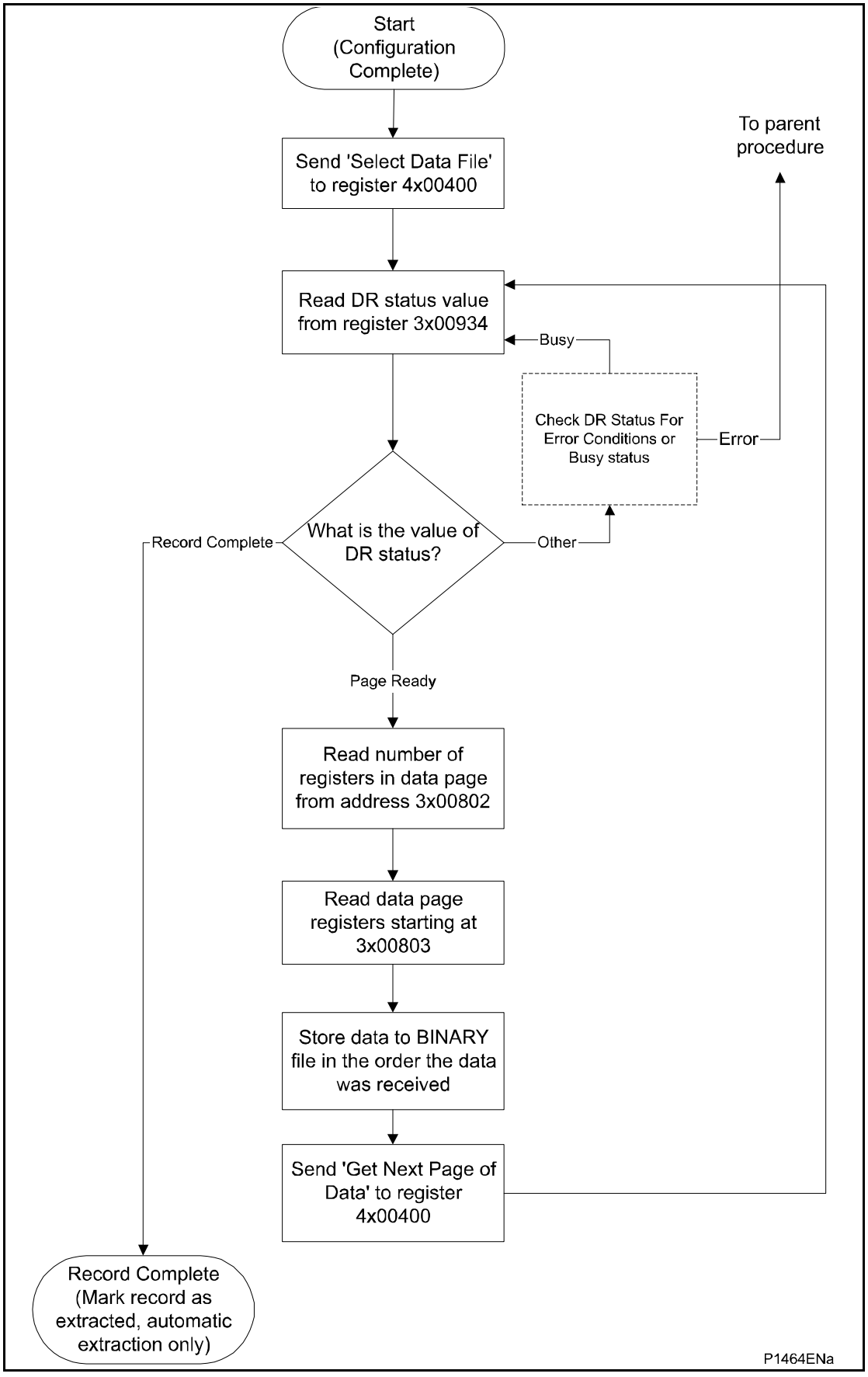


Figure 11: Extracting the COMTRADE binary data file

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During the extraction of a COMTRADE file, an error may occur that is reported in the disturbance record status register, 3x934. This can be caused by the product overwriting the record that is being extracted. It can also be caused by the master issuing a command that is not in the bounds of the extraction procedure.

4.12.3 Storage of extracted data

The extracted data needs to be written to two separate files. The first is the configuration file, which is in ASCII text format, and the second is the data file, which is in a binary format.

4.12.3.1 Storing the configuration file

As the configuration data is extracted from the product, it should be stored to an ASCII text file with a '.cfg' file extension. Each register in the page is a G1 format 16-bit unsigned integer that is transmitted in big-endian byte order. The master must write the configuration file page-data to the file in ascending register order with each register's high order byte written before its low order byte, until all the pages have been processed.

4.12.3.2 Storing the binary data file

As the binary data is extracted from the product, it should be stored to a binary file with the same name as the configuration file, but with a '.dat' file extension instead of the '.cfg' extension. Each register in the page is a G1-format 16-bit unsigned integer that is transmitted in big-endian byte order. The master must write the page data to a file in ascending register order with each register's high order byte written before its low order byte until all the pages have been processed.

4.12.4 Disturbance record deletion

All of the disturbance records stored in the product can be deleted ("cleared") by writing 5 to the record control register 4x401 (G6 data type). See also section 4.11.4 for details about event record deletion.

4.13 Setting changes

The product settings can be split into two categories:

- Control and support settings
- Disturbance record settings and protection setting groups

Changes to settings in the control and support area are executed immediately. Changes to the protection setting groups or the disturbance recorder settings are stored in a temporary 'scratchpad' area and must be confirmed before they are implemented. All the product settings are 4x page registers (see the Relay Menu Database document, *P34x/EN MD*). The following points should be noted when changing settings:

- Settings implemented using multiple registers must be written to using a multi-register write operation. The product does not support write access to sub-parts of multi-register data types.
- The first address for a multi-register write must be a valid address. If there are unmapped addresses within the range being written to then the data associated with these addresses will be discarded.
- If a write operation is performed with values that are out of range then an "illegal data" response code will be produced. Valid setting values within the same write operation will be executed.
- If a write operation is performed attempting to change registers that require a higher level of password access than is currently enabled then all setting changes in the write operation will be discarded.

4.13.1 Password protection

The product's settings can be subject to Password protection. The level of password protection required to change a setting is indicated in the 4x register-map table in the Relay

Menu Database document, *P34x/EN MD*. Level 2 is the highest level of password access, level 0 indicates that no password is required.

The following registers are available to control Password protection:

- 4x00001 & 4x00002 Password Entry
- 4x00022 Default Password Level
- 4x00023 & 4x00024 Setting to Change Password Level 1
- 4x00025 & 4x00026 Setting to Change Password Level 2
- 3x00010 Current Access Level (read only)

4.13.2 Control and support settings

Control and support settings are committed immediately when a value is written to such a register. The MODBUS registers in this category are:

- 4x00000-4x00599
- 4x00700-4x00999
- 4x02049 to 4x02052
- 4x10000-4x10999

4.13.2.1 Time synchronization

The value of the product's real time clock can be set by writing the desired time (see section 4.16) to registers 4x02049 through 4x02052. These registers are standard to MiCOM products, which makes it easier to broadcast of a time synchronization packet -being a block write to the time setting registers sent to slave address zero.

When the product's time has been set using these registers the Time Synchronized flag in the MODBUS Status Register (3x1: type G26) will be set. The product automatically clears this flag if more than five minutes has elapsed since these registers were last written to.

A "Time synchronization" event will be logged if the new time value is more than two seconds different from the current value.

4.13.3 Disturbance recorder configuration settings

Disturbance recorder configuration-settings are written to a scratchpad memory area. A confirmation procedure is required to commit the contents of the scratchpad to the disturbance recorder's set-up, which ensures that the recorders configuration is consistent at all times. The contents of the scratchpad memory can be discarded with the abort procedure. The scratchpad confirmation and abort procedures are described in section 4.13.5.

The disturbance recorder configuration registers are in the range:

- 4x00600-4x00699

4.13.4 Protection settings

Protection configuration-settings are written to a scratchpad memory area. A confirmation procedure is required to commit the contents of the scratchpad to the product's protection functions, which ensures that their configuration is consistent at all times. The contents of the scratchpad memory can be discarded with the abort procedure. The scratchpad confirmation and abort procedures are described in section 4.13.5.

The product supports four groups of protection settings. One protection-group is active and the other three are either dormant or disabled. The active protection-group can be selected by writing to register 4x00404. An illegal data response will be returned if an attempt is made to set the active group to one that has been disabled.

The MODBUS registers for each of the four groups are repeated within the following ranges:

- Group 1 4x01000-4x02999, 13 4x11000-4x12999
- Group 2 4x03000-4x04999, 4x13000-4x14999
- Group 3 4x05000-4x06999, 4x15000-4x16999
- Group 4 4x07000-4x08999, 4x17000-4x18999

4.13.5 Scratchpad management

Register 4x00405 can be used to either confirm or abort the setting changes in the scratchpad area. In addition to the basic editing of the protection setting groups, the following functions are provided:

- Default values can be restored to a setting group or to all of the product settings by writing to register 4x00402.
- It is possible to copy the contents of one setting group to another by writing the source group to register 4x00406 and the target group to 4x00407.
- It should be noted that the setting changes performed by either of the two operations defined above are made to the scratchpad area. These changes must be confirmed by writing to register 4x00405.

4.14 Register data types

The product maps one or more MODBUS registers to data-typed information contained within an internal database. These data-types are referred to as G-Types since they have a 'G' prefixed identifier. The Relay Menu Database document, *P34x/EN MD* gives a complete definition of the all of the G-Types used in the product.

Generally, the data types are transmitted in high byte to low byte order, also known as "Big Endian format". This may require the MODBUS master to reorder the received bytes into a format compliant with its byte-order and register order (for multi-register G-Types) conventions. Most MODBUS masters provide byte-swap and register-swap device (or data point) configuration to cope with the plethora of implementations.

The product's data-types are atomic in nature. This means that the multi-register types cannot be read (or written) on an individual register basis. All of the registers for a multi-register data-typed item must be read (or written) with a single block read (or write) command.

The following subsections provide some additional notes for a few of the more complex G-Types.

4.15 Numeric setting (data types G2 & G35)

Numeric settings are integer representations of real (non-integer) values. The register value is the number of setting increments (or steps) that the real value is away from the settings real minimum value. This is expressed by the following formula:

$S^{real} = S^{min.} + (S^{inc.} \times S^{numeric})$

Where:

- S^{real} - Setting real value
- $S^{min.}$ - Setting real minimum value
- $S^{inc.}$ - Setting real increment (step) value
- $S^{numeric}$ - Setting numeric (register) value

13 Note that registers 4x02049 to 4x02052 are not part of protection setting group #1 and therefore do not repeat in any of the other protection setting groups. These registers are for time synchronization purposes and are standard for most General Electric products. See section 4.13.2.1.

For example, a setting with a real value setting range of 0.01 to 10 in steps of 0.01 would have the following numeric setting values:

Real value (S_{real})	Numeric value ($S_{numeric}$)
0.01	0
0.02	1
1.00	99

Table 13: Numeric values

The G2 numeric data type uses 1 register as an unsigned 16-bit integer, whereas the G35 numeric data type uses 2 registers as an unsigned 32-bit integer. The G2 data type therefore provides a maximum setting range of 2^{16} x S_{inc}. Similarly the G35 data type provides a maximum setting range of 2^{32} x $S_{inc.}$

4.16 Date and time format (data type G12)

The date-time data type G12 allows real date and time information to be conveyed down to a resolution of 1 ms. The data-type is used for record time-stamps and for time synchronization (see section 4.13.2.1).

The structure of the data type is shown in Table 14 and is compliant with the IEC 60870-5-4 “Binary Time 2a” format.

Byte	Bit position							
	7	6	5	4	3	2	1	0
1	m7	m6	m5	m4	m3	m2	m1	m0
2	m15	m14	m13	m12	m11	m10	m9	m8
3	IV	R	I5	I4	I3	I2	I1	I0
4	SU	R	R	H4	H3	H2	H1	H0
5	W2	W1	W0	D4	D3	D2	D1	D0
6	R	R	R	R	M3	M2	M1	M0
7	R	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Table 14: G12 date & time data type structure

Where:

- m = 0…59,999ms
- I = 0…59 minutes
- H = 0…23 Hours
- W = 1…7 Day of week; Monday to Sunday, 0 for not calculated
- D = 1…31 Day of Month
- M = 1…12 Month of year; January to December
- Y = 0…99 Years (year of century)
- R = Reserved bit = 0
- SU = Summertime: 0=standard time, 1=summer time
- IV = Invalid value: 0=valid, 1=invalid
- range = 0ms…99 years

The seven bytes of the structure are packed into four 16-bit registers. Two packing formats are provided: standard and reverse. The prevailing format is selected by the G238 setting in the "Date and Time" menu column or by register 4x306. [14]

The standard packing format is the default and complies with the IEC 60870-5-4 requirement that byte 1 is transmitted first, followed by byte 2 through to byte 7, followed by a null (zero) byte to make eight bytes in total. Since register data is usually transmitted in big-endian format (high order byte followed by low order byte), byte 1 will be in the high-order byte position followed by byte 2 in the low-order position for the first register. The last register will contain just byte 7 in the high order position and the low order byte will have a value of zero.

The reverse packing format is the exact byte transmission order reverse of the standard format. That is, the null (zero) byte is sent as the high-order byte of the first register and byte 7 as the register's low-order byte. The second register's high-order byte contains byte 6 and byte 5 in its low order byte.

Both packing formats are fully documented in the Relay Menu Database document, *P34x/EN MD* for the G12 type.

The principal application of the reverse format is for date-time packet format consistency when a mixture of different manufacturers products are being used. This is especially true when there is a requirement for broadcast time synchronization with a mixture of products.

The data type provides only the year of century value; the century must be deduced. Simplistically the century could be imposed as 20 for applications not dealing with dates stored in this format from the previous (20th) century. Alternatively, the century can be calculated as the one that will produce the nearest time value to the current date. For example: 30-12-99 is 30-12-1999 when received in 1999 & 2000, but is 30-12-2099 when received in 2050. This technique allows 2 digit years to be accurately converted to 4 digits in a ±50 year window around the current datum.

The invalid bit has two applications:

13. It can indicate that the date-time information is considered inaccurate, but is the best information available.
14. Date-time information is not available.

The summertime bit is used to indicate that summertime (day light saving) is being used and, more importantly, to resolve the alias and time discontinuity which occurs when summertime starts and ends. This is important for the correct time correlation of time stamped records. (Note that the value of the summertime bit does not affect the time displayed by the product).

The day of the week field is optional and if not calculated will be set to zero.

The data type (and therefore the product) does not cater for the time zones so the end user must determine the time zone used by the product. UTC (universal coordinated time), is commonly used and avoids the complications of daylight saving timestamps.

4.17 Power and energy measurement data formats (G29 & G125)

The power and energy measurements are available in two data formats, G29 integer format and G125 IEEE754 floating point format. The G125 format is to be preferred over the older G29 format.

4.17.1 Data type G29

Data type G29 consists of three registers. The first register is the per unit power or energy measurement and is of type G28, which is a signed 16-bit quantity. The second and third registers contain a multiplier to convert the per unit value to a real value.

14 Note that this menu cell does not exist in P340 software revisions 01, 02, 03, 04, 05, 06, & 07. Maintenance revisions after software versions 03H, 04J, 05J, 06D and 07D will include just the time format selection register 4x306. Versions prior to this use just the standard time format.

The multiplier is of type G27, which is an unsigned 32-bit quantity. Therefore, the overall value conveyed by the G29 data type must be calculated as G29=G28×G27.

The product calculates the G28 per unit power or energy value as G28=((measured secondary quantity)/(CT secondary) × (110 V/(VT secondary)). Since data type G28 is a signed 16-bit integer, its dynamic range is constrained to ±32768. This limitation should be borne in mind for the energy measurements, as the G29 value will saturate a long time before the equivalent G125 does.

The associated G27 multiplier is calculated as G27=(CT primary) × (VT primary/110 V) when primary value measurements are selected, and as G27=(CT secondary) × (VT secondary/110 V) when secondary value measurements are selected.

Due to the required truncations from floating point values to integer values in the calculations of the G29 component parts and its limited dynamic range, the use of the G29 values is only recommended when the MODBUS master cannot deal with the G125 IEEE754 floating point equivalents.

Note: The G29 values must be read in whole multiples of three registers. It is not possible to read the G28 and G27 parts with separate read commands.

Example:

For A-Phase Power (Watts) (registers 3x00300 - 3x00302) for a 110 V nominal, In = 1A, VT ratio = 110V:110 V and CT ratio = 1A:1A.
Applying A-phase 1A @ 63.51 V
A-phase Watts = ((63.51 V × 1A) / In=1A) × (110/Vn=110 V) = 63.51 Watts
The G28 part of the value is the truncated per unit quantity, which will be equal to 64 (40h).
The multiplier is derived from the VT and CT ratios set in the product, with the equation ((CT Primary) × (VT Primary) / 110 V)). Therefore, the G27 part of the value will equal 1.
Hence the overall value of the G29 register set is 64×1 = 64 W.
The registers would contain:

3x00300 - 0040h
3x00301 - 0000h
3x00302 - 0001h

Using the previous example with a VT ratio = 110,000 V:110 V and CT ratio = 10,000A : 1A the G27 multiplier would be 10,000A×110,000 V/110 = 10,000,000. The overall value of the G29 register set is 64 × 10,000,000 = 640 MW. (Note that there is an actual error of 49 MW in this calculation due to loss of resolution).
The registers would contain:

3x00300 - 0040h
3x00301 - 0098h
3x00302 - 9680h

4.17.2 Data type G125

Data type G125 is a short float IEEE754 floating point format, which occupies 32-bits in two consecutive registers. The most significant 16-bits of the format are in the first (low order) register and the least significant 16-bits in the second register.

The value of the G125 measurement is as accurate as the product's ability to resolve the measurement after it has applied the secondary or primary scaling factors as required. It does not suffer from the truncation errors or dynamic range limitations associated with the G29 data format.

5 IEC 60870-5-103 INTERFACE

The IEC 60870-5-103 interface is a master/slave interface with the relay as the slave device. The relay conforms to compatibility level 2; compatibility level 3 is not supported.

The following IEC 60870-5-103 facilities are supported by this interface:

- Initialization (Reset)
- Time Synchronization
- Event Record Extraction
- General Interrogation
- Cyclic Measurements
- General Commands
- Disturbance Record Extraction
- Private Codes

5.1 Physical connection and link layer

Two connection options are available for IEC 60870-5-103, either the rear EIA(RS)485 port or an optional rear fiber optic port. If the fiber optic port is fitted the active port can be selected using the front panel menu or the front Courier port, however the selection will only be effective following the next relay power up.

For either of the two modes of connection it is possible to select both the relay address and baud rate using the front panel menu/front Courier. Following a change to either of these two settings a reset command is required to re-establish communications, see reset command description below.

5.2 Initialization

Whenever the relay has been powered up, or if the communication parameters have been changed a reset command is required to initialize the communications. The relay will respond to either of the two reset commands (Reset CU or Reset FCB). However, the Reset CU clears any unsent messages in the relay's transmit buffer.

The relay responds to the reset command with an identification message ASDU 5, the Cause of Transmission COT of this response will be either Reset CU or Reset FCB depending on the nature of the reset command. The content of ASDU 5 is described in the IEC 60870-5-103 section of the Relay Menu Database document, *P34x/EN MD*.

In addition to the ASDU 5 identification message, if the relay has been powered up it will also produce a power up event.

5.3 Time synchronization

The relay time and date can be set using the time synchronization feature of the IEC 60870-5-103 protocol. The relay corrects for the transmission delay as specified in IEC 60870-5-103. If the time synchronization message is sent as a send / confirm message, the relay responds with a confirm. Whether the time-synchronization message is sent as a send / confirm or a broadcast (send / no reply) message, a time synchronization Class 1 event is generated.

If the relay clock is being synchronized using the IRIG-B input, it is not be possible to set the relay time using the IEC 60870-5-103 interface. If the time is set using the interface, the relay creates an event with the current date and time taken from the internal clock, which is synchronized to IRIG-B.

5.4 Spontaneous events

Events are categorized using the following information:

- Function Type
- Information Number

The IEC 60870-5-103 profile in the Relay Menu Database document, *P34x/EN MD*, contains a complete listing of all events produced by the relay.

5.5 General interrogation

The GI request can be used to read the status of the relay, the function numbers, and information numbers that will be returned during the GI cycle are indicated in the IEC 60870-5-103 profile in the Relay Menu Database document, *P34x/EN MD*.

5.6 Cyclic measurements

The relay will produce measured values using ASDU 9 on a cyclical basis; this can be read from the relay using a Class 2 poll (note ADSU 3 is not used). The rate at which the relay produces new measured values can be controlled using the Measurement Period setting. This setting can be edited from the front panel menu/front Courier port and is active immediately following a change.

Note: The measurands transmitted by the relay are sent as a proportion of 2.4 times the rated value of the analog value.

5.7 Commands

A list of the supported commands is contained in the Relay Menu Database document, *P34x/EN MD*. The relay will respond to other commands with an ASDU 1, with a Cause of Transmission (COT) indicating 'negative acknowledgement'.

5.8 Test mode

Using either the front panel menu or the front Courier port, it is possible to disable the relay output contacts to allow secondary injection testing to be performed. This is interpreted as 'test mode' by the IEC 60870-5-103 standard. An event will be produced to indicate both entry to and exit from test mode. Spontaneous events and cyclic measured data transmitted whilst the relay is in test mode will have a COT of 'test mode'.

5.9 Disturbance records

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC 60870-5-103.

Note: IEC 60870-5-103 only supports up to 8 records.

5.10 Blocking of monitor direction

The relay supports a facility to block messages in the Monitor direction and also in the Command direction. Messages can be blocked in the Monitor and Command directions using the menu commands, Communications - CS103 Blocking - Disabled/Monitor Blocking/Command Blocking or DDB signals Monitor Blocked and Command Blocked.

6 DNP3.0 INTERFACE

6.1 DNP3.0 protocol

The DNP3.0 protocol is defined and administered by the DNP Users Group. For Information on the user group, DNP3.0 in general and the protocol specifications, see

www.dnp.org

The descriptions given here are intended to accompany the device profile document that is included in the Relay Menu Database document, *P34x/EN MD*. The DNP3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP3.0 implementation for the relay. This is the standard format DNP3.0 document that specifies which objects; variations and qualifiers are supported. The device profile document also specifies what data is available from the relay via DNP3.0. The relay operates as a DNP3.0 slave and supports subset level 2 of the protocol, plus some of the features from level 3.

DNP3.0 communication uses the EIA(RS)485 or Ethernet communication port at the rear of the relay. When using a serial interface, the data format is 1 start bit, 8 data bits, an optional parity bit and 1 stop bit. Parity is configurable. See the Settings chapter for DNP 3.0 settings.

DNP3.0 communication uses the EIA(RS)485 communication port at the rear of the relay. The data format is 1 start bit, 8 data bits, an optional parity bit and 1 stop bit. Parity is configurable (see menu settings below).

6.2 Object 1 binary inputs

Object 1, binary inputs, contains information describing the state of signals in the relay, which mostly form part of the digital data bus (DDB). In general these include the state of the output contacts and input optos, alarm signals and protection start and trip signals. The 'DDB number' column in the device profile document provides the DDB numbers for the DNP3.0 point data. These can be used to cross-reference to the DDB definition list that is also found in the Relay Menu Database document, *P34x/EN MD*. The binary input points can also be read as change events via object 2 and object 60 for class 1-3 event data.

6.3 Object 10 binary outputs

Object 10, binary outputs, contains commands that can be operated via DNP3.0. Therefore, the points accept commands of type pulse on [null, trip, close] and latch on/off as detailed in the device profile in the Relay Menu Database document, *P34x/EN MD* and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

Due to that fact that many of the relay's functions are configurable, it may be the case that some of the object 10 commands described below are not available for operation. In the case of a read from object 10 this will result in the point being reported as off-line and an operate command to object 12 will generate an error response.

There is an additional image of the control inputs. Described as alias control inputs, they reflect the state of the control input, but with a dynamic nature.

- If the Control Input DDB signal is already SET and a new DNP SET command is sent to the Control Input, the Control Input DDB signal goes momentarily to RESET and then back to SET.
- If the Control Input DDB signal is already RESET and a new DNP RESET command is sent to the Control Input, the Control Input DDB signal goes momentarily to SET and then back to RESET.
- Figure 12 shows the behavior when the Control Input is set to Pulsed or Latched.

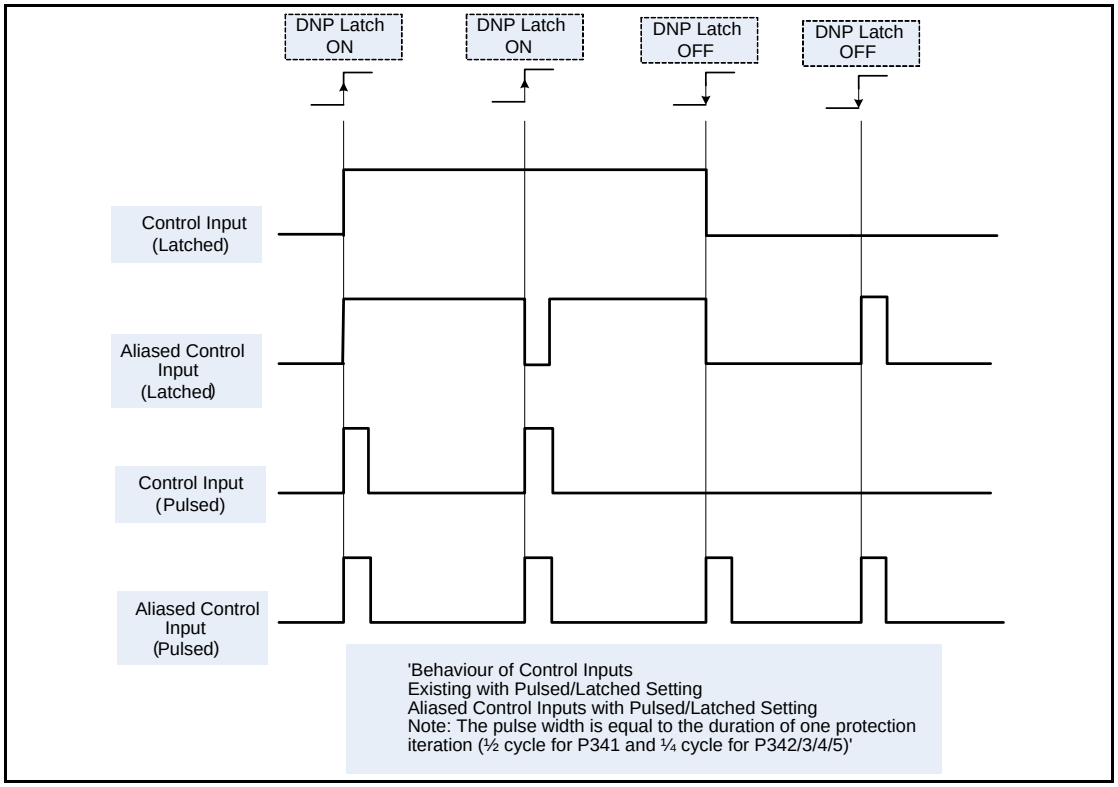


Figure 12: Behavior of control inputs

Examples of object 10 points that maybe reported as off-line are:

- Activate setting groups - Ensure setting groups are enabled
- CB trip/close - Ensure remote CB control is enabled
- Reset NPS thermal - Ensure NPS thermal protection is enabled
- Reset thermal O/L - Ensure thermal overload protection is enabled
- Reset RTD flags - Ensure RTD Inputs is enabled
- Control inputs - Ensure control inputs are enabled

6.4 Object 20 binary counters

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from object 20, or as a 'frozen' value from object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding object 21 frozen counter. The freeze and clear function resets the object 20 running counter to zero after freezing its value. Binary counter and frozen counter change event values are available for reporting from object 22 and object 23 respectively. Counter change events (object 22) only report the most recent change, so the maximum number of events supported is the same as the total number of counters. Frozen counter change events (object 23) are generated when ever a freeze operation is performed and a change has occurred since the previous freeze command. The frozen counter event queues will store the points for up to two freeze operations.

6.5 Object 30 analog input

Object 30, analog inputs, contains information from the relay's measurements columns in the menu. All object 30 points can be reported as 16 or 32 bit integer values with flag, 16 or 32 bit integer without flag as well as short floating-point values. Analogue values can be reported to the master station as primary, secondary or normalized values (which takes into account the relay's CT and VT ratios) and this is settable in the DNP3.0 Communications Column in the relay. Corresponding deadband settings can be displayed in terms of a primary, secondary or normalized value. Deadband point values can be reported and written using Object 34 variations. The deadband is the setting used to determine whether a change

event should be generated for each point. The change events can be read via object 32 or object 60 and will be generated for any point whose value has changed by more than the deadband setting since the last time the data value was reported.

Any analog measurement that is unavailable at the time it is read will be reported as offline, e.g. the frequency when the current and voltage frequency is outside the tracking range of the relay or the thermal state when the thermal protection is disabled in the configuration column.

6.6 Object 40 analog output

The conversion to fixed-point format requires the use of a scaling factor, which is configurable for the various types of data within the relay e.g. current, voltage, phase angle etc. All Object 40 points report the integer scaling values and Object 41 is available to configure integer scaling quantities.

6.7 DNP3.0 configuration using S1 Agile

A PC support package for DNP3.0 is available as part of S1 Agile to allow configuration of the relay's DNP3.0 response. The PC is connected to the relay via a serial cable to the 9-pin front part of the relay - see the Introduction chapter (*P34x/EN IT*). The configuration data is uploaded from the relay to the PC in a block of compressed format data and downloaded to the relay in a similar manner after modification. The new DNP3.0 configuration takes effect in the relay after the download is complete. The default configuration can be restored at any time by choosing 'All Settings' from the 'Restore Defaults' cell in the menu 'Configuration' column.

In S1 Agile, the DNP3.0 data is displayed on a three main tabbed screens, one screen each for the point configuration, integer scaling and default variation (data format). The point configuration also includes tabs for binary inputs, binary outputs, counters and analogue input configuration.

7 IEC 61850 ETHERNET INTERFACE

7.1 Introduction

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions within a substation, and additionally provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security which is essential in substations today.

The MiCOM protection relays can integrate with the PACiS substation control systems, to complete General Electric's offer of a full IEC 61850 solution for the substation. The majority of Px4x relay types can be supplied with Ethernet, in addition to traditional serial protocols. Relays which have already been delivered with UCA2.0 on Ethernet can be easily upgraded to IEC 61850.

7.2 What is IEC 61850?

IEC 61850 is a 14-part international standard, which defines a communication architecture for substations. It is more than just a protocol and provides:

- Standardized models for IEDs and other equipment within the substation
- Standardized communication services (the methods used to access and exchange data)
- Standardized formats for configuration files
- Peer-to-peer (e.g. relay to relay) communication

The standard includes mapping of data onto Ethernet. Using Ethernet in the substation offers many advantages, most significantly including:

- High-speed data rates (currently 100 Mbits/s, rather than 10's of kbits/s or less used by most serial protocols)
- Multiple masters (called "clients")
- Ethernet is an open standard in every-day use

General Electric has been involved in the Working Groups which formed the standard, building on experience gained with UCA2.0, the predecessor of IEC 61850.

7.2.1 Interoperability

A major benefit of IEC 61850 is interoperability. IEC 61850 standardizes the data model of substation IEDs. This responds to the utilities' desire of having easier integration for different vendors' products, i.e. interoperability. It means that data is accessed in the same manner in different IEDs from either the same or different IED vendors, even though, for example, the protection algorithms of different vendors' relay types remain different.

IEC 61850-compliant devices is described are not interchangeable, you cannot replace one product with another. However, the terminology is predefined and anyone with knowledge of IEC 61850 can quickly integrate a new device without mapping all of the new data. IEC 61850 improves substation communications and interoperability at a lower cost to the end user.

7.2.2 The data model

To ease understanding, the data model of any IEC 61850 IED can be viewed as a hierarchy of information. The categories and naming of this information is standardized in the IEC 61850 specification.

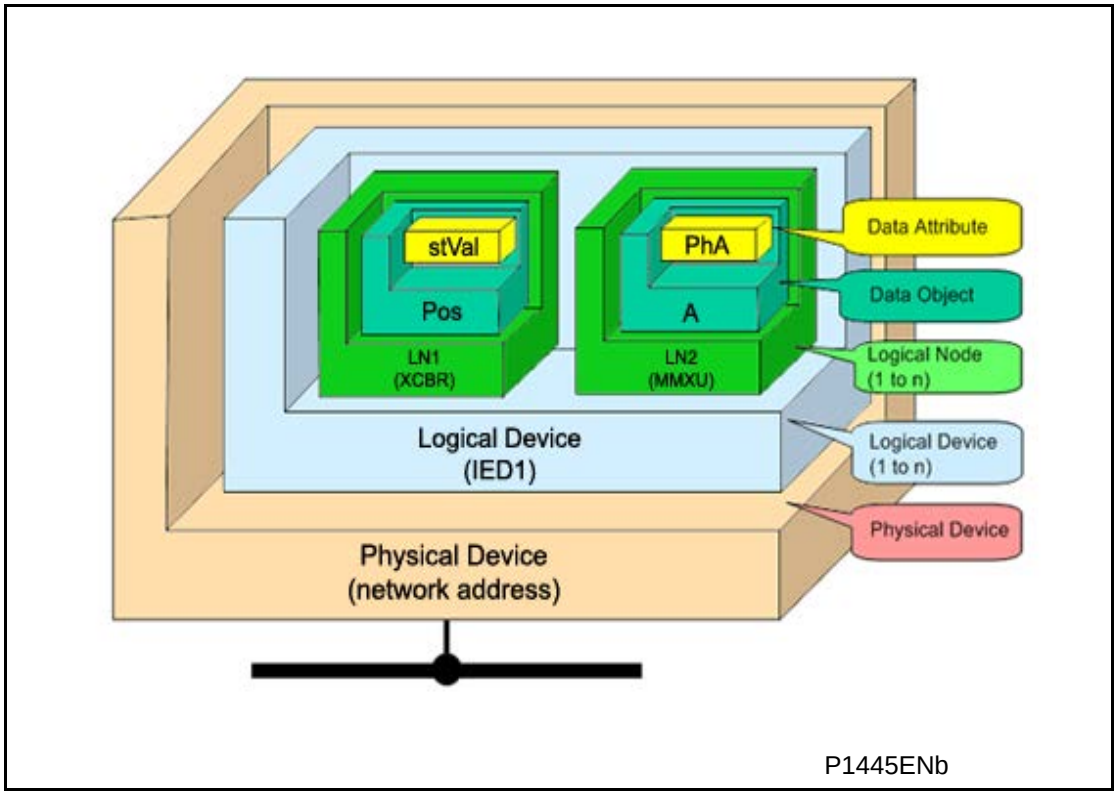


Figure 13: Data model layers in IEC 61850

The levels of this hierarchy can be described as follows:

- Physical Device – Identifies the actual IED within a system. Typically the device's name or IP address can be used (for example **Feeder_1 or 10.0.0.2**).
- Logical Device – Identifies groups of related Logical Nodes within the Physical Device. For the MiCOM relays, 5 Logical Devices exist: **Control, Measurements, Protection, Records, System**.
- Wrapper/Logical Node Instance – Identifies the major functional areas within the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name suffixed by an instance number. For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2).
- Data Object – This next layer is used to identify the type of data you will be presented with. For example, Pos (position) of Logical Node type XCBR.
- Data Attribute – This is the actual data (measurement value, status, description, etc.). For example, stVal (status value) indicating actual position of circuit breaker for Data Object type Pos of Logical Node type XCBR.

7.3 IEC 61850 in MiCOM relays

IEC 61850 is implemented in MiCOM relays by use of a separate Ethernet card. This card manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 "client" (or master), for example a DS Agile computer (C264) or HMI, or
- An "MMS browser", with which the full data model can be retrieved from the IED, without any prior knowledge

7.3.1 Capability

The IEC 61850 interface provides the following capabilities:

- Read access to measurements

All measurands are presented using the measurement Logical Nodes, in the 'Measurements' Logical Device. Reported measurement values are refreshed by the relay once per second, in line with the relay user interface.

- Generation of unbuffered reports on change of status/measurement

Unbuffered reports, when enabled, report any change of state in statuses and/or measurements (according to deadband settings).

- Support for time synchronization over an Ethernet link

Time synchronization is supported using SNTP (Simple Network Time Protocol); this protocol is used to synchronize the internal real time clock of the relays.

- GOOSE peer-to-peer communication

GOOSE communications of statuses are included as part of the IEC 61850 implementation. Please see section 6.6 for more details.

- Disturbance record extraction

Extraction of disturbance records, by file transfer, is supported by the MiCOM relays. The record is extracted as an ASCII format COMTRADE file.

- Controls

The following control services are available:

  - Direct Control
  - Direct Control with enhanced security
  - Select Before Operate (SBO) with enhanced security

Controls shall be applied to open and close circuit breakers via XCBR.Pos and DDB signals 'Control Trip' and 'Control Close'.

System/LLN0. LLN0.LEDRs shall be used to reset any trip LED indications.

- Reports

Reports only include data objects that have changed and not the complete dataset. The exceptions to this are a General Interrogation request and integrity reports.

- Buffered Reports

Eight Buffered Report Control Blocks, (BRCB), are provided in SYSTEM/LLN0 in Logical Device 'System'

Buffered reports are configurable to use any configurable dataset located in the same Logical device as the BRCB (i.e. SYSTEM/LLN0)

- Unbuffered Reports

Sixteen Unbuffered Report Control Blocks, (URCB) are provided in SYSTEM/LLN0 in Logical Device 'System'

Unbuffered reports are configurable to use any configurable dataset located in the same Logical device as the URCB (i.e. SYSTEM/LLN0)

- Configurable Data Sets

It is possible to create and configure datasets in any Logical Node using the IED Configurator. The maximum number of datasets will be specified in an IEDs ICD file. An IED is capable of handling 100 datasets.

- Published GOOSE message

Eight GOCBs are provided in SYSTEM/LLN0.

- Uniqueness of control

Uniqueness of control mechanism is implemented in the P34x to have consistency with the PACiS mechanism. This requires the relay to subscribe to the OrdRun signal from all devices in the system and be able to publish such a signal in a GOOSE message.

- Select Active Setting Group

Functional protection groups can be enabled/disabled via private mod/beh attributes in Protection/LLN0.OcpMod object. Setting groups are selectable using the Setting Group Control Block class, (SGCB). The Active Setting Group can be selected using the System/LLN0.SP.SGCB.ActSG data attribute in Logical Device 'System'.

- Quality for GOOSE

It is possible to process the quality attributes of any Data Object in an incoming GOOSE message. Devices that do not support IEC 61850 Quality flags shall send quality attributes as all zeros.

- Address List

An Address List document (to be titled ADL) is produced for each IED which shows the mapping between the IEC 61850 data model and the internal data model of the IED. It includes a mapping in the reverse direction, which may be more useful. This document is separate from the PICS/MICS document.

- Originator of Control

Originator of control mechanism is implemented for operate response message and in the data model on the ST of the related control object, consistent with the PACiS mechanism.

Setting changes (e.g. of protection settings) are not supported in the current IEC 61850 implementation. In order to keep this process as simple as possible, such setting changes are done using S1 Agile Settings & Records program. This can be done as previously using the front port serial connection of the relay, or now optionally over the Ethernet link if preferred (this is known as "tunneling").

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7.3.2 IEC 61850 configuration

One of the main objectives of IEC 61850 is to allow IEDs to be directly configured from a configuration file generated at system configuration time. At the system configuration level, the capabilities of the IED are determined from an IED capability description file (ICD) which is provided with the product. Using a collection of these ICD files from varying products, the entire protection of a substation can be designed, configured and tested (using simulation tools) before the product is even installed into the substation.

To help in this process, the S1 Agile Support Software provides an IED Configurator tool which allows the pre-configured IEC 61850 configuration file (an SCD file or CID file) to be imported and transferred to the IED. Alongside this, the requirements of manual configuration are satisfied by allowing the manual creation of configuration files for relays based on their original IED capability description (ICD file).

Other features include the extraction of configuration data for viewing and editing, and a sophisticated error checking sequence which ensures that the configuration data is valid for sending to the IED and that the IED will function within the context of the substation.

To help the user, some configuration data is available in the IED CONFIGURATOR column of the relay user interface, allowing read-only access to basic configuration data.

7.3.2.1 Configuration banks

To promote version management and minimize down-time during system upgrades and maintenance, the relays have incorporated a mechanism consisting of multiple configuration banks. These configuration banks are categorized as:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the relay is automatically stored into the inactive configuration bank, therefore not immediately affecting the current configuration. Both active and inactive configuration banks can be extracted at anytime.

When the upgrade or maintenance stage is complete, the IED Configurator tool can be used to transmit a command to a single IED. This command authorizes the activation of the new configuration contained in the inactive configuration bank, by switching the active and inactive configuration banks. This technique ensures that the system down-time is minimized to the start-up time of the new configuration. The capability to switch the configuration banks is also available via the **IED CONFIGURATOR** column.

For version management, data is available in the **IED CONFIGURATOR** column in the relay user interface, displaying the SCL Name and Revision attributes of both configuration banks.

7.3.2.2 Network connectivity

Note: This section presumes a prior knowledge of IP addressing and related topics. Further details on this topic may be found on the Internet (search for IP Configuration) and in numerous relevant books.

Configuration of the relay IP parameters (IP Address, Subnet Mask, Gateway) and SNTP time synchronization parameters (SNTP Server 1, SNTP Server 2) is performed by the IED Configurator tool, so if these parameters are not available via an SCL file, they must be configured manually.

If the assigned IP address is duplicated elsewhere on the same network, the remote communications will operate in an indeterminate way. However, the relay will check for a conflict on every IP configuration change and at power up. An alarm will be raised if an IP conflict is detected.

The relay can be configured to accept data from networks other than the local network by using the ‘Gateway’ setting.

7.4 The data model of MiCOM relays

The data model naming adopted in the Px40 relays has been standardized for consistency. Hence the Logical Nodes are allocated to one of the five Logical Devices, as appropriate, and the wrapper names used to instantiate Logical Nodes are consistent between the Px40 relays.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available separately. The MICS document provides lists of Logical Device definitions, Logical Node definitions, Common Data Class and Attribute definitions, Enumeration definitions, and MMS data type conversions. It generally follows the format used in Parts 7-3 and 7-4 of the IEC 61850 standard.

7.5 The communication services of MiCOM relays

The IEC 61850 communication services which are implemented in the Px40 relays are described in the Protocol Implementation Conformance Statement (PICS) document, which is available separately. The PICS document provides the Abstract Communication Service Interface (ACSI) conformance statements as defined in Annex A of Part 7-2 of the IEC 61850 standard.

7.6 Peer-to-peer (GSE) communications

The implementation of IEC 61850 Generic Substation Event (GSE) sets the way for cheaper and faster inter-relay communications. The generic substation event model provides the possibility for a fast and reliable system-wide distribution of input and output data values. The generic substation event model is based on the concept of an autonomous decentralization, providing an efficient method allowing the simultaneous delivery of the same generic substation event information to more than one physical device through the use of multicast services.

The use of multicast messaging means that IEC 61850 GOOSE uses a publisher-subscriber system to transfer information around the network*. When a device detects a change in one of its monitored status points it publishes (i.e. sends) a new message. Any device that is interested in the information subscribes (i.e. listens) to the data it contains.

Note: * Multicast messages cannot be routed across networks without specialized equipment.

Each new message is re-transmitted at user-configurable intervals until the maximum interval is reached, in order to overcome possible corruption due to interference, and collisions. In practice, the parameters which control the message transmission cannot be calculated. Time must be allocated to the testing of GSE schemes before or during commissioning, in just the same way a hardwired scheme must be tested.

7.6.1 Scope

A maximum of 32 virtual inputs are available within the PSL which can be mapped directly to a published dataset in a GOOSE message (only 1 fixed dataset is supported). All published GOOSE signals are BOOLEAN values.

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the 32 virtual inputs within the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

The relay can subscribe to all GOOSE messages but only the following data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2
- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

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7.6.2 IEC 61850 GOOSE configuration

All GOOSE configuration is performed via the IED Configurator tool available within the S1 Agile Support Software.

All GOOSE publishing configuration can be found under the ‘GOOSE Publishing’ tab in the configuration editor window. All GOOSE subscription configuration can be found under the

'External Binding' tab in the configuration editor window. Care should be taken to ensure that the configuration is correct, to ensure efficient GOOSE scheme operation.

Settings to enable GOOSE signaling and to apply Test Mode are available via the relay user interface.

7.7 Ethernet functionality

Settings relating to a failed Ethernet link are available in the 'COMMUNICATIONS' column of the relay user interface.

7.7.1 Ethernet disconnection

IEC 61850 'Associations' are unique and made to the relay between the client (master) and server (IEC 61850 device). In the event that the Ethernet is disconnected, such associations are lost, and will need to be re-established by the client. The TCP_KEEPALIVE function is implemented in the relay to monitor each association, and terminate any which are no longer active.

7.7.2 Loss of power

The relay allows the re-establishment of associations by the client without a negative impact on the relay's operation after having its power removed. As the relay acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost, and reports requested by connected clients are reset and must be re-enabled by the client when it next creates the new association to the relay.

7.8 Redundant ethernet communication ports

For information regarding the Redundant Ethernet communication ports and the three redundancy protocols available, RSTP (Rapid Spanning Tree Protocol), SHP (Self Healing Protocol), DHP (Dual Homing Protocol) and PRP (Parallel Redundancy Protocol), refer to the User Guide, *Px4x/EN REB*.

7.9 IEC61850-2-2 LE process bus ethernet communication (P348)

For information regarding the IEC 61850-9-2 LE Ethernet communication port, refer to the IEC 61850-9-2 LE Technical Manual, *Px4x_9-2LE-TM*.

8 SECOND REAR COMMUNICATIONS PORT (COURIER)

Relays with Courier, MODBUS, IEC 60870-5-103 or DNP3.0 protocol on the first rear communications port have the option of a second rear port, running the Courier language. The second port is designed typically for dial-up modem access by protection engineers/operators, when the main port is reserved for SCADA communication traffic. Communication is via one of three physical links: K-Bus, EIA(RS)485 or EIA(RS)232[1]. The port supports full local or remote protection and control access by S1 Agile software.

When changing the port configuration between K-Bus, EIA(RS)485 and EIA(RS)232 it is necessary to reboot the relay to update the hardware configuration of the second rear port.

There is also provision for the EIA(RS)485 and EIA(RS)232 protocols to be configured to operate with a modem, using an IEC 60870 10 bit frame.

Port configuration	Valid communication protocol
K-Bus	K-Bus
EIA(RS)232	IEC 60870 FT1.2, 11-bit frame IEC 60870, 10-bit frame
EIA(RS)485	IEC 60870 FT1.2, 11-bit frame IEC 60870, 10-bit frame

Table 15: Second rear comm. port communication protocol

If both rear communications ports are connected to the same bus, care should be taken to ensure their address settings are not the same, to avoid message conflicts.

8.1 Courier protocol

The following documentation should be referred to for a detailed description of the Courier protocol, command set and link description.

- R6509 K-Bus Interface Guide
- R6510 IEC 60870 Interface Guide
- R6511 Courier Protocol
- R6512 Courier User Guide

The second rear communications port is functionally the same as detailed in section 2.2 for a Courier rear communications port, with the following exceptions:

8.2 Event extraction

Automatic event extraction is not supported when the first rear port protocol is Courier, MODBUS or CS103. It is supported when the first rear port protocol is DNP3.0.

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8.3 Disturbance record extraction

Automatic disturbance record extraction is not supported when the first rear port protocol is Courier, MODBUS or CS103. It is supported when the first rear port protocol is DNP3.0.

8.4 Connection to the second rear port

The second rear Courier port connects using the 9-way female D-type connector (SK4) in the middle of the card end plate (in between IRIG-B connector and lower D-type). The connection is compliant to EIA(RS)574.

For IEC 60870-5-2 over EIA(RS)232.

Pin	Connection
1	No Connection
2	RxD
3	TxD
4	DTR#
5	Ground
6	No Connection
7	RTS#
8	CTS#
9	No Connection

Table 16: Second rear port RS232 connection

For K-bus or IEC 60870-5-2 over EIA(RS)485

Pin*	Connection
4	EIA(RS)485 - 1 (+ ve)
7	EIA(RS)485 - 2 (- ve)

Table 17: Second rear port RS485 connection

* - All other pins unconnected.

- These pins are control lines for use with a modem.

NOTES:

- Connector pins 4 and 7 are used by both the EIA(RS)232and EIA(RS)485 physical layers, but for different purposes. Therefore, the cables should be removed during configuration switches.
- For the EIA(RS)485 protocol an EIA(RS)485 to EIA(RS)232 converter will be required to connect a modem or PC running S1 Agile, to the relay.
- EIA(RS)485 is polarity sensitive, with pin 4 positive (+) and pin 7 negative (-).
- The K-Bus protocol can be connected to a PC via a KITZ101 or 102.

9 SK5 PORT CONNECTION

The lower 9-way D-type connector (SK5) is currently unsupported. Do not connect to this port.

SYMBOLS AND GLOSSARY

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 LOGIC SYMBOLS

Symbols	Explanation
<	Less than: Used to indicate an “under” threshold, such as undercurrent (current dropout).
>	Greater than: Used to indicate an “over” threshold, such as overcurrent (current overload).
&	Logical “AND”: Used in logic diagrams to show an AND-gate function.
1	Logical “OR”: Used in logic diagrams to show an OR-gate function.
o	A small circle on the input or output of a logic gate: Indicates a NOT (invert) function.
52a	A circuit breaker closed auxiliary contact: The contact is in the same state as the breaker primary contacts.
52b	A circuit breaker open auxiliary contact: The contact is in the opposite state to the breaker primary contacts.
64R	Rotor earth fault protection
64S	100% stator earth (ground) fault protection using a low frequency injection method.
Σ	“Sigma”: Used to indicate a summation, such as cumulative current interrupted.
τ	“Tau”: Used to indicate a time constant, often associated with thermal characteristics.
AC	Alternating current
BU	Backup: Typically a back-up protection element.
C/O	A changeover contact having normally closed and normally open connections: Often called a “form C” contact.
CB	Circuit breaker.
CB Aux	Circuit breaker auxiliary contacts: Indication of the breaker open/closed status.
CBF	Circuit breaker failure protection.
CLIO	Current Loop Input Output: 0-1 mA/0-10 mA/0-20 mA/4-20 mA transducer inputs and outputs CLI = current loop input - 0-1 mA/0-10 mA/0-20 mA/4-20 mA transducer input CLO = current loop output - 0-1 mA/0-10 mA/0-20 mA/4-20 mA transducer output
CS, Check Synch	Check Synchronizing function
CT	Current transformer
CTRL	Abbreviation of “Control”: As used for the Control Inputs function.
CTS	Current transformer supervision: To detect CT input failure.
DC	Direct current
DDB	Digital data bus within the programmable scheme logic: A logic point that has a zero or 1 status. DDB signals are mapped in logic to customize the relay’s operation.
DEF	Directional earth fault protection: A directionalized earth (ground) fault aided scheme.

Symbols	Explanation
DFIG/M	Double Fed Induction Generator/Motor
DFT	Discrete Fourier Transform
df/dt	Rate of change of frequency
Dly	Time delay.
DT	Abbreviation of “Definite Time”: An element which always responds with the same constant time delay on operation.
E/F	Earth fault: Directly equivalent to ground fault.
EMC	ElectroMagnetic Compatibility
ESD	Electrostatic Discharge
FAA	Ageing acceleration factor: Used by Loss of Life element
FFail	A field failure (loss of excitation) element: Could be labeled 40 in ANSI terminology.
FLC	Full load current: The nominal rated current for the circuit.
Flt	Abbreviation of “Fault”: Typically used to indicate faulted phase selection.
FN	Function.
Fwd	Indicates an element responding to a flow in the “Forward” direction.
F>	An overfrequency element: Could be labeled 81O in ANSI terminology.
F<	An underfrequency element: Could be labeled 81U in ANSI terminology.
Gen Diff	A generator differential element: Could be labeled 87G in ANSI terminology.
Gen-Xformer Diff	A generator-transformer differential element: Could be labeled 87GT in ANSI terminology.
Gnd	Abbreviation of “Ground”: Used to identify settings that relate to ground (earth) faults.
GRP	Abbreviation of “Group”: Typically an alternative setting group.
GUESS	Generator Unintentional Energization at StandStill.
I	Current.
I∧	Current raised to a power: Such as when breaker statistics monitor the square of ruptured current squared (∧ power = 2).
I<	An undercurrent element: Responds to current dropout.
I>	A phase overcurrent element: Could be labeled 50/51 in ANSI terminology.
IED	Intelligent Electronic Device
I0	Zero sequence current: Equals one third of the measured neutral/residual current.
I1	Positive sequence current.
I2	Negative sequence current.
I1	Positive sequence current.

Symbols	Explanation
I2	Negative sequence current.
I2>	Negative sequence overcurrent element Could be labeled 46OC in ANSI terminology.
I2therm>	A negative sequence thermal element: Could be labeled 46T in ANSI terminology.
I2pol	Negative sequence polarizing current.
IA	Phase A current: Might be phase L1, red phase.. or other, in customer terminology.
IB	Phase B current: Might be phase L2, yellow phase.. or other, in customer terminology.
IC	Phase C current: Might be phase L3, blue phase.. or other, in customer terminology.
ID	Abbreviation of “Identifier”: Often a label used to track a software version installed.
IDMT	Inverse definite minimum time: A characteristic whose trip time depends on the measured input (e.g. current) according to an inverse-time curve.
In	The rated nominal current of the relay: Software selectable as 1 amp or 5 amp to match the line CT input.
IN	Neutral current, or residual current: This results from an internal summation of the three measured phase currents.
IN>	A neutral (residual) overcurrent element: Detects earth (ground) faults. Could be labeled 50N/51N in ANSI terminology.
Inh	An inhibit signal.
IREF>	A Restricted Earth Fault overcurrent element: Detects earth (ground) faults. Could be labeled 64 in ANSI terminology.
ISEF>	A sensitive Earth Fault overcurrent element: Detects earth (ground) faults. Could be labeled 50N/51N in ANSI terminology.
Inst	An element with “instantaneous” operation: i.e. having no deliberate time delay.
I/O	Abbreviation of “Inputs and Outputs”: Used in connection with the number of optocoupled inputs and output contacts within the relay.
I/P	Abbreviation of “Input”.
LCD	Liquid crystal display: The front-panel text display on the relay.
LD	Abbreviation of “Level Detector”: An element responding to a current or voltage below its set threshold.
LED	Light emitting diode: Red or green indicator on the relay front-panel.
LoL	Loss of Life
LPF	Low Pass Filter
MCB	A “miniature circuit breaker”: Used instead of a fuse to protect VT secondary circuits.
N	Indication of “Neutral” involvement in a fault: i.e. a ground (earth) fault.
N/A	Not applicable.

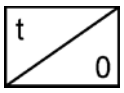
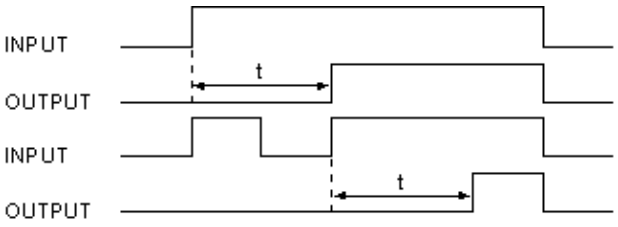
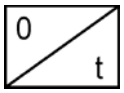
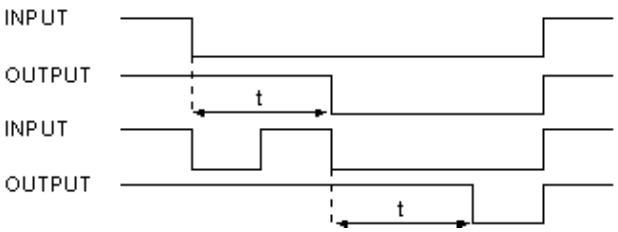
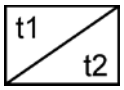
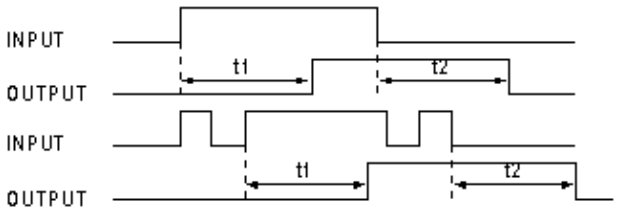
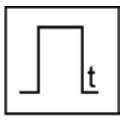
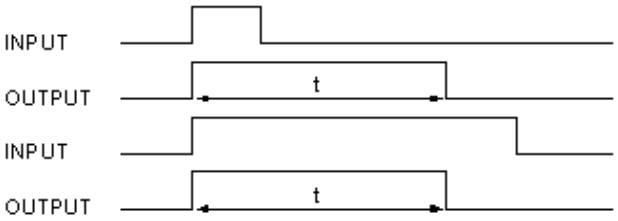
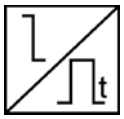
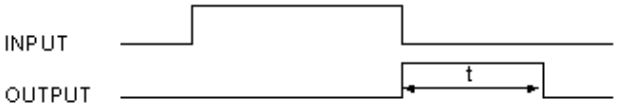
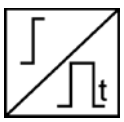
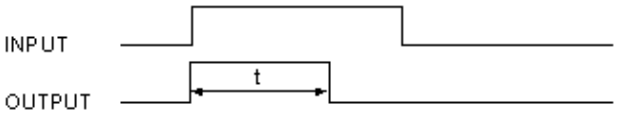
Symbols	Explanation
N/C	A normally closed or “break” contact: Often called a “form B” contact.
N/O	A normally open or “make” contact: Often called a “form A” contact.
NCCT	Non Conventional Current Transformer
NCIT	Non Conventional Instrument Transformer
NCVT	Non Conventional Voltage Transformer
NPS	Negative phase sequence.
NXT	Abbreviation of “Next”: In connection with hotkey menu navigation.
NVD	Neutral voltage displacement: Equivalent to residual overvoltage protection.
O/P	Abbreviation of “output”.
Opto	An optocoupled logic input: Alternative terminology: binary input.
P>	An active over power (W) element: Could be labeled 32P in ANSI terminology.
P<	An active under power (W) element: Could be labeled 32P in ANSI terminology.
P1	Used in IEC terminology to identify the primary CT terminal polarity: Replace by a dot when using ANSI standards.
P2	Used in IEC terminology to identify the primary CT terminal polarity: The non-dot terminal.
PC	Primary converter. Used to convert low voltage analogue output of Non Conventional Instrument Transformer to a digital signal.
PCB	Printed Circuit Board.
Ph	Abbreviation of “Phase”: Used in distance settings to identify settings that relate to phase-phase faults.
Pol	Abbreviation of “Polarizing”: Typically the polarizing voltage used in making directional decisions.
POW	Point on Wave
PN>	A Wattmetric earth fault element: Calculated using residual voltage and current quantities.
PSL	Programmable scheme logic: The part of the relay’s logic configuration that can be modified by the user, using the graphical editor within S1 Studio software.
PSlip	A Pole slip (out of step - OOS) element: Could be labeled 78 in ANSI terminology.
PWM	Pulse Width Modulated
Q>	A reactive over power (VAr) element: Could be labeled 32Q in ANSI terminology.
Q<	A reactive under power (VAr) element: Could be labeled 32Q in ANSI terminology.
R	Resistance (Ω).
64S R<	A 100% stator earth (ground) fault via low frequency injection under resistance element: Could be labeled 64S in ANSI terminology.

Symbols	Explanation
R Gnd	A distance zone resistive reach setting: Used for ground (earth) faults.
RCA	Abbreviation of “Relay Characteristic Angle”: The center of the directional characteristic.
REF	Restricted Earth (ground) Fault protection.
Rev	Indicates an element responding to a flow in the “reverse” direction.
RMS	The equivalent a.c. current: Taking into account the fundamental, plus the equivalent heating effect of any harmonics. Abbreviation of “root mean square”.
RP	Abbreviation of “Rear Port”: The communication ports on the rear of the relay.
RTD	Resistance temperature device.
Rx	Abbreviation of “Receive”: Typically used to indicate a communication receive line/pin.
S<	An apparent under power (VA) element
S1	Used in IEC terminology to identify the secondary CT terminal polarity: Replace by a dot when using ANSI standards.
S2	Used in IEC terminology to identify the secondary CT terminal polarity: The non-dot terminal. Also used to signify negative sequence apparent power, S2 = V2 x I2.
S2>	A negative sequence apparent power element, S2 = V2 x I2.
Sen	Sensitive
SEF	Sensitive Earth Fault Protection.
SV	Sampled Value. Analogue current and voltage signals are sampled x times per cycle.
t	A time delay.
TCS	Trip circuit supervision.
TD	The time dial multiplier setting: Applied to inverse-time curves (ANSI/IEEE).
TE	A standard for measuring the width of a relay case: One inch = 5TE units.
Thermal I>	A stator thermal overload element: Could be labeled 49 in ANSI terminology.
TMS	The time multiplier setting applied to inverse-time curves (IEC).
Tx	Abbreviation of “Transmit”: Typically used to indicate a communication transmit line/pin.
Thru/TF	Through Fault monitoring
V	Voltage.
V<	An undervoltage element: Could be labeled 27 in ANSI terminology.
V>	An overvoltage element: Could be labeled 59 in ANSI terminology.
V0	Zero sequence voltage: Equals one third of the measured neutral/residual voltage.
V1	Positive sequence voltage.
V2	Negative sequence voltage.
V2>	A negative phase sequence (NPS) overvoltage element: Could be labeled 47 in ANSI terminology.
V2pol	Negative sequence polarizing voltage.

Symbols	Explanation
VA	Phase A voltage: Might be phase L1, red phase.. or other, in customer terminology.
VB	Phase B voltage: Might be phase L2, yellow phase.. or other, in customer terminology.
VC	Phase C voltage: Might be phase L3, blue phase.. or other, in customer terminology.
VCO	Voltage controlled overcurrent element.
VDEP OC>	A voltage dependent overcurrent element: Could be a voltage controlled or voltage restrained overcurrent element. Could be labeled 51V in ANSI terminology.
V/Hz	An overfluxing element, flux is proportional to voltage/frequency: Could be labeled 24 in ANSI terminology.
Vk	IEC knee point voltage of a current transformer.
Vn	The rated nominal voltage of the relay: To match the line VT input.
VN	Neutral voltage displacement, or residual voltage.
VN>	A residual (neutral) overvoltage element: Could be labeled 59N in ANSI terminology.
VN3H>	A 100% stator earth (ground) fault 3rd harmonic residual (neutral) overvoltage element: Could be labeled 59TN in ANSI terminology.
VN3H<	A 100% stator earth (ground) fault 3rd harmonic residual (neutral) undervoltage element: Could be labeled 27TN in ANSI terminology..
Vres.	Neutral voltage displacement, or residual voltage.
VT	Voltage transformer.
VTS	Voltage transformer supervision: To detect VT input failure.
Vx	An auxiliary supply voltage: Typically the substation battery voltage used to power the relay.
Xformer	Transformer
Z<	An under impedance element: Could be labeled 21 in ANSI terminology.
Z0	Zero sequence impedance.
Z1	Positive sequence impedance.
Z2	Negative sequence impedance.

Table 1: Logic symbols

2 LOGIC TIMERS

Logic Symbols	Explanation	Time Chart
	Delay on pick-up timer, t	
	Delay on drop-off timer, t	
	Delay on pick-up/drop-off timer	
	Pulse timer	
	Pulse pick-up falling edge	
	Pulse pick-up raising edge	

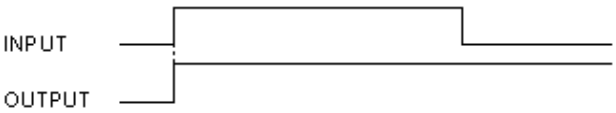
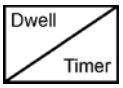
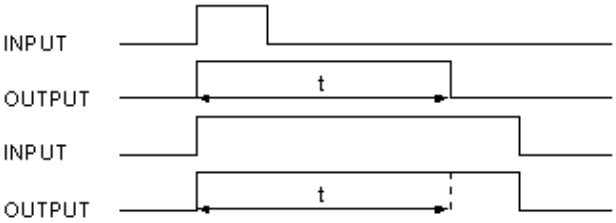
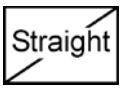
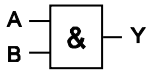
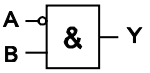
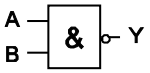
Logic Symbols	Explanation	Time Chart
	Latch	
	Dwell timer	
	Straight (non latching): Hold value until input reset signal	

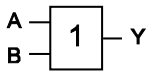
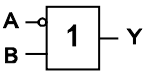
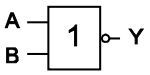
Table 2: Logic timers

3 LOGIC GATES

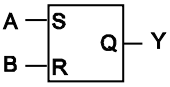
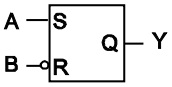
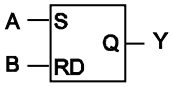
AND GATE

Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
	IN IN OUT 0 1 0 0 1 0 0 1 0 1 0 0 1 1 1		IN IN OUT A B Y 0 0 0 0 1 1 1 0 0 1 1 0		IN IN OUT A B Y 0 0 1 0 1 1 1 0 1 1 1 0

OR GATE

Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
	IN IN OUT A B Y 0 0 0 0 1 1 1 0 1 1 1 1		IN IN OUT A B Y 0 0 1 0 1 1 1 0 0 1 1 1		IN IN OUT A B Y 0 0 1 0 1 0 1 0 0 1 1 0

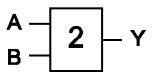
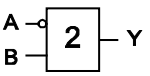
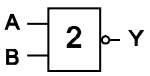
R - S FLIP-FLOP

Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
	A B QN QN+ Active Mode 0 0 Hold Mode 0 1 0 Hold Mode 1 0 Reset 0 1 Set 1 0 1 Hold Mode 0 0 - - Inhibit Mode		A B QN QN+ Active Mode 0 0 0 Hold Mode 1 0 Reset 0 1 Hold Mode 1 0 - - Inhibit Mode 0 1 Set 0 1 1 Hold Mode	 * RD = Reset Dominant	A B QN QN+ Active Mode 0 0 Hold Mode 0 1 0 0 1 Set 1 0 1 Hold Mode 1 1 0

EXCLUSIVE OR GATE

Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
	IN IN OUT A B Y 0 0 0 0 1 1 1 0 1 1 1 0		IN IN OUT A B Y 0 0 1 0 1 0 1 0 0 1 1 1		IN IN OUT A B Y 0 0 1 0 1 0 1 0 0 1 1 1

MULTI INPUT GATE

Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
	IN IN OUT A B Y 0 0 0 0 1 0 1 0 0 1 1 1		IN IN OUT A B Y 0 0 0 0 1 1 1 0 0 1 1 0		IN IN OUT A B Y 0 0 1 0 1 1 1 0 1 1 1 0

NOT GATE

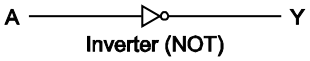
Symbol	Truth Table
	IN IN OUT A Y 0 1 1 0

Table 3: Logic gates

SG

CYBER SECURITY

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 OVERVIEW

In the past, substation networks were traditionally isolated and the protocols and data formats used to transfer information between devices were more often than not proprietary.

For these reasons, the substation environment was very secure against cyber attacks. The terms used for this inherent type of security are:

- Security by isolation (if the substation network is not connected to the outside world, it can't be accessed from the outside world).
- Security by obscurity (if the formats and protocols are proprietary, it is very difficult to interpret them.

The increasing sophistication of protection schemes coupled with the advancement of technology and the desire for vendor interoperability has resulted in standardization of networks and data interchange within substations. Today, devices within substations use standardized protocols for communication. Furthermore, substations can be interconnected with open networks, such as the internet or corporate-wide networks, which use standardized protocols for communication. This introduces a major security risk making the grid vulnerable to cyber-attacks, which could in turn lead to major electrical outages.

Clearly, there is now a need to secure communication and equipment within substation environments. This chapter describes the security measures that have been put in place for General Electric's range of Intelligent Electronic Devices (IEDs).

2 THE NEED FOR CYBER SECURITY

Cyber-security provides protection against unauthorized disclosure, transfer, modification, or destruction of information and/or information systems, whether accidental or intentional. To achieve this, there are several security requirements:

- Confidentiality (preventing unauthorized access to information)
- Integrity (preventing unauthorized modification)
- Availability / Authentication (preventing the denial of service and assuring authorized access to information)
- Non-Repudiation (preventing the denial of an action that took place)
- Traceability/Detection (monitoring and logging of activity to detect intrusion and analyze incidents)

The threats to cyber security may be unintentional (e.g. natural disasters, human error), or intentional (e.g. cyber attacks by hackers).

Good cyber security can be achieved with a range of measures, such as closing down vulnerability loopholes, implementing adequate security processes and procedures and providing technology to help achieve this.

Examples of vulnerabilities are:

- Indiscretions by personnel (e.g. users keep passwords on their computer)
- Bypassing of controls (e.g. users turn off security measures)
- Bad practice (users do not change default passwords, or everyone uses the same password to access all substation equipment)
- Inadequate technology (e.g. substation is not firewalled)

Examples of availability issues are:

- Equipment overload, resulting in reduced or no performance
- Expiry of a certificate prevents access to equipment.

To help tackle these issues, standards organizations have produced various standards, by which compliance significantly reduces the threats associated with lack of cyber security.

3 STANDARDS

There are several standards, which apply to substation cyber security (see Table 1).

	Country	
NERC CIP (North American Electric Reliability Corporation)	USA	Framework for the protection of the grid critical Cyber Assets
BDEW (German Association of Energy and Water Industries)	Germany	Requirements for Secure Control and Telecommunication Systems
ANSI ISA 99	USA	ICS oriented then Relevant for EPU completing existing standard and identifying new topics such as patch management
IEEE 1686	International	International Standard for substation IED cyber security capabilities
IEC 62351	International	Power system data and Comm. protocol
ISO/IEC 27002	International	Framework for the protection of the grid critical Cyber Assets
NIST SP800-53 (National Institute of Standards and Technology)	USA	Complete framework for SCADA SP800-82and ICS cyber security
CPNI Guidelines (Centre for the Protection of National Infrastructure)	UK	Clear and valuable good practices for Process Control and SCADA security

Table 1: Standards applicable to cyber security

The standards currently applicable to Alstom Grid IEDs are NERC and IEEE1686.

3.1 NERC Compliance

The North American Electric Reliability Corporation (NERC) created a set of standards for the protection of critical infrastructure. These are known as the CIP standards (Critical Infrastructure Protection). These were introduced to ensure the protection of Critical Cyber Assets, which control or have an influence on the reliability of North America's bulk electric systems.

These standards have been compulsory in the USA for several years now. Compliance auditing started in June 2007, and utilities face extremely heavy fines for non-compliance.

The group of CIP standards is listed in Table 2.

CIP Standard	Description
CIP-002-1 Critical Cyber Assets	Define and document the Critical Assets and the Critical Cyber Assets.
CIP-003-1 Security Management Controls	Define and document the Security Management Controls required to protect the Critical Cyber Assets.
CIP-004-1 Personnel and Training	Define and Document Personnel handling and training required protecting Critical Cyber Assets.
CIP-005-1 Electronic Security	Define and document logical security perimeter where Critical Cyber Assets reside and measures to control access points and monitor electronic access.
CIP-006-1 Physical Security	Define and document Physical Security Perimeters within which Critical Cyber Assets reside.

CIP Standard	Description
CIP-007-1 Systems Security Management	Define and document system test procedures, account and password management, security patch management, system vulnerability, system logging, change control and configuration required for all Critical Cyber Assets.
CIP-008-1 Incident Reporting and Response Planning	Define and document procedures necessary when Cyber Security Incidents relating to Critical Cyber Assets are identified.
CIP-009-1 Recovery Plans	Define and document Recovery plans for Critical Cyber Assets.

Table 2: NERC CIP standards

The following sections provide further details about each of these standards, describing the associated responsibilities of the utility company and where the IED manufacturer can help the utilities with the necessary compliance to these standards.

3.1.1 CIP 002

CIP 002 concerns itself with the identification of:

- Critical assets, such as overhead lines and transformers
- Critical cyber assets, such as IEDs that use routable protocols to communicate outside or inside the Electronic Security Perimeter; or are accessible by dial-up.

Power utility responsibilities:	General Electric's contribution:
Create the list of the assets	We can help the power utilities to create this asset register automatically. We can provide audits to list the Cyber assets.

3.1.2 CIP 003

CIP 003 requires the implementation of a cyber security policy, with associated documentation, which demonstrates the management's commitment and ability to secure its Critical Cyber Assets.

The standard also requires change control practices whereby all entity or vendor-related changes to hardware and software components are documented and maintained.

Power utility responsibilities:	General Electric's contribution:
To create a Cyber Security Policy	We can help the power utilities to have access control to its critical assets by providing centralized Access control. We can help the customer with its change control by providing a section in the documentation where it describes changes affecting the hardware and software.

3.1.3 CIP 004

CIP 004 requires that personnel having authorized cyber access or authorized physical access to Critical Cyber Assets, (including contractors and service vendors), have an appropriate level of training.

Power utility responsibilities:	General Electric's contribution:
To provide appropriate training of its personnel	We can provide cyber security training.

3.1.4 CIP 005

CIP 005 requires the establishment of an Electronic Security Perimeter (ESP), which provides:

- The disabling of ports and services that are not required
- Permanent monitoring and access to logs (24x7x365)
- Vulnerability Assessments (yearly at a minimum)
- Documentation of Network Changes

Power utility responsibilities:	General Electric's contribution:
To monitor access to the ESP To perform the vulnerability assessments To document network changes	To disable all ports not used in the IED To monitor and record all access to the IED

3.1.5 CIP 006

CIP 006 states that Physical Security controls, providing perimeter monitoring and logging along with robust access controls, must be implemented and documented. All cyber assets used for Physical Security are considered critical and should be treated as such:

Power utility responsibilities:	General Electric's contribution:
Provide physical security controls and perimeter monitoring. Ensure that people who have access to critical cyber assets don't have criminal records General Electric's contribution.	General Electric cannot provide additional help with this aspect.

3.1.6 CIP 007

CIP 007 covers the following points:

- Test procedures
- Ports and services
- Security patch management
- Antivirus
- Account management
- Monitoring
- An annual vulnerability assessment should be performed

Power utility responsibilities:	General Electric's contribution:
To provide an incident response team and have appropriate processes in place	Test procedures; We can provide advice and help on testing. Ports and services; Our devices can disable unused ports and services. Security patch management; We can provide assistance. Antivirus; We can provide advise and assistance. Account management; We can provide advice and assistance. Monitoring; Our equipment monitors and logs access.

3.1.7 CIP 008

CIP 008 requires that an incident response plan be developed, including the definition of an incident response team, their responsibilities and associated procedures.

Power utility responsibilities:	General Electric's contribution:
To provide an incident response team and have appropriate processes in place.	General Electric cannot provide additional help with this aspect.

3.1.8 CIP 009

CIP 009 states that a disaster recovery plan should be created and tested with annual drills.

Power utility responsibilities:	General Electric's contribution:
To implement a recovery plan	To provide guidelines on recovery plans and backup/restore documentation

3.2 IEEE 1686-2007

IEEE 1686-2007 is an IEEE Standard for substation IEDs' cyber security capabilities. It proposes practical and achievable mechanisms to achieve secure operations.

The following features described in this standard apply to General Electric Px40 relays:

- Passwords are 8 characters long and can contain upper-case, lower-case, numeric and special characters.
- Passwords are never displayed or transmitted to a user.
- IED functions and features are assigned to different password levels. The assignment is fixed.
- Record of an audit trail listing events in the order in which they occur, held in a circular buffer.
- Records contain all defined fields from the standard and record all defined function event types where the function is supported.
- No password defeat mechanism exists. Instead a secure recovery password scheme is implemented.
- Unused ports (physical and logical) may be disabled.

4 PX40 CYBER SECURITY IMPLEMENTATION

The General Electric IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

This section describes the current implementation of cyber security, valid for the release of platform software to which this manual pertains. This current cyber security implementation is known as Cyber Security Phase 1.

At the IED level, these cyber security measures have been implemented:

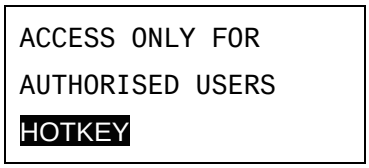
- Four-level Access
- Password strengthening
- Disabling of unused application and physical ports
- Inactivity timer
- Storage of security events (logs) in the IED
- NERC-compliant default display

External to the IEDs, the following cyber security measures have been implemented:

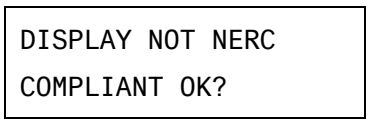
- Antivirus
- Security patch management

4.1 NERC-Compliant Display

For the IED to be NERC-compliant, it must provide the option for a NERC-compliant default display. The default display that is implemented in General Electric's cyber-security concept contains a warning that the IED can be accessed by authorised users.



If you try to change the default display from the NERC-compliant one, a further warning is displayed:



The default display navigation map shows how NERC-compliance is achieved with the product's default display concept.

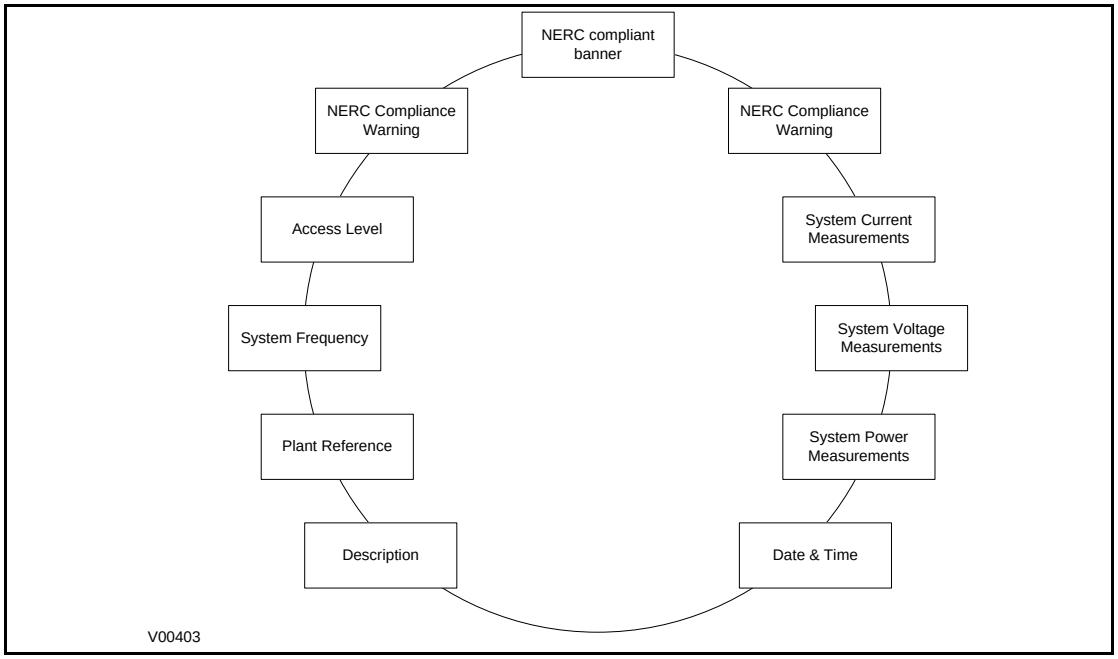


Figure 1: Standards applicable to cyber security

4.2 Four-level Access

The menu structure contains four levels of access three of which are password protected. These are summarized in Table 3.

Level	Meaning	Read Operation	Write Operation
0	Read Some Write Minimal	SYSTEM DATA column: Description Plant Reference Model Number Serial Number S/W Ref. Access Level Security Feature SECURITY CONFIG column: User Banner Attempts Remain Blk Time Remain Fallback PW level Security Code (UI only)	Password Entry LCD Contrast (UI only)
1	Read All Write Few	All data and settings are readable. Poll Measurements	All items writeable at level 0 Level 1 Password setting Select Event, Main and Fault (upload) Extract Events (e.g. via MiCOM S1 Agile)

Level	Meaning	Read Operation	Write Operation
2	Read All Write Some	All data and settings are readable. Poll Measurements	All items writeable at level 1 Setting Cells that change visibility (Visible/Invisible) Setting Values (Primary/Secondary) selector Commands: Reset Indication Reset Demand Reset Statistics Reset CB Data/counters Level 2 Password setting
3	Read All Write All	All data and settings are readable. Poll Measurements	All items writeable at level 2 Change all Setting cells Operations: Extract and download Setting file Extract and download PSL Extract and download MCL61850 (IED Config – IEC 61850) Extraction of Disturbance Recorder Courier/Modbus Accept Event (auto event extraction, e.g. via A2R) Commands: Change Active Group setting Close/Open CB Change Comms device address Set Date & Time Switch MCL banks/Switch Conf. Bank in UI (IED Config – IEC 61850) Enable/Disable Device ports (in SECURITY CONFIG column) Level 3 password setting

Table 3: Password levels

4.2.1 Blank passwords

A blank password is effectively a zero-length password. Through the front panel it is entered by confirming the password entry without actually entering any password characters. Through a communications port the Courier and Modbus protocols each have a means of writing a blank password to the IED. A blank password disables the need for a password at the level that this password applied.

Blank passwords have a slightly different validation procedure. If a blank password is entered through the front panel, the following text is displayed, after which the procedure is the same as already described:

```
BLANK PASSWORD
ENTERED
CONFIRM
```

Blank passwords cannot be configured if lower level password is not blank.

Blank passwords affect fall back level after inactivity timeout or logout.

The ‘fallback level’ is the password level adopted by the IED after an inactivity timeout, or after the user logs out. This will be either the level of the highest level password that is blank, or level 0 if no passwords are blank.

4.2.2 Default passwords

Default passwords are blank for Level 1 and **AAAA** for Levels 2 and 3.

4.2.3 Password rules

- Default passwords are blank for Level 1 and AAAA for Levels 2 and 3
- Passwords may be any length between 0 and 8 characters long
- Passwords may or may not be NERC compliant
- Passwords may contain any ASCII character in the range ASCII code 33 (21 Hex) to ASCII code 122 (7A Hex) inclusive
- Only one password is required for all the IED interfaces

4.2.4 Access level DDBs

In additional to having the 'Access level' cell in the 'System data' column (address 00D0), the current level of access for each interface is also available for use in the Programming Scheme Logic (PSL) by mapping to these Digital Data Bus (DDB) signals:

- HMI Access Lvl 1
- HMI Access Lvl 2
- FPort AccessLvl1
- FPort AccessLvl2
- RPrt1 AccessLvl1
- RPrt1 AccessLvl2
- RPrt2 AccessLvl1
- RPrt2 AccessLvl2

Where HMI is the Human Machine Interface.

Each pair of DDB signals indicates the access level as follows:

- Lvl 1 off, Lvl 2 off = 0
- Lvl 1 on, Lvl 2 off = 1
- Lvl 1 off, Lvl 2 on = 2
- Lvl 1 on, Lvl 2 on = 3

Key:

HMI = Human Machine Interface

FPort = Front Port

RPrt = Rear Port

Lvl = Level

4.3 Enhanced Password Security

Cyber-security requires strong passwords and validation for NERC compliance.

4.3.1 Password strengthening

NERC compliant passwords result in a minimum level of complexity, and include these requirements:

- At least one upper-case alpha character
- At least one lower-case alpha character
- At least one numeric character
- At least one special character (%,$...)
- At least six characters long

4.3.2 Password validation

The IED checks for NERC compliance. If the password is entered through the front panel then this is reflected on the panel Liquid Crystal Display (LCD) display.

If the entered password is NERC compliant, the following text is displayed:

```
NERC COMPLIANT
P/WORD WAS SAVED
```

The IED does not enforce NERC compliance. It is the responsibility of the user to ensure that compliance is adhered to as and when necessary. In the case that the password entered is not NERC-compliant, the user is required to actively confirm this, in which case the non-compliance is logged.

If the entered password is not NERC compliant, the following text is displayed:

```
NERC COMPLIANCE
NOT MET CONFIRM?
```

On confirmation, the non-compliant password is stored and the following acknowledgement message is displayed for 2 seconds.

```
NON-NERC P/WORD
SAVED OK
```

If the action is cancelled, the password is rejected and the following message displayed for 2 seconds.

```
NON-NERC P/WORD
NOT SAVE
```

If the password is entered through a communications port using Courier or Modbus protocols the IED will store the password, irrespective of whether it is or isn't NERC-compliant, and then uses appropriate response codes to inform the client that the password was NERC-compliant or not. The client then can choose if he/she wishes to enter a new password that is NERC-compliant or leave the entered one in place.

4.3.3 Password blocking

You are locked out temporarily, after a defined number of failed password entry attempts. The number of password entry attempts, and the blocking periods are configurable as shown in the table at the end of this section.

Each invalid password entry attempt decrements the 'Attempts Remain' data cell by 1. When the maximum number of attempts has been reached, access is blocked. If the attempts timer expires, or the correct password is entered *before* the 'attempt count' reaches the maximum number, then the 'attempts count' is reset to 0.

An attempt is only counted if the attempted password uses only characters in the valid range, but the attempted password is not correct (does not match the corresponding password in the IED). Any attempt where one or more characters of the attempted password are not in the valid range will not be counted.

Once the password entry is blocked, a 'blocking timer' is initiated. Attempts to access the interface whilst the 'blocking timer' is running results in an error message, irrespective of whether the correct password is entered or not. Only after the 'blocking timer' has expired will access to the interface be unblocked, whereupon the attempts counter is reset to zero.

Attempts to write to the password entry whilst it is blocked results in the following message, which is displayed for 2 seconds.

```
NOT ACCEPTED
ENTRY IS BLOCKED
```

Appropriate responses achieve the same result if the password is written through a communications port.

The attempts count, attempts timer and blocking timer can be configured, as shown in the table.

Setting	Cell Col Row	Units	Default Setting	Available Setting
Attempts Limit	25 02		3	0 to 3 step 1
Attempts Timer	25 03	Minutes	2	1 to 3 step 1
Blocking Timer	25 04	Minutes	5	1 to 30 step 1

Table 4: Password blocking configuration

4.4 Password Recovery

Password recovery is the means by which the passwords can be recovered on a device if the customer should mislay the configured passwords. To obtain the recovery password the customer must contact the General Electric Contact Centre and supply two pieces of information from the IED – namely the Serial Number and its Security Code. The Contact Centre will use these items to generate a Recovery Password which is then provided to the customer.

The security code is a 16-character string of upper case characters. It is a read-only parameter. The IED generates its own security code randomly. A new code is generated under the following conditions:

- On power up
- Whenever settings are set back to default
- On expiry of validity timer (see below)

- When the recovery password is entered

As soon as the security code is displayed on the LCD display, a validity timer is started. This validity timer is set to 72 hours and is not configurable. This provides enough time for the contact centre to manually generate and send a recovery password. The Service Level Agreement (SLA) for recovery password generation is one working day, so 72 hours is sufficient time, even allowing for closure of the contact centre over weekends and bank holidays.

To prevent accidental reading of the IED security code the cell will initially display a warning message:

```
PRESS ENTER TO
READ SEC. CODE
```

The security code will be displayed on confirmation, whereupon the validity timer will be started.

Note: The security code can only be read from the front panel.

4.4.1 Password recovery

The recovery password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once - for password recovery.

Entry of the recovery password causes the IED to reset all passwords back to default. This is all it is designed to do. After the passwords have been set back to default, it is up to the user to enter new passwords appropriate for the function for which they are intended, ensuring NERC compliance, if required.

On this action, the following message is displayed:

```
PASSWORDS HAVE BEEN
SET TO DEFAULT
```

The recovery password can be applied through any interface, local or remote. It will achieve the same result irrespective of which interface it is applied through.

4.4.2 Password Encryption

The IED supports encryption for passwords entered remotely. The encryption key can be read from the IED through a specific cell available only through communication interfaces, not the front panel. Each time the key is read the IED generates a new key that is valid only for the next password encryption write. Once used, the key is invalidated and a new key must be read for the next encrypted password write. The encryption mechanism is otherwise transparent to the user.

4.5 Disabling Physical Ports

It is possible to disable unused physical ports. A level 3 password is needed to perform this action.

To prevent accidental disabling of a port, a warning message is displayed according to whichever port is required to be disabled. For example if rear port 1 is to be disabled, the following message appears:

```
REAR PORT 1 TO BE
DISABLED
CONFIRM
```

Two to four ports can be disabled, depending on the model.

- Front port
- Rear port 1
- Rear port 2 (not implemented on all models)
- Ethernet port (not implemented on all models)

Note: It is not possible to disable a port from which the disabling port command originates.

4.6 Disabling Logical Ports

It is possible to disable unused logical ports. A level 3 password is needed to perform this action.

Note: The port disabling setting cells are not provided in the settings file.



Caution: Disabling the Ethernet port will disable all Ethernet based communications.

If it is not desirable to disable the Ethernet port, it is possible to disable selected protocols on the Ethernet card and leave others functioning.

Three protocols can be disabled:

- IEC61850
- DNP3 Over Ethernet
- Courier Tunnelling

Note: If any of these protocols are enabled or disabled, the Ethernet card will reboot.

4.7 Logging out

If you have been configuring the IED, you should 'log out'. You do this by going up to the top of the menu tree. When you are at the Column Heading level and you press the Up button, you may be prompted to log out with the following display:

```
DO YOU WANT TO LOG
OUT?
```

You will only be asked this question if your password level is higher than the fallback level.

If you confirm, the following message is displayed for 2 seconds:

```
LOGGED OUT
Access Level <x>
```

Where x is the current fallback level.

If you decide not to log out (i.e. you cancel), the following message is displayed for 2 seconds.

```
LOGOUT CANCELLED
Access Level <x>
```

Where x is the current access level.

4.8 Security Events Management

The implementation of NERC-compliant cyber security necessitates the generation of a range of Event records, which log security issues such as the entry of a non-NERC-compliant password, or the selection of a non-NERC-compliant default display. Table 5 lists all Security events.

Event Value	Display
PASSWORD LEVEL UNLOCKED	USER LOGGED IN ON <int> LEVEL <n>
PASSWORD LEVEL RESET	USER LOGGED OUT ON <int> LEVEL <n>
PASSWORD SET BLANK	P/WORD SET BLANK BY <int> LEVEL <p>
PASSWORD SET NON-COMPLIANT	P/WORD NOT-NERC BY <int> LEVEL <p>
PASSWORD MODIFIED	PASSWORD CHANGED BY <int> LEVEL <p>
PASSWORD ENTRY BLOCKED	PASSWORD BLOCKED ON <int>
PASSWORD ENTRY UNBLOCKED	P/WORD UNBLOCKED ON <int>
INVALID PASSWORD ENTERED	INV P/W ENTERED ON <int>
PASSWORD EXPIRED	P/WORD EXPIRED ON <int>
PASSWORD ENTERED WHILE BLOCKED	P/W ENT WHEN BLK ON <int>
RECOVERY PASSWORD ENTERED	RCVY P/W ENTERED ON <int>
IED SECURITY CODE READ	IED SEC CODE RD ON <int>
IED SECURITY CODE TIMER EXPIRED	IED SEC CODE EXP -
PORT DISABLED	PORT DISABLED BY <int> PORT <prt>
PORT ENABLED	PORT ENABLED BY <int> PORT <prt>
DEF. DISPLAY NOT NERC COMPLIANT	DEF DSP NOT-NERC
PSL SETTINGS DOWNLOADED	PSL STNG D/LOAD BY <int> GROUP <grp>
DNP SETTINGS DOWNLOADED	DNP STNG D/LOAD BY <int>
TRACE DATA DOWNLOADED	TRACE DAT D/LOAD BY <int>
IEC61850 CONFIG DOWNLOADED	IED CONFG D/LOAD BY <int>
USER CURVES DOWNLOADED	USER CRV D/LOAD BY <int> GROUP <crv>
PSL CONFIG DOWNLOADED	PSL CONFG D/LOAD BY <int> GROUP <grp>

Event Value	Display
SETTINGS DOWNLOADED	SETTINGS D/LOAD BY <int> GROUP <grp>
PSL SETTINGS UPLOADED	PSL STNG UPLOAD BY <int> GROUP <grp>
DNP SETTINGS UPLOADED	DNP STNG UPLOAD BY <int>
TRACE DATA UPLOADED	TRACE DAT UPLOAD BY <int>
IEC61850 CONFIG UPLOADED	IED CONFG UPLOAD BY <int>
USER CURVES UPLOADED	USER CRV UPLOAD BY <int> GROUP <crv>
PSL CONFIG UPLOADED	PSL CONFG UPLOAD BY <int> GROUP <grp>
SETTINGS UPLOADED	SETTINGS UPLOAD BY <int> GROUP <grp>
EVENTS HAVE BEEN EXTRACTED	EVENTS EXTRACTED BY <int> <nov> EVNTS
ACTIVE GROUP CHANGED	ACTIVE GRP CHNGE BY <int> GROUP <grp>
CS SETTINGS CHANGED	C & S CHANGED BY <int>
DR SETTINGS CHANGED	DR CHANGED BY <int>
SETTING GROUP CHANGED	SETTINGS CHANGED BY <int> GROUP <grp>
POWER ON	POWER ON -
SOFTWARE_DOWNLOADED	S/W DOWNLOADED -

Table 5: Security event values

Where:

int is the interface definition (UI, FP, RP1, RP2, TNL, TCP)

prt is the port ID (FP, RP1, RP2, TNL, DNP3, IEC, ETHR)

grp is the group number (1, 2, 3, 4)

crv is the Curve group number (1, 2, 3, 4)

n is the new access level (0, 1, 2, 3)

p is the password level (1, 2, 3)

nov is the number of events (1 – nnn)

Each event is identified with a unique number that is incremented for each new event so that it is possible to detect missing events as there will be a ‘gap’ in the sequence of unique identifiers. The unique identifier forms part of the event record that is read or uploaded from the IED.

Note: It is no longer possible to clear Event, Fault, Maintenance, and Disturbance Records

4.9 Cyber Security Settings

Cyber Security is important enough to warrant its own IED column called **SECURITY CONFIGURATION**, located at column number 25. In addition to this new group, settings are affected in the **SYSTEM DATA**, **COMMS SYS DATA** and **VIEW RECORDS** columns.

A summary of the relevant columns is shown in Table 6. A complete listing of the settings criteria is described in the Settings and Records chapter.

Parameter	Cell Col Row	Default Setting	Available Setting	Interface Applicability	In Setting file?
Password	00 02		ASCII 33 to 122	All	Yes
Access Level	00 D0		0 = Read Some, 1 = Read All, 2 = Read All + Write Some, 3 = Read All + Write All	All	Yes, Not Settable
Password Level 1	00 D2		ASCII 33 to 122	All	Yes
Password Level 2	00 D3		ASCII 33 to 122	All	Yes
Password Level 3	00 D4		ASCII 33 to 122	All	Yes
Security Feature	00 DF		1	All	Yes, Not Settable
SECURITY CONFIG	25 00			All	Yes
Use Banner	25 01	ACCESS ONLY FOR AUTHORISED USERS	ASCII 32 to 163	All	Yes
Attempts Limit	25 02	3	0 to 3 step 1	All	Yes
Attempts Timer	25 03	2	1 to 3 step 1	All	Yes
Blocking Timer	25 04	5	1 to 30 step 1	All	Yes
Front Port	25 05	Enabled	0 = Disabled or 1 = Enabled	All	No
Rear Port 1	25 06	Enabled	0 = Disabled or 1 = Enabled	All	No
Rear Port 2	25 07	Enabled	0 = Disabled or 1 = Enabled	All	No
Ethernet Port*	25 08	Enabled	0 = Disabled or 1 = Enabled	All	No
Courier Tunnel*†	25 09	Enabled	0 = Disabled or 1 = Enabled	All	No
IEC61850*†	25 0A	Enabled	0 = Disabled or 1 = Enabled	All	No
Attempts Remain	25 11			All	Yes, Not Settable
Blk Time Remain	25 12			All	Yes, Not Settable
Fallbck PW Level	25 20	0	0 = Password Level 0, 1 = Password Level 1, 2 = Password Level 2, 3 = Password Level 3	All	Yes, Not Settable

Parameter	Cell Col Row	Default Setting	Available Setting	Interface Applicability	In Setting file?
Security Code	25 FF			UI Only	No
Evt Unique Id (Normal Extraction)	01 FE			All	No
Evt Iface Source ± (Bits 0 - 7 of Event State)	01 FA			All	No
Evt Access Level ± (Bits 15 - 8 of Event State)	01 FB			All	No
Evt Extra Info 1 ± (Bits 23 - 16 of Event State)	01 FC			All	No
Evt Extra Info 2 ±Ω (Bits 31 - 24 of Event State)	01 FD			All	No

Table 6: Security cells summary

Where:

* - These cells will not be present in a non-Ethernet product

† - These cells will be invisible if the Ethernet port is disabled

± - These cells invisible if event is not a Security event

Ω - This cell is invisible in current phase as it does not contain any data. It is reserved for future use.

INSTALLATION

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

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1 RECEIPT OF RELAYS

Protective relays, although generally of robust construction, require careful treatment prior to installation on site. On receipt, relays should be examined immediately to ensure no external damage has been sustained in transit. If damage has been sustained, a claim should be made to the transport contractor and General Electric should be promptly notified.

Relays that are supplied unmounted and not intended for immediate installation should be returned to their protective polythene bags and delivery carton. Section 3 gives more information about the storage of relays.

2 HANDLING OF ELECTRONIC EQUIPMENT

A person's normal movements can easily generate electrostatic potentials of several thousand volts. Discharge of these voltages into semiconductor devices when handling electronic circuits can cause serious damage that, although not always immediately apparent, will reduce the reliability of the circuit. This is particularly important to consider where the circuits use complementary metal oxide semiconductors (CMOS), as is the case with these relays.

The relay's electronic circuits are protected from electrostatic discharge when housed in the case. Do not expose them to risk by removing the front panel or printed circuit boards unnecessarily.

Each printed circuit board incorporates the highest practicable protection for its semiconductor devices. However, if it becomes necessary to remove a printed circuit board, the following precautions should be taken to preserve the high reliability and long life for which the relay has been designed and manufactured.

1. Before removing a printed circuit board, ensure that you are at the same electrostatic potential as the equipment by touching the case.
2. Handle analog input modules by the front panel, frame or edges of the circuit boards. Printed circuit boards should only be handled by their edges. Avoid touching the electronic components, printed circuit tracks or connectors.
3. Do not pass the module to another person without first ensuring you are both at the same electrostatic potential. Shaking hands achieves equipotential.
4. Place the module on an anti-static surface, or on a conducting surface that is at the same potential as yourself.
5. If it is necessary to store or transport printed circuit boards removed from the case, place them individually in electrically conducting anti-static bags.

In the unlikely event that you are making measurements on the internal electronic circuitry of a relay in service, it is preferable that you are earthed to the case with a conductive wrist strap. Wrist straps should have a resistance to ground between 500 kΩ to 10 MΩ. If a wrist strap is not available you should maintain regular contact with the case to prevent a build-up of electrostatic potential. Instrumentation which may be used for making measurements should also be earthed to the case whenever possible.

More information on safe working procedures for all electronic equipment can be found in BS EN 100015: Part 1:1992. It is strongly recommended that detailed investigations on electronic circuitry or modification work should be carried out in a special handling area such as described in the aforementioned British Standard document.

3 STORAGE

If relays are not to be installed immediately upon receipt, they should be stored in a place free from dust and moisture in their original cartons. Where de-humidifier bags have been included in the packing they should be retained. The action of the de-humidifier crystals will be impaired if the bag is exposed to ambient conditions and may be restored by gently heating the bag for about an hour prior to replacing it in the carton.

To prevent battery drain during transportation and storage a battery isolation strip is fitted during manufacture. With the lower access cover open, presence of the battery isolation strip can be checked by a red tab protruding from the positive side.

Care should be taken on subsequent unpacking that any dust that has collected on the carton does not fall inside. In locations of high humidity the carton and packing may become impregnated with moisture and the de-humidifier crystals will lose their efficiency.

Prior to installation, relays should be stored at a temperature of between –25º to +70ºC (-13ºF to +158ºF).

4 UNPACKING

Care must be taken when unpacking and installing the relays so that none of the parts are damaged and additional components are not accidentally left in the packing or lost. Ensure that any User's CDROM or technical documentation is NOT discarded - this should accompany the relay to its destination substation.

Note: With the lower access cover open, the red tab of the battery isolation strip will be seen protruding from the positive side of the battery compartment. Do not remove this strip because it prevents battery drain during transportation and storage and will be removed as part of the commissioning tests.

Relays must only be handled by skilled persons.

The site should be well lit to facilitate inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies to installations that are being carried out at the same time as construction work.

5 P34x RELAY MOUNTING

MiCOM relays are dispatched either individually or as part of a panel/rack assembly.

Individual relays are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centers. This information can also be found in the product publication.

Secondary front covers can also be supplied as an option item to prevent unauthorized changing of settings and alarm status. They are available in sizes 40TE (GN0037 001) and 60TE/80TE (GN0038 001) for P34xxxxxxxxxxA/B/C and sizes 40TE (GN0242 001) and 60TE/80TE (GN0243 001) for P34xxxxxxxxxxJ/K/M/P.

The design of the relay is such that the fixing holes in the mounting flanges are only accessible when the access covers are open and hidden from sight when the covers are closed.

If a P991 or MMLG test block is to be included, it is recommended that, when viewed from the front, it be positioned on the right-hand side of the relay (or relays) with which it is associated. This minimizes the wiring between the relay and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

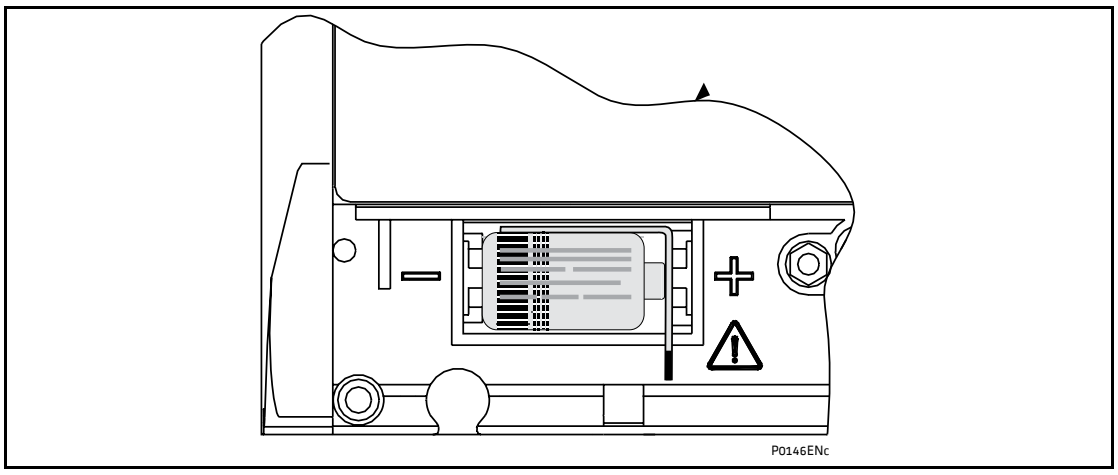


Figure 1: Location of battery isolation strip

If it is necessary to test correct relay operation during the installation, the battery isolation strip can be removed but should be replaced if commissioning of the scheme is not imminent. This will prevent unnecessary battery drain during transportation to site and installation. The red tab of the isolation strip can be seen protruding from the positive side of the battery compartment when the lower access cover is open. To remove the isolation strip, pull the red tab whilst lightly pressing the battery to prevent it falling out of the compartment. When replacing the battery isolation strip, ensure that the strip is refitted as shown in Figure 1, which is with the strip behind the battery with the red tab protruding.

5.1 Rack mounting

MiCOM relays may be rack mounted using single tier rack frames (our part number FX0021 101), as shown in Figure 2. These frames have been designed to have dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483 mm rack system this enables combinations of widths of case up to a total equivalent of size 80TE to be mounted side by side.

The two horizontal rails of the rack frame have holes drilled at approximately 26 mm intervals and the relays are attached via their mounting flanges using M4 Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

Note: Conventional self-tapping screws, including those supplied for mounting MiDOS relays, have marginally larger heads which can damage the front cover molding if used.

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

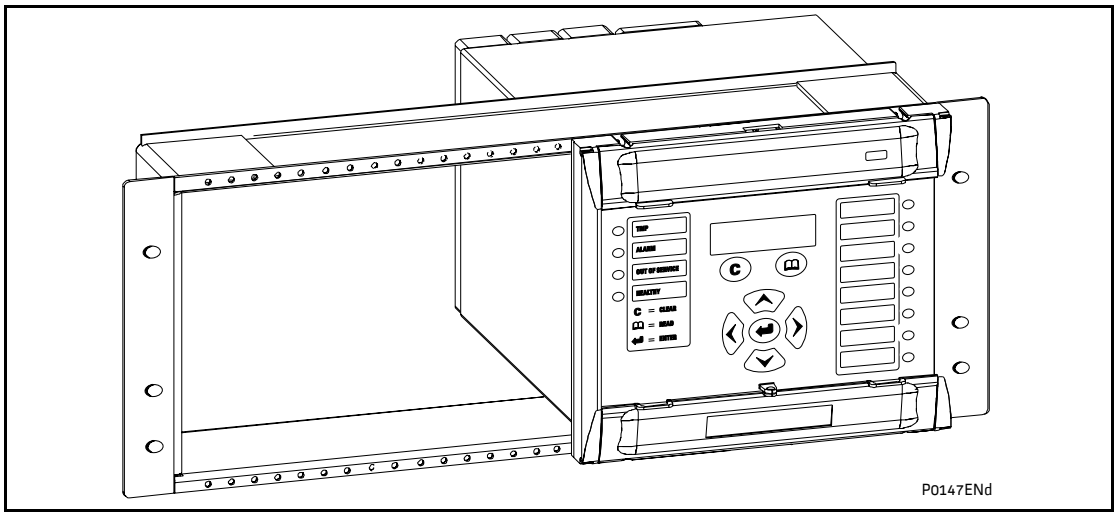


Figure 2: Rack mounting of relays

Relays can be mechanically grouped into single tier (4U) or multi-tier arrangements by means of the rack frame. This enables schemes using products from the MiCOM and MiDOS product ranges to be pre-wired together prior to mounting.

Where the case size summation is less than 80TE on any tier, or space is to be left for installation of future relays, blanking plates may be used. These plates can also be used to mount ancillary components. Table 1 shows the sizes that can be ordered.

Note: Blanking plates are only available in black.

Further details on mounting MiDOS relays can be found in publication R7012, “MiDOS Parts Catalogue and Assembly Instructions”.

Case size summation	Blanking plate part number
5TE	GJ2028 101
10TE	GJ2028 102
15TE	GJ2028 103
20TE	GJ2028 104
25TE	GJ2028 105
30TE	GJ2028 106
35TE	GJ2028 107
40TE	GJ2028 108

Table 1: Blanking plates

5.2 Panel mounting

The relays can be flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

Note: Conventional self-tapping screws, including those supplied for mounting MiDOS relays, have marginally larger heads which can damage the front cover molding if used.

Alternatively tapped holes can be used if the panel has a minimum thickness of 2.5 mm.

For applications where relays need to be semi-projection or projection mounted, a range of collars are available. Further details can be obtained from the Contracts Department of General Electric.

Where several relays are to be mounted in a single cut-out in the panel, it is advised that they are mechanically grouped together horizontally and/or vertically to form rigid assemblies prior to mounting in the panel.

Note: Do not fasten the relays using pop rivets as this will not allow the relay to be easily removed from the panel in the future if repair is necessary.

6 P34x RELAY WIRING

This section serves as a guide to selecting the appropriate cable and connector type for each terminal on the relay.



Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section/Safety Guide Pxxx-SG-4LM-2 or later issue and the ratings on the equipment's rating label.

6.1 Medium and heavy duty terminal block connections

Loose relays are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per relay terminal.

If required, we can supply M4 90° crimp ring terminals in three different sizes depending on wire size (see Table 3). Each type is available in bags of 100.

Part number	Wire size	Insulation color
ZB9124 901	0.25 – 1.65 mm^2 (22 - 16 AWG)	Red
ZB9124 900	1.04 – 2.63 mm^2 (16 - 14 AWG)	Blue
ZB9124 904	2.53 – 6.64 mm^2 (12 - 10 AWG)	Uninsulated*

Table 2: M4 90° crimp ring terminals

* To maintain the terminal block insulation requirements for safety, an insulating sleeve should be fitted over the ring terminal after crimping.

The following minimum wire sizes are recommended:

Current Transformers 2.5 mm^2

Auxiliary Supply, Vx 1.5 mm^2

EIA(RS)485 Port See separate section

Other Circuits 1.0 mm^2

Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0 mm^2 using ring terminals that are not pre-insulated. Where it is required to only use pre-insulated ring terminals, the maximum wire size that can be used is reduced to 2.63 mm^2 per ring terminal. If a larger wire size is required, two wires should be used in parallel, each terminated in a separate ring terminal at the relay.

The wire used for all connections to the medium and heavy duty terminal blocks, except the first rear EIA(RS)485 port and second rear EIA(RS)232/485 port, should have a minimum voltage rating of 300 Vrms.

It is recommended that the auxiliary supply wiring should be protected by a 16A high rupture capacity (HRC) fuse of type NIT or TIA. For safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.

Each opto input has selectable filtering. This allows use of a pre-set filter of ½ cycle which renders the input immune to induced noise on the wiring: although this method is secure it can be slow, particularly for intertripping. This can be improved by switching off the ½ cycle filter in which case one of the following methods to reduce ac noise should be considered. The first method is to use double pole switching on the input, the second is to use screened twisted cable on the input circuit. The recognition time of the opto inputs without the filtering is <2 ms and with the filtering is <12 ms.

6.2 EIA(RS)485 port

Connections to the first rear EIA(RS)485 port are made using ring terminals. It is recommended that a 2-core screened cable be used with a maximum total length of 1000 m or 200 nF total cable capacitance.

A typical cable specification would be:

Each core: 16/0.2 mm copper conductors PVC insulated

Nominal conductor area: 0.5 mm^2 per core

Screen: Overall braid, PVC sheathed

6.3 Ethernet port for IEC 61850-8-1 and DNP 3.0 OE (P34x) and IEC 61850-9-2 LE (P348)

Fiber Optic Port

The relays can have 100 Mbps Ethernet port. FO connection is recommended for use in permanent connections in a substation environment. The 100 Mbit port uses type ST connector, compatible with fiber multimode 50/125 µm or 62.5/125 µm - 13000 nm.

RJ-45 Metallic Port

The user can connect to either a 10Base-T or a 100Base-TX Ethernet hub; the port will automatically sense which type of hub is connected. Due to possibility of noise and interference on this part, it is recommended that this connection type be used for short-term connections and over short distance; ideally where the relays and hubs are located in the same cubicle.

The connector for the Ethernet port is a shielded RJ-45. Table 4 shows the signals and pins on the connector.

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

Table 3: Signals on the Ethernet connector

6.4 RTD connections (if applicable)

Where RTD inputs are available on a relay, the connections are made using screw clamp connectors on the rear of the relay that can accept wire sizes between 0.1 mm^2 and 1.5 mm^2. The connections between the relay and the RTDs must be made using a screened 3-core cable with a total resistance less than 25 Ω. The cable should have a minimum voltage rating of 300 Vrms.

A 3-core cable should be used even for 2-wire RTD applications, as it allows for the cable's resistance to be removed from the overall resistance measurement. In such cases the 3rd wire is connected to the 2nd wire at the point the cable is joined to the RTD.

The screen of each cable must only be earthed at one end, preferably at the relay end and must be continuous. Multiple earthing of the screen can cause circulating current to flow along the screen, which induces noise and is unsafe.

It is recommended to minimize noise pick-up in the RTD cables by keeping them close to earthed metal casings and avoiding areas of high electromagnetic and radio interference. The RTD cables should not be run adjacent to or in the same conduit as other high voltage or current cables.

A typical cable specification would be:

Each core:	7/0.2 mm copper conductors heat resistant PVC insulated
Nominal conductor area:	0.22 mm^2 per core
Screen:	Nickel-plated copper wire braid heat resistant PVC sheathed

The extract below may be useful in defining cable recommendations for the RTDs:

Noise pick up by cables can be categorized in to three types:

- Resistive
- Capacitive
- Inductive

Resistive coupling requires there to be an electrical connection to the noise source. So assuming that the wire and cable insulation is sound and that the junctions are clean then this can be dismissed.

Capacitive coupling requires there to be sufficient capacitance for the impedance path to the noise source to be small enough to allow for significant coupling. This is a function of the dielectric strength between the signal cable on the noise source and the potential (i.e. power) of the noise source.

Inductive coupling occurs when the signal cable is adjacent to a cable/wire carrying the noise or it is exposed to a radiated EMF.

Standard screened cable is normally used to protect against capacitively coupled noise, but for it to be effective the screen must only be bonded to the system ground at one point, otherwise a current could flow and the noise would be coupled in to the signal wires of the cable. There are different types of screening available, but basically there are two types: aluminum foil wrap and tin-copper braid.

Foil screens are good for low to medium frequencies and braid is good for high frequencies. High-fidelity screen cables provide both types.

Protection against magnetic inductive coupling requires very careful cable routing and magnetic shielding. The latter can be achieved with steel-armored cable and the use of steel cable trays. It is important that the armor of the cable is grounded at both ends so that the EMF of the induced current cancels the field of the noise source and hence shields the cables conductors from it. (However, the design of the system ground must be considered and care taken to not bridge two isolated ground systems since this could be hazardous and defeat the objectives of the original ground design). The cable should be laid in the cable trays as close as possible to the metal of the tray and under no circumstance should any power cable be in or near to the tray. (Power cables should only cross the signal cables at 90 degrees and never be adjacent to them).

Clearly, both the capacitive and inductive screens must be contigous from the RTD probes to the relay terminals.

The best types of cable are those provided by the RTD manufactures. These tend to be three conductors (a so call "triad") which are screened with foil. Such triad cables are available in armored forms as well as multi-triad armored forms.

6.5 Current loop input output (CLIO) connections (if applicable)

Where current loop inputs and outputs are available on a relay, the connections are made using screw clamp connectors, as per the RTD inputs, on the rear of the relay which can accept wire sizes between 0.1 mm^2 and 1.5 mm^2. It is recommended that connections between the relay and the current loop inputs and outputs are made using a screened cable. The wire should have a minimum voltage rating of 300 Vrms.

6.6 IRIG-B connections (if applicable)

The IRIG-B input has a BNC connection. It is recommended that the cable and connector have a characteristic impedance of 50 Ω. It is also recommended that connections between the IRIG-B equipment and the relay are made using coaxial cable 50 Ω characteristic impedance with a halogen free, fire retardant sheath, type RG58LSF.

6.7 EIA(RS)232 port

Short term connections to the EIA(RS)232 port, located behind the bottom access cover, can be made using a screened multi-core communication cable up to 15 m long, or a total capacitance of 2500 pF. The cable should be terminated at the relay end with a 9-way, metal shelled, D-type male plug. Section 1.9 of *P34x/EN GS* of this manual details the pin allocations.

6.8 Download/monitor port

Short term connections to the download/monitor port, located behind the bottom access cover, can be made using a screened 25-core communication cable up to 4 m long. The cable should be terminated at the relay end with a 25-way, metal shelled, D-type male plug. Section 1.9 of *P34x/EN GS* and section 3.5 of *P34x/EN CM* of this manual details the pin allocations.

6.9 Second EIA(RS)232/485 port

Relays with Courier, MODBUS, IEC 60870-5-103 or DNP3 protocol on the first rear communications port have the option of a second rear port, running Courier language. The second rear communications port can be used over one of three physical links: twisted pair K-Bus (non-polarity sensitive), twisted pair EIA(RS)485 (connection polarity sensitive) or EIA(RS)232[1].

6.9.1 Connection to the second rear port

The second rear Courier port connects via a 9-way female D-type connector (SK4) in the middle of the card end plate (in between IRIG-B connector and lower D-type). The connection is compliant to EIA(RS)574.

For IEC 60870-5-2 over EIA(RS)232/574

Pin	Connection
1	No Connection
2	RxD
3	TxD
4	DTR#
5	Ground
6	No Connection
7	RTS#
8	CTS#
9	No Connection

Table 4: Second rear port RS232 connection

Connections to the second rear port configured for EIA(RS)232 operation can be made using a screened multi-core communication cable up to 15 m long, or a total capacitance of 2500 pF. The cable should be terminated at the relay end with a 9-way, metal shelled, D-type male plug. The table above details the pin allocations.

For K-bus or IEC 60870-5-2 over EIA(RS)485

IN

[1] This port is actually compliant to EIA(RS)574; the 9-pin version of EIA(RS)232, see www.tiaonline.org.

Pin*	Connection
4	EIA(RS)485 - 1 (+ ve)
7	EIA(RS)485 - 2 (- ve)

Table 5: Second rear port RS485 connection

* - All other pins unconnected.

- These pins are control lines for use with a modem.

NOTES:

Connector pins 4 and 7 are used by both the EIA(RS)232/574 and EIA(RS)485 physical layers, but for different purposes. Therefore, the cables should be removed during configuration switches.

For the EIA(RS)485 protocol an EIA(RS)485 to EIA(RS)232/574 converter will be required to connect a modem or PC running S1, to the relay.

EIA(RS)485 is polarity sensitive, with pin 4 positive (+) and pin 7 negative (-).

The K-Bus protocol can be connected to a PC via a KITZ101 or 102.

It is recommended that a 2-core screened cable be used. To avoid exceeding the second communications port flash clearances it is recommended that the length of cable between the port and the communications equipment should be less than 300 m. This length can be increased to 1000 m or 200 nF total cable capacitance if the communications cable is not laid in close proximity to high current carrying conductors. The cable screen should be earthed at one end only.

A typical cable specification would be:

Each core:	16/0.2 mm copper conductors PVC insulated
Nominal conductor area:	0.5 mm^2 per core
Screen:	Overall braid, PVC sheathed

6.10 Protective conductor (earth) connection

Every relay must be connected to the local earth bar using the M4 earth studs in the bottom left hand corner of the relay case. The minimum recommended wire size is 2.5 mm^2 and should have a ring terminal at the relay end. Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0 mm^2 per wire. If a greater cross-sectional area is required, two parallel connected wires, each terminated in a separate ring terminal at the relay, or a metal earth bar could be used.

Note: To prevent any possibility of electrolytic action between brass or copper earth conductors and the rear panel of the relay, precautions should be taken to isolate them from one another. This could be achieved in a number of ways, including placing a nickel-plated or insulating washer between the conductor and the relay case, or using tinned ring terminals.

6.11 Field voltage connection

A new power supply module is implemented in the P34xxxxxxxxxxM/P relays. In the new PSU modules the 48V field voltage used to drive opto inputs has been removed. For the older models, the field voltage occupies terminals F/J/M 7, 8, 9 and 10 (dependant on the model) of the power supply board, which is shown on some of the connection diagrams. For the new models, it is important NOT to make any connections to these terminals.

7 P34x CASE DIMENSIONS

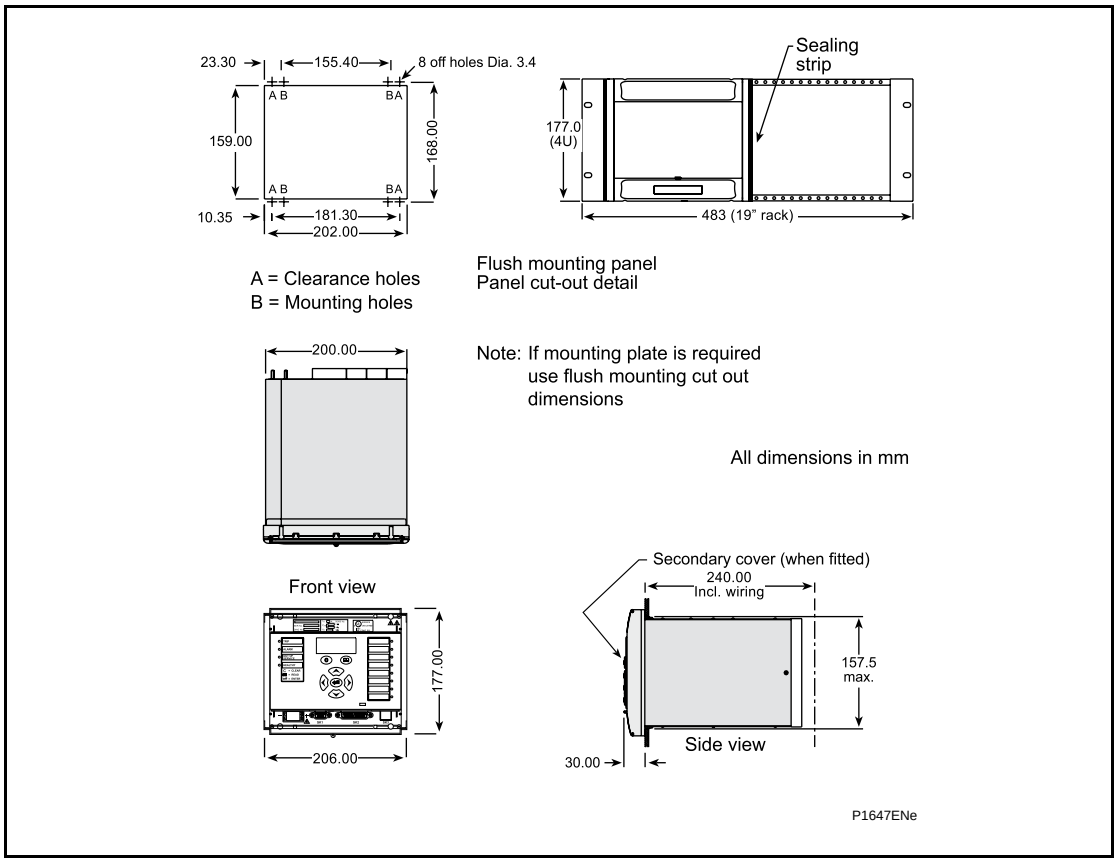


Figure 3: P342 case dimensions (40TE case)

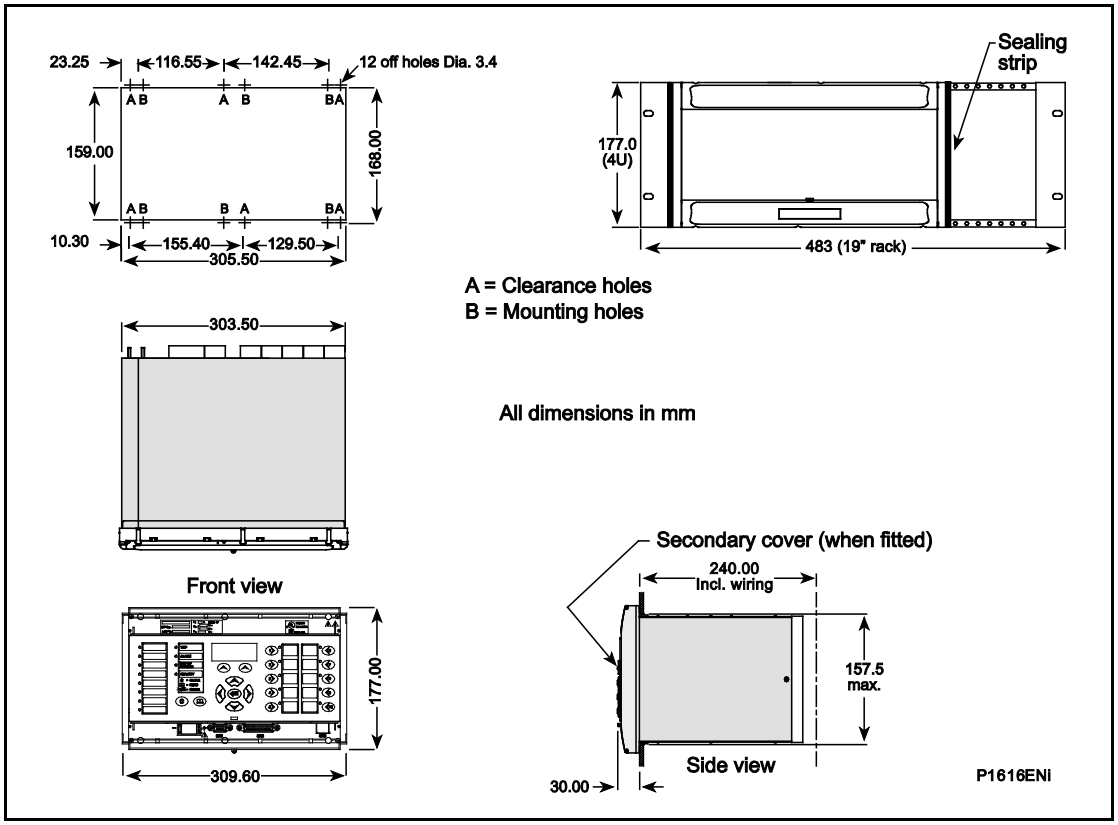


Figure 4: P343/4/6 case dimensions (60TE case)

IN

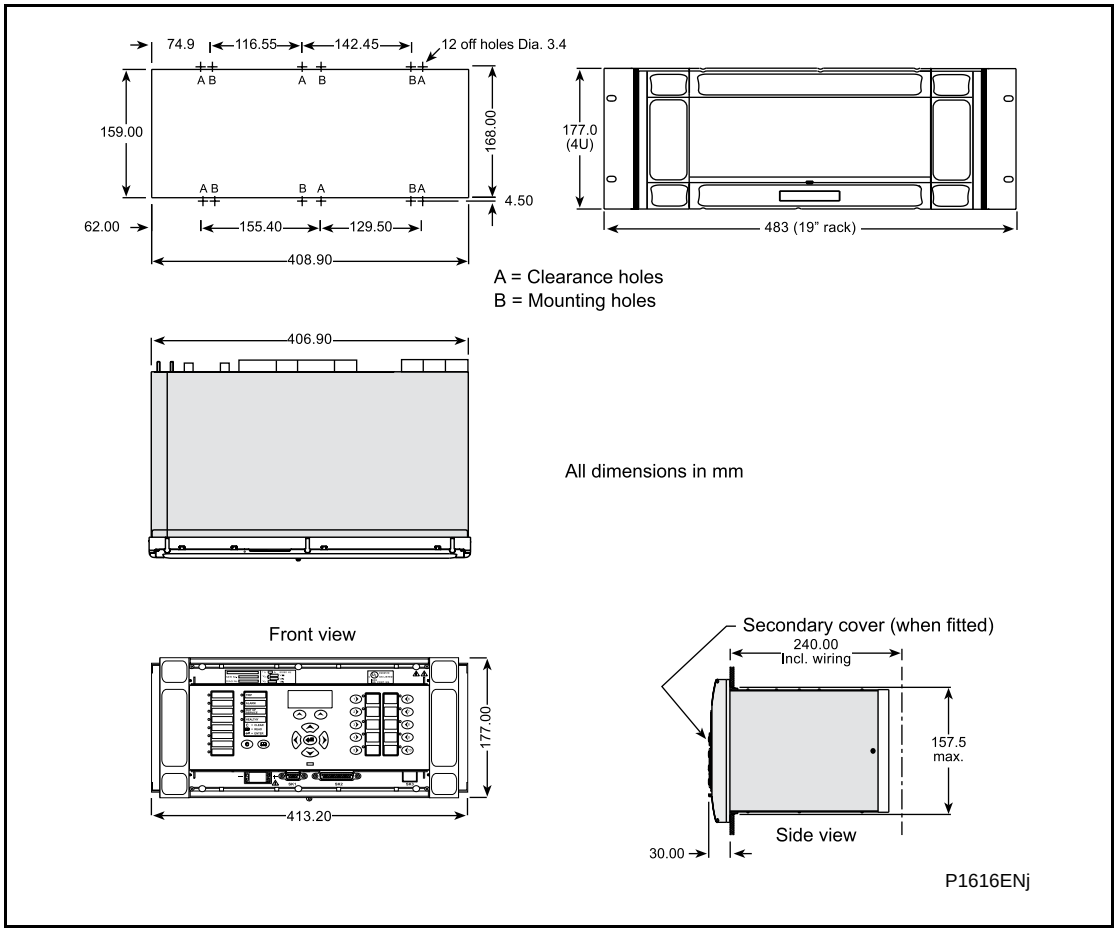


Figure 5: P343/4/5/6/8 case dimensions (80TE case)

8 P391 ROTOR EARTH FAULT UNIT (REFU) MOUNTING

The P391 unit is dispatched either individually or as part of a panel/rack/wall assembly.

Sufficient airflow must be maintained around the P391 at all times. For this reason it is essential that a minimum clearance from other equipment of 2U (89 mm) above and 1U (44.5 mm) below the P391 is maintained.

The REFU is normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centers. This information can also be found in the product publication.

8.1 Rack mounting

The P391 unit can be rack mounted into a rack with M6 x16 slotted pan head screws provided.

8.2 Panel mounting

The P391 unit can be flush mounted into panels using M4 x 8 Pan head Taptite self-tapping screws provided.

Alternatively tapped holes can be used if the panel has a minimum thickness of 2.5 mm.

8.3 Wall mounting

The P391 unit can be wall mounted using M6 anchor bolts or similar (not provided).

9 P391 ROTOR EARTH FAULT UNIT (REFU) MOUNTING

This section serves as a guide to selecting the appropriate cable and connector type for each terminal on the P391 unit.



The user shall be familiar with all safety statements listed in section 6.3.5 of the commissioning chapter and the Safety Section/Safety Guide Pxxx-SG-4LM-2 (or later issue) before undertaking any work on the P391.



Under no circumstances should the high voltage DC rotor winding supply be connected via MMLG or P990 test blocks. Both MMLG and P990 test blocks are not rated for continuous working voltages greater than 300 Vrms. These test blocks are not designed to withstand the inductive EMF voltages which will be experienced on disconnection or de-energization of the DC rotor winding supply.

9.1 Medium duty terminal block connections

Loose relays are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per relay terminal.

If required, General Electric can supply M4 90° crimp ring terminals in three different sizes depending on wire size (see Table 5). Each type is available in bags of 100.

Part number	Wire size	Insulation color
ZB9124 901	0.25 – 1.65 mm^2 (22 - 16 AWG)	Red
ZB9124 900	1.04 – 2.63 mm^2 (16 - 14 AWG)	Blue
ZB9124 904	2.53 – 6.64 mm^2 (12 - 10 AWG)	Uninsulated*

Table 6: M4 90° crimp ring terminals

*Note: To maintain the terminal block insulation requirements for safety, an insulating sleeve should be fitted over the ring terminal after crimping.

The following minimum wire sizes are recommended:

Auxiliary Supply, Vx 1.5 mm^2

Rotor winding to P391 1.0 mm^2

Other Circuits 1.0 mm^2



Wiring between the DC rotor winding and the P391 shall be suitably rated to withstand at least twice the rotor winding supply voltage to earth. This is to ensure that the wiring insulation can withstand the inductive Electro Motive Force (EMF) voltage which will be experienced on disconnection or de-energization of the DC rotor winding supply.

Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium terminals is 6.0 mm^2 using ring terminals that are not pre-insulated (protective conductor terminal (PCT) only). All P391 terminals, except PCT shall be pre-insulated ring terminals, the maximum wire size that can be used is reduced to 2.63 mm2 per ring terminal. If a larger wire size is required, two wires can be used in parallel, each terminated in a separate pre-insulated ring terminal.

Wiring between the DC rotor winding and the P391 shall be suitably rated to withstand at least twice the rotor winding supply voltage to earth. The wire used for other P391 connections to the medium duty terminal blocks should have a minimum voltage rating of 300 Vrms.

The dielectric withstand of P391 injection resistor connections (A16, B16, A8, B8) to earth is 5.8 kV rms, 1 minute.

It is recommended that the auxiliary supply wiring should be protected by a high rupture capacity (HRC) fuse of type NIT or TIA, rated between 2 A and 16 A. Other circuits should be appropriately fused to protect the wire used.

9.2 Current loop input output (CLIO) connections (if applicable)

A current loop output is available on the P391 relay, the connections are made using screw clamp connectors, on the rear of the relay which can accept wire sizes between 0.1 mm^2 and 1.5 mm^2. It is recommended that connections between the relay and the current loop inputs and outputs are made using a screened cable, connection of the screen is discussed in section 6.4. The wire should have a minimum voltage rating of 300 Vrms.

9.3 Protective conductor (earth) connection (PCT)

Every relay must be connected to the local earth bar using the M4 earth studs in the bottom left hand corner of the relay case. The minimum recommended wire size is 2.5 mm^2 and should have a ring terminal at the relay end. Due to the limitations of the ring terminal, the maximum wire size that can be used for the PCT is 6.0 mm^2 per wire. If a greater cross-sectional area is required, two parallel connected wires, each terminated in a separate ring terminal at the relay, or a metal earth bar could be used.

As DC currents of up to 29 mA will appear in the earth circuit under rotor earth fault conditions, the P391 shall be permanently connected to the local earth via the protective conductor terminal provided.

Note: To prevent any possibility of electrolytic action between brass or copper earth conductors and the rear panel of the relay, precautions should be taken to isolate them from one another. This could be achieved in a number of ways, including placing a nickel-plated or insulating washer between the conductor and the relay case, or using tinned ring terminals.

10 P391 CASE DIMENSIONS

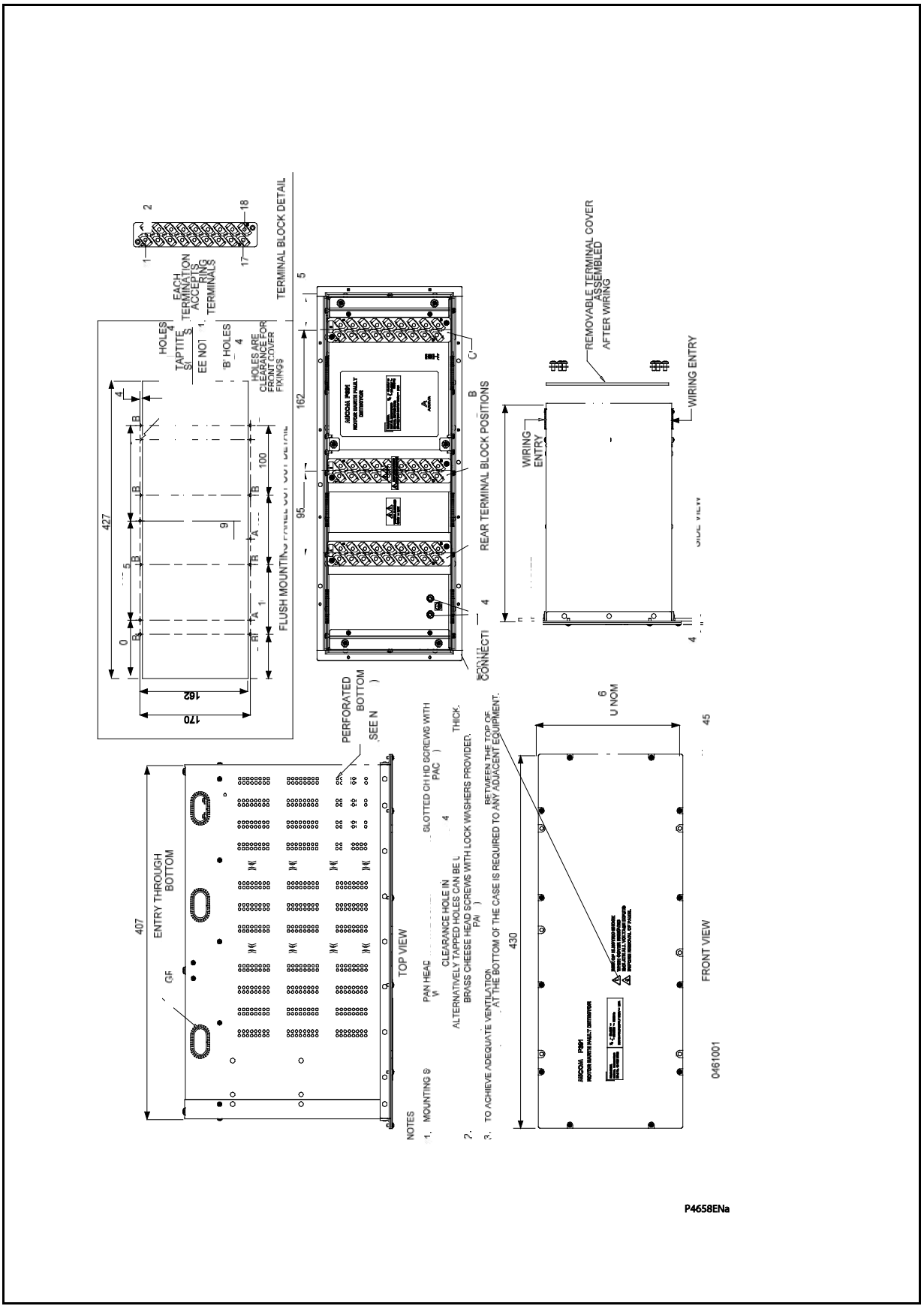


Figure 6: P391 outline and panel mounting details (80TE case)

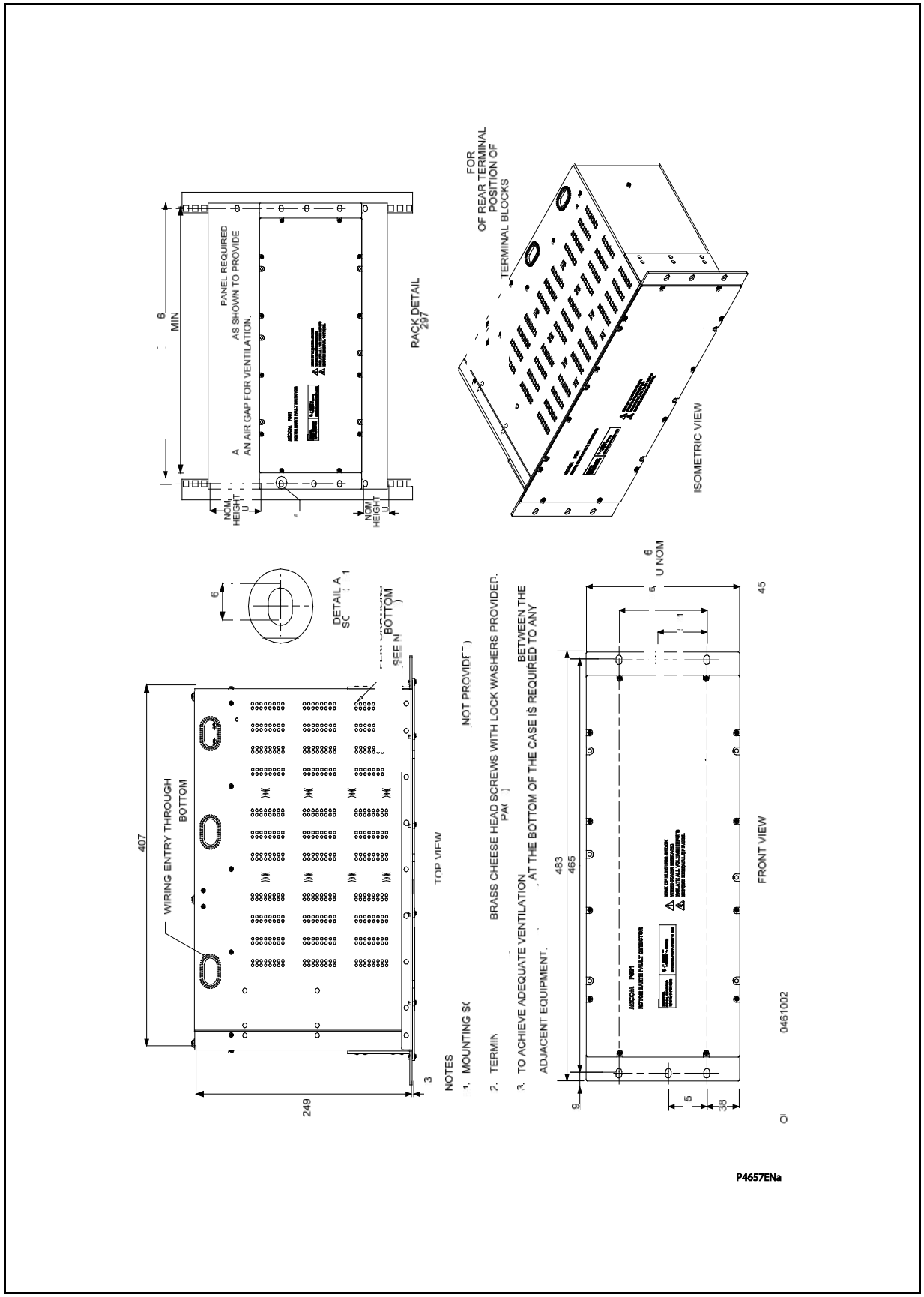


Figure 7: P391 outline and rack mounting details (80TE case)

IN

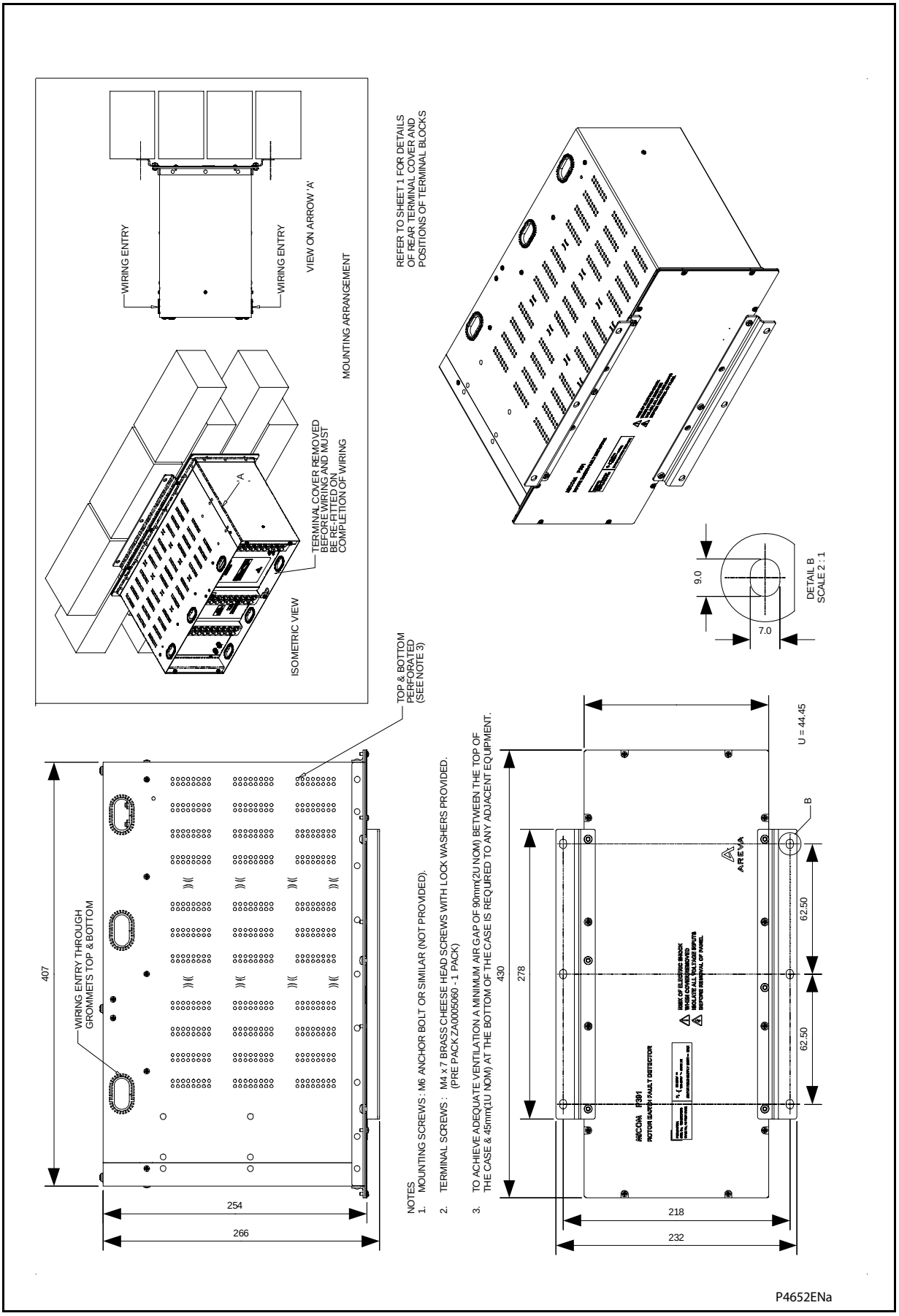


Figure 8: P391 outline and wall mounting details (80TE case)

11 ASSEMBLY DRAWINGS

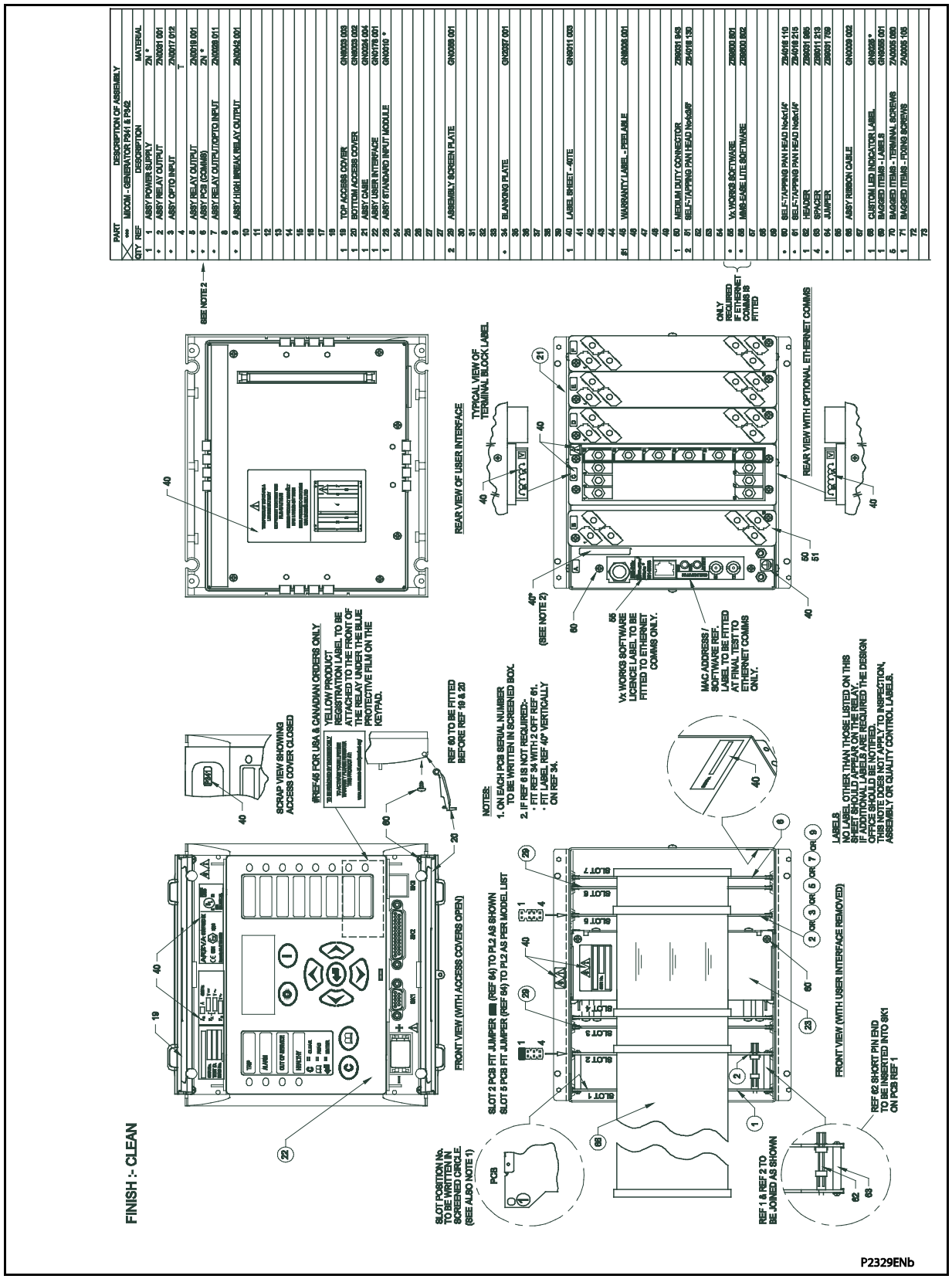


Figure 9: Assembly P341/2 generator protection relay (40TE) 8 I/P & 7 O/P with optional I/P & O/P)

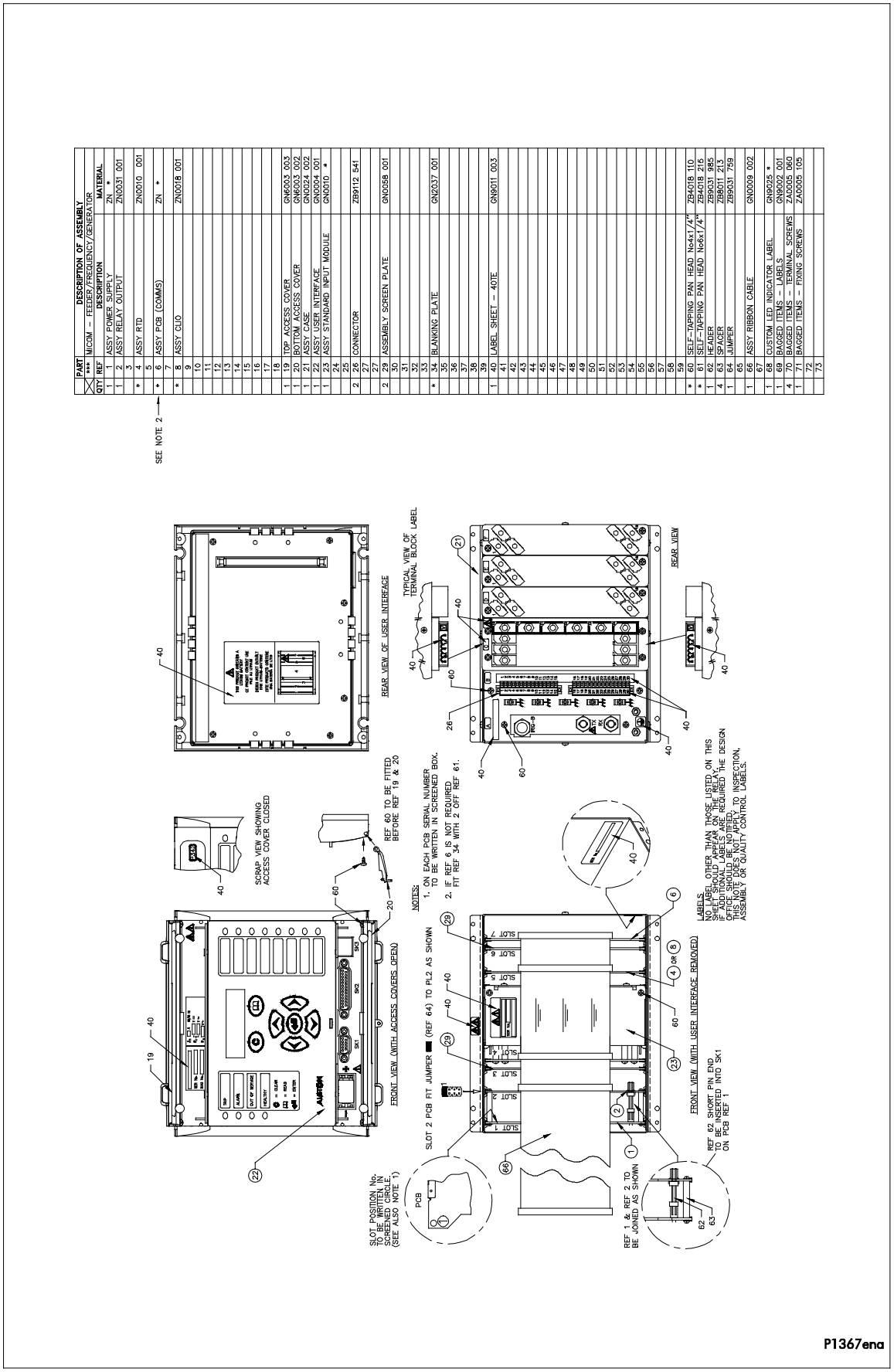


Figure 10: Assembly P342 generator protection relay (40TE) (8 I/P & 7 O/P with optional RTD & CLIO)

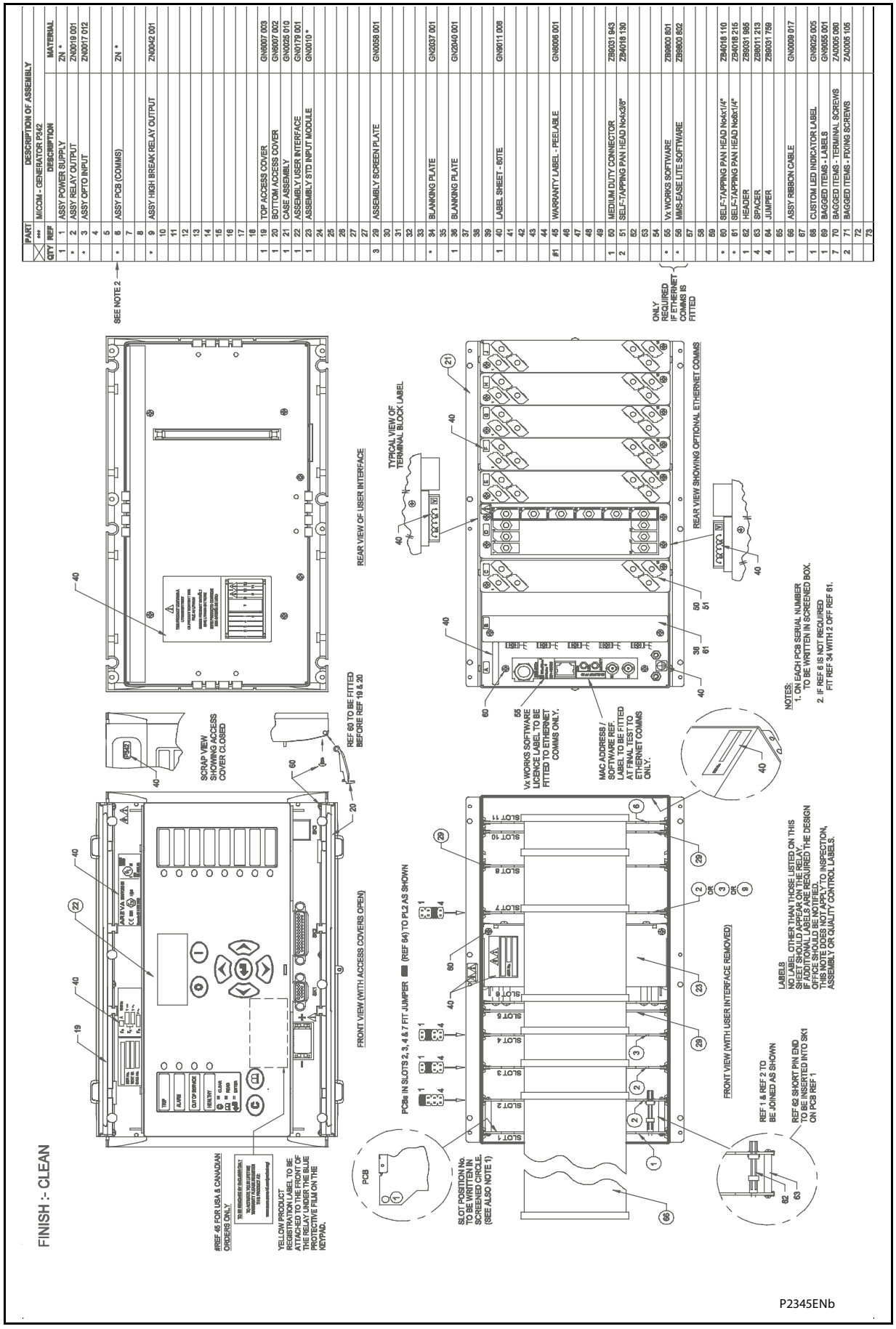


Figure 11: Assembly P342 generator protection relay (60TE) (16 I/P & 16 O/P with optional I/P & O/P)

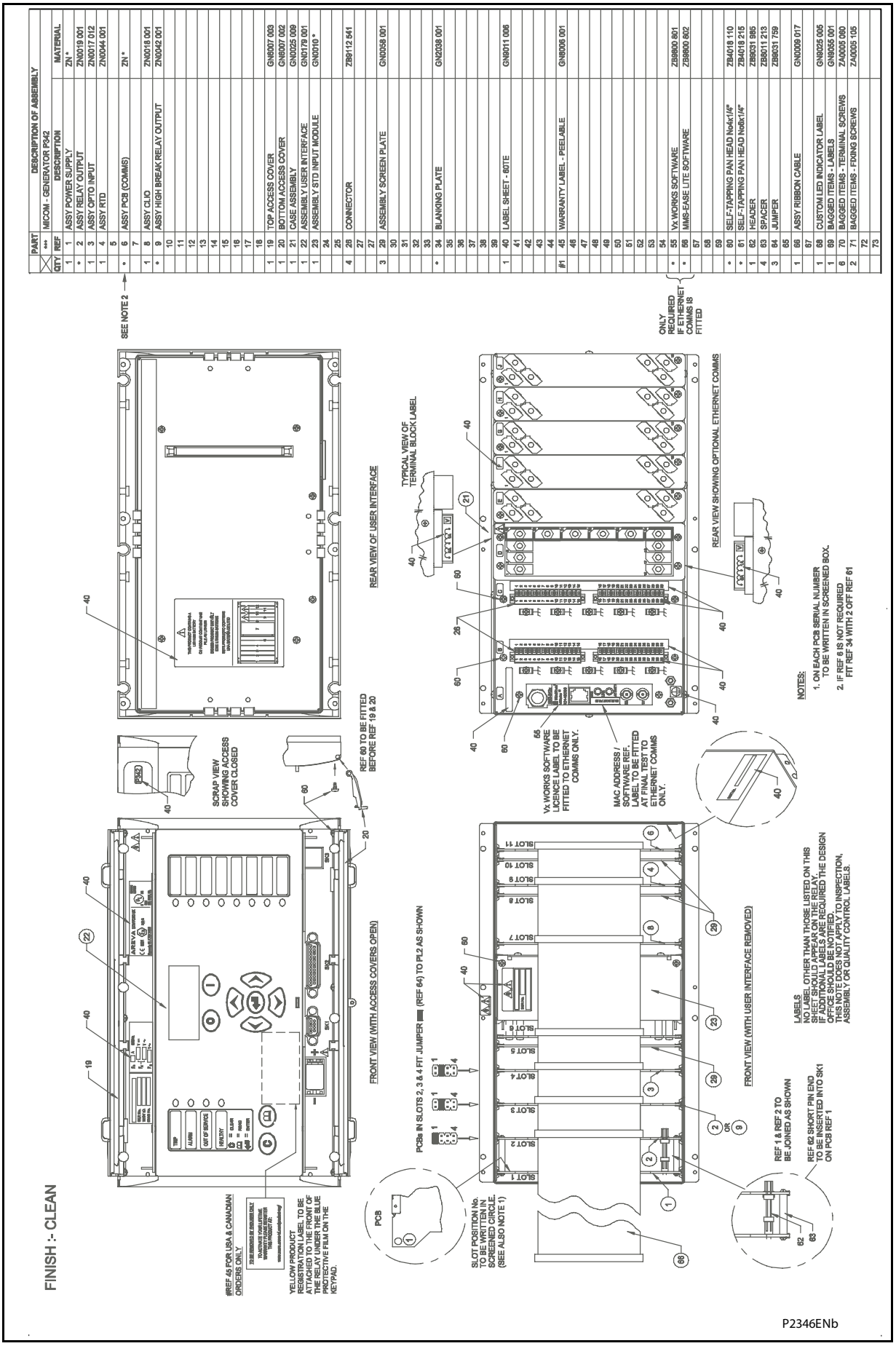


Figure 12: Assembly P342 generator protection relay (60TE) (16 I/P & 8/16 O/P with optional RTD & CLIO & HB O/P)

IN

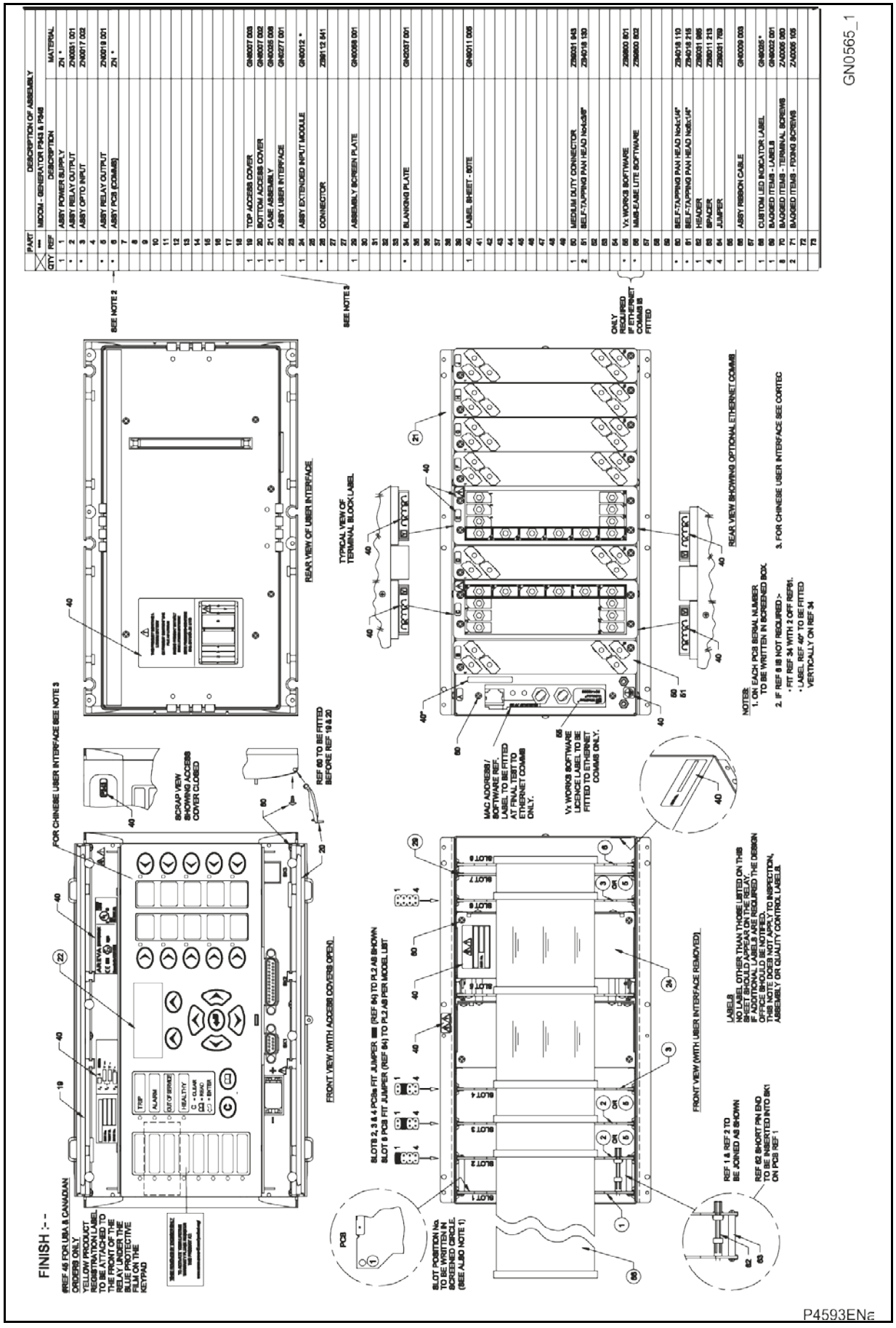


Figure 13: Assembly P343/6 generator protection relay (60TE) (16 I/P & 14 O/P with optional I/P & O/P)

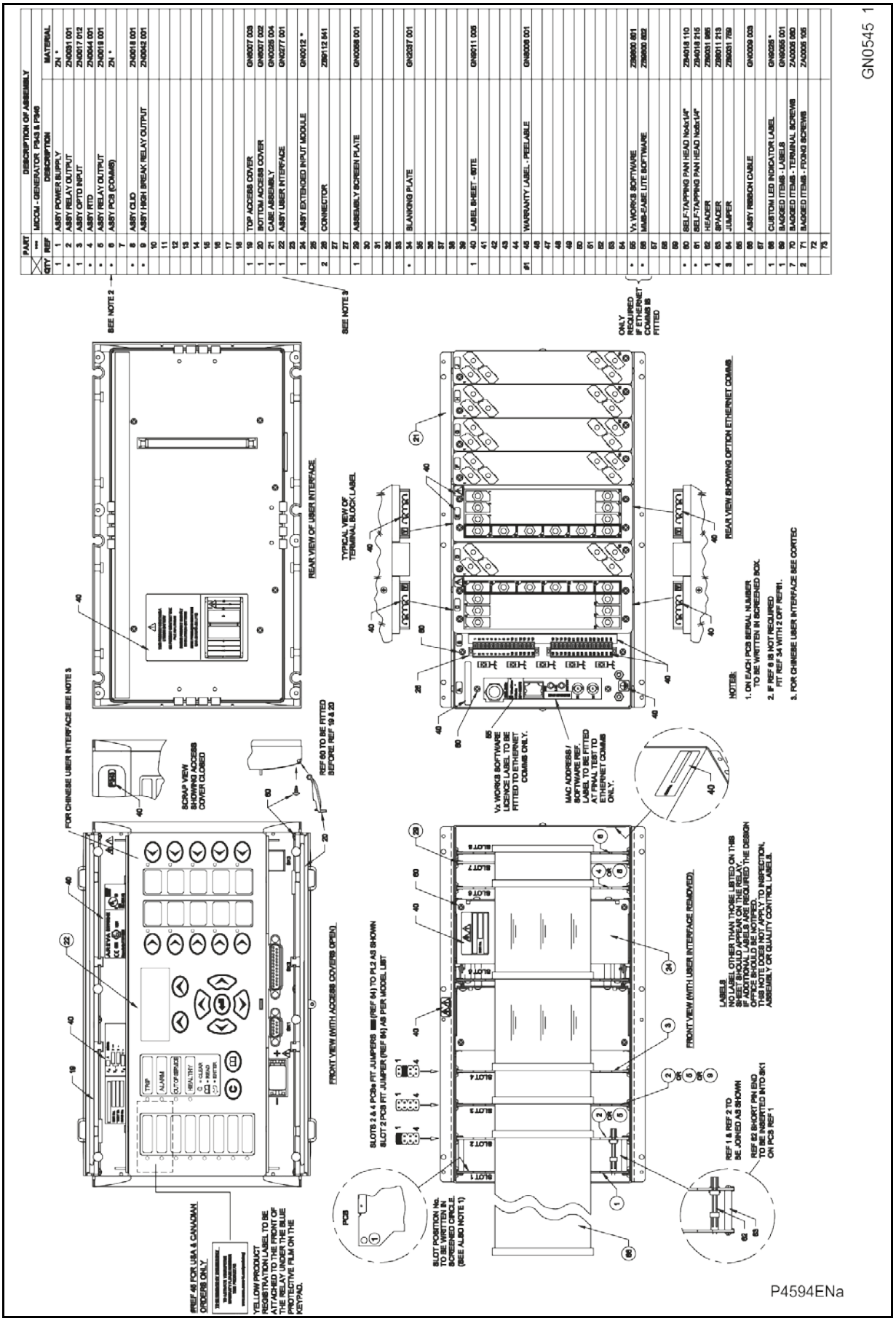


Figure 14: Assembly P343/6 generator protection relay (60TE) (16 I/P & 7/14 O/P with optional RTD & CLIO & HB O/P)

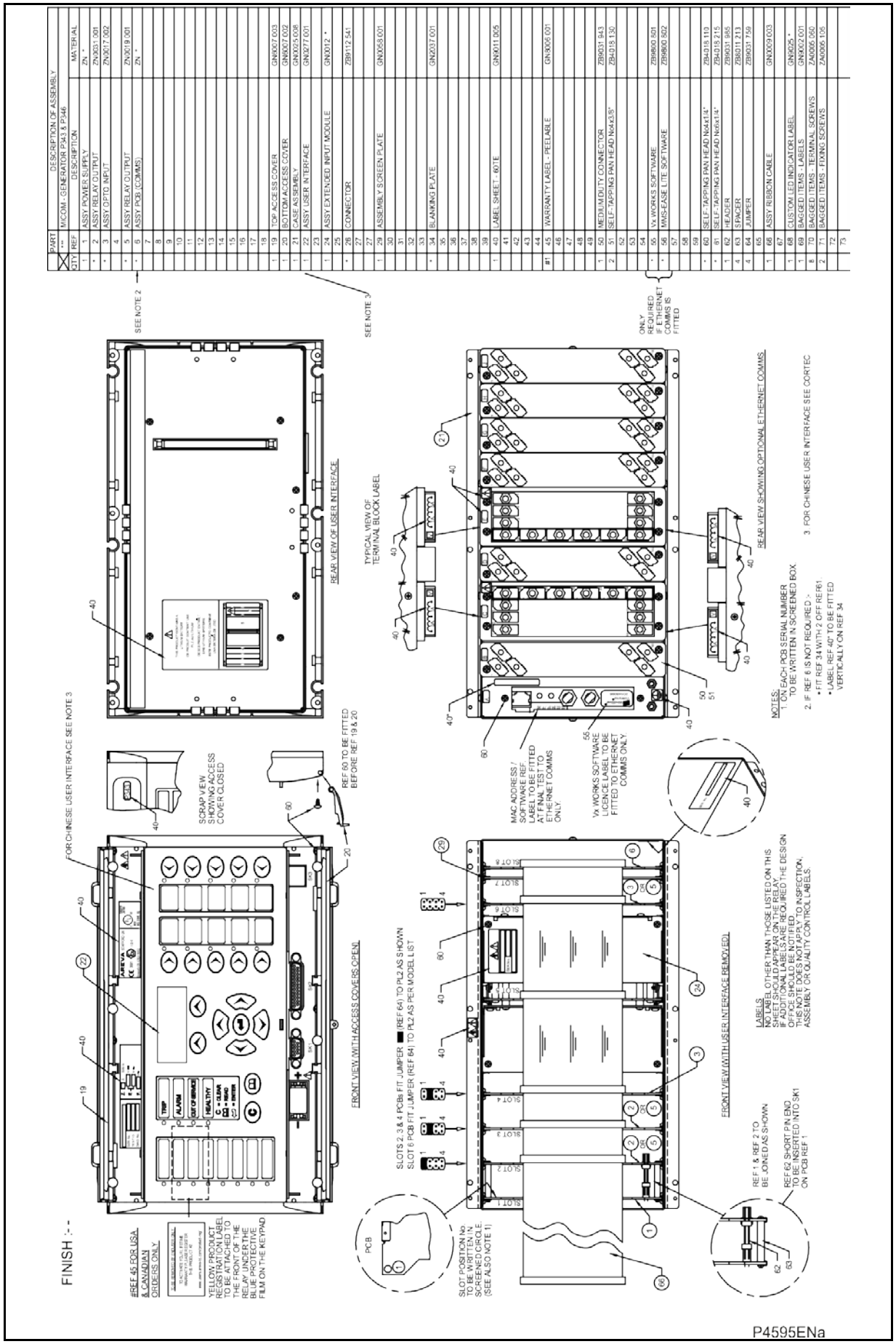


Figure 15: Assembly P343/4/6 generator protection relay (80TE) (16/24 I/P & 16/24 O/P with optional I/P & O/P)

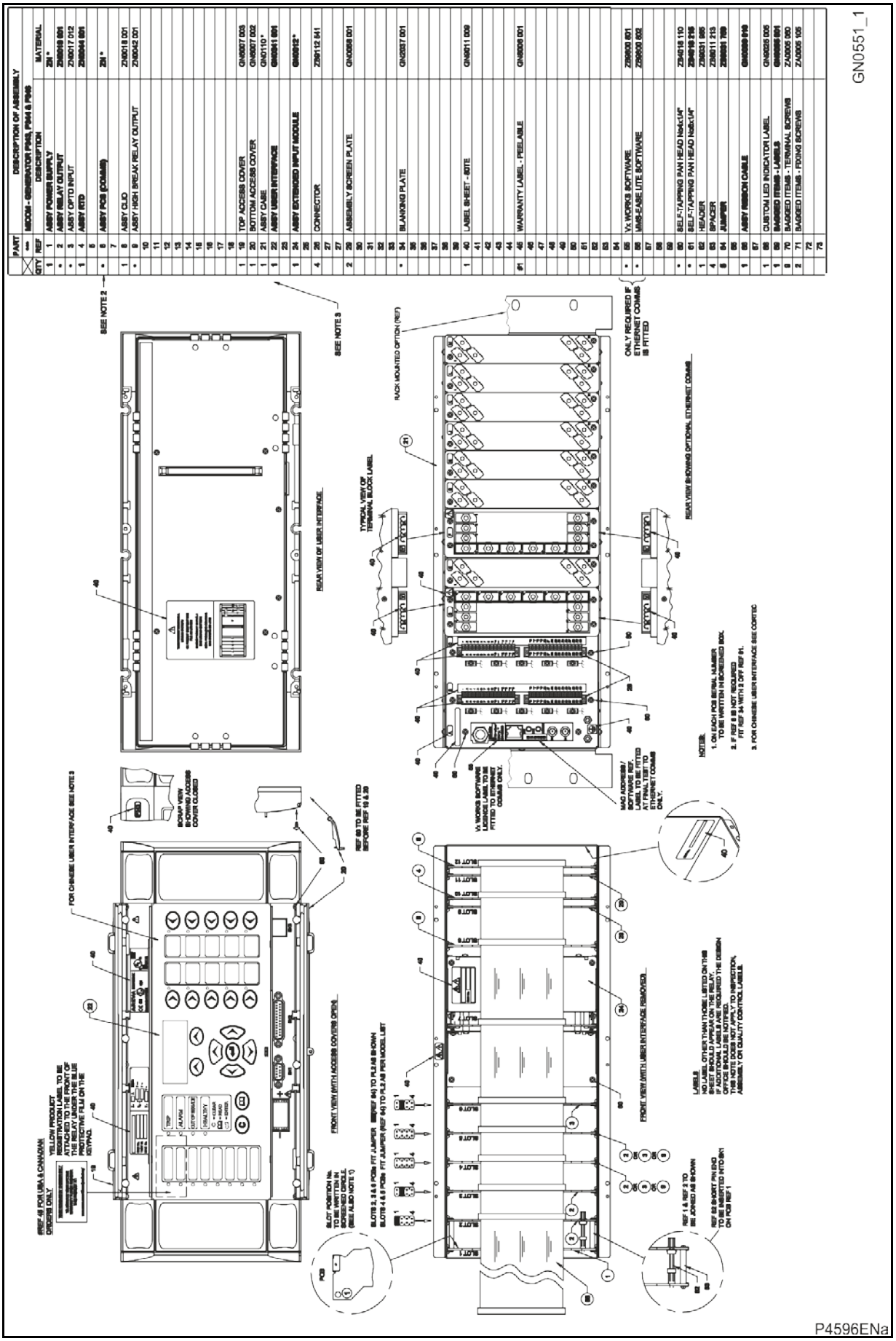


Figure 16: Assembly P343/4/6 generator protection relay (80TE) (16/24 I/P & 16/24 O/P with optional RTD & CLIO & HB O/P)

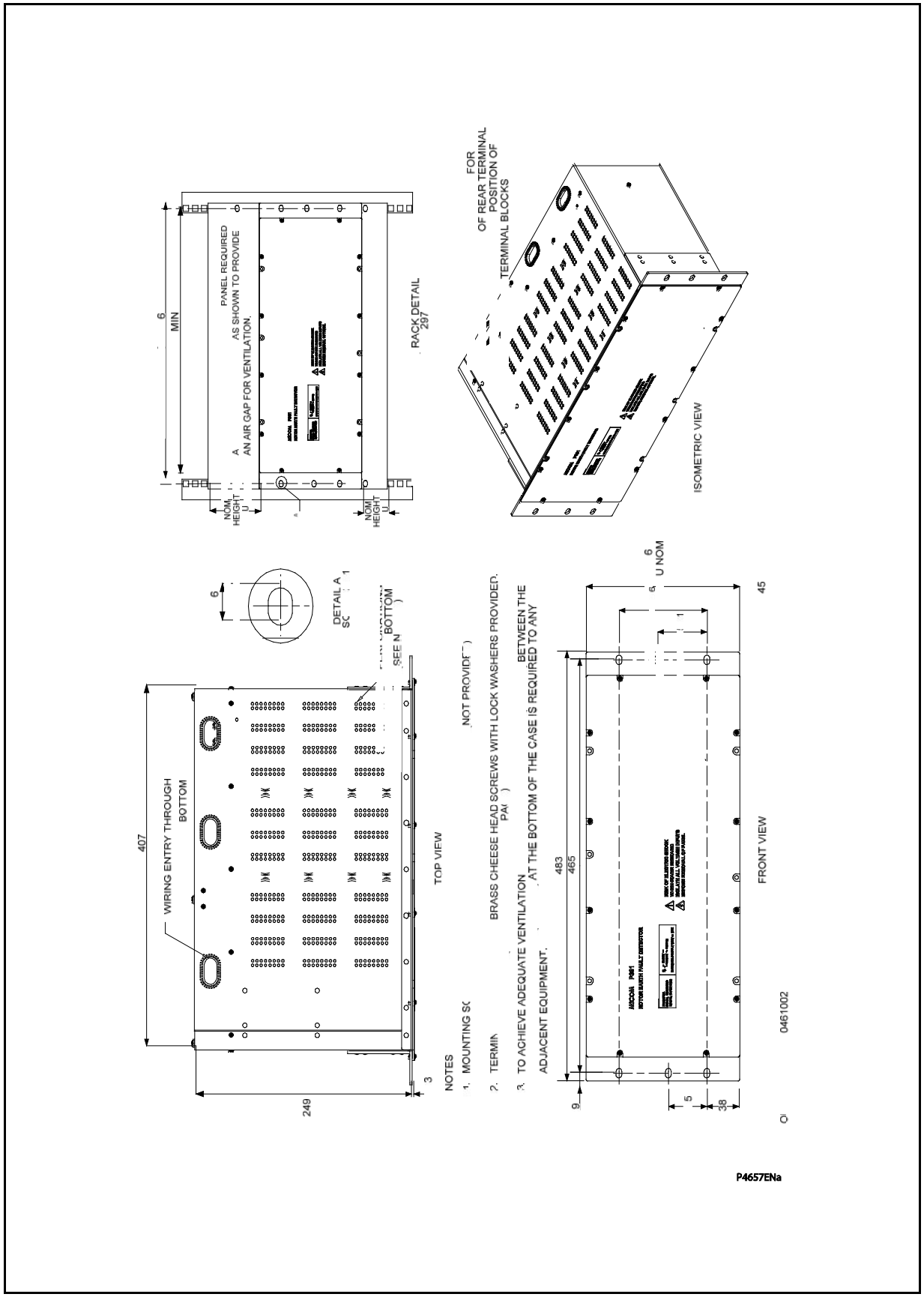


Figure 17: Final assembly drawing - P391 panel mounted

IN

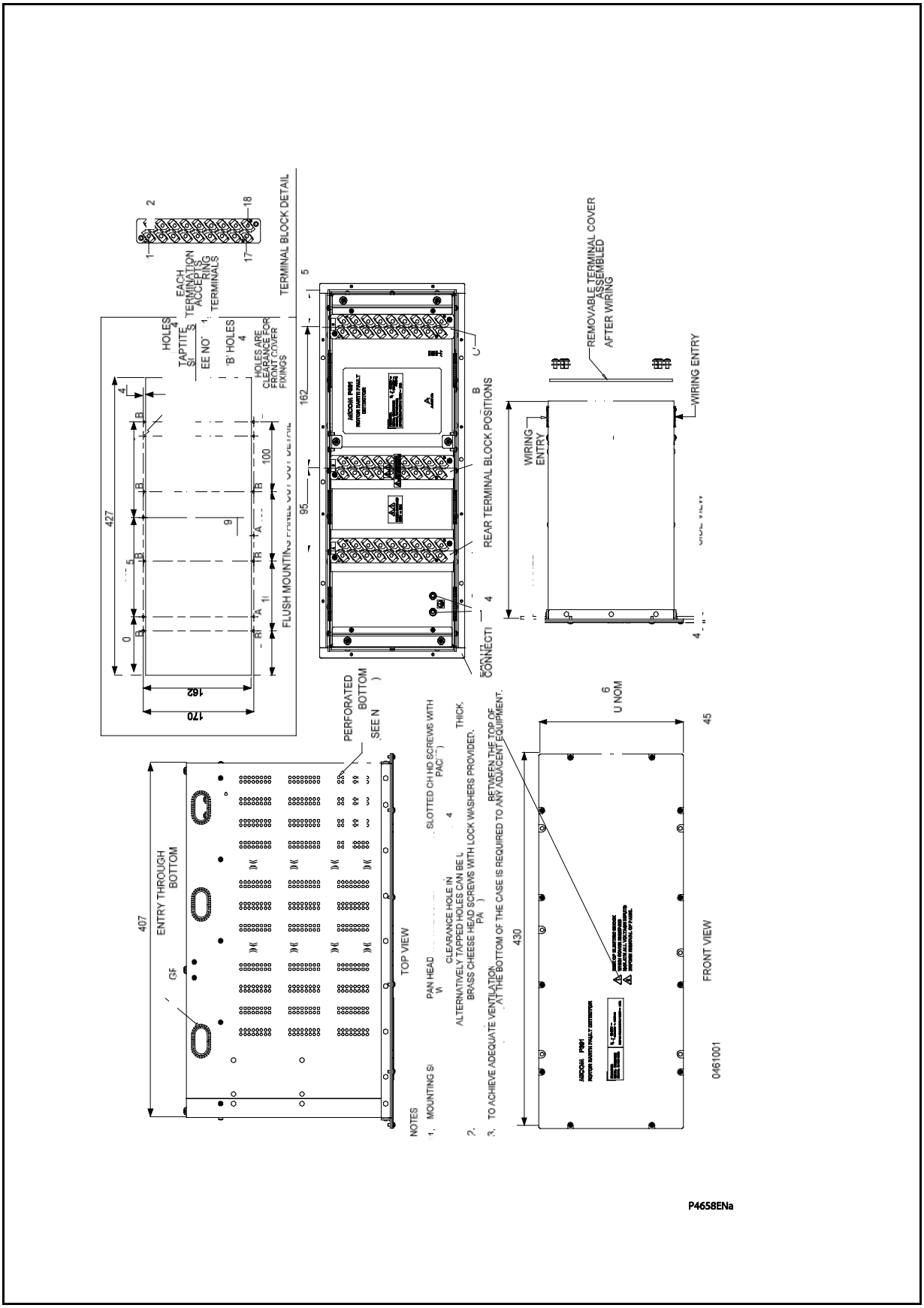


Figure 18: Final assembly drawing - P391 rack mounted

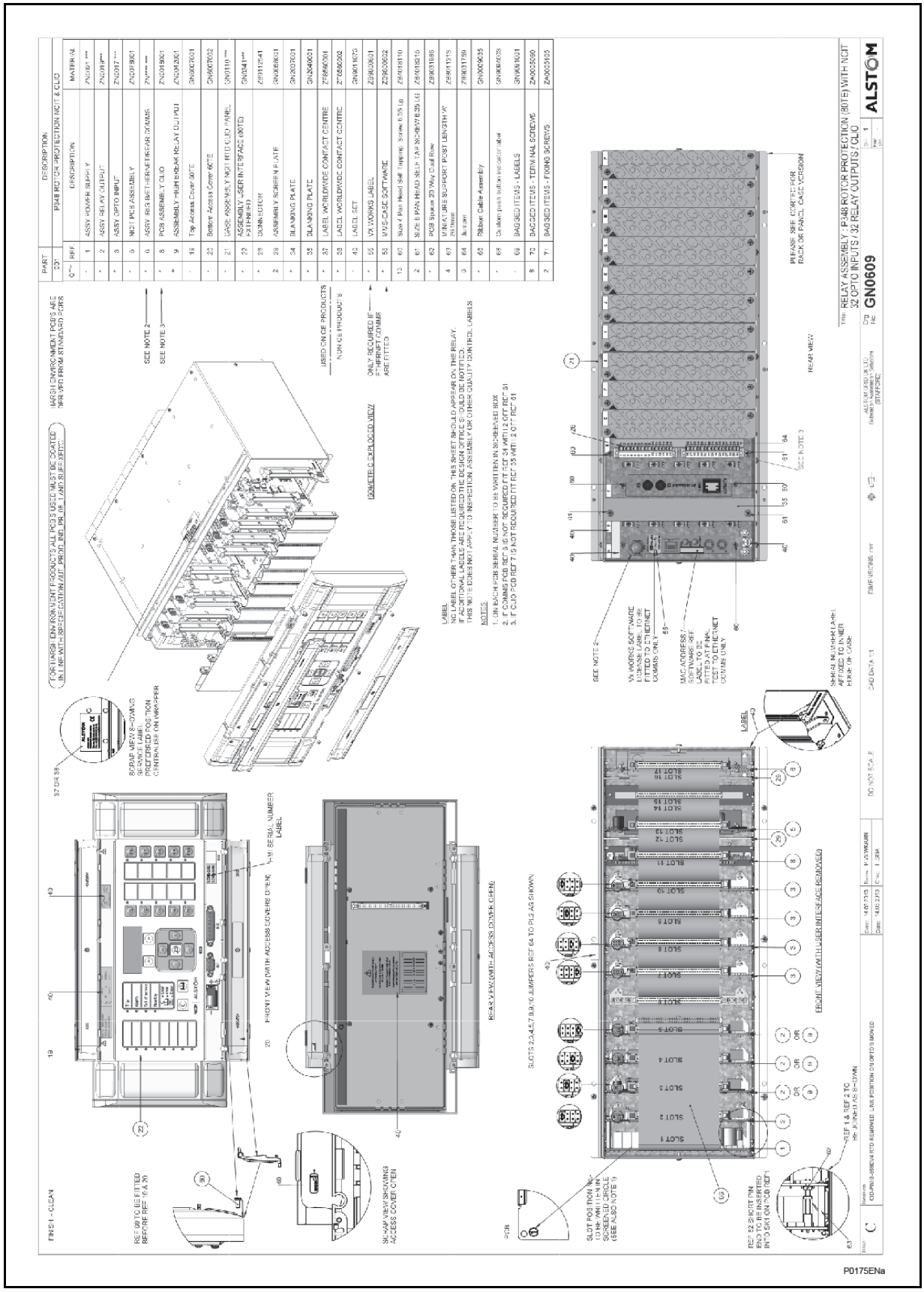
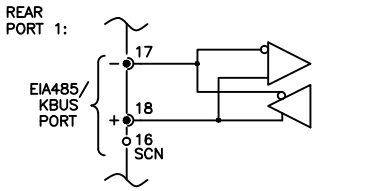


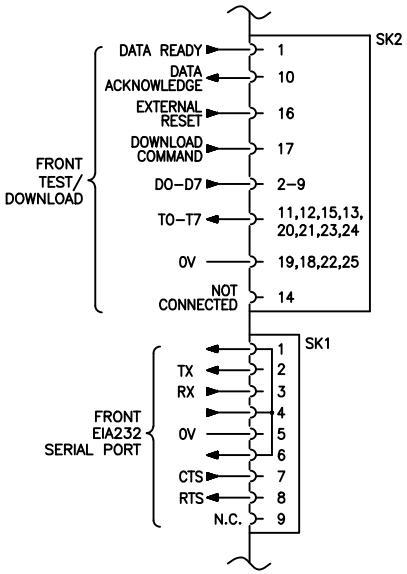
Figure 19: P348 Final assembly drawing

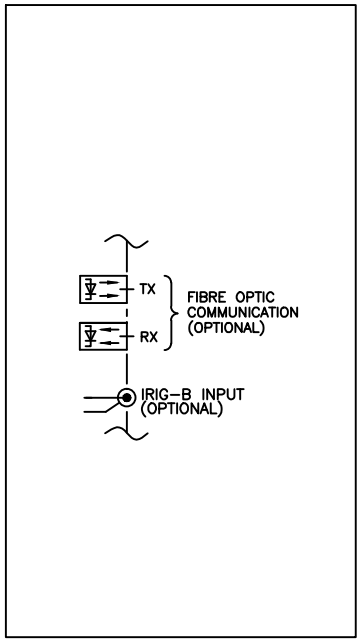
12 WIRING DIAGRAMS

Model	External Connection Diagram Title	Drawing-Sheet	Issue
All	COMMS OPTIONS MICOM Px40 PLATFORM	10Px4001-1	J
P342	GENERATOR PROTECTION RELAY (40TE) FOR GENERATOR. USING VEE CONNECTED VT's (8 I/P & 7 0/P)	10P34201-3	G
	GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR WITH SENSITIVE POWER (8 I/P & 7 0/P)	10P34201-4	E
	GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (8 I/P & 7 0/P + RTD)	10P34202-1	E
	GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (8 I/P & 7 O/P + CLIO)	10P34212-1	E
	GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (8 I/P & 11 O/P)	10P34215-1	D
	GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (8 I/P & 15 0/P)	10P34203-1	E
	GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (16 I/P & 7 0/P)	10P34204-1	E
	GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (12 I/P & 11 0/P)	10P34205-1	E
	GENERATOR PROTECTION RELAY (60TE) FOR SMALL GEN + V CHECK SYNC (16 I/P & 16 O/P)	10P34206-1	F
	GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR (24 I/P & 16 0/P)	10P34210-1	E
	GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR (16 I/P & 24 0/P)	10P34211-1	E
	GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR(16 I/P, 16 O/P + RTD & CLIO)	10P34214-1	E
	GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR (16 I/P & 20 O/P)	10P34216-3	D
	GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR (16 I/P & 12 O/P + CLIO & RTD)	10P34217-1	D
P343/6	GENERATOR PROTECTION RELAY (60TE) WITH HIGH IMPEDANCE DIFFERENTIAL (16 I/P & 14 0/P)	10P34301-2	H
	GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL USING VEE CONNECTED VTs (16 I/P & 14 0/P)	10P34301-5	G
	GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (16 I/P & 14 0/P)	10P34301-6	H
	GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL + V CHECK SYNC (16 I/P & 14 0/P)	10P34301-7	F
	GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (16 I/P & 14 0/P + RTD)	10P34302-1	L
	GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (24 I/P & 14 0/P)	10P34303-1	H
	GENERATOR PROTECTION RELAY (60TE) WITH HIGH IMPEDANCE DIFFERENTIAL (24 I/P & 14 0/P)	10P34303-3	F
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (32 I/P & 24 0/P + RTD)	10P34309-1	F
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (24 I/P & 32 0/P + RTD)	10P34310-1	F
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (32 I/P & 16 0/P + CLIO + RTD)	10P34311-1	F
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (24 I/P, 24 O/P + CLIO + RTD)	10P34313-1	E
	GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (16 I/P & 14 O/P + CLIO)	10P34314-1	E
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (16 I/P & 32 0/P + CLIO + RTD)	10P34315-1	F
	GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (16 I/P & 18 O/P 4 HIGH BREAK CONTACTS)	10P34316-1	D
	GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (16 I/P & 11 O/P 4 HIGH BREAK CONTACTS+ RTD)	10P34317-1	D
	GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL(16 I/P & 11 O/P 4 HIGH BREAK CONTACTS+ CLIO)	10P34318-1	D
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (16 I/P & 24 O/P 8 HIGH BREAK CONTACTS + CLIO & RTD)	10P34319-1	D
P344	GENERATOR PROTECTION RELAY (80 TE) WITH BIASED DIFFERENTIAL & NVD INTERTURN (24 IP & 24 OP)	10P34401-6	F
	GENERATOR PROTECTION RELAY (80 TE) WITH BIASED DIFFERENTIAL + NVD INTERTURN + V CHECK SYNC (24 I/P & 24 0/P)	10P34401-7	F
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL & NVD INTERTURN (24 I/P & 24 O/P+CLIO & RTD)	10P34406-1	D
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL & NVD INTERTURN (32 I/P & 24 O/P + RTD)	10P34407-1	D
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL & NVD INTERTURN (24 I/P & 32 O/P + RTD)	10P34408-1	D
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL & NVD INTERTURN (32 I/P & 16 O/P+CLIO & RTD)	10P34409-1	D
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL & NVD INTERTURN (16 I/P & 32 O/P+CLIO & RTD)	10P34410-1	C
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL & NVD INTERTURN (24 I/P & 20 O/P+CLIO & RTD)	10P34411-1	D
	GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL & NVD INTERTURN (16 I/P & 24 O/P+CLIO & RTD)	10P34412-1	D
P345	GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3rd HARMONIC) STATOR E/F & INTERTURN PROTECTION (24 I/P & 24 O/P = CLIO & RTD)	10P34501-1	E
	GENERATOR PROTECTION RELAY (80TE) WITH 100% STATOR E/F PROTECTION. VIA NEUTRAL EARTHING TRANSFROMER WITH SECONDARY LOADING RESISTOR (24 I/P & 24 O/P + CLIO & RTD)	10P34501-3	E
	GENERATOR PROTECTION RELAY (80TE) WITH 100% STATOR E/F PROTECTION. VIA NEUTRAL EARTHING TRANSFORMER. WITH PRIMARY LOADING RESISTOR (24 I/P & 24 O/P + CLIO & RTD)	10P34501-4	E
	GENERATOR PROTECTION RELAY (80TE) 100% STATOR EARTH FAULT (24 I/P & 24 O/P + CLIO & RTD)	10P34501-5	D.1
	GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3rd HARMONIC) STATOR E/ F & INTERTURN PROTECTION.(24 I/P & 24 O/P + CLIO & RTD)	10P34501-10	H
	GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3RD HARMONIC) STATOR E/F, INTERTURN PROTECTION & V CHK SYNC 24I/P & 24O/P + CLIO & RTD	10P34501-11	F
	GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3rd HARMONIC) STATOR E/ F PROTECTION & WATTMETRIC POWER (24 I/P & 24 O/P + CLIO & RTD)	10P34501-13	C
	GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3rd HARMONIC) STATOR EARTH FAULT & INTERTURN PROTECTION (24 I/P & 32 O/P + RTD)	10P34502-1	G
	GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3rd HARMONIC) STATOR E/F, INTERTURN PROTECTION & V CHECK SYNC (32 I/P & 24 O/P + RTD)	10P34503-1	F
	GENERATOR PROTECTION RELAY (80TE) WITH V CHECK SYNC 90% & 100% (3rd HARMONIC) STATOR E/F & INTERTURN PROTECTION (32 I/P & 16 O/P + CLIO & RTD)	10P34504-1	G
	GENERATOR PROTECTION RELAY (80TE) WITH V CHECK SYNC 90% & 100% (3rd HARMONIC) STATOR E/F & INTERTURN PROTECTION (16 I/P & 32 O/P + CLIO & RTD)	10P34505-1	G
	GENERATOR PROTECTION RELAY (80TE) WITH V CHECK SYNC 90% & 100% (3rd HARMONIC) STATOR E/F & INTERTURN PROTECTION (24 I/P & 20 O/P + CLIO & RTD)	10P34506-1	G
	GENERATOR PROTECTION RELAY (80TE) WITH V CHECK SYNC 90% & 100%G (3rd HARMONIC) STATOR E/F & INTERTURN PROTECTION (16 I/P & 24 O/P + CLIO & RTD)	10P34507-1	G
P348	VARIABLE SPEED MACHINE PROTECTION RELAY (80TE) (16 I/P & 20 O/P 4 HIGH BREAK CONTACTS & CLIO)	10P34801-1	D
	VARIABLE SPEED MACHINE PROTECTION RELAY (80TE) (32 I/P & 32 O/P & CLIO)	10P34802-1	B
P391	GENERATOR PROTECTION RELAY ROTOR EARTH FAULT PROTECTION DOUBLE ENDED CONNECTION	10P39101-1	D
	GENERATOR PROTECTION RELAY ROTOR EARTH FAULT PROTECTION SINGLE ENDED CONNECTION	10P39102-1	D



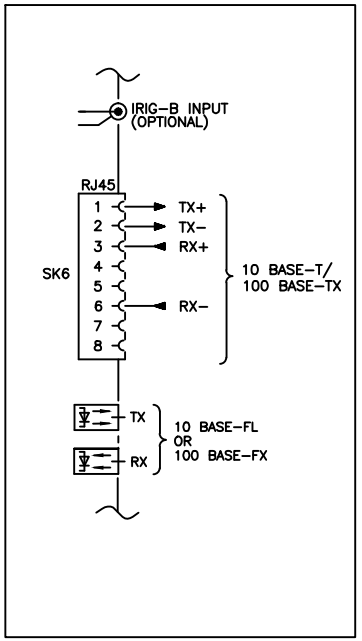
NOTE: FOR TERMINAL BLOCK CONNECTION
REFER TO RELEVANT EXTERNAL CONNECTION DIAGRAM.
(ALWAYS ON PSU BLOCK)





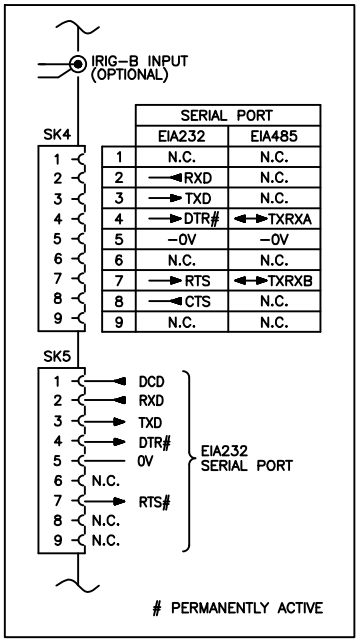
IRIG–B BOARD

OR



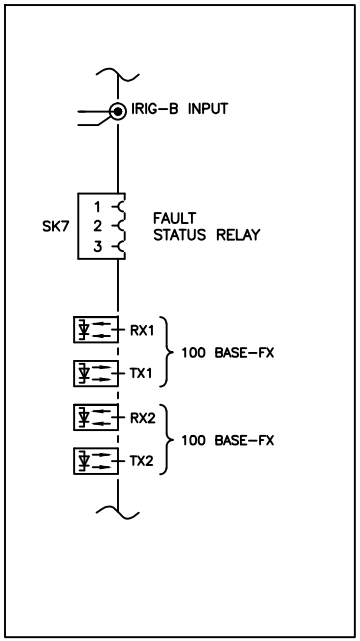
SINGLE PORT ETHERNET BOARD

OR



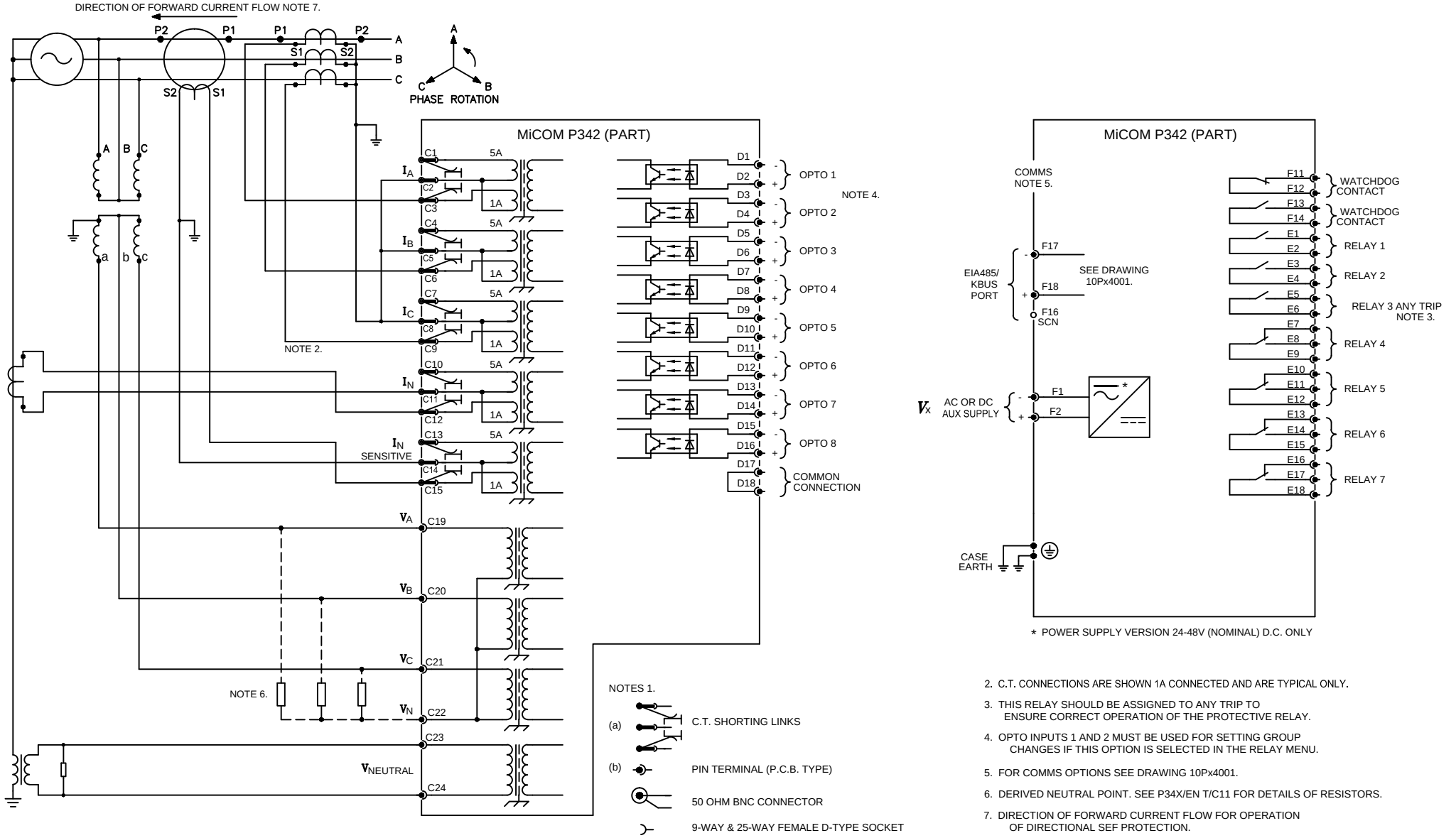
REAR COMMS BOARD

OR

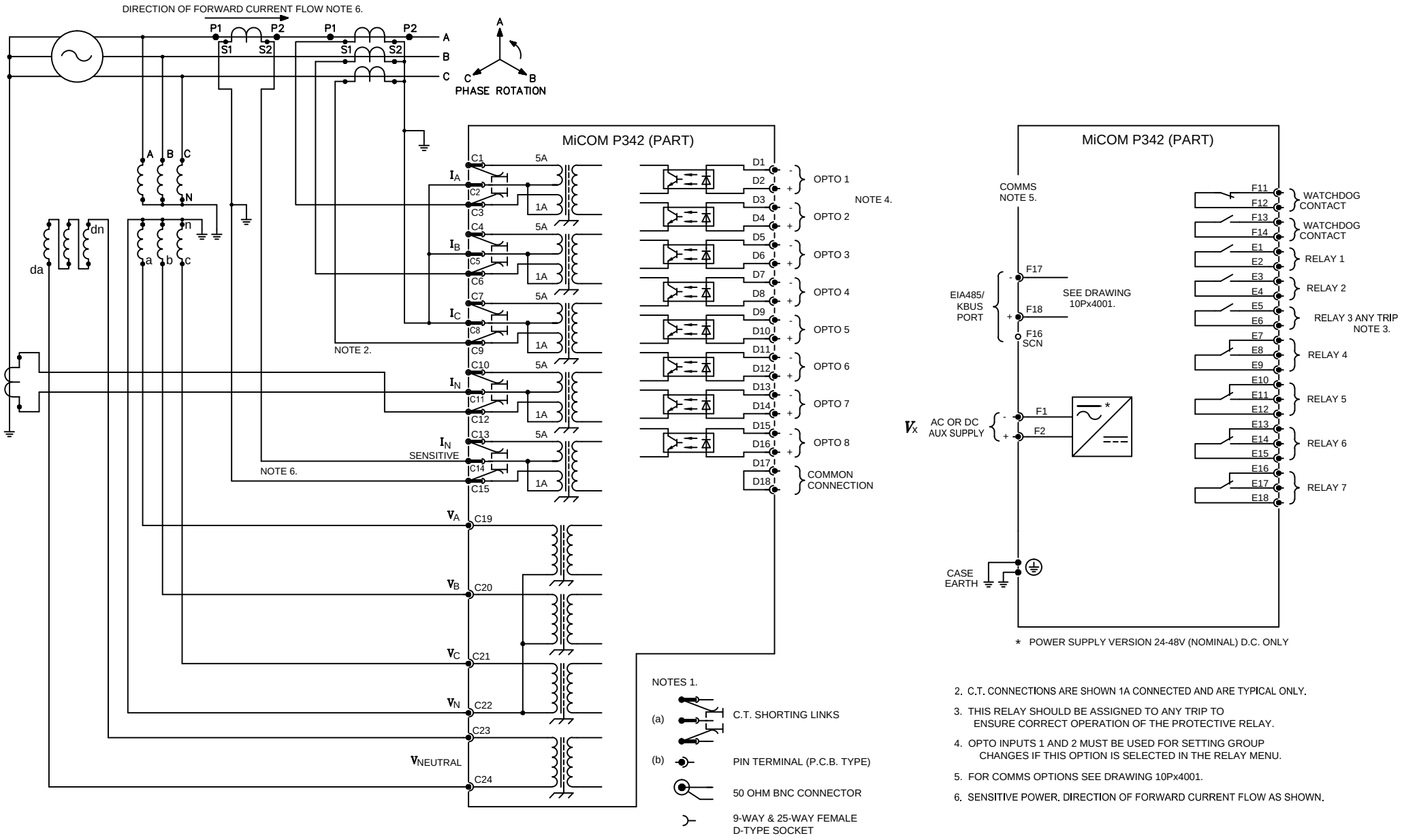


DUAL PORT REDUNDANT ETHERNET BOARD

Issue: J	Revision: DRAWING OUTLINE UPDATED. CID BLIN-8BHLDT			Title: EXTERNAL CONNECTION DIAGRAM: COMMS OPTIONS MICOM Px40 PLATFORM	
Date: 30/11/2010	Name: W.LINTERN	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10Px4001	Sht: 1
Date:	Chkd: S KELSALL				Next Sht: -



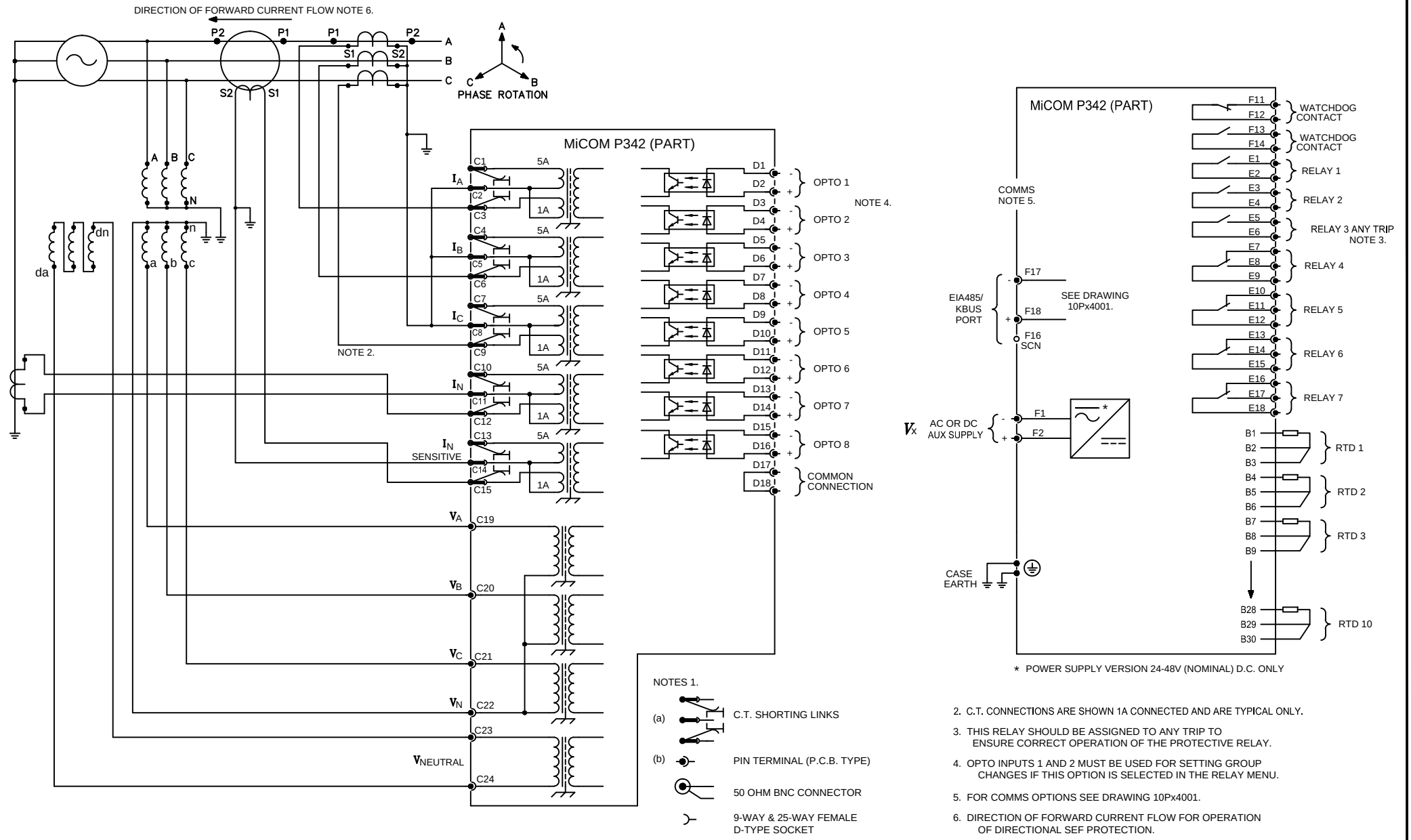
Issue: G	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A			Title: EXT.CONNECTION DIAG:GENERATOR PROTECTION RELAY(40TE) FOR GENERATOR. USING VEE CONNECTED VT's (8 I/P & 7 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34201	Sht: 3
Date:	Chkd: T.Y.				Next Sht: 4



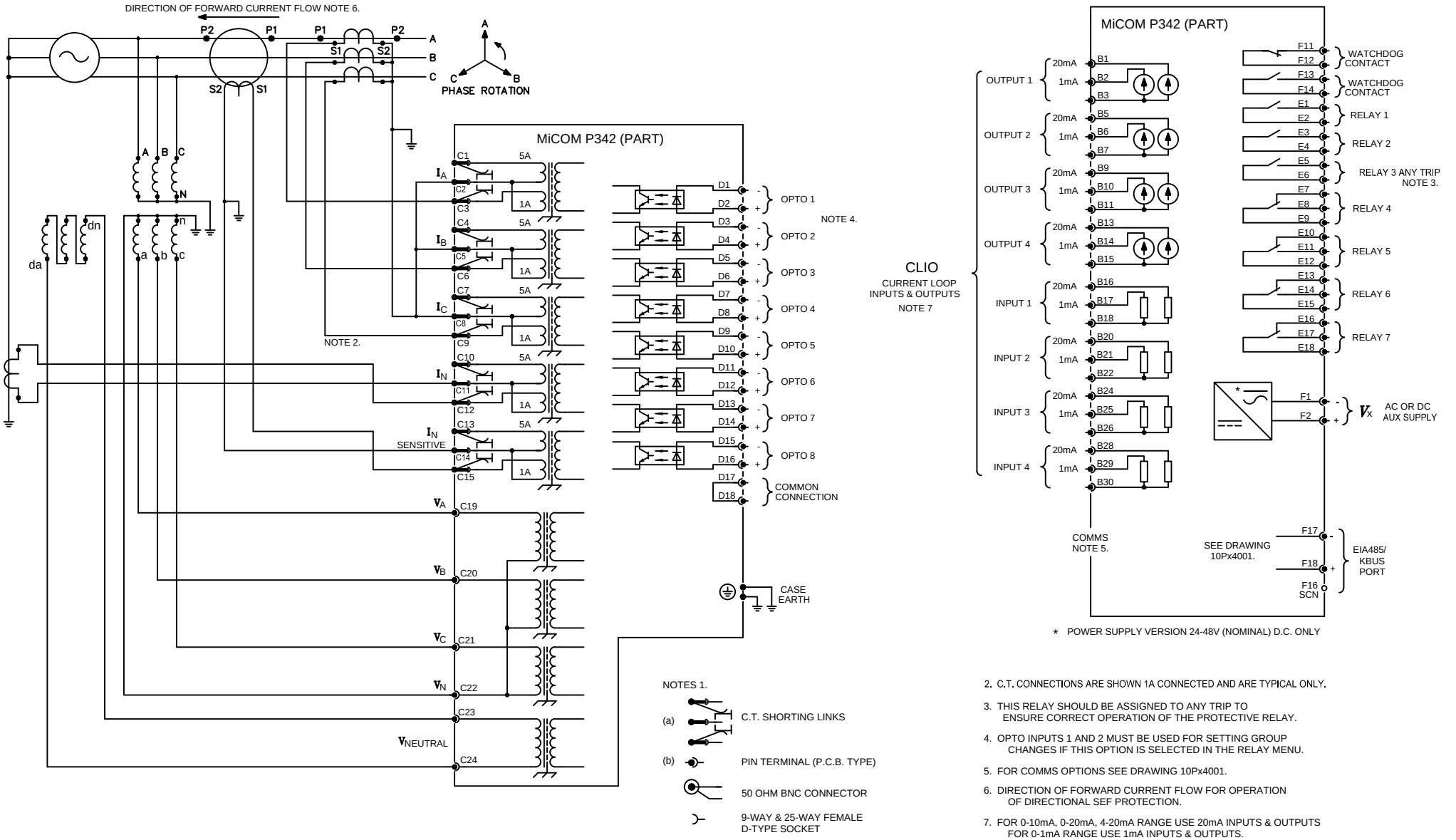
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. SENSITIVE POWER. DIRECTION OF FORWARD CURRENT FLOW AS SHOWN.

Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A			Title: EXT.CONNECTION DIAG:GENERATOR PROTECTION RELAY(40TE) FOR SMALL GENERATOR WITH SENSITIVE POWER (8 I/P & 7 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34201	Sht: 4
Date:	Chkd: T.Y.				Next Sht: -



Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (8 I/P & 7 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34202	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2



NOTES 1.

(a) C.T. SHORTING LINKS

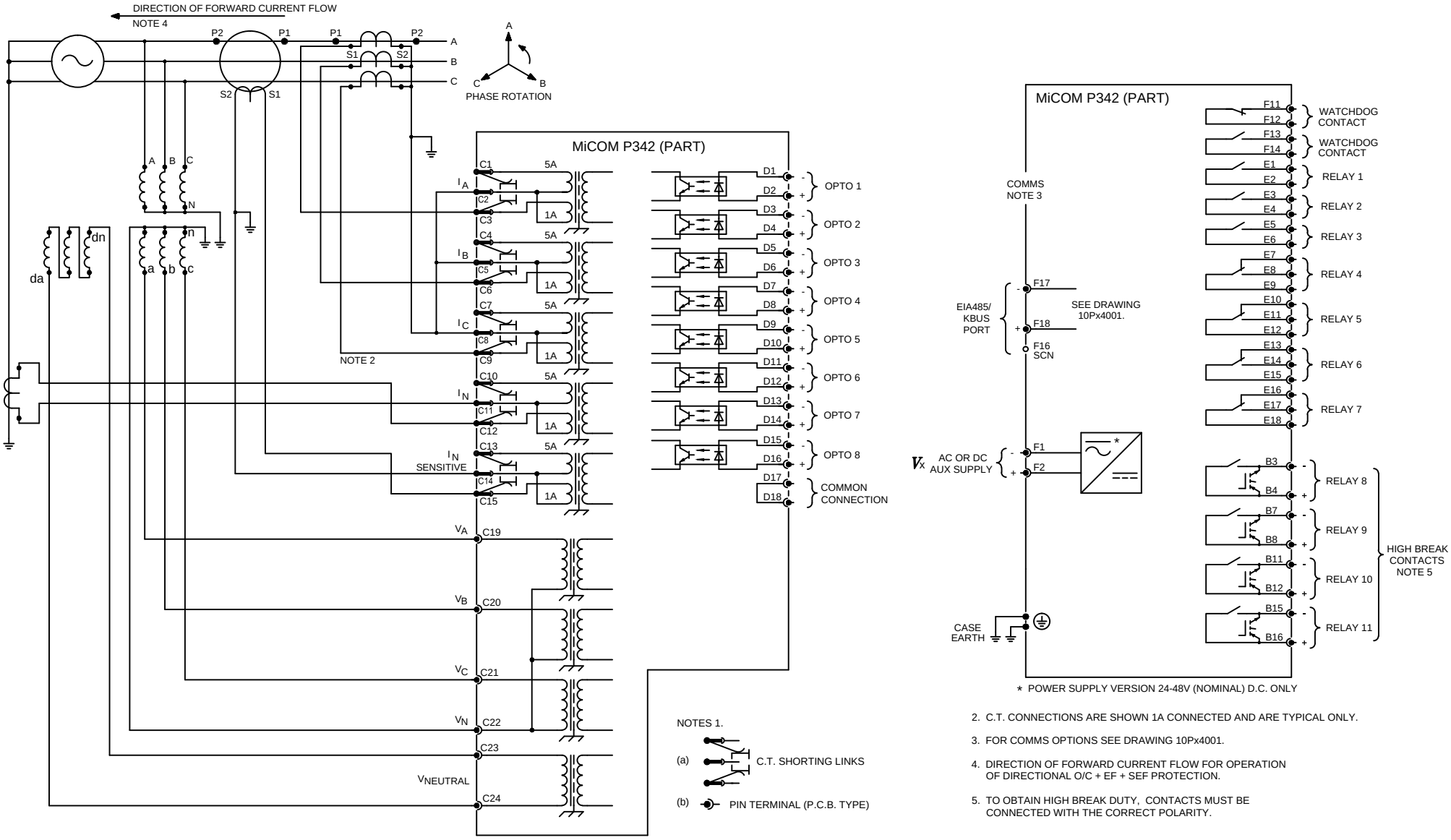
(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
7. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

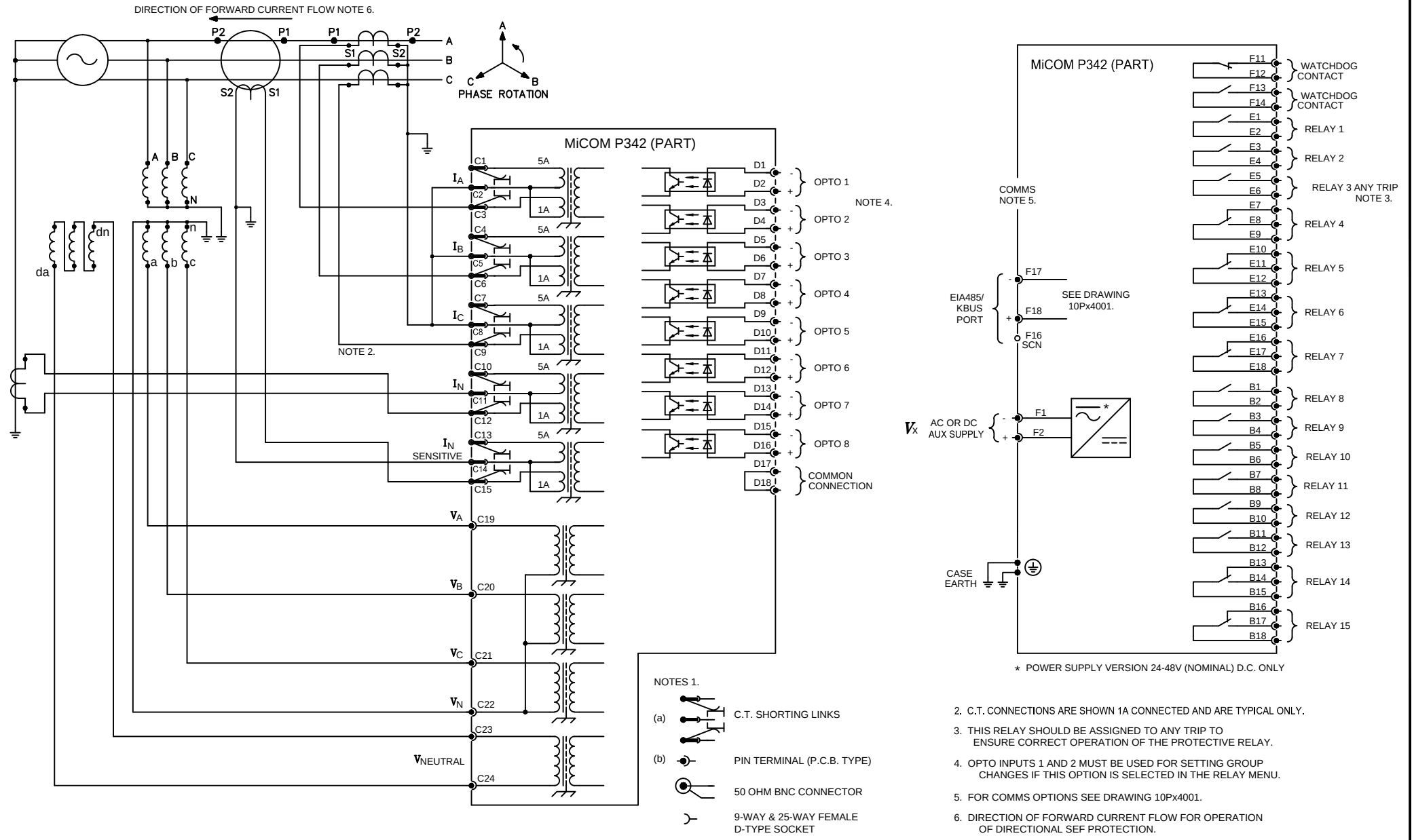
Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT CONN DIAGRAM: GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (8 I/P & 7 O/P + CLIO)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34212	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2



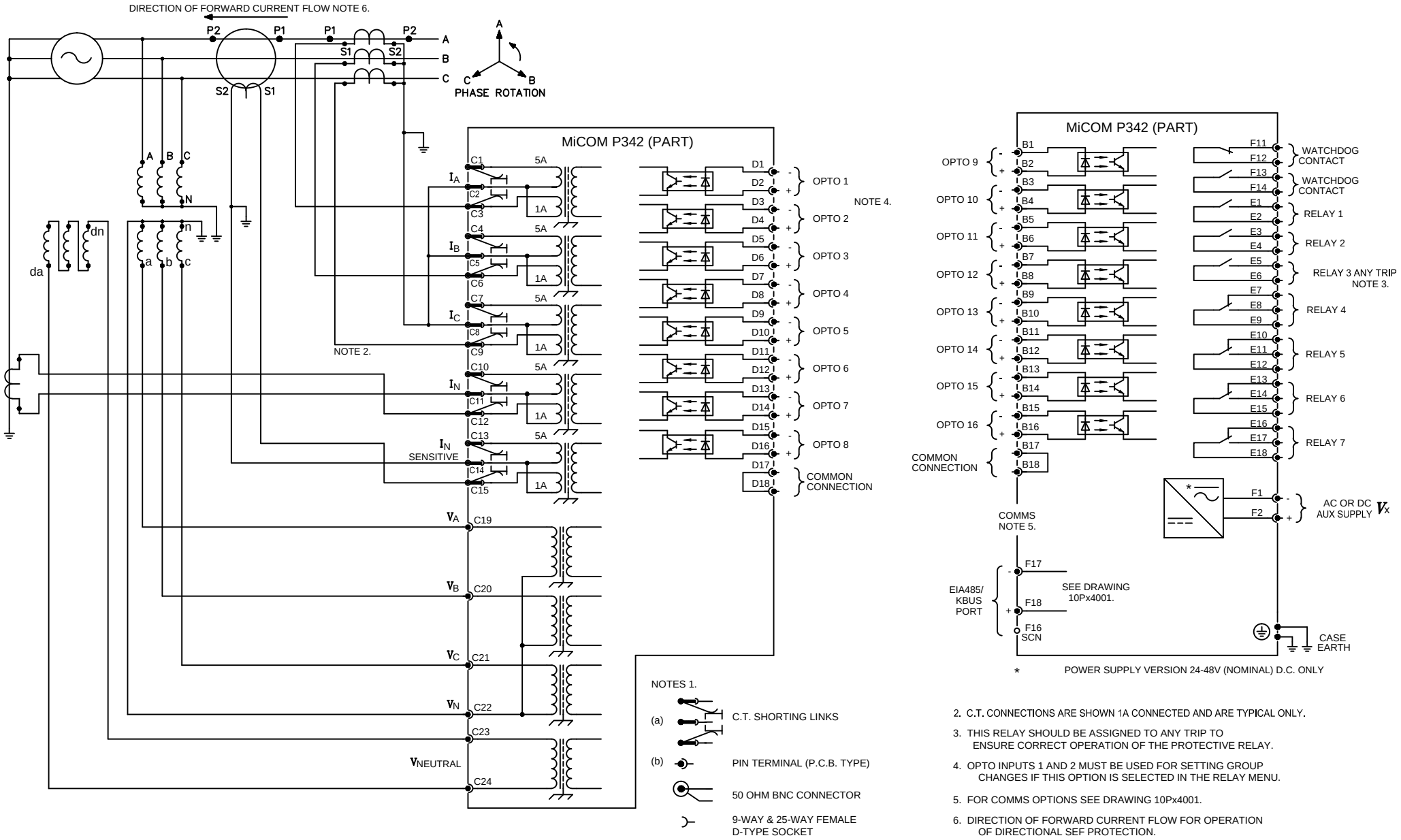
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL O/C + EF + SEF PROTECTION.
5. TO OBTAIN HIGH BREAK DUTY, CONTACTS MUST BE CONNECTED WITH THE CORRECT POLARITY.

Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (8 I/P & 11 O/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34215	Sht: 1
Date:	Chkd:				Next Sht: 2

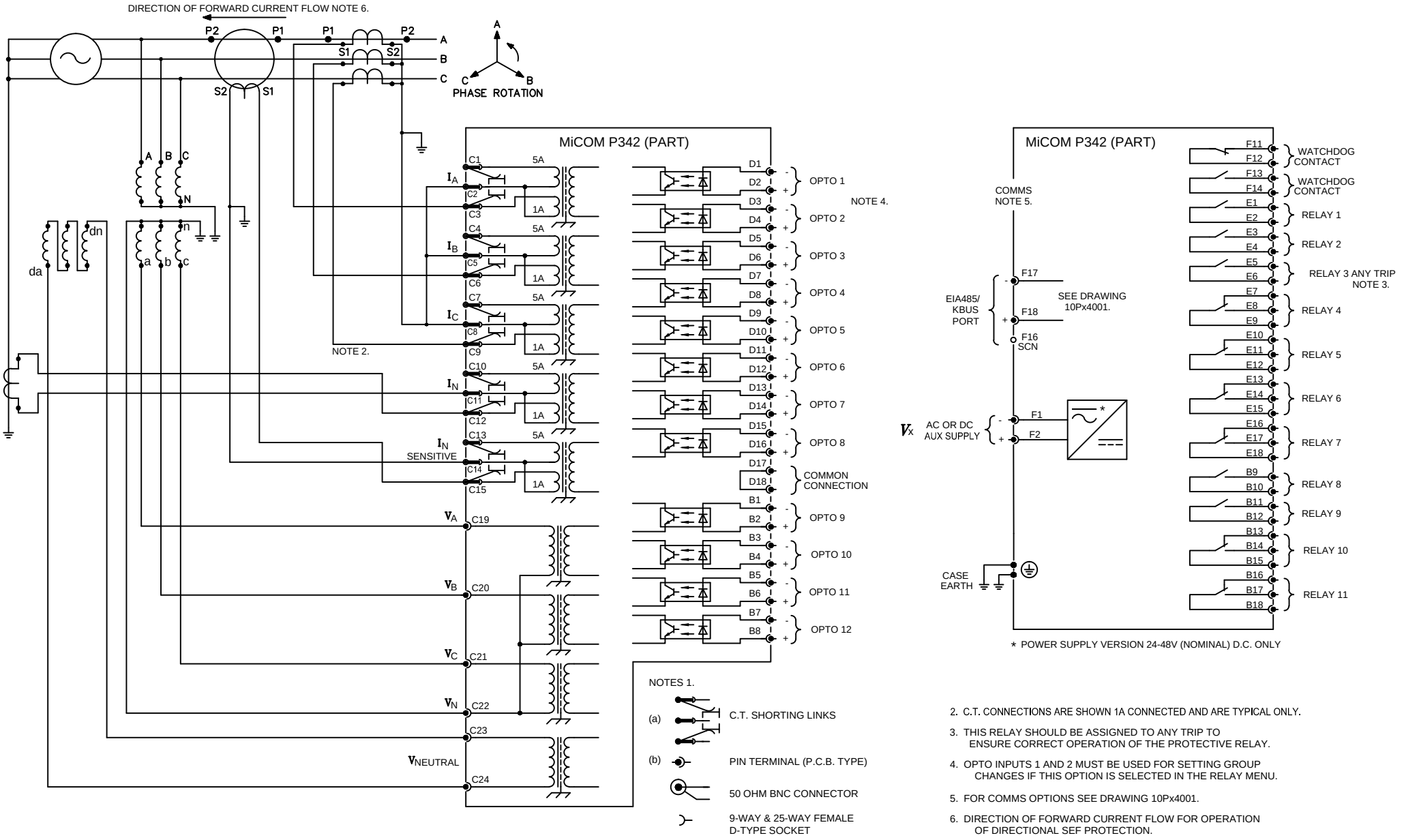


Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (8 I/P & 15 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34203	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2



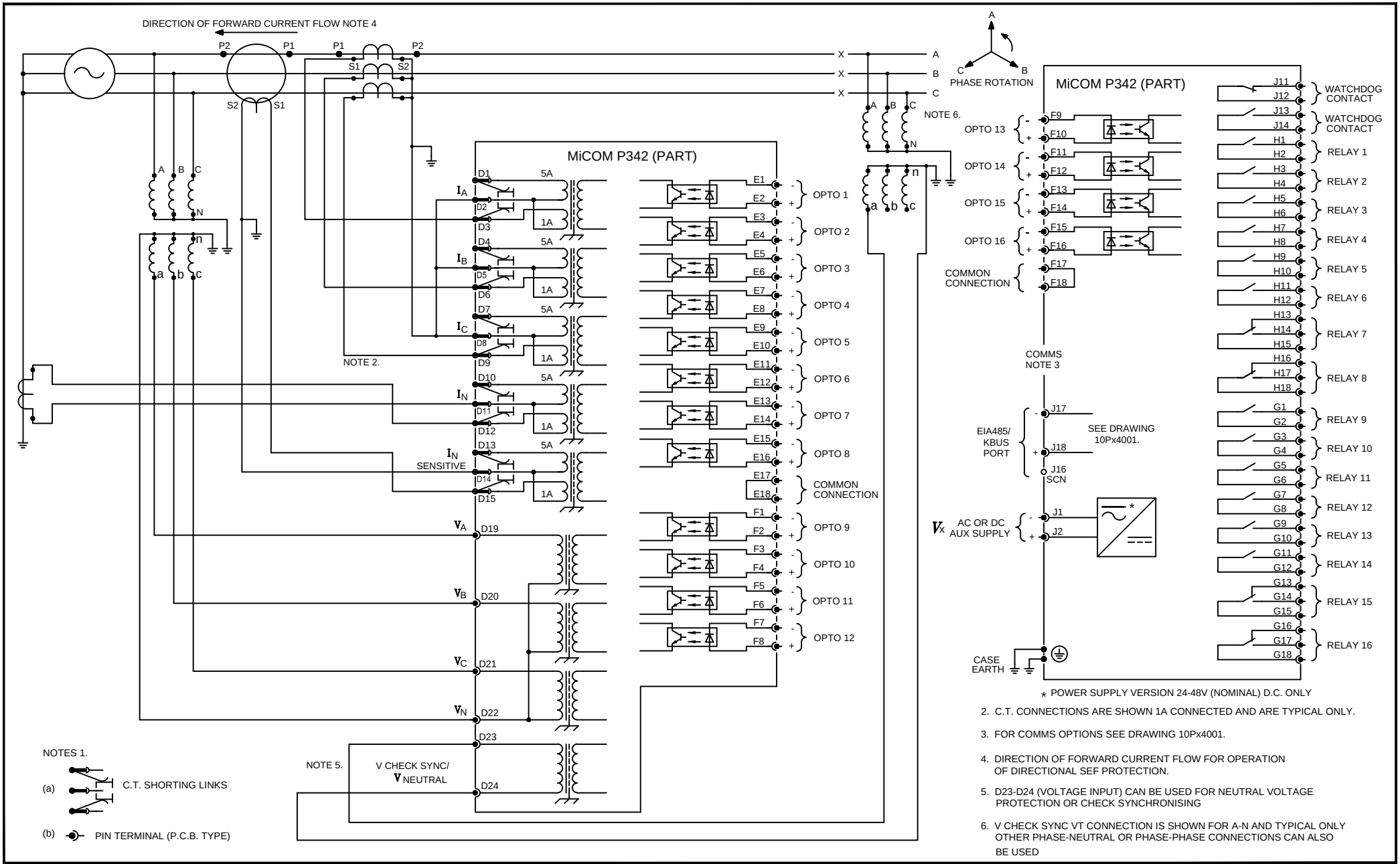
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.

Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (16 I/P & 7 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34204	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2



2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.

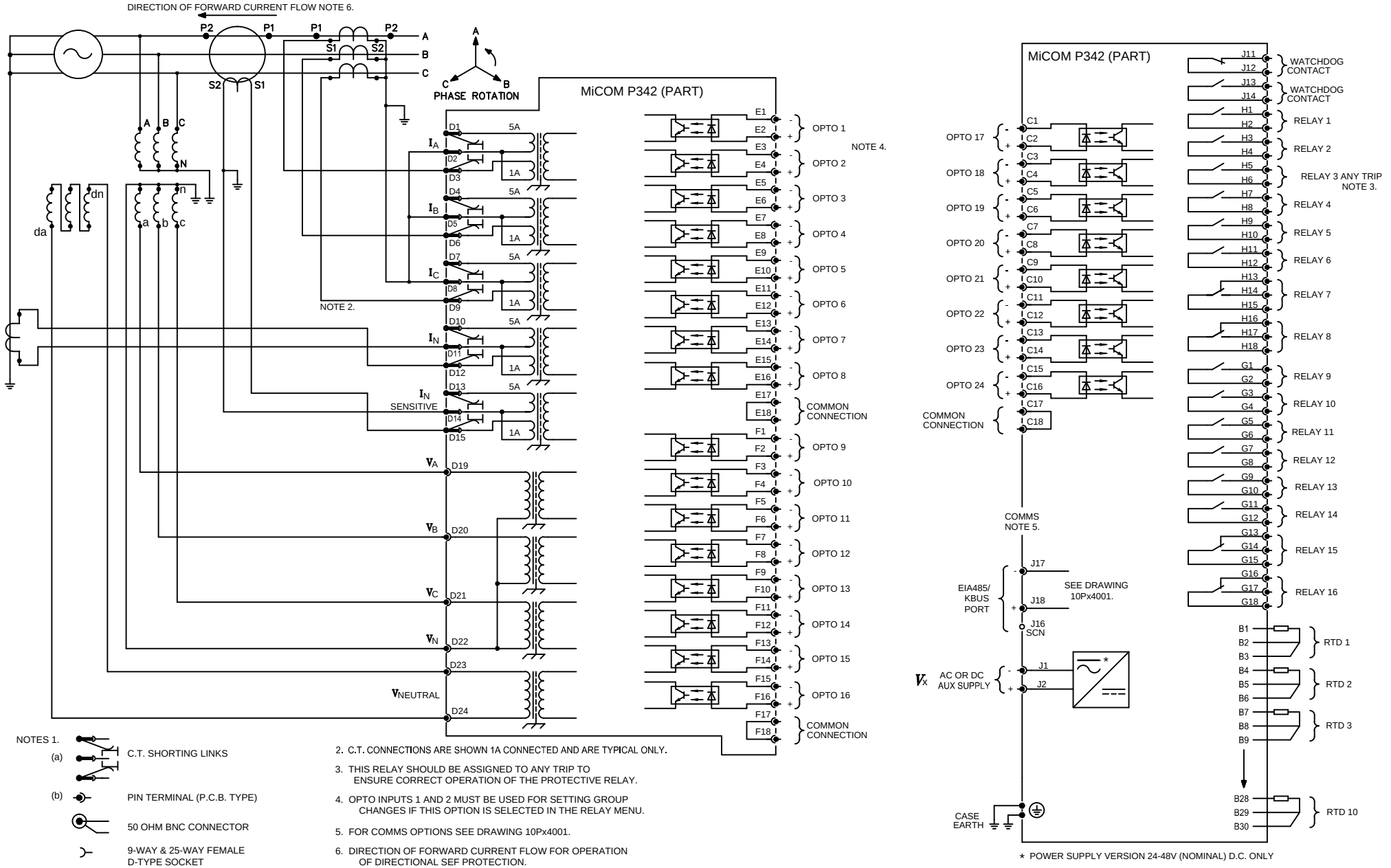
Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (40TE) FOR SMALL GENERATOR (12 I/P & 11 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34205	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2



* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
5. D23-D24 (VOLTAGE INPUT) CAN BE USED FOR NEUTRAL VOLTAGE PROTECTION OR CHECK SYNCHRONISING
6. V CHECK SYNC VT CONNECTION IS SHOWN FOR A-N AND TYPICAL ONLY OTHER PHASE-NEUTRAL OR PHASE-PHASE CONNECTIONS CAN ALSO BE USED

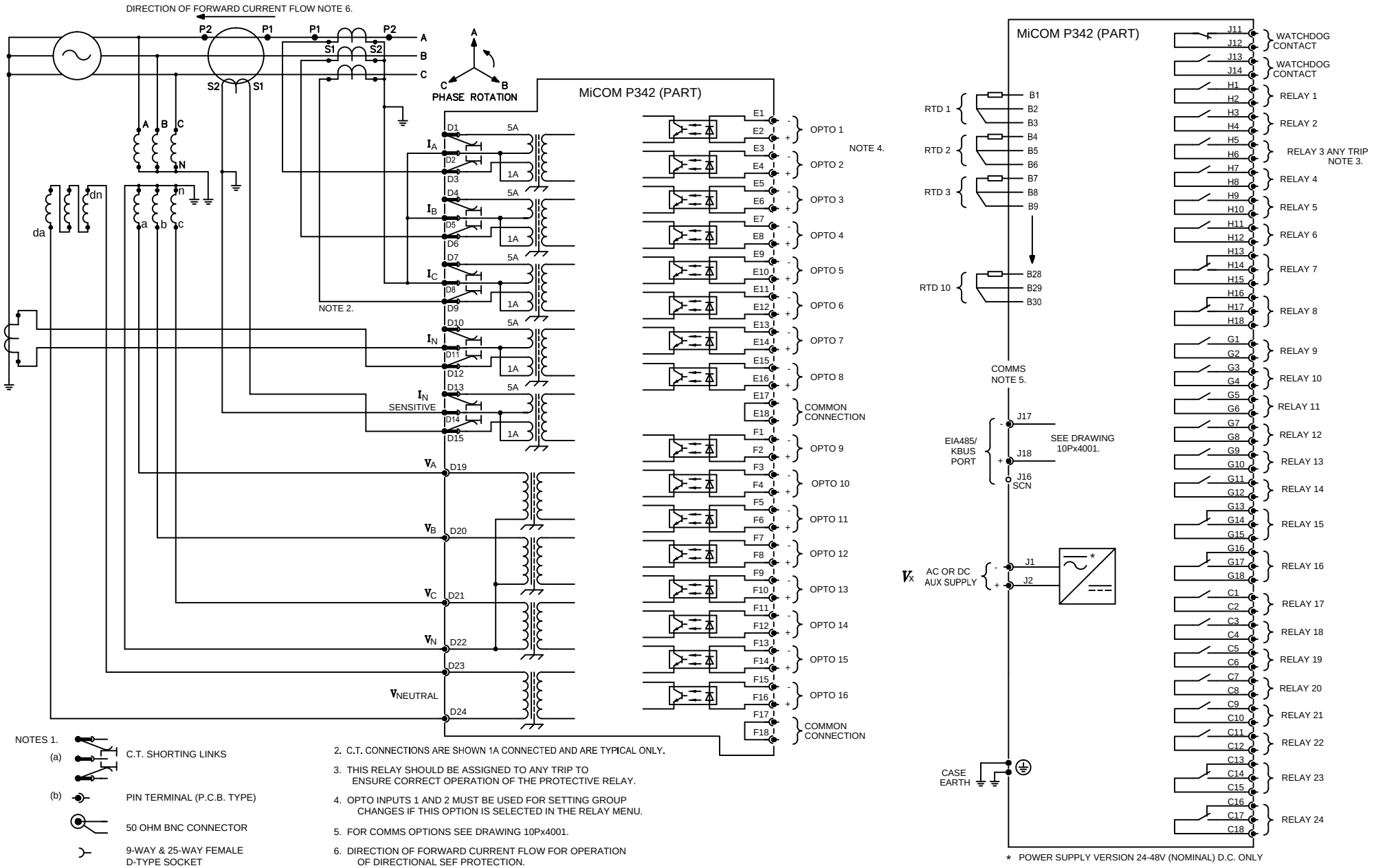
Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A			Title: EXTERNAL CONNECTION DIAGRAM:GENERATOR PROTECTION RELAY (60TE) FOR SMALL GEN + V CHECK SYNC (16 I/P & 16 O/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34206	Sht: 3
Date:	Chkd: G.L.				Next Sht: -



NOTES 1.
(a) C.T. SHORTING LINKS
(b) PIN TERMINAL (P.C.B. TYPE)
50 OHM BNC CONNECTOR
9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.

Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR (24 I/P & 16 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34210	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2



NOTES 1.

(a) C.T. SHORTING LINKS

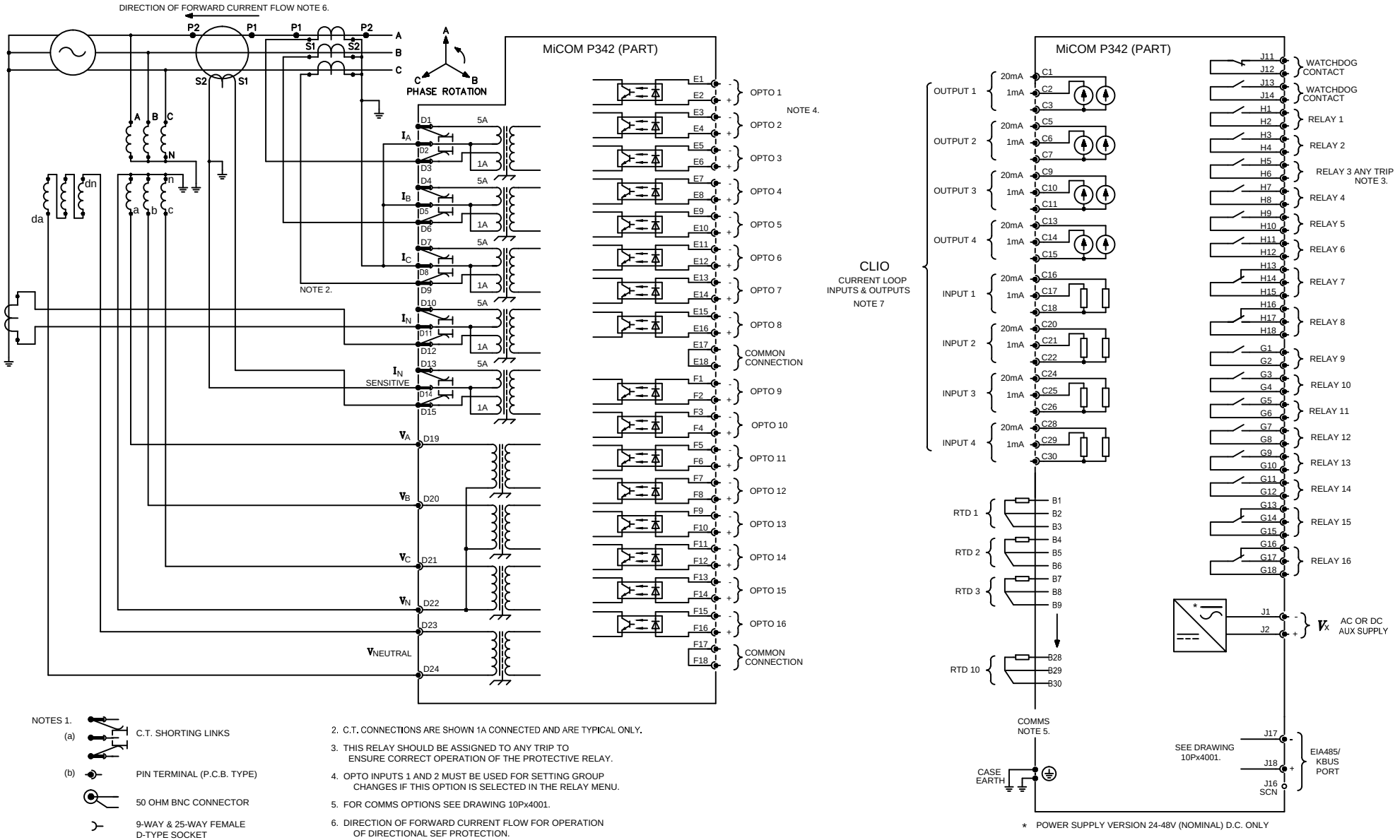
(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.

Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR (16 I/P & 24 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34211	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

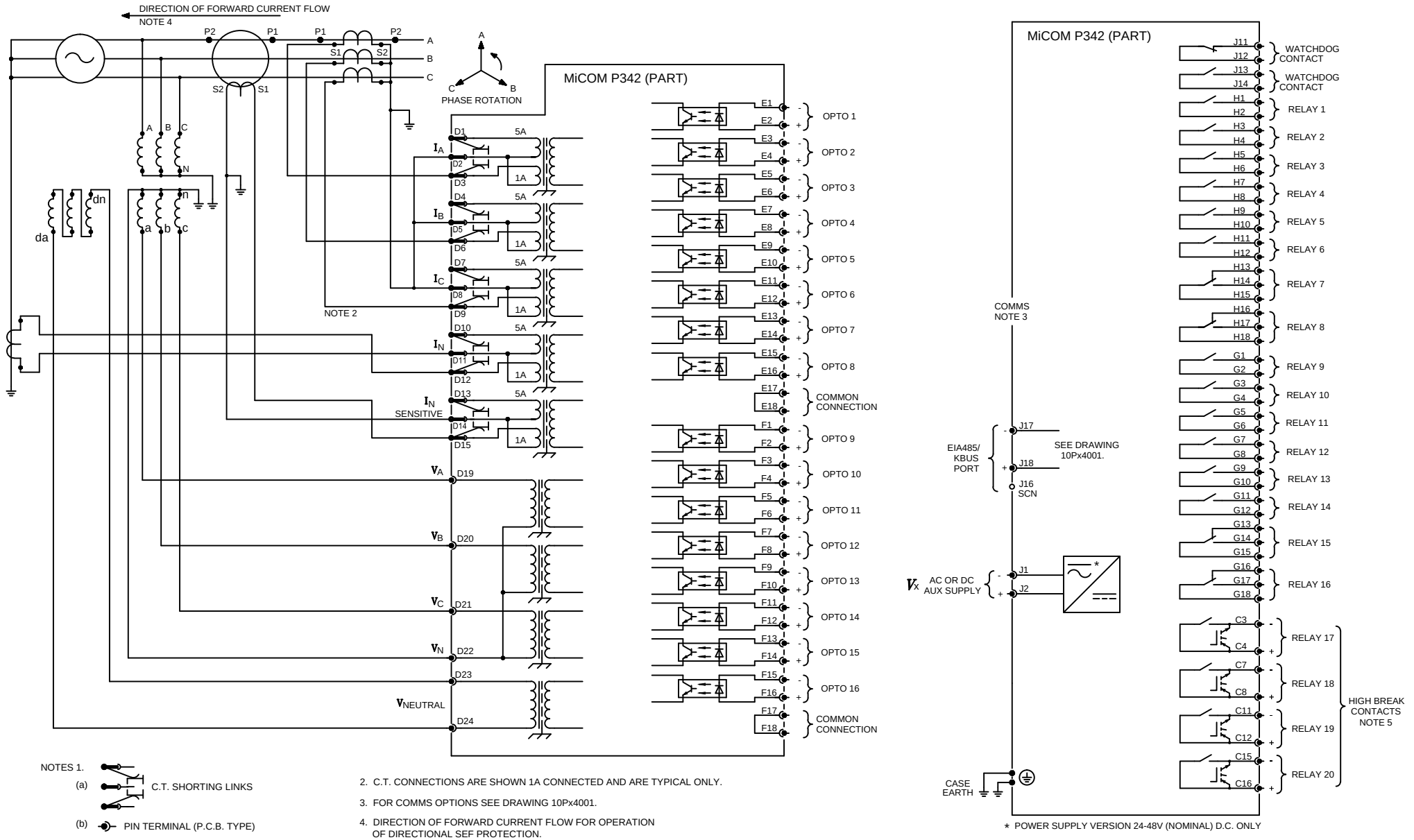
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
7. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT CONN DIAG: GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR(16 I/P, 16 O/P + RTD & CLIO)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34214	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2

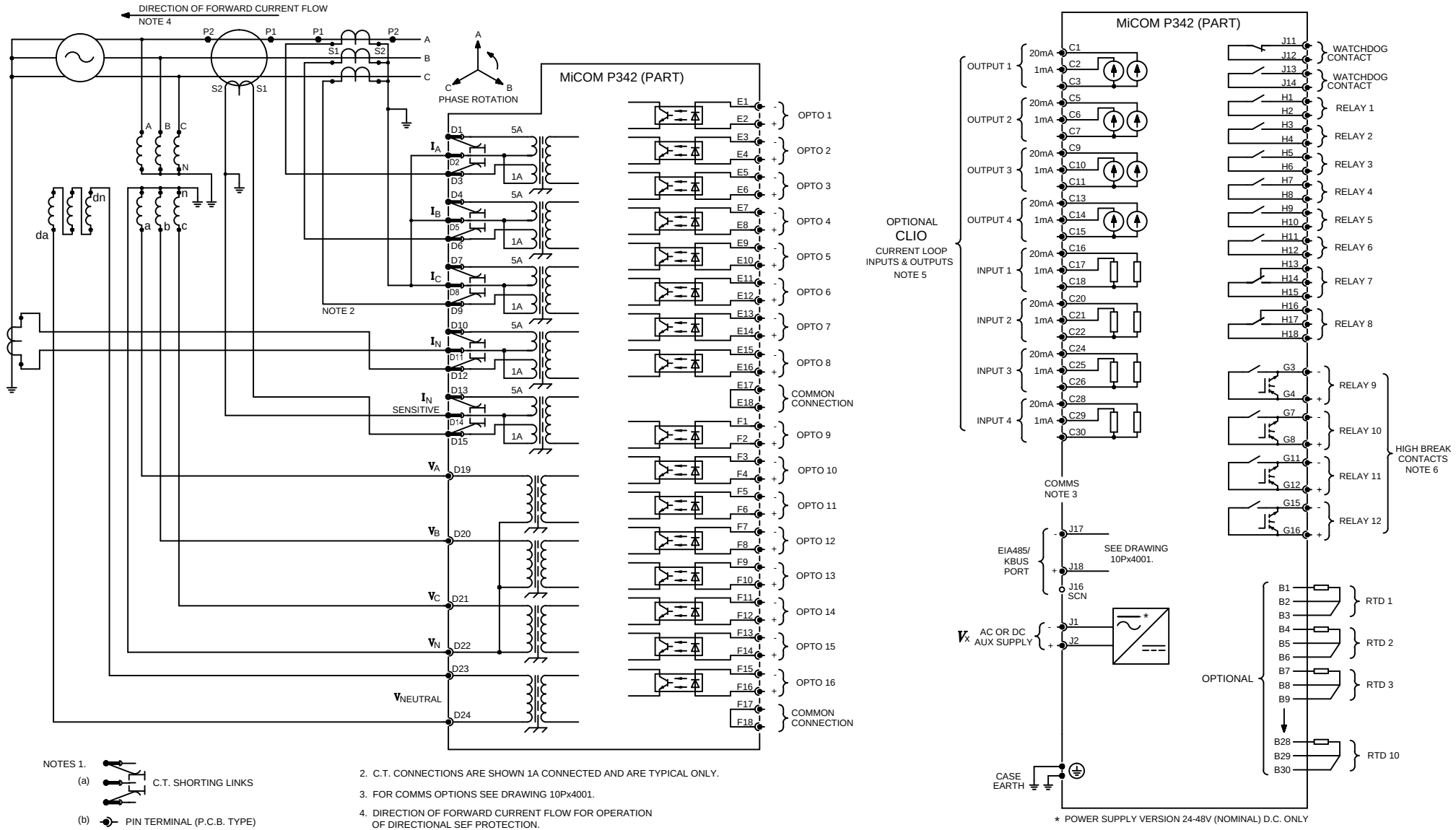


NOTES 1.
(a) C.T. SHORTING LINKS
(b) PIN TERMINAL (P.C.B. TYPE)

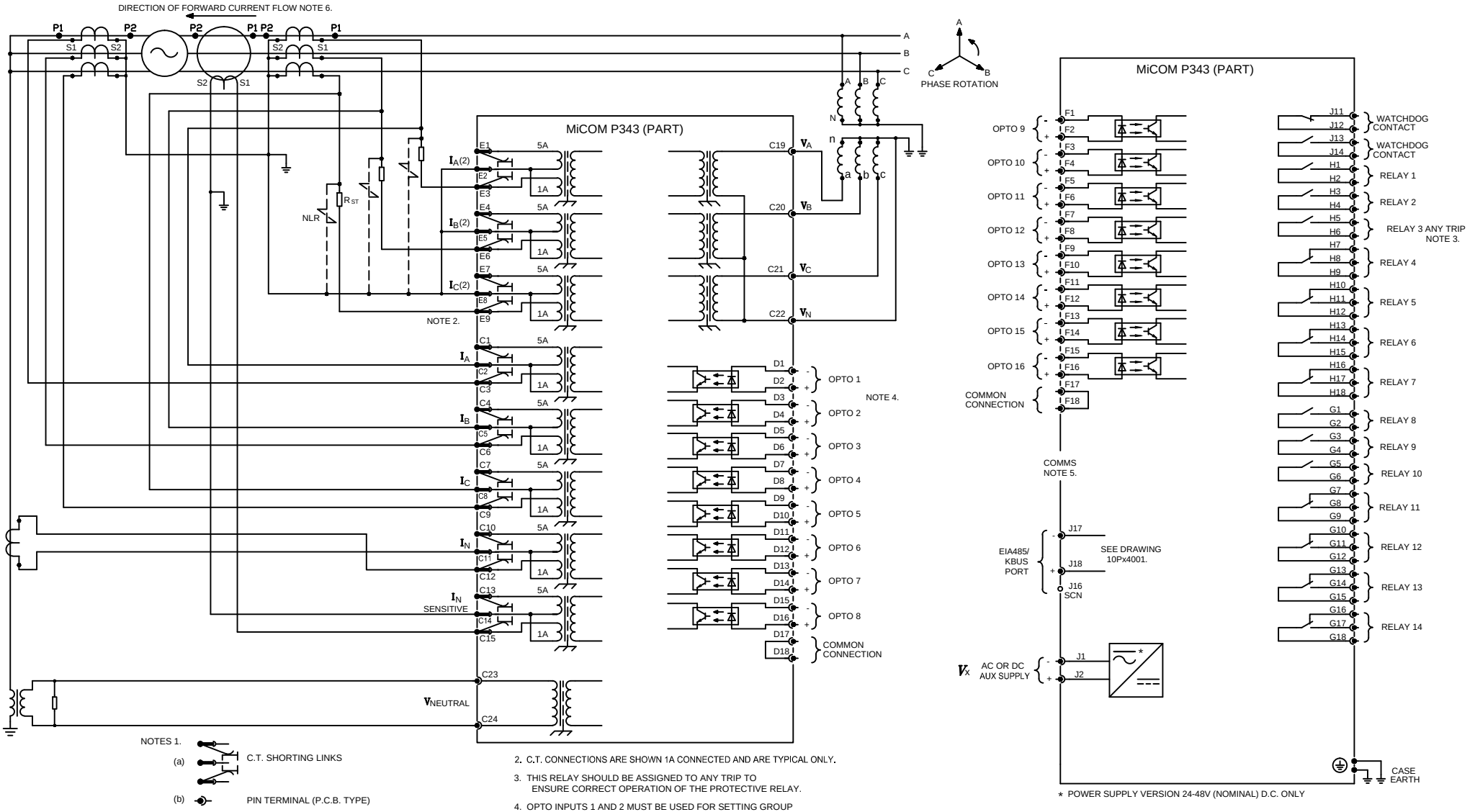
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
5. TO OBTAIN HIGH BREAK DUTY, CONTACTS MUST BE CONNECTED WITH THE CORRECT POLARITY.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR (16 I/P & 20 O/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34216	Sht: 1
Date:	Chkd:				Next Sht: 2



Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXTERNAL CONNECTION DIAG:GENERATOR PROTECTION RELAY (60TE) FOR SMALL GENERATOR (16 I/P & 12 O/P + CLIO & RTD)
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34217
Date:	Chkd:			Sht: 1	Next Sht: 2



NOTES 1.

(a) C.T. SHORTING LINKS

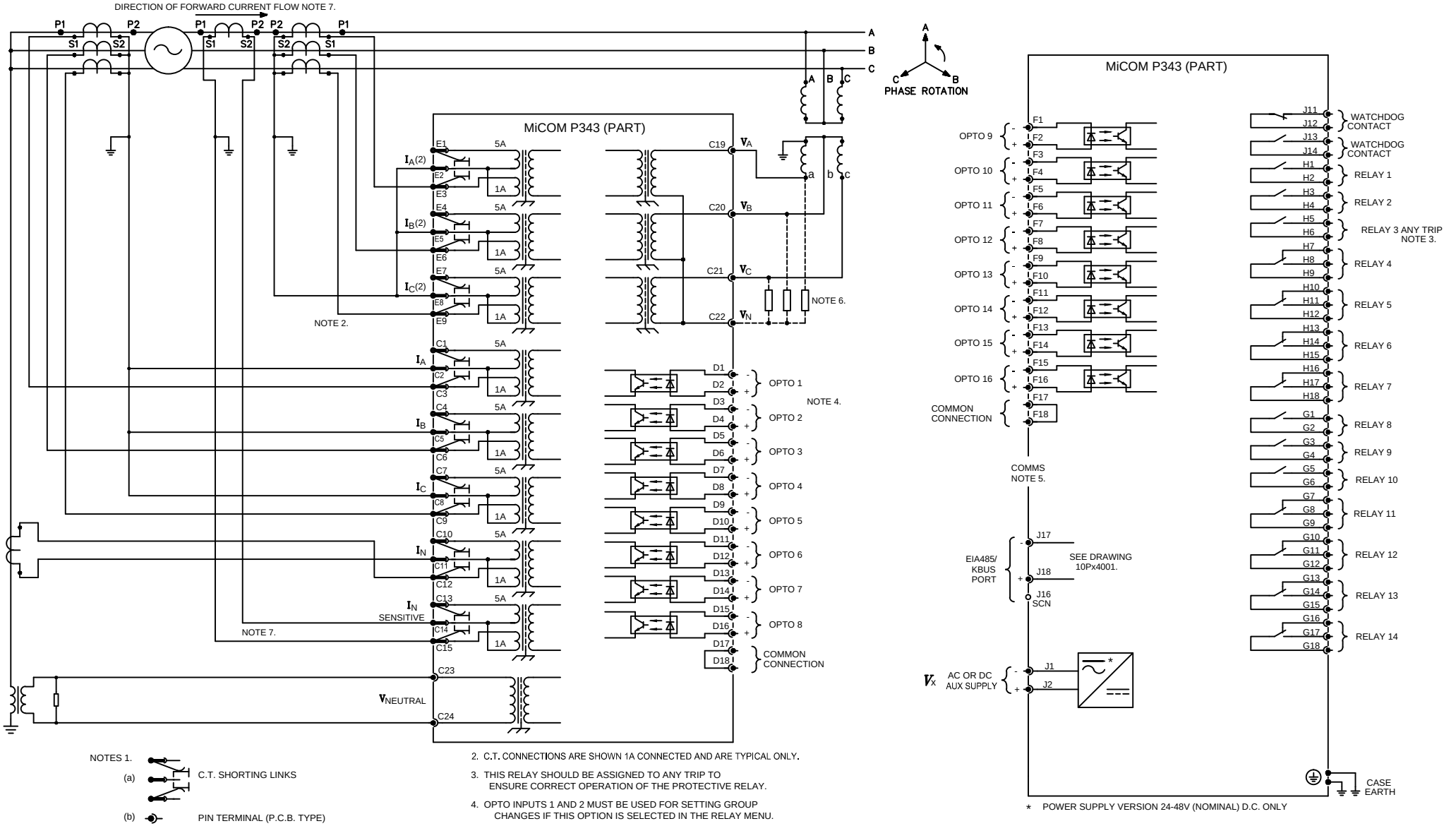
(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.

Issue: H	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) WITH HIGH IMPEDANCE DIFFERENTIAL (16 I/P & 14 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34301	Sht: 2
Date:	Chkd: T.Y.				Next Sht: 3



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

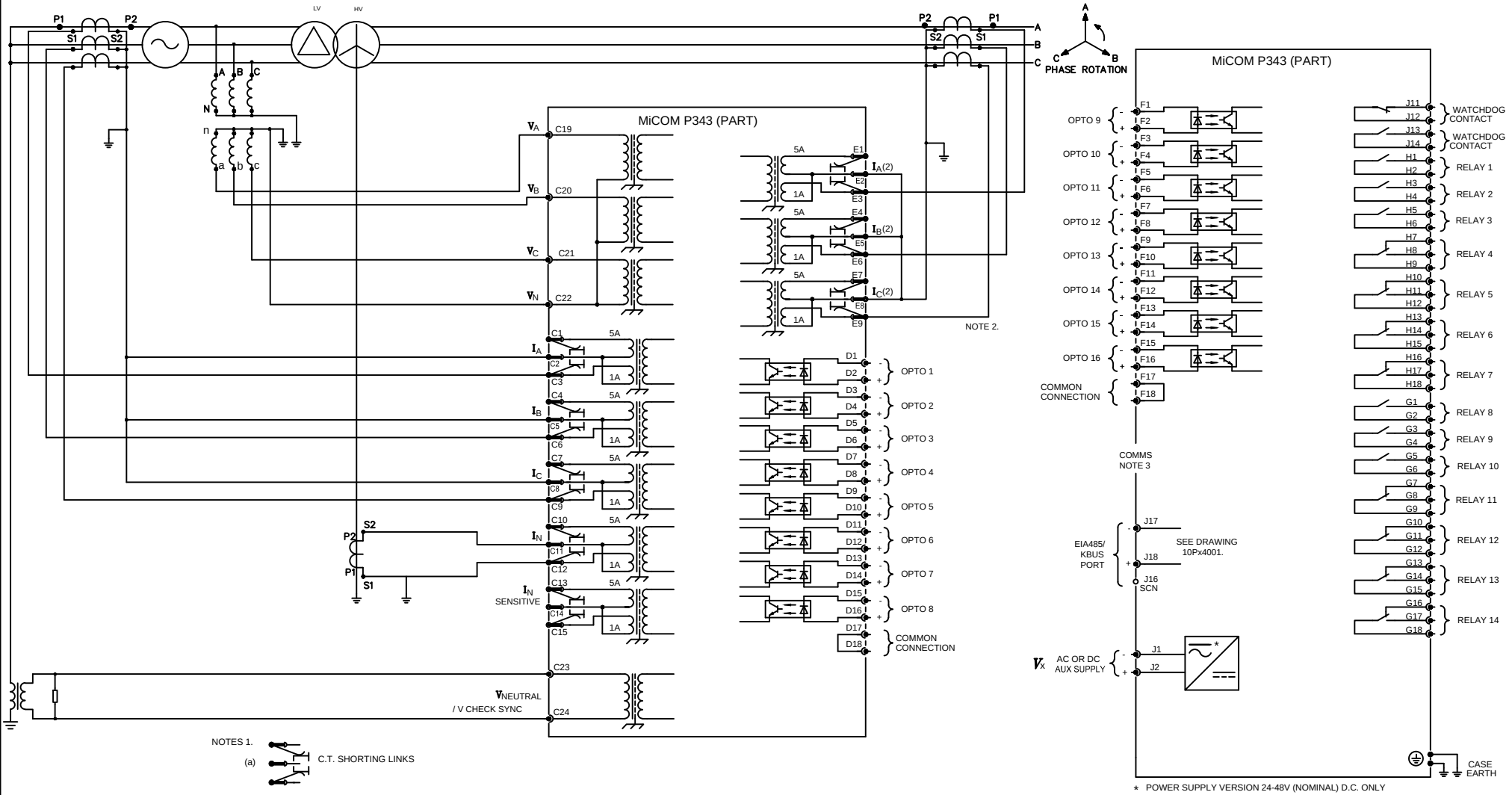
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

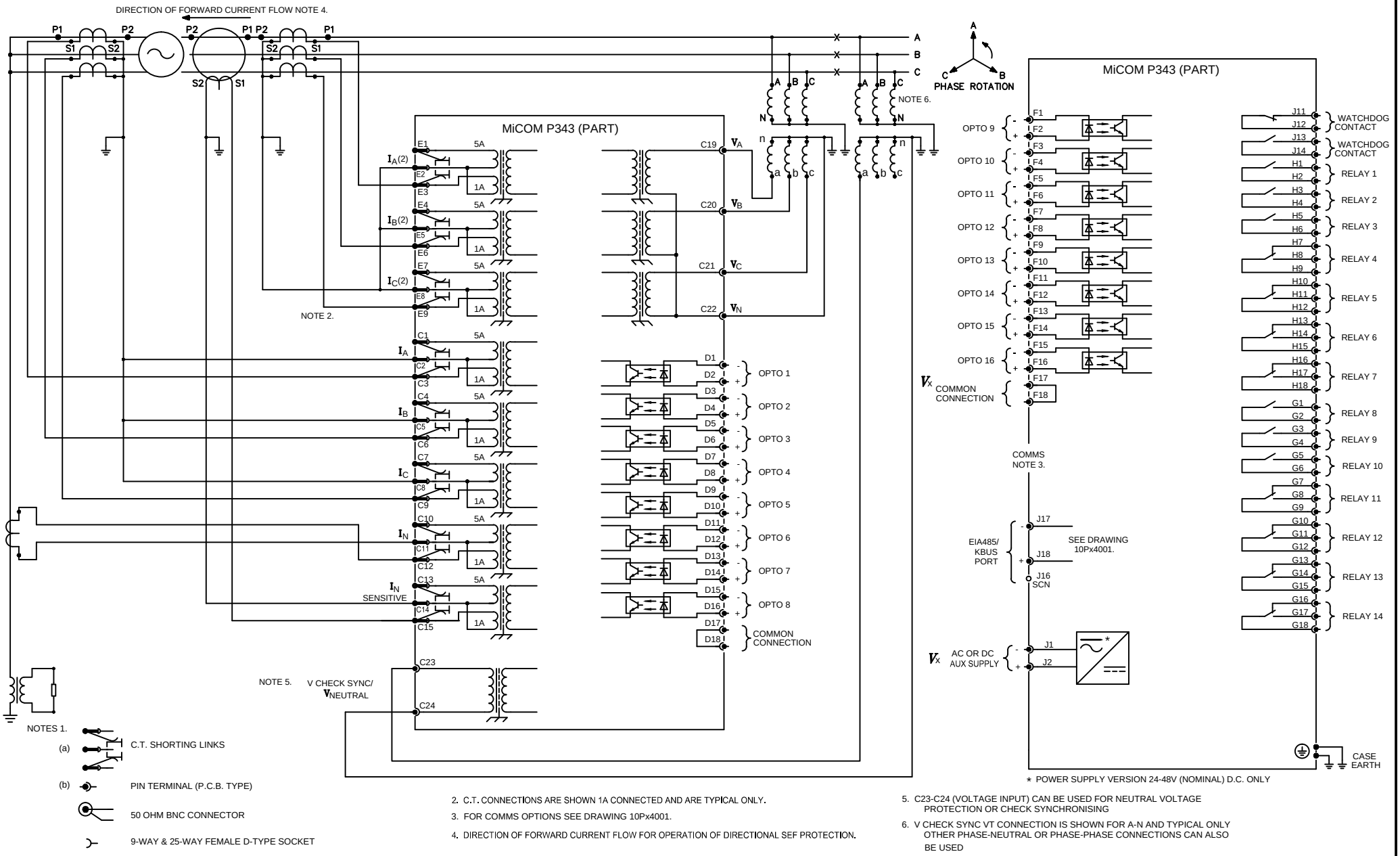
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DERIVED NEUTRAL POINT. SEE P34X/EN T/C11 FOR DETAILS OF RESISTORS.
7. SENSITIVE POWER. DIRECTION OF FORWARD CURRENT FLOW AS SHOWN.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

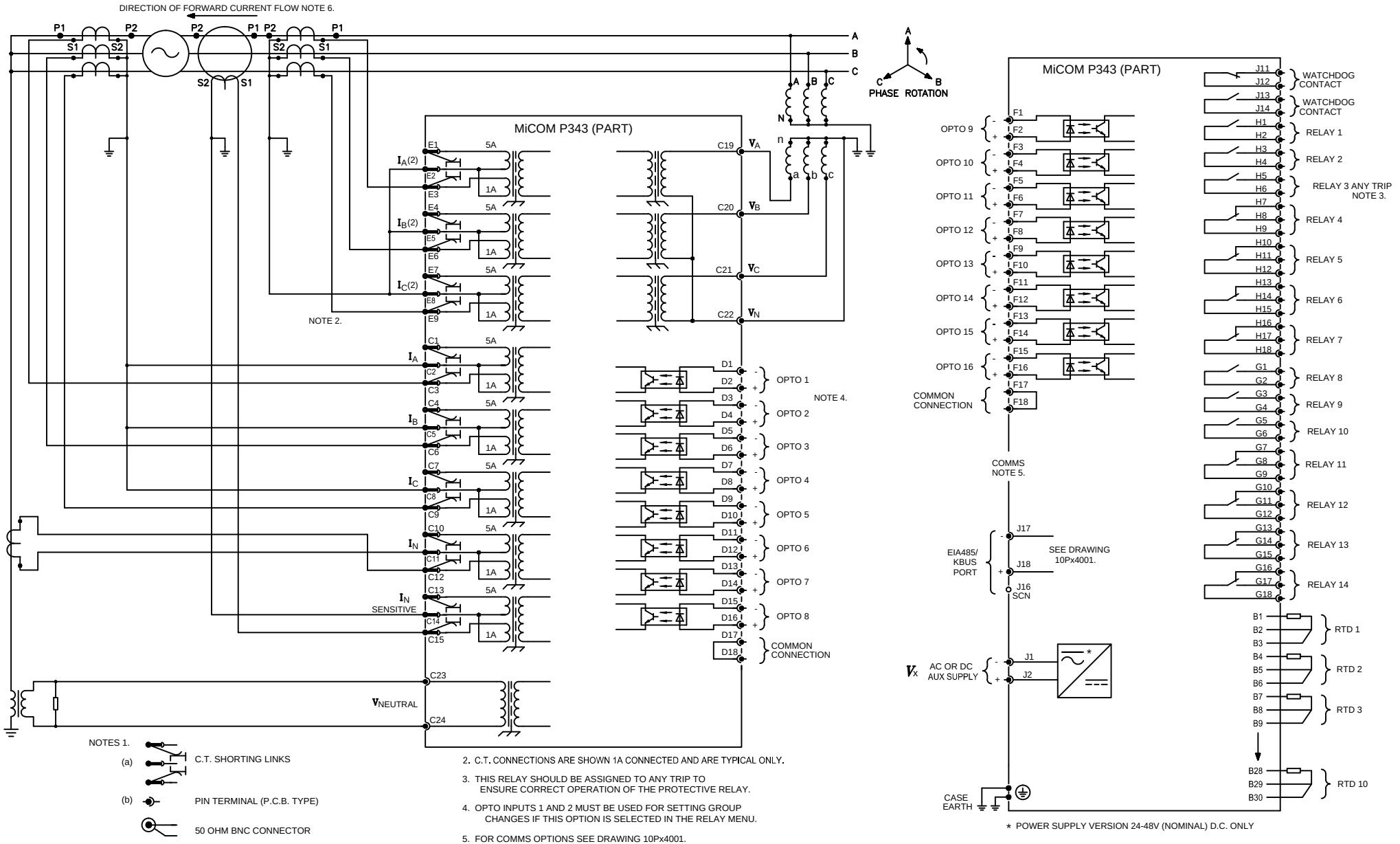
Issue: G	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROT RELAY WITH BIASED DIFFERENTIAL USING VEE CONNECTED VTs (16 I/P & 14 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34301	Sht: 5
Date:	Chkd: G.L.				Next Sht: 6



Issue: H	Revision: CID PWIG-8KMJ2K			Title: EXT. CONN DIAGRAM: GENERATOR/TRANSF PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (16 I/P & 14 0/P)	
Date: 05/03/2014	Name: P.WIGGIN	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34301	Sht: 6
Date: 05/03/2014	Chkd: G. LLOYD				Next Sht: 7



Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) BIASED DIFF + V CHK SYNC (16 I/P & 14 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34301	Sht: 7
Date:	Chkd: G.L.				Next Sht: -



NOTES 1.

(a) C.T. SHORTING LINKS

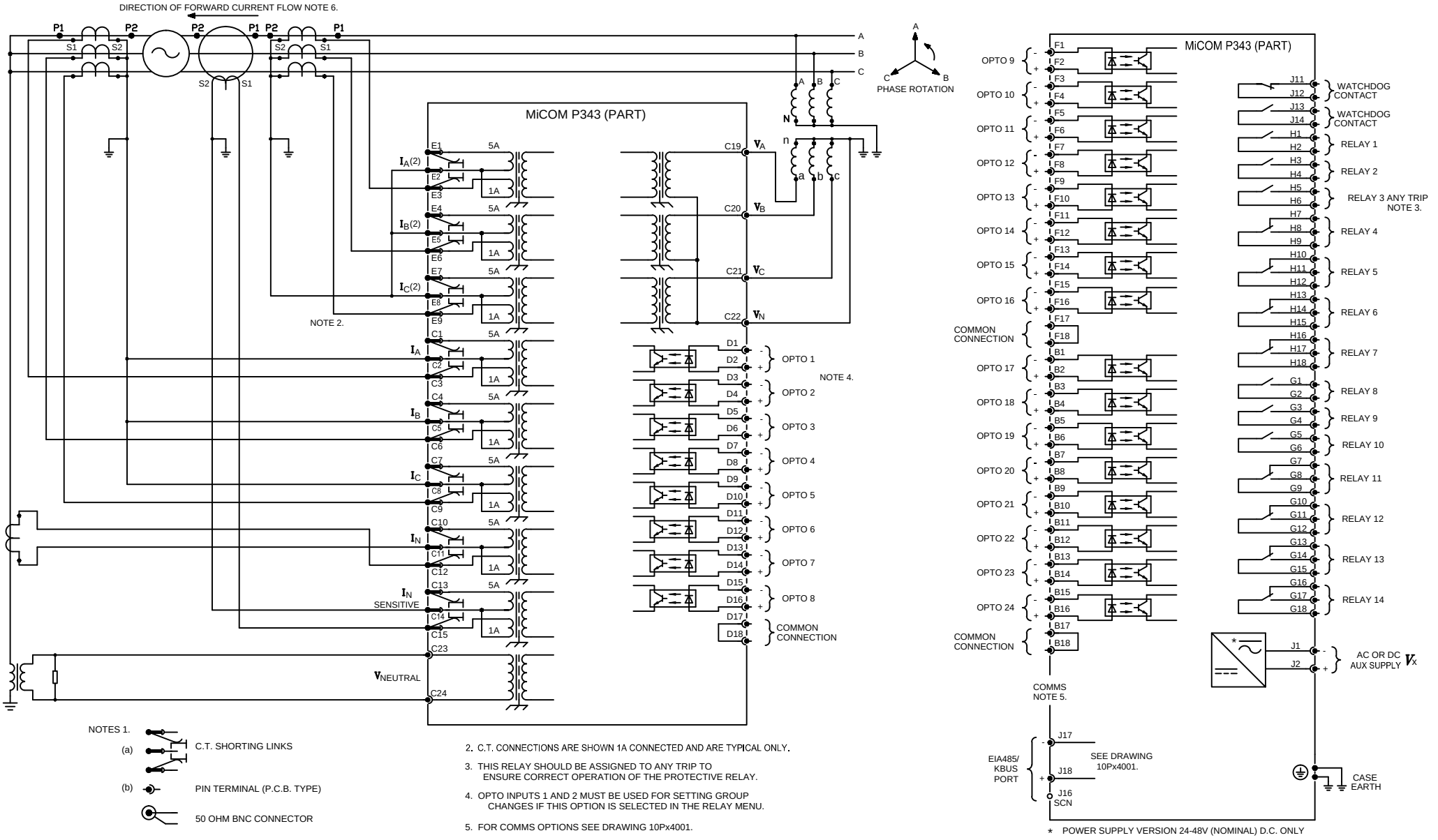
(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.

Issue: L	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (16 I/P & 14 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34302	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

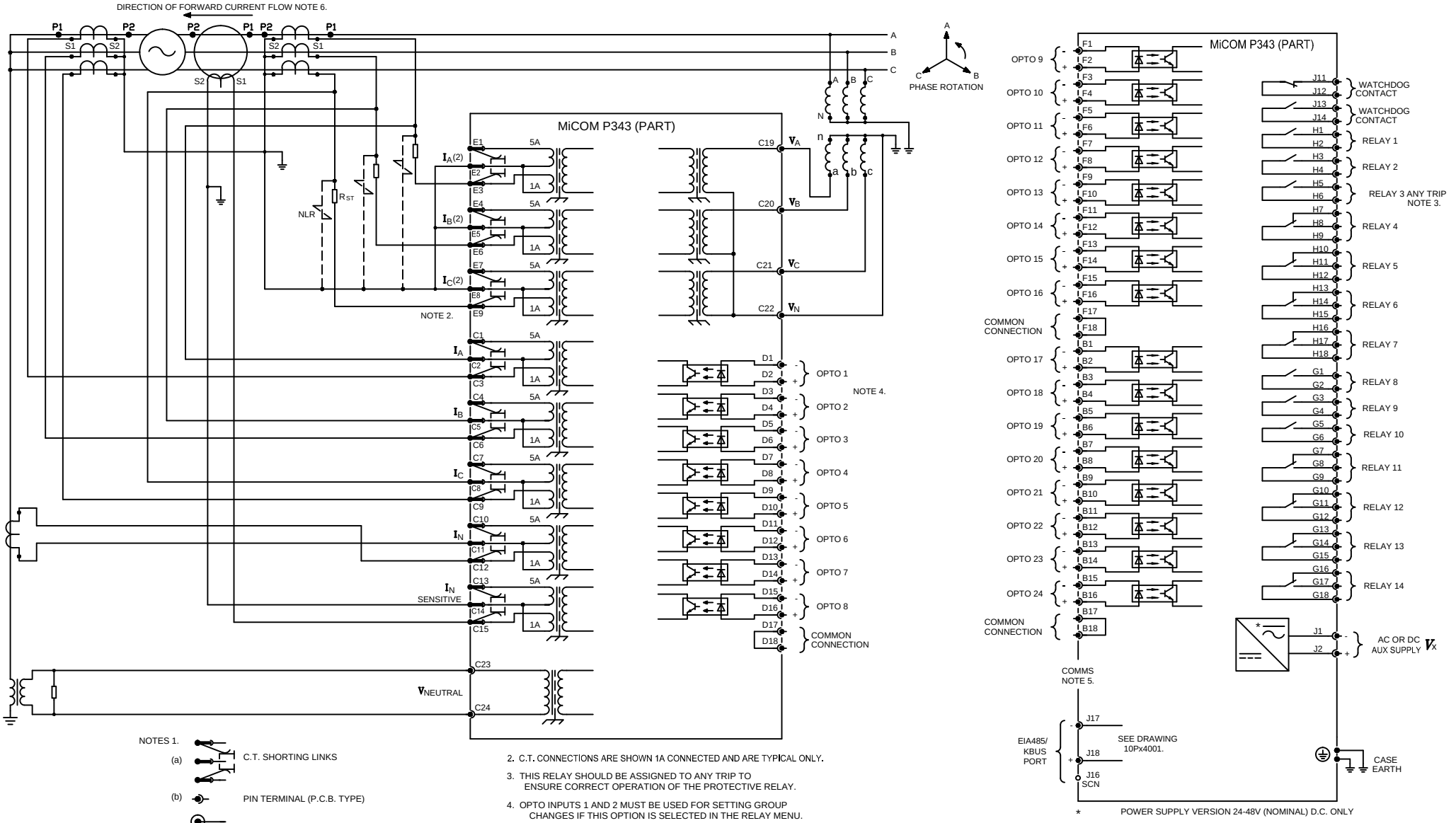
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

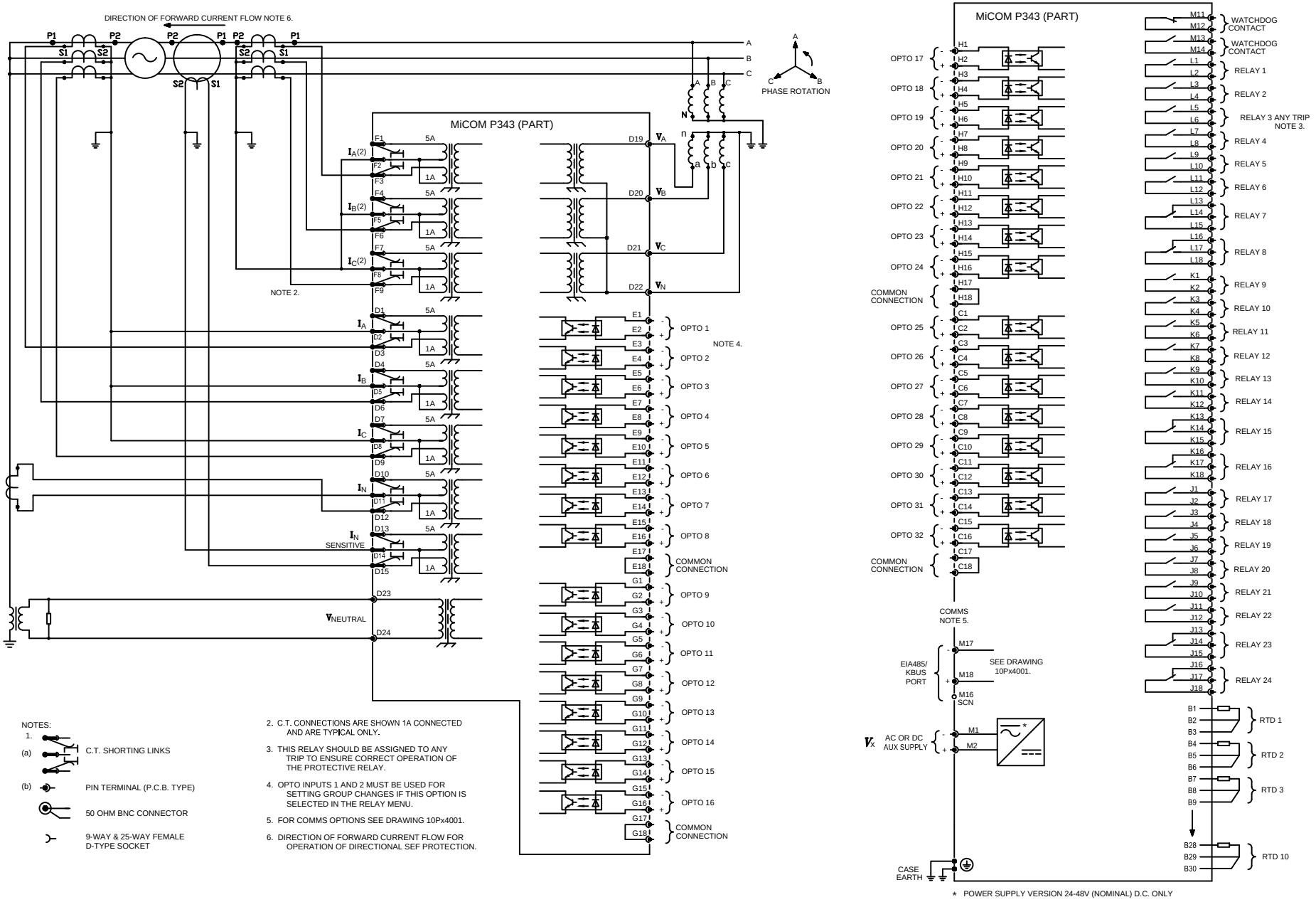
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

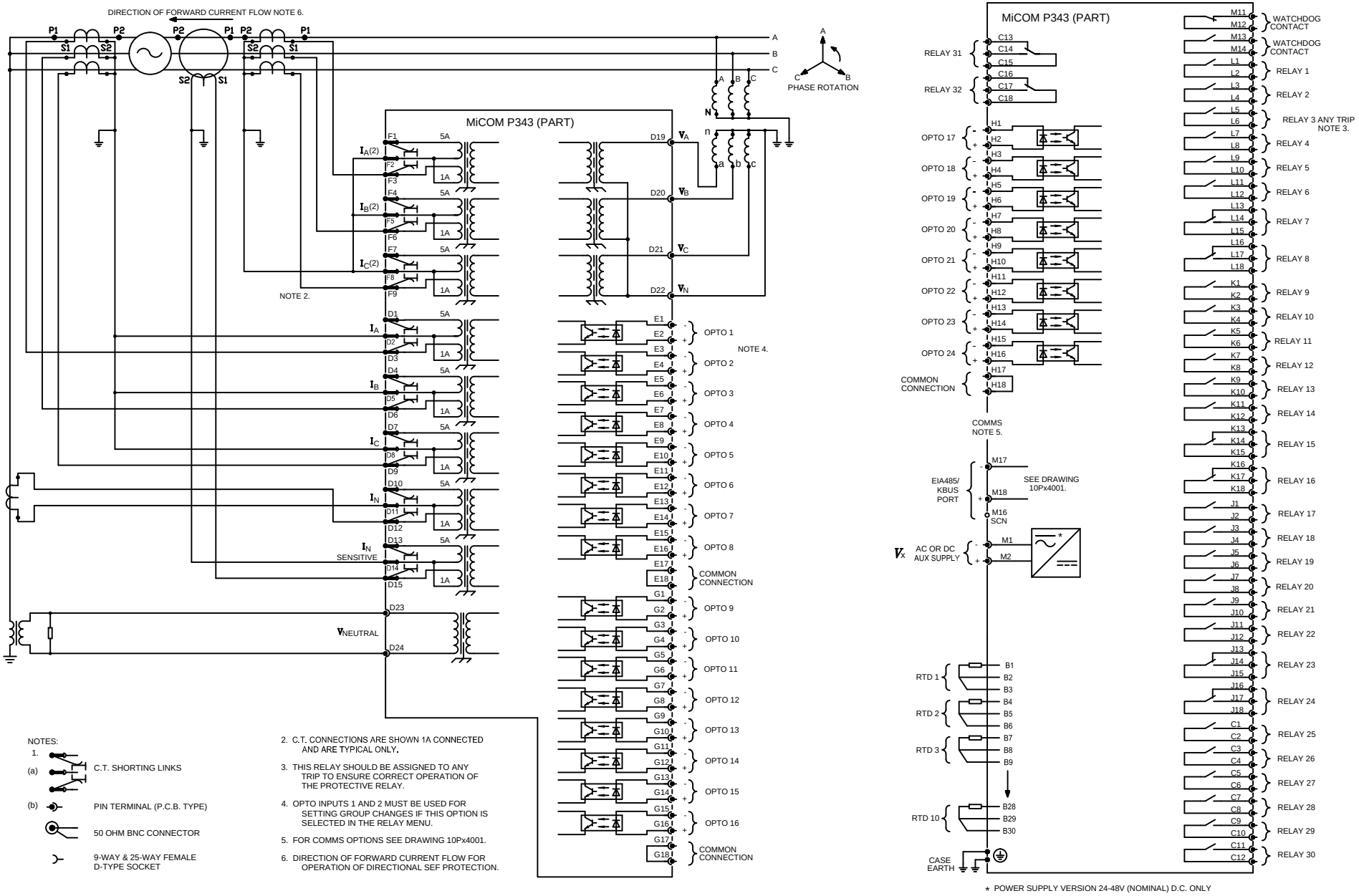
Issue: H	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (24 I/P & 14 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34303	Sht: 1
Date:	Chkd: T.Y.				Next Sht: 2



Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) WITH HIGH IMPEDANCE DIFFERENTIAL (24 I/P & 14 0/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34303	Sht: 3
Date:	Chkd: T.Y.				Next Sht: -



Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (32 I/P & 24 0/P)
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34309
Date:	Chkd: T.Y.			Sht: 1	Next Sht: 2

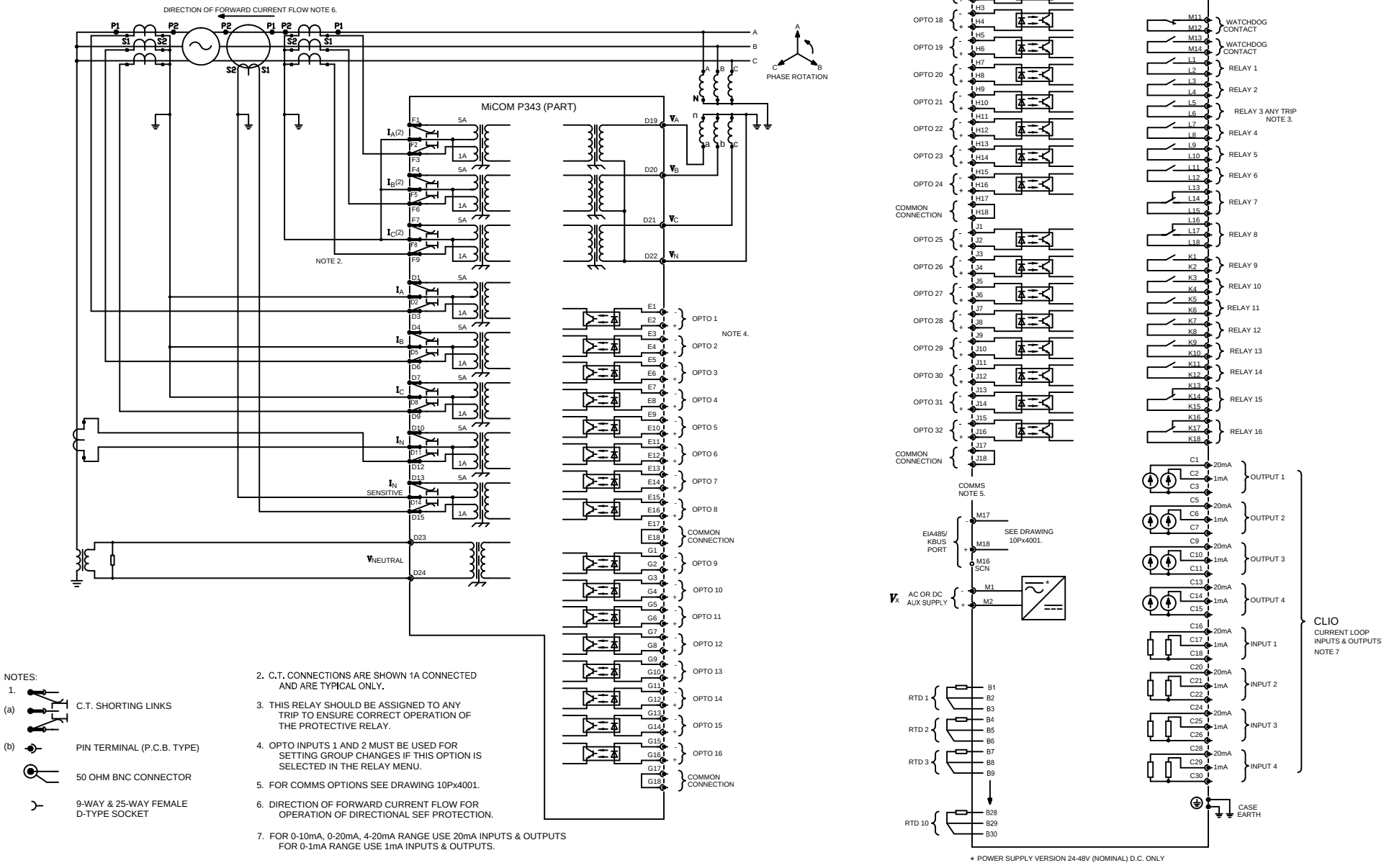


NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
   50 OHM BNC CONNECTOR
   9-WAY & 25-WAY FEMALE D-TYPE SOCKET
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

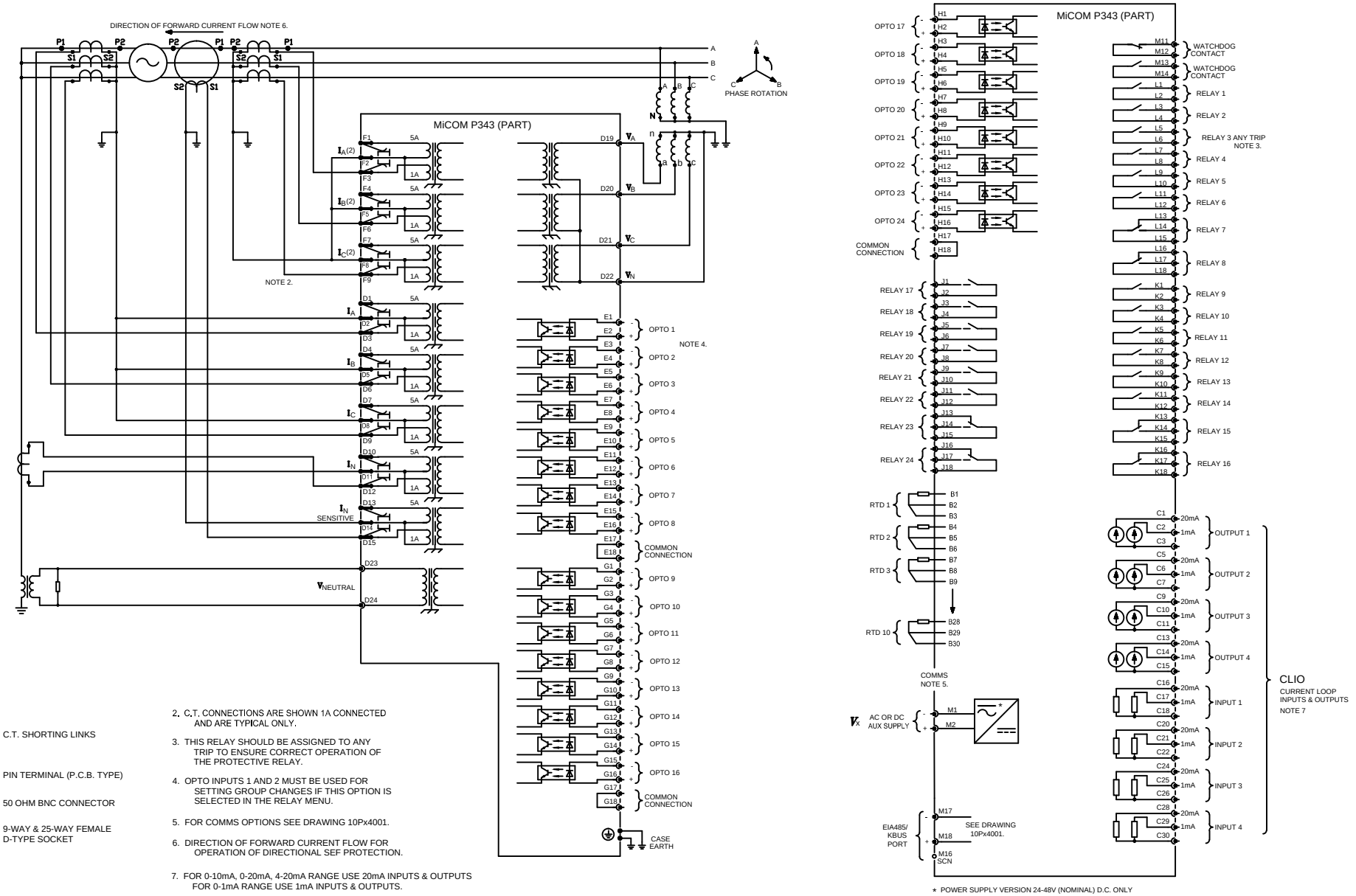
Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (24 I/P & 32 O/P)
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34310
Date:	Chkd: T.Y.			Sht: 1	Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
   50 OHM BNC CONNECTOR
   9-WAY & 25-WAY FEMALE D-TYPE SOCKET
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
7. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

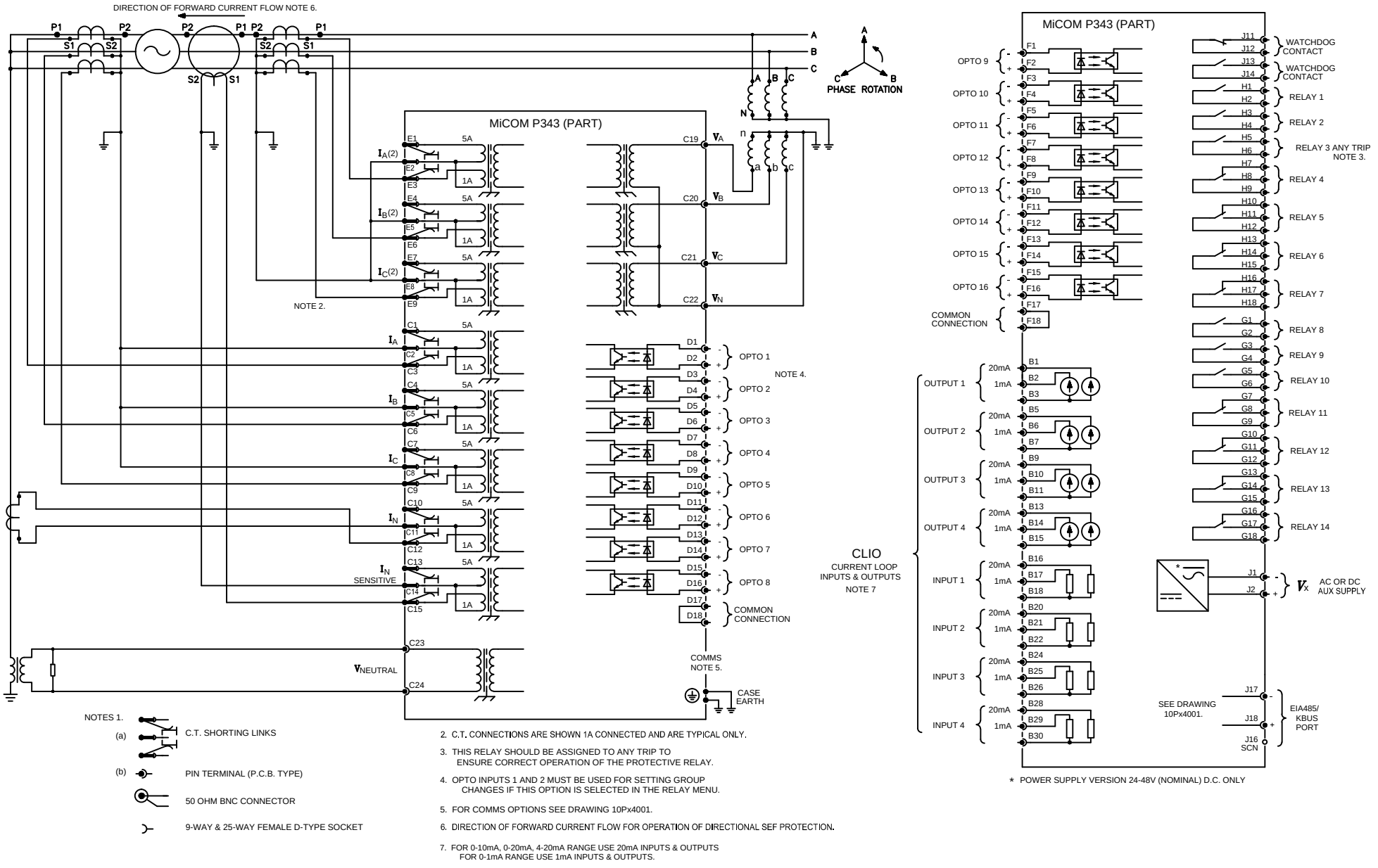
Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT CONN DIAG: (80TE) GENERATOR PROTECTION WITH BIASED DIFFERENTIAL (32 I/P & 16 0/P + CLIO + RTD)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34311	Sht: 1
Date:	Chkd:				Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
   50 OHM BNC CONNECTOR
   9-WAY & 25-WAY FEMALE D-TYPE SOCKET
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
7. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT CONN DIAG: (80TE) GENERATOR PROTECTION WITH BIASED DIFFERENTIAL (24 I/P, 24 O/P + CLIO + RTD)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34313	Sht: 1
Date:	Chkd:				Next Sht: 2



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

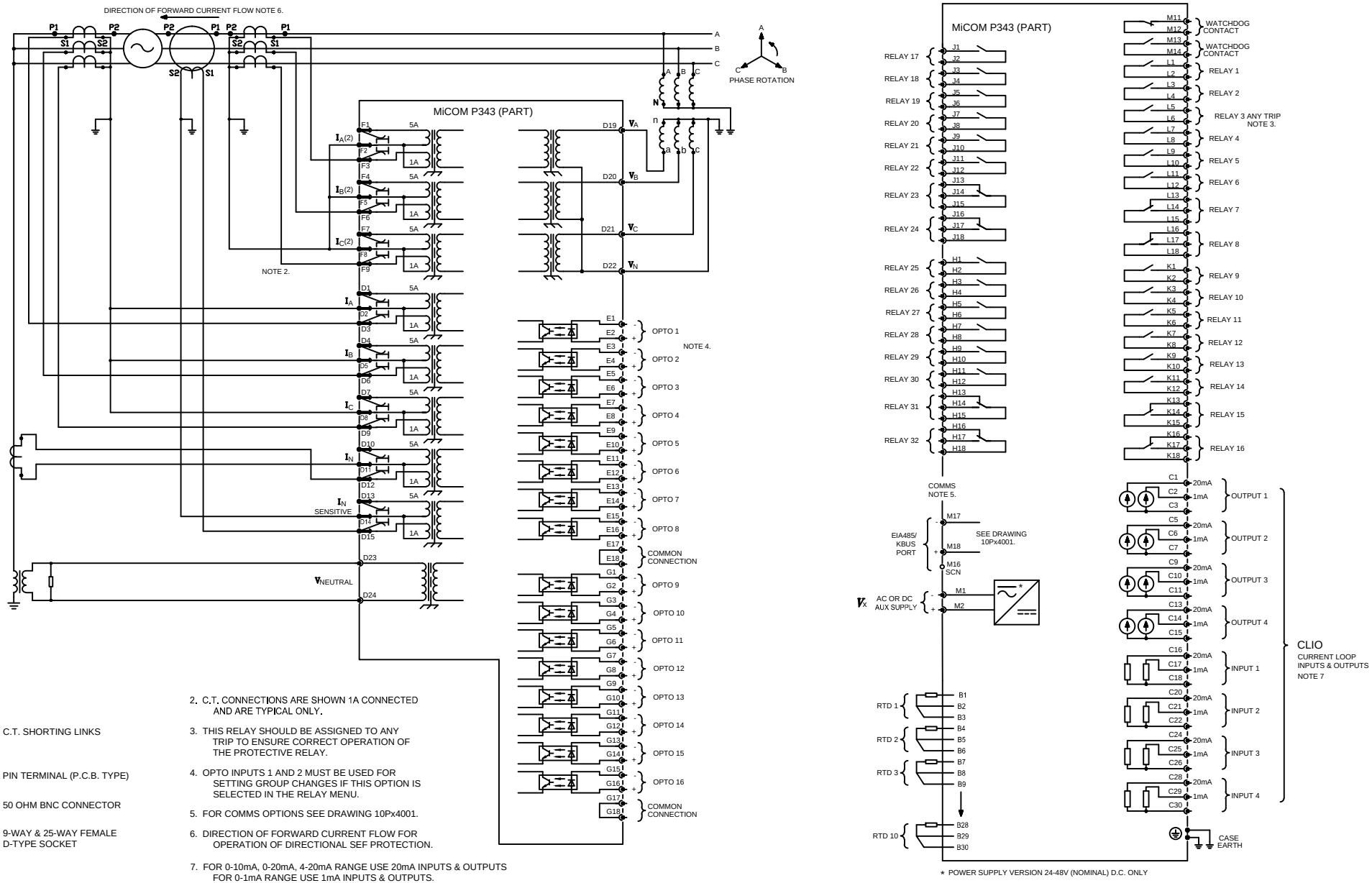
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
7. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

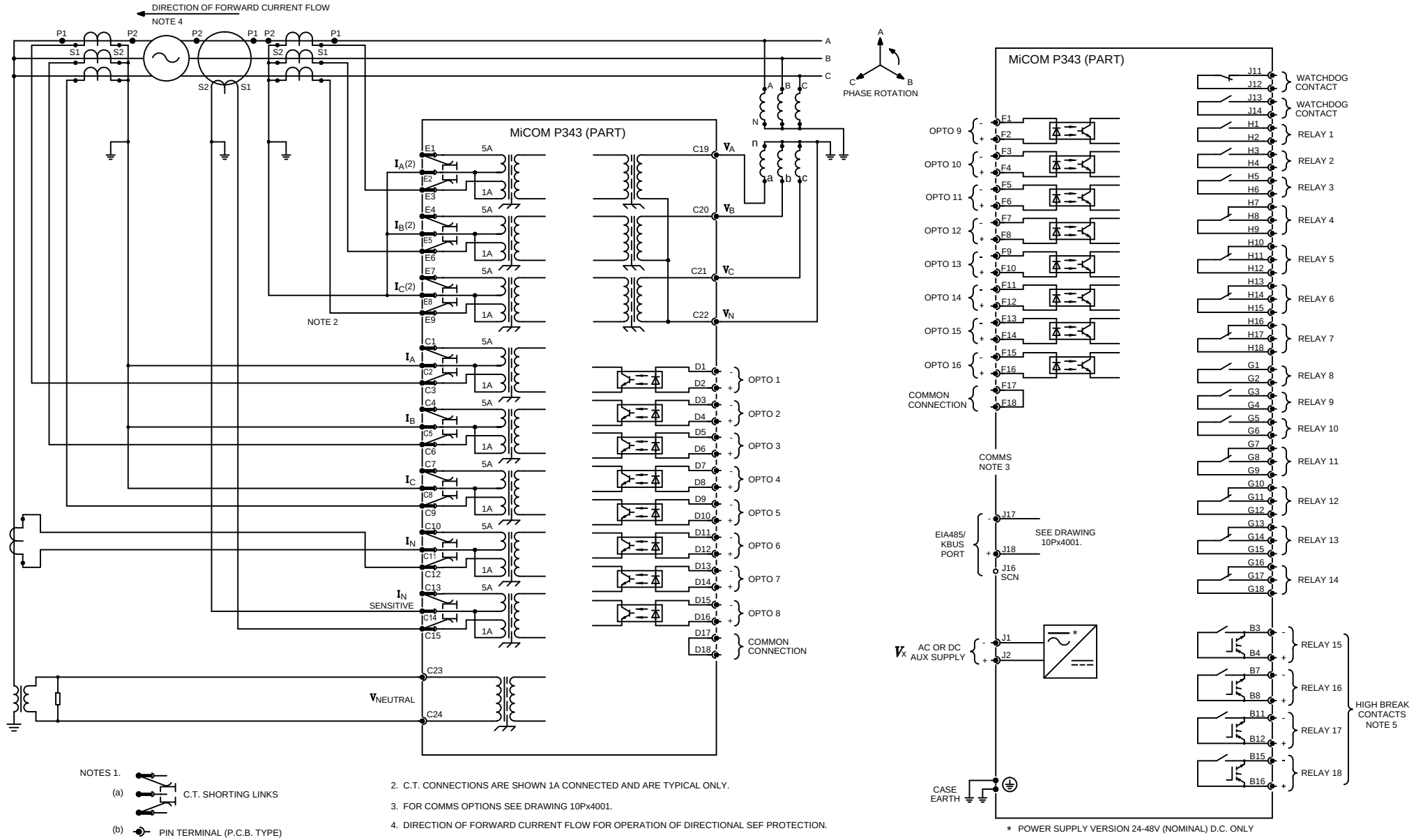
Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT CONN DIAG: (60TE) GENERATOR PROTECTION WITH BIASED DIFFERENTIAL (16 I/P & 14 O/P + CLIO)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34314	Sht: 1
Date:	Chkd:				Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
   50 OHM BNC CONNECTOR
   9-WAY & 25-WAY FEMALE D-TYPE SOCKET
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
7. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXT CONN DIAG: GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (16 I/P & 32 0/P + CLIO + RTD)
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34315
Date:	Chkd:			Sht: 1	Next Sht: 2



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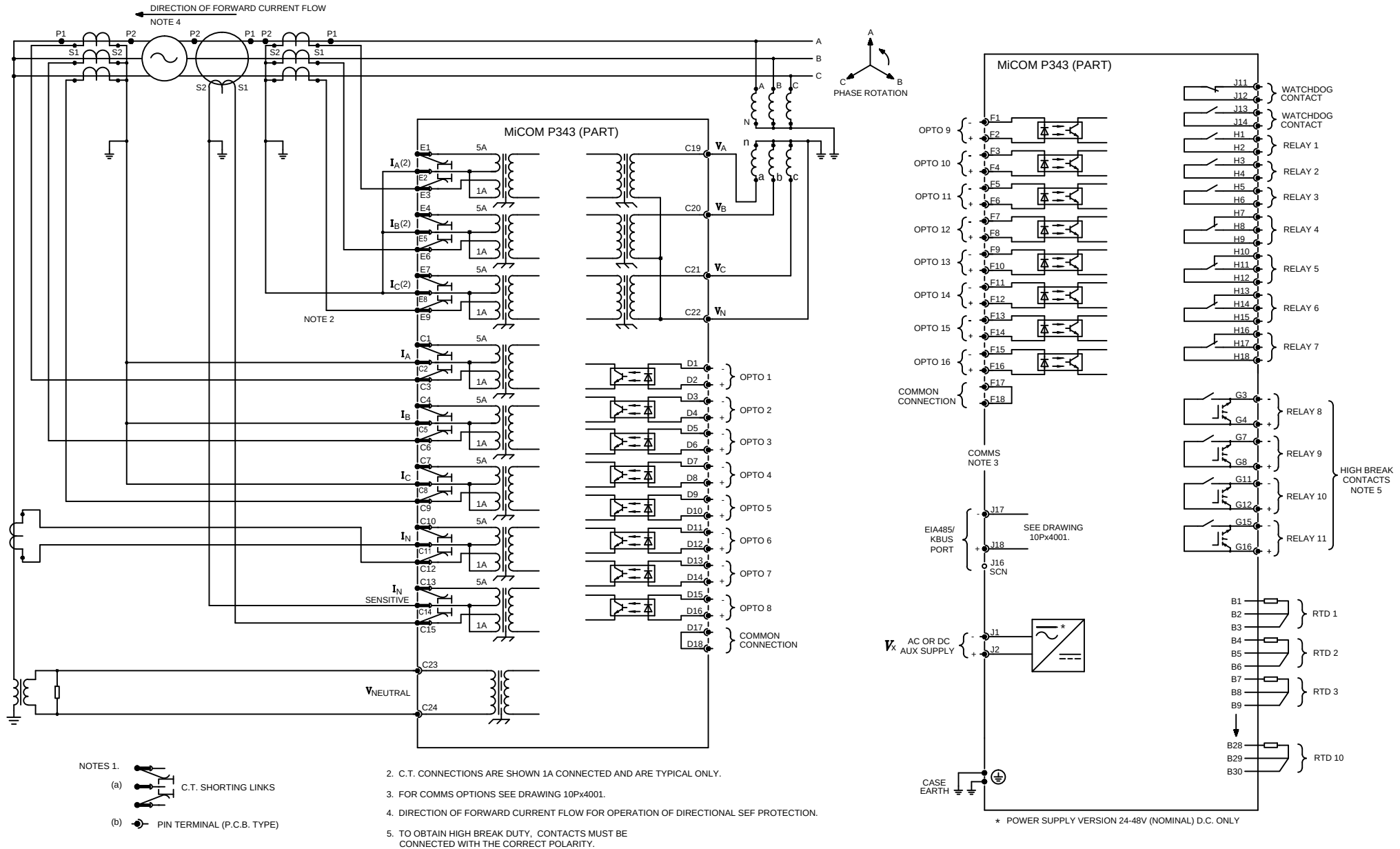
(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
5. TO OBTAIN HIGH BREAK DUTY, CONTACTS MUST BE CONNECTED WITH THE CORRECT POLARITY.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (16 I/P & 18 O/P)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34316	Sht: 1
Date:	Chkd:				Next Sht: 2



NOTES 1.

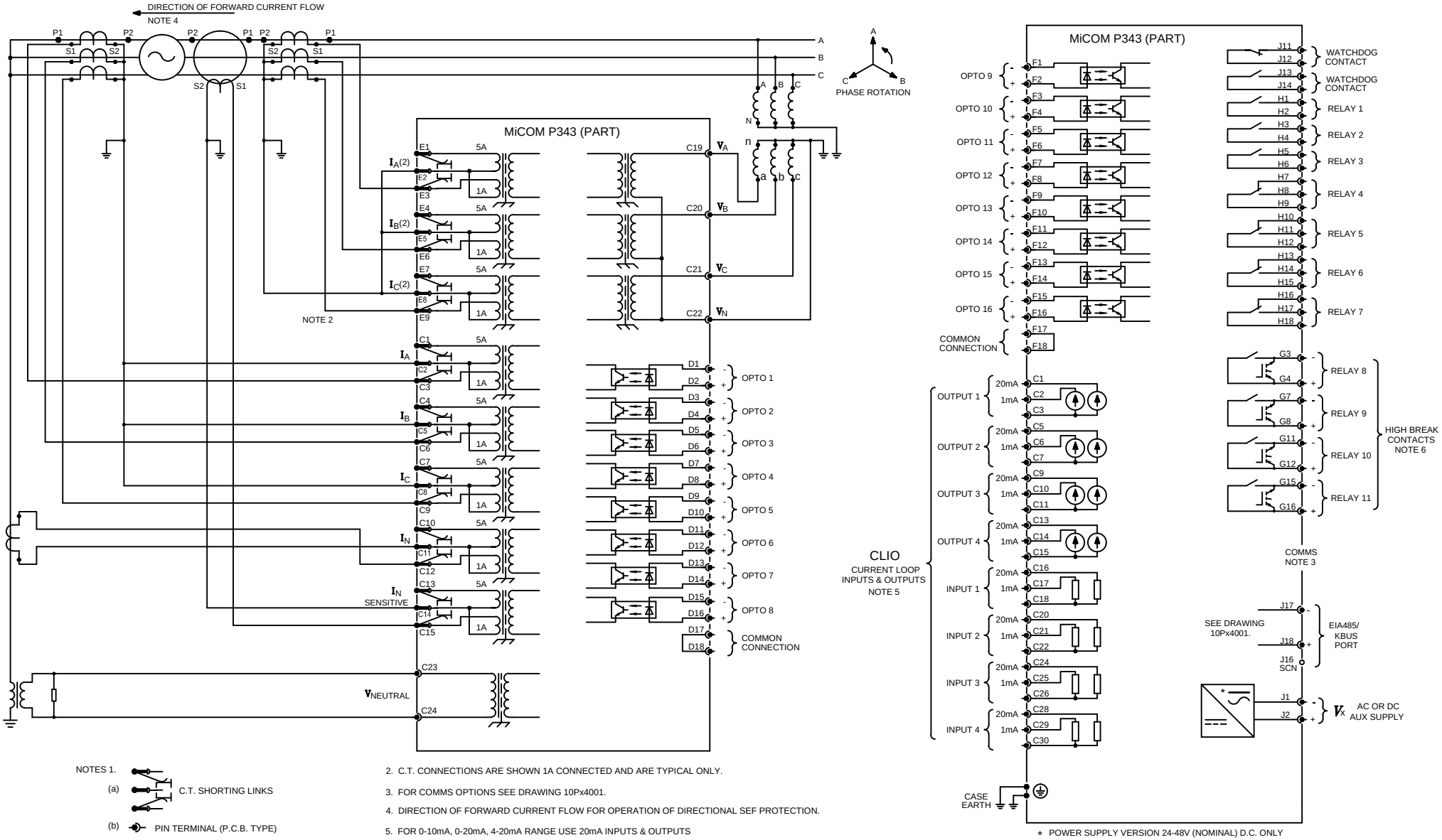
(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
5. TO OBTAIN HIGH BREAK DUTY, CONTACTS MUST BE CONNECTED WITH THE CORRECT POLARITY.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL (16 I/P & 11 O/P + RTD)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34317	Sht: 1
Date:	Chkd:				Next Sht: 2



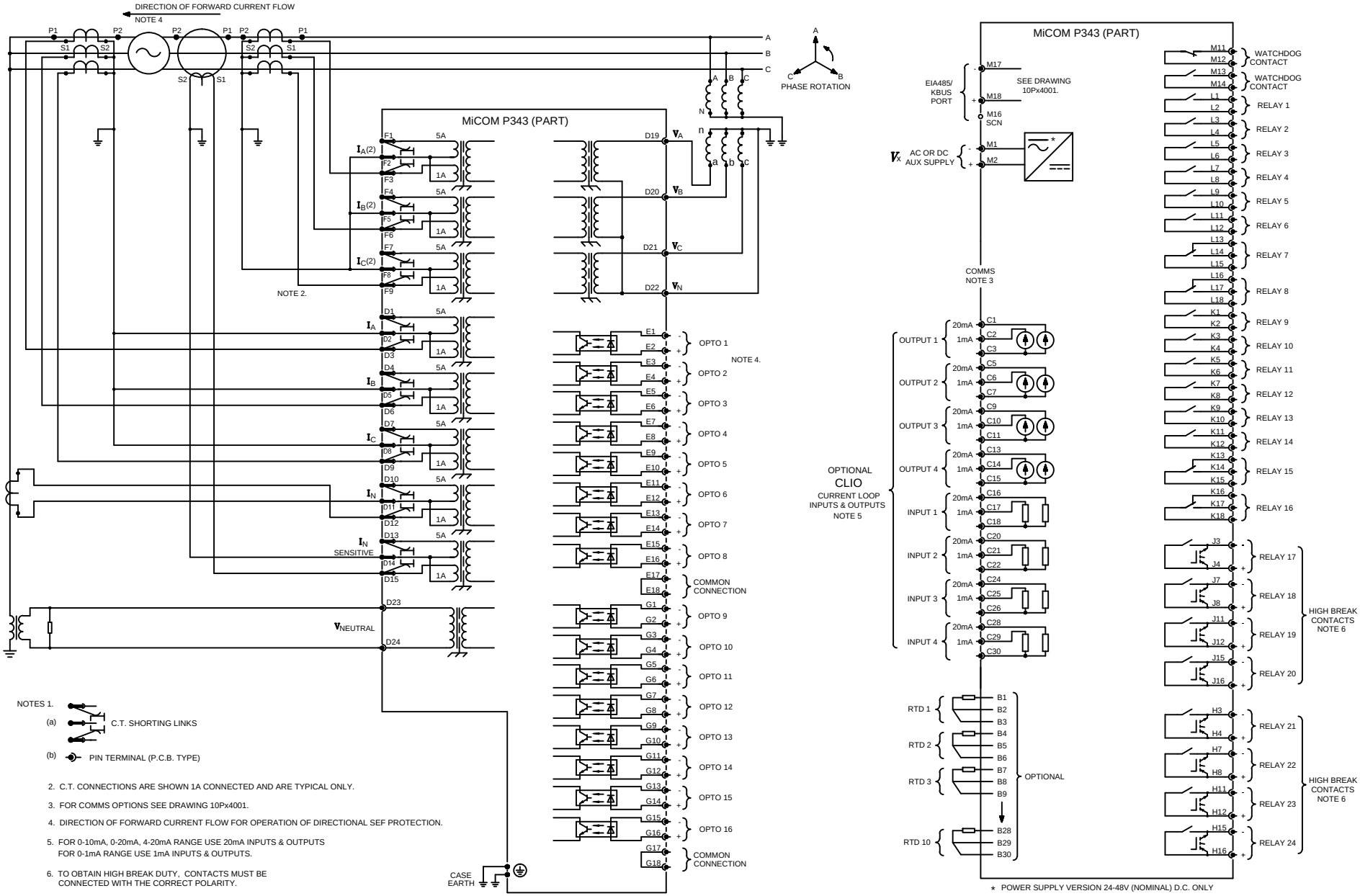
NOTES 1.

(a) C.T. SHORTING LINKS

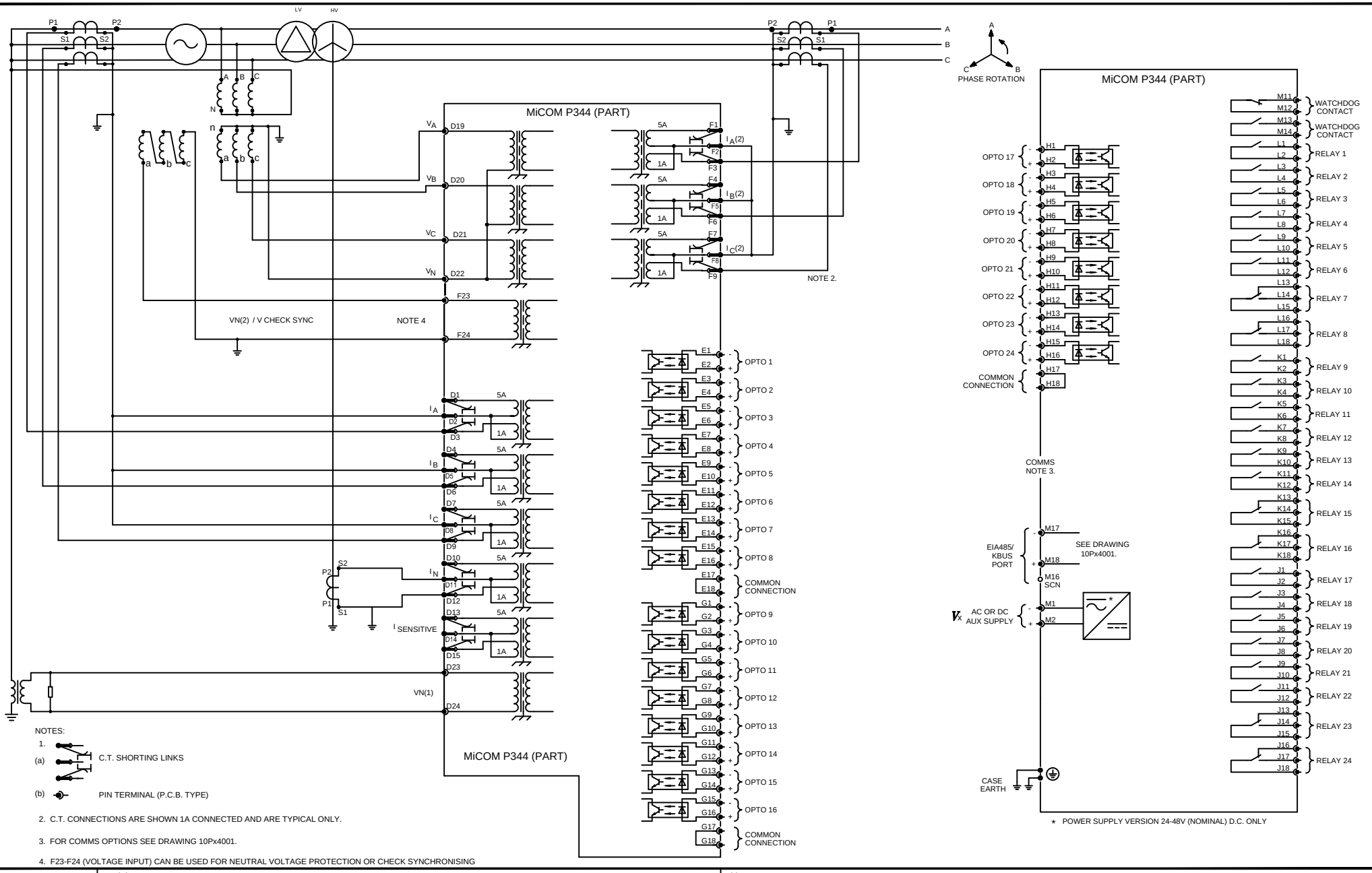
(b) PIN TERMINAL (P.C.B. TYPE)

2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
5. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.
6. TO OBTAIN HIGH BREAK DUTY, CONTACTS MUST BE CONNECTED WITH THE CORRECT POLARITY.

Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXTERNAL CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (60TE) WITH BIASED DIFFERENTIAL(16 I/P & 11 O/P + CLIO)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34318	Sht: 1
Date:	Chkd:				Next Sht: 2



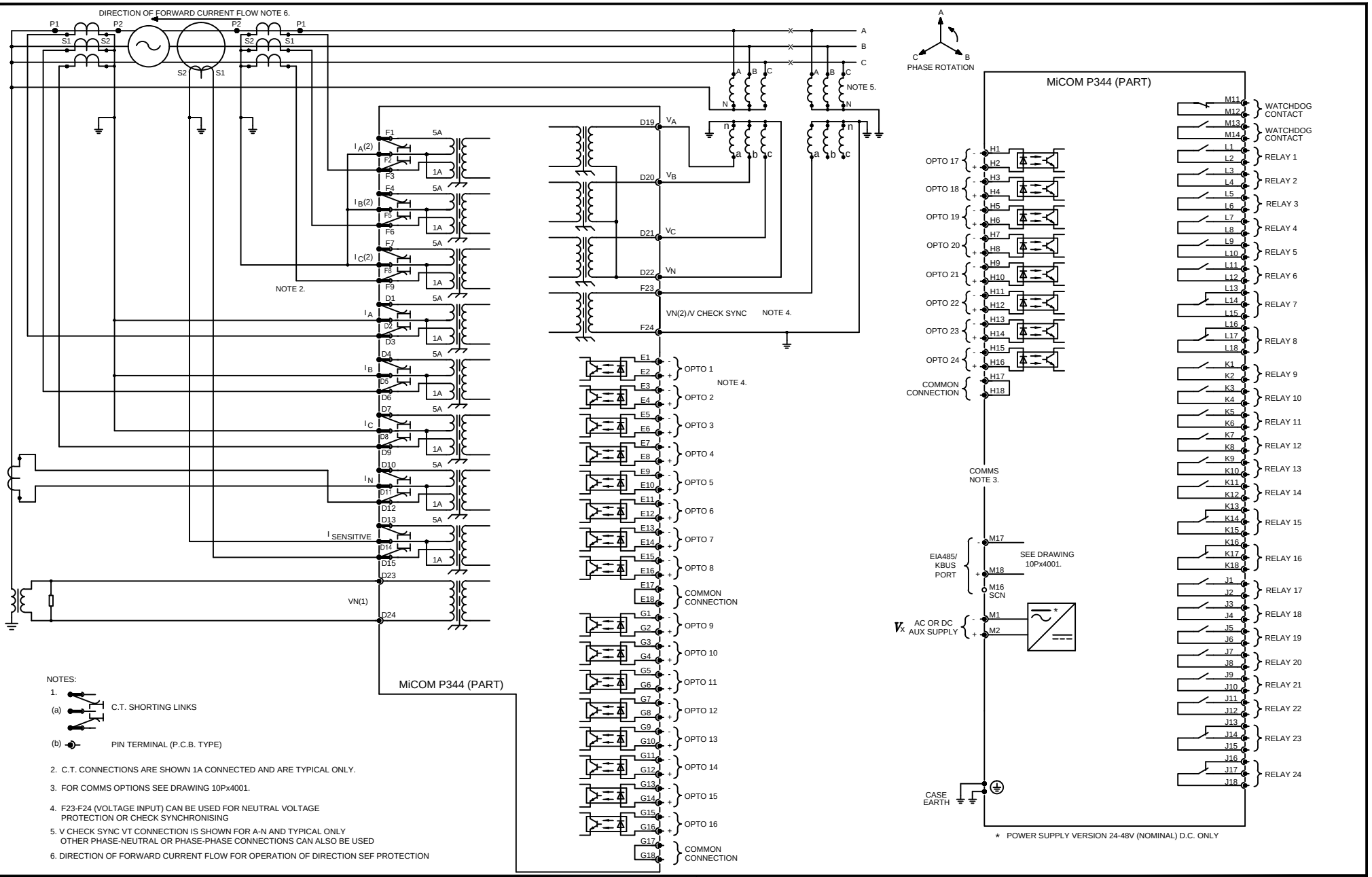
Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAG: GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFFERENTIAL (16 I/P & 24 O/P + CLIO & RTD)	
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34319	Sht: 1
Date:	Chkd:				Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. F23-F24 (VOLTAGE INPUT) CAN BE USED FOR NEUTRAL VOLTAGE PROTECTION OR CHECK SYNCHRONISING

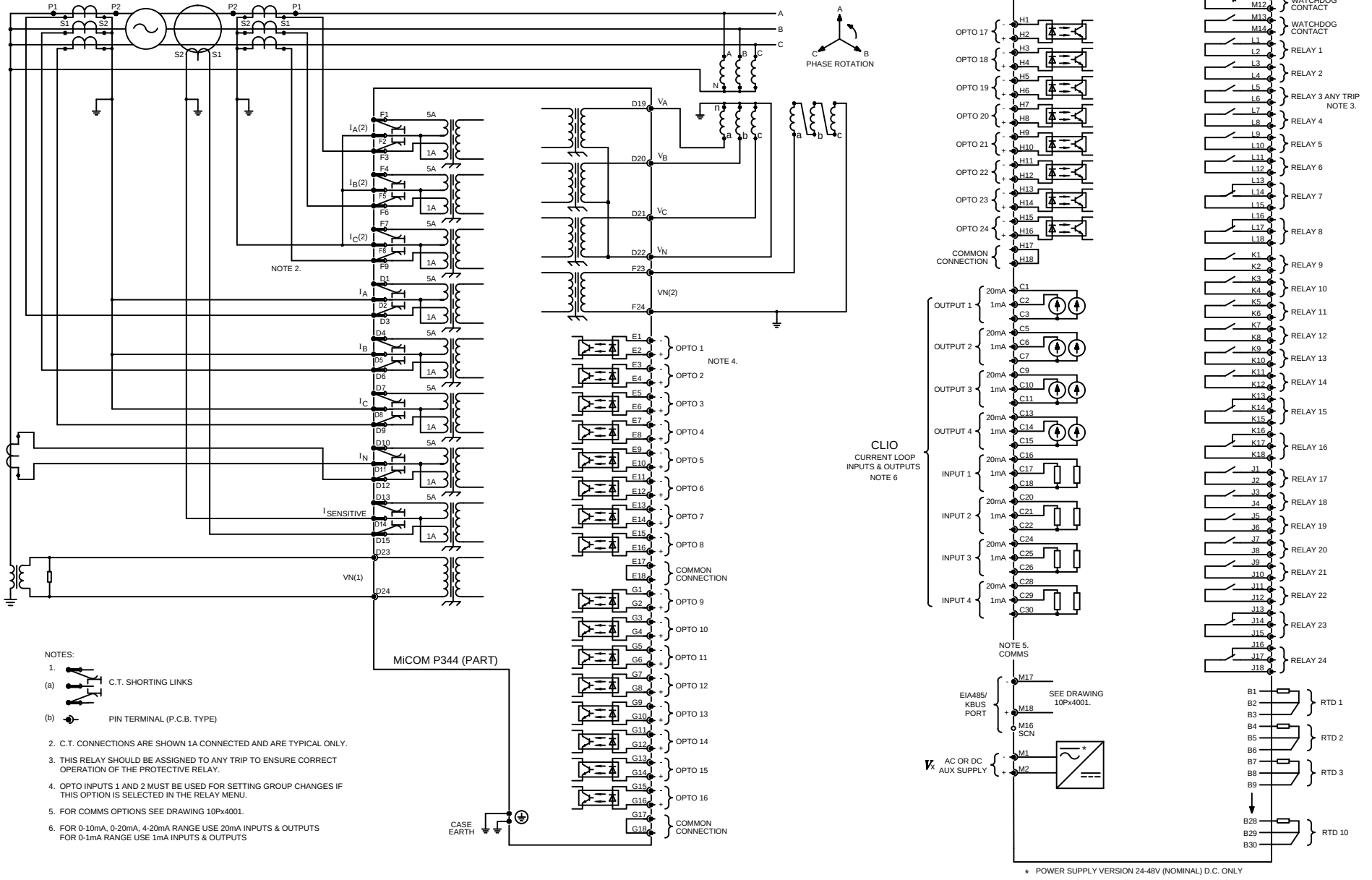
Issue: F	Revision: CID PWIG-8KMJ2K			Title:	EXT. CONN DIAGRAM: GENERATOR TRANSF PROTECTION RELAY (80 TE) WITH BIASED DIFF & NVD INTERTURN (24 IP & 24 OP)
Date: 05/03/2014	Name: P.WIGGIN	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34401
Date: 05/03/2014	Chkd: G LLOYD			Sht: 6	Next Sht: 7



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. F23-F24 (VOLTAGE INPUT) CAN BE USED FOR NEUTRAL VOLTAGE PROTECTION OR CHECK SYNCHRONISING
5. V CHECK SYNC VT CONNECTION IS SHOWN FOR A-N AND TYPICAL ONLY OTHER PHASE-NEUTRAL OR PHASE-PHASE CONNECTIONS CAN ALSO BE USED
6. DIRECTION OF FORWARD CURRENT FLOW FOR OPERATION OF DIRECTION SEF PROTECTION

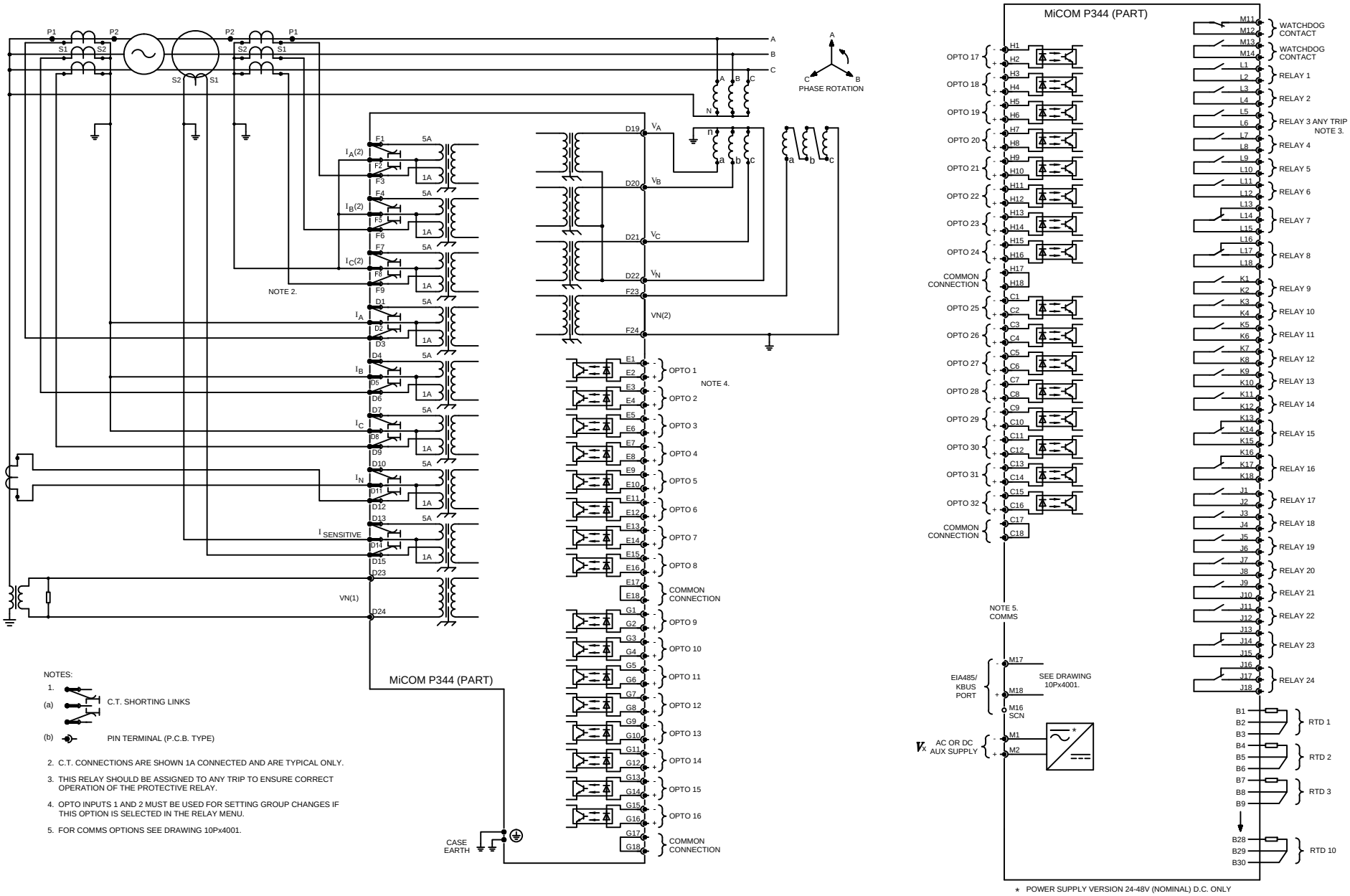
Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXTERNAL CONN DIAGRAM: GENERATOR PROTECTION RELAY BIASED DIFF + NVD INTERTURN + V CHECK SYNC (24 I/P & 24 0/P)
Date: 26/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34401
Date:	Chkd: G.L.			Sht: 7	Next Sht: -



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS

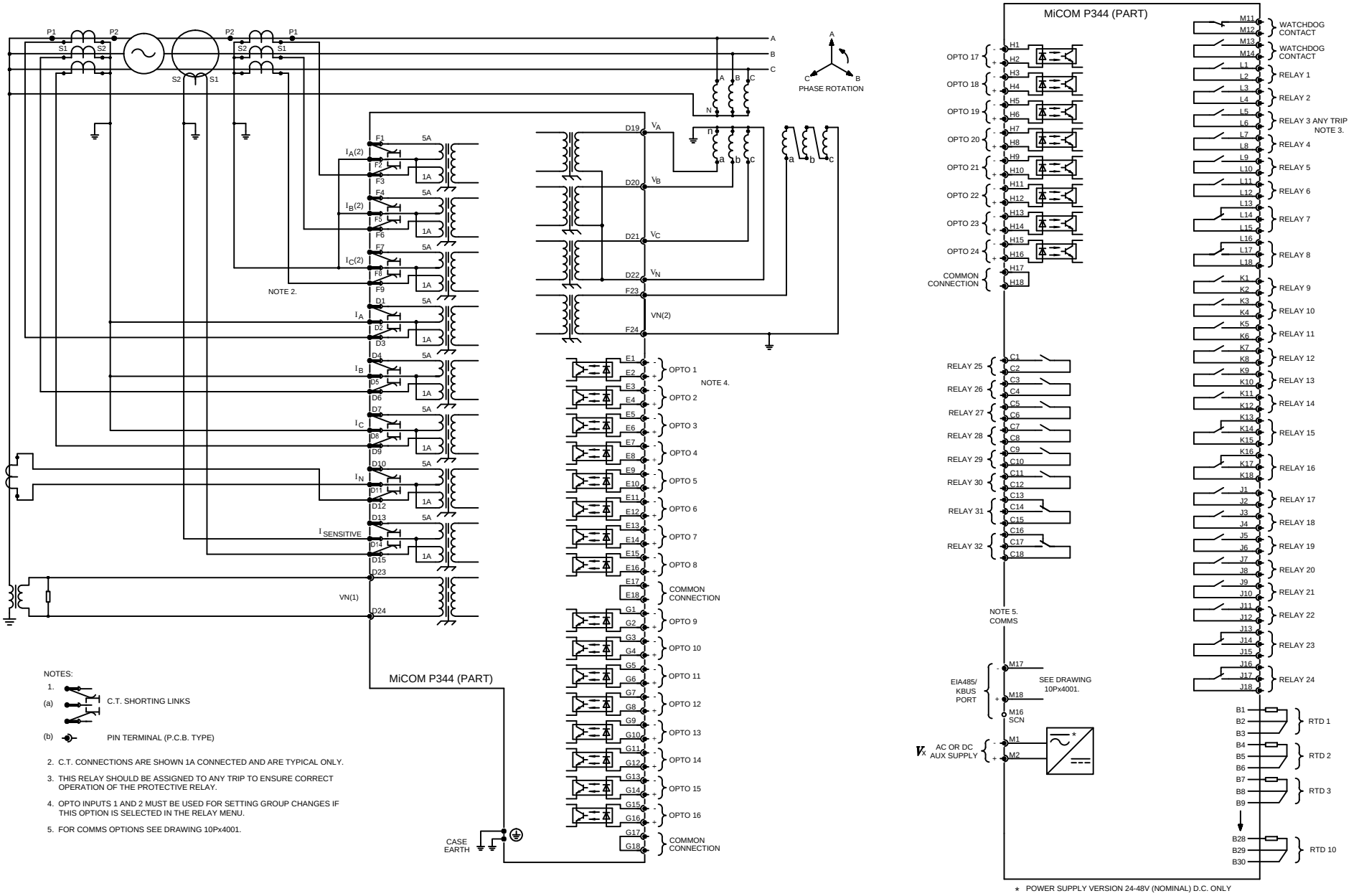
Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXT. CONN. DIAG: GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFF'TIAL & NVD INTERTURN (24 I/P & 24 O/P+CLIO & RTD)
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34406
Date:	Chkd: T. YIP			Sht: 1	Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

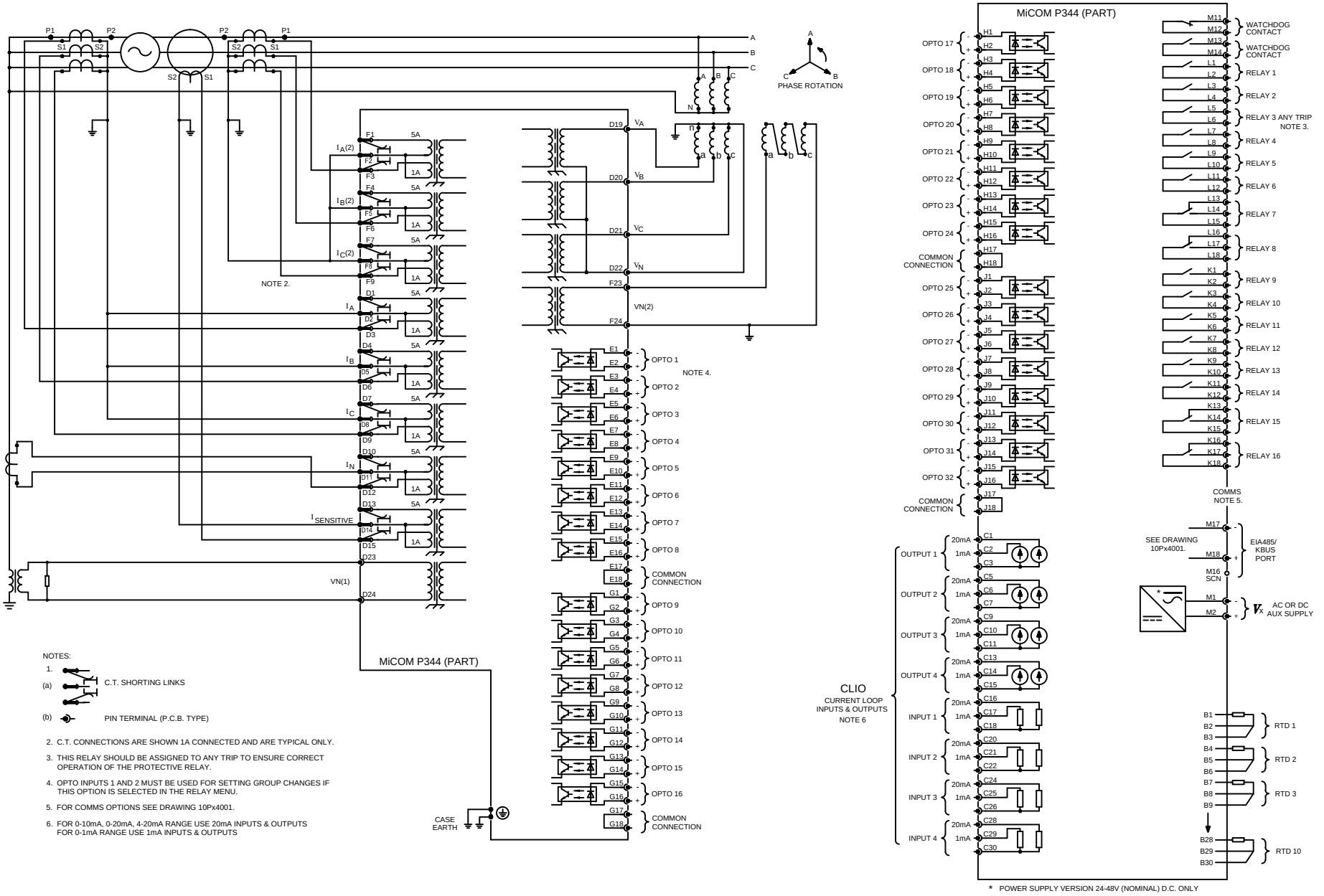
Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONN. DIAG: GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFF'TIAL & NVD INTERTURN (32 I/P & 24 O/P + RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34407	Sht: 1
Date:	Chkd: T. YIP				Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

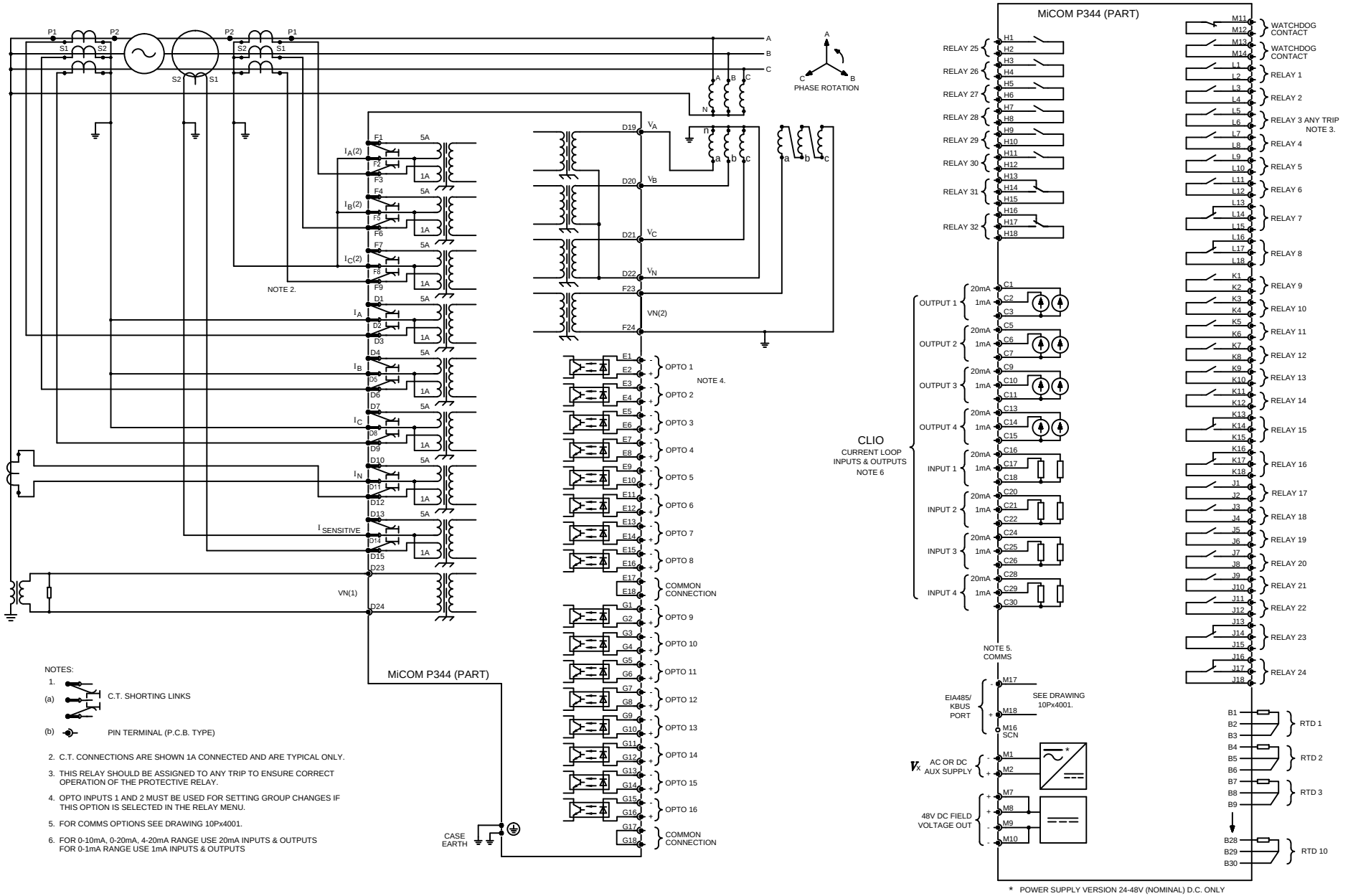
Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXT. CONN, DIAG GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFF'TIAL & NVD INTERTURN (24 I/P & 32 O/P + RTD)
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34408
Date:	Chkd: T. YIP			Sht: 1	Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS

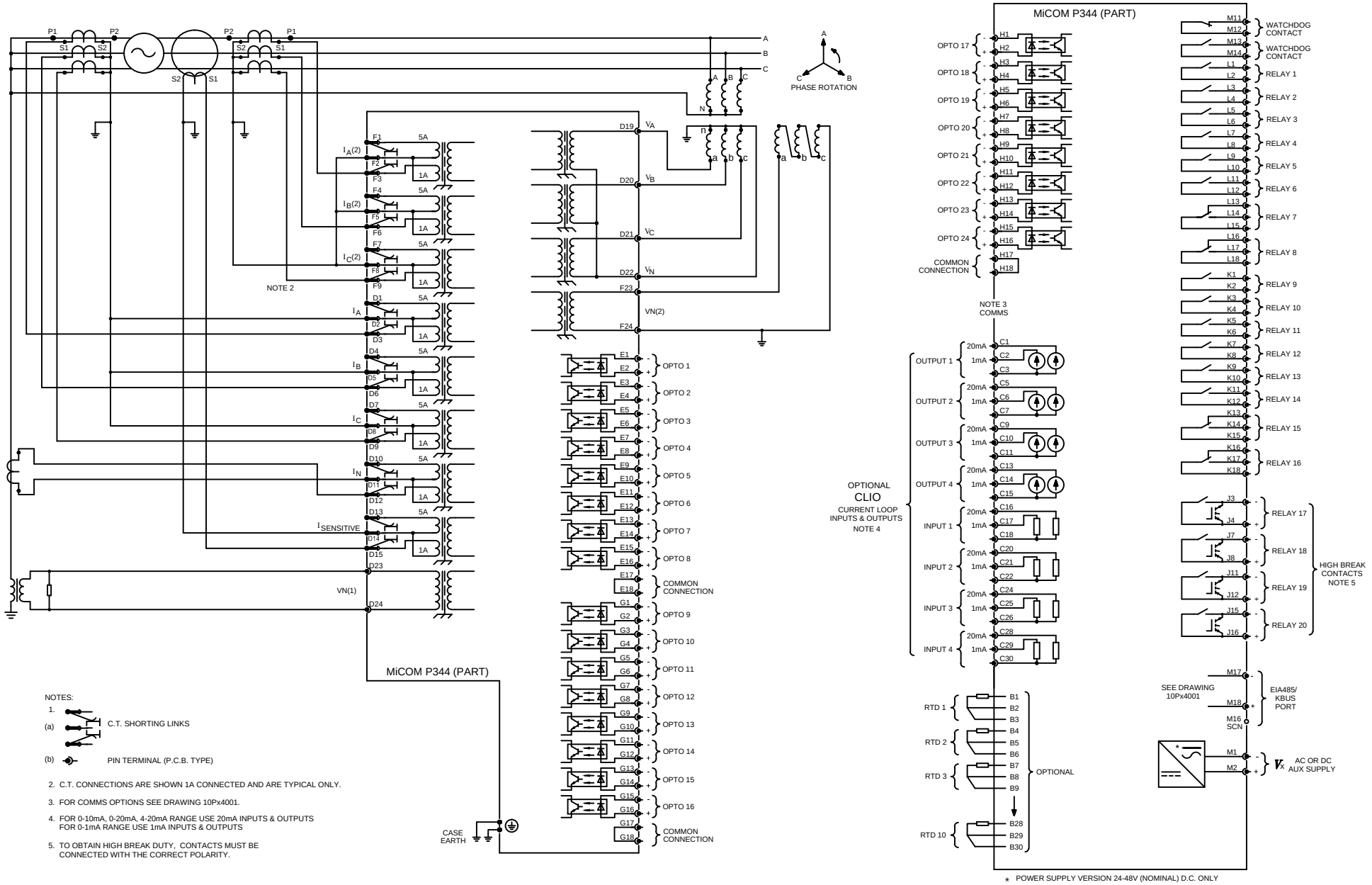
Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXT. CONN. DIAG: GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFF'TIAL & NVD INTERTURN (32 I/P & 16 O/P+CLIO & RTD)
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34409
Date:	Chkd: T. YIP			Sht: 1	Next Sht: 2



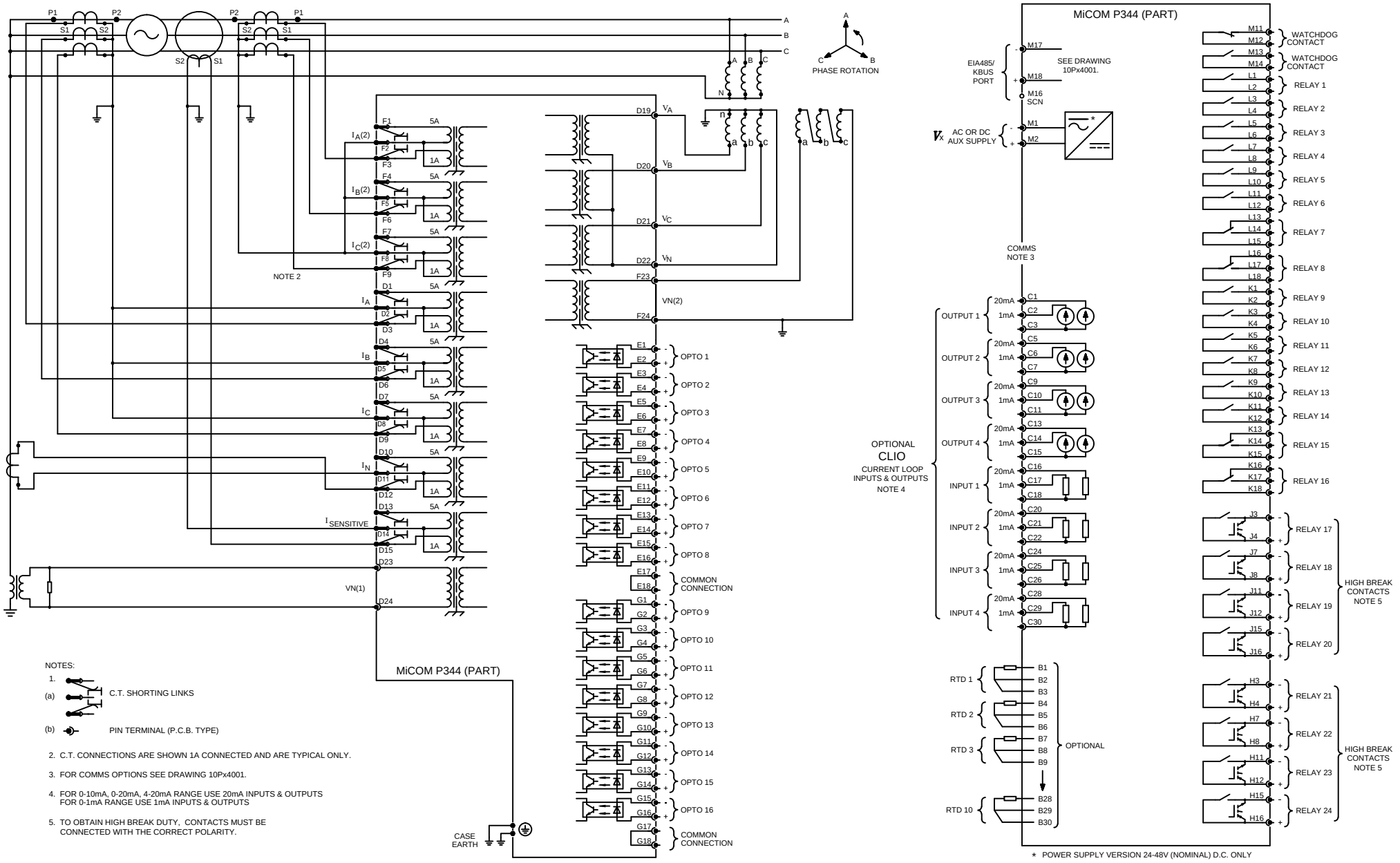
NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. THIS RELAY SHOULD BE ASSIGNED TO ANY TRIP TO ENSURE CORRECT OPERATION OF THE PROTECTIVE RELAY.
4. OPTO INPUTS 1 AND 2 MUST BE USED FOR SETTING GROUP CHANGES IF THIS OPTION IS SELECTED IN THE RELAY MENU.
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS

Issue: C	Revision: DRAWING OUTLINE UPDATED. CID BLIN-8BHLDT			Title: EXT. CONN DIAG GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFF'TIAL & NVD INTERTURN (16 I/P & 32 O/P+CLIO & RTD)	
Date: 26/11/2010	Name: W.LINTERN	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34410	Sht: 1
Date:	Chkd: T. YIP				Next Sht: 2



Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONN DIAG: GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFF'TIAL & NVD INTERTURN (24 I/P & 20 O/P+CLIO & RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34411	Sht: 1
Date:	Chkd:				Next Sht: 2



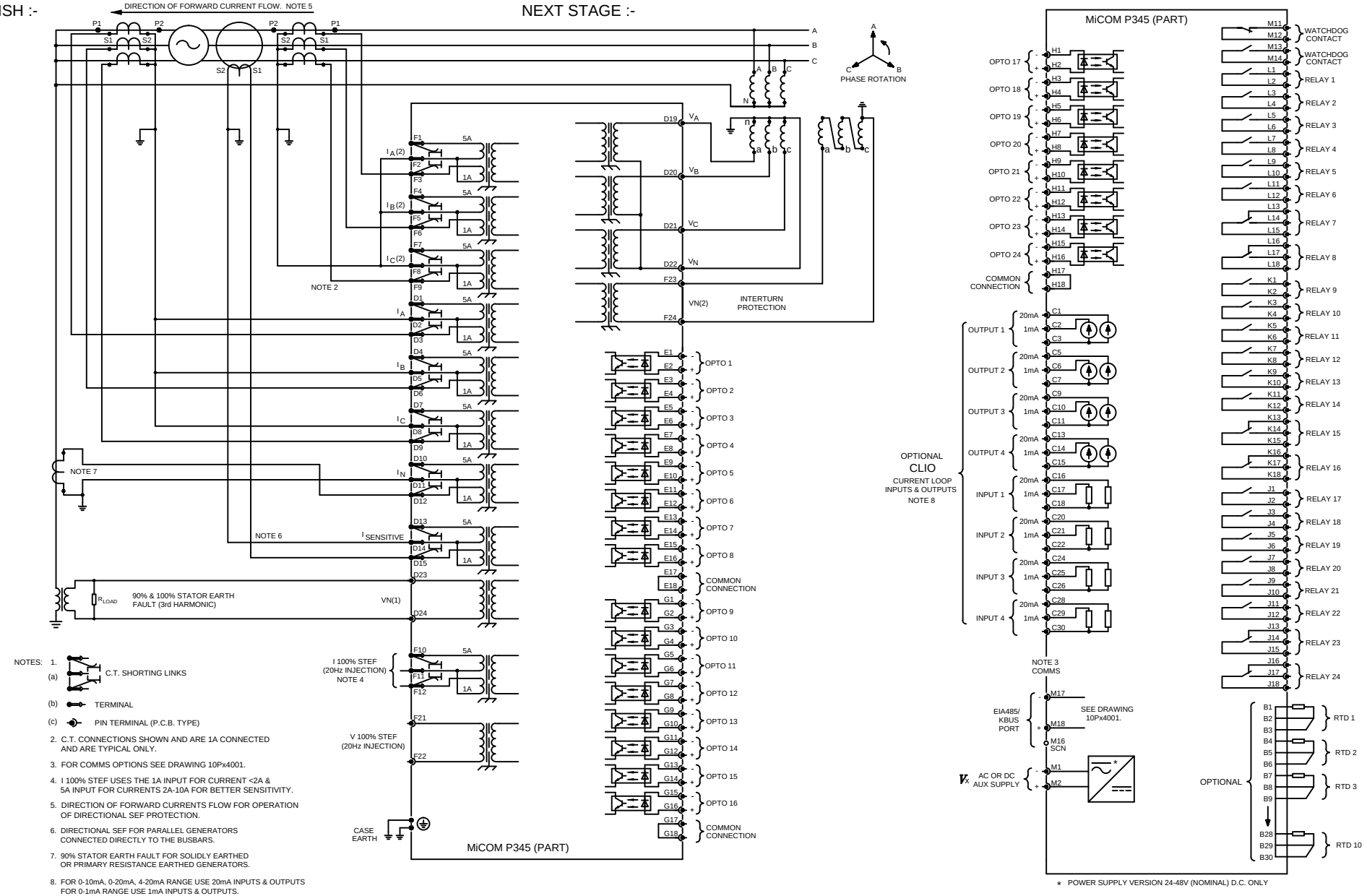
NOTES:

1. (a) C.T. SHORTING LINKS
   (b) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS
5. TO OBTAIN HIGH BREAK DUTY, CONTACTS MUST BE CONNECTED WITH THE CORRECT POLARITY.

Issue: D	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXT. CONN. DIAG: GENERATOR PROTECTION RELAY (80TE) WITH BIASED DIFF'TIAL & NVD INTERTURN (16 I/P & 24 O/P+CLIO & RTD)
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34412
Date:	Chkd:			Sht: 1	Next Sht: 2

FINISH :-

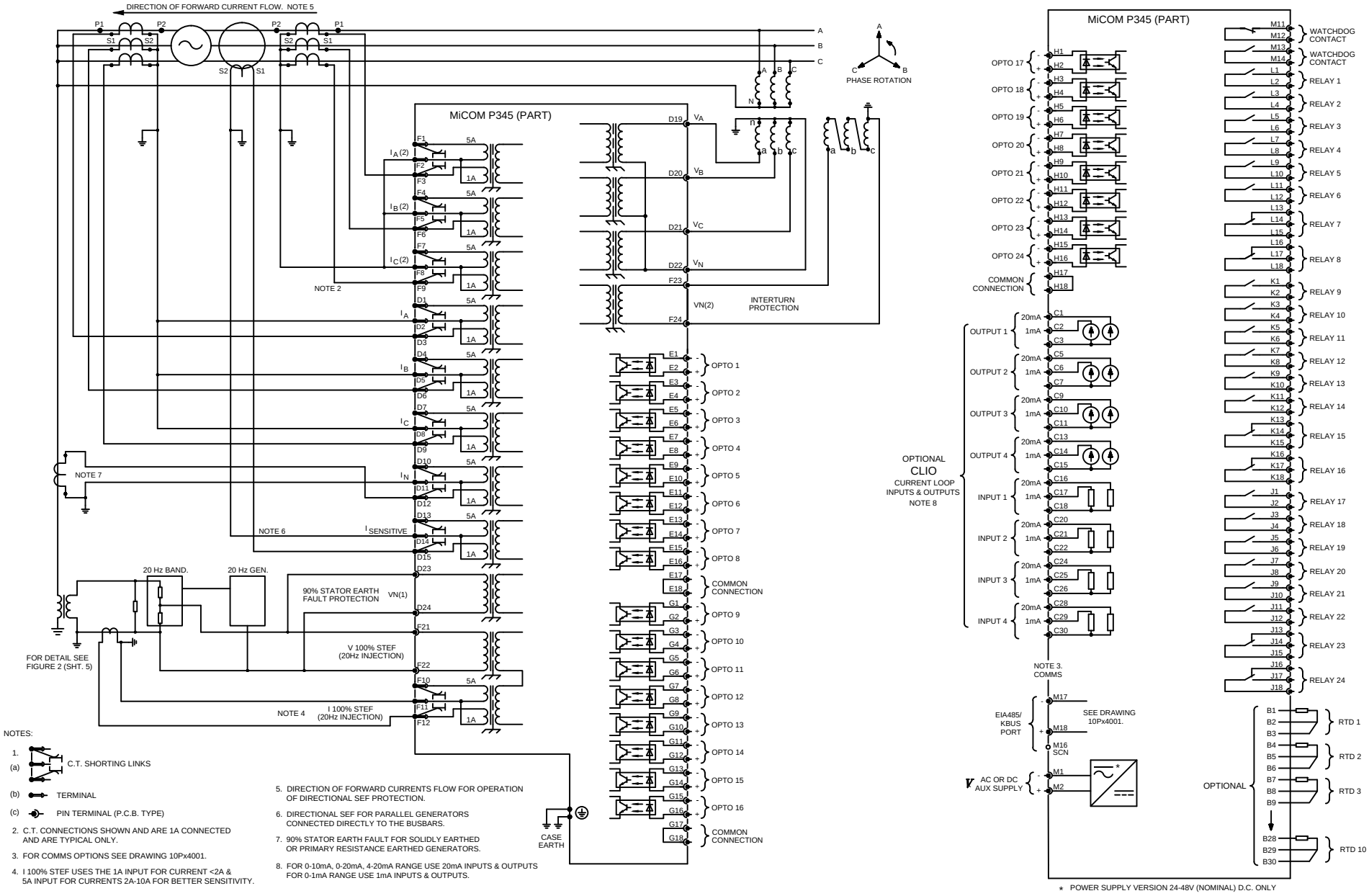
NEXT STAGE :-



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) TERMINAL
   (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. DIRECTION OF FORWARD CURRENTS FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
6. DIRECTIONAL SEF FOR PARALLEL GENERATORS CONNECTED DIRECTLY TO THE BUSBARS.
7. 90% STATOR EARTH FAULT FOR SOLIDLY EARTHED OR PRIMARY RESISTANCE EARTHED GENERATORS.
8. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

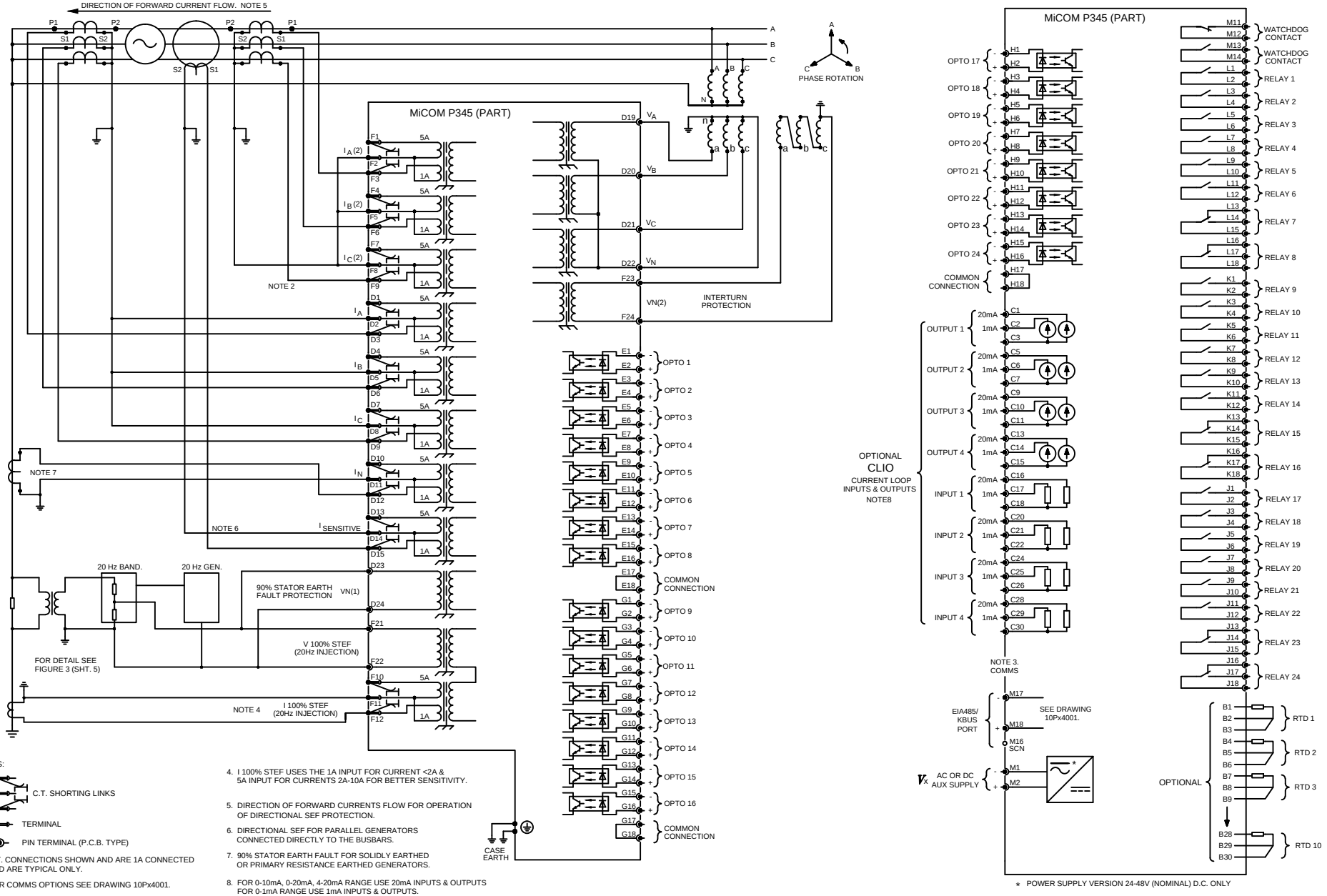
Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONN DIAG: GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3rd HARMONIC) STATOR E/F & INTERTURN PROT. (24 I/P & 24 O/P + CLIO & RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34501	Sht: 1
Date:	Chkd:				Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) TERMINAL
   (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. DIRECTION OF FORWARD CURRENTS FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
6. DIRECTIONAL SEF FOR PARALLEL GENERATORS CONNECTED DIRECTLY TO THE BUSBARS.
7. 90% STATOR EARTH FAULT FOR SOLIDLY EARTHED OR PRIMARY RESISTANCE EARTHED GENERATORS.
8. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONN. DIAG: GENERATOR PROT. RELAY (80TE) WITH 100% STATOR EARTH FAULT PROT. VIA NEUTRAL EARTHING TRANS. WITH SECONDARY LOADING RESISTOR (24 I/P & 24 O/P + CLIO & RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34501	Sht: 3
Date:	Chkd:				Next Sht: 4



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) TERMINAL
   (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. DIRECTION OF FORWARD CURRENTS FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
6. DIRECTIONAL SEF FOR PARALLEL GENERATORS CONNECTED DIRECTLY TO THE BUSBARS.
7. 90% STATOR EARTH FAULT FOR SOLIDLY EARTHED OR PRIMARY RESISTANCE EARTHED GENERATORS.
8. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: E	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONN. DIAG: GENERATOR PROT. RELAY (80TE) WITH 100% STATOR EARTH FAULT PROT. VIA NEUTRAL EARTHING TRANS. WITH PRIMARY LOADING RESISTOR (24 I/P & 24 O/P + CLIO & RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34501	Sht: 4
Date:	Chkd:				Next Sht: 5

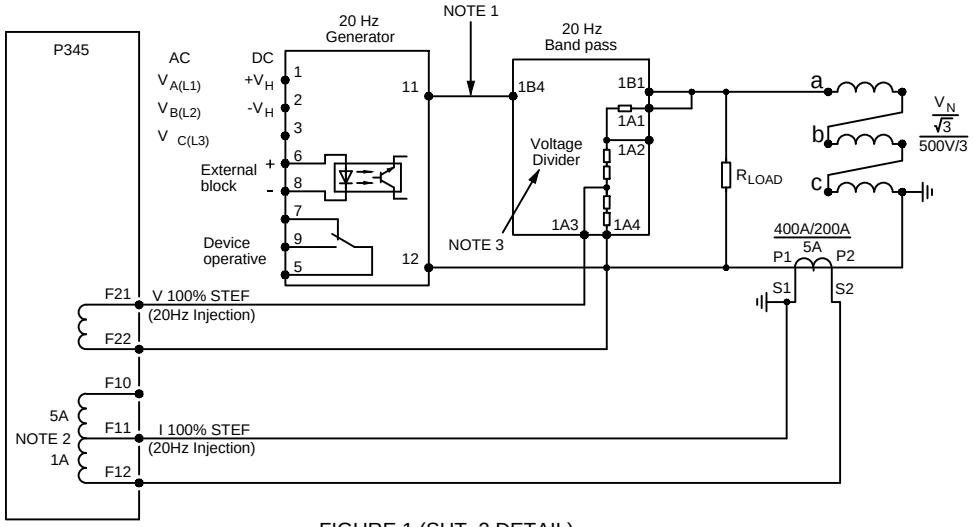


FIGURE 1 (SHT. 2 DETAIL)

100% STATOR EARTH FAULT PROTECTION (20Hz INJECTION) VIA TERMINAL EARTHING TRANSFORMER BROKEN DELTA WITH SECONDARY LOADING RESISTOR

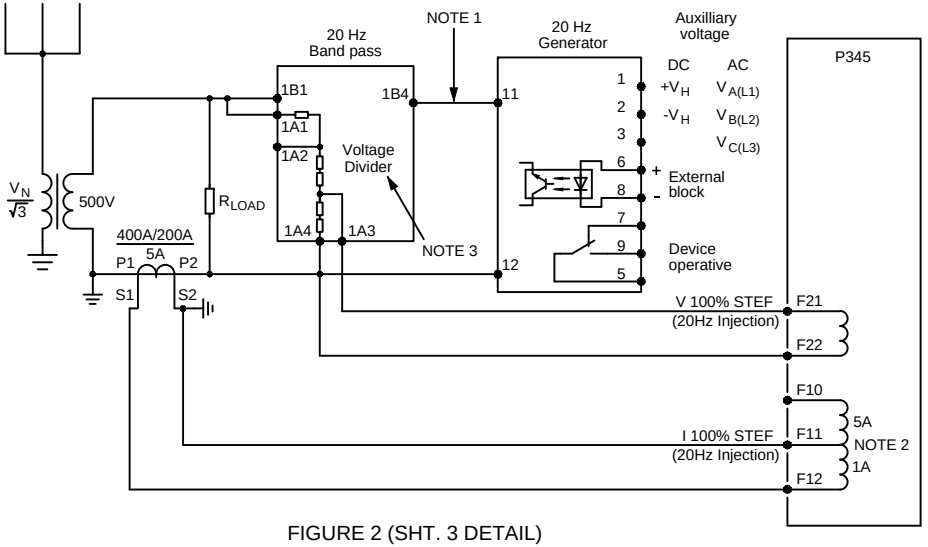


FIGURE 2 (SHT. 3 DETAIL)

100% STATOR EARTH FAULT PROTECTION (20Hz INJECTION) VIA NEUTRAL EARTHING TRANSFORMER DELTA WITH SECONDARY LOADING RESISTOR

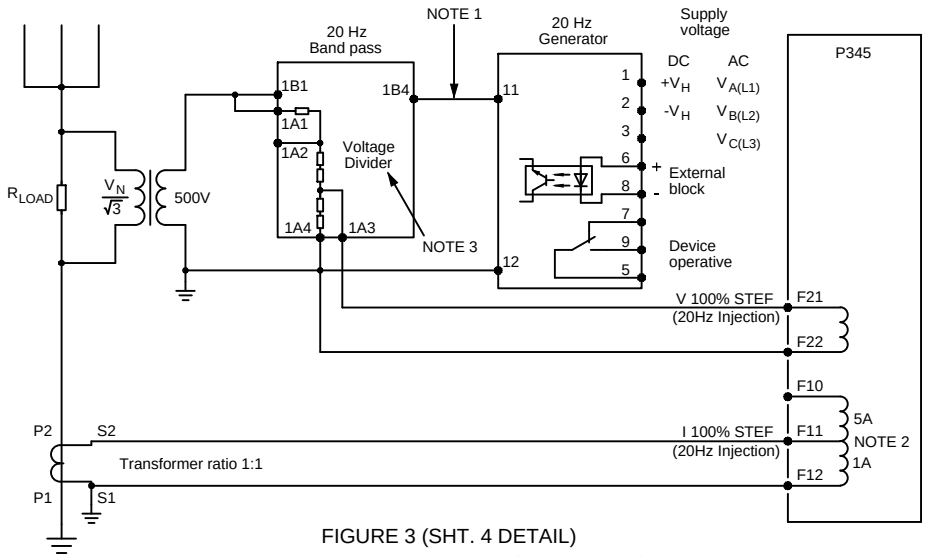


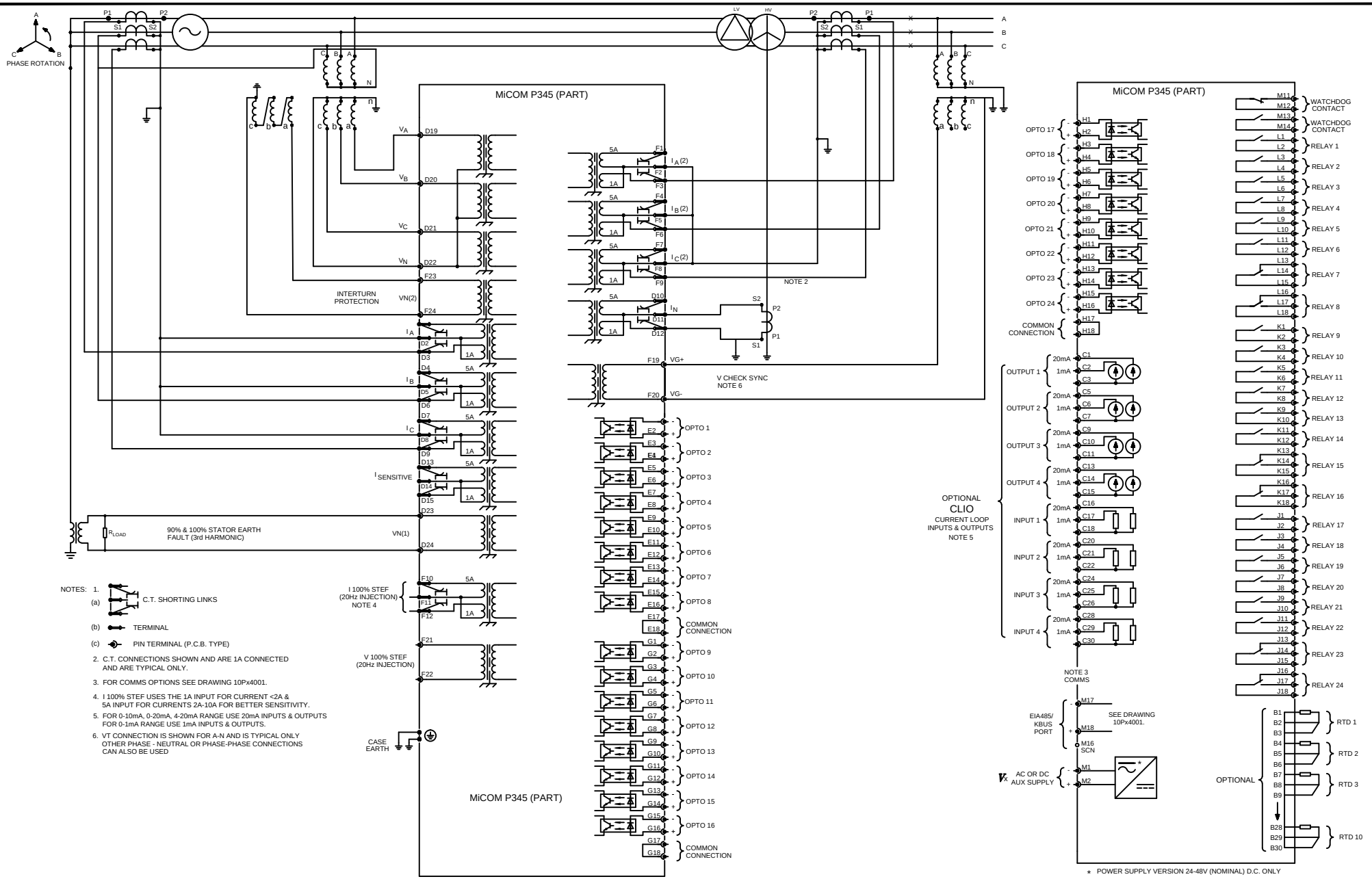
FIGURE 3 (SHT. 4 DETAIL)

100% STATOR EARTH FAULT PROTECTION (20Hz INJECTION) VIA NEUTRAL EARTHING TRANSFORMER WITH PRIMARY LOADING RESISTOR

NOTES

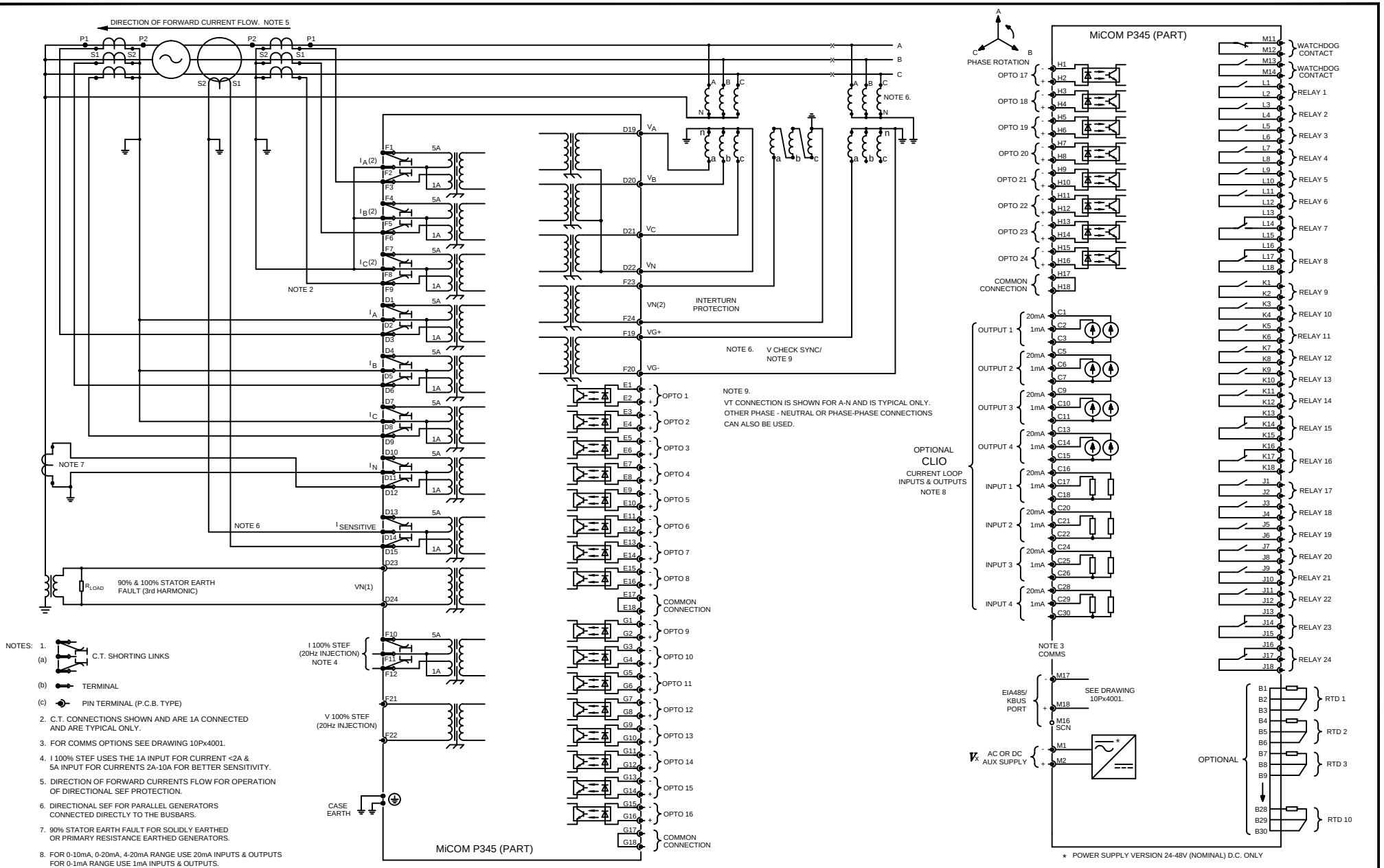
1. WIRING BETWEEN GENERATOR & BANDPASS FILTER TO BE SHIELDED IF IN DIFFERENT PANELS
2. FOR CURRENTS <2A USE 1A INPUTS & FOR CURRENTS 2A-10A USE 5A INPUTS
3. EACH OF THE 5 RESISTORS IN THE VOLTAGE DIVIDER (500V/200V) CIRCUIT = 330 OHMS 80 WATTS

Issue: D.1	Revision: CheckedOut for Editing			Title: EXTERNAL CONN. DIAG: GENERATOR PROTECTION RELAY (80TE) 100% STATOR EARTH FAULT (24 I/P & 24 O/P + CLIO & RTD)	
Date: 17/02/2014	Name: P.WIGGIN	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34501	Sht: 5
Date:	Chkd:				Next Sht: 6

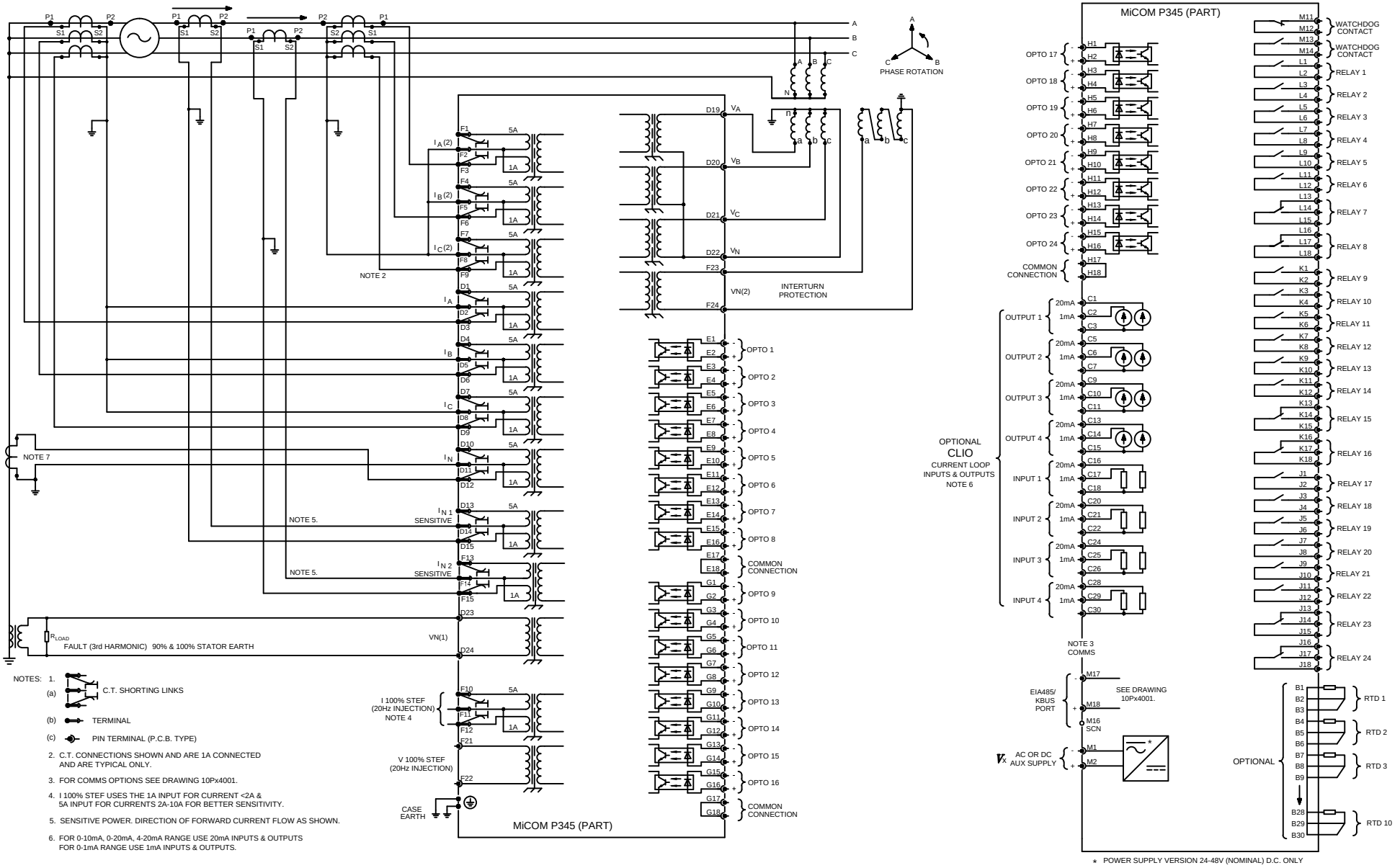


NOTES:
1. (a) C.T. SHORTING LINKS; (b) TERMINAL; (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.
6. VT CONNECTION IS SHOWN FOR A-N AND IS TYPICAL ONLY OTHER PHASE - NEUTRAL OR PHASE-PHASE CONNECTIONS CAN ALSO BE USED

Issue: H	Revision: CID PWIG-8KMJ2K			Title: EXT. CONN DIAGRAM: GEN TRANSF PROT RELAY (80TE) WITH 90% & 100% (3rd HRM) STR EARTH FAULT & INTERTURN PROT.(24 I/P & 24 O/P + CLIO & RTD)	
Date: 05/03/2014	Name: P.WIGGIN	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34501	Sht: 10
Date: 05/03/2014	Chkd: G.LLOYD				Next Sht: 11



Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3RD HRM) STR EARTH FAULT, INTERTURN PROT & V CHK SYNC 24I/P & 24O/P + CLIO & RTD	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34501	Sht: 11
Date:	Chkd:				Next Sht: -



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) TERMINAL
   (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. SENSITIVE POWER. DIRECTION OF FORWARD CURRENT FLOW AS SHOWN.
6. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: C	Revision: CID- RPAL-9Q4J8U-IN2 SENSITIVE INPUTS IS CHANGED FROM TERMINAL D TO F.			Title: EXT.CONN DIAG:GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3RD HARMONIC) STATOR E/F & WATTMETRIC POWER. 24 I/P & 24 O/P + CLIO & RTD	
Date: 17/11/2014	Name: R.PALANISAMY	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34501	Sht: 13
Date: 05/03/2014	Chkd: G.LIOYD				Next Sht: -

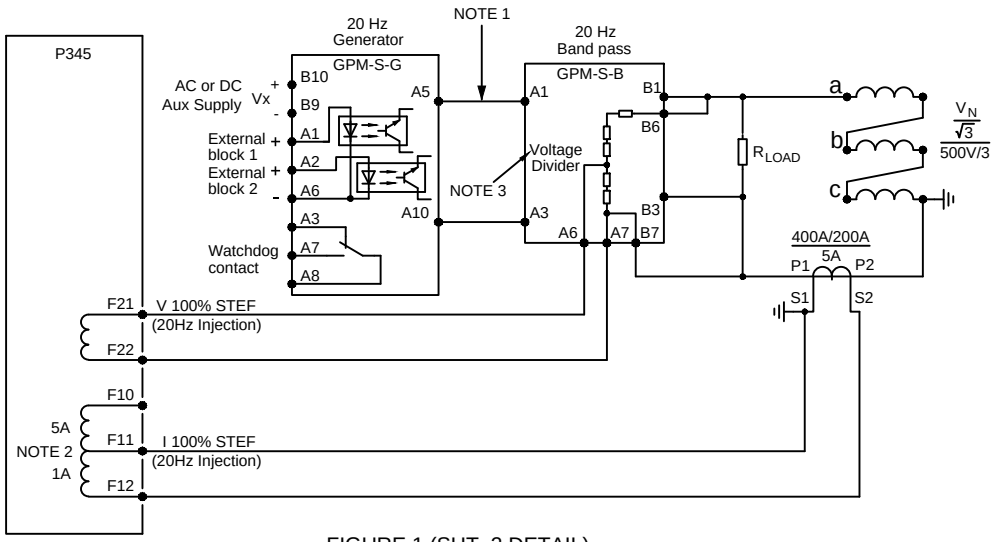


FIGURE 1 (SHT. 2 DETAIL)

100% STATOR EARTH FAULT PROTECTION (20Hz INJECTION) VIA TERMINAL EARTHING TRANSFORMER BROKEN DELTA WITH SECONDARY LOADING RESISTOR

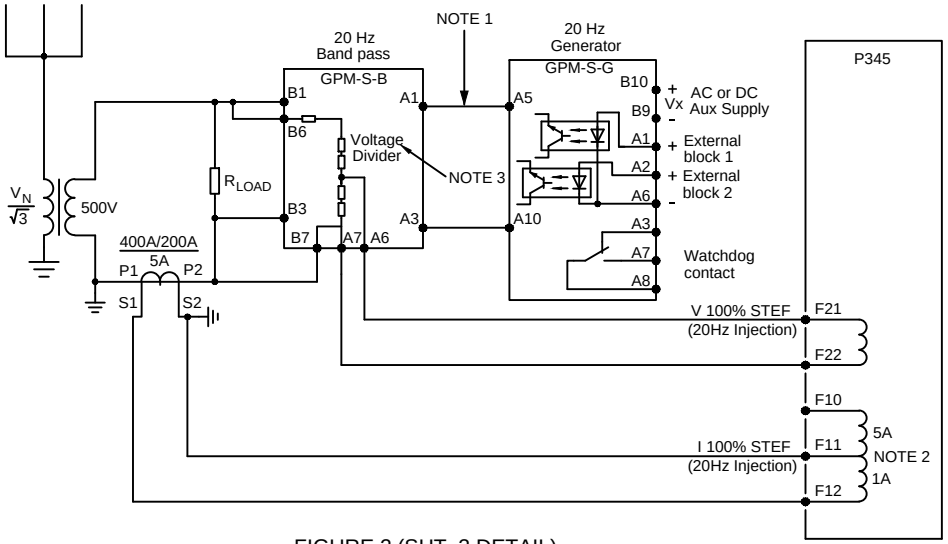


FIGURE 2 (SHT. 3 DETAIL)

100% STATOR EARTH FAULT PROTECTION (20Hz INJECTION) VIA NEUTRAL EARTHING TRANSFORMER DELTA WITH SECONDARY LOADING RESISTOR

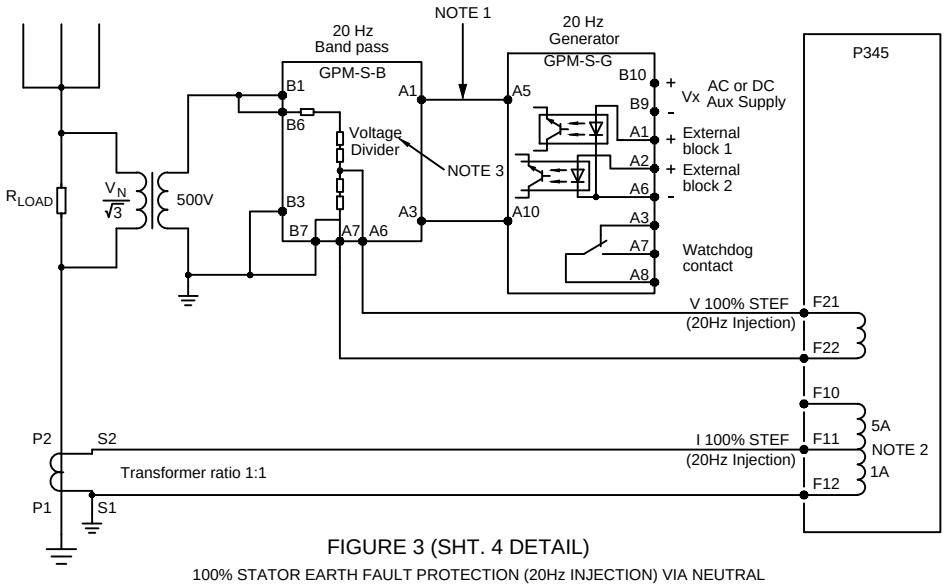


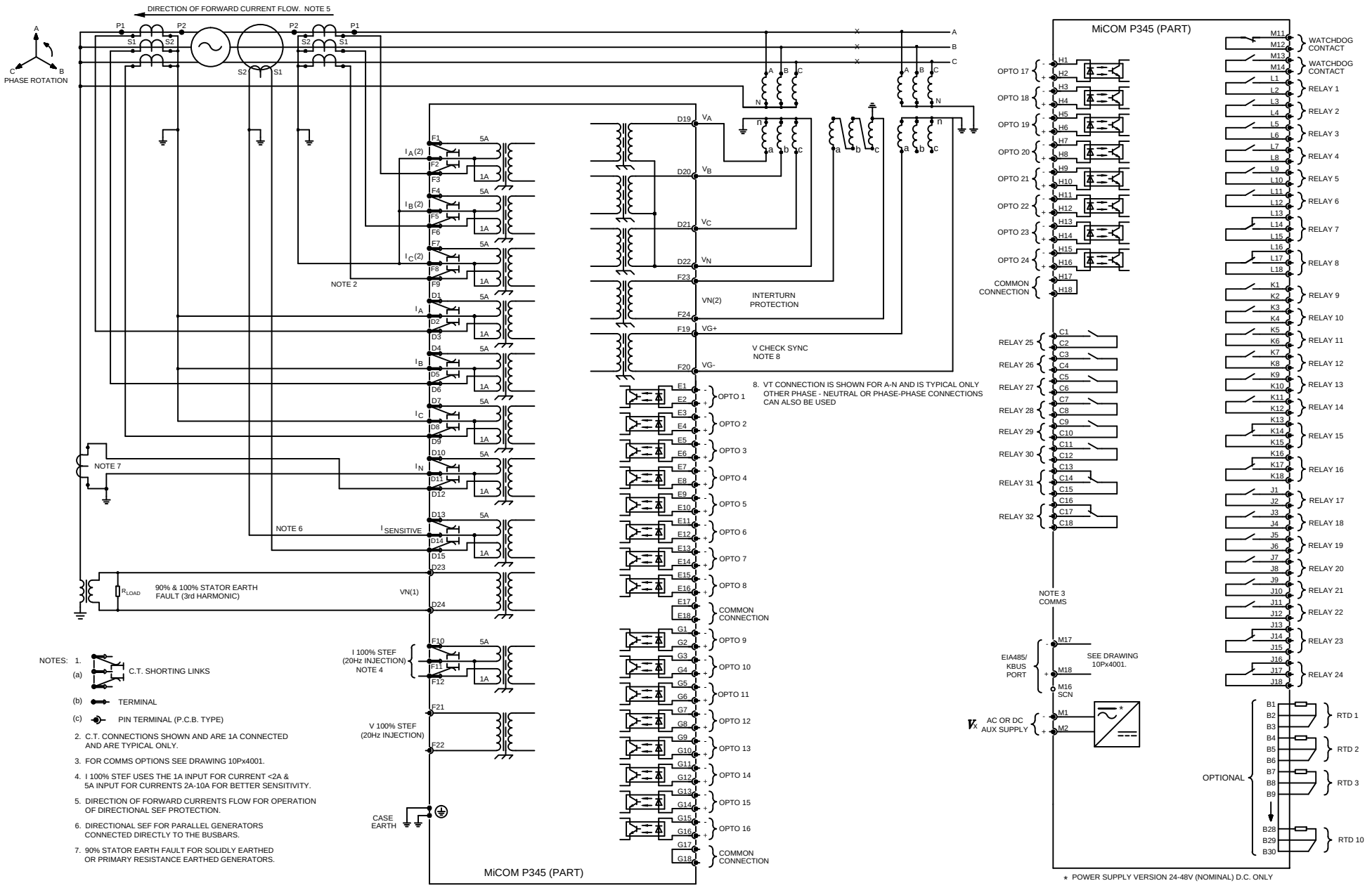
FIGURE 3 (SHT. 4 DETAIL)

100% STATOR EARTH FAULT PROTECTION (20Hz INJECTION) VIA NEUTRAL EARTHING TRANSFORMER WITH PRIMARY LOADING RESISTOR

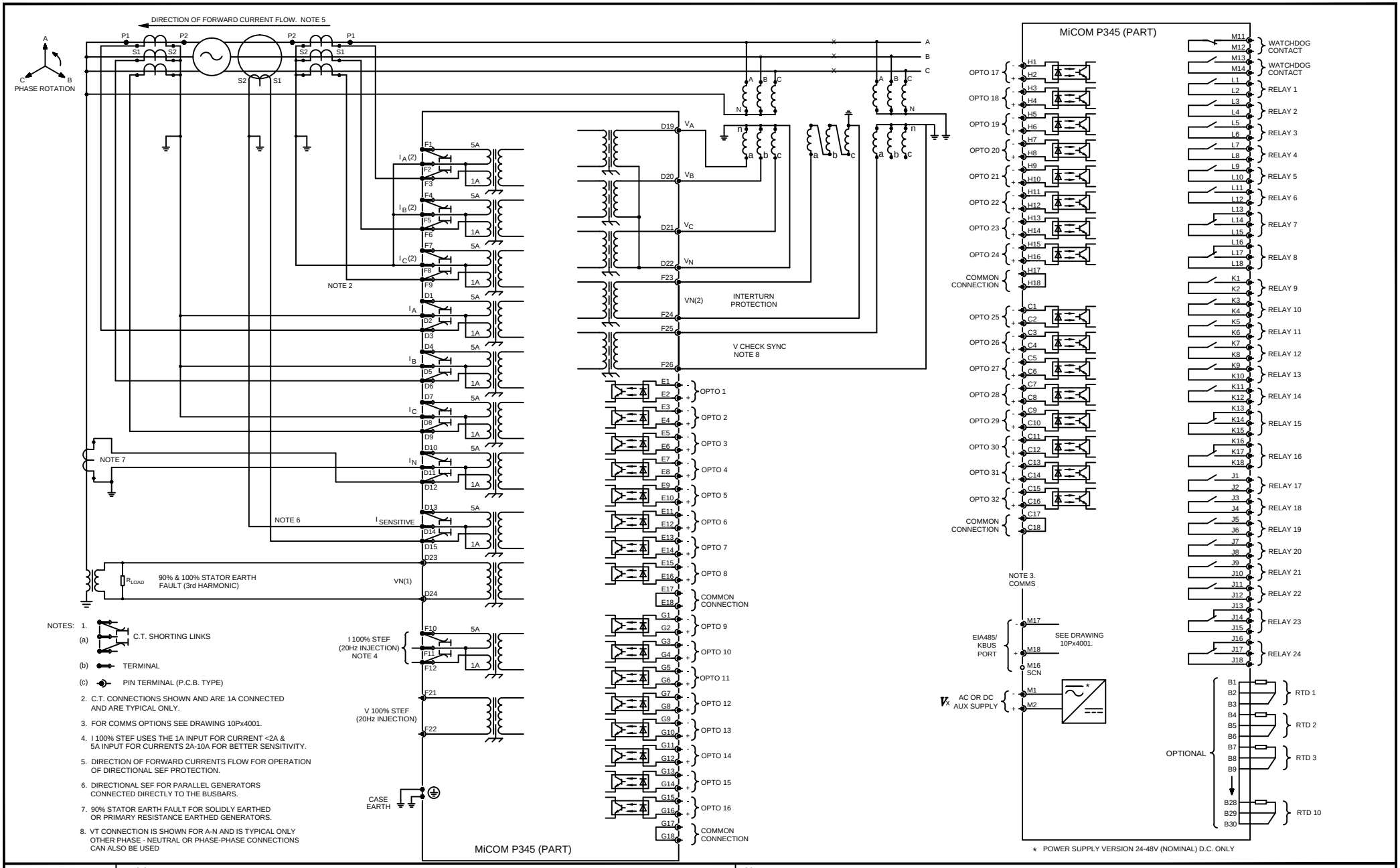
NOTES

1. WIRING BETWEEN GENERATOR & BANDPASS FILTER TO BE SHIELDED IF IN DIFFERENT PANELS
2. FOR CURRENTS <2A USE 1A INPUTS & FOR CURRENTS 2A-10A USE 5A INPUTS
3. EACH OF THE 5 RESISTORS IN THE VOLTAGE DIVIDER (500V/200V) CIRCUIT = 330 OHMS 50 WATTS
4. FAULTS SHOULD BE CLEARED WITHIN 10 SECONDS TO AVOID DAMAGE TO THE DIVIDER INPUT OF THE GPM-S-B

Issue: B	Revision: CID SWOO-AFABXA. INITIAL ISSUE			Title:	EXTERNAL CONN.DIAG: GENERATOR PROTECTION RELAY (80TE) 100% STATOR E/F WITH GPM-S (24 I/P & 24 O/P + CLIO & RTD)
Date: 18/01/2018	Name: S.WOOTTON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No:	10P34501
Date:	Chkd: G. LLOYD			Sht: 14	Next Sht: -



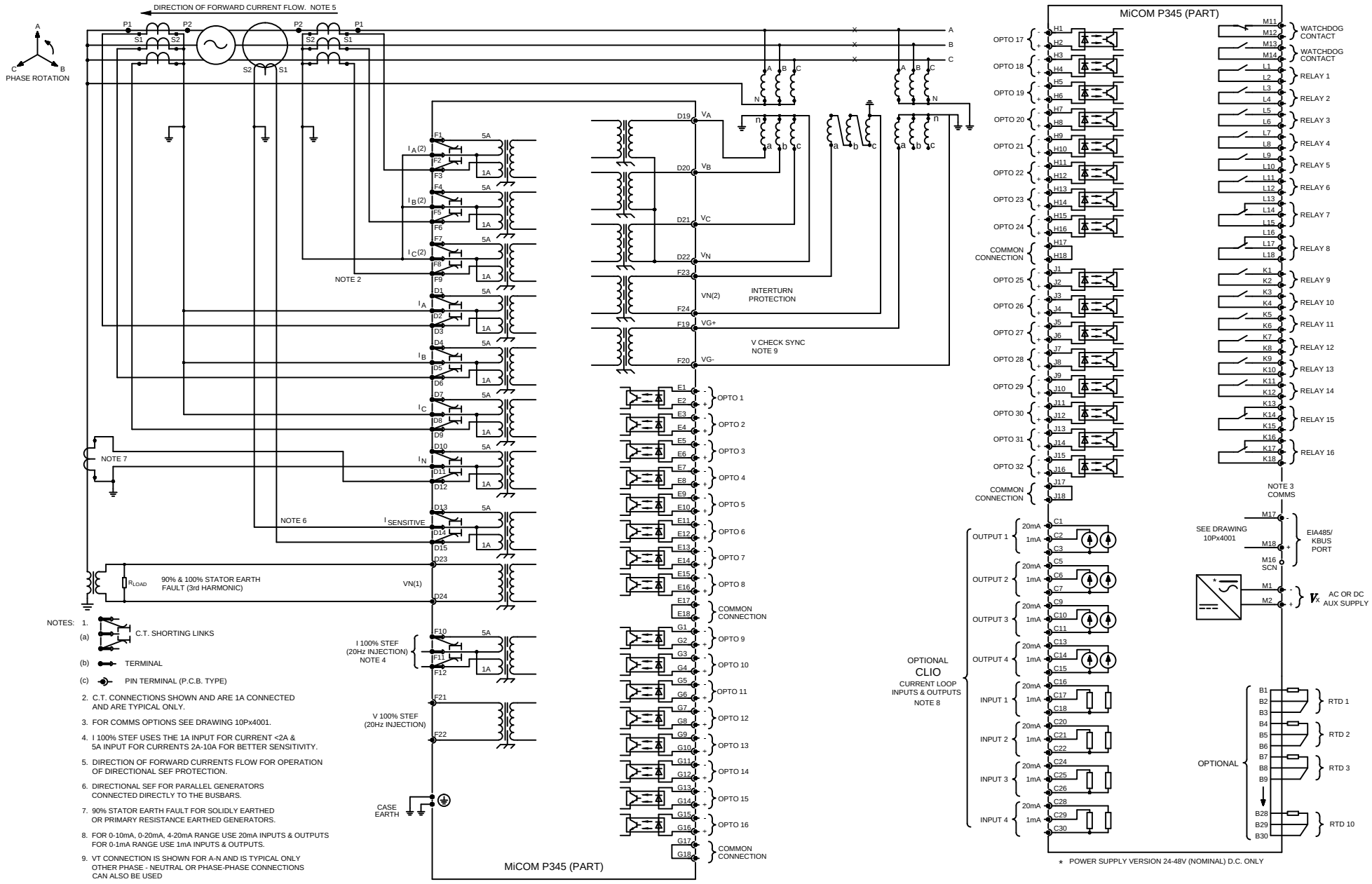
Issue: G	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONN. DIAGRAM: GENERATOR PROTECTION RELAY (80TE) WITH 90% & 100% (3rd HARMONIC) STATOR EARTH FAULT & INTERTURN PROT. (24 I/P & 32 O/P + RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34502	Sht: 1
Date:	Chkd:				Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) TERMINAL
   (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. DIRECTION OF FORWARD CURRENTS FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
6. DIRECTIONAL SEF FOR PARALLEL GENERATORS CONNECTED DIRECTLY TO THE BUSBARS.
7. 90% STATOR EARTH FAULT FOR SOLIDLY EARTHED OR PRIMARY RESISTANCE EARTHED GENERATORS.
8. VT CONNECTION IS SHOWN FOR A-N AND IS TYPICAL ONLY OTHER PHASE - NEUTRAL OR PHASE-PHASE CONNECTIONS CAN ALSO BE USED

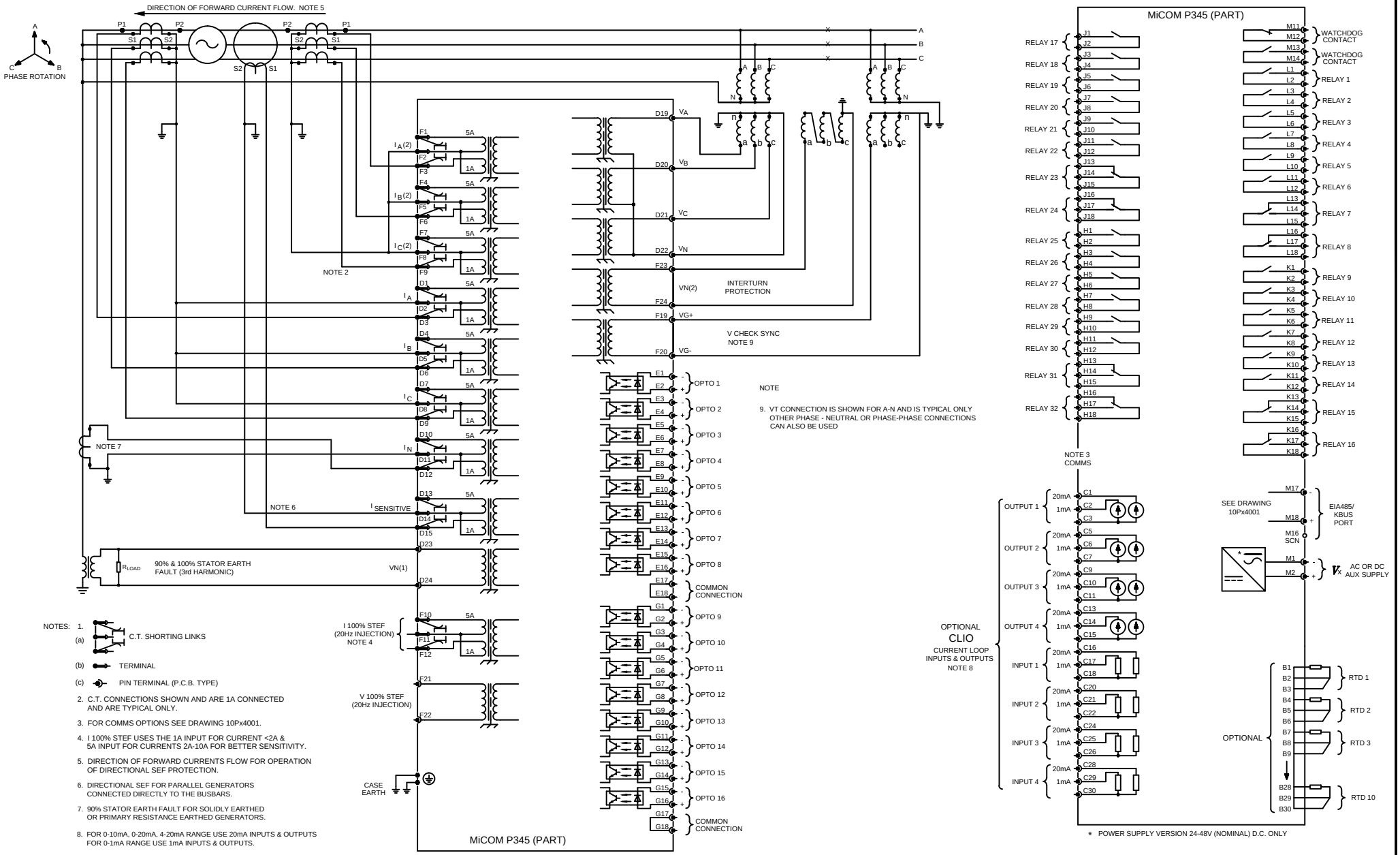
Issue: F	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title:	EXT. CONN. DIAGRAM: GEN. PROT. RELAY (80TE) + 90% & 100% (3rd HARM) STATOR EARTH FAULT, INTERTURN PROT.& V CHECK SYNC (32 I/P & 24 O/P + RTD)
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34503	Sht: 1
Date:	Chkd:				Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) TERMINAL
   (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. DIRECTION OF FORWARD CURRENTS FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
6. DIRECTIONAL SEF FOR PARALLEL GENERATORS CONNECTED DIRECTLY TO THE BUSBARS.
7. 90% STATOR EARTH FAULT FOR SOLIDLY EARTHED OR PRIMARY RESISTANCE EARTHED GENERATORS.
8. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.
9. VT CONNECTION IS SHOWN FOR A-N AND IS TYPICAL ONLY OTHER PHASE - NEUTRAL OR PHASE-PHASE CONNECTIONS CAN ALSO BE USED

Issue: G	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAGRAM: GEN. PROT. RELAY (80TE) + V CHECK SYNC 90% & 100% (3rd HARMONIC) STATOR EARTH FAULT & INTERTURN PROT. (32 I/P & 16 O/P + CLIO & RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34504	Sht: 1
Date:	Chkd:				Next Sht: 2



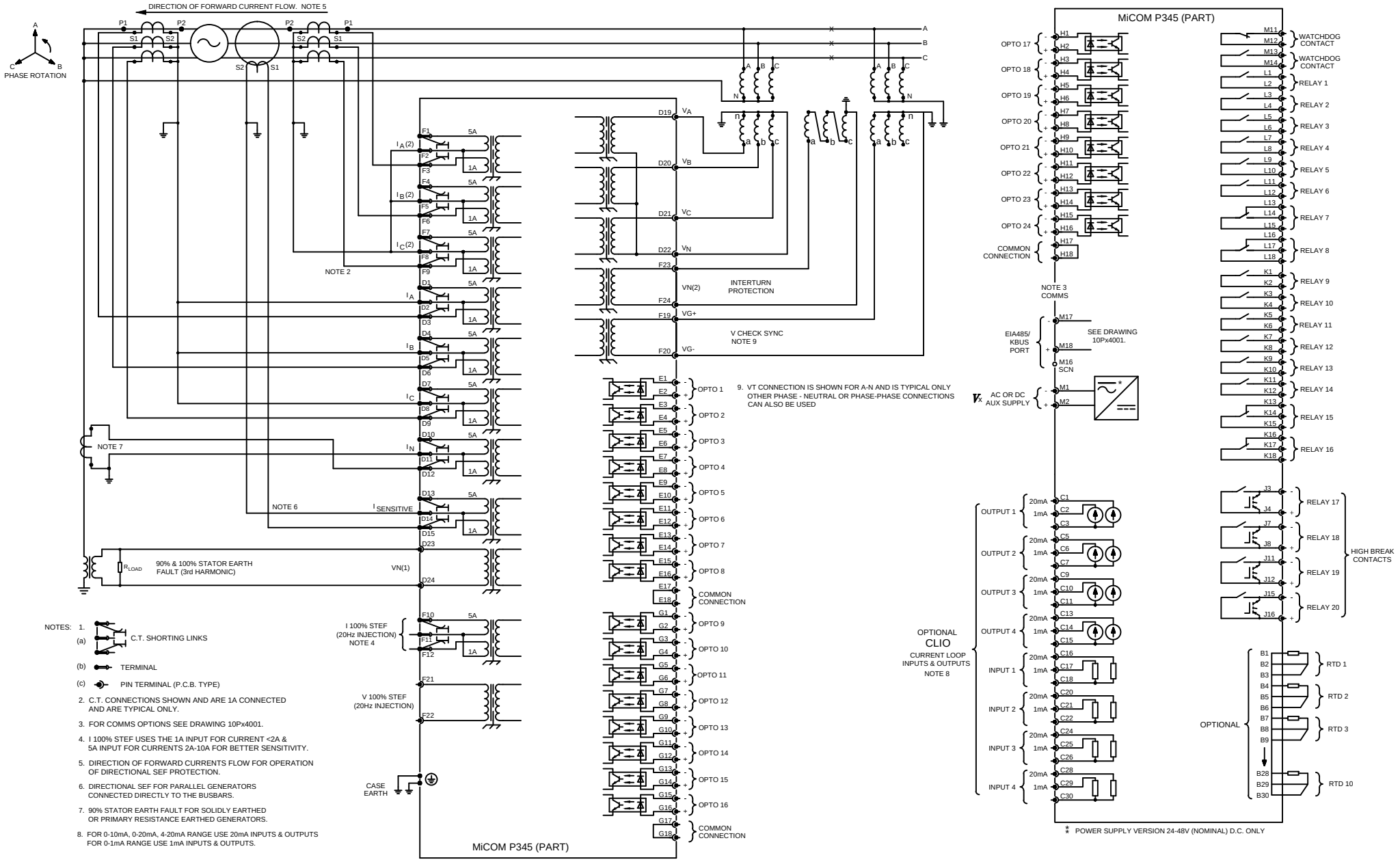
NOTES:

1. (a) C.T. SHORTING LINKS
   (b) TERMINAL
   (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. DIRECTION OF FORWARD CURRENTS FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
6. DIRECTIONAL SEF FOR PARALLEL GENERATORS CONNECTED DIRECTLY TO THE BUSBARS.
7. 90% STATOR EARTH FAULT FOR SOLIDLY EARTHED OR PRIMARY RESISTANCE EARTHED GENERATORS.
8. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

NOTE

9. VT CONNECTION IS SHOWN FOR A-N AND IS TYPICAL ONLY OTHER PHASE - NEUTRAL OR PHASE-PHASE CONNECTIONS CAN ALSO BE USED

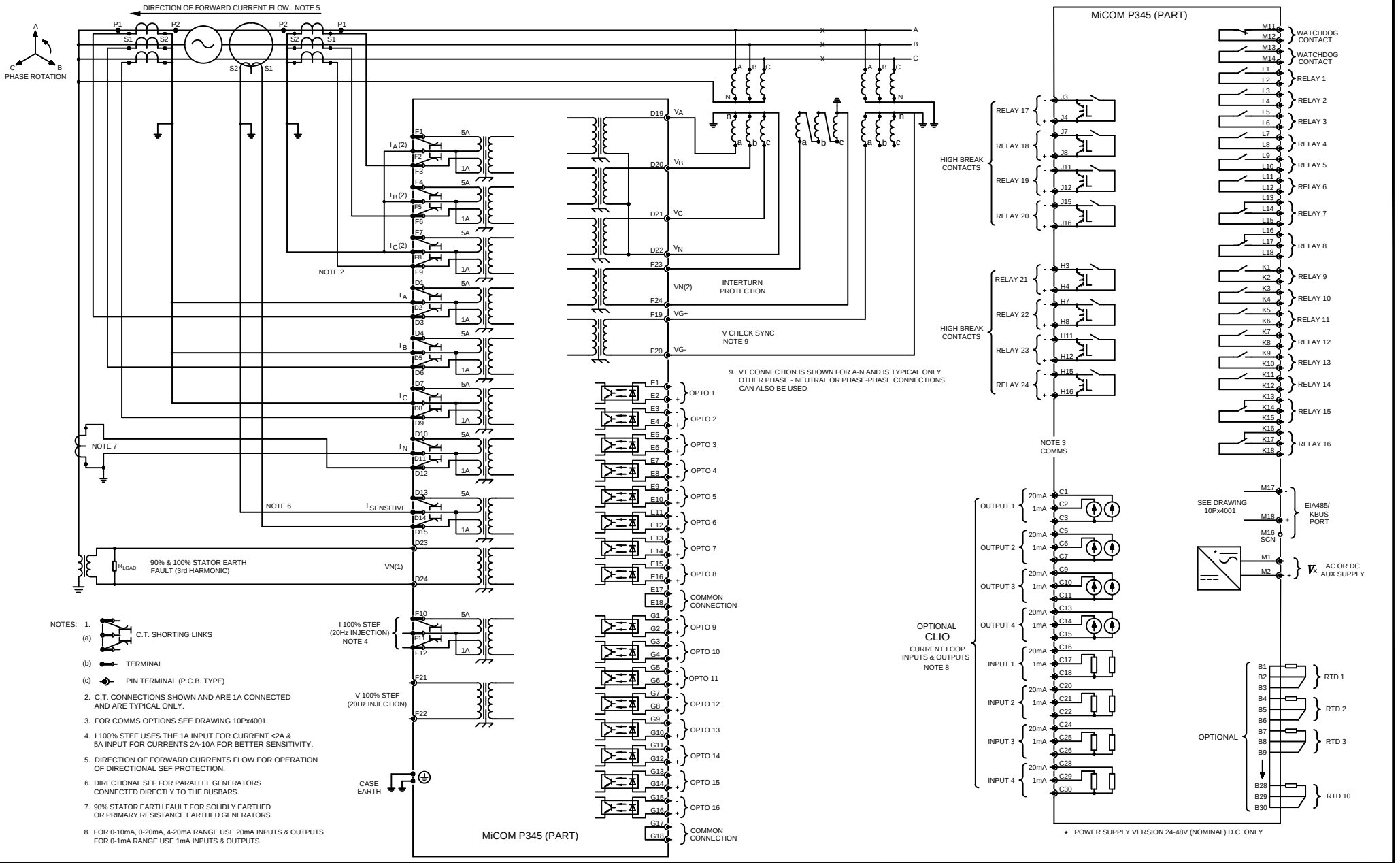
Issue: G	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAGRAM: GEN. PROT. RELAY (80TE) + V CHECK SYNC 90% & 100% (3rd HARMONIC) STATOR EARTH FAULT & INTERTURN PROT. (16 I/P & 32 O/P + CLIO & RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34505	Sht: 1
Date:	Chkd:				Next Sht: 2



NOTES:

1. (a) C.T. SHORTING LINKS
   (b) TERMINAL
   (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. DIRECTION OF FORWARD CURRENTS FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
6. DIRECTIONAL SEF FOR PARALLEL GENERATORS CONNECTED DIRECTLY TO THE BUSBARS.
7. 90% STATOR EARTH FAULT FOR SOLIDLY EARTHED OR PRIMARY RESISTANCE EARTHED GENERATORS.
8. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.
9. VT CONNECTION IS SHOWN FOR A-N AND IS TYPICAL ONLY OTHER PHASE - NEUTRAL OR PHASE-PHASE CONNECTIONS CAN ALSO BE USED

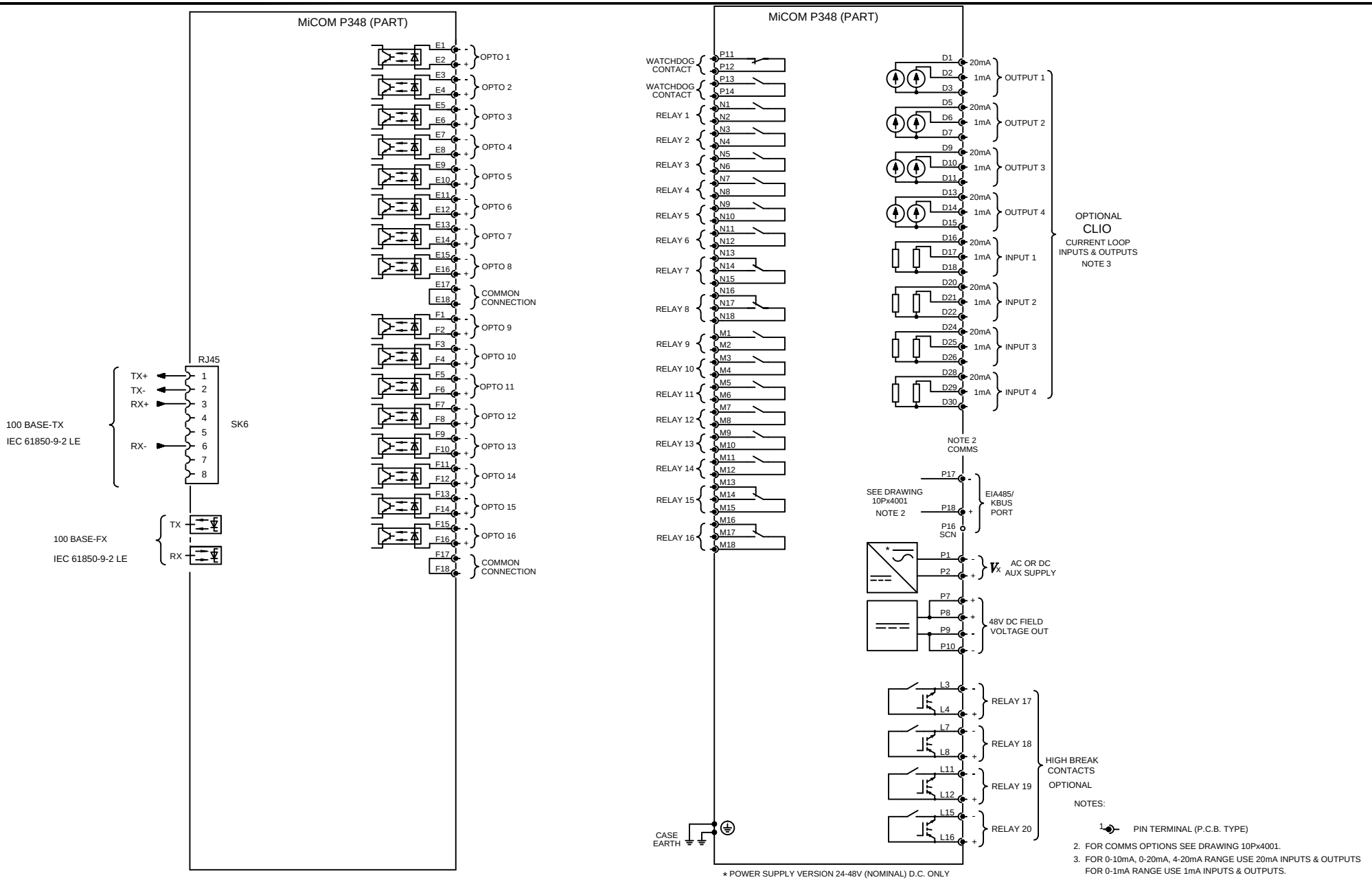
Issue: G	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAGRAM: GEN. PROT. RELAY (80TE) + V CHECK SYNC 90% & 100% (3rd HARMONIC) STATOR EARTH FAULT & INTERTURN PROT. (24 I/P & 20 O/P + CLIO & RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34506	Sht: 1
Date:	Chkd:				Next Sht: 2



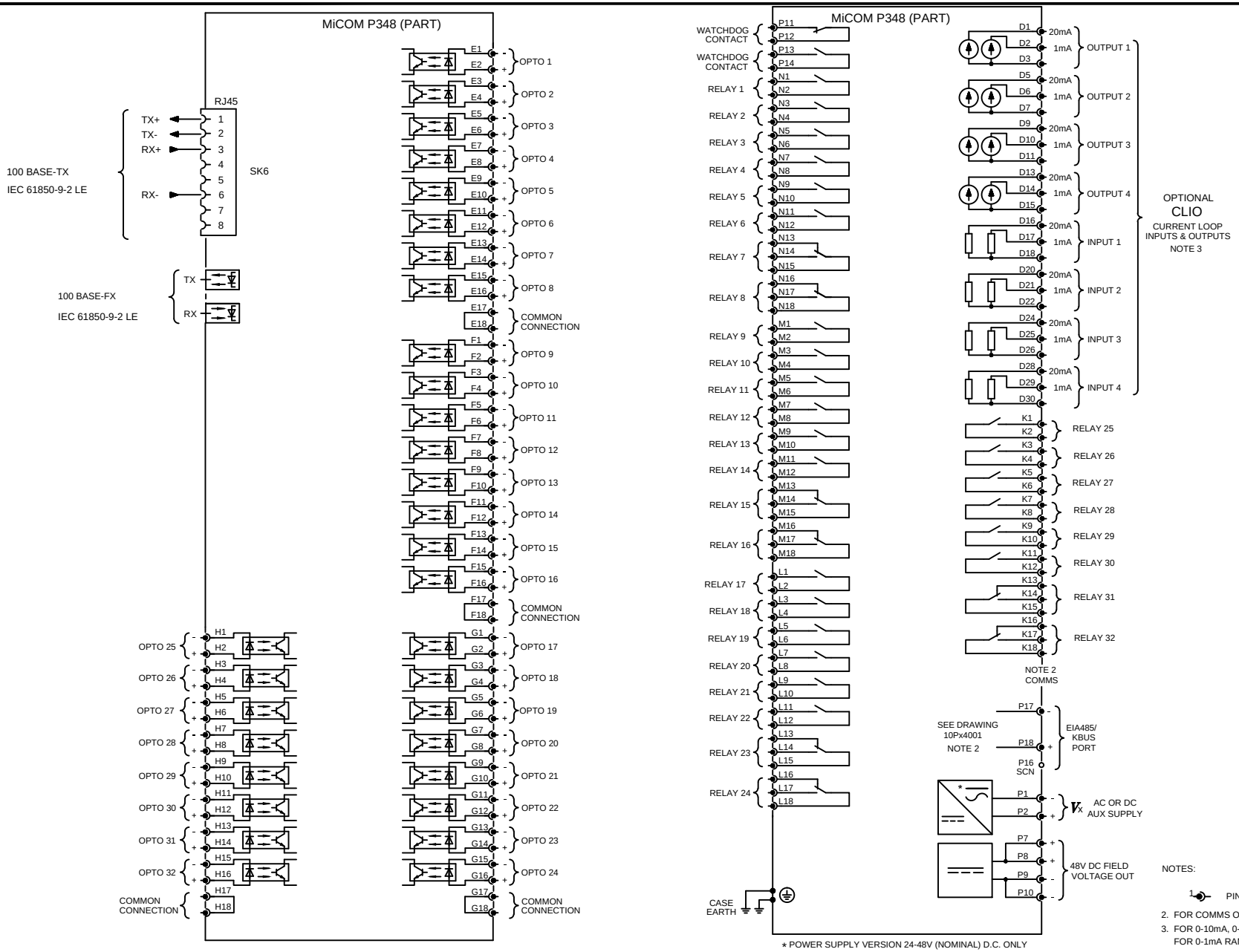
NOTES:

1. (a) C.T. SHORTING LINKS
   (b) TERMINAL
   (c) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS SHOWN AND ARE 1A CONNECTED AND ARE TYPICAL ONLY.
3. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
4. I 100% STEF USES THE 1A INPUT FOR CURRENT <2A & 5A INPUT FOR CURRENTS 2A-10A FOR BETTER SENSITIVITY.
5. DIRECTION OF FORWARD CURRENTS FLOW FOR OPERATION OF DIRECTIONAL SEF PROTECTION.
6. DIRECTIONAL SEF FOR PARALLEL GENERATORS CONNECTED DIRECTLY TO THE BUSBARS.
7. 90% STATOR EARTH FAULT FOR SOLIDLY EARTHED OR PRIMARY RESISTANCE EARTHED GENERATORS.
8. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

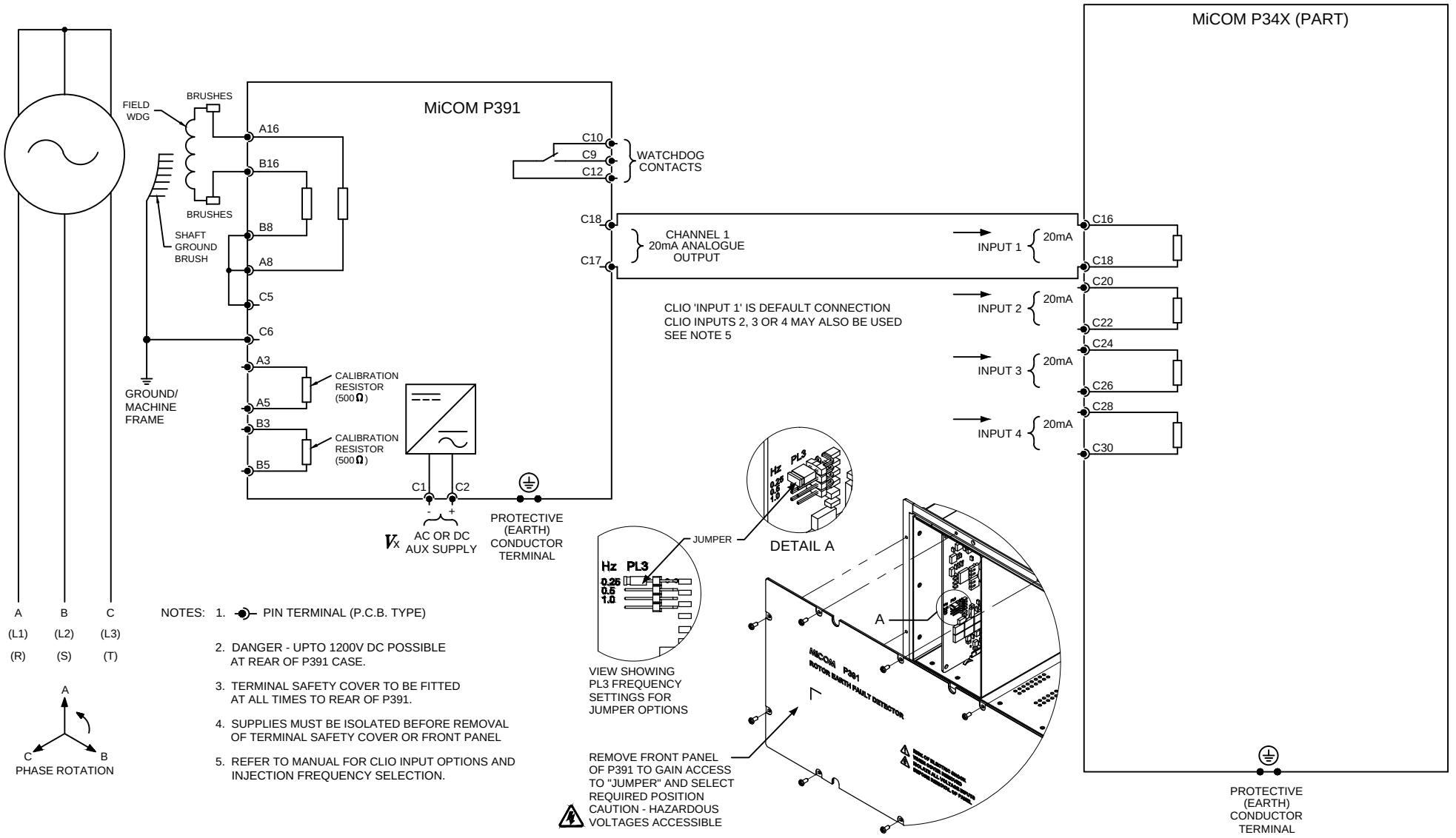
Issue: G	Revision: FIELD VOLTAGE OUTPUT REMOVED. CID HONG-98JC6A.			Title: EXT. CONNECTION DIAGRAM: GEN. PROT. RELAY (80TE) + V CHECK SYNC 90% & 100% (3rd HARMONIC) STATOR EARTH FAULT & INTERTURN PROT. (16 I/P & 24 O/P + CLIO & RTD)	
Date: 27/06/2013	Name: N.JOHNSON	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34507	Sht: 1
Date: 17/03/2012	Chkd: G.LLOYD				Next Sht: 2



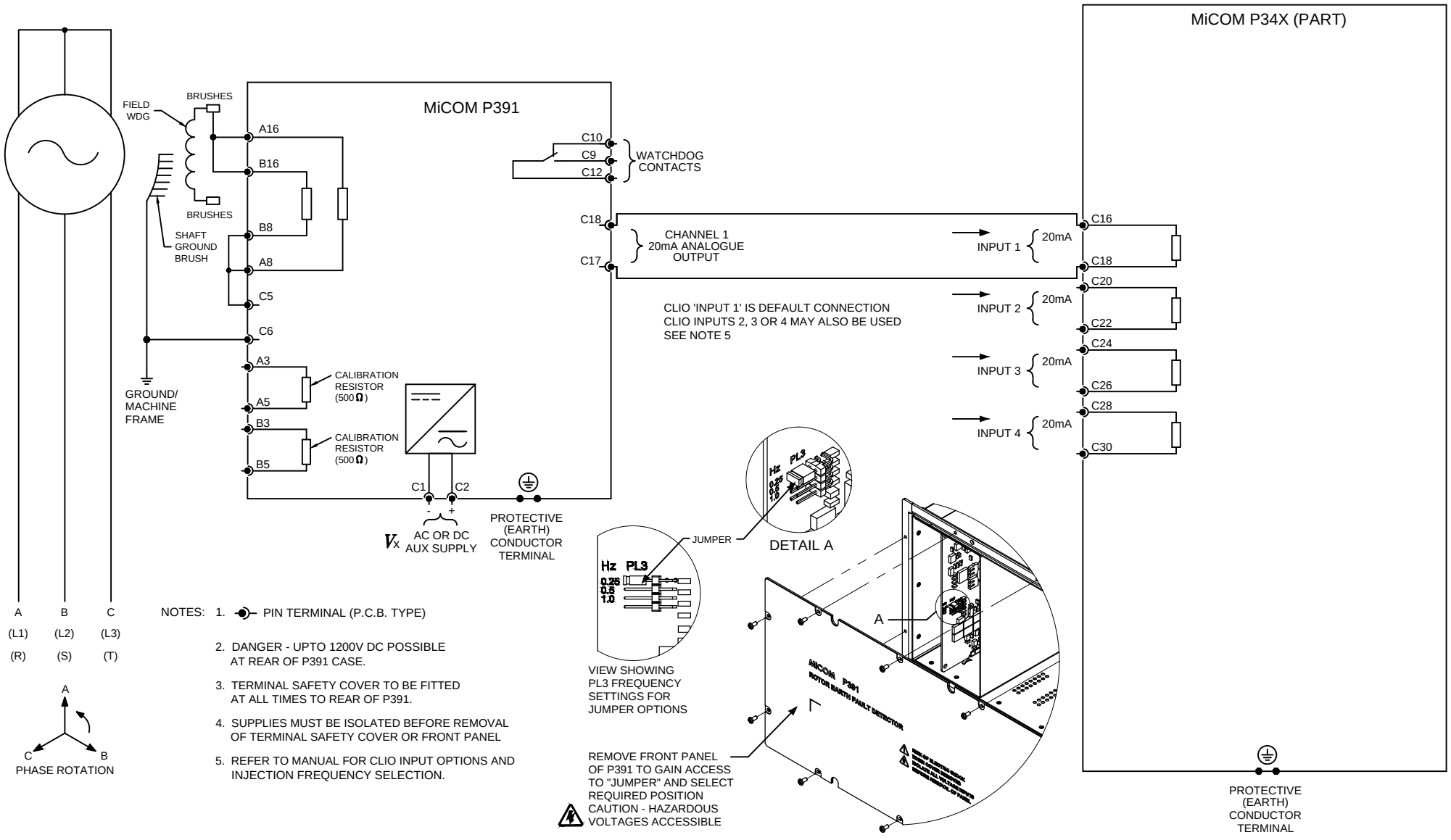
Issue: D	Revision: CID-RPAL-9Q4KLG- VARIOUS CHANGES REFER CID.			Title: EXT. CONN DIAG : VARSPEED PROTECTION 16 I/P & 16 O/P + CLIO 80TE	
Date: 17/11/2014	Name: R.PALANISAMY	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P34801	Sht: 1
Date: 10/13/2014	Chkd: H.SHAH				Next Sht: -



Issue: B	Revision: CID PWIG-959DV4			Title: EXT.CONN DIAG : VARSPEED PROTECTION 32 I/P & 32 O/P + CLIO	
Date: 17/03/2014	Name: P.WIGGIN	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: **10P34802**	Sht: 1
Date: 10/03/2014	Chkd: H.SHAH				Next Sht: -



Issue: D	Revision: DRAWING OUTLINE UPDATED. CID BLIN-8BHLDT			Title: EXT. CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY ROTOR EARTH FAULT PROTECTION DOUBLE ENDED CONNECTION	
Date: 29/11/2010	Name: W.LINTERN	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P39101	Sht: 1
Date:	Chkd:				Next Sht: -



NOTES:
1. PIN TERMINAL (P.C.B. TYPE)
2. DANGER - UPTO 1200V DC POSSIBLE AT REAR OF P391 CASE.
3. TERMINAL SAFETY COVER TO BE FITTED AT ALL TIMES TO REAR OF P391.
4. SUPPLIES MUST BE ISOLATED BEFORE REMOVAL OF TERMINAL SAFETY COVER OR FRONT PANEL
5. REFER TO MANUAL FOR CLIO INPUT OPTIONS AND INJECTION FREQUENCY SELECTION.

Issue: D	Revision: DRAWING OUTLINE UPDATED. CID BLIN-8BHLDT			Title: EXT. CONNECTION DIAGRAM: GENERATOR PROTECTION RELAY ROTOR EARTH FAULT PROTECTION SINGLE ENDED CONNECTION	
Date: 29/11/2010	Name: W.LINTERN	CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE	ALSTOM GRID UK LTD Substation Automation Solutions (STAFFORD)	Drg No: 10P39102	Sht: 1
Date:	Chkd:				Next Sht: -

FIRMWARE AND SERVICE MANUAL VERSION HISTORY

Hardware Suffix:	**P (P342) M (P343/4/5/6/8)** **A (P391)**
Software Version:	**38 (P342/3/4/5/6)** **37 (P348)**

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
01	A	A	Oct 1999	Original Issue	V1.09 or Later	TG8614A
	B	A	Dec 1999	✓ Corrected 90 degree phase angle displacement in measurement of Ia, Ib, Ic ✓ Corrected RTD temperature and invalid system frequency measurements in MODBUS fault records ✓ Corrected VT scaling factors for Va, Vb, Vc in fault records ✓ Minor bug fixes	V1.09 or Later	TG8614A
	C	A	Mar 2000	✓ Trip LED status saved during power cycling ✓ Corrections to omission of fault duration and CB operating time in fault record ✓ Corrected -90 degree phase angle displacement in measurement of VN and VN derived ✓ Reset of alarms and indications event added to event record ✓ Minor bug fixes	V1.09 or Later	TG8614A
02	A	A	Oct 2000	✓ DNP 3.0 protocol added ✓ Courier and MODBUS enhancements to improve compatibility with other protection (mainly PX20 products) ✓ Modifications to IEC60870-5-103 Test Mode ✓ Poledead logic DDB signals made visible in PSL ✓ Foreign Language text updated ✓ Active and reactive power added to MODBUS fault record ✓ Minor bug fixes	V1.10 or Later	TG8614B

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
03	A	A	Jan 2001	✓ Event filtering added ✓ Correction to energy measurement inaccuracy ✓ Minor bug fixes	V2.00 or Later	TG8614B
	B	A	May 2001	✓ Correction to NPS Alarm operation ✓ Minor bug fixes	V2.00 or Later	TG8614B
	C	A	Jan 2002	✓ Resolved possible reboot caused by Disturbance Recorder ✓ Minor bug fixes	V2.00 or Later	TG8614B
	D	A	Feb 2002	✓ Resolved possible reboot caused by invalid MODBUS requests ✓ Minor bug fixes	V2.00 or Later	TG8614B
	E	A	Dec 2002	✓ DNP 3.0 Object 12 “CROB” implementation is now compliant for simple function points ✓ DNP 3.0 Object 10 included in Class 0 poll ✓ DNP 3.0 support for season in time information ✓ Correction to MODBUS CB Trip and Close via "0" command ✓ Change to neutral voltage displacement protection and directional SEF protection so that they are not blocked by the VT supervision logic when the VN Input and ISEF>VNPol are selected as Measured ✓ Correction to undervoltage stage 2 (V<2) setting range. The setting range has been increased from 10-70V to 10-120V (Vn=110/120V) so that it is the same as V<1 ✓ Correction to VT ratio scaling problem in the disturbance recorder ✓ Improvement to the RTD start-up calibration routine ✓ Minor bug fixes	V2.00 or Later	TG8614B

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
03 Cont.	F	A	Mar 2004	✓ Improvement to the differential protection performance at low frequencies ✓ Correction to the fault recorder window for current based trips so that it can terminate properly once the FAULT_REC_TRIG signal (DDB 288) is reset. Previously it needed to wait for Relay 3 to reset also before termination ✓ Power measurement limits added to prevent non zero values with no current and voltage. Also power factor measurements limited to +/-1 ✓ Resolved possible reboot caused by failure to time sync. from DNP 3.0 when IRIG-B is active which is also providing the time sync. Now, any failure of the DNP 3.0 to time sync. will only produce a maintenance record ✓ Correction to French, German and Spanish language menu text for generator differential IS2 setting [3004] which incorrectly refers to the setting as IS1. ✓ Resolved possible problem with disturbance recorder triggering which could cause loss of disturbance record data, temporary freezing of the user interface or loss of rear port communications ✓ Resolved unreliable MODBUS framing ✓ Resolved creation of spurious password expired event when menu cell or MODBUS register is accessed ✓ Resolved error code 0x 8D840000 ✓ Minor bug fixes	V2.00 or Later	TG8614B

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
03 Cont.	G	A	Jun 2004	✓ For Courier/DNP 3.0/IEC60870-5-103 builds only ✓ Correction to parity setting for MODBUS and DNP 3.0 when the relay is powered up ✓ Improvement to the self checking of the analog channels and SRAM ✓ Minor bug fixes	V2.00 or later	TG8614B
	H	A	Jul 2004	✓ For MODBUS builds only ✓ Changes as for G ✓ Improvement to the MODBUS driver to cope better with spurious data transmissions and failures of the relay to respond to commands where the server response time is fast ✓ Minor bug fixes	V2.00 or later	TG8614B
	J	A	Jun 2005	✓ Correction to the alarm and trip indication of the faulted phase(s) for the second stage of the undervoltage and overvoltage protection in the fault record information on the relay LCD ✓ Correction to false frequency protection start at power-up ✓ MODBUS driver modified to prevent relay reboot with error code 0x8C810000 in hardware A/B/C relays for 60Hz applications where fast polling and high baud rates are used ✓ Modification to prevent reboot when large number of control and settings are sent to relay in quick succession over DNP 3.0 ✓ Minor bug fixes	V2.00 or later	TG8614B

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
04	A	A	Jun 2001	✓ **Not released to production** ✓ Pole slipping and sensitive reverse power added ✓ 100% stator earth fault protection enhancements. W/VAr/VA inhibit elements added to 3rd harmonic undervoltage protection and 3rd harmonic overvoltage protection added ✓ Neutral voltage displacement threshold, VN>1/2, increased from 50 to 80 V (Vn=100/120 V), 200 to 320 V (Vn=380/480 V) ✓ Earth fault polarizing voltage threshold, Vnpol, increased from 22 to 88 V (Vn=100/120 V) and 88 to 352 V (Vn=380/480 V) ✓ Cos phi and sin phi features added to SEF protection ✓ Minor bug fixes	V2.01 or later	TG8614B
	B	A	Jul 2001	✓ **Not released to production** ✓ Minor bug fix to background self-check diagnostics introduced in 04A	V2.01 or later	TG8614B
	C	A	Dec 2001	✓ Correction to Courier NPS thermal reset command ✓ Minor bug fixes	V2.01 or later	TG8614B
	D	A	Jan 2002	✓ Resolved possible reboot caused by Disturbance Recorder ✓ Minor bug fixes	V2.01 or later	TG8614B
	E	A	Feb 2002	✓ Resolved possible reboot caused by invalid MODBUS requests ✓ Minor bug fixes	V2.01 or later	TG8614B

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
04 Cont.	F	A	Dec 2002	✓ Enhanced DNP 3.0 Object 10 support for Pulse On/Close control points ✓ DNP 3.0 Object 10 included in Class 0 poll ✓ DNP 3.0 support for season in time information ✓ Correction to MODBUS CB Trip and Close via "0" command ✓ Change to neutral voltage displacement protection and directional SEF protection so that they are not blocked by the VT supervision logic when the VN Input and ISEF>VNPol are selected as Measured ✓ Correction to undervoltage stage 2 (V<2) setting range. The setting range has been increased from 10-70 V to 10-120 V (Vn=110/120 V) so that it is the same as V<1 ✓ Correction to VT ratio scaling problem in the disturbance recorder ✓ Improvement to the RTD start-up calibration routine ✓ Minor bug fixes	V2.01 or later	TG8614B
	G	A	Mar 2004	✓ Improvement to the differential protection performance at low frequencies ✓ Correction to the fault recorder window for current based trips so that it can terminate properly once the FAULT_REC_TRIG signal (DDB 288) is reset. Previously it needed to wait for Relay 3 to reset also before termination ✓ Power measurement limits added to prevent non zero values with no current and voltage. Also power factor measurements limited to +/-1	V2.01 or later	TG8614B

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
04 Cont.	G	A	Mar 2004	✓ Resolved possible reboot caused by failure to time sync. from DNP 3.0 when IRIG-B is active which is also providing the time sync. Now, any failure of the DNP 3.0 to time sync. will only produce a maintenance record ✓ Correction to French, German and Spanish language menu text for generator differential IS2 setting [3004] which incorrectly refers to the setting as IS1 ✓ Resolved possible problem with disturbance recorder triggering which could cause loss of disturbance record data, temporary freezing of the user interface or loss of rear port communications ✓ Resolved unreliable MODBUS framing ✓ Resolved creation of spurious password expired event when menu cell or MODBUS register is accessed ✓ Resolved error code 0x 8D840000 ✓ Minor bug fixes	V2.01 or later	TG8614B
	(1)G	A	Mar 2004	✓ Changes are the same as 04G ✓ Special for Powerformer stuck pole breaker fail application where the neutral voltage displacement setting range has been increased from 80 to 200 V (Vn-100/120 V) ✓ MODBUS build only	V2.01 or later	TG8614B
	H	A	Jun 2004	✓ For Courier/DNP 3.0/IEC60870-5-103 builds only ✓ Correction to parity setting for MODBUS and DNP 3.0 when the relay is powered up ✓ Improvement to the self checking of the analog channels and SRAM	V2.01 or later	TG8614B

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
04 Cont.	J	A	Jul 2004	✓ For MODBUS builds only ✓ Changes as for H ✓ Improvement to the MODBUS driver to cope better with spurious data transmissions and failures of the relay to respond to commands where the server response time is fast ✓ Minor bug fixes	V2.01 or later	TG8614B
	K	A	Jun 2005	✓ Changes are the same as 03J	V2.01 or later	TG8614B
05	A	A/B	Sep 2001	✓ Not released to production ✓ Thermal overload protection added ✓ Additional stage of under-impedance protection ✓ Control inputs added ✓ PSL DDB list of signals increased from 512 to 1023 signals ✓ PSL Data menu added with PSL Reference information for version history ✓ Optional additional opto inputs and output contacts with a larger case size option available ✓ New ‘Universal’ wide ranging opto inputs (Model number hardware suffix changed to B) ✓ New output contacts with better break and continuous carry ratings (Model number hardware suffix changed to B) ✓ Minor bug fixes ✓ Courier and MODBUS builds only	V2.05 or Later	P34x/EN T/C11

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
05 Cont.	B	A/B	Oct 2001	✓ Not released to production ✓ Correction to VT ratio scaling problem in the disturbance recorder ✓ Minor bug fixes ✓ Courier and MODBUS builds only	V2.05 or Later	P34x/EN T/C11
	1(C)	A/B	Aug 2000	✓ IEC60870-5-103 build with special private code mapping for ALSTOM Power project in Iceland. Includes private codes and uncompressed disturbance recorder ✓ Resolved possible reboot caused by Disturbance Recorder ✓ Minor bug fixes ✓ IEC60870-5-103 build only	V2.05 or Later	P34x/EN T/C11
	D	A/B	Feb 2002	✓ Resolved possible reboot caused by Disturbance Recorder ✓ Resolved possible reboot caused by invalid MODBUS requests ✓ Enhancements to IEC 60870-5-103 build to include private codes, monitor blocking and disturbance record extraction. New uncompressed disturbance recorder for IEC 60870-5-103 build only ✓ Correction to Courier NPS thermal reset command ✓ Correction to IEC 60870-5-103 voltage measurements for Vn=380/480 V relays ✓ Minor bug fixes	V2.05 or Later	P34x/EN T/C11

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
05 Cont.	E	A/B	Mar 2002	✓ Correction to foreign language text for System Backup protection not included in previous 05 software builds ✓ Minor bug fixes	V2.05 or Later	P34x/EN T/C11
	F	A/B	Oct 2002	✓ DNP 3.0 Object 12 “CROB” implementation is now compliant for simple function points ✓ Correction to MODBUS CB Trip and Close via "0" command ✓ Change to neutral voltage displacement protection and directional SEF protection so that they are not blocked by the VT supervision logic when the VN Input and ISEF>VNPol are selected as Measured ✓ Correction to undervoltage stage 2 (V<2) setting range. The setting range has been increased from 10-70 V to 10-120 V (Vn=110/120 V) so that it is the same as V<1 ✓ Improvement to the RTD start-up calibration routine ✓ Minor bug fixes	V2.05 or later	P34x/EN T/C11
	1(F)	A/B	Oct 2002	✓ IEC60870-5-103 build with special private code mapping for ALSTOM Power project in Iceland. Includes private codes and uncompressed disturbance recorder ✓ Correction to IEC60870-5-103 voltage measurements for Vn=380/480 V relays ✓ Correction to foreign language text for System Backup protection not included in previous 05 software builds ✓ Change to neutral voltage displacement protection and directional SEF protection so that they are not blocked by the VT supervision logic when the VN Input and ISEF>VNPol are selected as Measured	V2.05 or later	P34x/EN T/C11

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
05 Cont.	1(F)	A/B	Oct 2002	✓ Improvement to the RTD start-up calibration routine ✓ Minor bug fixes ✓ IEC60870-5-103 build only	V2.05 or later	P34x/EN T/C11
	G	A/B	Mar 2004	✓ Control input states added to non-volatile memory ✓ German language text updated ✓ Power measurement limits added to prevent non zero values with no current and voltage. Also power factor measurements limited to +/-1 ✓ In the Commissioning Test menu the DDB status has been made visible on the front panel display ✓ Support for Trip LED Status and Alarm Status added to G26 data type for MODBUS register 30001 ✓ Correction to the CB trip/Close functionality via MODBUS so that local/remote setting in the CB Control menu is not ignored ✓ Correction to MODBUS auto event extraction which does not work correctly ✓ DNP 3.0 Object 12 “CROB” implementation is now compliant for simple function points ✓ DNP 3.0 object 10 added to class 0 poll ✓ Correction to DNP 3.0 time sync. operation so that it does not modify the season bit in the time stamp ✓ Improvement to the differential protection performance at low frequencies	V2.05 or Later	P34x/EN T/C11

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
05 Cont.	G	A/B	Mar 2004	✓ Correction to the manual reset user alarms so that the event record shows the alarm turning off only when a reset command has been issued. Previously the "alarm off" event is produced once the initiating signal is removed ✓ Correction to the fault recorder window for current based trips so that it can terminate properly once the FAULT_REC_TRIG signal (DDB 288) is reset. Previously it needed to wait for Relay 3 to reset also before termination ✓ DDB 649 for pole slip reactance line start removed from the event list ✓ Resolved possible reboot caused by failure to time sync. from DNP 3.0 when IRIG-B is active which is also providing the time sync. Now, any failure of the DNP 3.0 to time sync. will only produce a maintenance record ✓ Correction to French, German and Spanish language menu text for generator differential IS2 setting [3004] which incorrectly refers to the setting as IS1 ✓ Correction to the alarm and trip indication of the faulted phase(s) for the second stage of the undervoltage and overvoltage protection in the fault record information on the relay LCD ✓ Correction to the C32CS error when extracting and saving an uncompressed disturbance record from the P34x through the front port using MiCOM S1 Studio. This only applies to P34x IEC60870-5-103 protocol builds since this is the only communication option that supports uncompressed disturbance records. The error is caused by unavailable opto inputs or relay contacts being assigned to digital inputs in the Disturbance Recorder menu	V2.05 or Later	P34x/EN T/C11

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
05 Cont.	G	A/B	Mar 2004	✓ Resolved possible problem with disturbance recorder triggering which could cause loss of disturbance record data, temporary freezing of the user interface or loss of rear port communications ✓ Resolved unreliable MODBUS framing ✓ Resolved creation of spurious password expired event when menu cell or MODBUS register is accessed ✓ Resolved error code 0x 8D840000 ✓ Minor bug fixes	V2.05 or Later	P34x/EN T/C11
	H	A/B	Jun 2004	✓ For Courier/DNP 3.0/IEC60870-5-103 builds only ✓ Correction to parity setting for MODBUS and DNP 3.0 when the relay is powered up ✓ Improvement to the self checking of the analog channels and SRAM ✓ Minor bug fixes	V2.05 or later	P34x/EN T/C11
	J	A/B	Jun 2004	✓ For MODBUS builds only ✓ Changes as for H ✓ Improvement to the MODBUS driver to cope better with spurious data transmissions and failures of the relay to respond to commands where the server response time is fast ✓ Minor bug fixes	V2.05 or later	P34x/EN T/C11
	K	A/B	Jun 2005	✓ MODBUS Time Transmission Format selectable via MODBUS only setting as Standard or Reverse for transmission of byte order	V2.05 or later	P34x/EN T/C11

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
05 Cont.	K	A/B	Jun 2005	✓ V/Hz Protection drop-off/pick-up (DO/PU) ratio changed from 95% to 98% ✓ DO/PU ratio changed from 95% to 98% for Over/Under Voltage protection. Trip threshold changed from 1.05, 0.95 Vs to 1 Vs for Over and Under Voltage and NVD protection. TMS setting of Under/Over Voltage protection reduced from 0.5 to 0.05. ✓ Correction to false frequency protection start at power-up ✓ MODBUS driver modified to prevent relay reboot with error code 0x8C810000 in hardware A/B/C relays for 60Hz applications where fast polling and high baud rates are used ✓ Modification to prevent reboot when large number of control and settings are sent to relay in quick succession over DNP 3.0 ✓ IEC60870-5-103. Status of summer bit now works correctly in time sync. command ✓ Correction to DNP 3.0 software where settings download from MiCOM S1 Studio can fail for relays that have model dependent I/O configurations ✓ Minor bug fixes	V2.05 or later	P34x/EN T/C11

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
05 Cont.	L	A/B	July 2007	✓ Correction to menu cell addressing for 05K. Version 05K software was built from 31 software to incorporate latest bug fixes. In doing this build of the 05K software the menu cell addressing changes that are in 06 software were included. These mainly affect the cell addresses of functions which have IDMT characteristics. The result is the default S1 files for 05 software are not compatible with a relay with 05K software. The 05L software fixes this problem so now the default S1 files for 05 software are compatible with a relay with 05L software. ✓ Minor bug fixes	V2.05 or later	P34x/EN T/C11
06	A	A/C	Aug 2000	✓ **Not released to production** ✓ Additional IDMT characteristics for overcurrent and voltage dependent overcurrent protection (rectifier and RI curve), earth fault protection (RI and IDG curve) and sensitive earth fault protection (IDG curve) ✓ Change to time dial setting range of IEEE and US curves. Previously curves were based on TD/7 where TD = 0.5-15. Now, curves are based on TD where TD = 0.01-100. Also, includes change to US ST Inverse (C02) curve. K constant and L constant multiplied x 7 because of change to TD, now K=0.16758 and L=0.11858 ✓ Angle measurements for sequence quantities in Measurements 1 menu added ✓ Interturn protection added ✓ Optional 2nd rear communication port added ✓ New power supply with increased output rating and reduced dc inrush current (typically < 10A). (Model number hardware changed to suffix C)	V2.06 or Later	P34x/EN T/D22

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
06 Cont.	A	A/C	Aug 2000	✓ Wider setting range for Power and Sensitive Power protection. P>1/2 (reverse power) and P<1/2 (low forward power) maximum setting changed from 40 In to 300 In W (Vn=100/120 V) and from 160 In W to 1200 In W (Vn=380/480 V). Sen. –P>1/2 and Sen. P<1/2 maximum setting changed from 15 In to 100 In W (Vn=100/120 V) and from 60 In to 400 In W (Vn=380/480 V). There is also an additional setting for the Power and Sensitive Power protection to select the Operating mode as Generating or Motoring ✓ Wider setting range for the voltage dependent overcurrent protection. Volt Dep. OC V<1 and V<2 minimum setting changed from 20 to 5 V (Vn=100/120 V) and from 80 to 20 V (Vn=380/480 V). V Dep. OC k Set minimum setting changed from 0.25 to 0.1 ✓ Maximum overfrequency protection setting increased from 65 to 68 Hz ✓ Change to undervoltage stage 2 (V<2) setting range to correct an error. The setting range has been increased from 10-70 V to 10-120 V (Vn=100/120 V) so that it is the same as V<1 ✓ Change to neutral voltage displacement protection and directional SEF protection so that they are now not blocked by the voltage transformer supervision logic when the VN Input and ISEF> VN Pol are selected as Measured ✓ Includes all the improvements and corrections in 05F software except for 2 enhancements shown for 06B ✓ Minor bug fixes	V2.06 or Later	P34x/EN T/D22

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
06 Cont.	B	A/C	Oct 2002	✓ Correction to undervoltage stage 2 (V<2) setting range. The setting range has been increased from 10-70 V to 10-120 V (Vn=110/120 V) so that it is the same as V<1 ✓ Enhancements to IEC60870-5-103 build to include private codes, monitor blocking and disturbance record extraction. New uncompressed disturbance recorder for IEC60870-5-103 build only ✓ Improvement to the RTD start-up calibration routine ✓ Minor bug fixes	V2.06 or Later	P34x/EN T/D22
	C	A/C	Mar 2004	✓ Changes are the same as 05G	V2.06 or Later	P34x/EN T/D22
	D	A/C	Jun 2004	✓ For Courier/DNP 3.0/IEC60870-5-103 builds only ✓ Correction to parity setting for MODBUS and DNP 3.0 when the relay is powered up ✓ Improvement to the self checking of the analogue channels and SRAM ✓ Minor bug fixes	V2.06 or later	P34x/EN T/D22
	E	A/C	Jul 2004	✓ For MODBUS builds only ✓ Changes as for D ✓ Improvement to the MODBUS driver to cope better with spurious data transmissions and failures of the relay to respond to commands where the server response time is fast ✓ Minor bug fixes	V2.06 or later	P34x/EN T/D22
	F	A/C	Jun 2005	✓ Changes are the same as 05K		

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
06 Cont.	G	A/C	July 2009	✓ This release is specific for Hydro Quebec (HQ) to provide a P343 relay with modified single phase sensitive power protection which uses B Phase to calculate sensitive power as apposed to A-Phase in the standard software versions.	V2.06 or later	P34x/EN T/D22
07	A	A/C	Apr 2003	✓ **Not released to production** ✓ Optional additional 4 analog inputs and 4 outputs (current loop inputs and outputs - CLIO) ✓ Additional setting to select the current inputs (IA-1, IB-1, IC-1 or IA-2, IB-2, IC-2) used for the breaker fail undercurrent ✓ Two new hardware configurations - (1) 32 Inputs, 16 Outputs, RTD, CLIO (2) 16 Inputs, 32 Outputs, RTD, CLIO ✓ Number of alarms increased from 64 to 96 (New Alarm Status 3 word - 32 bit) ✓ Additional user alarms. Previously 1 manual reset and 2 self reset user alarms, now 12 manual reset and 4 self reset user alarms ✓ Control Input states added to non volatile memory ✓ German language text updated ✓ Courier and MODBUS builds only ✓ Minor bug fixes	V2.09 or Later	P34x/EN T/E33 (ALSTOM) or P34x/EN T/F33 (AREVA)
	B	A/C	Oct 2003	✓ Power measurement limits added to prevent non zero values with no current and voltage. Also power factor measurements limited to +/-1 ✓ In the Commissioning Test menu the DDB status has been made visible on the front panel display	V2.09 or Later	P34x/EN T/E33 (ALSTOM) or P34x/EN T/F33 (AREVA)

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
07 Cont.	B	A/C	Oct 2003	✓ Support for Trip LED Status and Alarm Status added to G26 data type for MODBUS register 30001 ✓ Correction to the CB trip/Close functionality via MODBUS so that local/remote setting in the CB Control menu is not ignored ✓ Correction to MODBUS auto event extraction which does not work correctly in versions 05 and 06 software ✓ Extension of the control input functionality to support pulse and latch operations in DNP3.0 ✓ DNP 3.0 object 10 added to class 0 poll ✓ Correction to DNP 3.0 time sync. operation so that it does not modify the season bit in the time stamp ✓ Improvement to the differential protection performance at low frequencies ✓ Correction to the manual reset user alarms so that the event record shows the alarm turning off only when a reset command has been issued. Previously the "alarm off" event is produced once the initiating signal is removed ✓ Correction to the fault recorder window for current based trips so that it can terminate properly once the FAULT_REC_TRIG signal (DDB 288) is reset. Previously it needed to wait for Relay 3 to reset also before termination ✓ DDB 649 for pole slip reactance line start removed from the event list ✓ Minor bug fixes	V2.09 or Later	P34x/EN T/E33 (ALSTOM) or P34x/EN T/F33 (AREVA)

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
07 Cont.	C	A/C	Mar 2004	✓ Resolved possible reboot caused by failure to time sync. from DNP 3.0 when IRIG-B is active which is also providing the time sync. Now, any failure of the DNP 3.0 to time sync. will only produce a maintenance record ✓ Correction to French, German and Spanish language menu text for generator differential IS2 setting [3004] which incorrectly refers to the setting as IS1 ✓ Correction to the alarm and trip indication of the faulted phase(s) for the second stage of the undervoltage and overvoltage protection in the fault record information on the relay LCD ✓ Correction to the C32CS error when extracting and saving an uncompressed disturbance record from the P34x through the front port using MiCOM S1 Studio. This only applies to P34x IEC60870-5-103 protocol builds since this is the only communication option that supports uncompressed disturbance records. The error is caused by unavailable opto inputs or relay contacts being assigned to digital inputs in the Disturbance Recorder menu ✓ Resolved possible problem with disturbance recorder triggering which could cause loss of disturbance record data, temporary freezing of the user interface or loss of rear port communications ✓ Resolved unreliable MODBUS framing ✓ Resolved error code 0x 8D840000 ✓ Minor bug fixes	V2.09 or Later	P34x/EN T/E33 (ALSTOM) or P34x/EN T/F33 (AREVA)

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
07 Cont.	D	A/C	Jun 2004	✓ For Courier/DNP 3.0/IEC60870-5-103 builds only ✓ Correction to parity setting for MODBUS and DNP 3.0 when the relay is powered up ✓ Improvement to the self checking of the analog channels and SRAM ✓ Minor bug fixes	V2.09 or later	P34x/EN T/E33 (ALSTOM) or P34x/EN T/F33 (AREVA)
	E	A/C	Jul 2004	✓ For MODBUS builds only ✓ Changes as for D ✓ Improvement to the MODBUS driver to cope better with spurious data transmissions and failures of the relay to respond to commands where the server response time is fast ✓ Minor bug fixes	V2.09 or later	P34x/EN T/E33 (ALSTOM) or P34x/EN T/F33 (AREVA)
	F	A/C	Jun 2005	✓ Changes are the same as 05K	V2.09 or later	P34x/EN T/E33 (ALSTOM) or P34x/EN T/F33 (AREVA)
30	A	J	Nov 2004	✓ Not released to production ✓ Enhanced main processor board ✓ Company name change. 'ALSTOM' changed to 'MiCOM' in default Plant Reference cell and 'ALSTOM P' changed to 'MiCOM P' for ASDU5 message type, IEC protocol ✓ User interface enhancements - larger 100x33 pixel graphical display of 3 lines x 16 characters + 2 new buttons, direct access keys	V2.11 or later	P34x/EN M/G44

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
30 Cont.	A	J	Nov 2004	✓ Control input enhancements. Selection of latched or pulsed mode, control input labels added, disturbance recorder trigger from control inputs ✓ 16 PSL Timers (previously 8) ✓ Platform alarms mapped to the DDB (Alarm Status 3) ✓ Time synchronization using an opto input ✓ Opto input power frequency filter control, enabled/disabled ✓ Courier over EIA(RS)485 can be selected for the 1st rear port in addition to existing K-Bus configuration ✓ Transmission of the first rear port protocols (MODBUS/Courier/DNP3.0) using the fiber-optic port (IEC60870-5-103 previously available) ✓ Uncompressed disturbance recording added for Courier/MODBUS/DNP 3.0 (added to IEC60870-5-103 protocol in 05D, 06B software) ✓ Dual Characteristic DO/PU ratio Opto Inputs (DO/PU = 60/80% or 50/70%) ✓ 512 Event records (previously 250) ✓ DNP3 evolution. Scan interval for binary inputs (object 01) reduced from 5s to 0.5s. Scan interval for analog inputs (object 30) reduced from 2s to 1s. Improved minimum step size of analog input dead bands ✓ MODBUS Time Transmission Format selectable as Standard or Reverse for transmission of byte order ✓ V/Hz Protection drop-off/pick-up (DO/PU) ratio changed from 95% to 98%	V2.11 or later	P34x/EN M/G44

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
30 Cont.	A	J	Nov 2004	✓ DO/PU ratio changed from 95% to 98% for Over/Under Voltage protection. Trip threshold changed from 1.05, 0.95 Vs to 1 Vs for Over and Under Voltage and NVD protection. TMS setting of Under/Over Voltage protection reduced from 0.5 to 0.05 ✓ CT Supervision for 2nd set of 3 phase CTs. Previously only IA/IB/IC inputs supervised ✓ Default labels changed for the digital inputs and outputs in Input Labels and Output Labels menu. Changed to be more generic - Input Lx, Output Rx ✓ Correction to false frequency protection start at power-up ✓ IEC60870-5-103. Status of summer bit now works correctly in time sync command ✓ Minor bug fixes	V2.11 or later	P34x/EN M/G44
	B	J	Dec 2004	✓ Modification to prevent reboot when large number of control and settings are sent to relay in quick succession over DNP 3.0 ✓ Correction to 2nd rear comms. port channel failure for P34xxxxxxxxxxJ relays only ✓ Minor bug fixes	V2.11 or later	P34x/EN M/G44
31	A	J	Apr 2005	✓ New relay model available, the P344 (80TE case only). The P344 is based on the P343 but has an additional neutral voltage input, VN2, to provide 2 measured neutral voltage protection functions (59N) for earth fault and interturn protection ✓ 4 stages of directional overcurrent protection (67). Previous P342/3/4 software versions included 2 stages of non directional overcurrent protection	V2.11 or later	P34x/EN M/G44

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
31 Cont.	A	J	Apr 2005	✓ 1 stage of definite time negative phase sequence overpower protection (S2=I2xV2)(32NPS). This is used in China as an interlocking signal for the neutral voltage interturn protection ✓ Independent derived/measured neutral voltage protection (59N). P341/2/3 has 2 stages of measured and 2 stages of derived neutral voltage protection ✓ P344 has 2 measured neutral voltage inputs and so has 2x2 stages of measured and 2 stages of derived neutral voltage protection. Previous software versions included 2 stages of measured or derived neutral voltage protection ✓ 6 bands of generator abnormal frequency protection (81AB). Similar to P94x 81AB function ✓ 1 definite time stage of negative phase sequence overvoltage protection (47). Same as P14x (47) function ✓ 4 definite time stages of negative phase sequence overcurrent protection (46OC). Same as P14x (46OC) function ✓ P342/3 minimum three phase power settings reduced to 0.5%Pn, previously 2%Pn. P344 3 phase power setting range is as new P343 setting range ✓ 3 additional definite time delayed overfluxing protection stages. The inverse time overfluxing characteristic has been modified to make it more consistent with competitors and to aid future enhancements. The overfluxing protection now comprises of 1 definite time alarm + 1 inverse/DT trip stage + 3 definite time trip stages ✓ Correction to DNP 3.0 software where settings download from MiCOM S1 Studio can fail for relays that have model dependent I/O configurations	V2.11 or later	P34x/EN M/G44

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
31 Cont.	A	J	Apr 2005	✓ Minor bug fixes	V2.11 or later	P34x/EN M/G44
32	A	J	Mar 2006	✓ **Not released to production** ✓ Phase rotation function added. Can select phase rotation as ABC or ACB for all 3 phase current and voltage inputs. Can also individually select which 2 phases are swapped for any of the 3 phase current and voltage inputs. New menu column 'System Config' with phase rotation settings. 'Gen Diff' menu column moved to make way for 'System Config' menu ✓ In the disturbance recorder the maximum number of analogue channels that can be recorded is increased so that all analogue inputs can be recorded. Number of analogue channels is increased from 8 to 9/12/13 for P342/3/4 ✓ Number of PSL DDB signals increased from 1023 to 1408 and DDBs re-organized. This means that the PSL created in version 32 software is not compatible to PSL created in previous software versions and vice versa ✓ Setting Group selection via 2 new DDB signals makes it possible to select a setting group via any opto input or remotely via a Control Input. Previously, the 4 setting groups could be selected using fixed opto inputs, 1 and 2 ✓ An 'Any Trip' DDB has been created to allow any contact(s) to be used as the trip indication. Previously, the Any Trip signal was defined as operation of Relay contact 3. The Any Trip signal operates the Trip LED, initiates the breaker fail logic and maintenance counters and is used in the fault recorder logic ✓ Minor changes to description of CT and VT Ratio settings ✓ Number of maintenance records increased from 5 to 10	V2.14 or later	P34x/EN M/G44 P34x/EN AD/G54

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
32 Cont.	A	J	Mar 2006	✓ Inter frame gap added between frames in multi-frame transmission of DNP 3.0 messages to be compatible with C264 ✓ Correction to error in NPS directional overcurrent operating time delay. The excess in the operating time (always less than 1s) only occurs when set to directional ✓ Correction to intermittent incorrect IRIG-B status indication of 'Card Failed' with healthy IRIG-B source ✓ Minor bug fixes	V2.14 or later	P34x/EN M/G44 P34x/EN AD/G54
	B	J	May 2006	✓ Minor bug fixes	V2.14 or later	P34x/EN M/G44 P34x/EN AD/G54
	C	J	Oct 2006	✓ New P345 relay model. The P345 includes the same functions as the P344 plus 100% stator earth fault protection via low frequency injection. The P345 also includes a new front panel with 10 function keys and 10 associated programmable LEDs. All 18 of the P345 programmable LEDs are tri-color and can be set as red, yellow or green in the PSL. P345 not released to production. ✓ MODBUS allows individual 16 bit register pairs that make up 32 bit data to be accessed individually. ✓ Correction to fast operation of overcurrent protection with IEEE/US inverse time reset characteristic. ✓ Minor bug fixes	V2.14 or later	P34x/EN M/H65

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
32 Cont.	D	J	Dec 2006	✓ Correction to P34x Directional Sensitive Earth Fault (Forward or reverse) function. Function does not operate if SEF/REF Protection is initially disabled in the configuration column and SEF Mode is set to 'SEF' (default setting) when the relay is booted up. Correct operation will only occur when the SEF Mode setting is changed (submitted) and changed back to 'SEF' or the relay is rebooted with SEF/REF enabled in the configuration column. ✓ Minor bug fixes	V2.14 or later	P34x/EN M/H65
	E	J	April 2007	✓ P343 IEC61850 added. IEC61850 not released to production. ✓ Minor bug fixes	V2.14 or later	P34x/EN M/H65
	F	J/K	May 2007	✓ New P345 relay model released to production. The P345 includes the same functions as the P344 plus 100% stator earth fault protection via low frequency injection. The P345 also includes a new front panel with 10 function keys and 10 associated programmable LEDs. All 18 of the P345 programmable LEDs are tri-color and can be set as red, yellow or green in the PSL ✓ Improvement made to 100% stator earth fault (64S) measurement algorithm to improve accuracy. '64S Series X' setting removed and new '64S Fail' DDB (1076) added. ✓ Correction to VT secondary ratio setting for 32 software relays, Vn = 380/480 V rating. With a 1:1 VT ratio on a 380/480 V P340 relay with 32 software installed after power up the analogue quantities are 4 times too large. The error is corrected by re-appying the VT secondary (which is showing the correct value) setting.	V2.14 or later	P34x/EN M/H65

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
32 Cont.	F	J/K	May 2007	✓ Local time zone adjustments for daylight saving time added to Date and Time menu. ✓ Minor bug fixes	V2.14 or later	P34x/EN M/H65
	G	J/K	Sept 2007	✓ Correction to CT secondary ratio setting for 32F software relays. When relay is powered off and on the secondary CT ratio is applied incorrectly for a 5A rating such that currents measured are 5 times too small. CT ratio is applied correctly if settings re-applied when relay is powered on. ✓ Correction to incorrect year being set when date and time is set via the user interface with IRIG-B active. ✓ Minor bug fixes	V2.14 or later	P34x/EN M/H65
	H	J/K	Nov 2007	✓ Correction to the CT ratio scaling for 32 software relays. If the CT ratio secondary settings are set to 5A and the relay rebooted, if the setting group is changed the CT secondary scaling reverts to 1A. ✓ Minor bug fixes	V2.14 or later	P34x/EN M/H65
	J	J/K	Dec 2007	✓ IEC 61850 communications added. ✓ Support released for high break contacts and de-modulated IRIG-B in all P34x relays. P34x relays can be ordered with modulated or de-modulated IRIG-B and with 4 or 8 high break contacts depending on the model. ✓ Minor bug fixes	V2.14 or later	P34x/EN M/H65

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
32 Cont.	K	J/K	May 2008	✓ Correction to VT ratio problem. The VT ratio, if modified, is reset back to default values when the P345 relay is rebooted. This in turn causes the measurements to effectively display 'secondary' quantities as it now has a 1:1 ratio. This problem does not affect protection operation because the relay operates on 'per unit' quantities, which are unchanged. The primary and secondary ratios are used to scale the measurements and settings for display, communication and recording. ✓ Minor bug fixes	V2.14 or later	P34x/EN M/H65
	L	J/K	March 2009	✓ Correction to ISEF and IN Secondary CT ratio scaling incorrectly being applied if both not set to the same value (1A or 5A) - P345 only, P341/2/3/4 not affected. ✓ Minor bug fixes	V2.14 or later	P34x/EN M/H65
	M	J/K	March 2011	✓ Rebranding software to ALSTOM. ✓ Correction to Px4x which stops receiving (processing) GOOSE messages when managed Ethernet switch parameterised for VLAN.	V2.14 or later	P34x/EN M/H65
33	A	J/K	June 2008	✓ Rotor earth fault protection added to P342/3/4/5 when CLIO card is fitted. Rotor earth fault function also requires P391 low frequency injection, coupling and measurement unit. ✓ DNP 3.0 enhancements: configurable points table, default variations, SBO timeouts, integer scaling, floating point analogue values, disturbance record extraction, remote settable deadbands and class assignment, configurable message length and timeouts, data link confirmation, alias control inputs.	V3.0 (Studio) or later	P34x/EN M/J76

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
33 Cont.	A	J/K	June 2008	✓ Support for Russian language added. This is now an order option. ✓ PSL positional data is now downloaded to the relay with the logic so that when the PSL is extracted from the relay the positional data of signals etc is the same as when downloaded. ✓ Support for set/reset latches in the PSL added. ✓ Minor bug fixes	V3.0 (Studio) or later	P34x/EN M/J76
	B	J/K	March 2009	✓ Correction to ISEF and IN Secondary CT ratio scaling incorrectly being applied if both not set to the same value (1A or 5A) - P345 only, P341/2/3/4 not affected. ✓ Minor bug fixes	V 3.0 (Studio) or later	P34x/EN M/J76
	C	J/K	June 2009	✓ Correction to Residual O/V NVD protection where derived neutral voltage is used for all protection stages (VN>1/2/3/4/5/6) instead of VN>1/2 (derived), VN>2/3 (VN1 input, measured), VN>5/6 (VN2 input, measured, P344/5 only). This bug only affect 33B software. ✓ Minor bug fixes	V 3.0 (Studio) or later	P34x/EN M/J76
	D	J/K	Feb 2010	✓ Correction to several IEC61850 modeling issues for phase 1 of IEC 61850. ✓ (1) Correction to missing measurements (VN/IN Derived Mag/Angle, NPS Thermal, V/Hz) and incorrect sourcing in the P340 IEC 61850 Phase 1 data model implementation. ✓ (2) Correction to DDB signal status which is not available to 61850 model when events are configured to be filtered out.	V 3.0 (Studio) or later	P34x/EN M/J76

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
33 Cont.	D	J/K	Feb 2010	✓ (3) Correction to some of the strings for the Data Attributes under the 'NamPlt' Data Object under LLN0 (only) of some of the Logical Devices. ✓ Minor bug fixes	V3.0 (Studio) or later	P34x/EN M/J76
	E	J/K	March 2011	✓ Rebranding software to ALSTOM. ✓ Correction to Px4x which stops receiving (processing) GOOSE messages when managed Ethernet switch parameterised for VLAN.	V3.0 (Studio) or later	P34x/EN M/J76
35	A	J/K	Dec 2009	✓ Redundant Ethernet port option (IEC61850) ✓ IEC 61850 Phase 3 enhancements:Controls - Direct Control, Direct Control with enhanced security, Select Before Operate (SBO) with enhanced security, Eight Buffered Report Control Blocks and sixteen Unbuffered Report Control Blocks, Configurable Data Sets, Published GOOSE messages, Uniqueness of control, Select Active Setting Group, Quality for GOOSE, Address List, Originator of Control, Energy measurements and Reset controls for demand and thermal measurements using the MMTR Logical Node, Unit multipliers for all measurements. ✓ Read Only Mode for remote communications ports added ✓ Correction to DDB signal status not being available to 61850 model when events are configured to be filtered out ✓ Correction to some of the strings for the IEC61850 Data Attributes under the 'NamPlt' Data Object under LLN0 (only) of some of the Logical Devices ✓ Minor bug fixes	V3.0 (Studio) or later	P34x/EN AD/J86

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
35 Cont.	B	J/K	Nov 2010	✓ Improvements to IEC61850 comms fixing problems as described below: ✓ (1) A short on/off pulse state may cause the interim stage change to be not reported. ✓ (2) Occasionally an opto-input change of state is not registered in System\OptGGIO1.ST. ✓ (3) Applying XCBR1.CO.Pos Open/Close can cause the relay to reply with Invalid Position even though the Open/Close operation is successful ✓ (4) IEC61850 communications can terminate after operating a control with control status in RCB ✓ (5) IEC61850 buffered reporting stops working after a period of time when applying several faults to generate reports ✓ Minor bug fixes	V3.0 (Studio) or later	P34x/EN AD/J86
	C	J/K	March 2011	✓ Rebranding software to ALSTOM. ✓ Correction to Px4x which stops receiving (processing) GOOSE messages when managed Ethernet switch parameterised for VLAN.	V3.0 (Studio) or later	P34x/EN AD/I86
36	B	J/K	July 2011	✓ New relay model, P346. ✓ P346 is the same as P342 + differential protection. ✓ Transformer Differential protection, Differential CT Supervision and Circuitry Fault Alarm functions added to P343/4/5/6. ✓ Transformer thermal overload and Loss of Life functions added, based on the IEEE Standard C57.91-1995. ✓ Transformers Through Fault monitoring added.	V3.0 (Studio) or later	P34x/EN M/I96

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
36 Cont.	B	J/K	July 2011	✓ Check synchronization and CB Control functions added. ✓ 4 definite time stages of df/dt protection added. ✓ Selectable CT source - IA-1/IB-1/IC-1 or IA-2/IB-2/IC-2 for Overcurrent, NPS Overcurrent, Restricted Earth Fault, NPS Power and Dead Machine protection added. ✓ CT Polarity - Standard/Inverted added. ✓ Phase CT2 ratio added due to transformer differential protection (87T) being added. In previous software there was only 1 Phase CT ratio setting for the 2 sets of phase CTs used for generator differential protection (87G). Phase CT primary setting increased to 30k. ✓ Low Impedance biased restricted earth fault protection improved by addition of transient bias to make more stable for through faults. ✓ Improved undercurrent detector algorithm for CB Fail protection added. ✓ Support for Chinese language added. This is now an order option. ✓ Chinese HMI requires two language blocks so only 2 other languages are supported, by default these are English and French. ✓ IEC 60870-5-103 generic services added. This enables all measurements to be available with this protocol. ✓ New front panel for P343/4/6 the same as P345 with 18 tri-color leds and 10 function keys (K hardware - P34xxxxxxxxxxK).	V3.0 (Studio) or later	P34x/EN M/I96

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
36 Cont.	B	J/K	July 2011	✓ Number of PSL DDB signals increased from 1407 to 2047. ✓ IEC61850 improvements as 35B software. ✓ Minor bug fixes	V3.0 (Studio) or later	P34x/EN M/I96
	C	J/K	March 2011	✓ Rebranding software to ALSTOM. ✓ Correction to Px4x which stops receiving (processing) GOOSE messages when managed Ethernet switch parameterised for VLAN.	V3.0 (Studio) or later	P34x/EN M/I96
	D	J/K	Sept 2011	✓ Correction P34x SW36 relay with DNP3 protocol and second rear communication card fitted causing the relay to continually reboot with error an code. This software correction was made before any relays of this specific build was released to customers.	V3.0 (Studio) or later	P34x/EN M/I96
	E	J/K	May 2012	✓ Support for Parallel Redundancy Protocol (PRP) included. Order book for PRP opened in July 2012. The following 2 codes are used for digit 7 "Hardware Options" of the Px4x number/cortec, for PRP Ethernet redundancy: N - Redundant Ethernet PRP, 2 multi-mode fibre ports + Modulated IRIG-B [ZN0071 Part 009]. P - Redundant Ethernet PRP, 2 multi-mode fibre ports + Un-modulated IRIG-B [ZN0071 Part 010]. ✓ Generator Differential (87G) protection uses Phase CT ratio for both CT1 and CT2 phase current inputs in previous software versions. SW 36E uses Phase CT1 and Phase CT2 ratio for CT1 and CT2 phase current inputs respectively for the generator differential protection (87G) which is now consistent with how the transformer differential protection (87T) operates.	V3.0 (Studio) or later	P34x/EN M/I96

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
36 Cont.	E	J/K	May 2012	✓ Correction to Px4x relay which uses the wrong Disturbance Record analogue signals magnitudes if the CT and VT ratios (primary/secondary) are not integers. ✓ Minor bug fixes.	V3.0 (Studio) or later	P34x/EN M/I96
	F	J/K	Aug 2013	✓ Correction to the Fault Time time stamp in fault records which does not take into account the local time offset setting. ✓ Correction to Thermal Overload I> setting which doesn't rescale when CT primary or secondary rating changed in MiCOM S1. ✓ Correction to P34x transformer hot spot thermal element which trips in extreme situations ✓ IEC 61850 corrections - DATA name for 3 Phase Power(s) and Power factor are wrongly named, Non-standard modelling of angle measurements in IEC 61850, The mappings of Measurement/SecDlrMMXU1CFAmpPct$SIUnit and Protection/SenSefPTOC4STHealth$stVal are incorrect, There are some Data Attributes that are configured in the data model as Read Only, but are actually writeable; the Data Attributes in question are orCat and orIdent, Unit for Frequency (Hz) missing in Disturbance Record extracted over IEC 61850, Disconnection of one of IEC 61850 Client causes other IEC 61850 Connections being Lost. ✓ Minor bug fixes.	V3.0 (Studio) or later	P34x/EN M/I96
37	A	M	March 2014	✓ New relay model, P348 for variable speed double fed induction machine protection. P348 includes IEC 61850-9-2 LE inputs to connect to non conventional instrument transformers. V37 software applies to P348 model only.	V1.0 (S1 Agile) or later	P34x/EN M/Ia7

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
37 Cont.	A	M	March 2014	✓ P348 includes RMS/Peak overcurrent, RMS/Peak overvoltage, RMS NPS overcurrent, RMS neutral voltage and overfrequency protection. ✓ Cybersecurity added. ✓ New front panel for P348 with xCPU3 with extended memory (M hardware - P34xxxxxxxxxxM). ✓ New power supply modules with field voltage removed. Order code - 7/8/9 for new power supply option (previously 1/2/3). ✓ New opto inputs to provide compliance with the latest IEC EMC surge standards and comply with UK ESI48-4EB2 capacitor discharge tests without using external resistors to sink the energy. ✓ Platform bug fixes added as 36 software. ✓ Minor bug fixes.	V1.0 (S1 Agile) or later	P34x/EN M/Ia7
38	B	M/P	March 2014	✓ V38 software applies to P341-6 models only. ✓ New front panel for P341-6 with xCPU3 with extended memory (P hardware - P341/2xxxxxxxxxP and M hardware - P343/4/5/6xxxxxxxxxM). ✓ New power supply modules with field voltage removed. Order code - 7/8/9 for new power supply option (previously 1/2/3). ✓ New opto inputs to provide compliance with the latest IEC EMC surge standards and comply with UK ESI48-4EB2 capacitor discharge tests without using external resistors to sink the energy. ✓ Cybersecurity added. ✓ DNP 3.0 over Ethernet added.	V1.0 (S1 Agile) or later	P34x/EN M/Ia7

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
38 Cont.	B	M/P	✓ March 2014	✓ 16 PSL counters added. ✓ PSL Timer time delay settable in PSL or Settings. ✓ Power protection enhancements. ✓ Number of stages of 3 phase Power protection has been increased from 2 to 4. Can select as Active Power and new Reactive Power mode. Operation modes simplified - Forward/Reverse and Under/Over. Minimum setting reduced to approx 0.2%Sn. Single phase Sensitive Power has the same changes. Also includes new option to select the phase A or B or C. P345 Sensitive Power has 2 setting options 1 phase or new wattmetric power which uses 2 sensitive current inputs. ✓ Field failure protection has increased setting range for diameter and offset of the mho impedance characteristic. New directional line which can be used to block the mho characteristics in PSL. ✓ Independent voltage dependent overcurrent (51V) and underimpedance protection (21). Previously, only 51V or 21 could be enabled, now both can be enabled. ✓ 3rd stage undervoltage protection (V<3) added. ✓ Underimpedance setting range increased. 'Z<1/2 Setting' maximum value increased to 500/InΩ (Vn=100/120V). ✓ Overcurrent definite time setting range increased. 'I>1/2/3/4 Time Delay' maximum value increased to 200s. ✓ Overfrequency definite time setting range increased. 'F<1/2/3/4 Time Delay' maximum value is increased to 20000s.	V1.0 (S1 Agile) or later	P34x/EN M/la7

Relay type: P342/3/4/5/6/8 …						
Software version		**Hardware suffix**	**Original date of issue**	**Description of changes**	**S1 compatibility**	**Technical documentation**
Major	Minor					
38 Cont.	B	M/P	March 2014	✓ 3rd harmonic 100% stator earth fault under/over voltage minimum setting (100% St EF VN3H> and 100% St EF VN3H<) reduced to 0.1 V (Vn=100/120 V). ✓ Check synchronising phase angle setting range increased. 'CS1 Phase Angle' and 'CS2 Phase Angle' maximum value increased from 90 to 175 degree. ✓ User programmable curves added for overcurrent, earth fault, sensitive earth fault, under/overvoltage, neutral overvoltage and V/Hz protection. ✓ Disturbance record analogue channels increased to a maximum of 20 channels. ✓ Bug fixes added as 36 software. ✓ Minor bug fixes.	V1.0 (S1 Agile) or later	P34x/EN M/Ia7
	C	P/M	May 2014	✓ Corrected issue where relay will generate a Maint Record from PSL settable counter feature after downloading the firmware. ✓ Minor bug fixes.	V 1.0 (S1 Agile) or later	P34x/EN M/Ia7
	D	P/M	Feb 2016	✓ Corrected issue where the Timer Block DDBs for each of the 4 stages of under frequency protection do not work. ✓ Minor bug fixes.	V 1.0 (S1 Agile) or later	P34x/EN M/Ia8

| Setting File Software Version | Relay Software Version | | |

PSL File Software Version	Relay Software Version																								
		01	02	03	04	05	06	07	30	31	32 A-B	32 C-H	32 J-L	33	35	36	38								
	01	✓	✓	✓	✓	×	×	×	×	×	×	×	×	×	×	×	×								
	02	×	✓	✓	✓	×	×	×	×	×	×	×	×	×	×	×	×								
	03	×	×	✓	✓	×	×	×	×	×	×	×	×	×	×	×	×								
	04	×	×	×	✓	×	×	×	×	×	×	×	×	×	×	×	×								
	05	×	×	×	×	✓	✓	✓	×	×	×	×	×	×	×	×	×								
	06	×	×	×	×	✓	✓	✓	×	×	×	×	×	×	×	×	×								
	07	×	×	×	×	×	×	✓	×	×	×	×	×	×	×	×	×								
	30	×	×	×	×	×	×	×	✓	✓	×	×	×	×	×	×	×								
	31	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×	×								
	32A-B	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×								
	32C-H	×	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×								
	32J-L	×	×	×	×	×	×	×	×	×	×	×	✓	×	×	×	×								
	33	×	×	×	×	×	×	×	×	×	×	×	×	✓	✓	×	×								
	35	×	×	×	×	×	×	×	×	×	×	×	×	×	✓	×	×								
	36	×	×	×	×	×	×	×	×	×	×	×	×	×	×	✓	✓								
	38	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	✓								

Note 1: 05, 06 PSL compatible with 07 PSL except for user alarm DDBs. P345 PSL/Software compatibility is 32 A-E and F-L.

Menu Text File Software Version	Relay Software Version																						
	01	02	03	04	05 A-E	05 F-J	05K	06 A-E	06F	07 A-E	07F	30	31	32 A-B	32 C-D	32 E-L	33	35	36	38			
01	✓	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×			
02	×	✓	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×			
03	×	×	✓	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×			
04	×	×	×	✓	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×			
05A-E	×	×	×	×	✓	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×			
05F-J	×	×	×	×	×	✓	×	×	×	×	×	×	×	×	×	×	×	×	×	×			
05K	×	×	×	×	×	×	✓	×	×	×	×	×	×	×	×	×	×	×	×	×			
06A-E	×	×	×	×	×	×	×	✓	×	×	×	×	×	×	×	×	×	×	×	×			
06F	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×	×	×	×	×	×			
07A-E	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×	×	×	×	×			
07F	×	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×	×	×	×			
30	×	×	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×	×	×			
31	×	×	×	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×	×			
32A-B	×	×	×	×	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×			
32C-D	×	×	×	×	×	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×			
32 E-L	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	✓	×	×	×	×			
33	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	✓	×	×	×			
35	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	✓	×	×			
36	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	✓	×			
38	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	✓			

Menu text remains compatible within each software version (except 05/06/07) but is NOT compatible across different versions.

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