CT Saturation Tolerance for 87L Applications

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Abstract — This paper is exploring requirements for the line current differential function (87L) with regards to the tolerance to current transformer (CT) saturation. Typically, requirements provided by the manufacturers or standards are to eliminate CT saturation completely by proper sizing of CTs, which is not always practical.

First, the general knowledge of CT fundamental and saturation is introduced, including CT circuit model, simulation model, AC saturation, DC saturation and factors driving CT into saturation. Then the impact of CT saturation on the line current differential function is explained in terms of mathematical deduction and simulation, where the effects of saturation caused by internal and external faults on 87L are examined.

Percentage differential elements have algorithms designed to tolerate CT errors including CT saturation. How to use these algorithms properly and how to estimate reliability of the differential during CT saturation conditions is not an easy task. Therefore, techniques that have been used or can be used in 87L to reduce CT requirement and improve relay security are discussed.

Most important, a practical analysis tool is presented for different applications, including breaker-and-a-half or ring configurations, to analyze reliability of 87L during CT saturation, evaluate the differential relay security, investigate the effect of adjusting 87L settings, choose the proper size of CT and examine the possibility of reducing CT requirement.

Index Terms — Line Current Differential Relay, CT Saturation Tolerance

I. CT FUNDAMENTALS

Current Transformer (CT) is defined as "An instrument transformer that is intended to have its primary winding connected in series with the conductor carrying the current to be measured or controlled" [1], and "instrument transformer in which the secondary current, under normal conditions of use, is substantially proportional to the primary current and differs in phase from it by an angle which is approximately zero for an appropriate direction of the connections" [2].

Apparently, a CT is like any other kind of transformer, which consists of two windings magnetically coupled by the flux in a saturable steel core. A time varying voltage applied to one winding produces magnetic flux in the core, which induces the voltage in the second winding to deliver the secondary current. The transformer draws an exciting current to keep the core excited [3]. Similarly, CT's experience copper losses, core losses, eddy current losses and leakage flux. So the secondary current of a CT is not a perfectly true replica of the primary current in magnitude and there may exist a small phase shift.

Since AC voltage is time varying, the flux, the exciting current, the voltage and current induced in the second winding are also time varying. For transformers, it is common to use a hysteresis loop to relate the flux in the core to the exciting current, as illustrated in Figure 1. During the normal load condition, the exciting current is very small and non-sinusoidal.

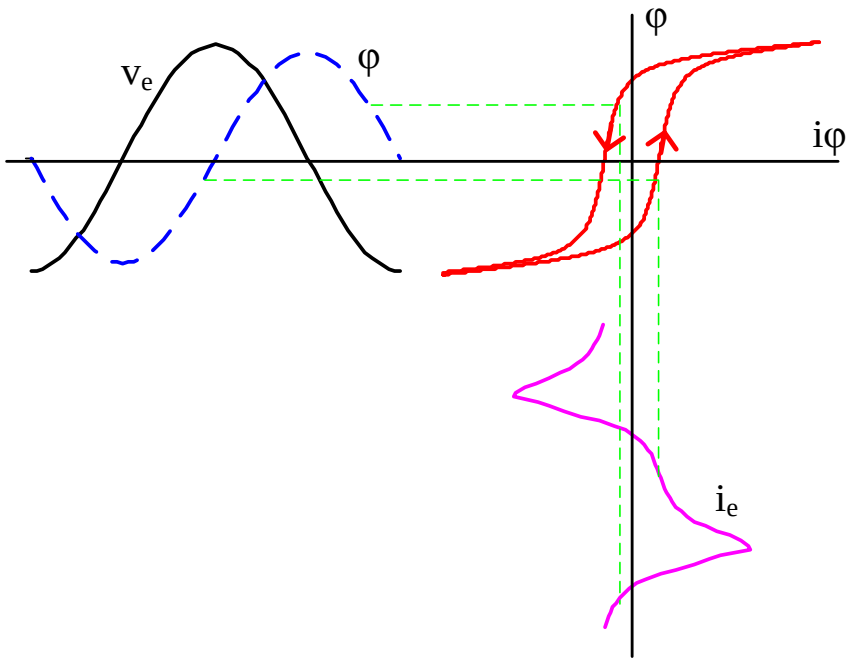


Figure 1. Relation of flux and exciting current in CT

A. Electrical circuit model

A current transformer is simply a transformer designed for the specific application of converting primary current to a secondary current for measurement, protection and control purposes. The actual performance of a CT, and the equivalent circuit model used for analysis purposes, are identical to that of any other transformer, as illustrated in Figure 2.

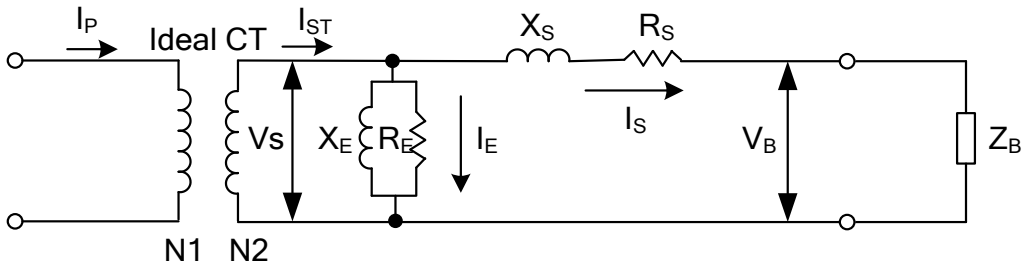


Figure 2. CT equivalent circuit model

V_S is the secondary CT exciting voltage, V_B is the CT terminal voltage across external burden, I_P is the primary current, I_{ST} is the total secondary current, I_S is the secondary load current, I_E is exciting current, R_E is the exciting resistance (negligible), X_E is the exciting reactance (nonlinear due to nonlinear magnetization process, negligible during complete saturation or 100-10000 ohms), R_S is the secondary resistance, X_S is the leakage reactance (negligible in Class C CTs) [4], Z_B is the burden impedance (including secondary devices and leads), and *N2/N1* is the CT turns ratio.

Besides the hysteresis curve shown in Figure 1, the CT secondary excitation characteristics curve is a more practical way to represent the CT steady-state performance, which is normally provided by manufacturers and can be easily verified during field tests. The excitation curve maps the relationship between the root-mean-square (rms) value of the secondary exciting voltage (V_S) and the rms value of the secondary exciting current (I_E). The Figure 3 shows a 2500:5A CT excitation characteristic obtained during a field test.

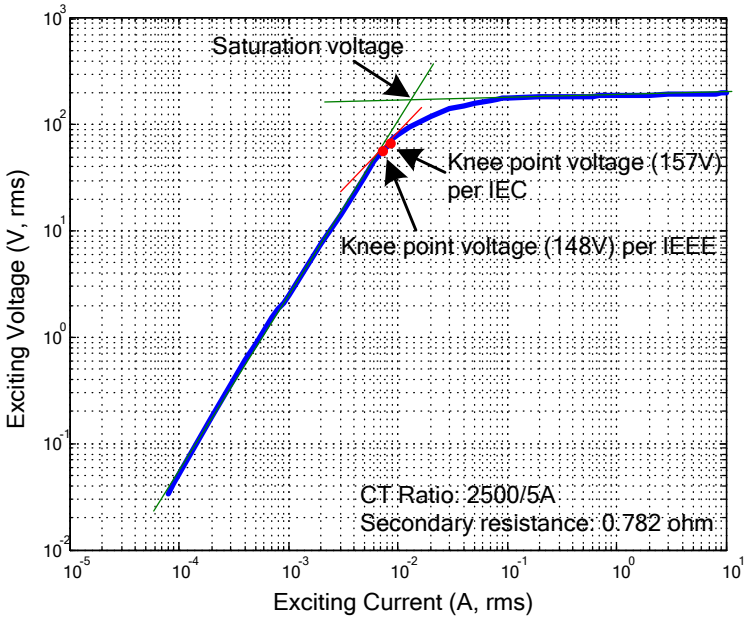


Figure 3. A CT secondary excitation characteristics obtained from the test

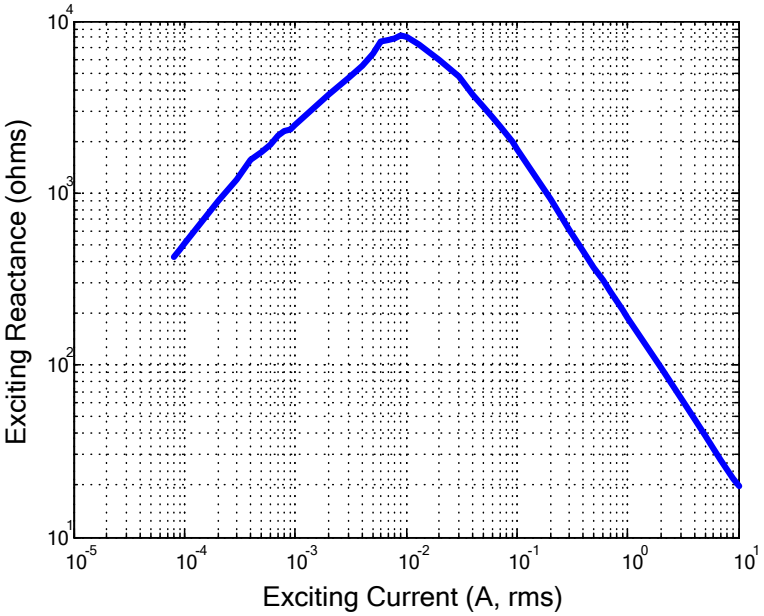


Figure 4. Exciting reactance calculated from the excitation curve in Figure 3

In IEEE C37.110-2007 standard, the knee point voltage is defined as the point in the curve where a 45 degree line drawn tangent to the abscissa. The knee-point is not the point of saturation. The saturation voltage is graphically located by the cross point of the straight lines of the excitation curve [1]. In IEC 61869-2 standard, the knee point voltage is defined as the voltage applied to the secondary terminals of the transformer, which, when increased by 10%, will result in the rms value of the exciting current to increase by 50% [2].

The steady state exciting reactance (X_E) can also be calculated from the excitation curve and its nonlinearity is illustrated in Figure 4.

Considering the same 2500:5A CT, the relation between true and ideal secondary currents is shown in Figure 5, where true secondary current would experience saturation under the higher fault current or larger CT burden. The ideal secondary current is equal to the primary current divided by the CT ratio.

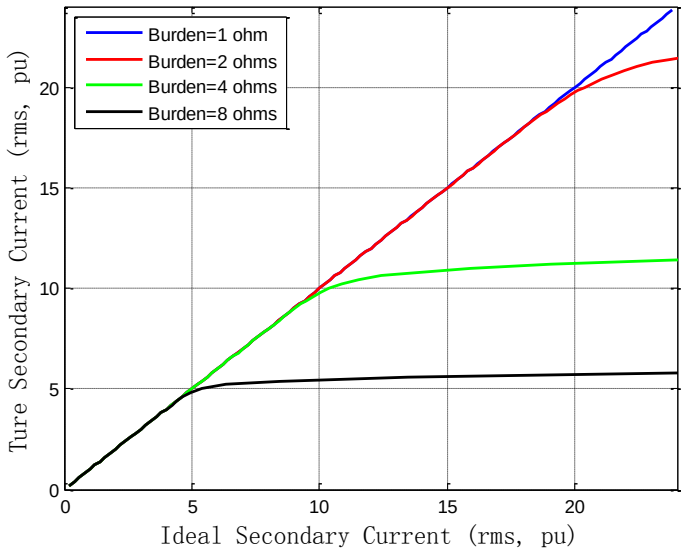


Figure 5. Ideal and true secondary currents

B. Computer simulation models

Many techniques have been proposed to model the behavior of iron-cored current transformers used for protective relaying purposes [5]. Many power system transient simulation tools provide the CT components to simulate fault transient for relay studies.

Electromagnetic Transient Program (EMTP) provides three nonlinear CT models, a true nonlinear model (Type-93) and two pseudo-nonlinear models (Type-96 and Type-98) [6]. The performance of the CT models has been experimentally evaluated, and the comparison indicates that CT models in EMTP give the satisfactory results for most of the cases [7].

Electromagnetic Transients including DC (EMTDC) program provides a Lucas model [8], and a model based on the Jiles-Atherton theory of ferromagnetic hysteresis [9].

The IEEE Power System Relaying Committee (PSRC) points out that "the excitation current in the region below the knee-point is a complex combination of magnetizing, hysteresis and eddy-current components, the parameters of which are usually not known in a particular case" [10]. A simplified CT mode is then proposed based on the assumption of the single-valued saturation curve, where the portion of waveform in the below-knee-point region has been ignored due to its negligible effect on the overall solution if exciting current enters into the saturated region.

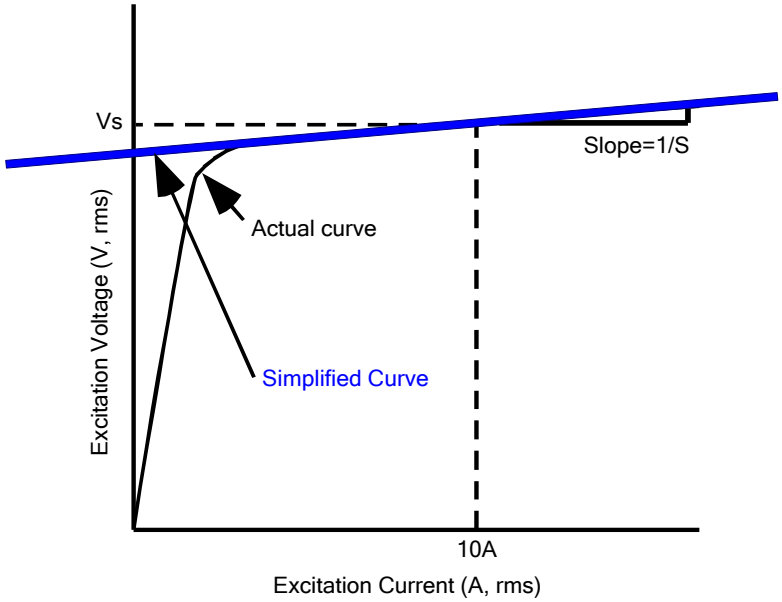


Figure 6. Simplified CT model - PSRC

The secondary current is calculated by the following equations,

$$i_s(t) = i_{st}(t) - i_e(t) \tag{1}$$

$$i_{st}(t) = \frac{i_p(t)}{N} \tag{2}$$

$$i_e(t) = \mathrm{sgn}(\lambda(t)) \bullet \frac{10\omega^S}{\left(\sqrt{2}V_S\right)^S RP} \bullet |\lambda(t)|^S \tag{3}$$

$$\lambda(t) = \lambda(t-1) + \Delta\lambda(t-1) \tag{4}$$

$$\Delta\lambda(t) = \frac{R_t i_s(t) + L_b \dfrac{di_s(t)}{dt} - R_t i_e(t)}{1 + L_b S |\lambda(t)|^{S-1} \dfrac{10\omega^S}{RP\left(\sqrt{2}V_S\right)^S}} \Delta t \tag{5}$$

$$RP = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \sin^{2S}(\omega t) dt} \tag{6}$$

where, i_s is the instantaneous secondary current, i_{st} is the instantaneous ideal secondary current, i_e is the instantaneous exciting current, i_p is the instantaneous primary current, N is the CT turn ratio, λ is the instantaneous flux linkage, $\omega = 2\pi f$, R_t is the total burden resistance, L_b is the burden inductance, S is the slope obtained from the excitation curve, V_s is the exciting voltage where the exciting current is equal to 10A, and Δt is the integration time step.

An Excel spreadsheet has been developed by the IEEE PSRC for the purpose of easy application [11].

This IEEE PSRC CT model has been verified by multiple parties [10] and validated in a high current laboratory [12]. The laboratory obtained saturated CT waveforms agreed to the IEEE PSRC CT model waveforms very closely. Therefore, this simplified CT model can be used for CT saturation modeling and is used in this paper as well.

II. CT SATURATION

When the exciting voltage is greater than the knee voltage in the excitation curve, the CT enters the saturated region, where the exciting current (I_E) is no longer negligible. Therefore, the ratio error ($I_E/I_S \times 100\%$) of the exciting current to the secondary current increases and the secondary current (I_S) is distorted, not being sinusoidal anymore.

A. AC saturation

AC saturation, also called steady state saturation, is caused by the symmetrical current with no DC component. A set of AC saturation examples is shown in the figure below.

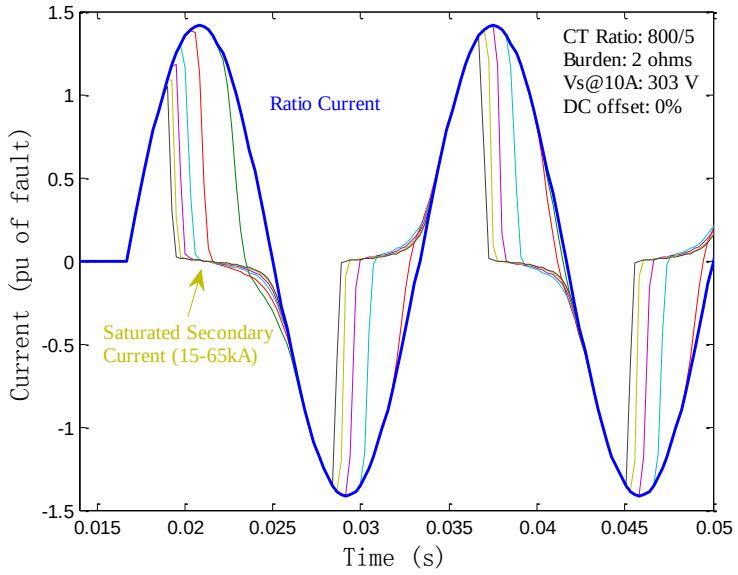


Figure 7. Examples of AC saturation

In order to avoid ac saturation, the secondary saturation voltage, V_X, must satisfy the following equation.

$$V_X > I_S \times Z_S \tag{7}$$

where, I_S is the primary current divided by the turns ratio, and Z_S is the total secondary burden (R_S + X_S + Z_B). It can be observed that the AC saturation may be caused by the higher primary current, lower ratio CT (such as ground CT), or larger CT burden (long lead length, and/or small AWG wire gage). Therefore, the AC saturation can be avoided by properly increasing the CT saturation voltage, CT ratio, or decreasing CT burden.

In real applications, a commonly used rule of thumb is to select a CT with the voltage rating of a Class C CT at least twice that required for the maximum steady state symmetrical fault current [1].

B. DC saturation

DC saturation, also called transient saturation, is commonly caused by the DC component in the fault current, unipolar half wave current or remnant flux in the CT. Once the transients decay enough or vanish so that the saturated region is not entered, the CT would get back to the steady state.

It is well known that the transient short-circuit current is defined by the following equation:

$$i(t) = \frac{\sqrt{2}E_P}{\sqrt{R^2 + (\omega L)^2}}\left[\sin(\omega t + \alpha - \theta) - \sin(\alpha - \theta)e^{-t/T_P}\right] \tag{8}$$

where, E_P is the system voltage, R is the system resistance, L is the system inductance, α is the fault inception angle, θ is the impedance angle, T_P is the time constant of the primary system. Considering the worst case condition where α-θ=90 °, the fault current contains the highest DC offset. A set of DC saturation examples caused by the fully DC offset is shown in the figure below.

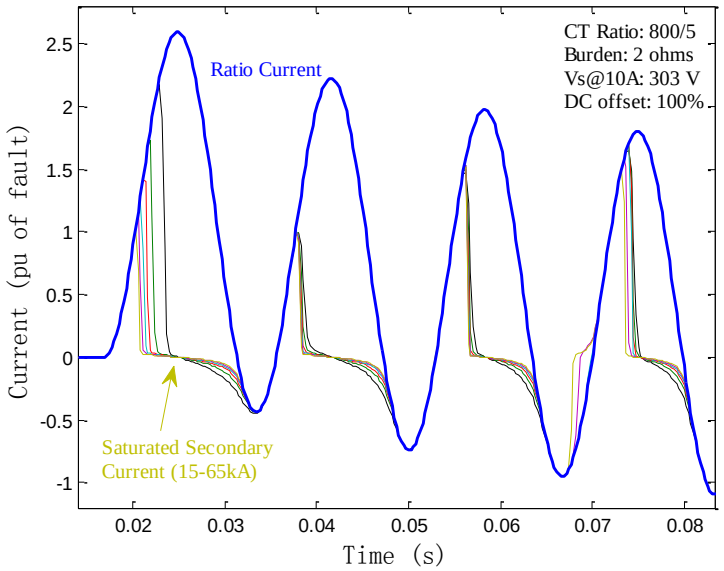


Figure 8. Examples of DC saturation

To avoid DC saturation (but ignoring effect of remanence), the required saturation voltage is given below,

$$V_X > I_S \times Z_S \times (1+\frac{X}{R}) \tag{9}$$

where, *X/R* is the primary system X/R ratio. Comparing Eq. (7) with Eq. (9), it can be found that the knee point voltage to avoid dc saturation must be *(1+X/R)* times that required for avoiding AC saturation.

C. Time to saturation

Because current in an inductance cannot change instantaneously, CT's take time to saturate. This is an important factor in the design and application of protective relays. For example if a relay uses digital signal processing to adjust the security of a protective function after CT saturation has been detected, the relay must have an adequate number of samples prior to saturation in order to make this determination.

An IEEE report [13] gives the detailed discussion and curves from which the time to saturation can be estimated. The IEEE standard [1] gives a conservative equation to estimate the time to saturation.

$$T_S = -T_1 \ln\left[1-\frac{V_X - I_S(R_S+R_B)}{\omega T_1 (I_S(R_S+R_B))}\right] \tag{10}$$

where, T_S is the time to saturation, T_1 is the primary system time constant, V_X is the saturation voltage, I_S is the primary current divided by the turns ratio, R_S is the secondary winding resistance, and R_B is the burden resistance.

A more detailed equation is described in [14], where the dc offset and percent remanence are included.

$$T_S = -T_1 \ln\left\{1-\frac{T_2 - T_1}{\omega T_2 T_1}\left[\frac{(1-percent\ remanence)V_x}{(pu\ offset)\ I_S(R_S+R_B)} - \frac{1}{\cos\varphi}\right]\right\} \tag{11}$$

where, T_2 is the secondary system time constant, and $cos\varphi$ is the secondary power factor.

D. Contributing factors to CT saturation

Regarding a specified CT, mostly, there are four factors which contribute to CT saturation:

- High primary fault current
- Excessive secondary burden
- Heavy DC offset in current
- Large percent remanence

Apparently, the increase in primary fault current will increase secondary current, sequentially, increase exciting voltage, enter into the saturated region and significantly increase exciting

current. As a result, the secondary current is greatly reduced and distorted. Both Figure 7 and Figure 8 show the saturated secondary currents.

Larger CT burdens increase exciting voltage under the same fault current, and increase exciting current. Then CT is more likely to saturate.

As indicated by the analysis of Eq. (8), the maximum DC component of a fault occurs when the instantaneous voltage is zero. Then the DC component starts decaying according to the time constant of the primary power system. The larger time constant will result in the longer decaying process, and then longer CT saturation period.

Remanence, also called remanent flux or residual flux, is the magnetic flux that is retained in the magnetic circuit after the removal of the excitation. Remanence may remain in either positive or negative direction. When the CT is subject to subsequent fault current again, the flux changes will start from the remanent value. Then the shifted remanence may worsen the transient response by pushing the core into deeper saturation within shorter time if the remanence and instantaneous flux have the same direction, or improve the transient response by keeping the core away from the deeper saturation if the remanence and instantaneous flux have the opposite direction.

III. IMPACT OF CT SATURATON ON 87L

The Eq. (9) describes the criterion of sizing CT to avoid DC saturation. However, it is not always practical or possible to satisfy for different applications. In practice, it is rarely possible to completely prevent the occurring of CT saturation for different fault events.

The distorted secondary current caused by CT saturation would inevitably affect the performance of current-based protection elements, such as overcurrent, directional overcurrent, distance, differential and others. The performance requirements of CT for various protection applications have been introduced in [15], [16]. This section will discuss the impact of CT saturation on line current differential relays.

A. Effect on current phasor estimation

Most of current-based protection functions are using the current phasor. This section will discuss the effect of CT saturation on one of mostly used phasor estimation techniques, Discrete Fourier Transform (DFT). It should be mentioned that in the real implementation of relays, some filtering techniques may be applied to remove DC decaying transients, or the cosine filter can be used for phasor estimation, however, these techniques are not considered in this paper.

The phasor of the secondary current is calculated by DFT as below,

$$\begin{aligned} I_S &= \frac{2}{NC}\sum_{p=0}^{NC-1} i_S \cdot e^{-i2\pi(p+0.5)/NC} \\ &= \frac{2}{NC}\sum_{p=0}^{NC-1} (i_{ST} - i_E) \cdot e^{-i2\pi(p+0.5)/NC} \\ &= \frac{2}{NC}\sum_{p=0}^{NC-1} i_{ST} \cdot e^{-i2\pi(p+0.5)/NC} - \frac{2}{NC}\sum_{p=0}^{NC-1} i_E \cdot e^{-i2\pi(p+0.5)/NC} \end{aligned} \quad (12)$$

$$= I_{ST} - \frac{2}{NC}\sum_{p=0}^{NC-1} i_E \cdot e^{-i2\pi(p+0.5)/NC}$$
$$= I_{ST} - I_E$$

where, I_S, I_{ST} and I_E are the phasors of the true secondary current, ideal secondary current and exciting current, i_S, i_{ST} and i_E are the instantaneous currents, NC is the amount of samples per cycle.

It can be found that an error exists between true and ideal current phasors caused by the exciting current (i_E). Since there are many factors affecting the saturation process and the exciting current is a quite nonlinear quantity, it is hard to give an accurate and definite analysis based on the Eq. (12). Therefore, some assumptions are applied for further analysis,

- Without saturation, the true and ideal currents have the exact same samples.
- During saturation, the true current samples are zero.
- Saturation is repeated each half cycle with the same pattern.
- There is no dc offset.
- The time to saturation longer than half cycle is not considered since the differential relays normally operate at the high speed.

An example of saturated current with assumptions is shown below, where the time to saturation is around 2.86 ms at 60 Hz.

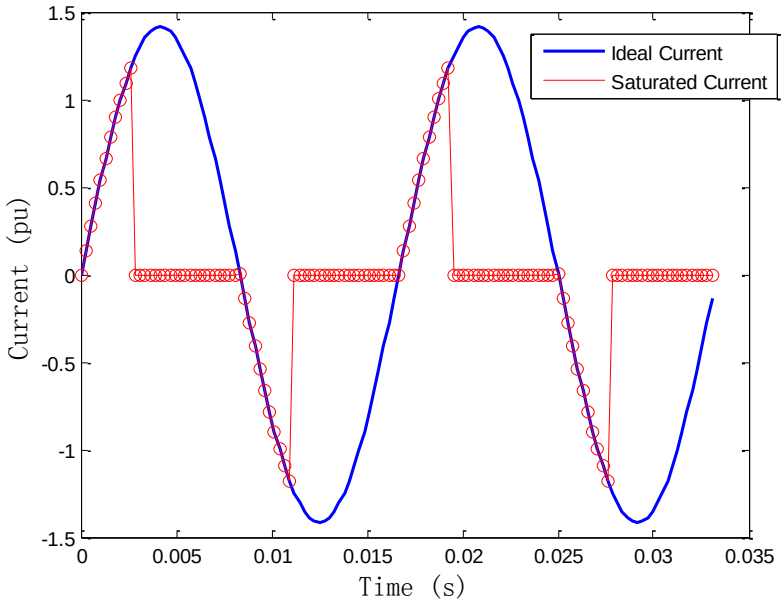


Figure 9. Example of simplified saturated current

Applying DFT to the saturated and ideal currents shown in the above figure, the magnitude and angle of phasors are shown in Figure 10.

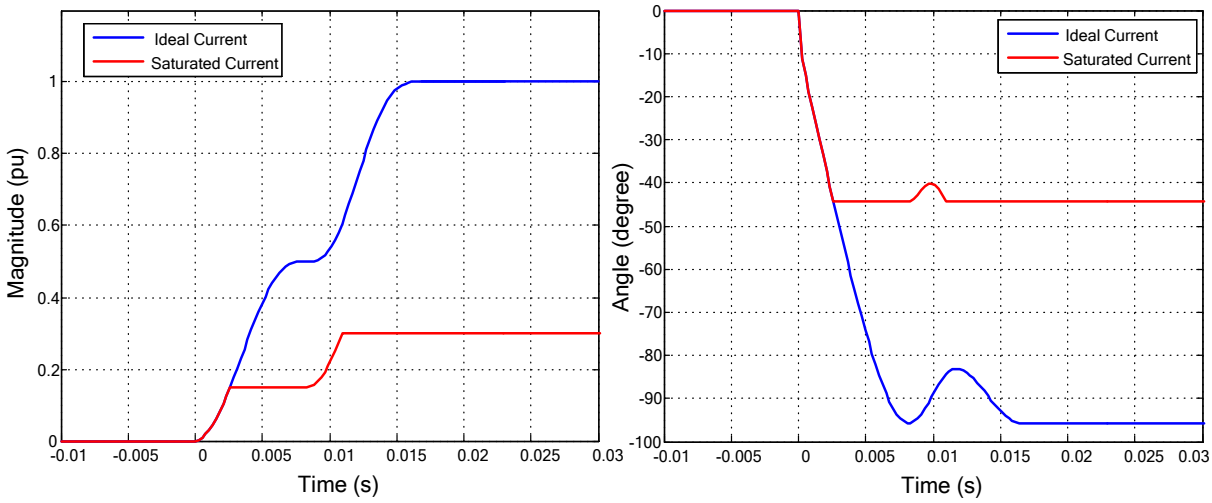


Figure 10. Magnitude and angle of currents in Figure 9

Then, the time to saturation is adjusted from 0 to 0.5 cycle, exclusively. After applying DFT analysis for each scenario, the fraction of the ideal rms and magnitude, and the angle shift from ideal are illustrated in Figure 11.

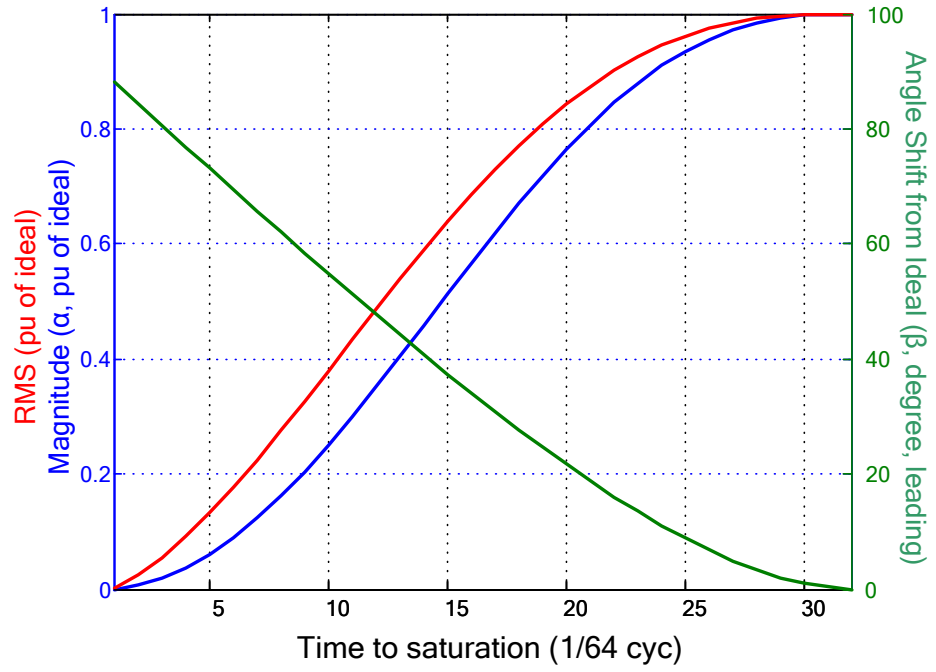


Figure 11. RMS, magnitude and angle shift of saturated currents

It can be concluded that:

- Both rms and fundamental magnitude will decrease under saturation. The deeper saturation, the larger decrease.

- The rms is always higher than the fundamental magnitude under the same saturation since the harmonics are considered in the rms value.
- The angle is becoming leading. The deeper saturation, the larger leading angle. The maximum angle shift is 88 degree leading in Figure 11 and the worst case shall be normally less than 90 degree.

It should be mentioned as well that in real cases, the saturation process is quite dynamic; as a result, both the magnitude and angle are changing dynamically through the fault as shown in the following figures.

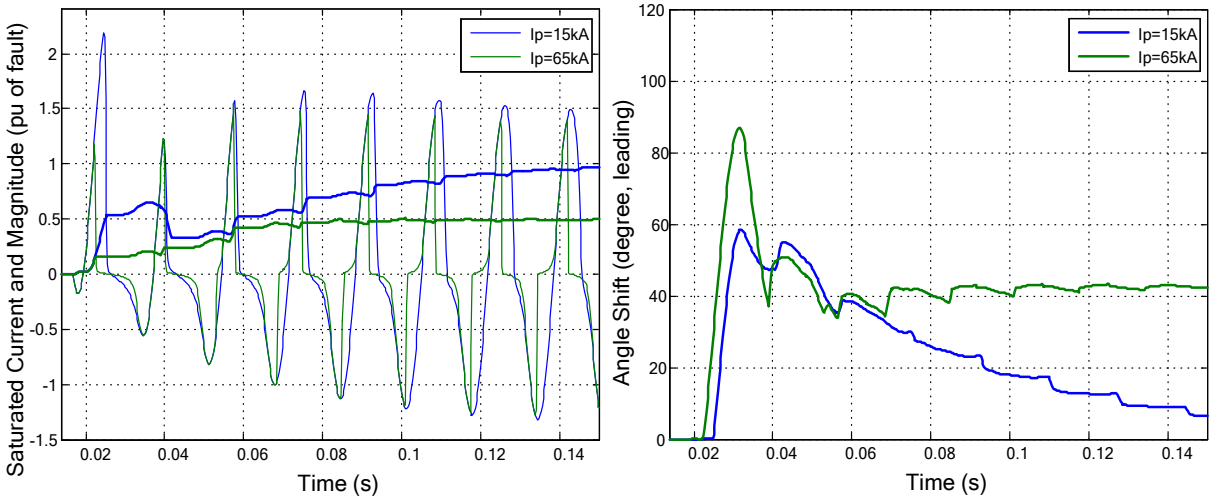


Figure 12. Fundamental magnitude and angle shift of two saturated currents

B. Effect on 87L

Using the result in Figure 11, the phasor of the saturated current can be expressed as,

$$I_{SAT} = \alpha(t_{SAT}) I_{IDEAL} \angle \beta(t_{SAT}) \tag{13}$$

where, I_{SAT} is the phasor of the saturated current, I_{IDEAL} is the magnitude of the ideal current, t_{SAT} is the time to saturation, the magnitude reducing factor α is expressed as a function of t_{SAT}, and the angle advancing factor β is also expressed as a function of t_{SAT}. The angle of the ideal current is assumed to zero.

The functions $\alpha(t_{SAT})$ and $\beta(t_{SAT})$ can be approximated by the three-order and two-order Fourier series respectively as below,

$$\begin{aligned} \alpha(t_{SAT}) = {} & 0.916 - 0.6565 \cdot \cos(4.324 t_{SAT}) - 0.3429 \cdot \sin(4.324 t_{SAT}) \\ & - 0.3008 \cdot \cos(8.648 t_{SAT}) + 0.1621 \cdot \sin(8.648 t_{SAT}) \\ & + 0.04234 \cdot \cos(12.972 t_{SAT}) - 0.01394 \cdot \sin(12.972 t_{SAT}) \\ & t_{SAT} \in (0,\ 0.5)\ cycle \end{aligned} \tag{14}$$

$$\begin{aligned}\beta(t_{SAT}) = 61.55 + 36.52 \cdot \cos(4.733 t_{SAT}) - 49.84 \cdot \sin(4.733 t_{SAT}) \\ - 6.392 \cdot \cos(9.466 t_{SAT}) + 0.4704 \cdot \sin(9.466 t_{SAT}) \\ t_{SAT} \in (0,\ 0.5)\ cycle\end{aligned} \tag{15}$$

Considering a traditional dual slope percentage differential scheme, the differential (operating) signal for an N-terminal line is defined as,

$$I_{DIFF} = |I_1 + I_2 + ... I_N| \tag{16}$$

The restraint signal is given as,

$$I_{RES} = |I_1| + |I_2| + ... + |I_N| \tag{17}$$

The operating conditions are the differential signal exceeds a constant pickup level,

$$I_{DIFF} > PKP \tag{18}$$

and exceeds a percentage of the restraining signal,

$$\begin{aligned}&I_{DIFF} > SLP1 * I_{RES},\ when\ I_{RES} \le BP,\ or \\ &I_{DIFF} > SLP2 * I_{RES} + (SLP1 - SLP2) \cdot BP,\ otherwise\end{aligned} \tag{19}$$

where, *SLP1* and *SLP2* are the slope rate of slope 1 and 2, and *BP* is the break point.

The effects of saturated currents caused by internal and external faults will be discussed in this section.

1) Saturation caused by internal faults

Considering a two-terminal line with internal faults, the local CT has no saturation and the fault current phasor is $I_P \angle \theta_L$, where, I_P is the fault current magnitude and θ_L is the impedance angle. The remote CT experiences saturation and the current phasor is $\alpha(t_{SAT}) K I_P \angle(\beta(t_{SAT}) + \gamma + \theta_L)$, where, γ is an angle difference tolerance factor to accommodate angle error, and K is a magnitude difference tolerance factor to accommodate,

- Different fault current level at the remote end
- Different CT performance between CTs located at two terminals
- Model difference between simplified saturation and real saturation
- Other errors caused by DC offset, asymmetrical saturation, etc.

Since θ_L has no effect on the differential calculation, it can be ignored, and then the local and remote current phasors are expressed as,

$$\begin{aligned}&I_L = I_P \\ &I_R = \alpha(t_{SAT}) K I_P \angle(\beta(t_{SAT}) + \gamma)\end{aligned} \tag{20}$$

The differential current is then given as,

$$\begin{aligned}I_{DIFF} &= |I_L + I_R| = |I_P + \alpha(t_{SAT}) K I_P \angle(\beta(t_{SAT}) + \gamma)| \\ &= I_P \cdot |1 + \alpha(t_{SAT}) K \angle(\beta(t_{SAT}) + \gamma)|\end{aligned} \tag{21}$$

The restraint current is given as,

$$\begin{aligned} I_{RES} &= |I_L| + |I_R| = I_P + \alpha(t_{SAT})KI_P \\ &= I_P \cdot (1 + \alpha(t_{SAT})K) \end{aligned} \tag{22}$$

In this scenario, I_P is normally greater than the break point *BP*, so the operating signal is determined by the following condition,

$$\frac{I_{DIFF}}{SLP2 \cdot I_{RES} + (SLP1 - SLP2) \cdot BP} > 1 \tag{23}$$

Because *(SLP1-SLP2)* is always less than 0, a more strict operating condition is given below,

$$\frac{I_{DIFF}}{SLP2 \cdot I_{RES}} > 1 \tag{24}$$

i.e.,

$$\frac{|1 + \alpha K \angle(\beta + \gamma)|}{SLP2 \cdot (1 + \alpha K)} = \frac{\sqrt{1 + 2\alpha K \cos(\beta + \gamma) + (\alpha K)^2}}{SLP2 \cdot (1 + \alpha K)} > 1 \tag{25}$$

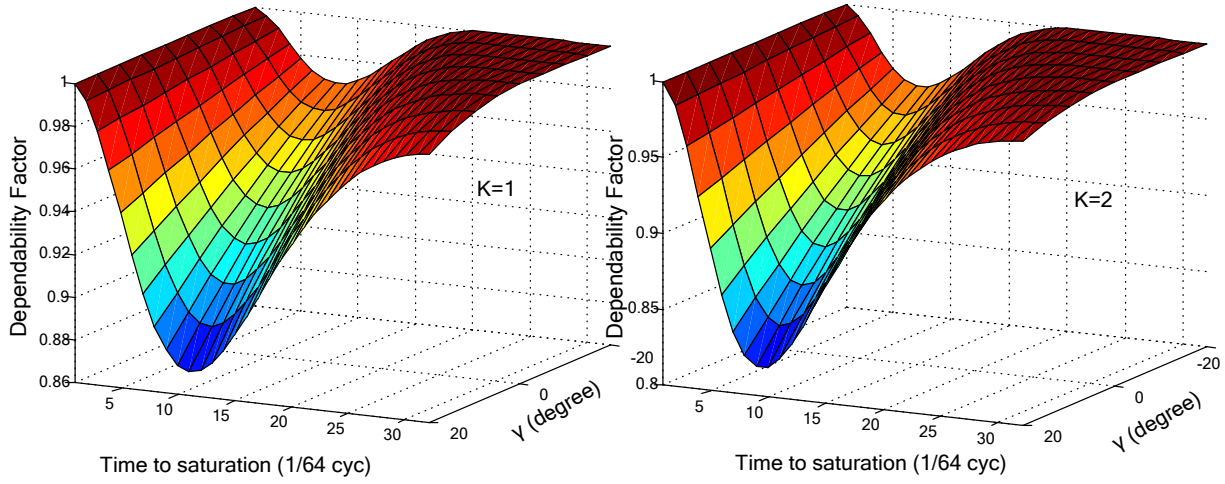
Furthermore, the above equation can be expressed as,

$$1 \geq \frac{\sqrt{1 + 2\alpha K \cos(\beta + \gamma) + (\alpha K)^2}}{(1 + \alpha K)} > SLP2 \tag{26}$$

Most important, the Dependability Factor (DF) is defined below to demonstrate the dependability of the differential function during internal faults,

$$DF = \frac{\sqrt{1 + 2\alpha K \cos(\beta + \gamma) + (\alpha K)^2}}{(1 + \alpha K)} \tag{27}$$

Using the approximation equations (14) and (15), the dependability factor with different *K* and γ is illustrated below.



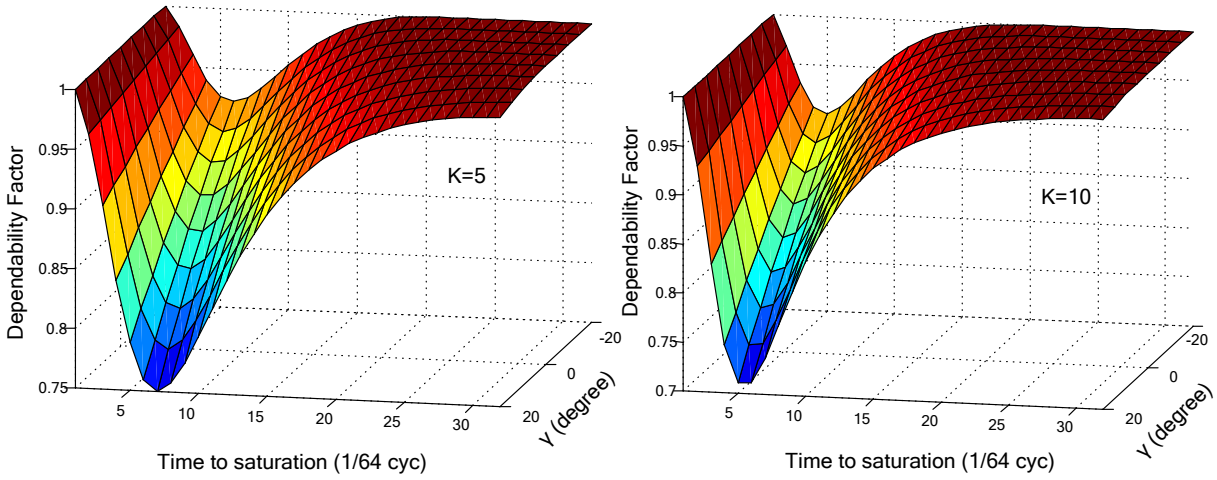


Figure 13. Dependability factor – internal faults

Observed from Figure 13, the 87L function would correctly operate on internal faults if the dependability factor is greater than 0.7, which also means the setting of *SLP2* shall be less than 0.7 according to Eq. (26). Actually in real applications, *SLP2* is normally set to a value less than 0.7

It can be concluded that the saturated currents caused by internal faults will rarely result in the failure to operate, if a proper restraint of the higher slope is set.

Even the above analysis and conclusion is based on the simplified saturated waveforms, they can still be applied for the real applications based on the following factors:

- Tolerance factors K and γ already accommodate the magnitude difference, magnitude error, and angle error.
- A more strict operating condition, Eq. (24), increases the restraint region and reduces the relay dependability in the analysis; fortunately, the higher slope in the traditional dual slope percentage plane would provide more dependability for the saturation caused by internal faults.

2) Saturation caused by external faults

Similarly, considering a two-terminal line with external faults closed to the remote end, the local CT has no saturation and the fault current phasor is $I_P\angle 0°$, where, I_P is the fault current magnitude. The remote CT experiences saturation and the current phasor is $\alpha(t_{SAT})KI_P\angle(\beta(t_{SAT})+\gamma+180°)$, where, K is a tolerance factor, which value is around 1, and γ is the angle error. The local and remote current phasors can be expressed as,

$$\begin{aligned} I_L &= I_P \\ I_R &= \alpha(t_{SAT})KI_P \angle(\beta(t_{SAT})+\gamma+180^\circ) \end{aligned} \tag{28}$$

The differential current is given as,

$$\begin{aligned} I_{DIFF} &= \left|I_L + I_R\right| = \left|I_P + \alpha(t_{SAT})KI_P \angle(\beta(t_{SAT}) + \gamma + 180^\circ)\right| \\ &= I_P \cdot \left|1 - \alpha(t_{SAT})K \angle(\beta(t_{SAT}) + \gamma)\right| \end{aligned} \tag{29}$$

The restraint current is given as,

$$\begin{aligned} I_{RES} &= \left|I_L\right| + \left|I_R\right| = I_P + \alpha(t_{SAT})KI_P \\ &= I_P \cdot \left(1 + \alpha(t_{SAT})K\right) \end{aligned} \tag{30}$$

In this scenario, I_P is normally greater than the break point *BP*, so the operating signal is determined by the following condition,

$$\frac{I_{DIFF}}{SLP2 \cdot I_{RES} + (SLP1 - SLP2) \cdot BP} > 1 \tag{31}$$

Increasing the security by removing the term, *(SLP1-SLP2)BP*,

$$\frac{I_{DIFF}}{SLP2 \cdot I_{RES}} > 1 \tag{32}$$

i.e.,

$$\frac{\left|1 - \alpha K \angle(\beta + \gamma)\right|}{SLP2 \cdot \left(1 + \alpha K\right)} = \frac{\sqrt{1 - 2\alpha K \cos(\beta + \gamma) + (\alpha K)^2}}{SLP2 \cdot \left(1 + \alpha K\right)} > 1 \tag{33}$$

Most important, the Security Factor (SF) is defined below to demonstrate the security of the differential function during external faults,

$$SF = \frac{\sqrt{1 - 2\alpha K \cos(\beta + \gamma) + (\alpha K)^2}}{\left(1 + \alpha K\right)} \tag{34}$$

Simply assuming $\gamma=0$, the security factor *SF* with different *K* is illustrated in Figure 14.

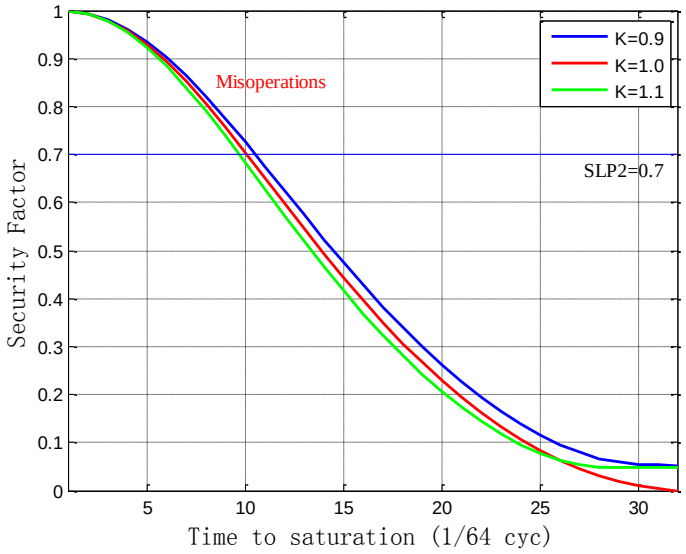


Figure 14. Security factor – external faults

It can be observed that there exists possibility of misoperation even though the 87L security has been increased by the Eq. (32). A similar result can be observed in the traditional percentage differential plane, the differential-restraint loci is shown in Figure 15, assuming *Ip=6 and 8 pu*, *K=1*, and *γ=0*.

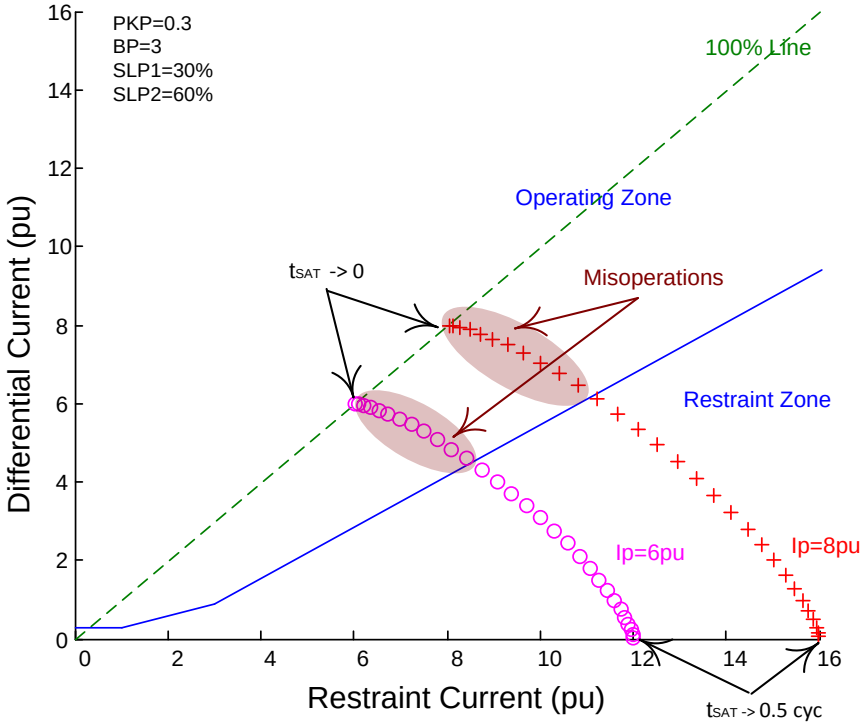


Figure 15. Differential characteristics – external faults

It can be concluded that CT saturation caused by external faults, particularly when it is more severe at one CT carrying the whole fault current in breaker-and-a-half applications or when CTs are different at opposite line terminals, introduces a spurious differential current that may cause the differential protection to misoperate.

IV. TECHNIQUES USED TO IMPROVE CT SATURATION TOLORENCE FOR 87L APPLICATIONS

It has been mentioned that it is not always practical to avoid CT saturation in real applications by using Equations (7) and (9) to size CT. Therefore, some techniques have to be applied in relays to deal with problems caused by CT saturation.

Based on the analysis in the previous section, protection engineers are mostly concerned with the techniques to increase the security during saturation caused by external faults.

External fault detectors are commonly applied in bus or transformer protection. These methods detect external faults before the occurrence of CT saturation to prevent relay misoperation on external faults.

Saturation detection techniques have been developed as well to block/unblock the operation of protection elements. These algorithms are slower than the external fault detectors that specially use sampled-based detection techniques, because saturation detectors would be asserted until the occurrence of CT saturation.

Some compensation methods have been proposed to reconstruct the distorted secondary current waveform caused by saturation conditions. Then, the reconstructed and undistorted waveform will be used for relay calculations. However, there still have some issues for real implementation, such as precision, speed and computation burden.

With respect to the application of current differential relays, one or more extra security measures listed below can be applied upon the detection the external fault.

- Add a portion of current distortions such as harmonics, saturated CT signal and noise, into the restraint signal; therefore, the restraint region is adaptively increased.
- Dynamically switch the differential settings to more secure values to deal with external faults. Normally, the more secure settings would result in the larger restraint region.
- Constantly use the transient bias as the additional restraint signal. An external fault or a sudden surge of the load current will cause a positive change (delta) in the restraint current, and then this delta signal is mixed into the transient bias to increase the restraint signal. If the delta signal vanished, the transient bias would start decaying exponentially.

A technique utilizing the adaptive restraint and CT saturation detection is explained below in details [17], [18].

The adaptive restraint characteristic dynamically adjusts the operating-restraint boundary which is the decision boundary between situations that are declared to be a fault and those that are not. The adaptive decision process is based on an on-line computation of the sources of measurement error. Sources of error include power system noise, transients, inaccuracy in line charging current computation, current sensor gain, phase and saturation error, clock error, and asynchronous sampling.

The relay computes the error caused by power system noise, CT saturation, harmonics, and transients. These errors arise because power system currents are not always exactly sinusoidal. The intensity of these errors varies with time; for example, growing during fault conditions, switching operations, or load variations. Current transformer saturation is included with noise and transient error. The measurement error, also called goodness of fit, is computed as a sum of squared differences between the actual waveform and an ideal sinusoid over one data window.

$$I^2_{LOC\_ADA\_A(k)} = \frac{4}{NC}\left(\frac{4}{NC} \sum_{p=0}^{NC/2-1} \left(i_{LOC\_A(k-p)}\right)^2 - I^2_{LOC\_MAG\_A} \right) \tag{35}$$

where, $I_{LOC\_ADA\_A}$ is the local phase A adaptive restraint term, NC is the amount of samples per cycle, i_{LOC_A} is the local phase A samples after the dc removal filtering, and $I_{LOC\_MAG\_A}$ is the local phase A magnitude.

A dedicated mechanism is applied in the line current differential relay to cope with CT saturation and ensure security of protection for external faults. The relay dynamically increases the weight of the adaptive restraint portion ($I_{LOC\_ADA\_A}$ in Eq. (35)) in the total restraint quantity, but for external faults only. The following logic is applied:

- First, the terminal currents are compared against a threshold of 3 pu to detect overcurrent conditions that may be caused by a fault and may lead to CT saturation.
- For all the terminal currents that are above the 3 pu level, the relative angle difference is calculated.
- Depending on the angle difference between the terminal currents, the adaptive restraint current is increased by the multiple factor of 1, 5, or 2.5 to 5 as shown in Figure 16. As seen from the figure, a factor of 1 is used for internal faults, and a factor of 2.5 to 5 is used for external faults. This allows the relay to be simultaneously sensitive for internal faults and robust for external faults with a possible CT saturation.
- If more than one CT is connected to the relay (breaker-and-the half applications), the CT saturation mechanism is executed between the maximum local current against the sum of all others, then between the maximum local and remote currents to select the secure multiplier *MULT*. A maximum of two (local and remote) is selected and then applied to adaptive restraint.

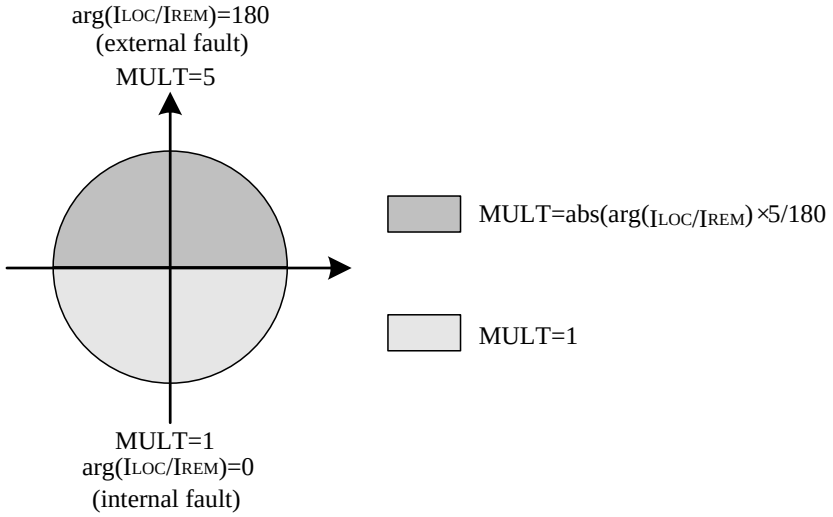


Figure 16. Adaptive restraint multiplier

MULT in the above figure denotes a multiplier that increases restraint if CT saturation is detected.

The final restraining current is calculated as a sum of squared local and all remote restraints (assuming two terminals here).

$$I_{RESTT\_A} = \sqrt{\left(I_{LOC\_RESTRAINT\_A}\right)^2 + \left(I_{REM\_RESTRAINT\_A}\right)^2}$$
$$I^2_{LOC\_RESTRAINT\_A} = \left(I_{LOC\_TRAD\_REST\_A}\right)^2 + MULT_{LOC\_A}\left(I_{LOC\_ADA\_A}\right)^2 \quad (36)$$
$$I^2_{REM\_RESTRAINT\_A} = \left(I_{REM\_TRAD\_REST\_A}\right)^2 + MULT_{REM\_A}\left(I_{REM\_ADA\_A}\right)^2$$

Where, I_{REST_A} is the final phase A restraint current, $I_{LOC\_RESTRAINT\_A}$ is the final local phase A restraint current, $I_{REM\_RESTRAINT\_A}$ is the final remote phase A restraint current, $I_{LOC\_TRAD\_REST\_A}$ is the traditional local phase A restraint current, $I_{REM\_TRAD\_REST\_A}$ is the traditional remote phase A restraint current, $MULT_{LOC\_A}$ is local phase A multiplier obtained from Figure 16, and $I_{LOC\_ADA\_A}$ is the local phase A adaptive restraint obtained from Eq. (35).

The Eq. (36) is based on the adaptive strategy. When the adaptive portion of the restraint current is small, the restraint region shrinks. When the adaptive portion of the restraint current increases, the restraint region grows to reflect the uncertainty of the measurement. Raising the restraint multiplier corresponds to demanding a greater confidence interval and has the effect of decreasing sensitivity, while lowering it is equivalent to relaxing the confidence interval and increases sensitivity. Thus, the restraint multiplier is an application adjustment that is used to achieve the desired balance between sensitivity and security.

V. A CT SATURATION ANALYSIS TOOL FOR 87L

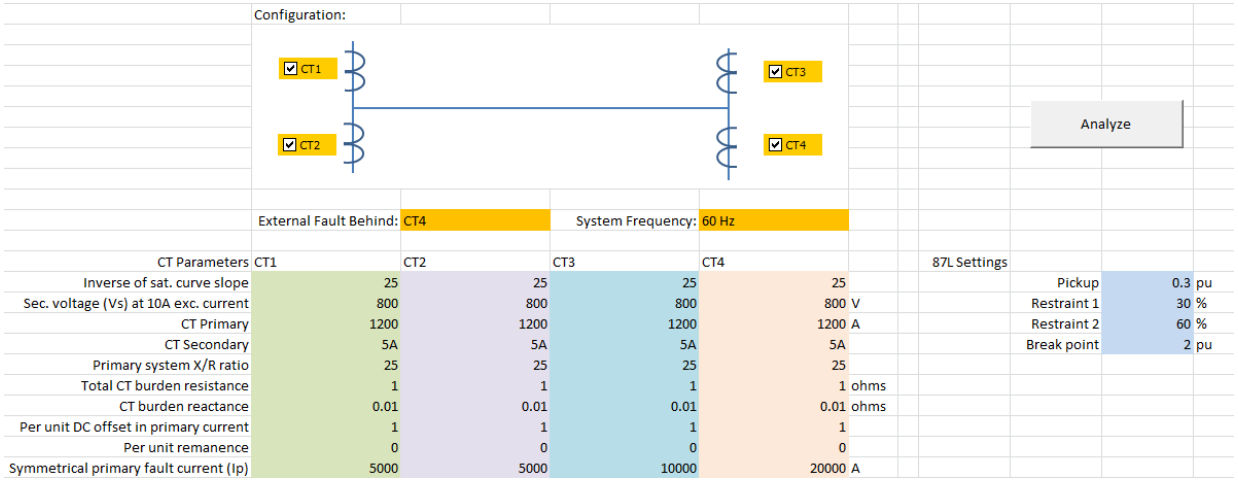
The questions were recently raised for the practicality of the IEEE (*1+X/R*) criteria, especially for applications with the low CT ratio but high fault current [19]. Ultimately, utility customers are looking for the relay manufacturer recommendations and warranties for the CT selection at their system with particular relay models. CT selection recommendations are different from one manufacturer to another and there cannot be any standard giving specific recommendations. It is possible to verify relay performance for a given application by modelling CTs with RTDS or any other simulation tools, but this is not always available to utility customer, is expensive and requires lot of efforts and time.

Regarding responsibility of relay manufacturers, it has been particularly mentioned that “only the relay manufacturer knows the proprietary design of the protection relay; consequently, only the relay manufacturer can confirm the CT/relay system application” [20]. Besides relay algorithms, complexity arises from the fault current distribution in breaker-and-a-half applications, possible different CT ratios or even different CT characteristics in real life applications.

In order to analyze the line current differential relay reliability during CT saturation caused by an external fault, investigate the effect of adjusting 87L settings, choose the proper size of CT and examine possibility of reducing CT requirement, it is possible to develop a type of CT saturation analysis tool that is able to emulate the CTs and the relay behavior. The following description is an example of such a tool.

The tool utilizes the CT model and CT saturation calculation algorithm proposed by the IEEE PSRC, and simulates the analog/digital signal processing and data calculations exactly existing in

the line current differential relay. It seamlessly incorporates the CT performance and relay system application. The Figure 17 shows the example of the interface of such analysis tool.



CT Parameters	CT1	CT2	CT3	CT4		87L Settings		
Inverse of sat. curve slope	25	25	25	25		Pickup	0.3	pu
Sec. voltage (Vs) at 10A exc. current	800	800	800	800	V	Restraint 1	30	%
CT Primary	1200	1200	1200	1200	A	Restraint 2	60	%
CT Secondary	5A	5A	5A	5A		Break point	2	pu
Primary system X/R ratio	25	25	25	25				
Total CT burden resistance	1	1	1	1	ohms			
CT burden reactance	0.01	0.01	0.01	0.01	ohms			
Per unit DC offset in primary current	1	1	1	1				
Per unit remanence	0	0	0	0				
Symmetrical primary fault current (Ip)	5000	5000	10000	20000	A			

Figure 17. CT saturation analysis tool

For the system where the CTs are already installed, the CT and system parameters are known. The users can use the following procedure to analyze the reliability of the 87L relay during CT saturation and investigate the effect of adjusting 87L settings.

- Select the single CT or breaker-and-a-half configuration for each terminal. At least one CT shall be selected at each terminal. If only a single CT is applied in one terminal, check any one CT from that end.
- Specify the CT behind which the external fault is located.
- Choose the system frequency, 60Hz or 50Hz.
- Based on the datasheet provided by the CT manufacturer, input the CT parameters for each CT, including inverse of saturation curve slope, secondary voltage (Vs) at 10A exciting current, CT primary current, CT secondary current. The details can be referred to the IEEE PSRC documents [10] and [11].
- Determine the corresponding primary circuit X/R ratio.
- Calculate the total CT burden for each CT, including CT secondary winding resistance, loop lead resistance, and the relay burden at rated secondary current.
- Input the per-unit DC offset in primary current, normally set to 1 (100%) for the worst case analysis.
- Input the per-unit remanence, normally set to 0 for the selected CTs.
- Determine the maximum fault current supplied by each selected CT which is not closed to the external fault. The maximum fault current for the CT closed to the fault is the summation of currents flowing through all other CTs. These currents are in primary amperes.
- Set the 87L settings of a percentage differential characteristic, including pickup level, restraint slope 1, restraint slope 2, and break point.

- Click the Analyze button, then the CT secondary currents, differential current, restraint current and operate signal will be illustrated. An example is shown in Figure 18.
- Try different fault locations and fault distribution through all CTs.

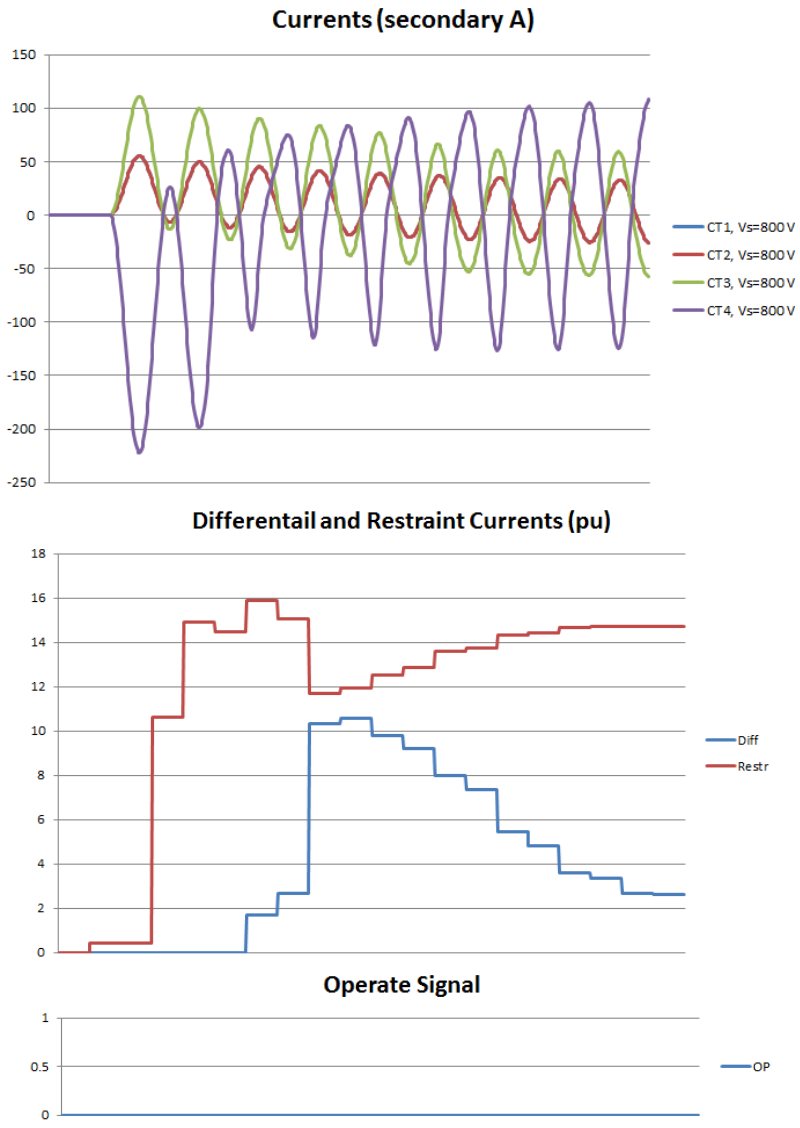


Figure 18. Analysis tool results

It should be noted that,

- Application is considered safe when $I_{restr}/I_{diff}>1.25$ with selected settings and all fault scenarios considered.
- Adjusting the 87L settings, especially *Restraint 2*, is helpful to increase the security during CT saturation caused by external faults.

In the case to size CTs, normally, CT primary and secondary currents can be pre-determined by some criteria, such as maximum load conditions. The inverse of saturation curve slope is

almost identical for the same CT model, so it can be calculated from the CT datasheet. Therefore, the users are mostly concerning the selection of V_S value. The following procedure can be used.

- Set V_S to zero and use the approximate CT secondary winding resistance (R_{CT}) for all the CTs to be sized.
- The tool will automatically examine the different V_S, starting from 3000V to 50V in steps of -50V. Once a misoperation is detected, the tool will stop calculation and give the boundary V_S.
- Select the CT having the maximum fault current or highest CT primary current, add a 120%~140% safety margin to the boundary V_S, find the true V_S and secondary winding resistance from the CT datasheet, and input these values into the tool for this CT only.
- Repeat the above step until all the CTs are sized.
- Try different fault locations and fault distribution through all CTs.

VI. EXPANSION TO OTHER PROTECTION FUNCTIONS

The presented CT saturation analysis tool is specially designed for the line current differential relay. Similarly, the CT saturation analysis tool can be designed for the other differential relays as well, such as bus, transformer, motor and generator. Additionally, this analysis mechanism can be expanded to other relay protection functions. Some examples are introduced below.

With respect to applications where relatively low-ratio CTs are applied for protective relaying of feeders carrying relatively small loads from switchgear and motor controllers with a high short-circuit capacity. Assuming that the load current is less than 50A, theoretically CTs rated as low as 50:5 with a protection class C10 may be applied for protection purposes. In the worst-case scenario, fault currents can be as high as 64kA which is 1080 times the rated current of the 50:5 CT. Therefore, CT subjected to a primary fault current hundreds of times its rated current will saturate severely - only relatively short duration peaks of limited current will be observed from the secondary of the CT. These peaks can be as low as 5-10% of the primary fault current divided by CT ratio (theoretically, saturation free) current and will last a small fraction of the half-cycle, down to 1-2ms in extreme cases. As a result, only a very small portion of the actual fault current is available to protective relays fed from such severely saturated CTs. In order to deal with such application, the CT saturation and overcurrent protection function needs to be modeled and the relay behavior during saturation can be analyzed. Accordingly, the input quantity (fundamental magnitude or rms value) and pickup setting of the overcurrent function can be properly selected based on the analysis result.

The low-ratio core balance CT (CBCT) feeding the differential current to the motor relay must be mounted in the motor line and neutral leads. The distance between the CBCT and the relay is typically quite large, ranging from several hundreds of meters to over 1000 meters. As a result, the effective burden resistance of the CBCT could be very different from the typical burden. Therefore, in order to ensure the sensitivity and dependability of the unbiased differential function in the motor relay, the effect of the cable resistance needs to be investigated and the behavior of the CBCT and differential function can be analyzed. Thereby, the pickup setting of the differential function can be properly set according to the analysis result.

VII. CONCLUSIONS

By analyzing and simulating the simplified saturation current waveforms on the percentage differential characteristic plane, it has been concluded that,

- The saturation caused by internal faults will rarely result in the failure to operate
- The saturation caused by external faults, particularly when it is more severe at one CT carrying the whole fault current in breaker-and-a-half applications or when CTs are different at opposite line terminals, introduces a spurious differential current that may cause the differential protection to misoperate.

The techniques that have been used in 87L to tolerate CT errors, reduce CT requirement and improve relay security are discussed. An adaptive restraint logic and CT saturation detection method is explained in details.

Seamlessly incorporating the CT performance and relay system application, a practical CT saturation analysis tool is presented to analyze reliability of 87L during CT saturation, evaluate the differential relay security, investigate the effect of adjusting 87L settings, choose the proper size of CT and examine the possibility of reducing CT requirement. This tool can also be applied for different applications, including breaker-and-a-half or ring configurations. Furthermore, the analysis mechanism is able to be expanded to the other relay functions (like overcurrent protection) and different applications (such as low ratio CT and high fault current for switchgears, etc.).

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IX. BIOGRAPHIES

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